IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

LIBERTY PATENTS LLC, Plaintiff, v. LATTICE SEMICONDUCTOR CORPORATION, Defendant.	CIVIL ACTION NO. 6:21-cv-692 ORIGINAL COMPLAINT FOR PATENT INFRINGEMENT **JURY TRIAL DEMANDED**

ORIGINAL COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Liberty Patents LLC ("Liberty Patents" or "Plaintiff") files this original complaint against Defendant Lattice Semiconductor Corporation ("Lattice" or "Defendant"), alleging, based on its own knowledge as to itself and its own actions and based on information and belief as to all other matters, as follows:

PARTIES

1. Liberty Patents is a limited liability company formed under the laws of the State of Texas, with its principal place of business at 2325 Oak Alley, Tyler, Texas, 75703.

2. Defendant Lattice Semiconductor Corporation is a corporation organized and existing under the laws of the state of Delaware. Lattice Semiconductor Corporation may be served with process through its registered agent, Corporation Service Company d/b/a/ CSC-Lawyers Incorporating Service Company at 211 East 7th Street, Suite 620, Austin, Texas, 78701-3218.

3. Lattice describes itself as a "global leader in smart connectivity solutions, providing market leading intellectual property and low-power, small form-factor devices that enable more than 8,000 global customers to quickly deliver innovative and differentiated cost

and power efficient products."[1] It is the world's largest volume supplier of FPGAs.[2] According to Lattice, "[a]n FPGA's parallel architecture enables faster processing than competing devices, such as microcontrollers, allowing for a user experience with shorter pauses and fewer delays."[3]

4. Further, Lattice states that its "FPGAs are among the lowest power consumption in the industry, enabling the application processor and other high-power components to remain dormant longer, resulting in longer battery life."[4] Lattice also states that it enables thinner end products than others in the industry.[5]

JURISDICTION AND VENUE

5. This is an action for infringement of a United States patent arising under 35 U.S.C. §§ 271, 281, and 284–85, among others. This Court has subject matter jurisdiction of the action under 28 U.S.C. § 1331 and § 1338(a).

6. This Court has personal jurisdiction over Lattice pursuant to due process and/or the Texas Long Arm Statute because, *inter alia*, (i) Lattice has done and continues to do business in Texas; (ii) Lattice has committed and continues to commit acts of patent infringement in the State of Texas, including making, using, offering to sell, and/or selling accused products in Texas, and/or importing accused products into Texas, including by Internet sales and/or sales via retail and wholesale stores, inducing others to commit acts of patent infringement in Texas,

[1] https://ir.latticesemi.com/

[2] https://ir.latticesemi.com/static-files/1a0364e1-427b-475e-a979-092577f59207.

[3] Lattice Semiconductor Corp. Form 10-K at 5 (2019), https://ir.latticesemi.com/static-files/845b07bb-eb8f-48ff-97ba-0bcdb2b4b563.

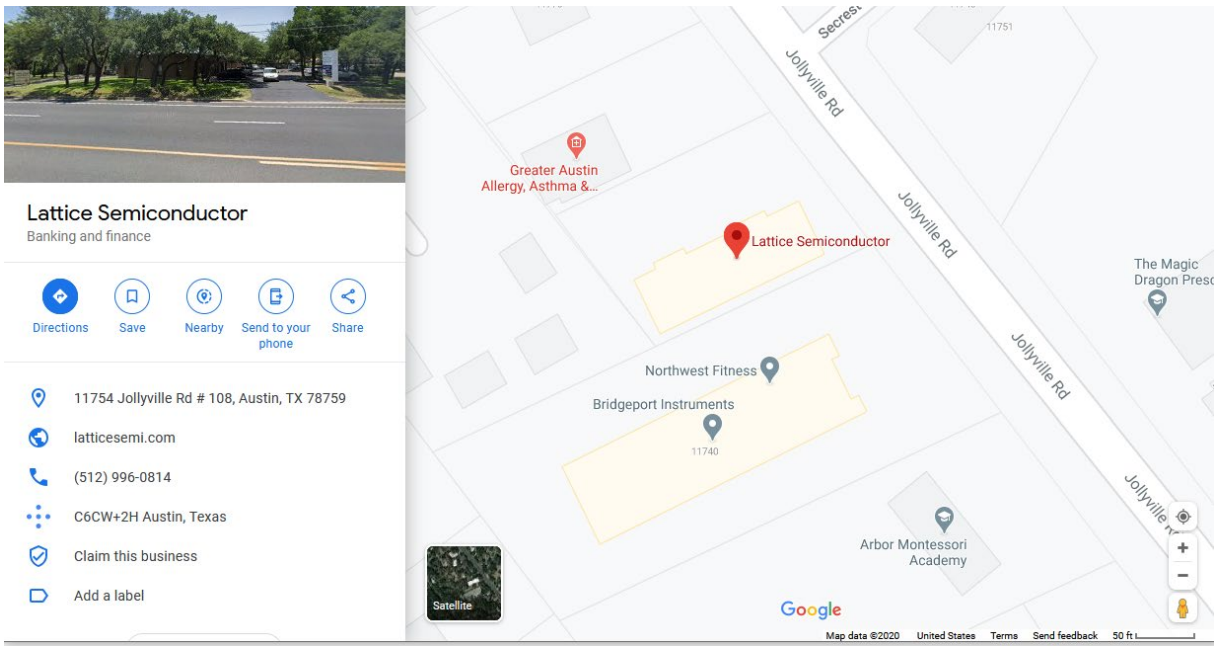
[4] *Id*.

[5] *Id*.

and/or committing at least a portion of any other infringements alleged herein in Texas, and (iii) Lattice is registered to do business in Texas.

7. Venue is proper in this district under 28 U.S.C. § 1400(b). Venue is further proper because Lattice has committed and continues to commit acts of patent infringement in this district, including making, using, offering to sell, and/or selling accused products in this district, and/or importing accused products into this district, including by Internet sales and/or sales via retail and wholesale stores, inducing others to commit acts of patent infringement in this district, and/or committing at least a portion of any other infringements alleged herein in this district.

8. Lattice also has a regular and established place of business in this district, including at least at 11754 Jollyville Rd., #108, Austin, Texas, 78759:



Source: https://goo.gl/maps/fSg65aoPYQMH8Boa9

BACKGROUND

9. The patents-in-suit generally relate to body biasing voltages used in integrated circuits (ICs). They teach application of body biasing techniques that improve circuit

performance and reduce power consumption in one or more power modes. Specifically, the patents-in-suit disclose systems and methods for generating body biasing voltages so that a processor can operate with increased power savings. For example, the patents-in-suit describe techniques for using body biasing voltages to decrease power consumption during high performance applications. Other examples disclose use of body biasing voltages during low-power modes.

10. The use of body biasing voltages in ICs has become an increasingly necessary design feature in many applications today. Coupled with the explosive demand for ICs over the last few years, the more stringent requirement that ICs consume less and less power has focused the industry towards using body biasing voltages. Body biasing voltage techniques are now being used in applications ranging from automotive technologies to industrial IoT devices. Whether an application requires high performance circuitry or ultra low-power modes (or both), body biasing techniques have become essential.

11. The technology described by the patents-in-suit was developed by engineers at Transmeta Corp. Transmeta was a technology company formed in 1995 and best known for designing high performance processors, such as the Crusoe and the Efficeon in the early 2000s. In particular, Transmeta's major focus was on developing low power, high performance ICs. To achieve such high power savings, one of the major techniques used by Transmeta engineers was to apply body biasing voltages to its ICs.

12. Industry experts have recognized the technological innovation of Transmeta's processors, and some have noted that Transmeta's energy-saving processors were ahead of their

time.[6] The inventions disclosed in the patents-in-suit are extremely important to multiple industries, and have been cited by major technology companies and processor developers like Canon, Freescale Semiconductor (now part of NXP), Nvidia, Packet Digital, and Smart Technologies (now part of Foxconn).

COUNT I

DIRECT INFRINGEMENT OF U.S. PATENT NO. 7,509,504

13. On March 24, 2009, U.S. Patent No. 7,509,504 ("the '504 Patent") was duly and legally issued by the United States Patent and Trademark Office for an invention entitled "Systems and Methods for Control of Integrated Circuits Comprising Body Biasing Systems."

14. Liberty Patents is the owner of the '504 Patent, with all substantive rights in and to that patent, including the sole and exclusive right to prosecute this action and enforce the '504 Patent against infringers, and to collect damages for all relevant times.

15. Lattice made, had made, used, imported, provided, supplied, distributed, sold, and/or offered for sale products and/or systems including, for example, Lattice's CrossLink-NX family of FPGA devices and other products[7] that are capable of applying body biasing voltages during a power mode of a processor or other integrated circuit ("accused products"):

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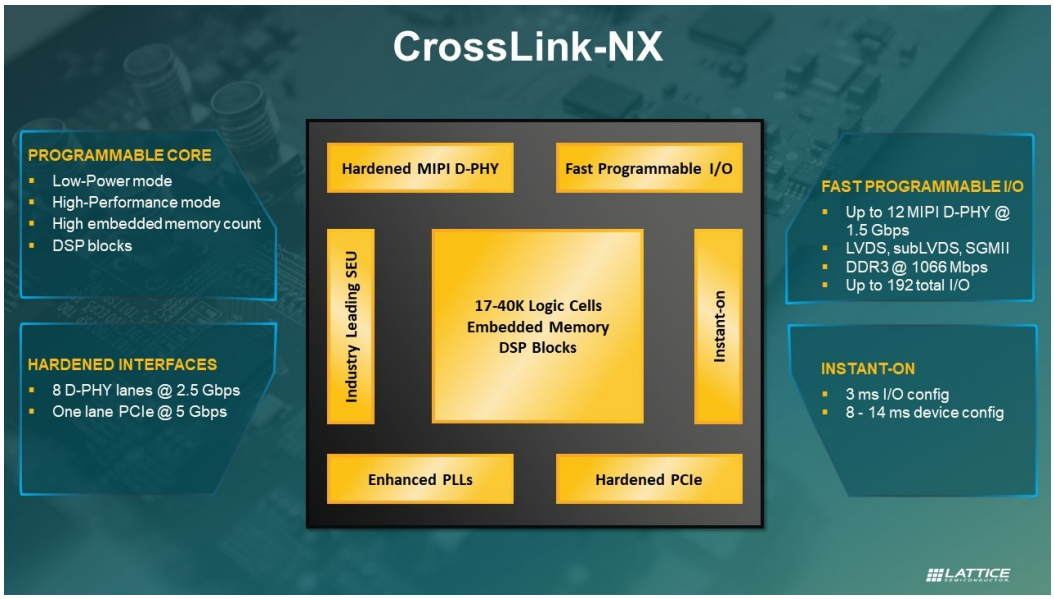
[6] *See, e.g.*, *Chip Hall of Fame: Transmeta Corp. Crusoe Processor*, IEEE Spectrum (June 30, 2017) ("Ahead of its time, this chip heralded the mobile era when energy use, not processing power, would become the most important spec."), https://spectrum.ieee.org/tech-history/silicon-revolution/chip-hall-of-fame-transmeta-corp-crusoe-processor.

[7] *See, e.g.*, Lattice LIFCL-40-7BG400C, LIFCL-40-9MG289C, LIFCL-40-7SG72CES, LIFCL-40-8SG72C, LIFCL-40-9BG256C, LIFCL-40-7MG121I, LIFCL-40-7BG400CES, LIFCL-40-7MG121CES, LIFCL-40-7SG72IES, LIFCL-40-8BG400C, LIFCL-40-8BG256C, LIFCL-40-8MG121C, LIFCL-40-7MG289I, LIFCL-40-8MG121I, LIFCL-40-8SG72I, LIFCL-40-9MG289IES, LIFCL-40-8MG289I, LIFCL-40-8MG289C, LIFCL-40-9MG289I, LIFCL-40-7MG121IES, LIFCL-40-9BG400I, LIFCL-40-9BG256I, LIFCL-40-9MG289IES2, LIFCL-40-7MG121C, LIFCL-40-8BG256I, LIFCL-40-7BG256C, LIFCL-40-7BG256I, LIFCL-40-7BG400C, LIFCL-40-7BG400I, LIFCL-40-7MG289C, LIFCL-40-8BG400I, LIFCL-40-

9BG400C, LIFCL-40-9MG121C, LIFCL-40-9MG121I, LIFCL-40-9SG72C, LIFCL-40-9SG72I, LIFCL-17-7MG121C, LIFCL-17-9MG121I, LIFCL-17-9BG256C, LIFCL-17-7MG121I, LIFCL-17-7UWG72CES, LIFCL-17-8MG121C, LIFCL-17-8UWG72I, LIFCL-17-8SG72I, LIFCL-17-9SG72I, LIFCL-17-8MG121I, LIFCL-17-7MG121CES, LIFCL-17-7UWG72C, LIFCL-17-7UWG72I, LIFCL-17-7SG72C, LIFCL-17-7MG121IES, LIFCL-17-7BG256C, LIFCL-17-7BG256I , LIFCL-17-7SG72I , LIFCL-17-8BG256C , LIFCL-17-8BG256I , LIFCL-17-8SG72C, LIFCL-17-8UWG72C, LIFCL-17-9BG256I, LIFCL-17-9MG121C, LIFCL-17-9SG72C, LIFCL-17-9UWG72C, LIFCL-17-9UWG72I, LFD2NX-17-7MG121C, LFD2NX-17-7MG121I, LFD2NX-17-8MG121C, LFD2NX-17-8MG121I, LFD2NX-17-9MG121C, LFD2NX-17-9MG121I, LFD2NX-40-7BG256I, LFD2NX-40-7BG196C, LFD2NX-40-9MG121IES, LFD2NX-40-9MG121I, LFD2NX-40-9BG196I, LFD2NX-40-7BG256C, LFD2NX-40-8BG256I, LFD2NX-40-7MG121C, LFD2NX-40-7MG121I, LFD2NX-40-8BG196C, LFD2NX-40-8BG196I, LFD2NX-40-8MG121C, LFD2NX-40-8MG121I, LFD2NX-40-9BG196C, LFD2NX-40-9BG256C, LFD2NX-40-9BG256I, LFD2NX-40-9MG121C, LFD2NX-40-7BG196I, LFD2NX-40-8BG256C, LIFCL-VVML-EVN, LIFCL-40-EVN, LIFCL-VIP-SI-EVN, LFD2NX-VERSA-EVN, etc.



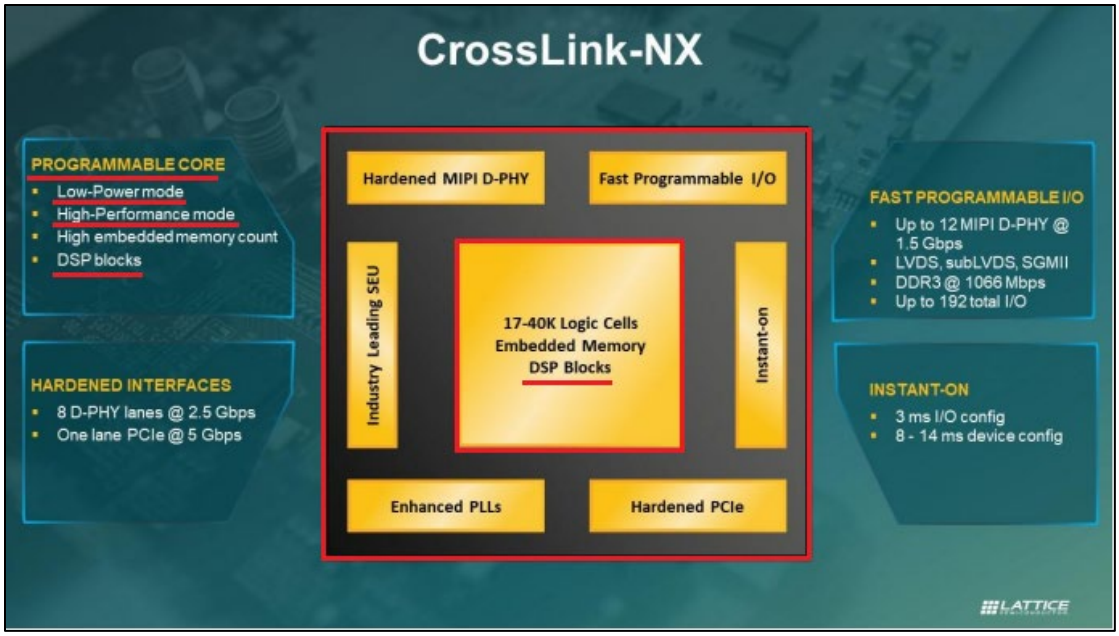
Source: https://www.businesswire.com/news/home/20191210005349/en/New-Lattice-CrossLink-NX-FPGAs-Bring-Power-and-Performance-Leadership-to-Embedded-Vision-and-Edge-AI-Applications

16. By doing so, Lattice has directly infringed (literally and/or under the doctrine of equivalents) at least Claim 9 of the '504 Patent. Lattice's infringement in this regard is ongoing.

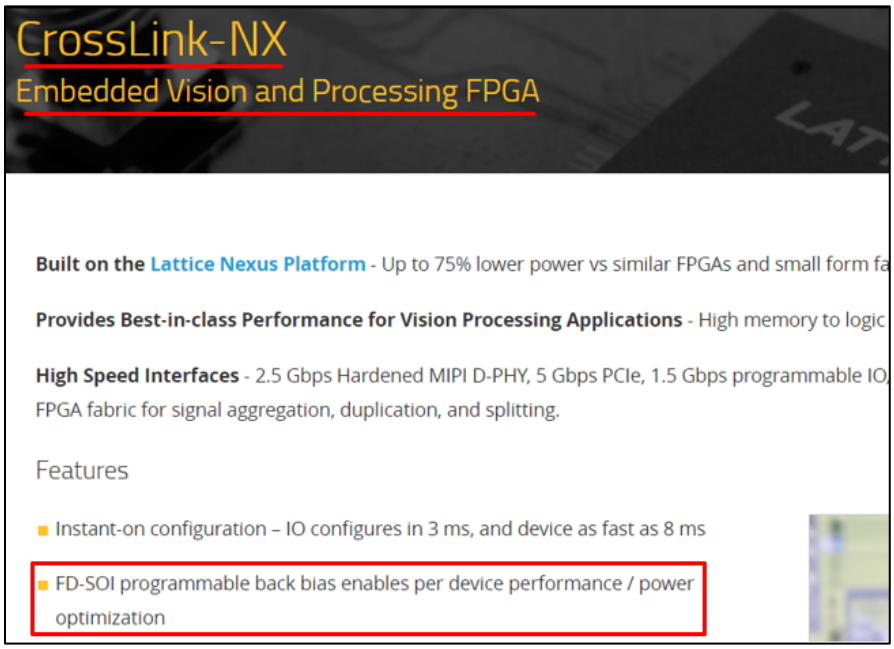
17. Lattice's CrossLink-NX family of FPGA devices are exemplary accused products.

18. Lattice has infringed the '504 Patent by using the accused products and thereby practicing a method for determining a body biasing voltage applied to a microprocessor.

19. For example, Lattice's CrossLink-NX family of FPGA devices ("computer system") includes logic cells and digital signal processing (DSP) blocks ("microprocessor") for applications like signal processing, Edge AI processing, video processing, etc. A CrossLink-NX device uses FD-SOI programmable back-bias technology for power optimization. The FD-SOI technology allows application of programmable body bias voltages to the die.



Source: https://www.tiriasresearch.com/wp-content/uploads/2020/04/TIRIAS_Research-Lattice_Crosslink_NX.pdf (Page 6)

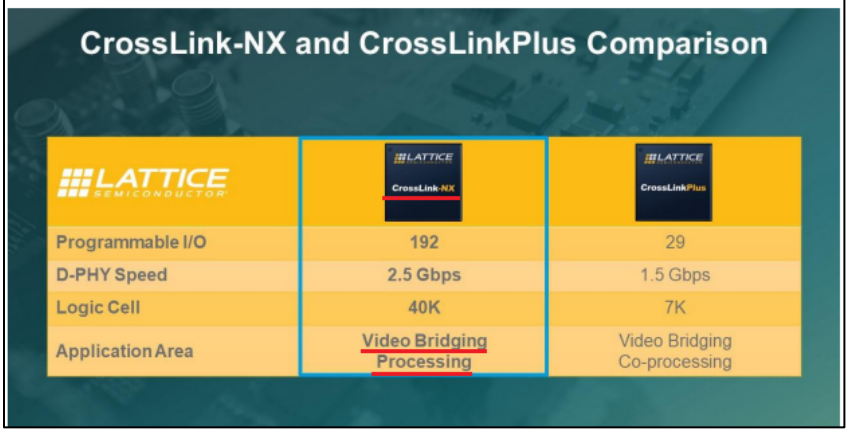


Source: https://www.latticesemi.com/Products/FPGAandCPLD/CrossLink-NX?ActiveTab=User+Manual

detection. Supporting embedded vision applications at the Edge, however, requires devices offer certain design and performance characteristics: low power consumption, high performance, high reliability and a small form factor. For these applications, Lattice has built a new family of FPGAs under the Lattice CrossLink-NX™ brand. Lattice's new chips are designed to address the latest trends in video processing: mixing multiple sensors and displays, higher resolution video, multiple interfaces, and Edge AI processing.

CrossLink meets Nexus

To help developers support new and existing embedded vision systems, Lattice Semiconductor created the CrossLinkPlus™ family of specialized, small-footprint, low-power FPGAs.



Source: https://www.tiriasresearch.com/wp-content/uploads/2020/04/TIRIAS_Research-Lattice_Crosslink_NX.pdf (Page 1)

1. Introduction

CrossLink-NX™ low power FPGA devices from Lattice Semiconductor help stretch the battery life of an application by lowering power consumption. CrossLink-NX features the ability to dynamically shut down used blocks in user mode. In addition, there is the ability to switch the device from High Performance (HP) to Low Power (LP) mode by changing the technology back bias via a performance grade selection.

Source: http://www.latticesemi.com/-/media/LatticeSemi/Documents/ApplicationNotes/PT2/FPGA-TN-02075-1-0-Power-Management-Calculation-for-CrossLinkNX-Devices.ashx?document_id=52795 (Page 5)

FD-SOI Enables Innovative New Power Modes and Higher Reliability

The use of FD-SOI allowed Lattice to create an innovative way for developers to manage power. The process allows the application of a voltage on the back side of the die (back-bias) that changes the threshold voltage. This allows Lattice to offer two operating modes – lower power mode and a higher performing mode. With power optimizations, the operating power at higher frequencies can be in the 200mW range, with only a few 10's of mW static leakage. Power consumption for CrossLink-NX FPGAs is up to 75 percent lower than other competing devices of a similar class.

Source: https://www.tiriasresearch.com/wp-content/uploads/2020/04/TIRIAS_Research-Lattice_Crosslink_NX.pdf (Page 4)

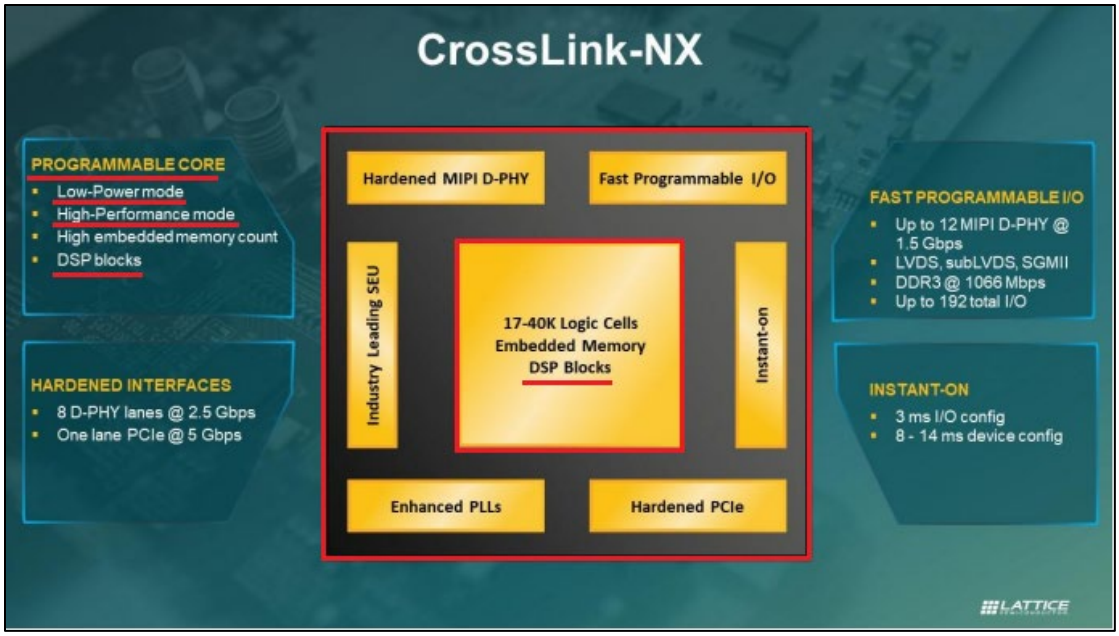
> The first is that whole-chip electric field control is available through substrate biasing ('back-biasing') – allowing device speed to be traded off for power consumption. According to Hands, this is used during product manufacture, and is available to users (although not on-the-fly – device configuration must be re-loaded after a bias change).

Source: https://www.electronicsweekly.com/news/products/fpga-pld/lattice-moves-fd-soi-redesigns-fpgas-embedded-vision-edge-ai-2019-12/

20. The method practiced using the accused products comprises receiving a command to change to a different power condition of a computer system comprising the microprocessor. The power condition comprises a different microprocessor clock frequency and/or a different microprocessor operating voltage.

21. For example, Lattice's CrossLink-NX family of FPGA devices ("computer system") includes logic cells and digital signal processing (DSP) blocks ("microprocessor") for applications like signal processing, Edge AI processing, video processing, etc. A CrossLink-NX device supports two power modes: High Performance (HP) mode and Low Power (LP) mode. Each power mode is associated with a performance grade. The power mode of the device can be switched from HP mode to LP mode via a performance grade selection.

22. Accordingly, a command can be received to change the power mode of the device from HP to LP ("a different power condition"). Further, each performance grade (i.e., power mode) is associated with a different speed ("clock frequency") and voltage ("operating voltage").



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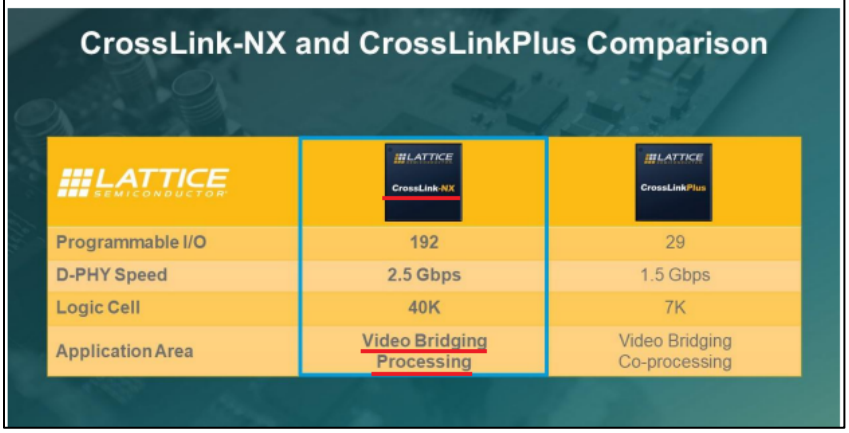

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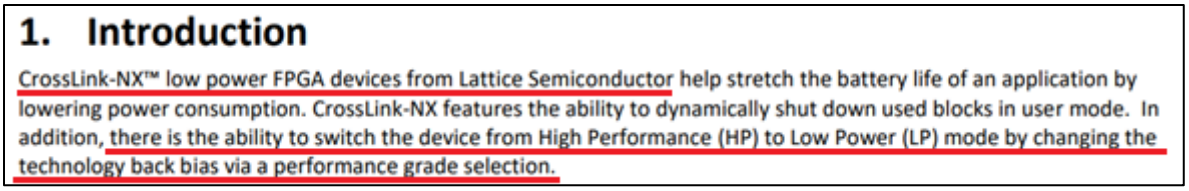

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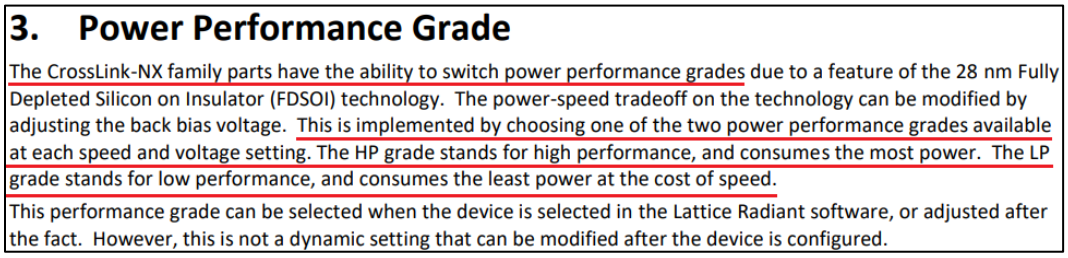


3. Power Performance Grade

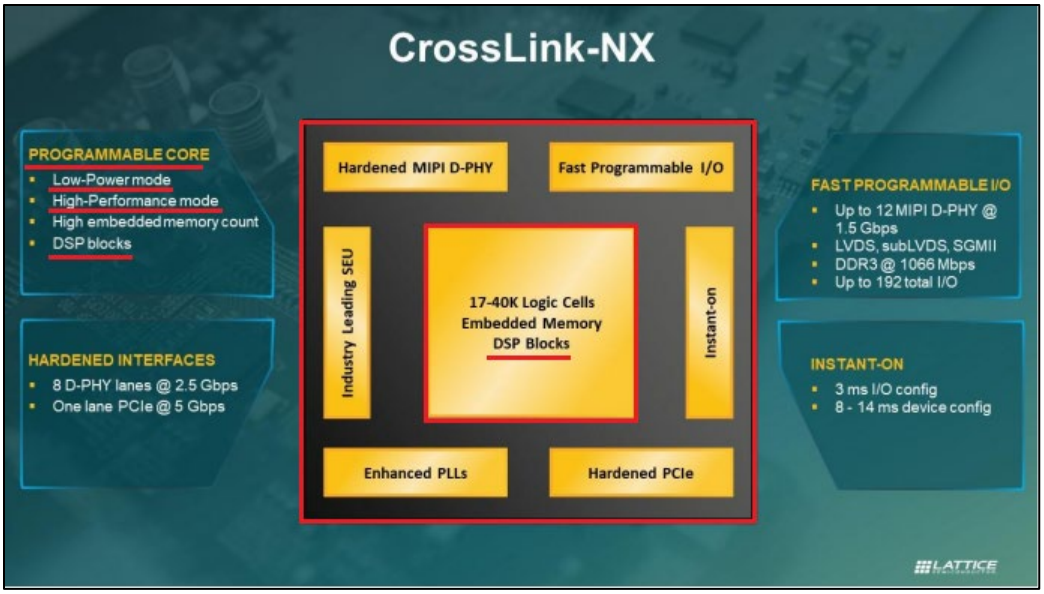
The CrossLink-NX family parts have the ability to switch power performance grades due to a feature of the 28 nm Fully Depleted Silicon on Insulator (FDSOI) technology. The power-speed tradeoff on the technology can be modified by adjusting the back bias voltage. This is implemented by choosing one of the two power performance grades available at each speed and voltage setting. The HP grade stands for high performance, and consumes the most power. The LP grade stands for low performance, and consumes the least power at the cost of speed.

This performance grade can be selected when the device is selected in the Lattice Radiant software, or adjusted after the fact. However, this is not a dynamic setting that can be modified after the device is configured.

Source: http://www.latticesemi.com/-/media/LatticeSemi/Documents/ApplicationNotes/PT2/FPGA-TN-02075-1-0-Power-Management-Calculation-for-CrossLinkNX-Devices.ashx?document_id=52795 (Page 9)

23. The method practiced using the accused products further comprises accessing body biasing voltage information corresponding to the power condition.

24. For example, Lattice's CrossLink-NX family of FPGA devices includes logic cells and digital signal processing (DSP) blocks ("microprocessor") for applications like signal processing, Edge AI processing, video processing, etc. A CrossLink-NX device uses FD-SOI programmable back-bias technology for power optimization. The FD-SOI technology allows application of programmable body bias voltages to the die. The power mode of the device can be switched from HP mode to LP mode by changing the value of the back-bias voltage ("body biasing voltage information"). Accordingly, the programmed back-bias voltage of the LP mode ("said power condition") can be accessed.



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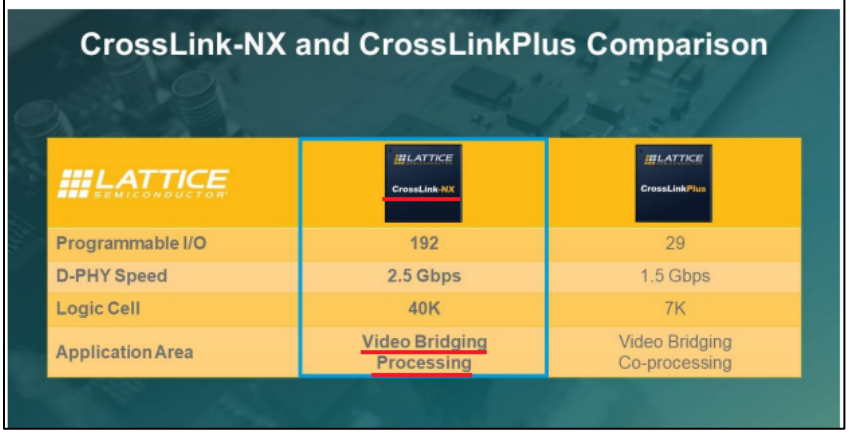

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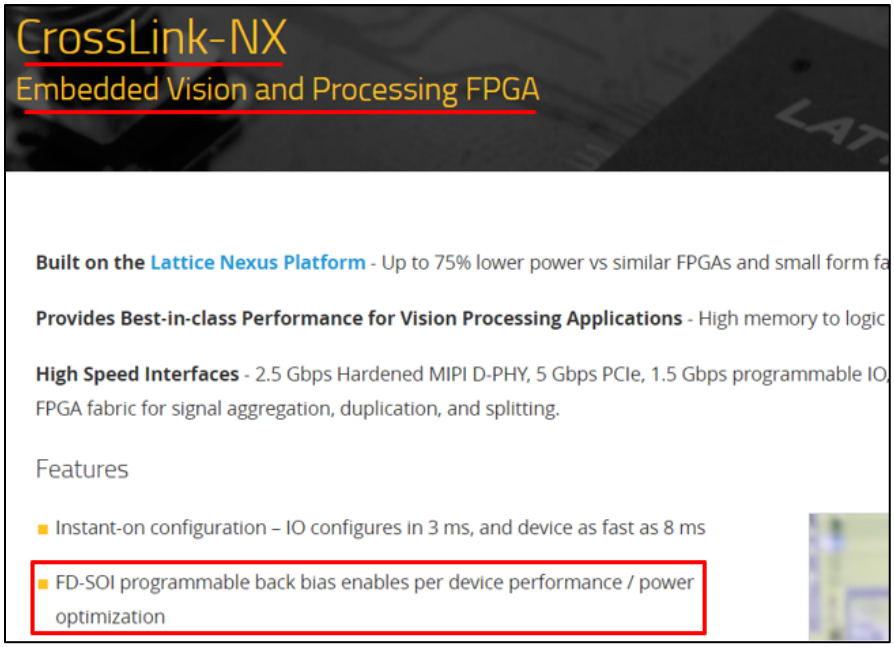

Source: https://www.latticesemi.com/Products/FPGAandCPLD/CrossLink-NX?ActiveTab=User+Manual

In video surveillance and security applications, CrossLink-NX can be used for sensor aggregation and bridging, in addition to powering AI inferencing to preprocess the sensor data with functions such as facial recognition or presence detection.

The chip can be used as an embedded vision co-processor to merge up to 14 sensors. It can also be used for video scaling, rotation, and color space conversions. With this chip, one sensor stream can be sent to multiple locations, which is useful in applications such as automotive, where cameras need to feed multiple processing units.

Source: https://www.tiriasresearch.com/wp-content/uploads/2020/04/TIRIAS_Research-Lattice_Crosslink_NX.pdf (Page 3)

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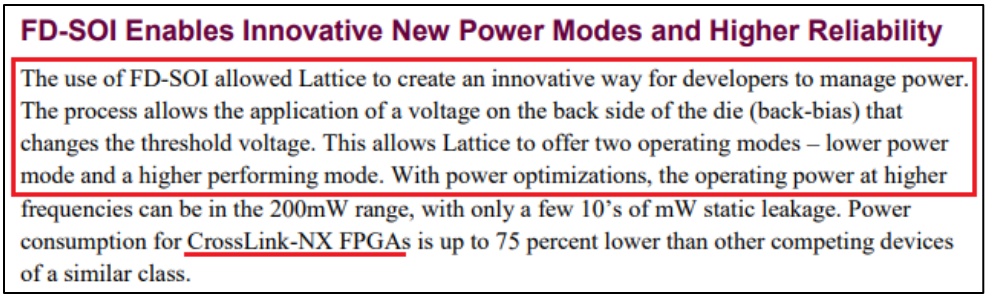

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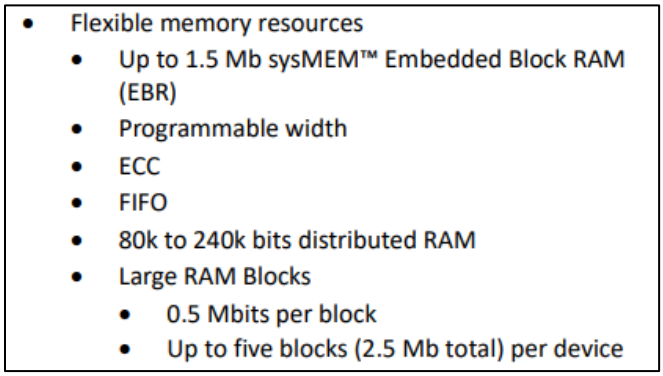
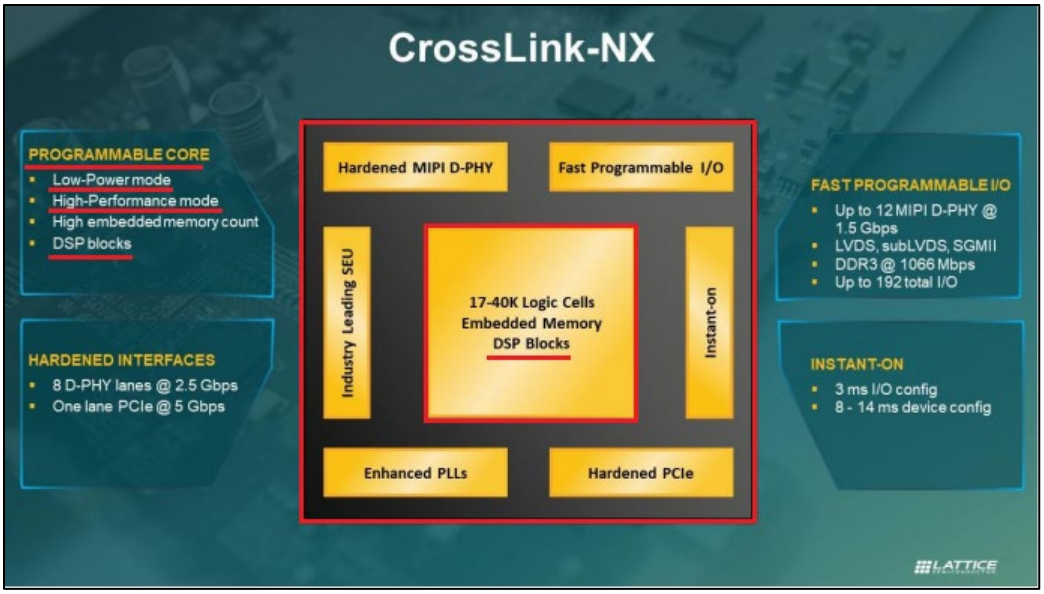


- Flexible memory resources
  - Up to 1.5 Mb sysMEM™ Embedded Block RAM (EBR)
  - Programmable width
  - ECC
  - FIFO
  - 80k to 240k bits distributed RAM
  - Large RAM Blocks
    - 0.5 Mbits per block
    - Up to five blocks (2.5 Mb total) per device

Source: https://www.latticesemi.com/view_document?document_id=52780 (Page 12)

25. The method practiced using the accused products further comprises commanding a voltage supply coupled to a body terminal of the microprocessor to generate a voltage corresponding to the body biasing voltage information corresponding to the power condition.

26. For example, Lattice's CrossLink-NX family of FPGA devices includes logic cells and digital signal processing (DSP) blocks ("microprocessor") for applications like signal processing, Edge AI processing, video processing, etc. A CrossLink-NX device uses FD-SOI programmable back-bias technology for power optimization. The power mode of the device can be switched from HP mode to LP mode by changing the value of the back-bias voltage ("said body biasing voltage information"). Accordingly, using the programmed back-bias voltage information of the LP mode ("said power condition"), a voltage supply coupled to the body terminal of the die can generate the corresponding body bias voltage based on a command.



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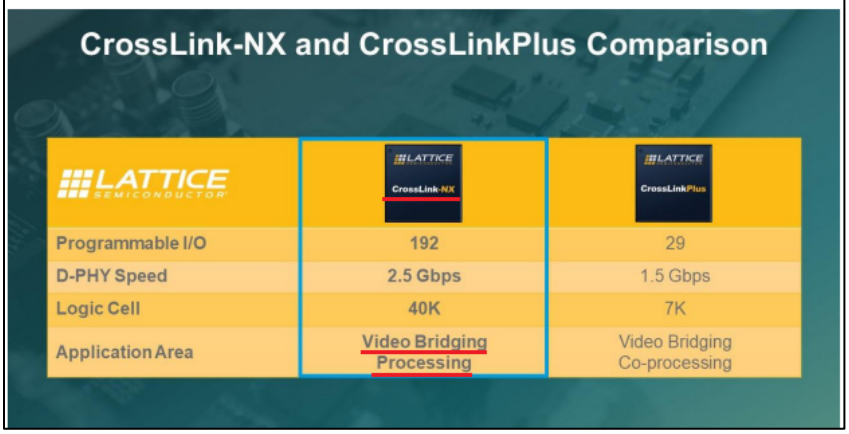
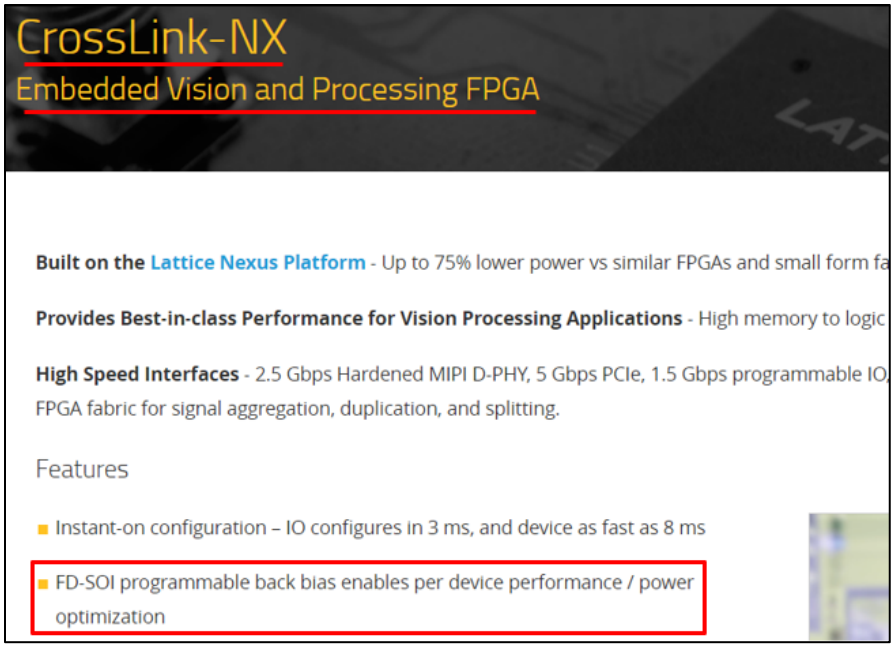


Source: https://www.tiriasresearch.com/wp-content/uploads/2020/04/TIRIAS_Research-Lattice_Crosslink_NX.pdf (Page 1)



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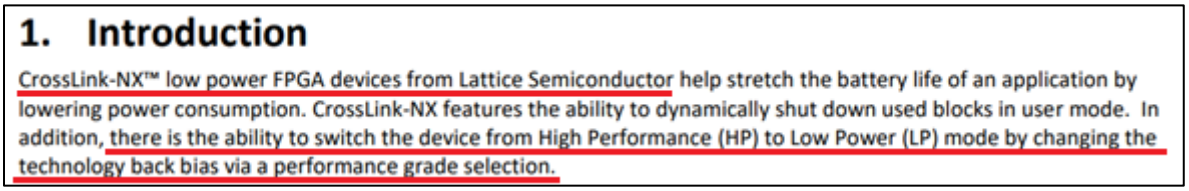

1. Introduction

CrossLink-NX™ low power FPGA devices from Lattice Semiconductor help stretch the battery life of an application by lowering power consumption. CrossLink-NX features the ability to dynamically shut down used blocks in user mode. In addition, there is the ability to switch the device from High Performance (HP) to Low Power (LP) mode by changing the technology back bias via a performance grade selection.

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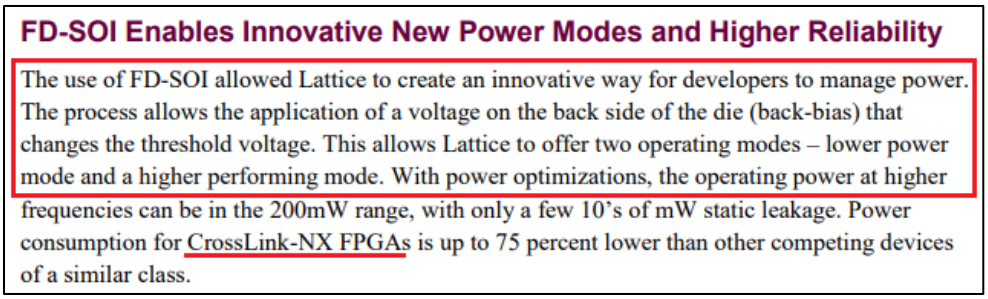

FD-SOI Enables Innovative New Power Modes and Higher Reliability

The use of FD-SOI allowed Lattice to create an innovative way for developers to manage power. The process allows the application of a voltage on the back side of the die (back-bias) that changes the threshold voltage. This allows Lattice to offer two operating modes – lower power mode and a higher performing mode. With power optimizations, the operating power at higher frequencies can be in the 200mW range, with only a few 10's of mW static leakage. Power consumption for CrossLink-NX FPGAs is up to 75 percent lower than other competing devices of a similar class.

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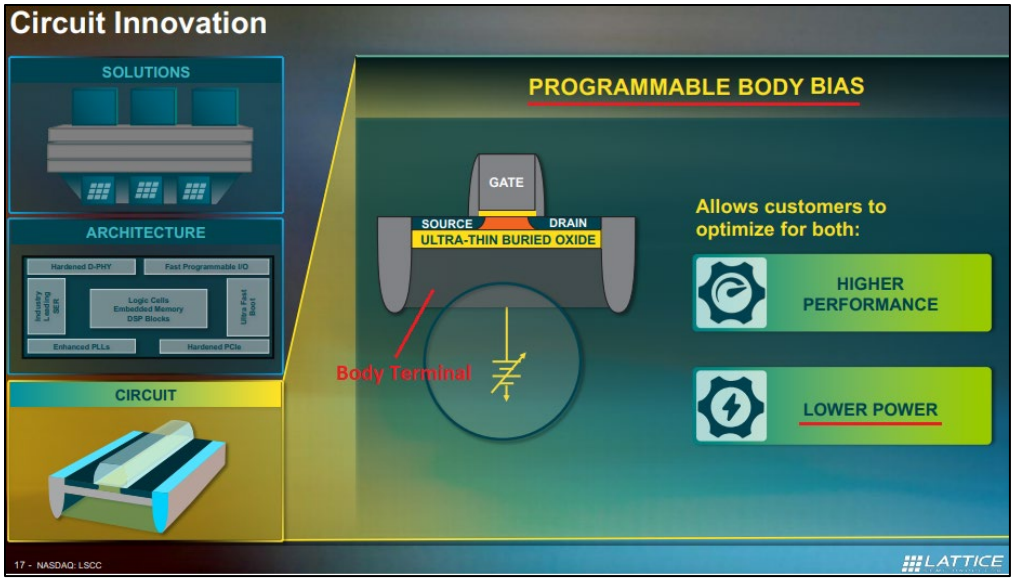

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Source: https://www.electronicsweekly.com/news/products/fpga-pld/lattice-moves-fd-soi-redesigns-fpgas-embedded-vision-edge-ai-2019-12/

27. Lattice has had knowledge of the '504 Patent at least as of the date when it was notified of the filing of this action.

28. Liberty Patents has been damaged as a result of the infringing conduct by Lattice alleged above. Thus, Lattice is liable to Liberty Patents in an amount that adequately compensates it for such infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

29. Liberty Patents and/or its predecessors-in-interest have satisfied all statutory obligations required to collect pre-filing damages for the full period allowed by law for infringement of the '504 Patent.

COUNT II

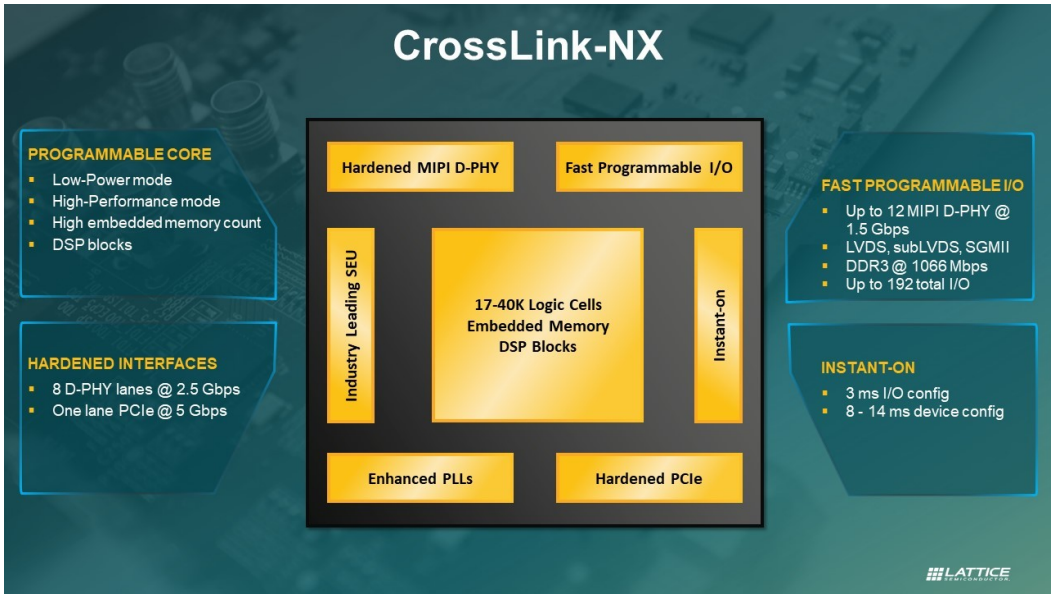
DIRECT INFRINGEMENT OF U.S. PATENT NO. 8,127,156

30. On February 28, 2012, U.S. Patent No. 8,127,156 ("the '156 Patent") was duly and legally issued by the United States Patent and Trademark Office for an invention entitled "Systems and Methods for Control of Integrated Circuits Comprising Body Biasing Systems."

31. Liberty Patents is the owner of the '156 Patent, with all substantive rights in and to that patent, including the sole and exclusive right to prosecute this action and enforce the '156 Patent against infringers, and to collect damages for all relevant times.

32. Lattice made, had made, used, imported, provided, supplied, distributed, sold, and/or offered for sale products and/or systems including, for example, Lattice's CrossLink-NX family of FPGA devices and other products[8] that are capable of applying body biasing voltages during a power mode of a processor or other integrated circuit ("accused products"):

[8] *See, e.g.*, Lattice LIFCL-40-7BG400C, LIFCL-40-9MG289C, LIFCL-40-7SG72CES, LIFCL-40-8SG72C, LIFCL-40-9BG256C, LIFCL-40-7MG121I, LIFCL-40-7BG400CES, LIFCL-40-7MG121CES, LIFCL-40-7SG72IES, LIFCL-40-8BG400C, LIFCL-40-8BG256C, LIFCL-40-8MG121C, LIFCL-40-7MG289I, LIFCL-40-8MG121I, LIFCL-40-8SG72I, LIFCL-40-9MG289IES, LIFCL-40-8MG289I, LIFCL-40-8MG289C, LIFCL-40-9MG289I, LIFCL-40-7MG121IES, LIFCL-40-9BG400I, LIFCL-40-9BG256I, LIFCL-40-9MG289IES2, LIFCL-40-7MG121C, LIFCL-40-8BG256I, LIFCL-40-7BG256C, LIFCL-40-7BG256I, LIFCL-40-7BG400C, LIFCL-40-7BG400I, LIFCL-40-7MG289C, LIFCL-40-8BG400I, LIFCL-40-9BG400C, LIFCL-40-9MG121C, LIFCL-40-9MG121I, LIFCL-40-9SG72C, LIFCL-40-9SG72I, LIFCL-17-7MG121C, LIFCL-17-9MG121I, LIFCL-17-9BG256C, LIFCL-17-7MG121I, LIFCL-17-7UWG72CES, LIFCL-17-8MG121C, LIFCL-17-8UWG72I, LIFCL-17-8SG72I, LIFCL-17-9SG72I, LIFCL-17-8MG121I, LIFCL-17-7MG121CES, LIFCL-17-7UWG72C, LIFCL-17-7UWG72I, LIFCL-17-7SG72C, LIFCL-17-7MG121IES, LIFCL-17-7BG256C, LIFCL-17-7BG256I , LIFCL-17-7SG72I , LIFCL-17-8BG256C , LIFCL-17-8BG256I , LIFCL-17-8SG72C, LIFCL-17-8UWG72C, LIFCL-17-9BG256I, LIFCL-17-9MG121C, LIFCL-17-



Source: https://www.businesswire.com/news/home/20191210005349/en/New-Lattice-CrossLink-NX-FPGAs-Bring-Power-and-Performance-Leadership-to-Embedded-Vision-and-Edge-AI-Applications

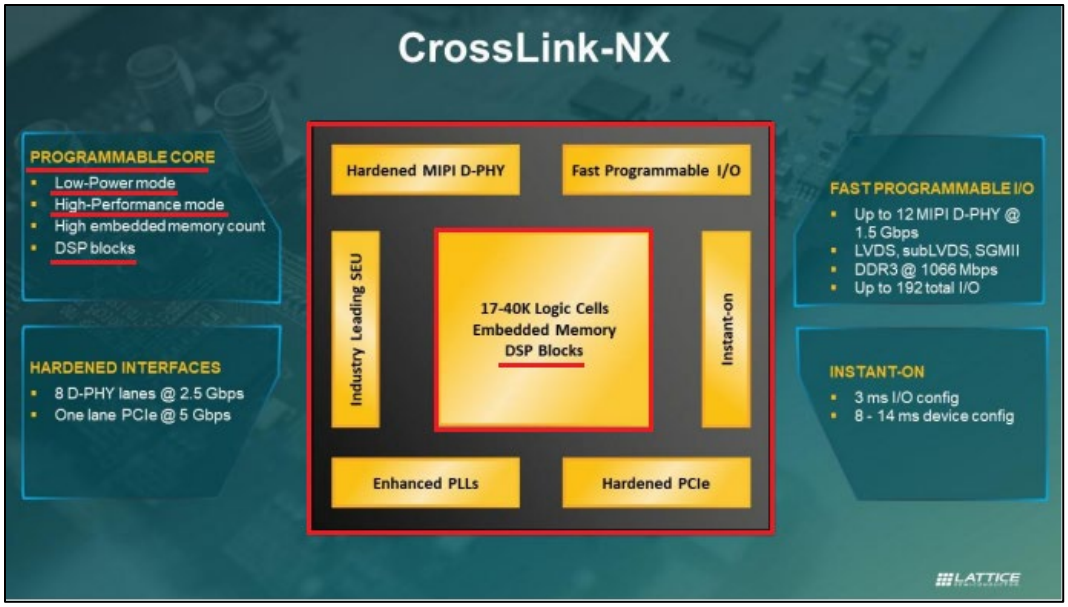
9SG72C, LIFCL-17-9UWG72C, LIFCL-17-9UWG72I, LFD2NX-17-7MG121C, LFD2NX-17-7MG121I, LFD2NX-17-8MG121C, LFD2NX-17-8MG121I, LFD2NX-17-9MG121C, LFD2NX-17-9MG121I, LFD2NX-40-7BG256I, LFD2NX-40-7BG196C, LFD2NX-40-9MG121IES, LFD2NX-40-9MG121I, LFD2NX-40-9BG196I, LFD2NX-40-7BG256C, LFD2NX-40-8BG256I, LFD2NX-40-7MG121C, LFD2NX-40-7MG121I, LFD2NX-40-8BG196C, LFD2NX-40-8BG196I, LFD2NX-40-8MG121C, LFD2NX-40-8MG121I, LFD2NX-40-9BG196C, LFD2NX-40-9BG256C, LFD2NX-40-9BG256I, LFD2NX-40-9MG121C, LFD2NX-40-7BG196I, LFD2NX-40-8BG256C, LIFCL-VVML-EVN, LIFCL-40-EVN, LIFCL-VIP-SI-EVN, LFD2NX-VERSA-EVN, etc.

33. By doing so, Lattice has directly infringed (literally and/or under the doctrine of equivalents) at least Claim 9 of the '156 Patent. Lattice's infringement in this regard is ongoing.

34. Lattice's CrossLink-NX family of FPGA devices are exemplary accused products.

35. Lattice has infringed the '156 Patent by using the accused products and thereby practicing a method for determining a desirable power condition, of a set of power conditions, of a computer system comprising a microprocessor, wherein the set of power conditions comprises a power down state.

36. For example, Lattice's CrossLink-NX family of FPGA devices ("computer system") includes logic cells and digital signal processing (DSP) blocks ("microprocessor") for applications like signal processing, Edge AI processing, video processing, etc. A CrossLink-NX device supports two power modes ("a set of power conditions"): High Performance (HP) mode and Low Power (LP) mode. Each power mode is associated with a performance grade. The power mode of the device can be switched from HP mode to LP mode via a performance grade selection. Accordingly, a desirable power mode of a CrossLink-NX device can be determined by selecting a performance grade. Further, the LP mode of the device is a low power state (i.e., "a power down state").



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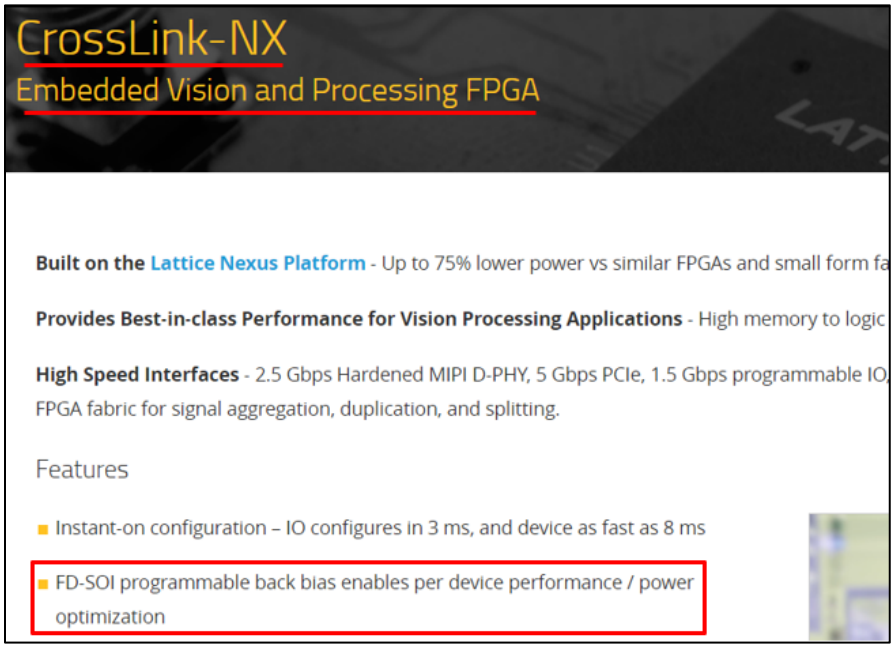
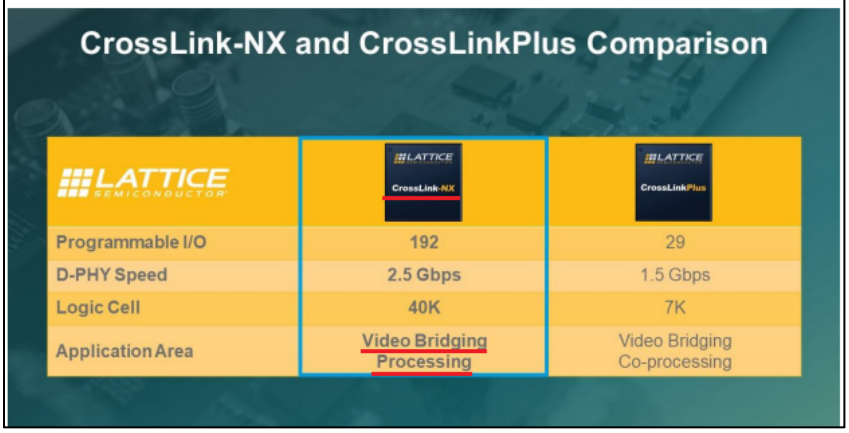


Source: https://www.latticesemi.com/Products/FPGAandCPLD/CrossLink-NX?ActiveTab=User+Manual

detection. Supporting embedded vision applications at the Edge, however, requires devices offer certain design and performance characteristics: low power consumption, high performance, high reliability and a small form factor. For these applications, Lattice has built a new family of FPGAs under the Lattice CrossLink-NX™ brand. Lattice's new chips are designed to address the latest trends in video processing: mixing multiple sensors and displays, higher resolution video, multiple interfaces, and Edge AI processing.

CrossLink meets Nexus

To help developers support new and existing embedded vision systems, Lattice Semiconductor created the CrossLinkPlus™ family of specialized, small-footprint, low-power FPGAs.



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In video surveillance and security applications, CrossLink-NX can be used for sensor aggregation and bridging, in addition to powering AI inferencing to preprocess the sensor data with functions such as facial recognition or presence detection.

The chip can be used as an embedded vision co-processor to merge up to 14 sensors. It can also be used for video scaling, rotation, and color space conversions. With this chip, one sensor stream can be sent to multiple locations, which is useful in applications such as automotive, where cameras need to feed multiple processing units.

Source: https://www.tiriasresearch.com/wp-content/uploads/2020/04/TIRIAS_Research-Lattice_Crosslink_NX.pdf (Page 3).

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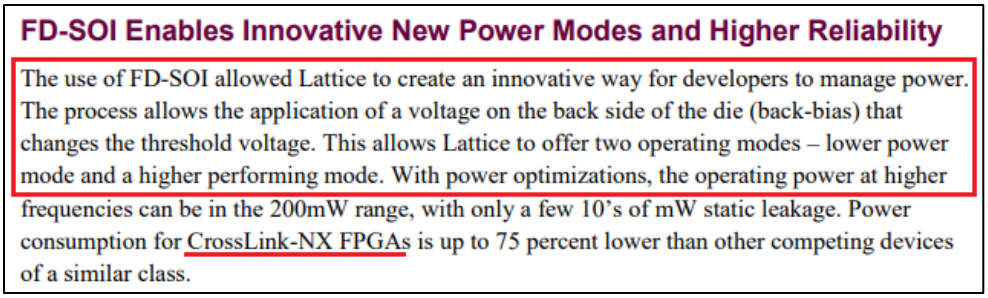

FD-SOI Enables Innovative New Power Modes and Higher Reliability

The use of FD-SOI allowed Lattice to create an innovative way for developers to manage power. The process allows the application of a voltage on the back side of the die (back-bias) that changes the threshold voltage. This allows Lattice to offer two operating modes – lower power mode and a higher performing mode. With power optimizations, the operating power at higher frequencies can be in the 200mW range, with only a few 10's of mW static leakage. Power consumption for CrossLink-NX FPGAs is up to 75 percent lower than other competing devices of a similar class.

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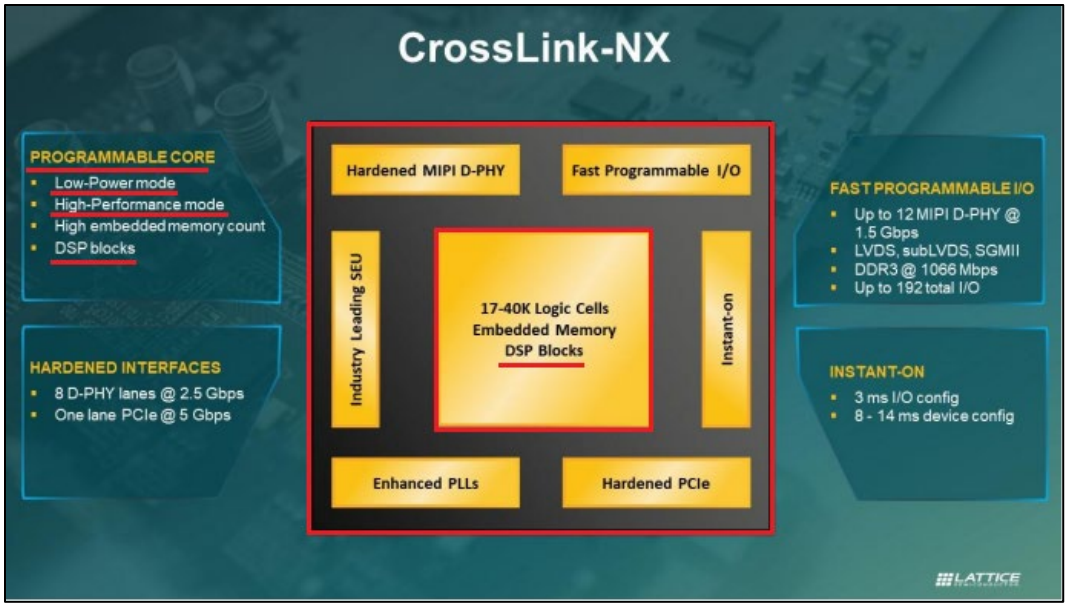
37. The method practiced using the accused products further comprises accessing body biasing voltage information corresponding to the power condition.

38. For example, Lattice's CrossLink-NX family of FPGA devices includes logic cells and digital signal processing (DSP) blocks ("microprocessor") for applications like signal processing, Edge AI processing, video processing, etc. A CrossLink-NX device uses FD-SOI programmable back-bias technology for power optimization. The power mode of the device can be switched from HP mode to LP mode by changing the value of the back-bias voltage ("body biasing voltage information"). Accordingly, the programmed back-bias voltage of the LP mode ("said power condition") can be accessed.



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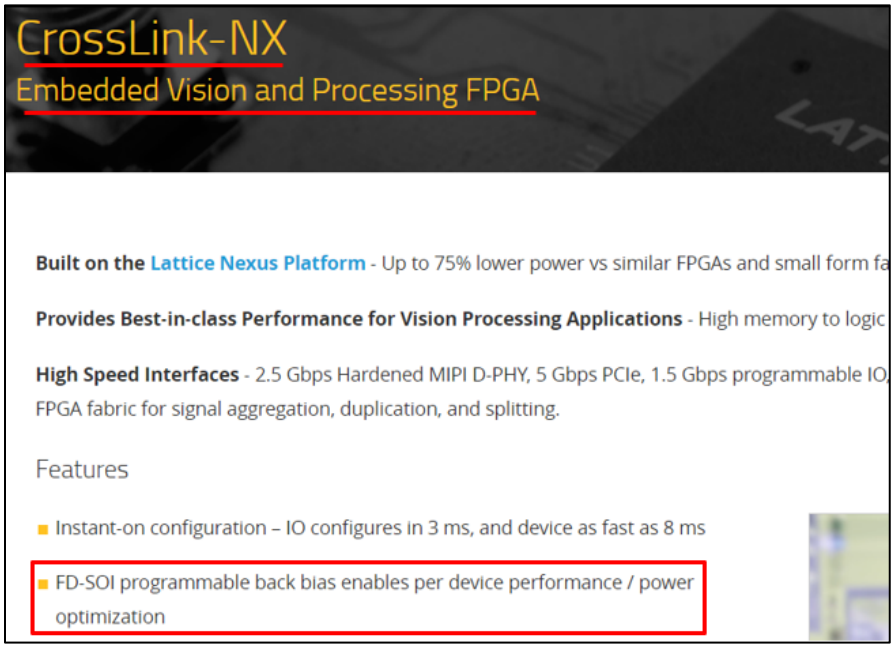

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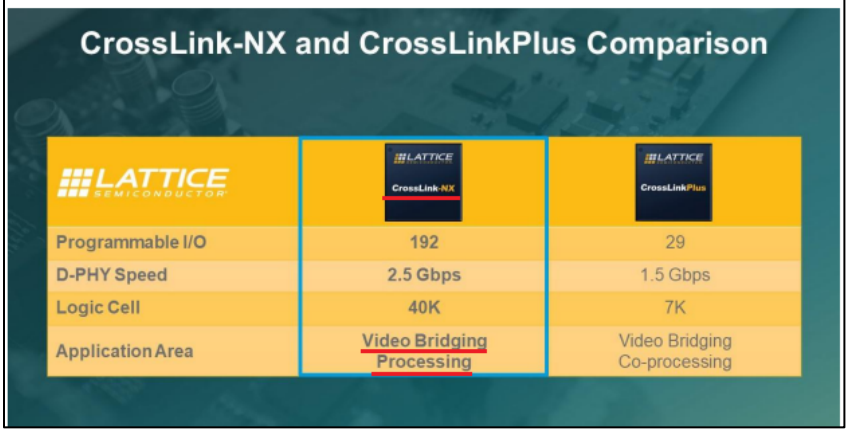

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39. The method practiced using the accused products further comprises commanding a voltage supply coupled to a body terminal of the microprocessor to generate a voltage corresponding to the body biasing voltage information corresponding to the power condition.

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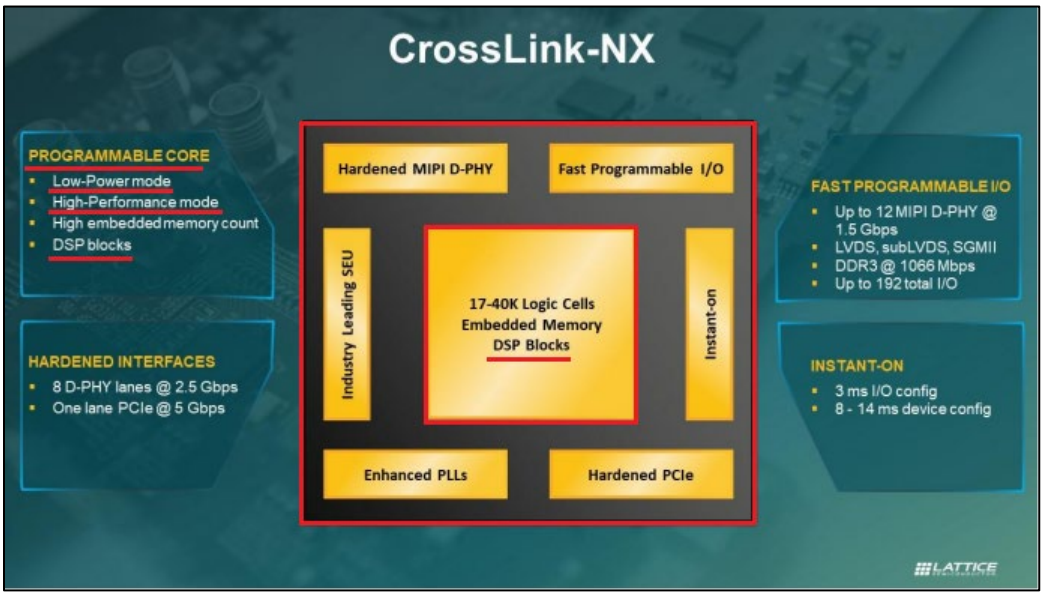

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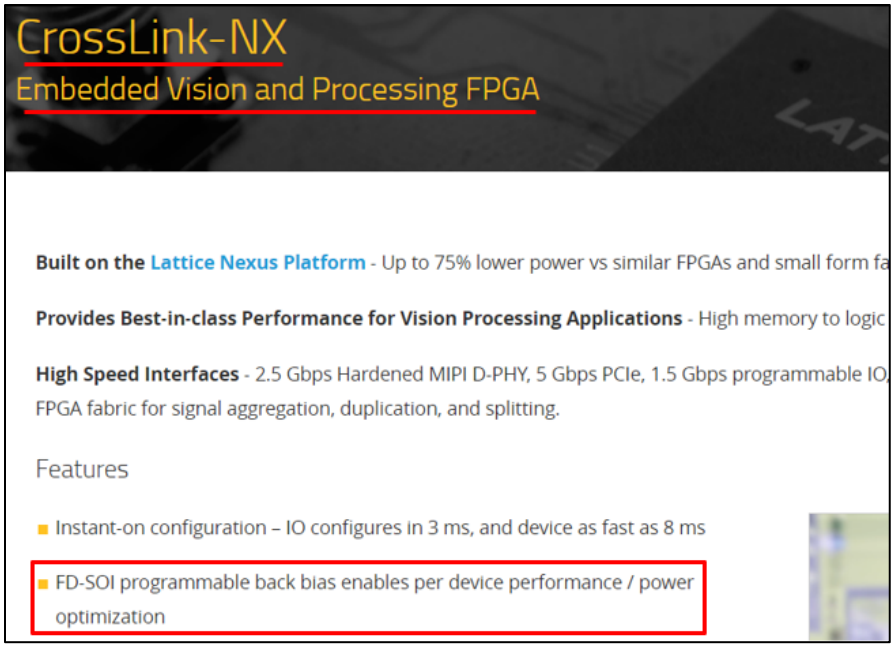

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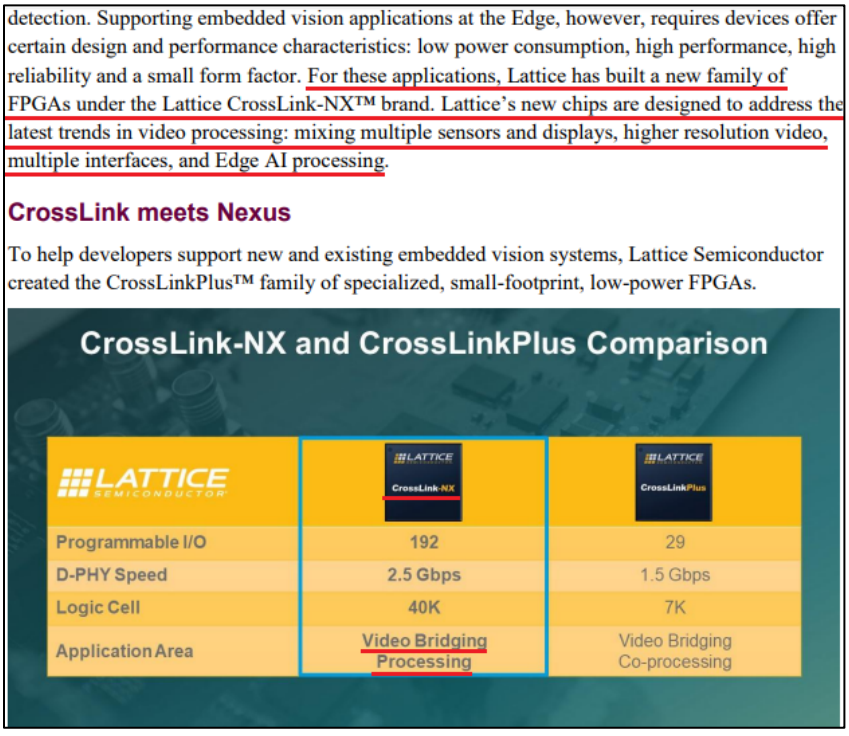

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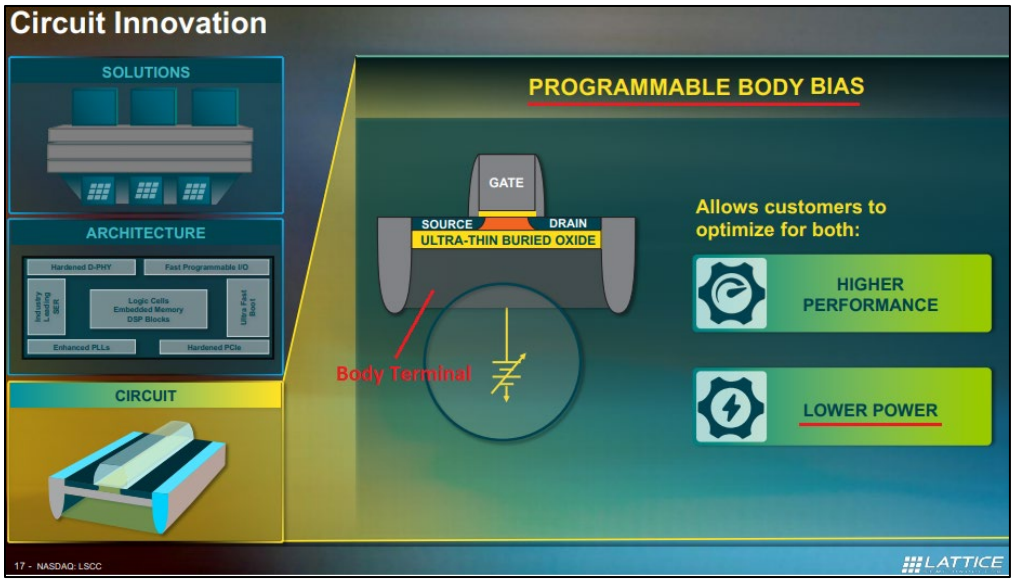

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41. Lattice has had knowledge of the '156 Patent at least as of the date when it was notified of the filing of this action.

42. Liberty Patents has been damaged as a result of the infringing conduct by Lattice alleged above. Thus, Lattice is liable to Liberty Patents in an amount that adequately compensates it for such infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

43. Liberty Patents and/or its predecessors-in-interest have satisfied all statutory obligations required to collect pre-filing damages for the full period allowed by law for infringement of the '156 Patent.

COUNT III

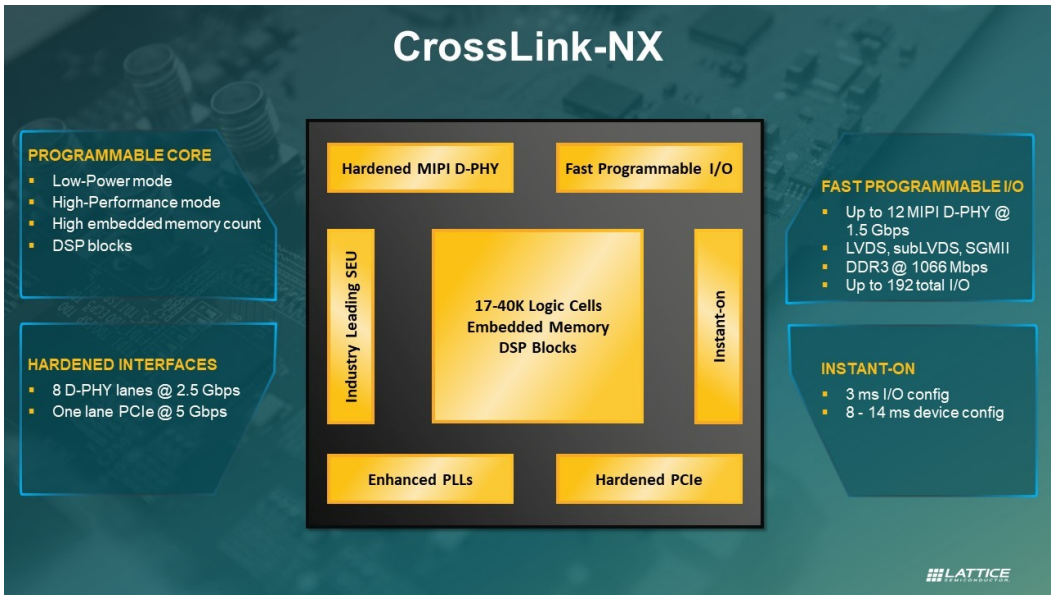
DIRECT INFRINGEMENT OF U.S. PATENT NO. 8,458,496

44. On June 4, 2013, U.S. Patent No. 8,458,496 ("the '496 Patent") was duly and legally issued by the United States Patent and Trademark Office for an invention entitled "Systems and Methods for Control of Integrated Circuits Comprising Body Biasing Systems."

45. Liberty Patents is the owner of the '496 Patent, with all substantive rights in and to that patent, including the sole and exclusive right to prosecute this action and enforce the '496 Patent against infringers, and to collect damages for all relevant times.

46. Lattice made, had made, used, imported, provided, supplied, distributed, sold, and/or offered for sale products and/or systems including, for example, Lattice's CrossLink-NX family of FPGA devices and other products[9] that are capable of applying body biasing voltages during a power mode of a processor or other integrated circuit ("accused products"):

[9] *See, e.g.*, Lattice LIFCL-40-7BG400C, LIFCL-40-9MG289C, LIFCL-40-7SG72CES, LIFCL-40-8SG72C, LIFCL-40-9BG256C, LIFCL-40-7MG121I, LIFCL-40-7BG400CES, LIFCL-40-7MG121CES, LIFCL-40-7SG72IES, LIFCL-40-8BG400C, LIFCL-40-8BG256C, LIFCL-40-8MG121C, LIFCL-40-7MG289I, LIFCL-40-8MG121I, LIFCL-40-8SG72I, LIFCL-40-9MG289IES, LIFCL-40-8MG289I, LIFCL-40-8MG289C, LIFCL-40-9MG289I, LIFCL-40-7MG121IES, LIFCL-40-9BG400I, LIFCL-40-9BG256I, LIFCL-40-9MG289IES2, LIFCL-40-7MG121C, LIFCL-40-8BG256I, LIFCL-40-7BG256C, LIFCL-40-7BG256I, LIFCL-40-7BG400C, LIFCL-40-7BG400I, LIFCL-40-7MG289C, LIFCL-40-8BG400I, LIFCL-40-9BG400C, LIFCL-40-9MG121C, LIFCL-40-9MG121I, LIFCL-40-9SG72C, LIFCL-40-9SG72I, LIFCL-17-7MG121C, LIFCL-17-9MG121I, LIFCL-17-9BG256C, LIFCL-17-7MG121I, LIFCL-17-7UWG72CES, LIFCL-17-8MG121C, LIFCL-17-8UWG72I, LIFCL-17-8SG72I, LIFCL-17-9SG72I, LIFCL-17-8MG121I, LIFCL-17-7MG121CES, LIFCL-17-7UWG72C, LIFCL-17-7UWG72I, LIFCL-17-7SG72C, LIFCL-17-7MG121IES, LIFCL-17-7BG256C, LIFCL-17-7BG256I , LIFCL-17-7SG72I , LIFCL-17-8BG256C , LIFCL-17-8BG256I , LIFCL-17-8SG72C, LIFCL-17-8UWG72C, LIFCL-17-9BG256I, LIFCL-17-9MG121C, LIFCL-17-9SG72C, LIFCL-17-9UWG72C, LIFCL-17-9UWG72I, LFD2NX-17-7MG121C, LFD2NX-17-7MG121I, LFD2NX-17-8MG121C, LFD2NX-17-8MG121I, LFD2NX-17-9MG121C, LFD2NX-17-9MG121I, LFD2NX-40-7BG256I, LFD2NX-40-7BG196C, LFD2NX-40-9MG121IES, LFD2NX-40-9MG121I, LFD2NX-40-9BG196I, LFD2NX-40-7BG256C, LFD2NX-40-8BG256I, LFD2NX-40-7MG121C, LFD2NX-40-7MG121I, LFD2NX-40-8BG196C, LFD2NX-40-8BG196I, LFD2NX-40-8MG121C, LFD2NX-40-8MG121I, LFD2NX-40-9BG196C, LFD2NX-40-9BG256C, LFD2NX-40-9BG256I, LFD2NX-40-9MG121C, LFD2NX-40-7BG196I, LFD2NX-40-8BG256C, LIFCL-VVML-EVN, LIFCL-40-EVN, LIFCL-VIP-SI-EVN, LFD2NX-VERSA-EVN, etc.



Source: https://www.businesswire.com/news/home/20191210005349/en/New-Lattice-CrossLink-NX-FPGAs-Bring-Power-and-Performance-Leadership-to-Embedded-Vision-and-Edge-AI-Applications

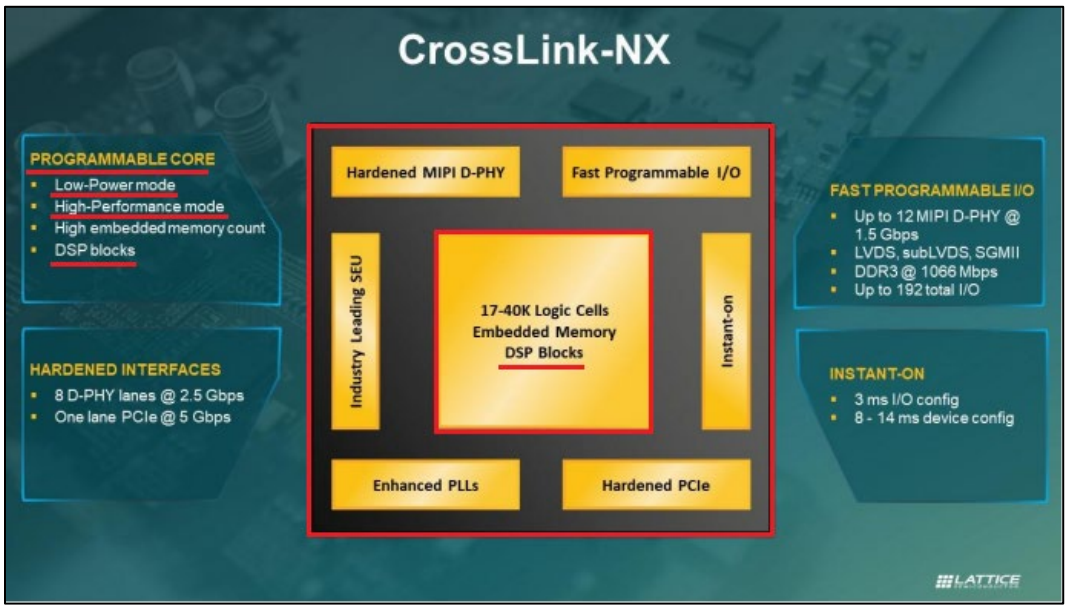
47. By doing so, Lattice has directly infringed (literally and/or under the doctrine of equivalents) at least Claim 9 of the '496 Patent. Lattice's infringement in this regard is ongoing.

48. Lattice's CrossLink-NX family of FPGA devices are exemplary accused products.

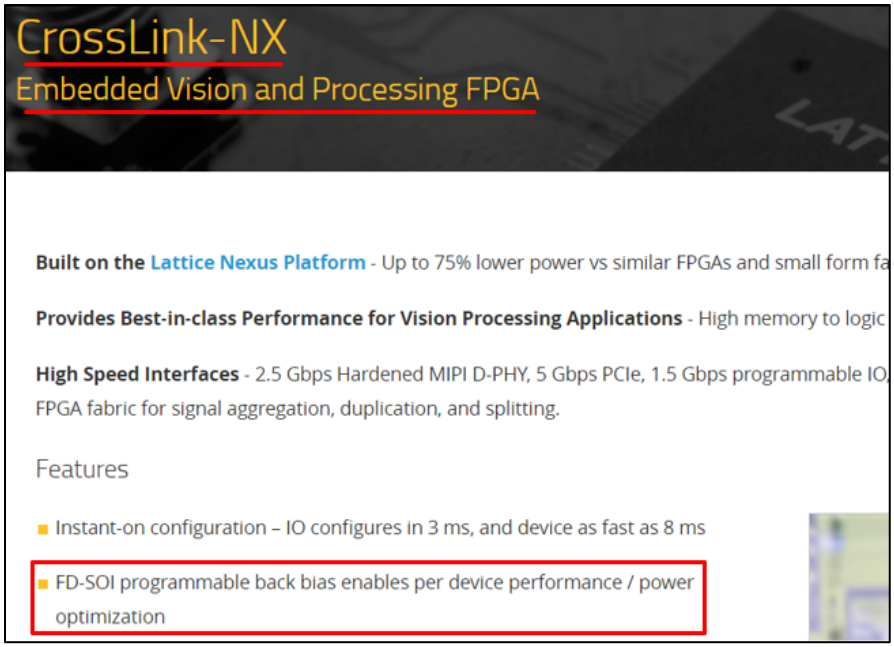
49. Lattice's CrossLink-NX family of FPGA devices includes means for determining a particular power condition, of a set of power conditions, of a computer system comprising a microprocessor, wherein the set of power conditions comprises a power down state.

50. For example, Lattice's CrossLink-NX family of FPGA devices ("computer system") includes logic cells and digital signal processing (DSP) blocks ("microprocessor") for applications like signal processing, Edge AI processing, video processing, etc. A CrossLink-NX device supports two power modes ("a set of power conditions"): High Performance (HP) mode and Low Power (LP) mode. Each power mode is associated with a performance grade. The power mode of the device can be switched from HP mode to LP mode via a performance grade

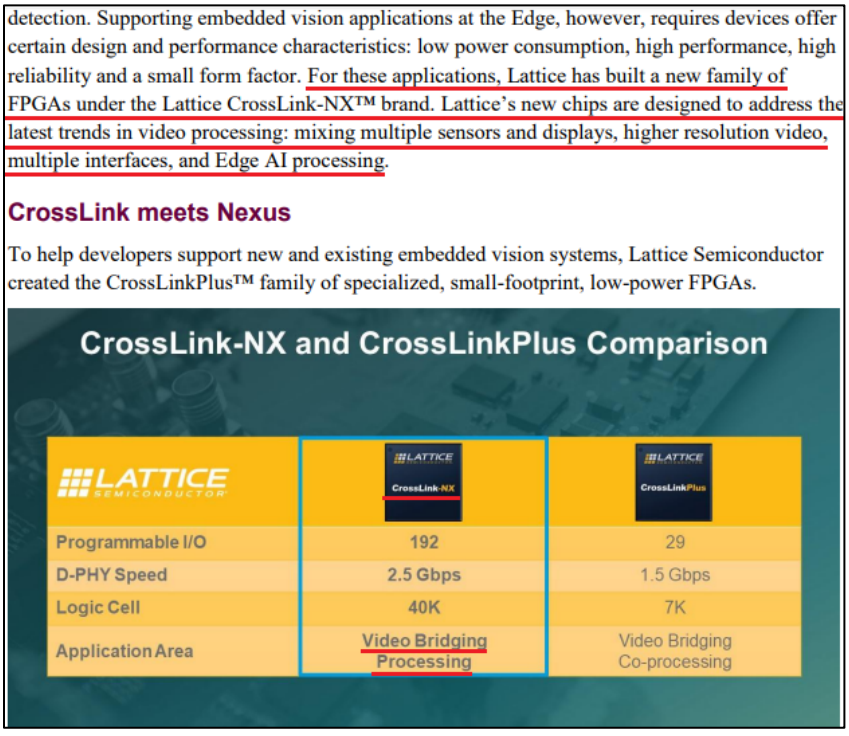
selection. Accordingly, a CrossLink-NX device includes means for determining and selecting a performance grade of a particular power mode of the device. Further, the LP mode of the device is a low power state (i.e., "a power down state").



Source: https://www.tiriasresearch.com/wp-content/uploads/2020/04/TIRIAS_Research-Lattice_Crosslink_NX.pdf (Page 6)



Source: https://www.latticesemi.com/Products/FPGAandCPLD/CrossLink-NX?ActiveTab=User+Manual



Source: https://www.tiriasresearch.com/wp-content/uploads/2020/04/TIRIAS_Research-Lattice_Crosslink_NX.pdf (Page 1)

> In video surveillance and security applications, CrossLink-NX can be used for sensor aggregation and bridging, in addition to powering AI inferencing to preprocess the sensor data with functions such as facial recognition or presence detection.
>
> The chip can be used as an embedded vision co-processor to merge up to 14 sensors. It can also be used for video scaling, rotation, and color space conversions. With this chip, one sensor stream can be sent to multiple locations, which is useful in applications such as automotive, where cameras need to feed multiple processing units.

Source: https://www.tiriasresearch.com/wp-content/uploads/2020/04/TIRIAS_Research-Lattice_Crosslink_NX.pdf (Page 3).

> **1. Introduction**
>
> CrossLink-NX™ low power FPGA devices from Lattice Semiconductor help stretch the battery life of an application by lowering power consumption. CrossLink-NX features the ability to dynamically shut down used blocks in user mode. In addition, there is the ability to switch the device from High Performance (HP) to Low Power (LP) mode by changing the technology back bias via a performance grade selection.

Source: http://www.latticesemi.com/-/media/LatticeSemi/Documents/ApplicationNotes/PT2/FPGA-TN-02075-1-0-Power-Management-Calculation-for-CrossLinkNX-Devices.ashx?document_id=52795 (Page 5)

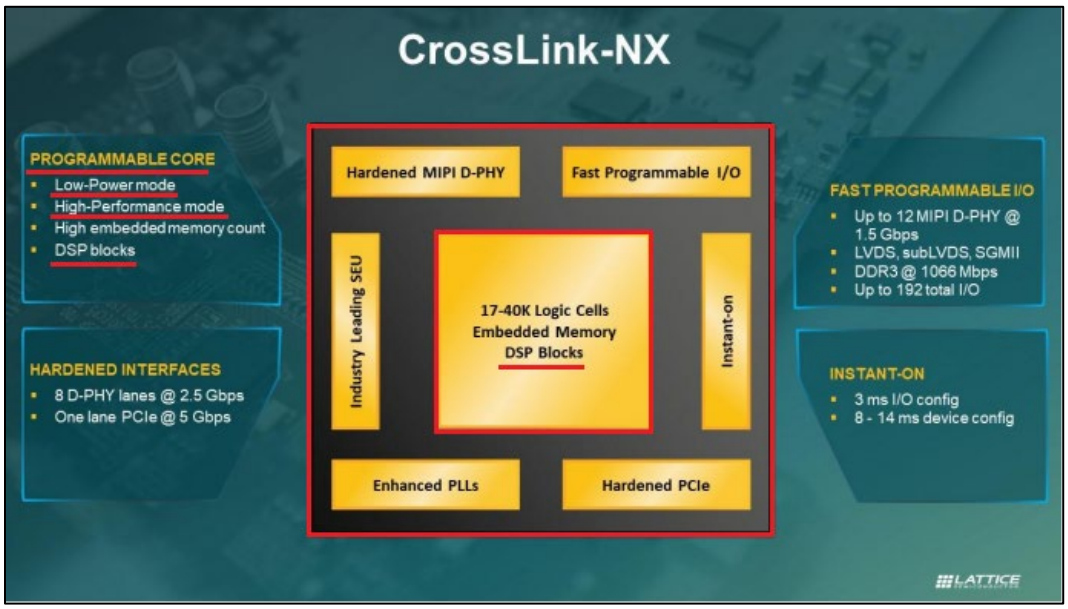
> **FD-SOI Enables Innovative New Power Modes and Higher Reliability**
>
> The use of FD-SOI allowed Lattice to create an innovative way for developers to manage power. The process allows the application of a voltage on the back side of the die (back-bias) that changes the threshold voltage. This allows Lattice to offer two operating modes – lower power mode and a higher performing mode. With power optimizations, the operating power at higher frequencies can be in the 200mW range, with only a few 10's of mW static leakage. Power consumption for CrossLink-NX FPGAs is up to 75 percent lower than other competing devices of a similar class.

Source: https://www.tiriasresearch.com/wp-content/uploads/2020/04/TIRIAS_Research-Lattice_Crosslink_NX.pdf (Page 4)

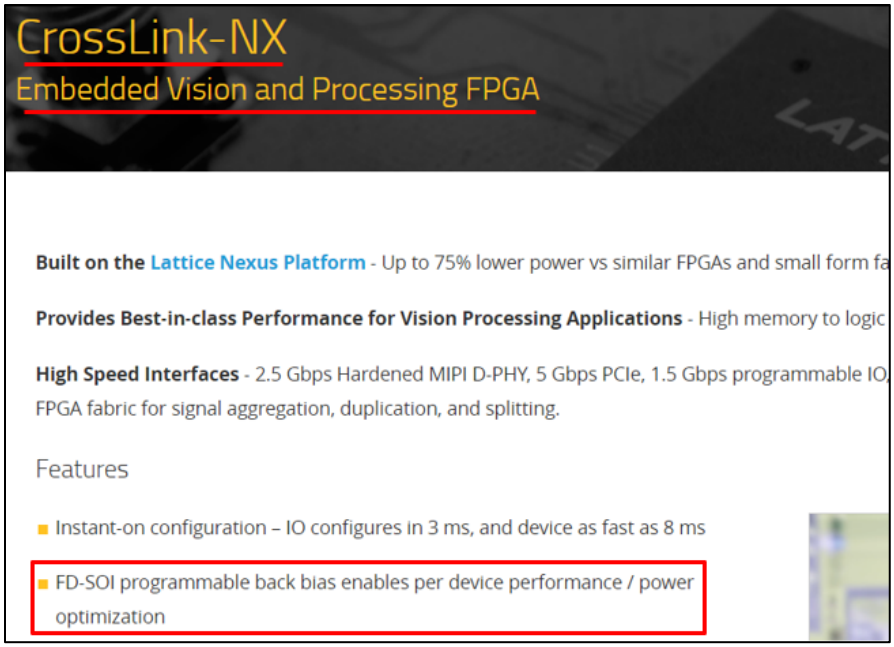
51. Lattice's CrossLink-NX family of FPGA devices includes means for accessing body biasing voltage information corresponding to the particular power condition.

52. For example, Lattice's CrossLink-NX family of FPGA devices includes logic cells and digital signal processing (DSP) blocks ("microprocessor") for applications like signal processing, Edge AI processing, video processing, etc. A CrossLink-NX device uses FD-SOI programmable back-bias technology for power optimization. The power mode of the device can

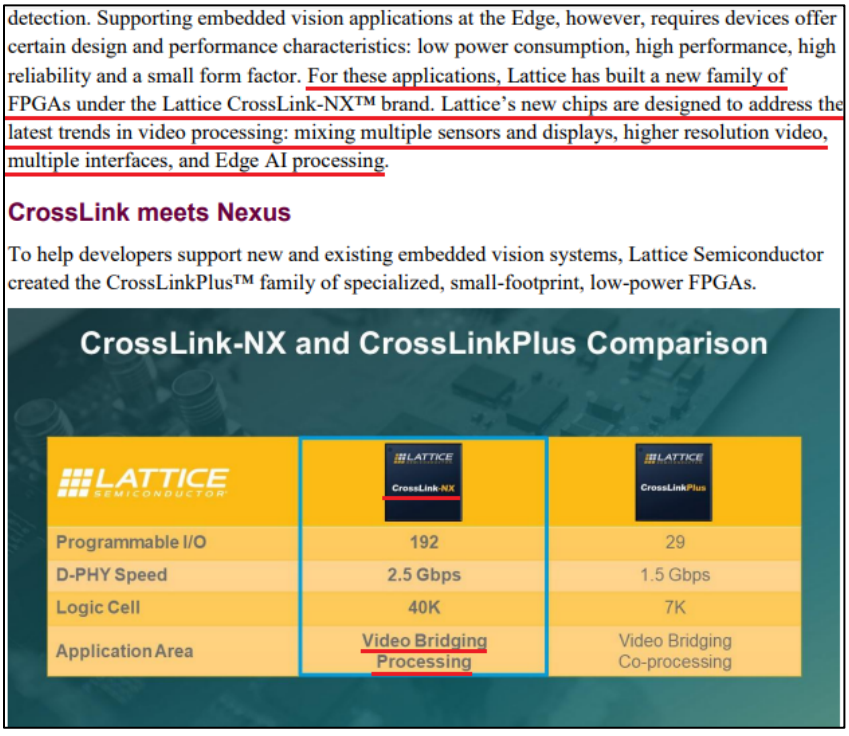
be switched from HP mode to LP mode by changing the value of the back-bias voltage ("body biasing voltage information"). Accordingly, a CrossLink-NX device includes means for accessing the programmed back-bias voltage of the LP mode ("said particular power condition").



Source: https://www.tiriasresearch.com/wp-content/uploads/2020/04/TIRIAS_Research-Lattice_Crosslink_NX.pdf (Page 6)



Source: https://www.latticesemi.com/Products/FPGAandCPLD/CrossLink-NX?ActiveTab=User+Manual



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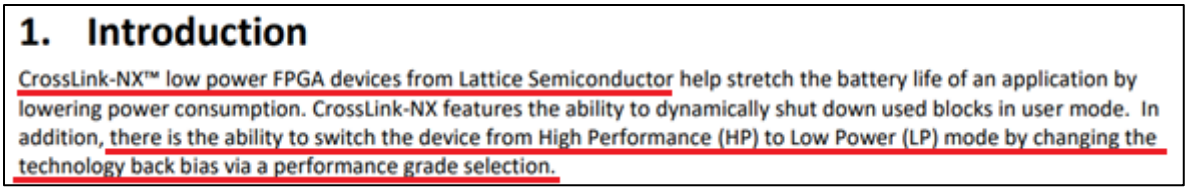

1. Introduction

CrossLink-NX™ low power FPGA devices from Lattice Semiconductor help stretch the battery life of an application by lowering power consumption. CrossLink-NX features the ability to dynamically shut down used blocks in user mode. In addition, there is the ability to switch the device from High Performance (HP) to Low Power (LP) mode by changing the technology back bias via a performance grade selection.

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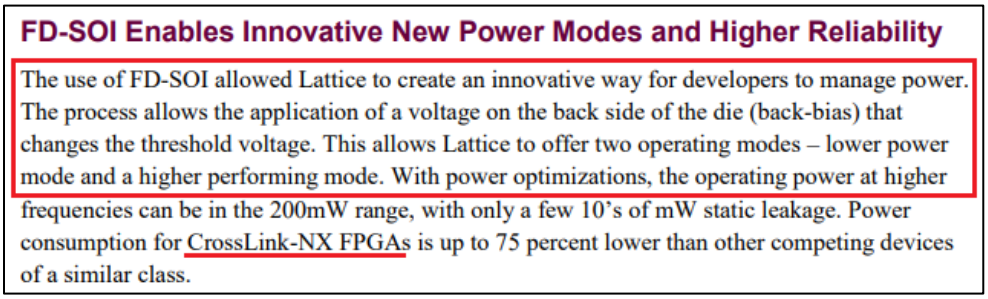


FD-SOI Enables Innovative New Power Modes and Higher Reliability

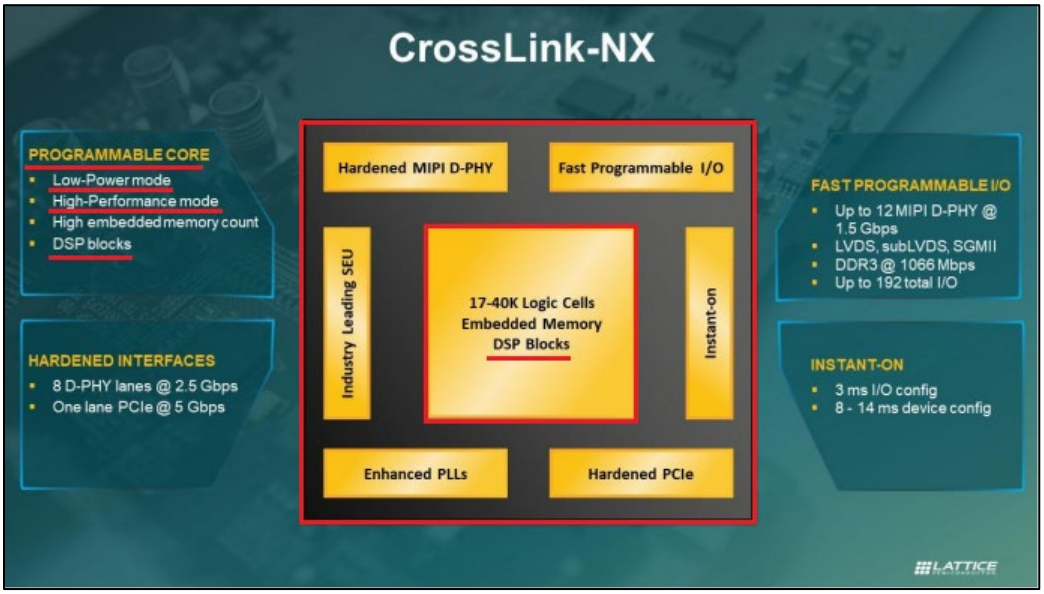
The use of FD-SOI allowed Lattice to create an innovative way for developers to manage power. The process allows the application of a voltage on the back side of the die (back-bias) that changes the threshold voltage. This allows Lattice to offer two operating modes – lower power mode and a higher performing mode. With power optimizations, the operating power at higher frequencies can be in the 200mW range, with only a few 10's of mW static leakage. Power consumption for CrossLink-NX FPGAs is up to 75 percent lower than other competing devices of a similar class.

Source: https://www.tiriasresearch.com/wp-content/uploads/2020/04/TIRIAS_Research-Lattice_Crosslink_NX.pdf (Page 4)

53. Lattice's CrossLink-NX family of FPGA devices includes means for commanding a voltage supply coupled to a body terminal of the microprocessor to generate a voltage corresponding to the body biasing voltage information corresponding to the particular power condition.

54. For example, Lattice's CrossLink-NX family of FPGA devices includes logic cells and digital signal processing (DSP) blocks ("microprocessor") for applications like signal processing, Edge AI processing, video processing, etc. A CrossLink-NX device uses FD-SOI programmable back-bias technology for power optimization. The power mode of the device can be switched from HP mode to LP mode by changing the value of the back-bias voltage ("body biasing voltage information"). Using the programmed back-bias voltage information of the LP mode ("said power condition"), a voltage supply coupled to the body terminal of the die can generate the corresponding body bias voltage based on a command. Accordingly, a CrossLink-

NX device includes means for commanding the voltage supply to generate a body biasing voltage corresponding to the body biasing voltage information.



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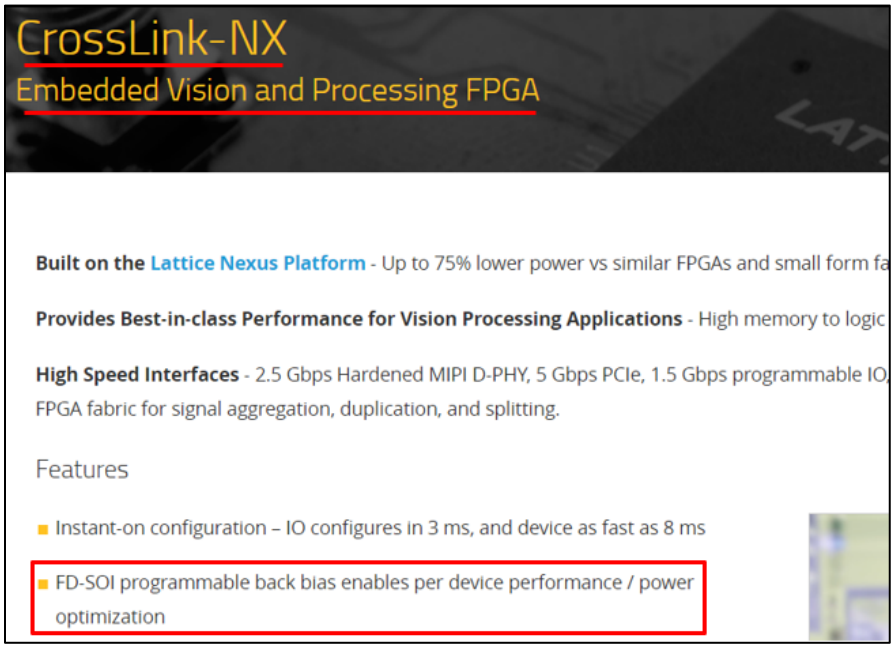
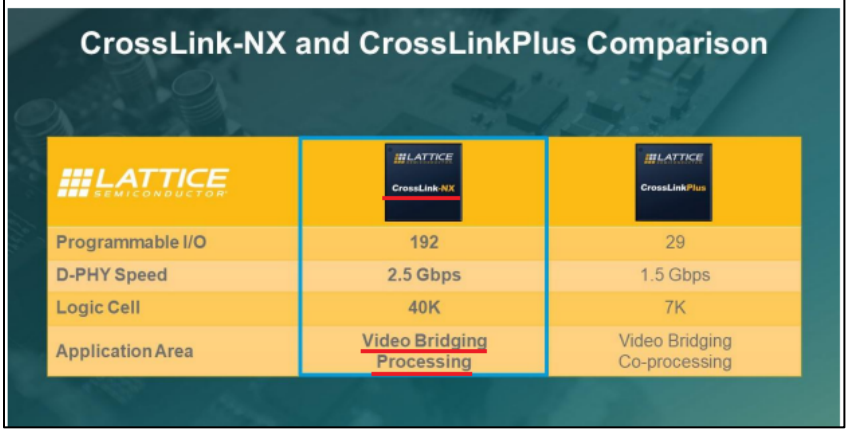


Source: https://www.latticesemi.com/Products/FPGAandCPLD/CrossLink-NX?ActiveTab=User+Manual

detection. Supporting embedded vision applications at the Edge, however, requires devices offer certain design and performance characteristics: low power consumption, high performance, high reliability and a small form factor. For these applications, Lattice has built a new family of FPGAs under the Lattice CrossLink-NX™ brand. Lattice's new chips are designed to address the latest trends in video processing: mixing multiple sensors and displays, higher resolution video, multiple interfaces, and Edge AI processing.

CrossLink meets Nexus

To help developers support new and existing embedded vision systems, Lattice Semiconductor created the CrossLinkPlus™ family of specialized, small-footprint, low-power FPGAs.



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1. Introduction

CrossLink-NX™ low power FPGA devices from Lattice Semiconductor help stretch the battery life of an application by lowering power consumption. CrossLink-NX features the ability to dynamically shut down used blocks in user mode. In addition, there is the ability to switch the device from High Performance (HP) to Low Power (LP) mode by changing the technology back bias via a performance grade selection.

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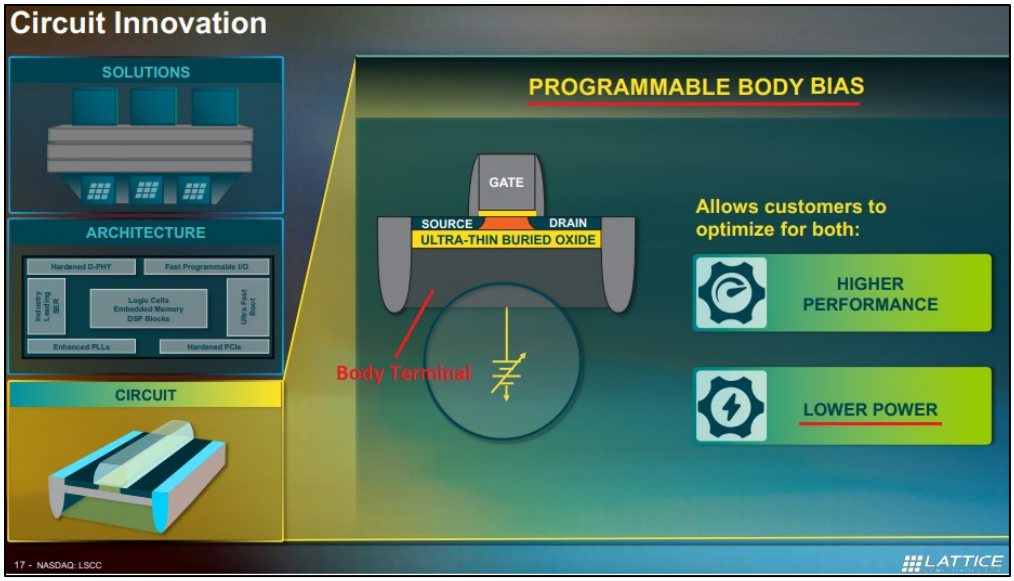

Source: http://ir.latticesemi.com/static-files/e5b359ca-385a-4c96-b697-f0f0ccbe00d6 (Slide 17)

> The first is that whole-chip electric field control is available through substrate biasing ('back-biasing') – allowing device speed to be traded off for power consumption. According to Hands, this is used during product manufacture, and is available to users (although not on-the-fly – device configuration must be re-loaded after a bias change).

Source: https://www.electronicsweekly.com/news/products/fpga-pld/lattice-moves-fd-soi-redesigns-fpgas-embedded-vision-edge-ai-2019-12/

55. Lattice has had knowledge of the '496 Patent at least as of the date when it was notified of the filing of this action.

56. Liberty Patents has been damaged as a result of the infringing conduct by Lattice alleged above. Thus, Lattice is liable to Liberty Patents in an amount that adequately compensates it for such infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

57. Liberty Patents and/or its predecessors-in-interest have satisfied all statutory obligations required to collect pre-filing damages for the full period allowed by law for infringement of the ’496 Patent.

ADDITIONAL ALLEGATIONS REGARDING INFRINGEMENT AND PERSONAL JURISDICTION

58. Lattice has also indirectly infringed the ’504 Patent, the ’156 Patent, and the ’496 Patent by inducing others to directly infringe the ’504 Patent, the ’156 Patent, and the ’496 Patent.

59. Lattice has induced the end users and/or Lattice’s customers to directly infringe (literally and/or under the doctrine of equivalents) the ’504 Patent, the ’156 Patent, and the ’496 Patent by using the accused products.

60. Lattice took active steps, directly and/or through contractual relationships with others, with the specific intent to cause them to use the accused products in a manner that infringes one or more claims of the patents-in-suit, including, for example, claim 9 of the ’504 Patent, claim 9 of the ’156 Patent, and claim 9 of the ’496 Patent.

61. Such steps by Lattice included, among other things, advising or directing customers and end users to use the accused products in an infringing manner; advertising and promoting the use of the accused products in an infringing manner; and/or distributing instructions that guide users to use the accused products in an infringing manner.

62. Lattice performed these steps, which constitute induced infringement, with the knowledge of the ’504 Patent, the ’156 Patent, and the ’496 Patent and with the knowledge that the induced acts constitute infringement.

63. Lattice was and is aware that the normal and customary use of the accused products by Lattice's customers would infringe the '504 Patent, the '156 Patent, and the '496 Patent. Lattice's inducement is ongoing.

64. Lattice has also induced its affiliates, or third-party manufacturers, shippers, distributors, retailers, or other persons acting on its or its affiliates' behalf, to directly infringe (literally and/or under the doctrine of equivalents) the '504 Patent, the '156 Patent, and the '496 Patent by importing, selling or offering to sell the accused products.

65. Lattice has a significant role in placing the accused products in the stream of commerce with the expectation and knowledge that they will be purchased by consumers in Texas and elsewhere in the United States.

66. Lattice purposefully directs or controls the making of accused products and their shipment to the United States, using established distribution channels, for sale in Texas and elsewhere within the United States.

67. Lattice purposefully directs or controls the sale of the accused products into established United States distribution channels, including sales to nationwide retailers. Lattice's established United States distribution channels include one or more United States based affiliates.

68. Lattice purposefully directs or controls the sale of the accused products online and in nationwide retailers, including for sale in Texas and elsewhere in the United States, and expects and intends that the accused products will be so sold.

69. Lattice purposefully places the accused products—whether by itself or through subsidiaries, affiliates, or third parties—into an international supply chain, knowing that the

accused products will be sold in the United States, including Texas. Therefore, Lattice also facilitates the sale of the accused products in Texas.

70. Lattice took active steps, directly and/or through contractual relationships with others, with the specific intent to cause such persons to import, sell, or offer to sell the accused products in a manner that infringes one or more claims of the ’504 Patent, the ’156 Patent, and the ’496 Patent.

71. Such steps by Lattice included, among other things, making or selling the accused products outside of the United States for importation into or sale in the United States, or knowing that such importation or sale would occur; and directing, facilitating, or influencing its affiliates, or third-party manufacturers, shippers, distributors, retailers, or other persons acting on its or its affiliates’ behalf, to import, sell, or offer to sell the accused products in an infringing manner.

72. Lattice performed these steps, which constitute induced infringement, with the knowledge of the ’504 Patent, the ’156 Patent, and the ’496 Patent, and with the knowledge that the induced acts would constitute infringement.

73. Lattice performed such steps in order to profit from the eventual sale of the accused products in the United States.

74. Lattice’s inducement is ongoing.

75. Lattice has also indirectly infringed by contributing to the infringement of the ’504 Patent, the ’156 Patent, and the ’496 Patent. Lattice has contributed to the direct infringement of the ’504 Patent, the ’156 Patent, and the ’496 Patent by the end user of the accused products.

76. The accused products have special features that are specially designed to be used in an infringing way and that have no substantial uses other than ones that infringe the ’504

Patent, the ’156 Patent, and the ’496 Patent, including, for example, claim 9 of the ’504 Patent, claim 9 of the ’156 Patent, and claim 9 of the ’496 Patent.

77. The special features include, for example, components and/or features for applying body biasing voltages during a power mode of a processor or other integrated circuit in a manner that infringes the ’504 Patent, the ’156 Patent, and the ’496 Patent.

78. These special features constitute a material part of the invention of one or more of the claims of the ’504 Patent, the ’156 Patent, and the ’496 Patent, and are not staple articles of commerce suitable for substantial non-infringing use.

79. Lattice’s contributory infringement is ongoing.

80. Lattice has had actual knowledge of the ’504 Patent, the ’156 Patent, and the ’496 Patent at least as of the date when it was notified of the filing of this action. Since at least that time, Lattice has known the scope of the claims of the ’504 Patent, the ’156 Patent, and the ’496 Patent, the products that practice the ’504 Patent, the ’156 Patent, and the ’496 Patent, and that Liberty Patents is the owner of the ’504 Patent, the ’156 Patent, and the ’496 Patent.

81. By the time of trial, Lattice will have known and intended (since receiving such notice) that its continued actions would infringe and actively induce and contribute to the infringement of one or more claims of the ’504 Patent, the ’156 Patent, and the ’496 Patent.

82. Furthermore, Lattice has a policy or practice of not reviewing the patents of others (including instructing its employees to not review the patents of others), and thus has been willfully blind of Liberty Patents’ patent rights. *See, e.g.*, M. Lemley, “Ignoring Patents,” 2008 Mich. St. L. Rev. 19 (2008).

83. Lattice's actions are at least objectively reckless as to the risk of infringing valid patents, and this objective risk was either known or should have been known by Lattice. Lattice has knowledge of the '504 Patent, the '156 Patent, and the '496 Patent.

84. Lattice's customers have infringed the '504 Patent, the '156 Patent, and the '496 Patent. Lattice has encouraged its customers' infringement.

85. Lattice's direct and indirect infringement of the '504 Patent, the '156 Patent, and the '496 Patent has been, and/or continues to be willful, intentional, deliberate, and/or in conscious disregard of Liberty Patents' rights under the patents-in-suit.

86. Liberty Patents has been damaged as a result of Lattice's infringing conduct alleged above. Thus, Lattice is liable to Liberty Patents in an amount that adequately compensates it for such infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

JURY DEMAND

Liberty Patents hereby requests a trial by jury on all issues so triable by right.

PRAYER FOR RELIEF

Liberty Patents requests that the Court find in its favor and against Lattice, and that the Court grant Liberty Patents the following relief:

a. Judgment that one or more claims of the '504 Patent, the '156 Patent, and the '496 Patent have been infringed, either literally and/or under the doctrine of equivalents, by Lattice and/or all others acting in concert therewith;

b. A permanent injunction enjoining Lattice and its officers, directors, agents, servants, affiliates, employees, divisions, branches, subsidiaries, parents, and all others acting in concert therewith from infringement of the '504 Patent, the '156 Patent, and the '496 Patent; or, in the alternative, an award of a reasonable ongoing royalty for future infringement of the '504

Patent, the '156 Patent, and the '496 Patent by such entities;

c. Judgment that Lattice account for and pay to Liberty Patents all damages to and costs incurred by Liberty Patents because of Lattice's infringing activities and other conduct complained of herein, including an award of all increased damages to which Liberty Patents is entitled under 35 U.S.C. § 284;

d. That Liberty Patents be granted pre-judgment and post-judgment interest on the damages caused by Lattice's infringing activities and other conduct complained of herein;

e. That this Court declare this an exceptional case and award Liberty Patents its reasonable attorney's fees and costs in accordance with 35 U.S.C. § 285; and

f. That Liberty Patents be granted such other and further relief as the Court may deem just and proper under the circumstances.

Dated: June 30, 2021

Respectfully submitted,

/s/ Zachariah S. Harrington

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