UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
WACO DIVISION

3D SURFACES, LLC, Plaintiff, v. DELL TECHNOLOGIES INC. and DELL INC. Defendants.	Civil Action No. 6:21-cv-1107 **JURY TRIAL DEMANDED**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff 3D Surfaces, LLC ("3D Surfaces" or "Plaintiff"), by and through its undersigned counsel, complains and alleges against Dell Technologies Inc. and Dell Inc. (collectively "Dell" or "Defendants") as follows:

NATURE OF THE ACTION

1. This is a civil action for infringement of U.S. Patent Nos. 7,245,299 and RE42,534 (collectively, "the Asserted Patents") arising under the patent laws of the United States, 35 U.S.C. §§ 1 et seq.

THE PARTIES

2. 3D Surfaces is a corporation organized under the laws of the State of California, with its principal place of business in Cupertino, California.

3. On information and belief, defendant Dell Technologies Inc. is a Delaware corporation with its principal place of business at One Dell Way, Round Rock, Texas 78682.

4. On information and belief, defendant Dell Inc. is a Delaware corporation with its principal place of business at One Dell Way, Round Rock, Texas 78682.

JURISDICTION AND VENUE

5. This Court has jurisdiction over the subject matter of this action under 28 U.S.C. §§ 1331 and 1338(a).

6. This Court has personal jurisdiction over Dell pursuant to due process and/or the Texas Long Arm Statute because Dell has committed and continues to commit acts of patent infringement, including acts giving rise to this action, within the State of Texas and this District, and because Dell recruits Texas residents, directly or through an intermediary located in this state, for employment inside or outside this state. The Court's exercise of jurisdiction over Dell would not offend traditional notions of fair play and substantial justice because Dell has established minimum contacts with the forum.

7. Venue is proper in this judicial district pursuant to 28 U.S.C. §§ 1391 and 1400 because a substantial part of the events or omissions giving rise to the claims occurred in this District, and Dell has committed acts of infringement and has a regular and established place of business in this District.

8. Dell has committed acts of infringement in this District, directly and/or through intermediaries, by, among other things, making, using, offering to sell, selling, and/or importing products and/or services that infringe the Asserted Patents, as alleged herein.

9. Dell has regular and established places of business in this District including a shared corporate office at One Dell Way, Round Rock, Texas 78682. Dell is also registered to do business in Texas.

3D SURFACES' ASSERTED PATENTS

10. On July 17, 2007, the United States Patent Office issued U.S. Patent No. 7,245,299, titled "Bicubic Surface Real-Time Tesselation Unit" (the "'299 patent"). A true and correct copy of the '299 patent is attached hereto as Exhibit A.

11. On July 12, 2011, the United States Patent Office issued U.S. Patent No.

RE42,534, titled "Bicubic Surface Real-Time Tesselation Unit" (the "'534 patent"). A true and correct copy of the '534 patent is attached hereto as Exhibit B.

12. 3D Surfaces is the owner of all right, title, and interest in and to each of the Asserted Patents with full and exclusive right to bring suit to enforce the Asserted Patents, including the right to recover for past damages and/or royalties prior to the expiration of the Asserted Patents.

13. The Asserted Patents are valid and enforceable.

BACKGROUND

14. Dell manufactures, uses, imports, offers for sale, and/or sells products, including computers, that perform real-time tessellation of graphics objects ("Accused Products"). The Accused Products include, but are not limited to, laptops (*e.g.*, Latitude, Vostro, Inspiron, XPS, G-Series, Rugged, Chromebook Enterprise, Education, and Alienware), tablets and 2-in-1s (*e.g.*, XPS, Latitude, Inspiron, Rugged, Chromebook Enterprise, and Education) and desktops (*e.g.*, Alienware, OptiPlex and OptiPlex Ultra) that support DirectX 11 and higher 3D graphics technology.

COUNT I

Infringement of the '299 Patent

15. 3D Surfaces re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

16. In violation of 35 U.S.C. § 271(a), Dell has infringed and continues to infringe the '299 patent by making, using, selling, offering for sale, and/or importing into the United States, without authority, the Accused Products which contain each and every limitation of claim 11 of the '299 patent. Dell has infringed and contines to infringe literally and/or under the doctrine of equivalents.

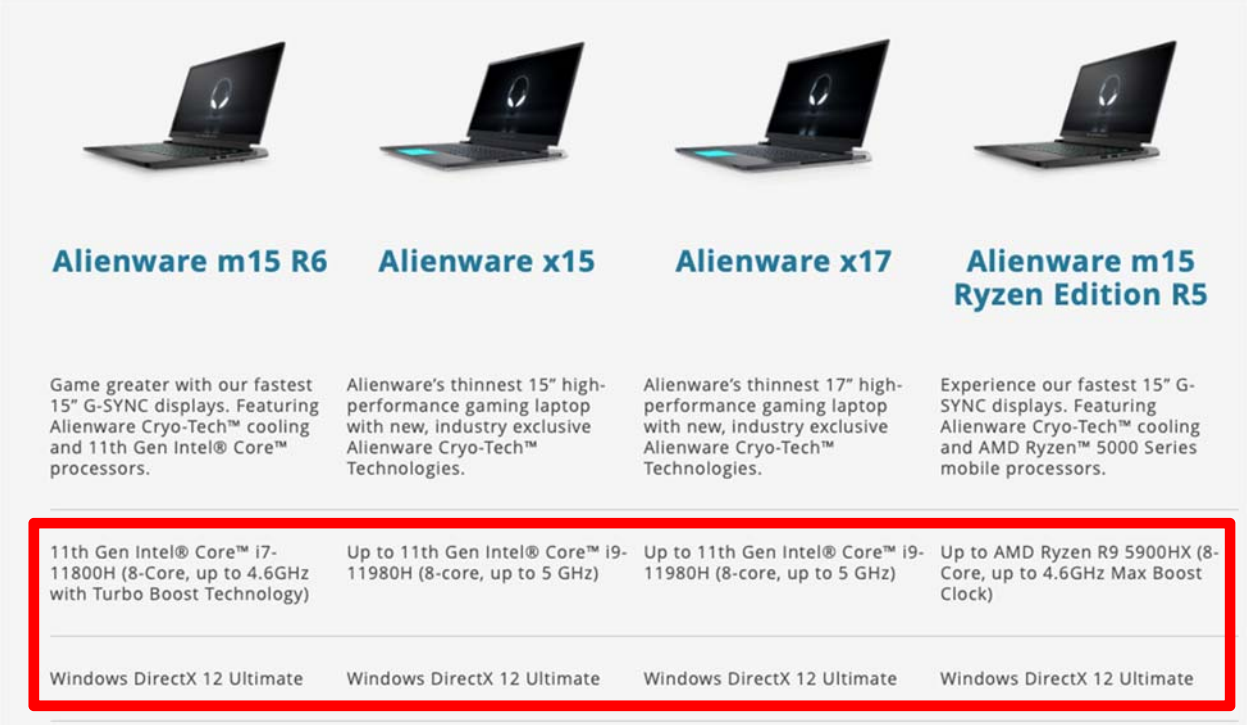
17. The Accused Products are a system comprising a processor and a graphics

processing unit (GPU). The Accused Products support DirectX 11 and higher 3D graphics technology. By way of example, the Accused Products include AMD processors or Intel Core processors (4th gen and later) with integrated GPUs that support DirectX 11.1 and higher. *See, e.g.*,

Table 1.1: Comparing the best of Intel 3rd generation with Intel 4th generation processor graphics

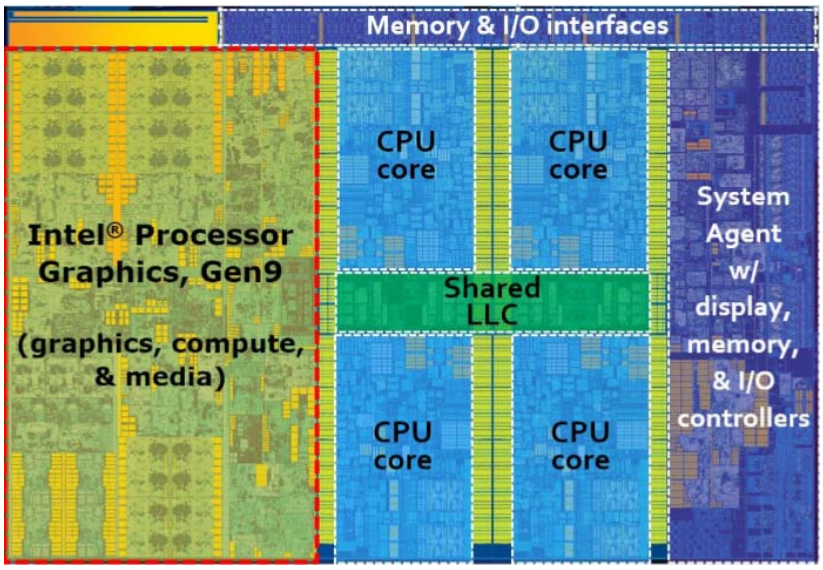
	3rd gen Intel® Core™ processor	4th gen Intel® Core™ processor		
	Intel® HD Graphics 4000	Intel® HD Graphics	Intel® HD Graphics 4200/4400/4600	Intel® Iris™ Pro Graphics 5200, Intel™ Iris™ Graphics 5100, Intel® HD Graphics 5000
APIs	DirectX* 11.0 DirectX Shader Model 5.0 OpenGL* 4.0 OpenCL* 1.1	DirectX* 11.1 DirectX Shader Model 5.0 OpenGL* 4.2 OpenCL* 1.2		

https://www.intel.com/content/dam/develop/external/us/en/documents/4th-gen-core-graphics-dev-guide.pdf at 3.



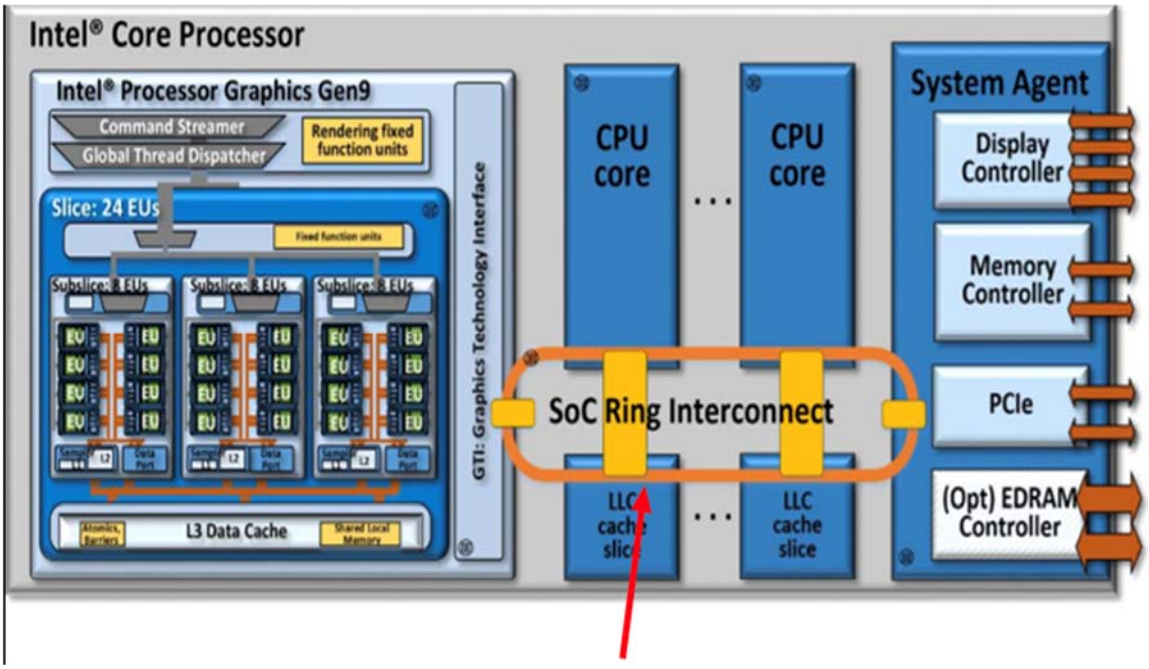
https://www.dell.com/en-us/gaming/alienware-laptops?~ck=mn.

18. For example, each of the Accused Products is a computer with a microprocessor (*e.g.*, an Intel processor) that includes both a CPU (identified as the 4 CPU cores above) which runs applications and a graphics processing unit GPU (highlighted by the red dashed box)) on the same semiconductor die. The GPU is used to render objects output to it by applications running on the CPU (*e.g.*, 3D image objects from game software).



Die Image of an Intel microprocessor with a Gen9 integrated graphics processor (The Compute Architecture of Intel Processor Graphics Gen9, Version 1.0 at 3)

19. The graphics processing unit (GPU) is coupled to the processor, and the GPU includes a transform unit, a lighting unit, a renderer unit, and a tessellate unit coupled between the transform unit and the lighting unit. For example, each of the Accused Products includes a microprocessor that has a bus – shown as the "SoC Ring Interconnect" below – that connects the CPU to the GPU and over which data, including objects to be rendered, are transmitted to the GPU from the CPU running an application, such as a game.



"4.2 RING INTERCONNECT The **on-die bus** between CPU cores, caches, and Intel processor graphics is a ring-based topology with dedicated local interfaces for each connected "agent". This SoC ring interconnect is a bi-directional ring that has a 32-byte wide data bus, with separate lines for request, snoop, and acknowledge. Every on-die CPU core is regarded as a unique agent. Similarly, Intel processor graphics is treated as a unique agent on the interconnect ring"

High level architecture of an Intel microprocessor with a Gen9 integrated graphics processor (The Compute Architecture of Intel Processor Graphics Gen9, Version 1.0 at 3-4) (emphasis added)

20. The GPU includes a transform unit, a lighting unit, a renderer unit, and a tessellate unit coupled between the transform unit and the lighting unit. Objects to be rendered are sent from the CPU to the GPU.

> by a collection of primitives. In most cases, primitives are triangles defined by vertices. Vertex information consists of geometric position and further attributes such as normal vector, texture coordinates, color, or opacity.
>
> Primitives are sent from CPU to GPU as a stream of vertices, which are then transformed by the *vertex processor*. In the traditional fixed-function

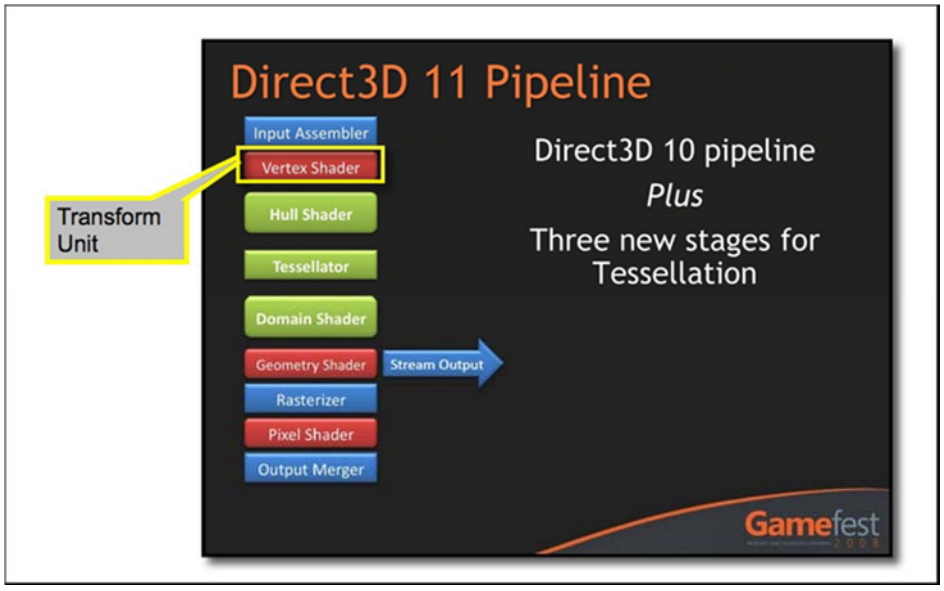
Daniel Weiskopf., GPU-based interactive visualization techniques. Springer-Verlag New York, LLC. p. 4

"The 3DPRIMITIVE command (defined in the VF Stage chapter) is used to submit 3D primitives to be processed by the 3D pipeline. Typically the processing results in the rendering of pixel data into the render targets, but this is not required. . . . In this spec, we will try to avoid ambiguity by using the term 'object' to represent the basic shapes (point, line, triangle), and 'topology' to represent input geometry (strips, lists, etc.)."

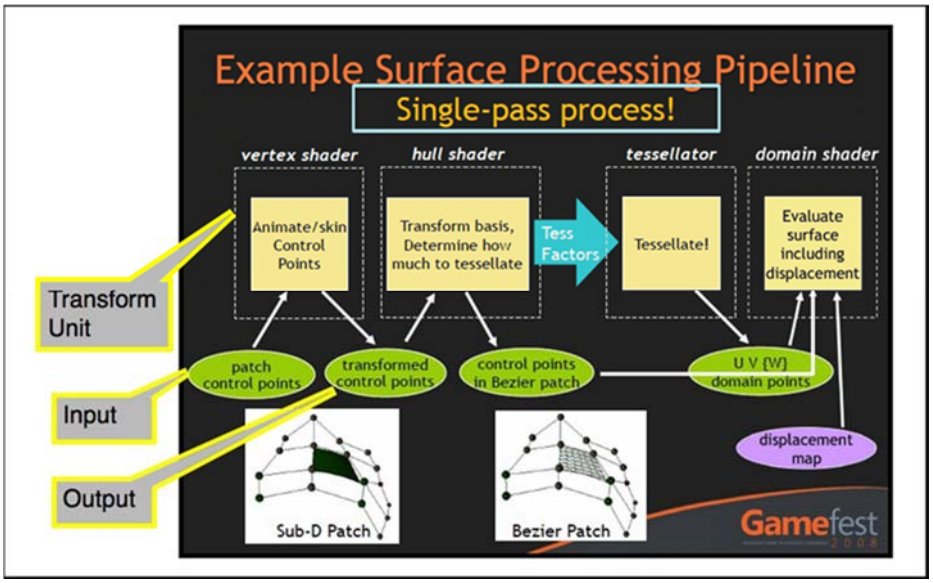
Intel® Open Source HD Graphics, Intel Iris™ Graphics, and Intel Iris™ Pro Graphics Programmer's Reference Manual For the 2015 - 2016 Intel Core™ Processors, Celeron™ Processors, and Pentium™ Processors based on the "Skylake" Platform, Volume 7: 3D-Media-GPGPU, page 419, May 2016, Revision 1.0 l; Vol 7 ("Intel Gen9 PRM").

21. The Accused Products' microprocessor transmits the objects to be rendered (primitives) to the GPU 3D Pipeline.

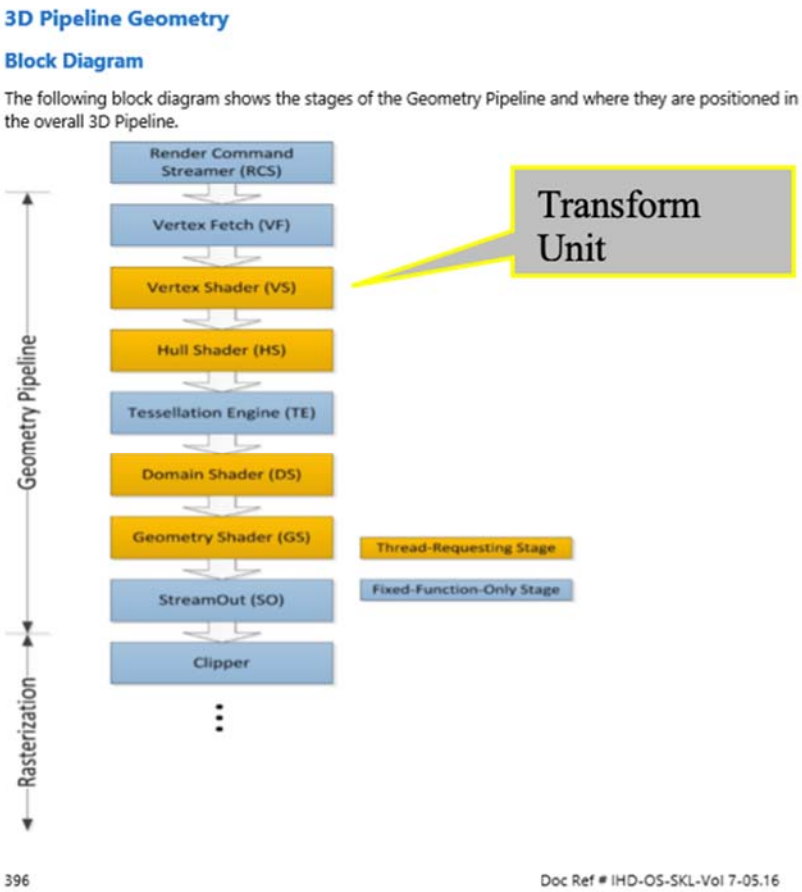
22. The graphics pipeline of a GPU with DirectX 11 (and higher) support contains a transform unit, which is referred to as a Vertex Shader in DirectX 11 (and higher). The Vertex Shader takes control points of a patch as an input and transforms those control points into transformed control objects (*e.g.*, vertices) that can be further processed by the real-time tessellation unit, which is the function of the transform unit of the '299 patent. In the '299 patent, the transform unit transforms control points into transformed data (*i.e.*, vertices) that can be acted upon by the tessellation unit. *See, e.g.*, '299 patent, col. 7:9-14.



Introduction to Direct 3D 11 Graphics Pipeline, Gamefest Microsoft Game Technology Conference, Microsoft Corp, p. 12



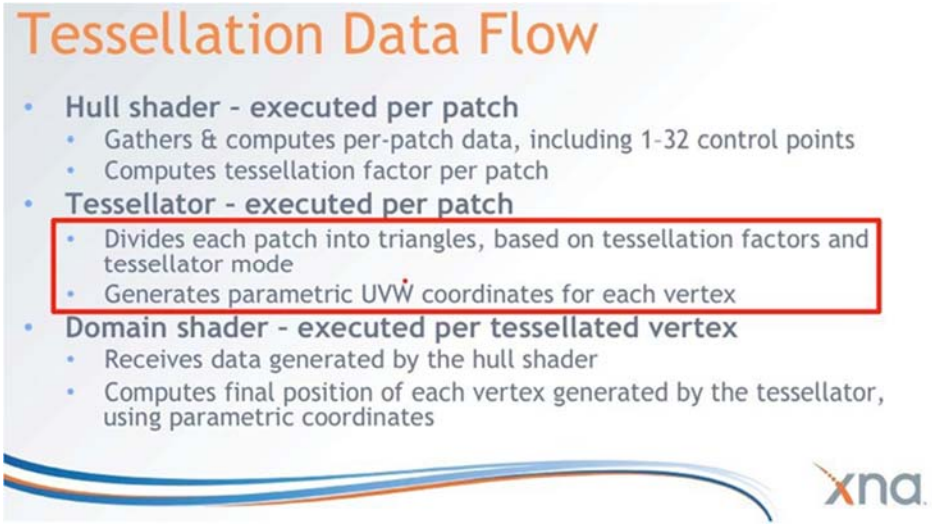
Introduction to Direct 3D 11 Graphics Pipeline, Gamefest Microsoft Game Technology Conference, Microsoft Corp, p. 17



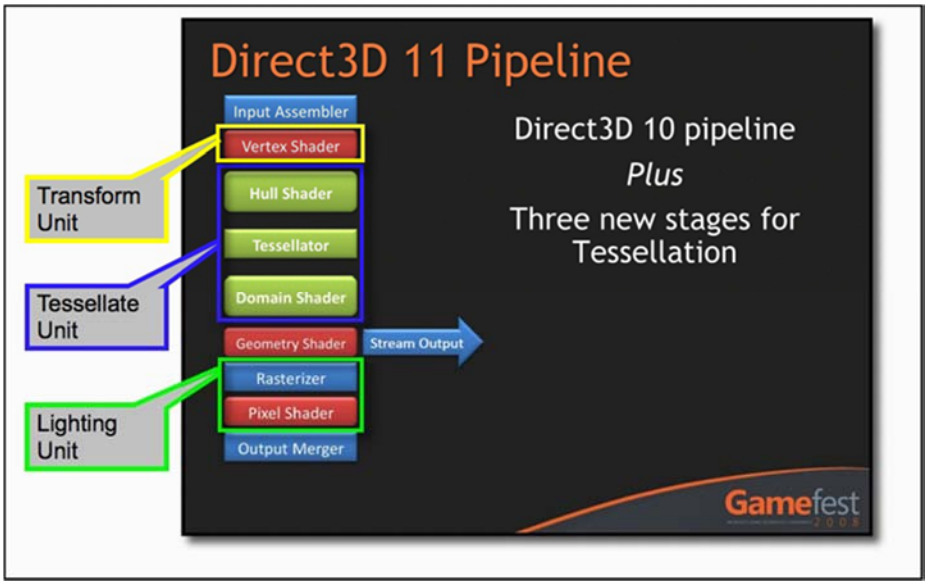
"The Vertex Shader stage is responsible for processing (shading) incoming vertices by passing them to VS threads."

Intel Gen9 PRM at pages 392, 396.

23. The graphics pipeline of a GPU with DirectX 11 (and higher) support contains a tessellate unit, which comprises the Hull Shader, Tessellator and Domain Shader (Three new stages for Tessellation) in DirectX 11 (and higher), and the tessellation unit is coupled between the transform unit and lighting unit such that transformed primitive objects are passed through the pipeline from the Vertex Shader to the tesselate unit, and the output of the tesselate unit flows to the lighting unit.

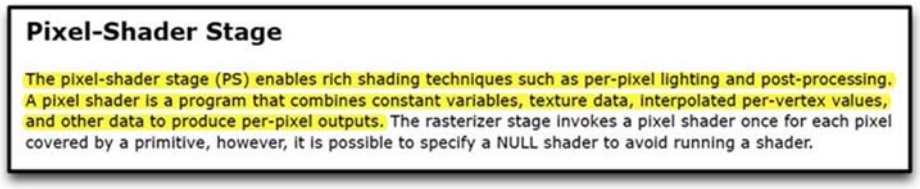


Direct3D 11 Tessellation Deep Dive, XNA, Microsoft Corp, 2009, p. 9

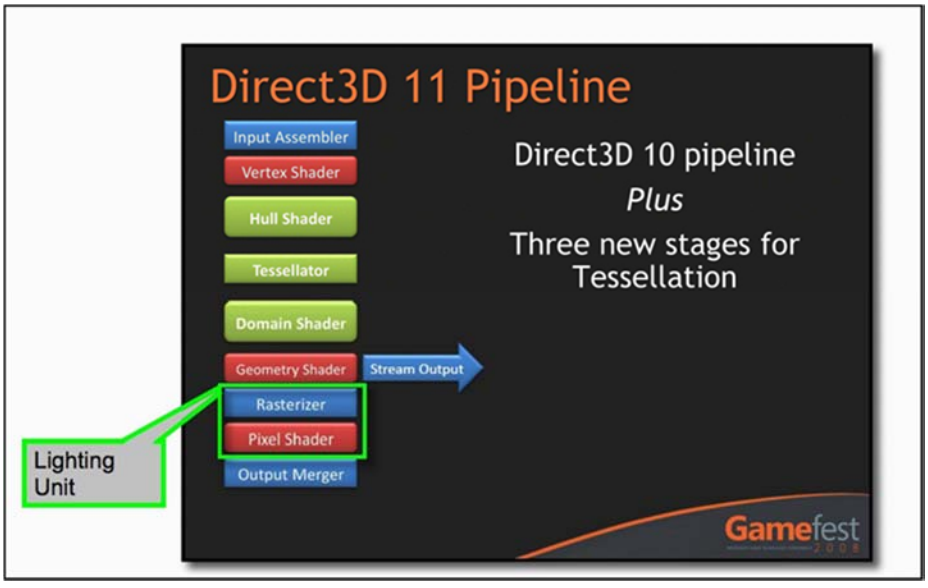


Introduction to Direct 3D 11 Graphics Pipeline, Gamefest Microsoft Game Technology Conference, Microsoft Corp, p. 12

24. The graphics pipeline of a GPU with DirectX 11 (and higher) support (including the Accused Dell Products) contains a lighting unit (called Rasterizer and Pixel Shader in DirectX 11 (and higher)) that lights triangles based on data of previous stages (tessellation). The rasterizer generates the interpolated per-vertex values and the Pixel Shader generates lighting calculations by using the interpolated per-vertex values.

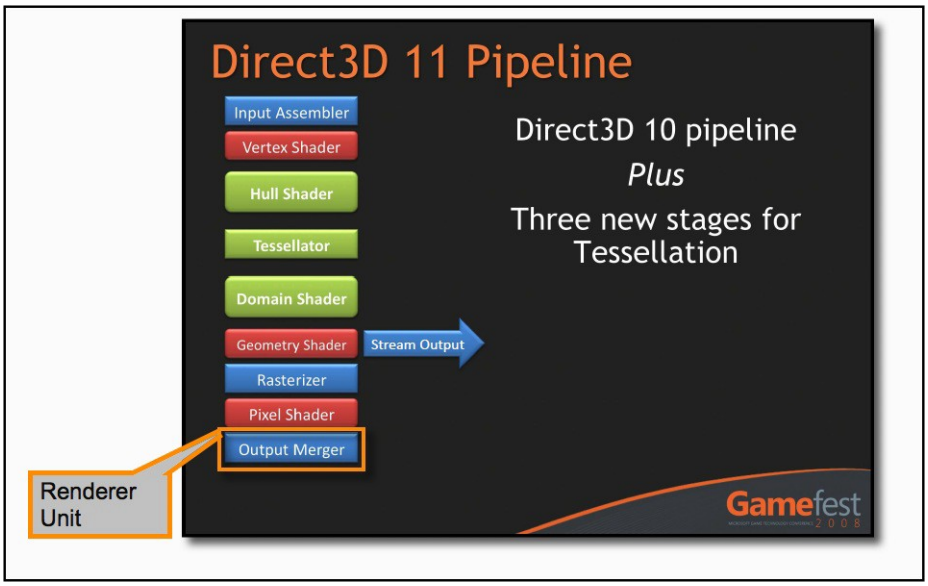


Shader Stages (Direct3D 10), DirectX SDK, Microsoft Corp, p. 4

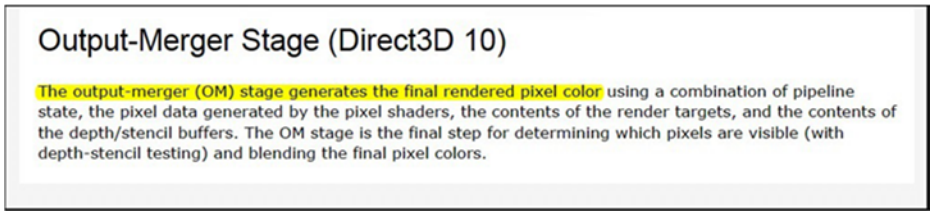


Introduction to Direct 3D 11 Graphics Pipeline, Gamefest Microsoft Game Technology Conference, Microsoft Corp, p. 12

25. The graphics pipeline of a GPU with DirectX 11 (and higher) support contains a renderer unit, which is referred to as Output Merger/ Render Backend in DirectX 11 (and higher). The Output Merger (rendering unit) generates the final rendered pixel color.

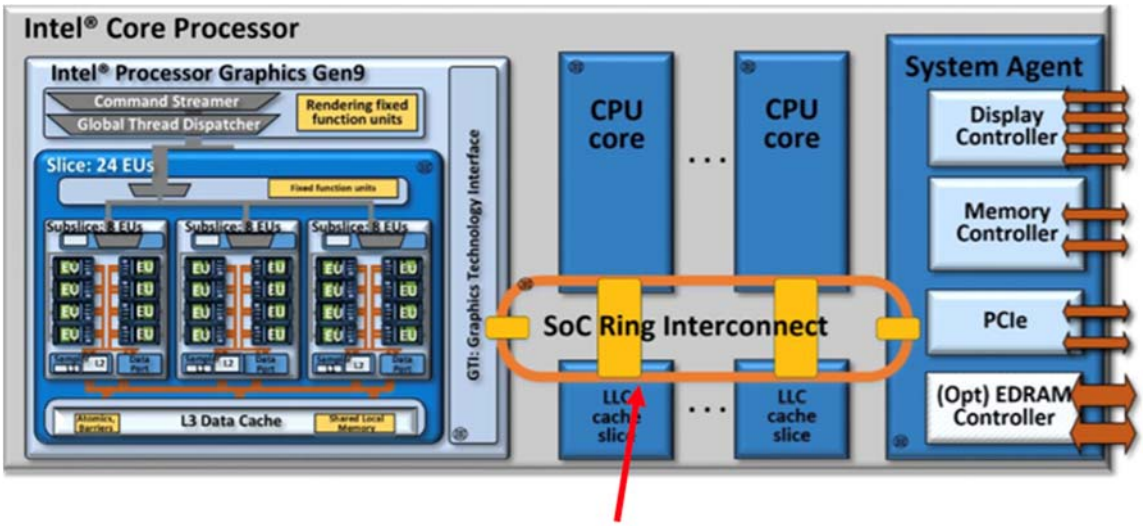


Introduction to Direct 3D 11 Graphics Pipeline, Gamefest Microsoft Game Technology Conference, Microsoft Corp, p. 12



Output Merger Stage (Direct3D 10), DirectX SDK, Microsoft Corp, p. 1

26. The processor in the Accused Products transmits objects to be rendered to the GPU as control points. Each of the Accused Products includes a microprocessor that has a bus – shown as the "SoC Ring Interconnect" – that connects the CPU to the GPU and over which data, including objects to be rendered, are transmitted to the GPU from the CPU running an application, such as a game.



High level architecture of an Intel microprocessor with a Gen9 integrated graphics processor (The Compute Architecture of Intel Processor Graphics Gen9, Version 1.0 at 3-4)

27. Objects to be rendered (primitives) are sent from a CPU to a GPU as control points.

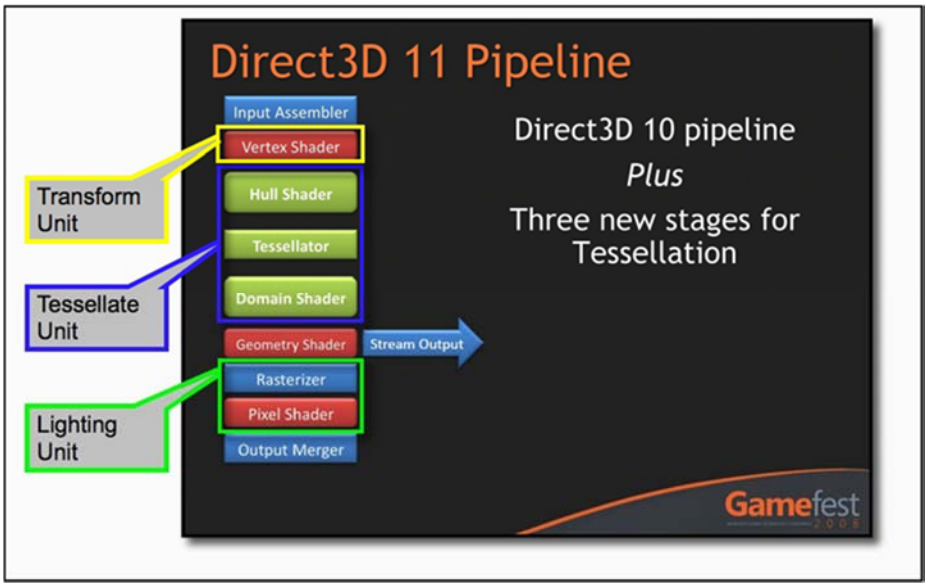
> by a collection of primitives. In most cases, primitives are triangles defined by vertices. Vertex information consists of geometric position and further attributes such as normal vector, texture coordinates, color, or opacity.
>
> Primitives are sent from CPU to GPU as a stream of vertices, which are then transformed by the *vertex processor*. In the traditional fixed-function

Daniel Weiskopf., GPU-based interactive visualization techniques. Springer-Verlag New York, LLC, p. 4

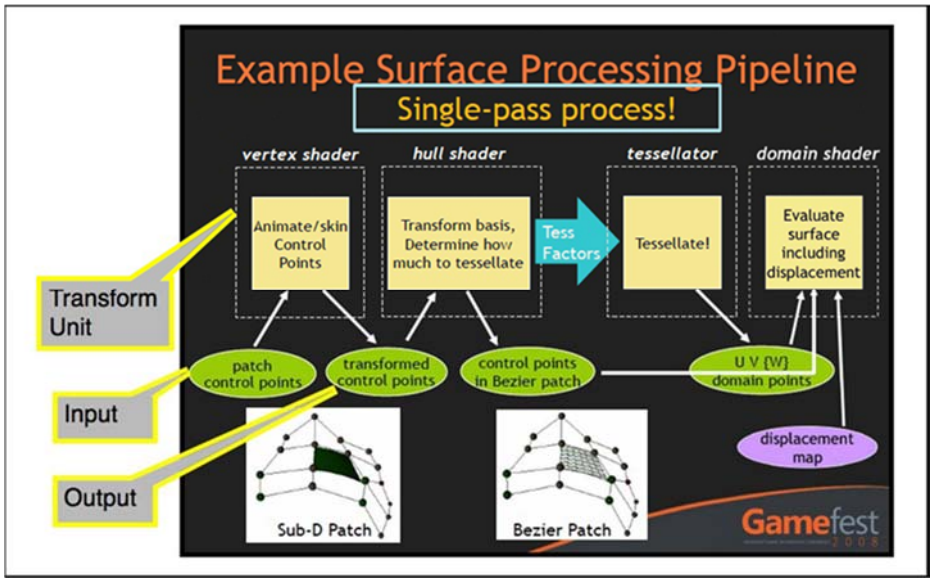
"The 3DPRIMITIVE command (defined in the VF Stage chapter) is used to submit 3D primitives to be processed by the 3D pipeline. Typically the processing results in the rendering of pixel data into the render targets, but this is not required. . . . In this spec, we will try to avoid ambiguity by using the term 'object' to represent the basic shapes (point, line, triangle), and 'topology' to represent input geometry (strips, lists, etc.)."

Intel® Open Source HD Graphics, Intel Iris™ Graphics, and Intel Iris™ Pro Graphics Programmer's Reference Manual For the 2015 - 2016 Intel Core™ Processors, Celeron™ Processors, and Pentium™ Processors based on the "Skylake" Platform, Volume 7: 3D-Media-GPGPU, page 419, May 2016, Revision 1.0 l; Vol 7 ("Intel Gen9 PRM")

28. The transform unit in the Accused Products transforms the control points.

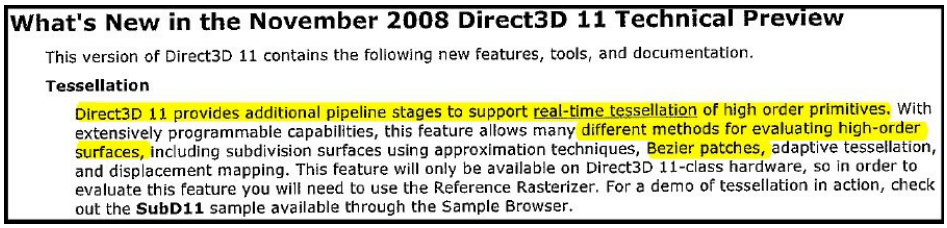


Introduction to Direct 3D 11 Graphics Pipeline, Gamefest Microsoft Game Technology Conference, Microsoft Corp, p. 12



Introduction to Direct 3D 11 Graphics Pipeline, Gamefest Microsoft Game Technology Conference, Microsoft Corp, p. 17

29. The tessellate unit in the Accused Products executes a first set of instructions for tessellating both rational and non-rational object surfaces in real-time. The tessellate unit (Hull Shader, Tessellator and Domain Shader) performs real-time tessellation of Bezier object surfaces (Bezier patches, Bezier rational patches and any other types of bicubic or subdivision patches such as beta-splines and NURBS).



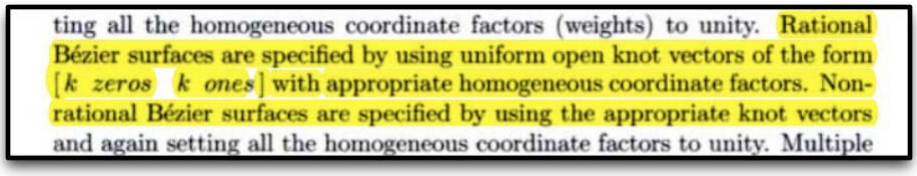
What's New in the November 2008 Direct3D 11 Technical Preview

This version of Direct3D 11 contains the following new features, tools, and documentation.

Tessellation

Direct3D 11 provides additional pipeline stages to support real-time tessellation of high order primitives. With extensively programmable capabilities, this feature allows many different methods for evaluating high-order surfaces, including subdivision surfaces using approximation techniques, Bezier patches, adaptive tessellation, and displacement mapping. This feature will only be available on Direct3D 11-class hardware, so in order to evaluate this feature you will need to use the Reference Rasterizer. For a demo of tessellation in action, check out the **SubD11** sample available through the Sample Browser.

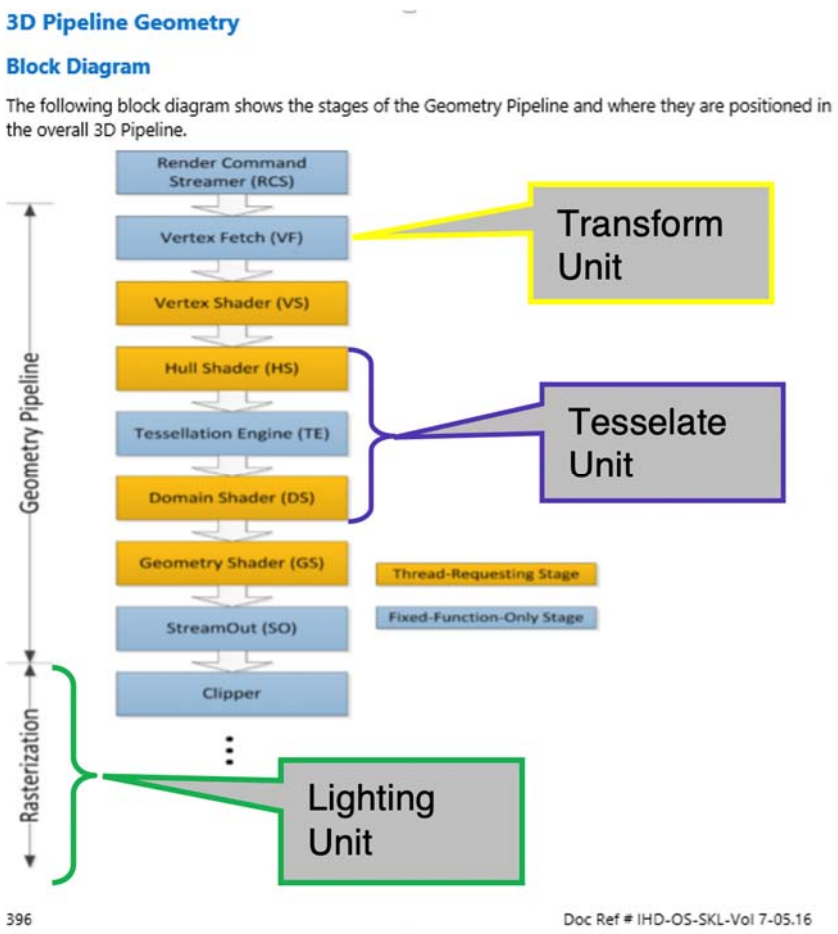
What's New in the November 2008 Direct3D 11 Technical Preview, DirectX SDK, Microsoft Corp,
p. 1



ting all the homogeneous coordinate factors (weights) to unity. Rational Bézier surfaces are specified by using uniform open knot vectors of the form [*k zeros* *k ones*] with appropriate homogeneous coordinate factors. Non-rational Bézier surfaces are specified by using the appropriate knot vectors and again setting all the homogeneous coordinate factors to unity. Multiple

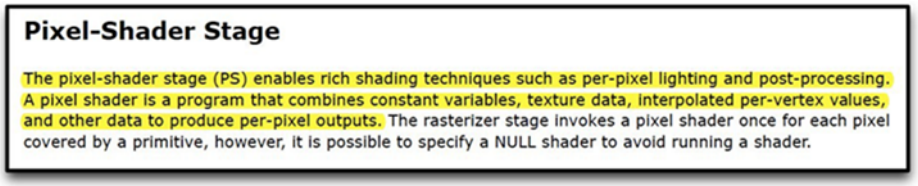
David F. Rogers., An introduction to NURBS: with historical perspective. Morgan Kaufmann Publishers, Inc., p. 263

30. In the ’299 patent, the tesselate unit is coupled between the transform unit and the lighting unit if for a particular object (data) that is ultimately rendered by the GPU, the object is first processed by the transform unit, then the tesselate unit and then the lighting unit. *See e.g.*, ’299 patent, Fig. 3 and related description. In the Intel 3D Pipeline, any PATCHLIST_n topology data is processed in this sequence before it is rendered. The 3D graphics pipeline of the Accused Products supports DirectX 11 (and higher) and comprises a tesselate unit that is functionally coupled between the transform unit and the lighting unit.

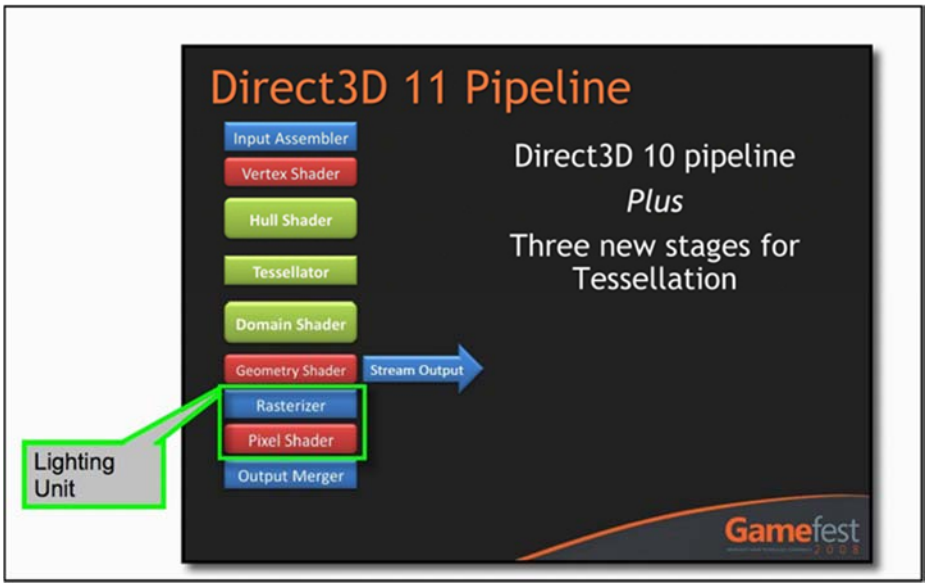


Intel Gen9 PRM at page 396.

31. The lighting unit in the Accused Products lights vertices of the triangles. The graphics pipeline of a GPU with DirectX 11(and higher) support (including the Accused Products) contains a lighting unit (called Rasterizer and Pixel Shader in DirectX 11 (and higher)) that lights triangles based on data of previous stages (tessellation).

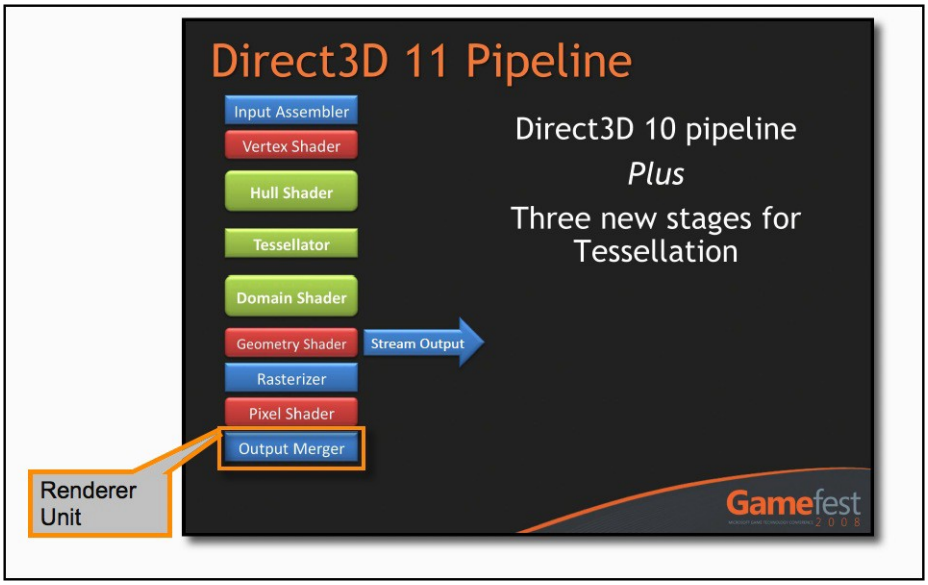


Shader Stages (Direct3D 10), DirectX SDK, Microsoft Corp, p. 4

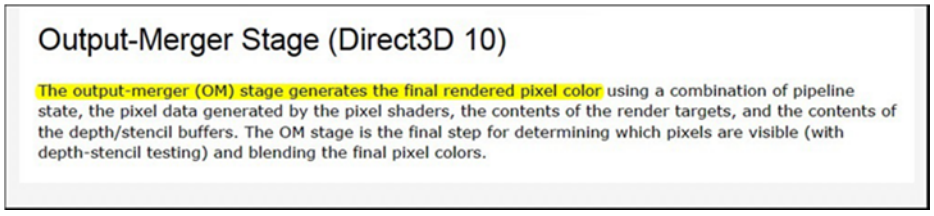


Introduction to Direct 3D 11 Graphics Pipeline, Gamefest Microsoft Game Technology Conference, Microsoft Corp, p. 12

32. The renderer unit in the Accused Products renders the triangles by executing a second set of instructions. The graphics pipeline of a GPU with DirectX 11 (and higher) support contains a renderer unit, which is referred to as Output Merger/ Render Backend in DirectX 11 (and higher). The Output Merger (rendering unit) generates the final rendered pixel color and therefore is the renderer unit. These processes involve software and/or firmware functionality performed "by executing a second set of instructions," as recited in the claim.



Introduction to Direct 3D 11 Graphics Pipeline, Gamefest Microsoft Game Technology Conference, Microsoft Corp, p. 12



Output Merger Stage (Direct3D 10), DirectX SDK, Microsoft Corp, p. 1

33. Dell was made aware of the '299 patent and its infringement thereof at least as early as December 23, 2009, when 3D Surfaces provided notice of Dell's infringement of the '299 patent to Michael S. Dell, the founder, chairman and CEO of Dell. After at least the time Dell received notice, Dell induced and continues to induce others to infringe at least one claim of the '299 patent under 35 U.S.C. § 271(b) by, among other things, and with specific intent or willful blindness, actively aiding and abetting others to infringe, including but not limited to Dell's clients, customers, and end users, whose use of the Accused Product constituted direct infringement of at least one claim of the '299 patent. In particular, Dell's actions that aided and abetted others such as customers and end users to infringe included advertising and distributing the Accused Products and providing instruction materials, training, and services regarding the Accused Products. *See e.g.*,https://www.dell.com/support/home/en-us?app=drivers&~ck=mn; https://www.dell.com/support/contents/en-us/article/product-support/self-support-knowledgebase/dell-gaming/gaming-support; www.dell.com/support; https://www.dell.com/en-us/gaming/alienware-laptops?gacd=9614064-1054-5763017-266796622-0&dgc=st&ds_rl=1286018&msclkid=98a3b4adb85b12500fefd5f62840ec09&gclid=98a3b4adb85b12500fefd5f62840ec09&gclsrc=3p.ds&nclid=TF9OEC8yMUdWryaTl9NJuror7mX02yDYnqyPD5BuCHY-l30o3WLoDqZKec3Pd-gn;https://www.dell.com/en-us/shop/servicesforhome/cp/supportforgaming?~ck=mn. Dell engaged in such actions with specific intent to cause infringement or with willful blindness to the resulting infringement because

Dell had actual knowledge of the '299 patent and knowledge that its acts were inducing infringement of the '299 patent since at least the date Dell received notice that such activities infringed the '299 patent.

34. Dell is liable as a contributory infringer of the '299 patent under 35 U.S.C. § 271(c) by having offered to sell, sold and imported and continuing to offer to sell, selling and importing into the United States computers including CPU and GPUs coupled together including a graphics pipeline having a tessellation unit that is operatively coupled between a transform unit and a lighting unit to be especially made or adapted for use in an infringement of the '299 patent. The Accused Product is a material component for use in practicing the '299 patent and is specifically made and is not a staple article of commerce suitable for substantial non-infringing use.

35. Upon information and belief, since the date of its receipt of notice, Dell's infringement of the '299 patent was willful and intentional under the standard announced in *Halo Elecs., Inc. v. Pulse Elecs., Inc.*, 136 S.Ct. 1923, 195 L.Ed 2d 278 (2016). From at least December 23, 2009, Dell willfully infringed the '299 patent by refusing to take a license and continuing to make, use, test, sell, license, offer for sale/license and/or import the Accused Products. Dell was aware that it infringed the '299 patent from at least December 23, 2009, and instead of taking a license, Dell opted to make the business decision to "efficiently infringe" the '299 patent. In doing so, Dell willfully infringed and continues to willfully infringe the '299 Patent.

36. Dell is not licensed or otherwise authorized to practice the claims of the '299 patent.

37. By reason of Dell's infringement, 3D Surfaces has suffered and continues to suffer damages.

38. 3D Surfaces is entitled to recover the damages sustained as a result of Dell's wrongful acts in an amount subject to proof at trial.

COUNT II

Infringement of the '534 Patent

39. 3D Surfaces re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

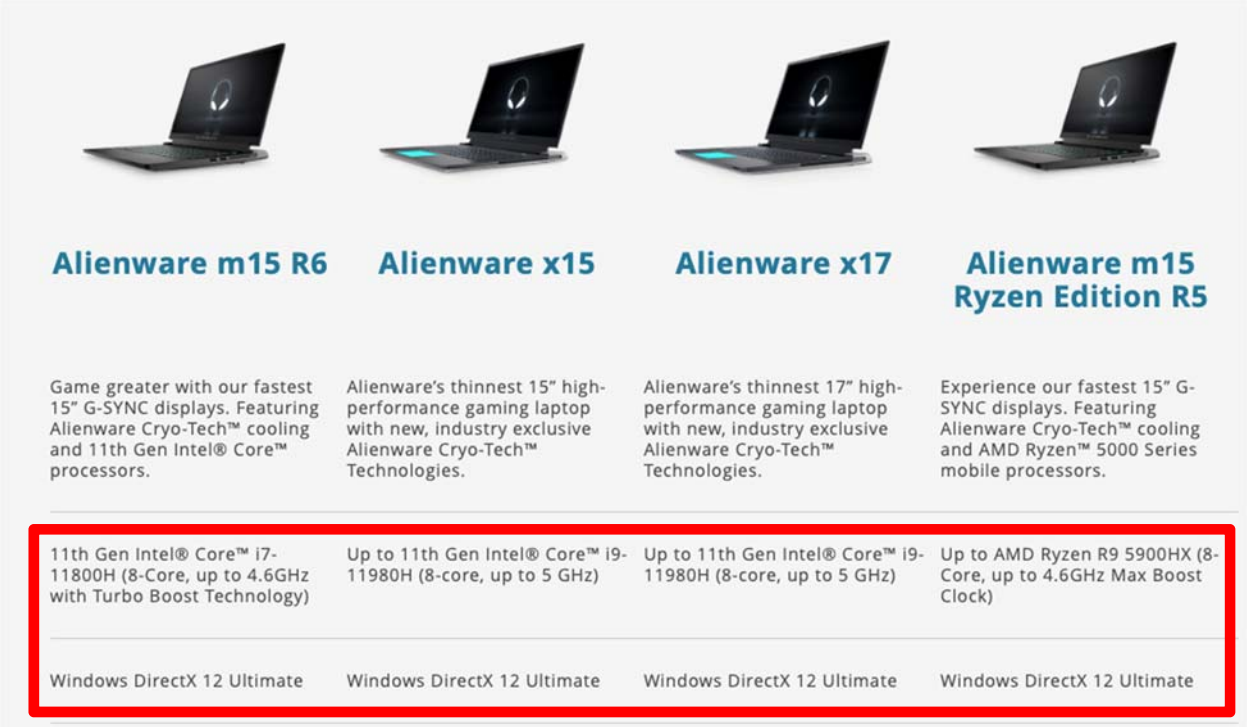
40. In violation of 35 U.S.C. § 271(a), Dell has infringed the '534 patent by making, using, selling, offering for sale, and/or importing into the United States, without authority, the Accused Products which practiced each and every limitation of at least claim 15 of the '534 patent. Dell has infringed literally and/or under the doctrine of equivalents.

41. The Accused Products are each include a central processing unit (CPU) and a graphics processing unit (GPU). The Accused Products support DirectX 11 and higher 3D graphics technology. By way of example, the Accused Products include AMD processors or Intel Core processors (4th gen and later) with integrated GPUs that support DirectX 11.1 and higher.

Table 1.1: Comparing the best of Intel 3rd generation with Intel 4th generation processor graphics

	3rd gen Intel® Core™ processor	4th gen Intel® Core™ processor		
	Intel® HD Graphics 4000	Intel® HD Graphics	Intel® HD Graphics 4200/4400/4600	Intel® Iris™ Pro Graphics 5200, Intel™ Iris™ Graphics 5100, Intel® HD Graphics 5000
APIs	DirectX* 11.0 DirectX Shader Model 5.0 OpenGL* 4.0 OpenCL* 1.1	DirectX* 11.1 DirectX Shader Model 5.0 OpenGL* 4.2 OpenCL* 1.2		

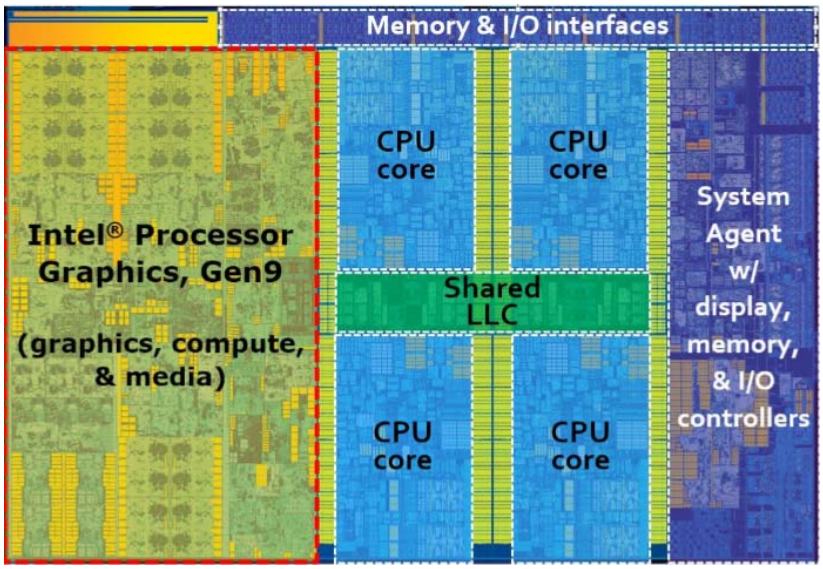
https://www.intel.com/content/dam/develop/external/us/en/documents/4th-gen-core-graphics-dev-guide.pdf at 3.

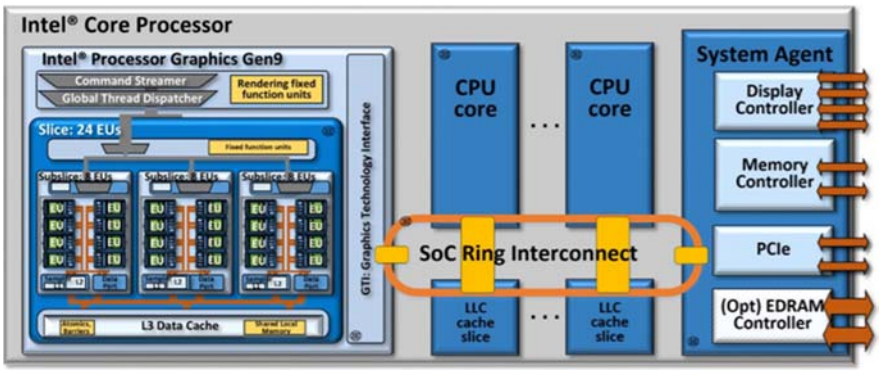


Alienware m15 R6	Alienware x15	Alienware x17	Alienware m15 Ryzen Edition R5
Game greater with our fastest 15" G-SYNC displays. Featuring Alienware Cryo-Tech™ cooling and 11th Gen Intel® Core™ processors.	Alienware's thinnest 15" high-performance gaming laptop with new, industry exclusive Alienware Cryo-Tech™ Technologies.	Alienware's thinnest 17" high-performance gaming laptop with new, industry exclusive Alienware Cryo-Tech™ Technologies.	Experience our fastest 15" G-SYNC displays. Featuring Alienware Cryo-Tech™ cooling and AMD Ryzen™ 5000 Series mobile processors.
11th Gen Intel® Core™ i7-11800H (8-Core, up to 4.6GHz with Turbo Boost Technology)	Up to 11th Gen Intel® Core™ i9-11980H (8-core, up to 5 GHz)	Up to 11th Gen Intel® Core™ i9-11980H (8-core, up to 5 GHz)	Up to AMD Ryzen R9 5900HX (8-Core, up to 4.6GHz Max Boost Clock)
Windows DirectX 12 Ultimate	Windows DirectX 12 Ultimate	Windows DirectX 12 Ultimate	Windows DirectX 12 Ultimate

https://www.dell.com/en-us/gaming/alienware-laptops?~ck=mn.

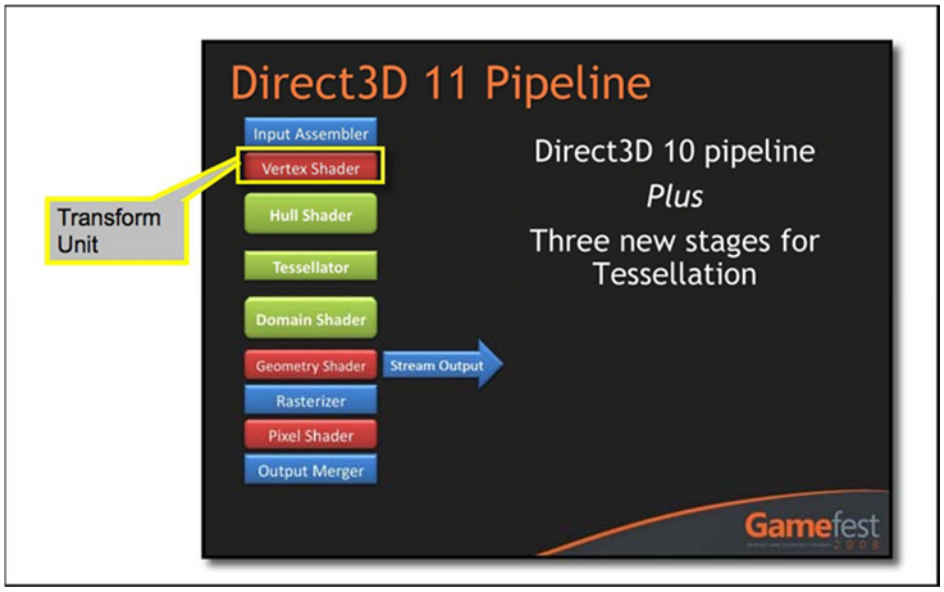
42. The Accused Products perform a method comprising providing a tessellation unit coupled between a transform unit and a lighting unit. Each of the Accused Dell Products has a microprocessor with a central processing unit (comprising the 4 CPU cores shown below), a graphics processing unit (GPU) (highlighted by red box below) and a bus that operatively connects to both the CPU and the GPU (shown as the "SoC Ring Interconnect" below).



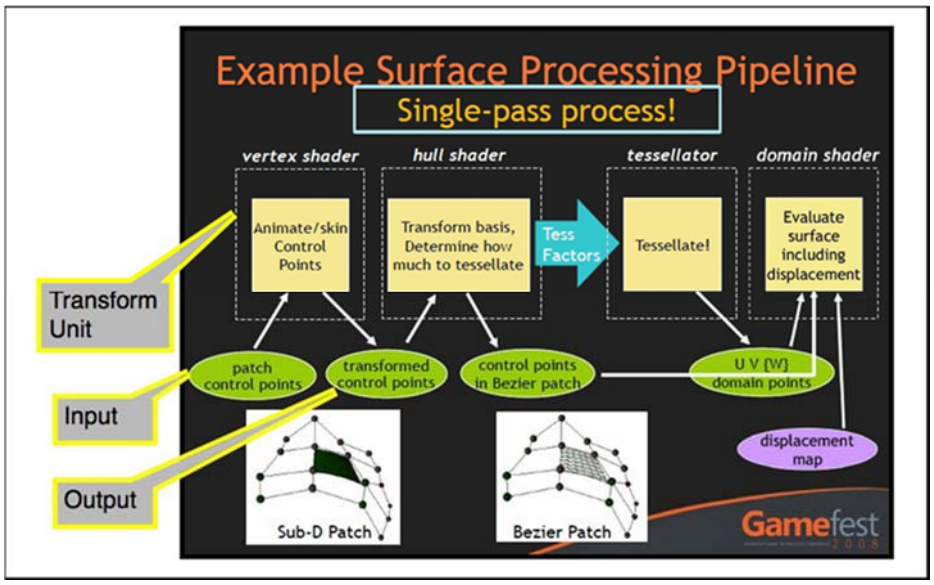


"4.2 RING INTERCONNECT The on-die bus between CPU cores, caches, and Intel processor graphics is a ring based topology with dedicated local interfaces for each connected "agent". This SoC ring interconnect is a bi-directional ring that has a 32-byte wide data bus, with separate lines for request, snoop, and acknowledge. Every on-die CPU core is regarded as a unique agent. Similarly, Intel processor graphics is treated as a unique agent on the interconnect ring."
High level architecture of an Intel microprocessor with a Gen9 integrated graphics processor (The Compute Architecture of Intel Processor Graphics Gen9, Version 1.0 at 3-4)

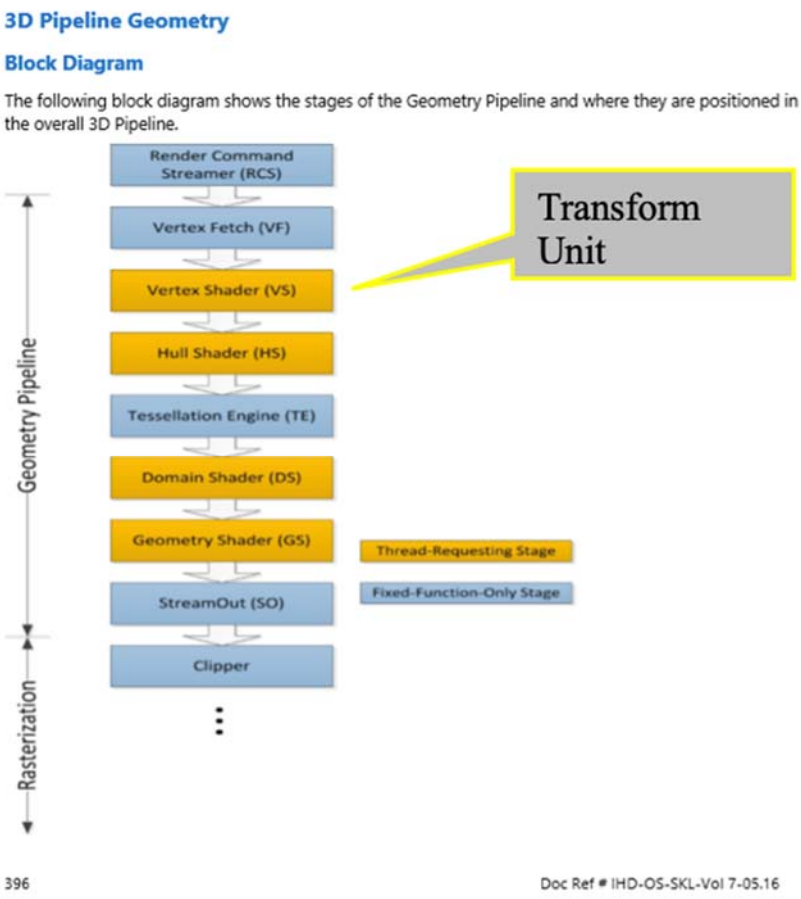
43. A tessellation unit is provided, coupled between the transform unit and lighting unit. The 3D graphics pipeline of the Accused Products supports DirectX 11 (and higher) and accordingly comprises a transform unit shown as the Vertex Shader that transforms control point information into information that can be further processed by the tessellation stages. The Vertex Shader takes control points of a patch as an input and transforms those control points into transformed control objects (e.g., vertices) that can be further processed by the real-time tessellation unit, which is the function of the transform unit of the '534 patent. In the '534 patent, the transform unit transforms control points into transformed data (i.e., vertices) that can be acted upon by the tessellation unit.



Introduction to Direct 3D 11 Graphics Pipeline, Gamefest Microsoft Game Technology Conference, Microsoft Corp, p. 12



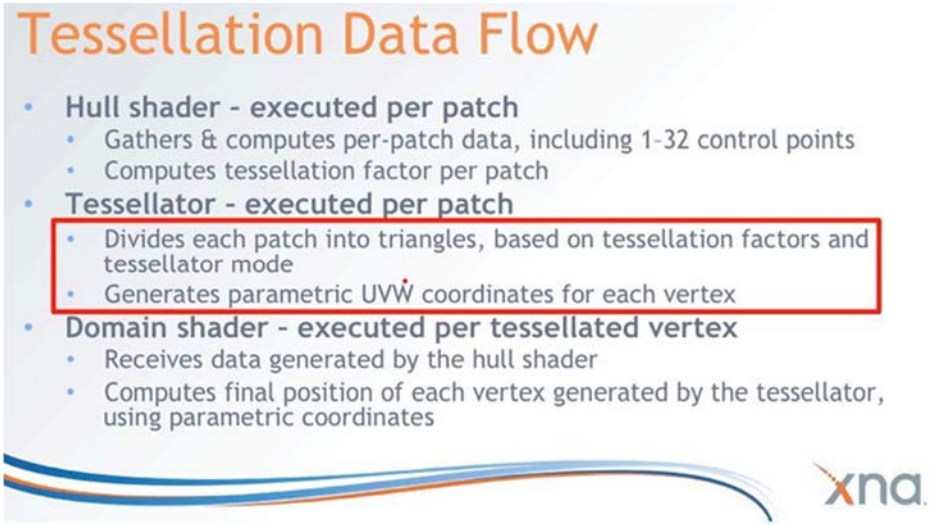
Introduction to Direct 3D 11 Graphics Pipeline, Gamefest Microsoft Game Technology Conference, Microsoft Corp, p. 17



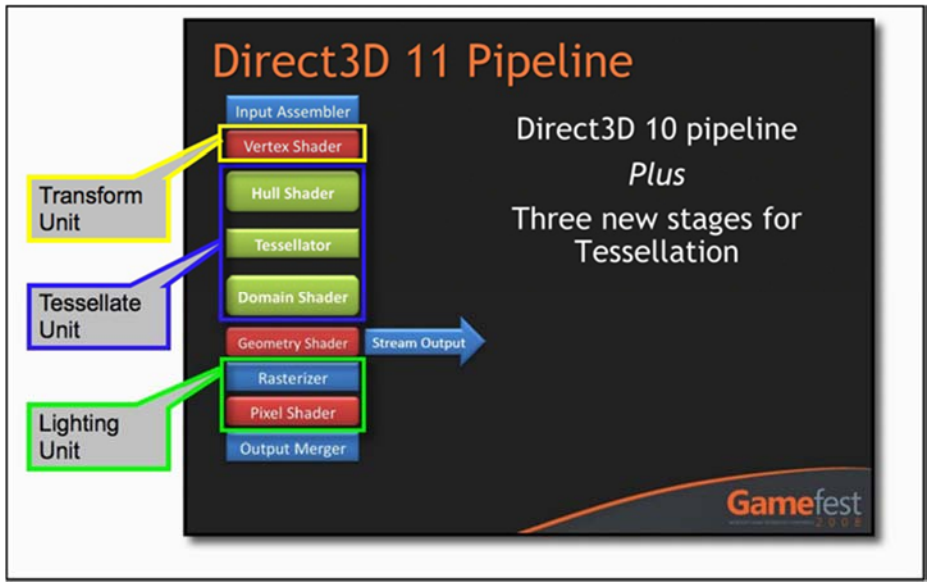
"The Vertex Shader stage is responsible for processing (shading) incoming vertices by passing them to VS threads." Intel Gen9 PRM at pages 392, 396. The incoming vertices to the Vertex Shader stage, in the case of processing 3D primitives associated with patches (i.e., the "PATCHLIST_n" 3D topology) are called "Input Control Points." Intel Gen9 PRM at page 455.

"The Vertex Shader (VS) stage of the 3D Pipeline is used to perform processing ("shading") of vertices after they are assembled and written to the URB by the VF function. The primary function of the VS stage is to pass vertices that miss in the VS Cache to VS threads, and then pass the VS thread-generated vertices down the pipeline. Vertices that hit in the VS Cache have already been shaded and are therefore passed down the pipeline unmodified." Intel Gen9 PRM at page 450.

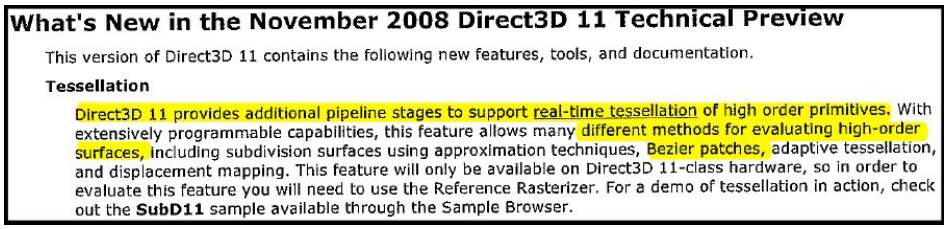
44. The graphics pipeline of the Accused Products, which support DirectX 11 (and higher), contains a tessellation unit, which comprises the Hull Shader, Tessellator and Domain Shader (Three stages for Tessellation). The tessellation unit is operatively coupled between the transform unit and lighting unit such that transformed primitive objects are passed through the pipeline from the Vertex Shader to the tesselate unit, and the output of the tesselate unit flows to the lighting unit.



Direct3D 11 Tessellation Deep Dive, XNA, Microsoft Corp, 2009, p. 9



Introduction to Direct 3D 11 Graphics Pipeline, Gamefest Microsoft Game Technology Conference, Microsoft Corp, p. 12



What's New in the November 2008 Direct3D 11 Technical Preview

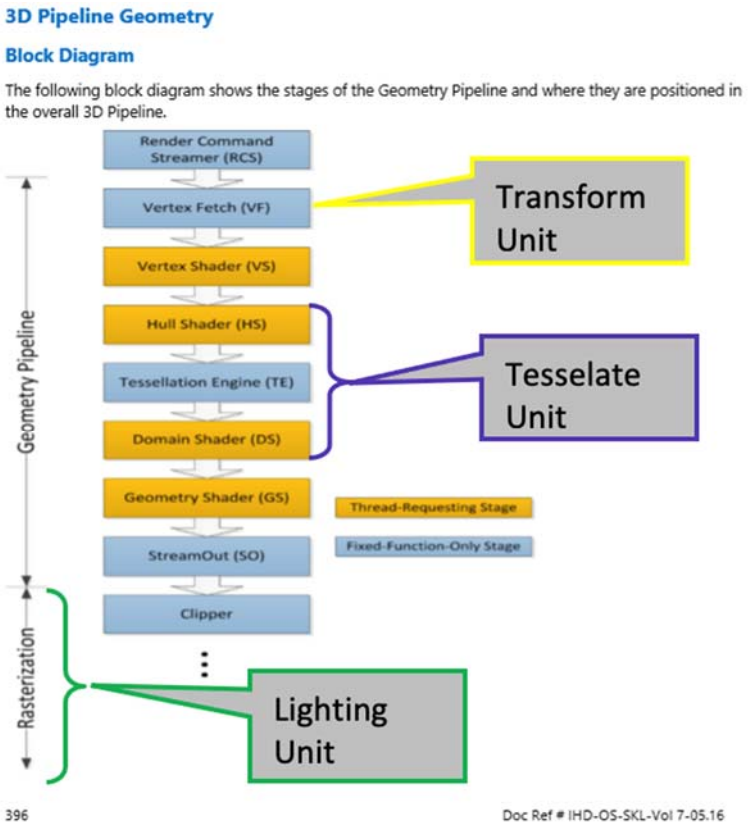
This version of Direct3D 11 contains the following new features, tools, and documentation.

Tessellation

Direct3D 11 provides additional pipeline stages to support real-time tessellation of high order primitives. With extensively programmable capabilities, this feature allows many different methods for evaluating high-order surfaces, including subdivision surfaces using approximation techniques, Bezier patches, adaptive tessellation, and displacement mapping. This feature will only be available on Direct3D 11-class hardware, so in order to evaluate this feature you will need to use the Reference Rasterizer. For a demo of tessellation in action, check out the **SubD11** sample available through the Sample Browser.

What's New in the November 2008 Direct3D 11 Technical Preview, DirectX SDK, Microsoft Corp.

p. 1



Intel Gen9 PRM at page 396.

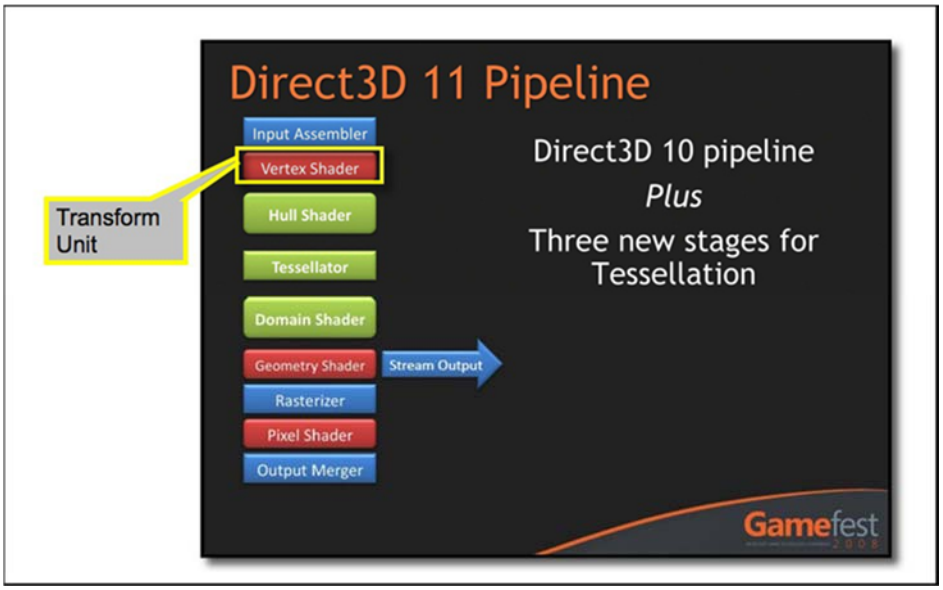
45. The Accused Products perform the step of receiving graphics objects to be rendered by a graphics processing unit. For example, the Accused Products run applications on the CPU which generate graphic objects that are transmitted to and received by the GPU over the Ring Interconnect bus.

> "The 3DPRIMITIVE command (defined in the VF Stage chapter) is used to submit 3D primitives to be processed by the 3D pipeline. Typically, the processing results in the rendering of pixel data into the render targets, but this is not required. . . . In this spec, we will try to avoid ambiguity by using the term 'object' to represent the basic shapes (point, line, triangle), and 'topology' to represent input geometry (strips, lists, etc.)."
>
> Intel® Open Source HD Graphics, Intel Iris™ Graphics, and Intel Iris™ Pro Graphics Programmer's Reference Manual For the 2015 - 2016 Intel Core™ Processors, Celeron™ Processors, and Pentium™ Processors based on the "Skylake" Platform, Volume 7: 3D-Media-GPGPU, page 419, May 2016, Revision 1.0 l; Vol 7 ("Intel Gen9 PRM")

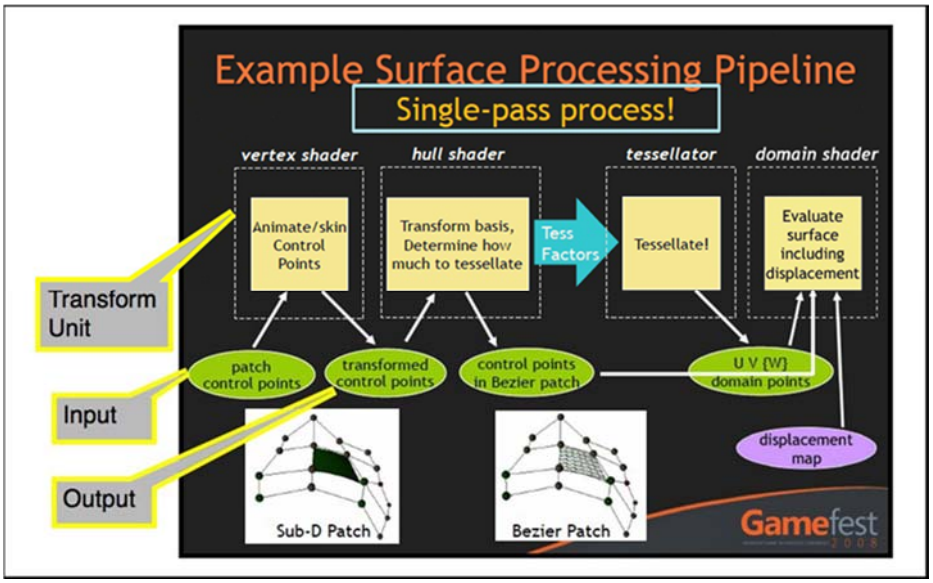
> by a collection of primitives. In most cases, primitives are triangles defined by vertices. Vertex information consists of geometric position and further attributes such as normal vector, texture coordinates, color, or opacity.
>
> Primitives are sent from CPU to GPU as a stream of vertices, which are then transformed by the *vertex processor*. In the traditional fixed-function

Daniel Weiskopf., GPU-based interactive visualization techniques. Springer-Verlag New York, LLC, p. 4

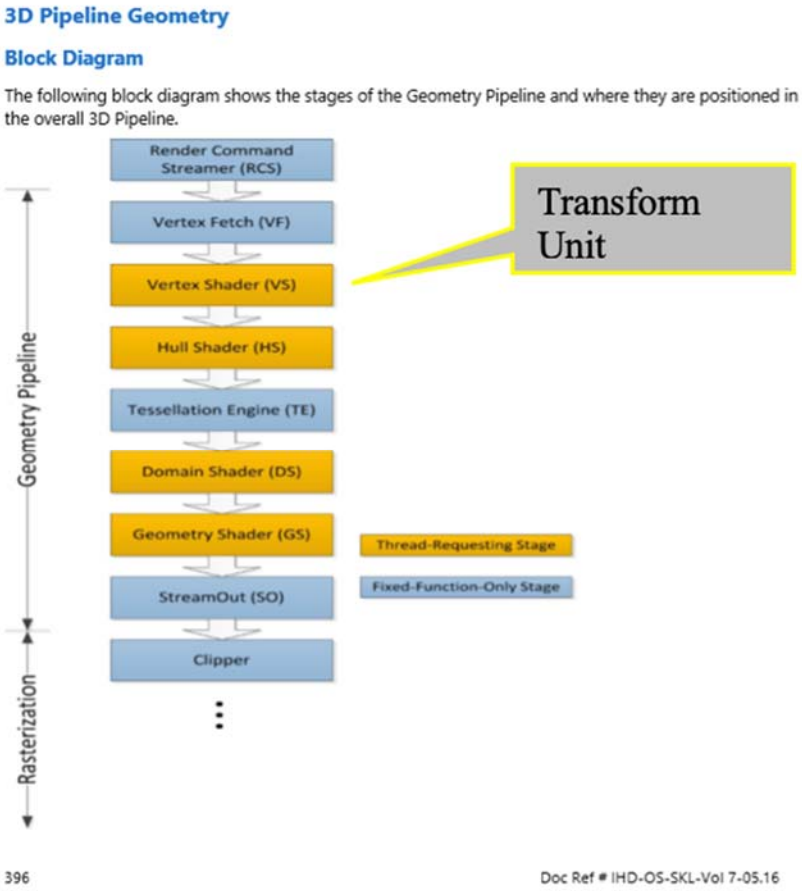
46. The Accused Products perform the step of transforming the graphics objects into transformed objects using said transform unit. For example, the graphics pipeline of the Accused Products' GPU with DirectX 11 (and higher) support contains a transform unit, which is referred to as a Vertex Shader in DirectX 11 (and higher). The Vertex Shader takes control points of a patch as an input and transforms those control points into transformed control objects (*e.g.*, vertices) that can be further processed by the real-time tessellation unit, which is the function of the transform unit of the '534 patent. In the '534 patent, the transform unit transforms control points into transformed data (*i.e.*, vertices) that can be acted upon by the tessellation unit.



Introduction to Direct 3D 11 Graphics Pipeline, Gamefest Microsoft Game Technology Conference, Microsoft Corp, p. 12



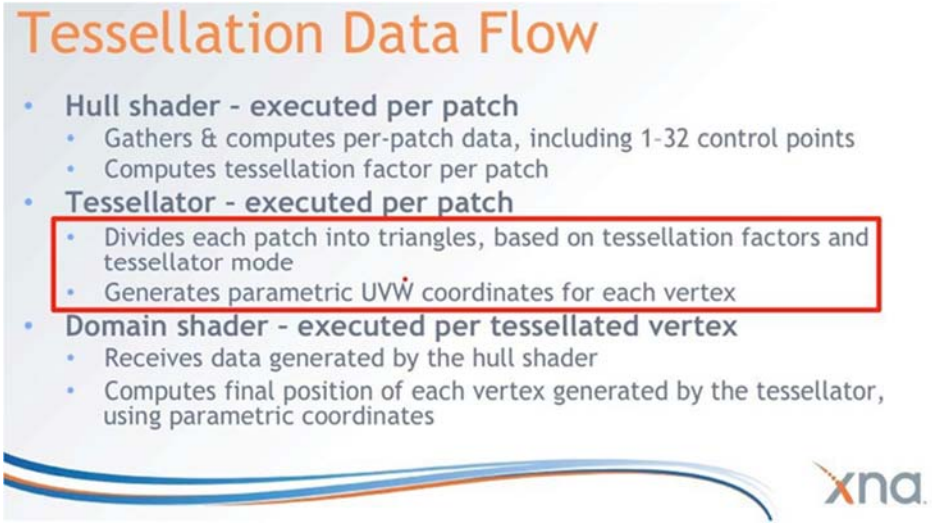
Introduction to Direct 3D 11 Graphics Pipeline, Gamefest Microsoft Game Technology Conference, Microsoft Corp, p. 17



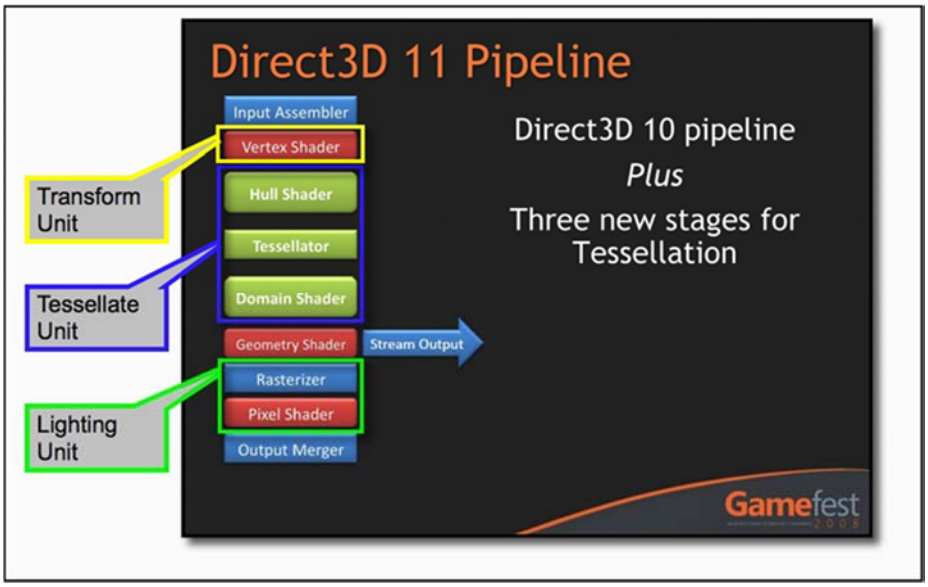
"The Vertex Shader stage is responsible for processing (shading) incoming vertices by passing

them to VS threads." Intel Gen9 PRM at pages 392, 396.

47. The Accused Products perform the step of tessellating the transformed objects using the tessellation unit. The graphics pipeline of the Accused Products' GPU with DirectX 11 (and higher) support contains a tessellation unit, which comprises the Hull Shader, Tessellator and Domain Shader (Three stages for Tessellation) in DirectX 11 (and higher), and the tessellation unit is operatively coupled between the transform unit and the lighting unit such that transformed primitive objects are passed through the pipeline from the Vertex Shader to the tesselate unit, and the output of the tesselate unit flows to the lighting unit. The tessellate unit (Hull Shader, Tessellator and Domain Shader) performs real-time tessellation of Bezier object surfaces (Bezier patches, Bezier rational patches and any other types of bicubic or subdivision patches such as beta-splines and NURBS).



Direct3D 11 Tessellation Deep Dive, XNA, Microsoft Corp, 2009, p. 9



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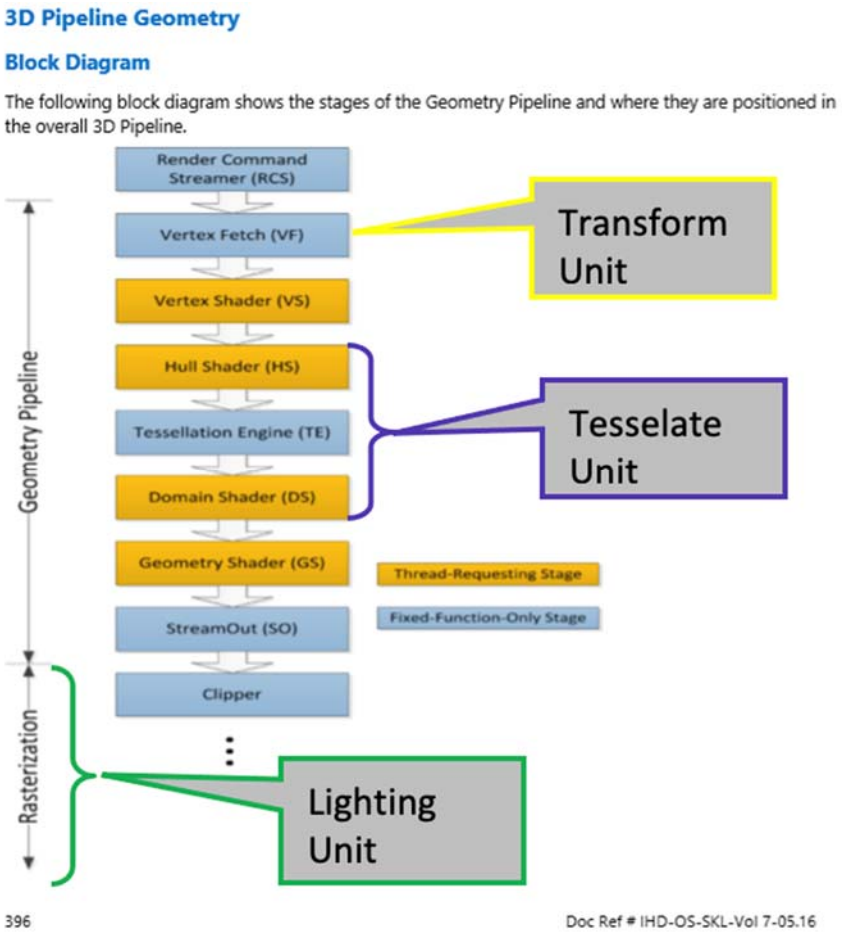
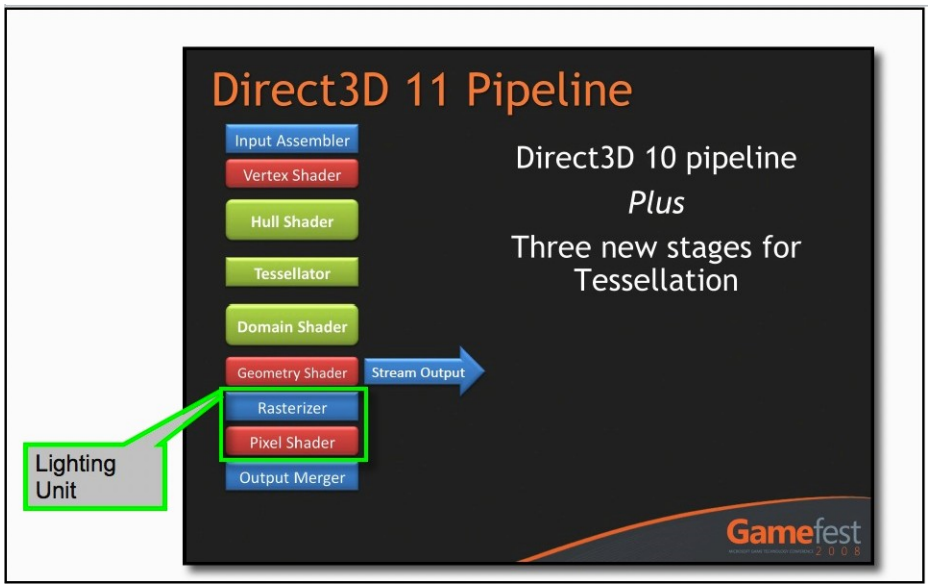
What's New in the November 2008 Direct3D 11 Technical Preview, DirectX SDK, Microsoft Corp,
p. 1



Intel Gen9 PRM at page 396.

48. The Accused Products perform the step of lighting vertices of triangles resultant from said tessellating using said lighting unit. The graphics pipeline of the Accused Products' GPU with DirectX 11 (and higher) support (including the microprocessor of the Accused Products) contains a lighting unit (called Rasterizer and Pixel Shader in DirectX 11 (and higher)) that lights triangles based on data of previous stages (tessellation).



Introduction to Direct 3D 11 Graphics Pipeline, Gamefest Microsoft Game Technology Conference, Microsoft Corp, p. 11

Geometry-Shader Stage

The geometry-shader (GS) stage runs application-specified shader code with vertices as input and the ability to generate vertices on output. Unlike vertex shaders, which operate on a single vertex, the geometry shader's inputs are the vertices for a full primitive (two vertices for lines, three vertices for triangles, or single vertex for point). Geometry shaders can also bring in the vertex data for the edge-adjacent primitives as input (an additional two vertices for a line, an additional three for a triangle).

Shader Stages (Direct3D 10), DirectX SDK, Microsoft Corp, p. 1

Rasterizer Stage (Direct3D 10)

The rasterization stage converts vector information (composed of shapes or primitives) into a raster image (composed of pixels) for the purpose of displaying real-time 3D graphics. During rasterization, each primitive is converted into pixels, while interpolating per-vertex values across each primitive. Rasterization includes clipping vertices to the view frustum, performing a divide by z to provide perspective, mapping primitives to a 2D viewport, and determining how to invoke the pixel shader. While using a pixel shader is optional, the rasterizer stage always performs clipping, a perspective divide to transform the points into homogeneous space, and maps the vertices to the viewport.

Rasterizer Stage (Direct3D 10), DirectX SDK, Microsoft Corp, p. 1

Pixel-Shader Stage

The pixel-shader stage (PS) enables rich shading techniques such as per-pixel lighting and post-processing. A pixel shader is a program that combines constant variables, texture data, interpolated per-vertex values, and other data to produce per-pixel outputs. The rasterizer stage invokes a pixel shader once for each pixel covered by a primitive, however, it is possible to specify a NULL shader to avoid running a shader.

Shader Stages (Direct3D 10), DirectX SDK, Microsoft Corp, p. 4

49. Dell was made aware of the '534 patent and its infringement thereof at least as early as September 7, 2011, when 3D Surfaces provided notice of Dell's infringement of the '534 patent to Anthony Peterman, currently VP of IP and IP Litigation at Dell Technologies. After at least the time Dell received notice, Dell induced others to infringe at least one claim of the '534 patent under 35 U.S.C. § 271(b) by, among other things, and with specific intent or willful blindness, actively aiding and abetting others to infringe, including but not limited to Dell's clients, customers, and end users, whose use of the Accused Product constituted direct infringement of at least one claim of the '534 patent. In particular, Dell's actions that aided and abetted others such as customers and end users to infringe included advertising and distributing the Accused Products and providing instruction materials, training, and services regarding the Accused Products. *See e.g.*,https://www.dell.com/support/home/en-us?app=drivers&~ck=mn; https://www.dell.com/support/contents/en-us/article/product-support/self-support-knowledgebase/dell-gaming/gaming-support; www.dell.com/support; https://www.dell.com/en-us/gaming/alienware-laptops?gacd=9614064-1054-5763017-266796622-0&dgc=st&ds_rl=1286018&msclkid=98a3b4adb85b12500fefd5f62840ec09&gclid=98a3b4adb85b12500fefd5f62840ec09&gclsrc=3p.ds&nclid=TF9OEC8yMUdWryaTl9NJuror7mX02yDYnqyPD5BuCHY-l30o3WLoDqZKec3Pd-gn;https://www.dell.com/en-us/shop/servicesforhome/cp/supportforgaming?~ck=mn. Dell engaged in such actions with specific intent to cause infringement or with willful blindness to the resulting infringement because Dell had actual knowledge of the '534 patent and knowledge that its acts were inducing infringement of the '534 patent since at least the date Dell received notice that such activities infringed the '534 patent.

50. Dell is liable as a contributory infringer of the '534 patent under 35 U.S.C. § 271(c) by having offered to sell, sold and imported into the United States computers including CPU and GPUs coupled together including a graphics pipeline having a tessellation unit that is operatively

coupled between a transform unit and a lighting unit to be especially made or adapted for use in an infringement of the '534 patent. The Accused Product is a material component for use in practicing the '534 patent and is specifically made and is not a staple article of commerce suitable for substantial non-infringing use.

51. Upon information and belief, since the date of its receipt of notice, Dell's infringement of the '534 patent was willful and intentional under the standard announced in *Halo Elecs., Inc. v. Pulse Elecs., Inc.,* 136 S.Ct. 1923, 195 L.Ed 2d 278 (2016). From at least September 7, 2011, Dell willfully infringed the '534 patent by refusing to take a license and continuing to make, use, test, sell, license, offer for sale/license and/or import the '534 Accused Products. Dell was aware that it infringed the '534 patent from at least September 7, 2011 and instead of taking a license, Dell opted to make the business decision to "efficiently infringe" the '534 patent. In doing so, Dell willfully infringed the '534 Patent.

52. Dell was not licensed or otherwise authorized to practice the claims of the '534 patent.

53. By reason of Dell's infringement, 3D Surfaces has suffered damages.

54. 3D Surfaces is entitled to recover the damages sustained as a result of Dell's wrongful acts in an amount subject to proof at trial.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Federal Rules of Civil Procedure, Plaintiff hereby demands a trial by jury as to all issues so triable.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff respectfully prays for the following relief:

(a) A judgment that Defendants have infringed each of the Asserted Patents;

(b) Damages adequate to compensate 3D Surfaces for Defendants' infringement of

the Asserted Patents pursuant to 35 U.S.C. § 284, together with interest and costs fixed by the Court including an accounting of all infringements and/or damages not presented at trial;

(c) That the Court declare this an exceptional case and award Plaintiff its attorneys' fees, as provided by 35 U.S.C. § 285 and that Plaintiff be awarded enhanced damages up to treble damages for willful infringement as provided by 35 U.S.C. § 284;

(d) Pre-judgment interest;

(e) Post-judgment interest; and

(f) Such other relief as the Court deems just and equitable.

Dated: October 25, 2021

/s/ Marc Belloli w/permission Wesley Hill
Marc Belloli (*pro hac vice* to be filed)
mbelloli@feinday.com
M. Elizabeth Day (*pro hac vice* to be filed)
eday@feinday.com
David Alberti (*pro hac vice* to be filed)
dalberti@feinday.com
Hong Lin (*pro hac vice* to be filed)
hlin@feinday.com
Jerry D. Tice II
Texas Bar No. 24093263
jtice@feinday.com
FEINBERG DAY KRAMER ALBERTI LIM TONKOVICH & BELLOLI LLP
577 Airport Boulevard, Suite 250
Burlingame, California 94010
Telephone: (650) 825-4300
Facsimile: (650) 460-8443

Wesley Hill (Texas Bar No. 24032294)
wh@wsfirm.com
WARD, SMITH & HILL, PLLC
1507 Bill Owens Parkway
Longview, Texas 75604
Tel: 903-757-6400
Fax: 903-757-2323

Attorneys for Plaintiff 3D Surfaces, LLC