IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

RAMPART ASSET MANAGEMENT LLC,	§	Case No.
Plaintiff,	§	**JURY TRIAL DEMANDED**
v.	§	
TEXAS INSTRUMENTS, INC.,	§	
Defendant.	§	

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Rampart Asset Management LLC ("Rampart" or "Plaintiff") for its Complaint against Defendant Texas Instruments, Inc., ("Defendant") alleges as follows:

THE PARTIES

1. Rampart is a limited liability company organized and existing under the laws of the State of Texas, with its principal place of business located at 133 East Tyler Street, Longview, Texas, 75601.

2. Upon information and belief, Defendant Texas Instruments, Inc. ("TI") is a publicly traded corporation organized and existing under the laws of the State of Delaware, with its principal place of business located at 12500 TI Boulevard, Dallas, Texas 75243.

3. On information and belief, TI is a technology company in the business of researching, developing, making, using, and selling semiconductor products, including the TI-branded products accused of infringement in this case by Rampart (the "Accused Products" defined below).

JURISDICTION

4. This is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. §§ 1, *et seq*. This Court has jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and 1338(a) and 1367.

5. This Court has personal jurisdiction over the Defendant consistent with the requirements of the Due Process Clause of the United States Constitution and the Texas Long Arm Statute. Defendant TI has its principal place of business in Dallas, Texas, where it employs more than 20,000 employees.

6. TI has, thereby, committed acts of direct infringement in the United States and in this District in violation of Rampart's intellectual property rights.

7. Venue is proper in this Judicial District pursuant to 28 U.S.C. §§ 1391(b) and 1400(b) because Defendant is subject to personal jurisdiction in this District, has committed acts of patent infringement in this District, and has a regular and established place of business in this District, including at least a commercial manufacturing facility located at 6412 U.S. Highway 75, Sherman, Texas, 75090. In addition to its existing facilities in this District, Texas Instruments has, upon information and belief, commenced its construction activities with respect to a new $30 billion chip manufacturing facility also located in this District. Further, upon information and belief, Defendant has previously admitted or not contested proper venue in this District in other patent infringement actions.

PATENTS-IN-SUIT

8. On June 14, 2016, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 9,367,248 (the "'248 Patent") entitled "Memory Component with Pattern

Register Circuitry to Provide Data Patterns for Calibration." A true and correct copy of the '248 Patent is attached as Exhibit A.

9. On August 1, 2017, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 9,721,642 (the "'642 Patent") entitled "Memory Component with Pattern Register Circuitry to Provide Data Patterns for Calibration." A true and correct copy of the '642 Patent is attached as Exhibit B.

10. On January 29, 2019, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 10,192,609 (the "'609 Patent") entitled "Memory Component with Pattern Register Circuitry to Provide Data Patterns for Calibration." A true and correct copy of the '609 Patent is attached as Exhibit C.

11. On May 29, 2007, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 7,225,311 (the "'311 Patent") entitled "Method and Apparatus for Coordinating Memory Operations Among Diversely-Located Memory Components." A true and correct copy of the '311 Patent is attached as Exhibit D.

12. On July 3, 2012, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 8,214,616 (the "'616 Patent") entitled "Memory Controller Device Having Timing Offset Capability." A true and correct copy of the '616 Patent is attached as Exhibit E.

13. On June 25, 2013, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 8,472,511 (the "'511 Patent") entitled "Selectable-Tap Equalizer." A true and correct copy of the '511 Patent is attached as Exhibit F.

14. Rampart is the sole and exclusive owner of all right, title, and interest in the'248 Patent, the '642 Patent, the '609 Patent, the '311 Patent, the '616 Patent, and the '511 Patent, (collectively, the "Patents-in-Suit"), and holds the exclusive right to take all actions necessary to

enforce its rights to the Patents-in-Suit, including the filing of this patent infringement lawsuit. Rampart also has the right to recover all damages for past, present, and future infringement of the Patents-in-Suit and to seek injunctive relief as appropriate under the law.

15. Rampart has at all times complied with the marking provisions of 35 U.S.C. § 287 with respect to the Patents-in-Suit.

FACTUAL ALLEGATIONS

16. The Patents-in-Suit generally cover systems and methods for coordinating memory operations and providing data patterns for calibration of memory systems.

17. The '248 Patent generally relates to the field of digital circuits and, more particularly, to an apparatus and method for phase adjustment and memory device signaling systems. The technology described in the '248 Patent was developed by Craig E. Hampel, Richard E. Perego, Stefanos Sidiropoulos, Ely K. Tsern, and Frederick A. Ware. By way of example, this technology is implemented today in memory systems that adjust the phase of data signals to compensate for phase offset variations between devices during normal operation.

18. The '642 Patent generally relates to the field of digital circuits and, more particularly, to an apparatus and method for phase adjustment and memory device signaling systems. The technology described in the '642 Patent was developed by Craig E. Hampel, Richard E. Perego, Stefanos Sidiropoulos, Ely K. Tsern, and Frederick A. Ware. By way of example, this technology is implemented today in memory systems that adjust the phase of data signals to compensate for phase offset variations between devices during normal operation.

19. The '609 Patent generally relates to the field of digital circuits and, more particularly, to an apparatus and method for phase adjustment and memory device signaling systems. The technology described in the '609 Patent was developed by Craig E. Hampel, Richard

E. Perego, Stefanos Sidiropoulos, Ely K. Tsern, and Frederick A. Ware. By way of example, this technology is implemented today in memory systems that adjust the phase of data signals to compensate for phase offset variations between devices during normal operation.

20. The '311 Patent generally relates to information storage and retrieval and, more specifically, to coordinating memory operations among diversely-located memory components. The technology described in the '311 Patent was developed by Frederick A. Ware, Ely K. Tsern, Richard E. Perego, and Craig E. Hampel. By way of example, this technology is implemented today in memory systems that configure multiple memory components to account for address bus and data bus propagation delays.

21. The '616 Patent generally relates to information storage and retrieval and, more specifically, to coordinating memory operations among diversely-located memory components. The technology described in the '616 Patent was developed by Frederick A. Ware, Ely K. Tsern, Richard E. Perego, and Craig E. Hampel. By way of example, this technology is implemented today in memory systems that configure multiple memory components to account for address bus and data bus propagation delays.

22. The '511 Patent generally relates to high speed signaling within and between integrated circuit devices and, more particularly, to reducing latent signal distortions in high speed signaling systems. The technology described in the '511 Patent was developed by Jared L. Zerbe, Vladimir M. Stojanovic, and Fred F. Chen. By way of example, this technology is implemented today in memory systems that perform iterative testing of signal wires and use pass/fail to correctly set a parameter during initialization.

23. TI has infringed and is continuing to infringe one or more of the Patents-in-Suit by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make,

use, sell, offer to sell, and/or import memory controllers that support one or more of the DDR3, DDR3L, and DDR4 (the "Accused Products"). Such products include, but are not limited to, the TI DRA780, DRA781, DRA782, DRA783, DRA784, DRA785, DRA786, DRA787, DRA788, TMS320C6655, TMS320C6657, 66AK2G12, 66AK2H06, 66AK2H12, 66AK2H14, DRA744P, DRA745P, DRA746P, DRA750P, DRA751P, DRA752P, DRA754P, DRA755P, DRA756P, DRA710, DRA712, DRA714, DRA716, DRA724, DRA722, DRA725, DRA767P, DRA77xP, DRA790, DRA791, DRA793, DRA797, TDA2P-ABZ, TDA2P-ACD, TDA2EG-17, TDA2EG, TDA2EGABC, TDA2HF, TDA2SX, TDA2SG, TDA2SA, TDA2HG, TDA2HV, TDA2LF, AM4372, AM4376, AM4377, AM4378, AM4379, AM5748, AM5749, AM5706, AM5708, AM5716, AM5718, AM5726, AM5728, AM5729, AM6441, AM6442, AM6421, AM6412, and AM6411 Sitara Processors

COUNT I
(Infringement of the '248 Patent)

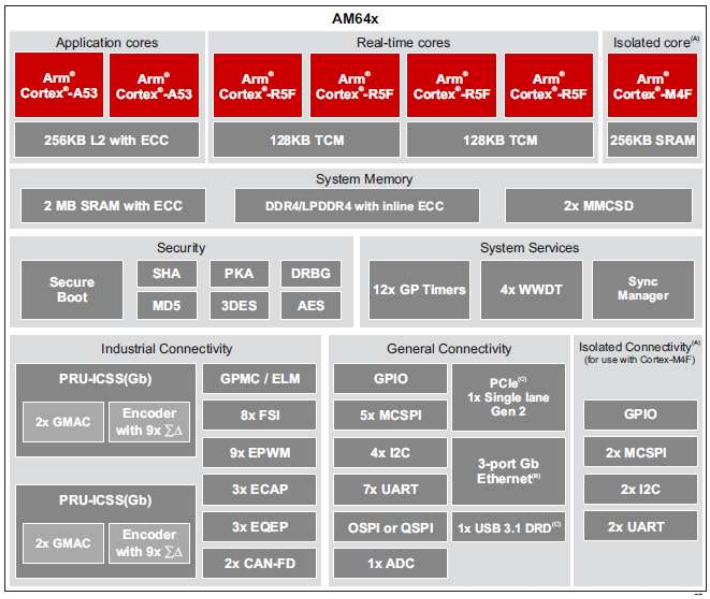
24. Paragraphs 1 through 23 are incorporated by reference as if fully set forth herein.

25. Rampart has not licensed or otherwise authorized Defendant to make, use, offer for sale, sell, or import any products that embody the inventions of the '248 Patent.

26. Defendant has and continues to directly infringe the '248 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products including, but not limited to, products supporting DDR4 external memories, such as the TI AM6442, AM6441, AM6421, AM6412, and AM6411 Sitara Processors.

27. For example, Defendant has and continues to directly infringe at least Claim 1 of the '248 Patent by making, using, offering to sell, selling, and/or importing into the United States products that include a memory controller that complies with the DDR4 standard. For example,

the TI AM6442 processor includes DDR4 memory controllers capable of controlling a memory system consisting of DDR4 SDRAM memory integrated circuits, each of which is compliant with the JEDEC standard JESD79-4, as shown by the AM64x Sitara Processors Datasheet, SPRSP56B, dated August 2021, p.5:



Memory subsystem:

- Up to 2MB of On-chip RAM (OCSRAM) with SECDED ECC:
  - Can be divided into smaller banks in increments of 256KB for as many as 8 separate memory banks
  - Each memory bank can be allocated to a single core to facilitate software task partitioning
- DDR Subsystem (DDRSS)
  - Supports LPDDR4, DDR4 memory types
  - 16-Bit data bus with inline ECC
  - Supports speeds up to 1600 MT/s

AM64x Sitara Processors Datasheet, SPRSP56B, August 2021, p. 1.

Table 5-1. Device Comparison

FEATURES	REFERENCE NAME	AM6442	AM6441	AM6422	AM6421	AM6412	AM6411
CTRLMMR_WKUP_JTAG_DEVICE_ID[31:13] DEVICE_ID register bit field value[1]		D: 0x19464 E: 0x19465 F: 0x19466	D: 0x19264 E: 0x19265 F: 0x19266	C: 0x19423	D: 0x19224 E: 0x19225 F: 0x19226	C: 0x19403	C: 0x19203
PROCESSORS AND ACCELERATORS							
Speed Grades		See Table 7-1					
Arm Cortex-A53 Microprocessor Subsystem	Arm A53	Dual Core	Single Core	Dual Core	Single Core	Dual Core	Single Core
Arm Cortex-R5F	Arm R5F	2 x Dual Core	2 x Dual Core	1 x Dual Core	1 x Dual Core	Single Core	Single Core
Arm Cortex-M4F	Arm M4F	Single Core					
Device Management Security Controller	DMSC-L	Yes					
Cryto Accelerators	Security	Yes					
MCU domain with Arm Cortex-M4F	Safety	Yes					
PROGRAM AND DATA STORAGE							
On-Chip Shared Memory (RAM) in MAIN Domain	OCSRAM	2MB					
R5F Tightly Coupled Memory (TCM)	TCM	256KB	256KB	256KB	256KB	128KB	128KB
On-Chip Shared Memory (RAM) in M4F Domain	MCU_MSRAM	256KB					
DDR4/LPDDR4 DDR Subsystem	DDRSS	Up to 2GB (16-bit data) with inline ECC					

AM64x Sitara Processors Datasheet, SPRSP56B, August 2021, p. 7.

28. The required characteristics of DDR4 memories and memory systems and, therefore, of DDR4 memory controllers and their encompassing integrated circuits are defined by JEDEC in a collection of publicly available standards. In particular, standard JESD79-4 is the standard defining DDR4 SDRAMs, and JESD79-4D is the latest version of that standard, dated July 2021:

> This document defines the DDR4 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this Standard is to define the minimum set of requirements for JEDEC compliant 2 Gb through 16 Gb for x4, x8, and x16 DDR4 SDRAM devices. This standard was created based on the DDR3 standards (JESD79-3) and some aspects of the DDR and DDR2 standards (JESD79, JESD79-2).

JESD79-4D, p. 1.

29. The Accused Products including DDR4 memory controllers include a first circuit to transmit commands to the memory component, the commands including a read command that specifies data to be accessed from a memory core of the memory component. DDR4 SDRAM memory controllers, including the TI AM6442 processor, include a first circuit which is a driver circuit that sends commands to the DDR4 SDRAM using certain pins (*e.g.*, DDR0_RAS_n, DDR0_CAS_n, and DDR0_WE_n). One such command is a read command that specifies the data to be accessed from a memory core.

6.3.2 DDRSS

6.3.2.1 MAIN Domain

Table 6-3. DDRSS0 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	ALV
DDR0_ACT_n	O	DDRSS Activation Command	H2
DDR0_ALERT_n	IO	DDRSS Alert	H1
DDR0_CAS_n	O	DDRSS Column Address Strobe	J5
DDR0_PAR	O	DDRSS Command and Address Parity	K5
DDR0_RAS_n	O	DDRSS Row Address Strobe	F6
DDR0_WE_n	O	DDRSS Write Enable	H4

AM64x Sitara Processors Datasheet, SPRSP56B, August 2021, p. 74.

JESD79-4 calls these signals at the DDR4 SDRAMs RAS_n/A16, CAS_n/A15, and WE_n/A14.

2.7 Pinout Description

Table 3 — Pinout Description

Symbol	Type	Function
		…
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS_n/ A15. WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table

JESD79-4D p. 5.

4.1 Command Truth Table

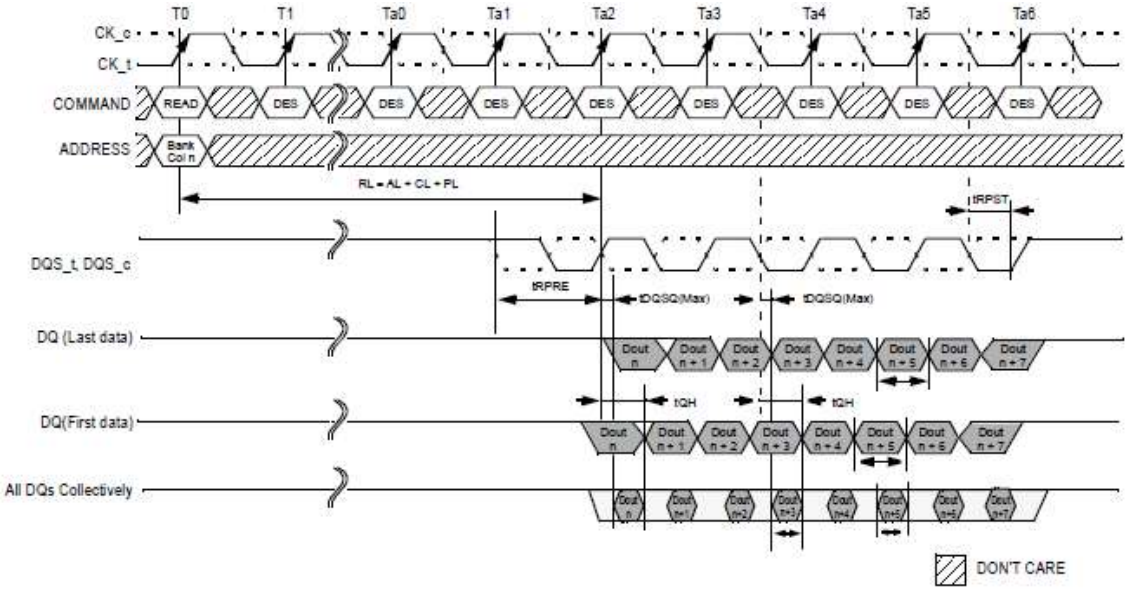
(a) Note 1,2,3 and 4 apply to the entire Command truth table
(b) Note 5 applies to all Read/Write commands.
[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, BC_n=Burst Chop, X=Don't Care, V=Valid].

Table 35 — Command Truth Table

Function	Abbreviation	CKE		CS_n	ACT_n	RAS_n /A16	CAS_n /A15	WE_n/ A14	BG0-BG1	BA0-BA1	C2-C0	A12/ BC_n	A17, A13, A11	A10/ AP	A0-A9	NOTE
		Previous Cycle	Current Cycle													
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V	OP Code				12
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	7,9
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	7,8,9, 10
				L	H	H	H	H	V	V	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	L	V	
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	H	V	
RFU	RFU	H	H	L	H	L	H	H	RFU							
Bank Activate	ACT	H	H	L	L	Row Address (RA)			BG	BA	V	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	6
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	6
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	H	V	
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	L	V	

JESD79-4D, p. 29.

Among the commands that DDR4 SDRAMs can respond to are Read commands. A Read command is provided to a DDR4 SDRAM by sending a command in which ACT_n is H, RAS_n/A16 is H, CAS_n/A15 is L, and WE_n/A14 is H, where H and L represent voltage levels representing logic states, as defined in Section 8 of JESD79-4. A Read command presented to a DDR4 SDRAM causes it to convey an addressed memory location to its pins for conveyance to the memory controller, as described in Section 4.24 of JESD79-4.



JESD79-4D, p. 96.

The DDR4 SDRAMs have a memory core consisting of 16 banks. Read operations are burst oriented, beginning at a selected location within the memory code:

3.2 Basic Functionality

The DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as sixteen-banks, 4 bank group with 4 banks for each bank group for x4/x8 and eight-banks, 2 bank group with 4 banks for each bankgroup for x16 DRAM.

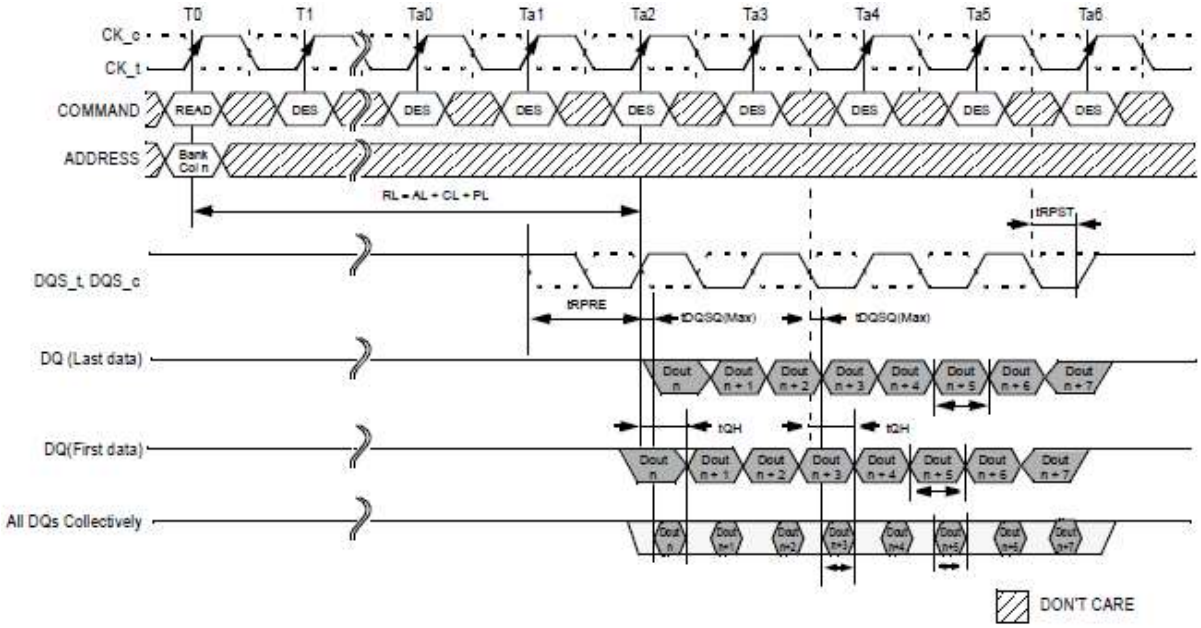
The DDR4 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR4 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered coincident with the ACTIVATE Command are used to select the bank and row to be activated (BG0-BG1 in x4/8 and BG0 in x16 select the bankgroup; BA0-BA1 select the bank; A0-A17 select the row; refer to "DDR4 SDRAM Addressing" on Section 2.8 for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

JESD79-4D, p. 11.

30. Additionally, the Accused Products including DDR4 memory controllers, including the TI AM6442 processor, include a second circuit to receive data sent by the memory component via an external bus, the data sent by the memory component in response to the read command. A read command presented to a DDR4 SDRAM causes the DDR4 SDRAM to convey an addressed

memory location to its pins for conveyance to the memory controller, as described in Section 4.24 of JESD79-4.



JESD79-4D, p. 96.

The DQ lines are defined as Data Input/Output lines that bi-directionally carry data into and out of the DRAM. For Read commands, the data is output on the DQ lines and conveyed on an external bus comprised of signal traces to the memory controller. The DQ pins of the DDR4 SDRAMs are connected to DDR0_DQ pins via said external bus.

Table 3 — Pinout Description (Cont'd)

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used.

JESD79-4D, p. 6.

6.3.2 DDRSS

6.3.2.1 MAIN Domain

Table 6-3. DDRSS0 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	ALV
DDR0_DQ0	IO	DDRSS Data	A3
DDR0_DQ1	IO	DDRSS Data	A2
DDR0_DQ2	IO	DDRSS Data	B5
DDR0_DQ3	IO	DDRSS Data	A4
DDR0_DQ4	IO	DDRSS Data	B3
DDR0_DQ5	IO	DDRSS Data	C4
DDR0_DQ6	IO	DDRSS Data	C2
DDR0_DQ7	IO	DDRSS Data	B4
DDR0_DQ8	IO	DDRSS Data	N5
DDR0_DQ9	IO	DDRSS Data	L4
DDR0_DQ10	IO	DDRSS Data	L2
DDR0_DQ11	IO	DDRSS Data	M3
DDR0_DQ12	IO	DDRSS Data	N4
DDR0_DQ13	IO	DDRSS Data	N3
DDR0_DQ14	IO	DDRSS Data	M4
DDR0_DQ15	IO	DDRSS Data	N2

AM64x Sitara Processors Datasheet, SPRSP56B, August 2021, pp. 74-75.

These pins located in the DDR4 SDRAM Memory Interface within the Accused Products, including the AM6442 processor, necessarily have a second circuit to receive the data being sent from the memory component as a result of a Read command.

31. Additionally, the Accused Products including DDR4 memory controllers, including the TI AM6442 processor, include calibration circuitry, operable during calibration, to receive at least a first data pattern and a second data pattern from the memory component. DDR4 SDRAMs include a calibration mode called DQ Read Training. Read Training is performed as part of power-up initialization:

3.3.1 Power-up Initialization Sequence

The following sequence is required for POWER UP and Initialization and is shown in Figure 7.

1. Apply power (RESET_n and TEN are recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). RESET_n needs to be maintained below 0.2 x VDD for minimum 200us with stable power and TEN needs to be maintained below 0.2 x VDD for minimum 700us with stable power. CKE is pulled "Low" anytime before RESET_n being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to V_{DD} min must be no greater than 200ms; and during the ramp, $V_{DD} \geq V_{DDQ}$ and $(V_{DD}-V_{DDQ}) < 0.3$volts. VPP must ramp at the same time or earlier than VDD and VPP must be equal to or higher than VDD at all times.

15. The DDR4 SDRAM is now ready for read/Write training (include Vref training and Write leveling).

JESD79-4D, pp. 11-12.

32. Read DQ Training is the mechanism by which the DDR4 memory controllers, including the TI AM6442, adjust their receive timing to reliably capture read data from the memory components. The circuitry in the DDR4 memory controller coupled to the DQ receivers that calibrates the DQ receivers is the claimed calibration circuitry.

33. Additionally, the Accused Products including DDR4 memory controllers include pattern register circuitry. In DDR4 SDRAMs the Multi-Purpose Register (MPR) is a collection of 4-four 8-bit registers that provide the data source for DQ Training data patterns.

4.10 Multi Purpose Register

4.10.1 DQ Training with MPR

The DDR4 DRAM contains four 8bit programmable MPR registers used for DQ bit pattern storage. These registers once programmed are activated with MRS read commands to drive the MPR bits on to the DQ bus during link training.

And DDR4 SDRAM only supports following command, MRS, RD, RDA WR, WRA, DES, REF and Reset during MPR enable Mode: MR3 [A2 = 1].

Note that in MPR mode RDA/WRA has the same functionality as a READ/WRITE command which means the auto precharge part of RDA/WRA is ignored. Power-Down mode and Self-Refresh command also is not allowed during MPR enable Mode. No other command can be issued within tRFC after REF command and 1x Refresh is only allowed when MPR mode is Enable. During MPR operations, MPR read or write sequence must be complete prior to a refresh command.

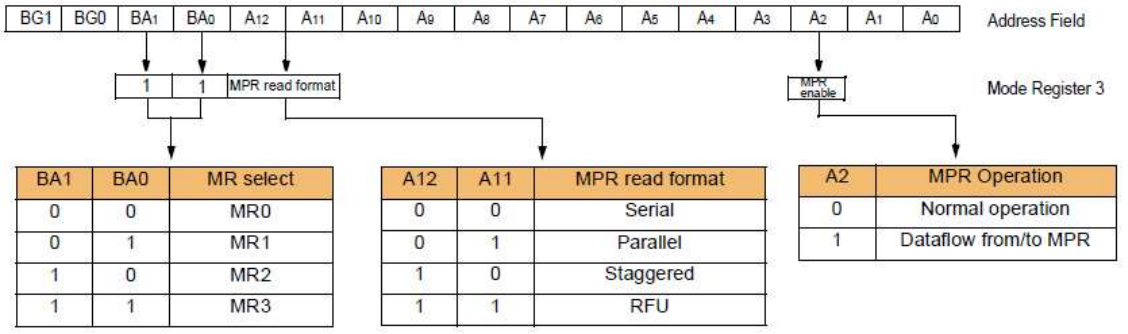
JESD79-4D, p. 43.

The contents of at least two of the MPRs are the first data pattern and the second data pattern in the memory component. The MPR functional unit, including the two MPRs, is thus the pattern register circuitry. Mode register 3 (MR3) in the DDR4 SDRAMs is used to control the programming of the MPR registers:

4.10.2 MR3 definition

Mode register MR3 controls the Multi-Purpose Registers (MPR) used for training. MR3 is written by asserting CS_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 low, ACT_n, BA0 and BA1 high and BG1[1] and BG0 low while controlling the states of the address pins according to Table 44.

Table 44 — MR3 Programming



BA1	BA0	MR select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A12	A11	MPR read format
0	0	Serial
0	1	Parallel
1	0	Staggered
1	1	RFU

A2	MPR Operation
0	Normal operation
1	Dataflow from/to MPR

Read or Write with MPR LOCATION :

A1	A0	MPR Page Selection
0	0	Page 0
0	1	Page 1
1	0	Page 2
1	1	Page 3

Default value for MPR0 @ Page0= 01010101
Default value for MPR1 @ Page0 = 00110011
Default value for MPR2 @ Page0 = 00001111
Default value for MPR3 @ Page0 = 00000000

JESD79-4D, p. 43.

The command that sets the MR3 mode register A2 bit to 1 to direct dataflow to be to and from the MPR from and onto the DQ pins is a precursor to the read command that causes the contents of the MPR to flow onto DQ pins of the DDR4 SDRAM. In DQ Training, the memory controller can use the default values of the different MPR registers, or program them to other values. These values are communicated from the DDR4 SDRAM memory components to the memory controller on the DQ external bus as a result of MPR Read operations:

4.10.3 MPR Reads

MPR reads are supported using BL8 and BC4(Fixed) modes. BC4 on the fly is not supported for MPR reads.

In MPR Mode:

Reads (back-to-back) from Page 0 may use tCCD_S or tCCD_L timing between read commands; Reads (back-to-back) from Pages 1, 2, or 3 may not use tCCD_S timing between read commands; tCCD_L must be used for timing between read commands

MPR reads using BC4:

BA1 and BA0 indicate the MPR location within the selected page in MPR Mode.

A10 and other address pins are don't care including BG1 and BG0.

Read commands for BC4 are supported with starting column address of A2:A0 of '000' and '100'.

Data Bus Inversion (DBI) is not allowed during MPR Read operation. During MPR Read, DRAM ignores Read DBI Enable setting in MR5 bit A12 in MPR mode.

DDR4 MPR mode is enabled by programming bit A2=1 and then reads are done from a specific MPR location.
MPR location is specified with the Read command using Bank address bits BA1 and BA0.

Each MPR location is 8 bit wide.

JESD79-4D, p. 44.

Read command

- A[1:0] = '00'b (data burst order is fixed starting at nibble, always 00b here)
- A[2]= '0'b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)
  (For BC=4, burst order is fixed at 0,1,2,3,T,T,T,T)

or

- A[2]= 1 (For BL=8 : Not Support)
  (For BC=4, burst order is fixed at 4,5,6,7,T,T,T,T)
- A12/BC= 0 or 1 : Burst length supports only BL8 and BC4(Fixed), not supports BC4(OTF).

When MR0 A[1:0] is set "01" , A12/BC must be always '1'b in MPR read commands (BL8 only).

- BA1 and BA0 indicate the MPR location
- A10 and other address pins are don't care including BG1and BG0

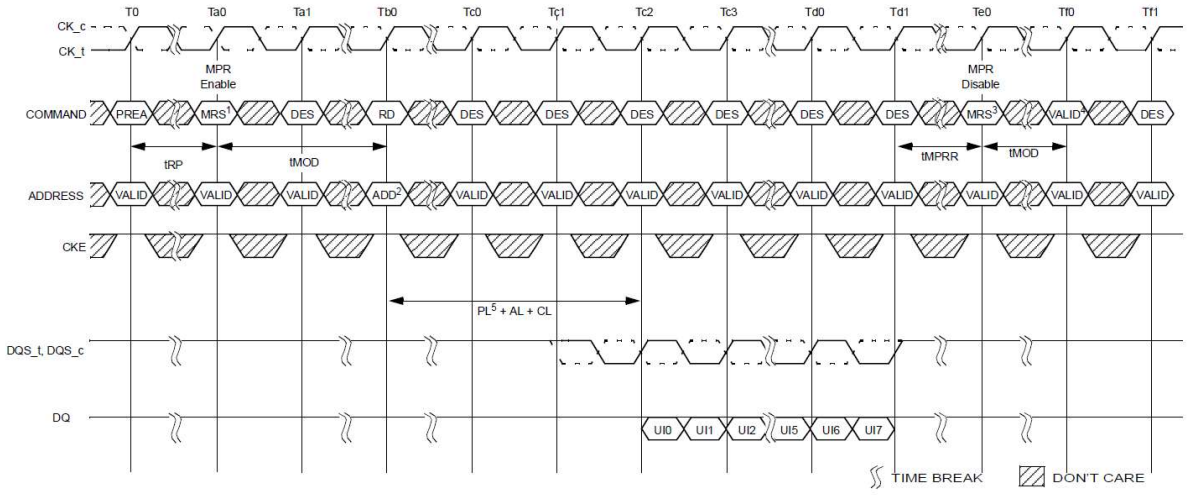
JESD79-4D, p. 44.

Memory controller repeats these calibration reads until read data capture at memory controller is optimized. Read MPR location can be a different location as specified by the Read command

JESD79-4D, p. 44.

4.10.3 MPR Reads (cont'd)

This process is depicted below(PL=0).



NOTE 1 Multi-Purpose Registers Read/Write Enable (MR3 A2 = 1)
- Redirect all subsequent read and writes to MPR locations

NOTE 2 Address setting
- A[1:0] = "00"b (data burst order is fixed starting at nibble, always 00b here)
- A[2]= "0"b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)
- BA1 and BA0 indicate the MPR location
- A10 and other address pins are don't care including BG1 and BG0. A12 is don't care when MR0 A[1:0] = "00" or "10" , and must be '1'b when MR0 A[1:0] = "01"

JESD79-4D, p. 45.

Once the MR3 A2 bit is set to 0, a selected one of the first data pattern and the second data pattern is transmitted by the memory component from an MPR register onto the external bus in response to a RD (Read) command. Once such command is, illustrated above, being provided to the memory component at time Tb0.

34. Defendant has and continues to indirectly infringe one or more claims of the '248 Patent by knowingly and intentionally inducing others, including TI customers and end-users, to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products.

35. Defendant, with knowledge that these products, or the use thereof, infringe the '248 Patent at least as of the date of this Complaint, knowingly and intentionally induced, and continues

to knowingly and intentionally induce, direct infringement of the '248 Patent by providing these products to end-users for use in an infringing manner.

36. Rampart has suffered damages as a result of Defendant's direct and indirect infringement of the '248 Patent in an amount to be proved at trial.

37. Rampart has suffered, and will continue to suffer, irreparable harm as a result of Defendant's infringement of the '248 Patent for which there is no adequate remedy at law, unless Defendant's infringement is enjoined by this Court.

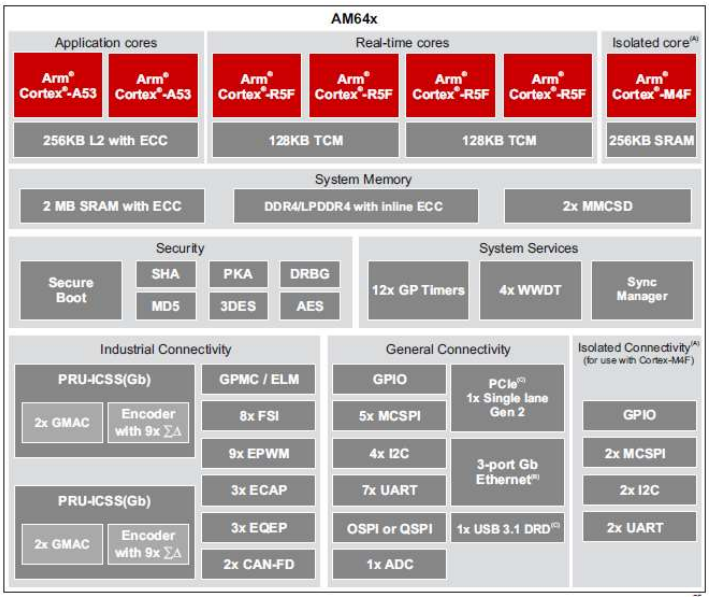
COUNT II
(Infringement of the '642 Patent)

38. Paragraphs 1 through 23 are incorporated by reference as if fully set forth herein.

39. Rampart has not licensed or otherwise authorized Defendant to make, use, offer for sale, sell, or import any products that embody the inventions of the '642 Patent.

40. Defendant has and continues to directly infringe the '642 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products including, but not limited to, products supporting DDR4 external memories, such as the TI AM6442, AM6441, AM6421, AM6412, and AM6411 Sitara Processors.

41. For example, Defendant has and continues to directly infringe at least Claim 1 of the '642 Patent by making, using, offering to sell, selling, and/or importing into the United States products that include a memory controller that complies with the DDR4 standard. For example, the TI AM6442 includes DDR4 external memory controllers capable of controlling a memory system consisting of DDR4 SDRAMs, each of which is compliant with the JEDEC standard JESD79-4, as shown by the AM64x Sitara Processors Datasheet, SPRSP56B (dated August, 2021) p.5:



Memory subsystem:

- Up to 2MB of On-chip RAM (OCSRAM) with SECDED ECC:
  - Can be divided into smaller banks in increments of 256KB for as many as 8 separate memory banks
  - Each memory bank can be allocated to a single core to facilitate software task partitioning
- DDR Subsystem (DDRSS)
  - Supports LPDDR4, DDR4 memory types
  - 16-Bit data bus with inline ECC
  - Supports speeds up to 1600 MT/s

AM64x Sitara Processors Datasheet, SPRSP56B, August 2021, page 1.

Table 5-1. Device Comparison

FEATURES	REFERENCE NAME	AM6442	AM6441	AM6422	AM6421	AM6412	AM6411
CTRLMMR_WKUP_JTAG_DEVICE_ID[31:13] DEVICE_ID register bit field value(1)		D: 0x19464 E: 0x19465 F: 0x19466	D: 0x19264 E: 0x19265 F: 0x19266	C: 0x19423	D: 0x19224 E: 0x19225 F: 0x19226	C: 0x19403	C: 0x19203
PROCESSORS AND ACCELERATORS							
Speed Grades		See Table 7-1					
Arm Cortex-A53 Microprocessor Subsystem	Arm A53	Dual Core	Single Core	Dual Core	Single Core	Dual Core	Single Core
Arm Cortex-R5F	Arm R5F	2 x Dual Core	2 x Dual Core	1 x Dual Core	1 x Dual Core	Single Core	Single Core
Arm Cortex-M4F	Arm M4F	Single Core					
Device Management Security Controller	DMSC-L	Yes					
Cryto Accelerators	Security	Yes					
MCU domain with Arm Cortex-M4F	Safety	Yes					
PROGRAM AND DATA STORAGE							
On-Chip Shared Memory (RAM) in MAIN Domain	OCSRAM	2MB					
R5F Tightly Coupled Memory (TCM)	TCM	256KB	256KB	256KB	256KB	128KB	128KB
On-Chip Shared Memory (RAM) in M4F Domain	MCU_MSRAM	256KB					
DDR4/LPDDR4 DDR Subsystem	DDRSS	Up to 2GB (16-bit data) with inline ECC					

AM64x Sitara Processors Datasheet, SPRSP56B, August 2021, page 7.

42. The required characteristics of DDR4 memories and memory systems and, therefore, of DDR4 memory controllers and their encompassing integrated circuits are defined by JEDEC in a collection of publicly available standards. In particular, standard JESD79-4 is the standard defining DDR4 SDRAMs, and JESD79-4D is the latest version of that standard, dated July 2021.

This document defines the DDR4 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this Standard is to define the minimum set of requirements for JEDEC compliant 2 Gb through 16 Gb for x4, x8, and x16 DDR4 SDRAM devices. This standard was created based on the DDR3 standards (JESD79-3) and some aspects of the DDR and DDR2 standards (JESD79, JESD79-2).

JESD79-4D page 1.

43. The Accused Products including DDR4 memory controllers, including the TI AM6442, include a first circuit to transmit commands to the memory component, the commands including a Read command that specifies data to be accessed from a memory core of the memory component. DDR4 SDRAM memory controllers, including the TI AM6442 processor, include a first circuit, which is a driver circuit that sends commands to the DDR4 SDRAMs by outputting signals onto command pins DDR0_RAS_n, DDR0_CAS_n, and DDR0_WE_n:

6.3.2 DDRSS

6.3.2.1 MAIN Domain

Table 6-3. DDRSS0 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	ALV
DDR0_ACT_n	O	DDRSS Activation Command	H2
DDR0_ALERT_n	IO	DDRSS Alert	H1
DDR0_CAS_n	O	DDRSS Column Address Strobe	J5
DDR0_PAR	O	DDRSS Command and Address Parity	K5
DDR0_RAS_n	O	DDRSS Row Address Strobe	F6
DDR0_WE_n	O	DDRSS Write Enable	H4

AM64x Sitara Processors Datasheet, SPRSP56B, August 2021, p. 74.

JESD79-4 refers to these signals at the DDR4 SDRAMs, as RAS_n/A16, CAS_n/A15, and WE_n/A14.

2.7 Pinout Description

Table 3 — Pinout Description

Symbol	Type	Function
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS_n/ A15. WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table
		Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data

JESD79-4D p. 5.

4.1 Command Truth Table

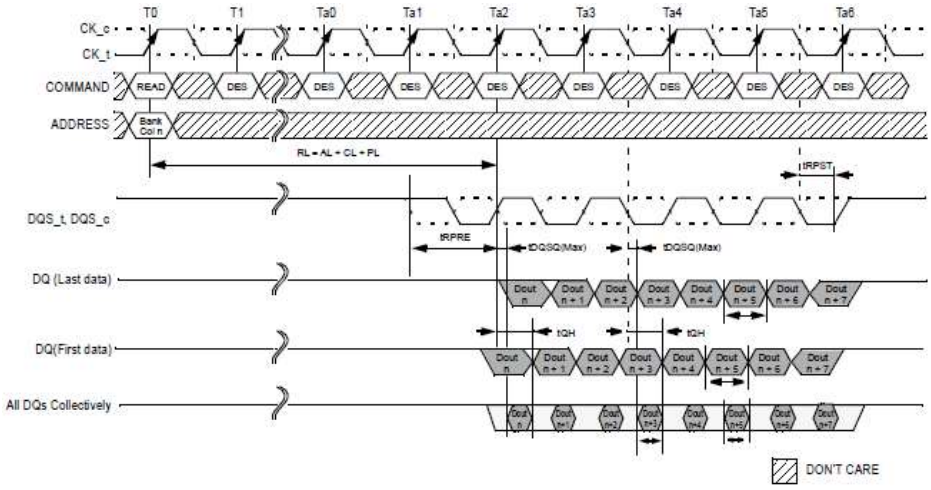
(a) Note 1,2,3 and 4 apply to the entire Command truth table
(b) Note 5 applies to all Read/Write commands.
[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, BC_n=Burst Chop, X=Don't Care, V=Valid].

Table 35 — Command Truth Table

Function	Abbreviation	CKE		CS_n	ACT_n	RAS_n /A16	CAS_n /A15	WE_n/ A14	BG0-BG1	BA0-BA1	C2-C0	A12/ BC_n	A17, A13, A11	A10/ AP	A0-A9	NOTE
		Previous Cycle	Current Cycle													
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V	OP Code				12
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	7,9
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	7,8,9, 10
				L	H	H	H	H	V	V	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	L	V	
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	H	V	
RFU	RFU	H	H	L	H	L	H	H	RFU							
Bank Activate	ACT	H	H	L	L	Row Address (RA)			BG	BA	V	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	6
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	6
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	H	V	
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	L	V	

JESD79-4D, p. 29.

44. The Accused Products including DDR4 memory controllers include circuits that drive these command signals toward the DDR4 SDRAMs. Among the commands that DDR4 SDRAMs can respond to are Read commands. A Read command is provided to a DDR4 SDRAM by sending a command in which ACT_n is H, RAS_n/A16 is H, CAS_n/A15 is L, and WE_n/A14 is H, where H and L represent voltage levels representing logic states, as defined in section 8 of JESD79-4. A Read command presented to a DDR4 SDRAM causes it to convey an addressed memory location to its pins for conveyance to the memory controller, as described in Section 4.24 of JESD79-4:



JESD79-4D, p. 96.

The DDR4 SDRAMs have a memory core consisting of 16 banks. Read operations are burst oriented, beginning at a selected location within the memory code:

3.2 Basic Functionality

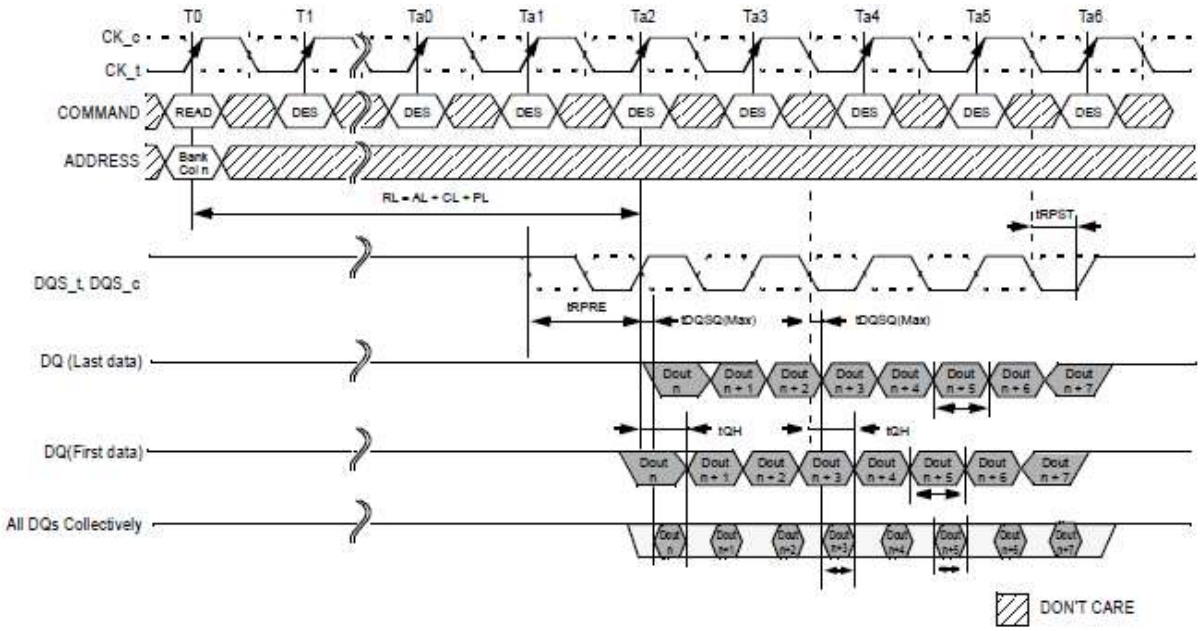
The DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as sixteen-banks, 4 bank group with 4 banks for each bank group for x4/x8 and eight-banks, 2 bank group with 4 banks for each bankgroup for x16 DRAM.

The DDR4 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR4 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered coincident with the ACTIVATE Command are used to select the bank and row to be activated (BG0-BG1 in x4/8 and BG0 in x16 select the bankgroup; BA0-BA1 select the bank; A0-A17 select the row; refer to "DDR4 SDRAM Addressing" on Section 2.8 for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

JESD79-4D, pg. 11.

45. Additionally, the Accused Products including DDR4 memory controllers, including the TI AM6442, include a second circuit to receive data sent by the memory component via an external bus, the data sent by the memory component in response to the Read command. A Read command presented to a DDR4 SDRAM by DDR4 SDRAM memory controllers, causes the DDR4 SDRAM to convey an addressed memory location to its pins for conveyance to the memory controller, as described in Section 4.24 of JESD79-4. The Accused Products, including the TI AM6442, necessarily have a second circuit to receive the data being sent from the memory component as a result of a Read command.



JESD79-4D, p. 96.

The DQ lines are defined as Data Input/Output lines that bi-directionally carry data into and out of the DRAM. For Read commands, the data is output on the DQ lines and conveyed on an external bus comprised of signal traces to the memory controller. The DQ pins of the DDR4 SDRAMs are connected to DDR0_DQ pins via said external bus. These pins in the DDR SDRAM Memory Interface necessarily have circuitry within the AM6442 processor to receive the data being sent from the memory component as a result of a read command. This circuitry is the second circuit.

Table 3 — Pinout Description (Cont'd)

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used.

JESD79-4D, p. 6.

6.3.2 DDRSS

6.3.2.1 MAIN Domain

Table 6-3. DDRSS0 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	ALV
DDR0_DQ0	IO	DDRSS Data	A3
DDR0_DQ1	IO	DDRSS Data	A2
DDR0_DQ2	IO	DDRSS Data	B5
DDR0_DQ3	IO	DDRSS Data	A4
DDR0_DQ4	IO	DDRSS Data	B3
DDR0_DQ5	IO	DDRSS Data	C4
DDR0_DQ6	IO	DDRSS Data	C2
DDR0_DQ7	IO	DDRSS Data	B4
DDR0_DQ8	IO	DDRSS Data	N5
DDR0_DQ9	IO	DDRSS Data	L4
DDR0_DQ10	IO	DDRSS Data	L2
DDR0_DQ11	IO	DDRSS Data	M3
DDR0_DQ12	IO	DDRSS Data	N4
DDR0_DQ13	IO	DDRSS Data	N3
DDR0_DQ14	IO	DDRSS Data	M4
DDR0_DQ15	IO	DDRSS Data	N2

AM64x Sitara Processors Datasheet, SPRSP56B, August 2021, pp. 74-75.

46. Additionally, the Accused Products including DDR4 memory controllers, including the TI AM6442, include calibration circuitry, operable during calibration, to receive from the memory component, in response to one of the commands, a pattern selected from at least one of a first data pattern and a second data pattern and to, based on the selected pattern, adjust a timing of a timing reference signal for sampling the data at the second receive circuit, wherein the timing of the timing reference signal is initially set using an initial calibration sequence and then updated during one or more subsequent calibration sequences. DDR4 SDRAMs include a calibration mode called DQ Read Training (also known as Read Leveling). Read Training is performed as part of power-up initialization:

3.3.1 Power-up Initialization Sequence

The following sequence is required for POWER UP and Initialization and is shown in Figure 7.

1. Apply power (RESET_n and TEN are recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). RESET_n needs to be maintained below 0.2 x VDD for minimum 200us with stable power and TEN needs to be maintained below 0.2 x VDD for minimum 700us with stable power. CKE is pulled "Low" anytime before RESET_n being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to V_{DD} min must be no greater than 200ms; and during the ramp, $V_{DD} \geq V_{DDQ}$ and $(V_{DD}-V_{DDQ}) < 0.3$volts. VPP must ramp at the same time or earlier than VDD and VPP must be equal to or higher than VDD at all times.

15. The DDR4 SDRAM is now ready for read/Write training (include Vref training and Write leveling).

JESD79-4D, pp. 11-12.

47. Read DQ Training is the mechanism by which the DDR4 memory controllers, including the TI AM6442, adjust their receive timing to reliably capture read data from the memory components. The circuitry in the DDR4 memory controller coupled to the DQ receivers that calibrates the DQ receivers is the claimed calibration circuitry.

48. Additionally, the Accused Products including DDR4 memory controllers include pattern register circuitry. The Multi-Purpose Register (MPR) is a collection of 4-four 8-bit registers that provide the data source for DQ Training data patterns.

4.10 Multi Purpose Register

4.10.1 DQ Training with MPR

The DDR4 DRAM contains four 8bit programmable MPR registers used for DQ bit pattern storage. These registers once programmed are activated with MRS read commands to drive the MPR bits on to the DQ bus during link training.

And DDR4 SDRAM only supports following command, MRS, RD, RDA WR, WRA, DES, REF and Reset during MPR enable Mode: MR3 [A2 = 1].

Note that in MPR mode RDA/WRA has the same functionality as a READ/WRITE command which means the auto precharge part of RDA/WRA is ignored. Power-Down mode and Self-Refresh command also is not allowed during MPR enable Mode. No other command can be issued within tRFC after REF command and 1x Refresh is only allowed when MPR mode is Enable. During MPR operations, MPR read or write sequence must be complete prior to a refresh command.

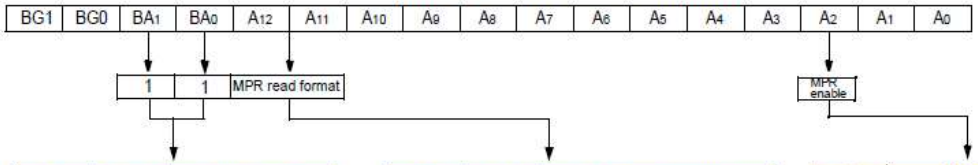
JESD79-4D, p. 43.

The contents of at least two of the MPRs are the first data pattern and the second data pattern in the memory component. Mode register 3 (MR3) in the DDR4 SDRAMs is used to control the programming of the MPR registers:

4.10.2 MR3 definition

Mode register MR3 controls the Multi-Purpose Registers (MPR) used for training. MR3 is written by asserting CS_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 low, ACT_n, BA0 and BA1 high and BG1[1] and BG0 low while controlling the states of the address pins according to Table 44.

Table 44 — MR3 Programming



BA1	BA0	MR select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A12	A11	MPR read format
0	0	Serial
0	1	Parallel
1	0	Staggered
1	1	RFU

A2	MPR Operation
0	Normal operation
1	Dataflow from/to MPR

Read or Write with MPR LOCATION :

A1	A0	MPR Page Selection
0	0	Page 0
0	1	Page 1
1	0	Page 2
1	1	Page 3

Default value for MPR0 @ Page0= 01010101
Default value for MPR1 @ Page0 = 00110011
Default value for MPR2 @ Page0 = 00001111
Default value for MPR3 @ Page0 = 00000000

JESD79-4D, p. 43.

The command that sets the MR3 mode register A2 bit to 1 to direct dataflow to and from the MPR from and onto the DQ pins is a precursor to the Read command that causes the contents of the MPR to flow onto DQ pins of the DDR4 SDRAM.

49. In DQ Training, the memory controller can use the default values of the different MPR registers, or program them to other values. These values are communicated from the DDR4 SDRAM memory components to the memory controller on the DQ external bus as a result of MPR Read operations:

4.10.3 MPR Reads

MPR reads are supported using BL8 and BC4(Fixed) modes. BC4 on the fly is not supported for MPR reads.

In MPR Mode:

Reads (back-to-back) from Page 0 may use tCCD_S or tCCD_L timing between read commands; Reads (back-to-back) from Pages 1, 2, or 3 may not use tCCD_S timing between read commands; tCCD_L must be used for timing between read commands

MPR reads using BC4:

BA1 and BA0 indicate the MPR location within the selected page in MPR Mode.

A10 and other address pins are don't care including BG1 and BG0.

Read commands for BC4 are supported with starting column address of A2:A0 of '000' and '100'.

Data Bus Inversion (DBI) is not allowed during MPR Read operation. During MPR Read, DRAM ignores Read DBI Enable setting in MR5 bit A12 in MPR mode.

DDR4 MPR mode is enabled by programming bit A2=1 and then reads are done from a specific MPR location.
MPR location is specified with the Read command using Bank address bits BA1 and BA0.

Each MPR location is 8 bit wide.

JESD79-4D, p. 44.

Read command

- A[1:0] = '00'b (data burst order is fixed starting at nibble, always 00b here)
- A[2]= '0'b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)
  (For BC=4, burst order is fixed at 0,1,2,3,T,T,T,T)

or

- A[2]= 1 (For BL=8 : Not Support)
  (For BC=4, burst order is fixed at 4,5,6,7,T,T,T,T)
- A12/BC= 0 or 1 : Burst length supports only BL8 and BC4(Fixed), not supports BC4(OTF).

When MR0 A[1:0] is set "01" , A12/BC must be always '1'b in MPR read commands (BL8 only).

- BA1 and BA0 indicate the MPR location
- A10 and other address pins are don't care including BG1and BG0

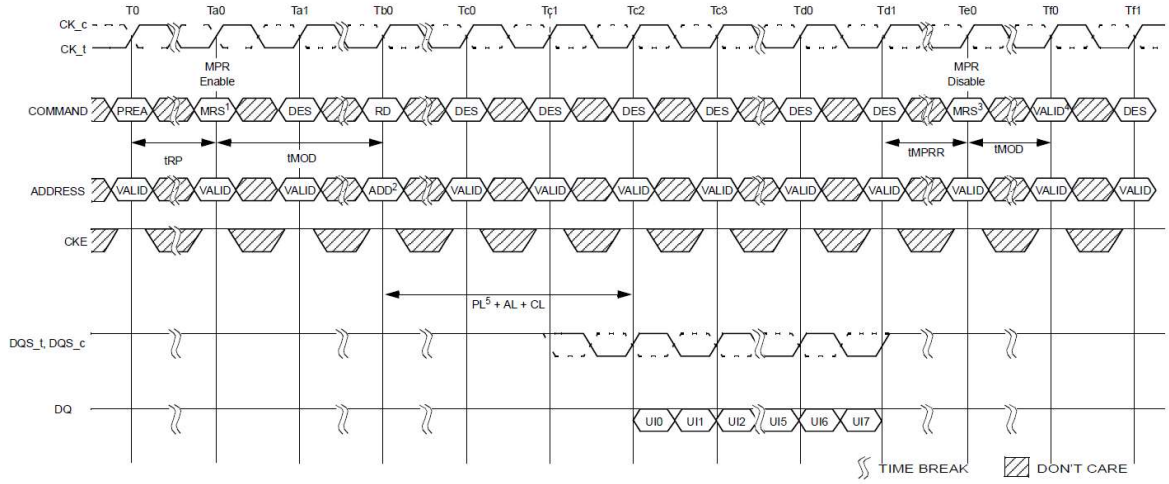
JESD79-4D, p. 44.

Memory controller repeats these calibration reads until read data capture at memory controller is optimized. Read MPR location can be a different location as specified by the Read command

JESD79-4D, p. 44.

4.10.3 MPR Reads (cont'd)

This process is depicted below(PL=0).



NOTE 1 Multi-Purpose Registers Read/Write Enable (MR3 A2 = 1)
- Redirect all subsequent read and writes to MPR locations

NOTE 2 Address setting
- A[1:0] = "00"b (data burst order is fixed starting at nibble, always 00b here)
- A[2]= "0"b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)
- BA1 and BA0 indicate the MPR location
- A10 and other address pins are don't care including BG1 and BG0. A12 is don't care when MR0 A[1:0] = "00" or "10" , and must be '1'b when MR0 A[1:0] = "01"

JESD79-4D, p. 45.

Once the MR3 A2 bit is set to 0, a selected one of the first data pattern and the second data pattern is transmitted by the memory component from an MPR register onto the external bus in response to a RD (read) command. Once such command is, illustrated above, being provided to the memory component at time Tb0.

51. Additionally, the Accused Products including DDR4 memory controllers, including the TI AM6442, include DQ Training to adjust a timing of a timing reference signal for sampling the data at the second receive circuit. The MPR data sequences are used during the DQ Training (Read Leveling) phase of initialization of a DDR4 memory subsystem. The timing reference signal in need of adjustment during initialization is the delay of the edges in the DQS signal to place them in the center of the eye of the DQ data signals so that the delayed DQS signals can reliably be used to sample the incoming read data from the DDR4 SDRAMs.

52. Defendant has and continues to indirectly infringe one or more claims of the ’642 Patent by knowingly and intentionally inducing others, including TI customers and end-users, to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products.

53. Defendant, with knowledge that these products, or the use thereof, infringe the ’642 Patent at least as of the date of this Complaint, knowingly and intentionally induced, and continues to knowingly and intentionally induce, direct infringement of the ’642 Patent by providing these products to end-users for use in an infringing manner.

54. Rampart has suffered damages as a result of Defendant’s direct and indirect infringement of the ’642 Patent in an amount to be proved at trial.

55. Rampart has suffered, and will continue to suffer, irreparable harm as a result of Defendant’s infringement of the ’642 Patent, for which there is no adequate remedy at law, unless Defendant’s infringement is enjoined by this Court.

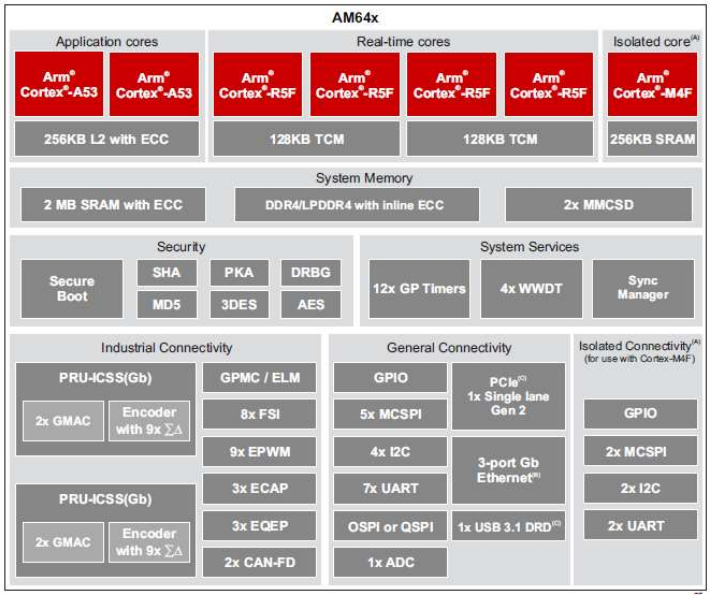
COUNT III
(Infringement of the ’609 Patent)

57. Paragraphs 1 through 23 are incorporated by reference as if fully set forth herein.

58. Rampart has not licensed or otherwise authorized Defendant to make, use, offer for sale, sell, or import any products that embody the inventions of the ’609 Patent.

59. Defendant has and continues to directly infringe the ’609 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products including, but not limited to, products supporting DDR4 external memories, such as the TI AM6442, AM6441, AM6421, AM6412, and AM6411 Sitara Processors.

60. For example, Defendant has and continues to directly infringe at least Claim 1 of the '609 Patent by making, using, offering to sell, selling, and/or importing into the United States products that include a memory controller that complies with the DDR4 standard. For example, the Accused Products, including the TI AM6442 includes DDR4 external memory controllers including a controller capable of controlling a memory system consisting of DDR4 SDRAMs, each of which is compliant with the JEDEC standard JESD79-4, as shown by the AM64x Sitara Processors Datasheet, SPRSP56B (August 2021, p.5):



Memory subsystem:

- Up to 2MB of On-chip RAM (OCSRAM) with SECDED ECC:
  - Can be divided into smaller banks in increments of 256KB for as many as 8 separate memory banks
  - Each memory bank can be allocated to a single core to facilitate software task partitioning
- DDR Subsystem (DDRSS)
  - Supports LPDDR4, DDR4 memory types
  - 16-Bit data bus with inline ECC
  - Supports speeds up to 1600 MT/s

AM64x Sitara Processors Datasheet, SPRSP56B, August 2021, p. 1.

Table 5-1. Device Comparison

FEATURES	REFERENCE NAME	AM6442	AM6441	AM6422	AM6421	AM6412	AM6411
CTRLMMR_WKUP_JTAG_DEVICE_ID[31:13] DEVICE_ID register bit field value[1]		D: 0x19464 E: 0x19465 F: 0x19466	D: 0x19264 E: 0x19265 F: 0x19266	C: 0x19423	D: 0x19224 E: 0x19225 F: 0x19226	C: 0x19403	C: 0x19203
PROCESSORS AND ACCELERATORS							
Speed Grades		See Table 7-1					
Arm Cortex-A53 Microprocessor Subsystem	Arm A53	Dual Core	Single Core	Dual Core	Single Core	Dual Core	Single Core
Arm Cortex-R5F	Arm R5F	2 x Dual Core	2 x Dual Core	1 x Dual Core	1 x Dual Core	Single Core	Single Core
Arm Cortex-M4F	Arm M4F	Single Core					
Device Management Security Controller	DMSC-L	Yes					
Cryto Accelerators	Security	Yes					
MCU domain with Arm Cortex-M4F	Safety	Yes					
PROGRAM AND DATA STORAGE							
On-Chip Shared Memory (RAM) in MAIN Domain	OCSRAM	2MB					
R5F Tightly Coupled Memory (TCM)	TCM	256KB	256KB	256KB	256KB	128KB	128KB
On-Chip Shared Memory (RAM) in M4F Domain	MCU_MSRAM	256KB					
DDR4/LPDDR4 DDR Subsystem	DDRSS	Up to 2GB (16-bit data) with inline ECC					

AM64x Sitara Processors Datasheet, SPRSP56B, August 2021, p. 7.

61. The required characteristics of DDR4 memories and memory systems and therefore of DDR4 memory controllers and their encompassing integrated circuits are defined by JEDEC in a collection of publicly available standards. In particular, standard JESD79-4 is the standard defining DDR4 SDRAMs, and JESD79-4D is the latest version of that standard, dated July 2021:

> This document defines the DDR4 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this Standard is to define the minimum set of requirements for JEDEC compliant 2 Gb through 16 Gb for x4, x8, and x16 DDR4 SDRAM devices. This standard was created based on the DDR3 standards (JESD79-3) and some aspects of the DDR and DDR2 standards (JESD79, JESD79-2).

JESD79-4D page 1.

62. The Accused Products including DDR4 memory controllers, including the TI AM6442 processor, include a first circuit to transmit commands to the memory component. DDR4 SDRAM memory controllers, including the AM6442 processor, include a first circuit which is a driver circuit that outputs signals onto the command pins DDR0_RAS_n. DDR0_CAS_n, and DDR0_WE_n:

6.3.2 DDRSS

6.3.2.1 MAIN Domain

Table 6-3. DDRSS0 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	ALV
DDR0_ACT_n	O	DDRSS Activation Command	H2
DDR0_ALERT_n	IO	DDRSS Alert	H1
DDR0_CAS_n	O	DDRSS Column Address Strobe	J5
DDR0_PAR	O	DDRSS Command and Address Parity	K5
DDR0_RAS_n	O	DDRSS Row Address Strobe	F6
DDR0_WE_n	O	DDRSS Write Enable	H4

AM64x Sitara Processors Datasheet, SPRSP56B, August 2021, p. 74.

JESD79-4 refers to these signals at the SDRAMs, as ACT_n, RAS_n/A16, CAS_n/A15, and WE_n/A14.

2.7 Pinout Description

Table 3 — Pinout Description

Symbol	Type	Function
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16, CAS_n/ A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table

JESD79-4D p. 5.

4.1 Command Truth Table

(a) Note 1,2,3 and 4 apply to the entire Command truth table

(b) Note 5 applies to all Read/Write commands.

[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, BC_n=Burst Chop, X=Don't Care, V=Valid].

Table 35 — Command Truth Table

Function	Abbreviation	CKE		CS_n	ACT_n	RAS_n /A16	CAS_n /A15	WE_n/ A14	BG0-BG1	BA0-BA1	C2-C0	A12/ BC_n	A17, A13, A11	A10/ AP	A0-A9	NOTE
		Previous Cycle	Current Cycle													
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V	OP Code				12
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	7,9
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	7,8,9, 10
				L	H	H	H	H	V	V	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	L	V	
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	H	V	
RFU	RFU	H	H	L	H	L	H	H	RFU							
Bank Activate	ACT	H	H	L	L	Row Address (RA)			BG	BA	V	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	6
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	6
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	H	V	
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	L	V	

JESD79-4D, p. 29.

63. Additionally, the Accused Products including DDR4 memory controllers, including the TI AM6442, initiate a first command that specifies a first data pattern to be stored in a first register of the memory component. DDR4 SDRAMs, including DDR4 SDRAMs used with the TI AM6442 processor, include a Multi-Purpose Register (MPR) for storing bit patterns for use in initialization/channel calibration:

4.10 Multi Purpose Register

4.10.1 DQ Training with MPR

The DDR4 DRAM contains four 8bit programmable MPR registers used for DQ bit pattern storage. These registers once programmed are activated with MRS read commands to drive the MPR bits on to the DQ bus during link training.

And DDR4 SDRAM only supports following command, MRS, RD, RDA WR, WRA, DES, REF and Reset during MPR enable Mode: MR3 [A2 = 1].

Note that in MPR mode RDA/WRA has the same functionality as a READ/WRITE command which means the auto precharge part of RDA/WRA is ignored. Power-Down mode and Self-Refresh command also is not allowed during MPR enable Mode. No other command can be issued within tRFC after REF command and 1x Refresh is only allowed when MPR mode is Enable. During MPR operations, MPR read or write sequence must be complete prior to a refresh command.

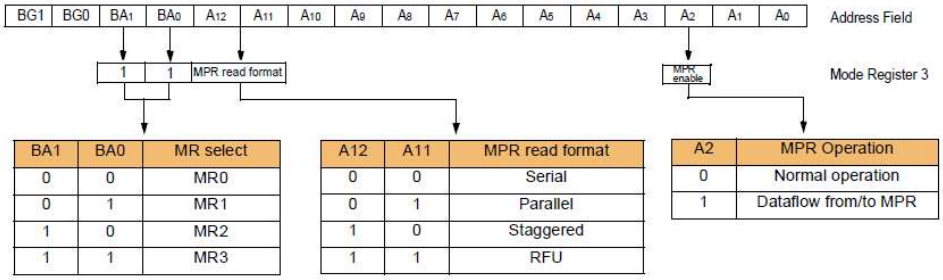
JESD79-4D, p. 43.

Each of the four (4) MPR registers can be written by write command (WR) after the SDRAM is placed into appropriate mode, as indicated by a write into Mode Register 3 (MR3):

4.10.2 MR3 definition

Mode register MR3 controls the Multi-Purpose Registers (MPR) used for training. MR3 is written by asserting CS_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 low, ACT_n, BA0 and BA1 high and BG1[1] and BG0 low while controlling the states of the address pins according to Table 44.

Table 44 — MR3 Programming



BA1	BA0	MR select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A12	A11	MPR read format
0	0	Serial
0	1	Parallel
1	0	Staggered
1	1	RFU

A2	MPR Operation
0	Normal operation
1	Dataflow from/to MPR

Read or Write with MPR LOCATION :

A1	A0	MPR Page Selection
0	0	Page 0
0	1	Page 1
1	0	Page 2
1	1	Page 3

Default value for MPR0 @ Page0= 01010101
Default value for MPR1 @ Page0 = 00110011
Default value for MPR2 @ Page0 = 00001111
Default value for MPR3 @ Page0 = 00000000

JESD79-4D, p. 43.

4.10.4 MPR Writes

DDR4 allows 8 bit writes to the MPR location using the address bus A7:A0.

Table 45 — UI and Address Mapping for MPR Location

MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
SDRAM Address	A7	A6	A5	A4	A3	A2	A1	A0
UI	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7

STEPS:
DLL must be locked prior to MPR Writes. If DLL is Enabled : MR1[A0 = 1]
Precharge all
Wait until tRP is satisfied
MRS MR3, Opcode A2='1'b
Redirect all subsequent read and writes to MPR locations

Wait until tMRD and tMOD satisfied.

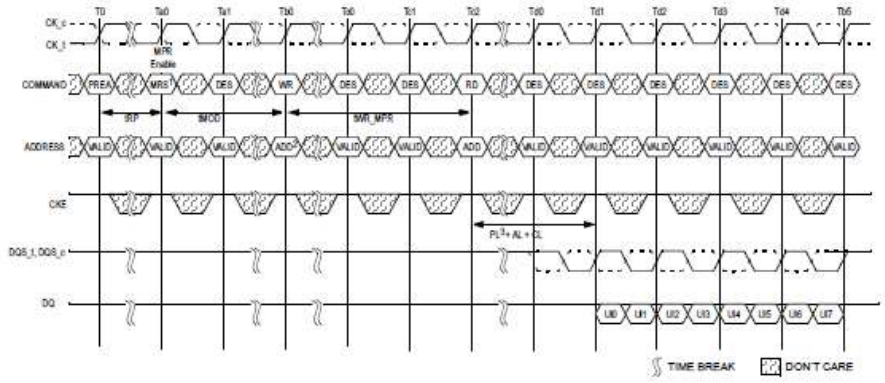
Write command
BA1 and BA0 indicate the MPR location
A [7:0] = data for MPR

Wait until tWR_MPR satisfied, so that DRAM to complete MPR write transaction.

Memory controller repeats these calibration writes and reads until data capture at memory controller is optimized.
After end of last MPR read burst, wait until tMPRR is satisfied
MRS MR3, Opcode A2= '0b'
All subsequent reads and writes from DRAM array

JESD79-4D, p. 46.

4.10.4 MPR Writes (cont'd)

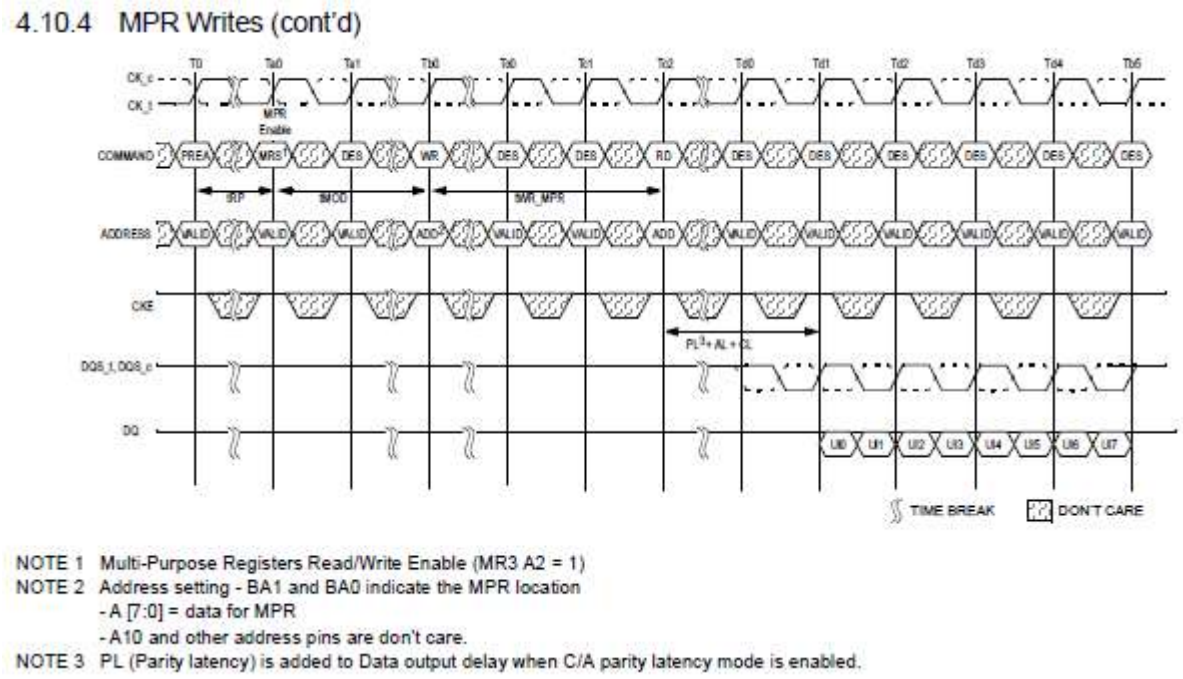


NOTE 1 Multi-Purpose Registers Read/Write Enable (MR3 A2 = 1)
NOTE 2 Address setting - BA1 and BA0 indicate the MPR location
- A [7:0] = data for MPR
- A10 and other address pins are don't care.
NOTE 3 PL (Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

JESD79-4D, p. 47.

During such a write command, as indicated at time Tb0, address signals BA1 and BA0 indicate which MPR register is to be written with the specified bit pattern provided on A[7:0]. The Accused Products, including the TI AM6442 processor, perform a write command writing a first one of the four MPR registers, which is a first command that specifies a first data pattern to be stored in a first register of the memory component.

64. Additionally, the Accused Products including DDR4 memory controllers initiate a second command that specifies a second data pattern to be stored in a second register of the memory component. Subsequent to the writing of a first MPR register with a first bit pattern, a second MPR is written with a second bit pattern with a second MPR register, as addressed by the BA1 and BA0 address bits in conjunction with the Write command:

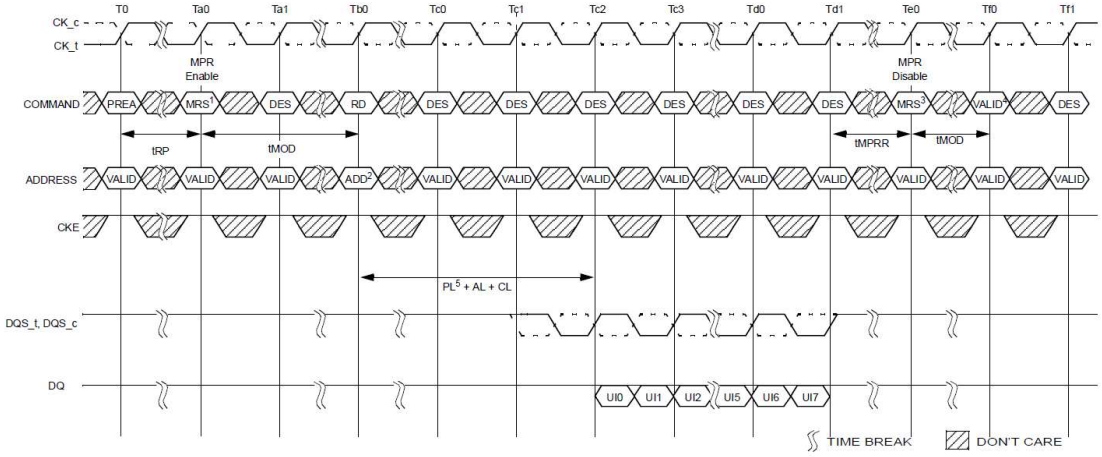


JESD79-4D, p. 47.

65. Additionally, the Accused Products including DDR4 memory controllers initiate a third command to select one of the first data pattern or the second data pattern to be output by the memory component. Subsequent to the writing of the MPR registers with desired bit patterns, the contents of the MPR registers are read out with Read commands (RD) onto the DQ lines for use in DQ Training. Once the MR3 A2 bit is set to 0, a selected one of the first data pattern and the second data pattern is transmitted by the memory component from an MPR register onto the external bus in response to a RD (read) command. One such command is illustrated below as being provided to the memory component at time Tb0.

4.10.3 MPR Reads (cont'd)

This process is depicted below(PL=0).



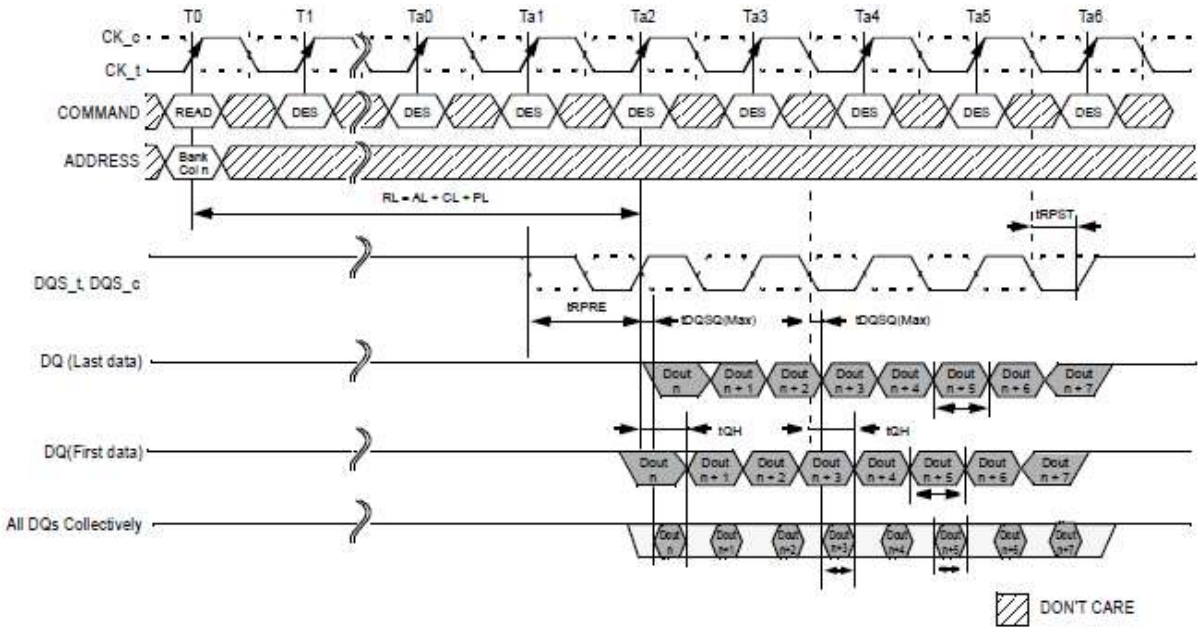
NOTE 1 Multi-Purpose Registers Read/Write Enable (MR3 A2 = 1)
- Redirect all subsequent read and writes to MPR locations

NOTE 2 Address setting
- A[1:0] = "00"b (data burst order is fixed starting at nibble, always 00b here)
- A[2]= "0"b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)
- BA1 and BA0 indicate the MPR location
- A10 and other address pins are don't care including BG1 and BG0. A12 is don't care when MR0 A[1:0] = "00" or "10" , and must be '1'b when MR0 A[1:0] = "01"

JESD79-4D, page 45.

A RD command while MPR mode is enabled, outputting the contents of either the first or the second MPR register previously written by a WR command is a third command to select one of the first data pattern or the second data pattern to be output by the memory component.

66. Additionally, the Accused Products including DDR4 memory controllers, including the AM6442, include a second circuit to receive from the memory component as a received data pattern, the one of the first data pattern or the second data pattern output by the memory component as selected by the third command. A Read command presented to a DDR4 SDRAM causes it to convey an addressed memory location or MPR register to its pins for conveyance to the memory controller, as described in Section 4.24 of JESD79-4.



JESD79-4D, pg. 96.

The DQ lines are defined as Data Input/Output lines that bi-directionally carry data into and out of the DRAM. For Read commands, the data is output on the DQ lines and conveyed on an external bus comprised of signal traces to the memory controller.

Table 3 — Pinout Description (Cont'd)

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used.

JESD79-4D, p. 6.

The DQ pins of the DDR4 SDRAMs are connected to DDR0_DQ pins via said external bus.

6.3.2 DDRSS

6.3.2.1 MAIN Domain

Table 6-3. DDRSS0 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	ALV
DDR0_DQ0	IO	DDRSS Data	A3
DDR0_DQ1	IO	DDRSS Data	A2
DDR0_DQ2	IO	DDRSS Data	B5
DDR0_DQ3	IO	DDRSS Data	A4
DDR0_DQ4	IO	DDRSS Data	B3
DDR0_DQ5	IO	DDRSS Data	C4
DDR0_DQ6	IO	DDRSS Data	C2
DDR0_DQ7	IO	DDRSS Data	B4
DDR0_DQ8	IO	DDRSS Data	N5
DDR0_DQ9	IO	DDRSS Data	L4
DDR0_DQ10	IO	DDRSS Data	L2
DDR0_DQ11	IO	DDRSS Data	M3
DDR0_DQ12	IO	DDRSS Data	N4
DDR0_DQ13	IO	DDRSS Data	N3
DDR0_DQ14	IO	DDRSS Data	M4
DDR0_DQ15	IO	DDRSS Data	N2

AM64x Sitara Processors Datasheet, SPRSP56B, August 2021, pp. 74-75.

These pins in the DDR SDRAM Memory Interface necessarily have circuitry within the TI AM6442 to receive the data being sent from the memory component, either memory core contents or MPR register contents, as a result of a read command. This circuitry is the second circuit.

67. Additionally, the Accused Products including DDR4 memory controllers, including the TI AM6442 processor, include calibration circuitry, operable during calibration, to receive a data pattern and adjust the timing of a timing reference signal for sampling data at the second circuit. DDR4 SDRAMs include a calibration mode called DQ Read Training (Read Leveling). Read Training is performed as part of power-up initialization:

3.3.1 Power-up Initialization Sequence

The following sequence is required for POWER UP and Initialization and is shown in Figure 7.

1. Apply power (RESET_n and TEN are recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). RESET_n needs to be maintained below 0.2 x VDD for minimum 200us with stable power and TEN needs to be maintained below 0.2 x VDD for minimum 700us with stable power. CKE is pulled "Low" anytime before RESET_n being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to V_{DD} min must be no greater than 200ms; and during the ramp, $V_{DD} \geq V_{DDQ}$ and (V_{DD}-V_{DDQ}) < 0.3volts. VPP must ramp at the same time or earlier than VDD and VPP must be equal to or higher than VDD at all times.

15. The DDR4 SDRAM is now ready for read/Write training (include Vref training and Write leveling).

JESD79-4D, p. 11-12.

Read DQ Training is the mechanism by which the DDR4 memory controller adjusts its receive timing to reliably capture read data from the memory components. The circuitry in the DDR4 memory controller coupled to the DQ receivers that calibrates the DQ receivers is the claimed calibration circuitry. The DDR Memory Controller in the Accused Products necessarily includes calibration circuitry operating on the received data pattern, to adjust a timing of a timing reference signal for sampling data at the second circuit as part of DQ Training.

68. Defendant has and continues to indirectly infringe one or more claims of the '609 Patent by knowingly and intentionally inducing others, including TI customers and end-users, to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products.

69. Defendant, with knowledge that these products, or the use thereof, infringe the '609 Patent at least as of the date of this Complaint, knowingly and intentionally induced, and continues to knowingly and intentionally induce, direct infringement of the '609 Patent by providing these products to end-users for use in an infringing manner.

70. Rampart has suffered damages as a result of Defendant's direct and indirect infringement of the '609 Patent in an amount to be proved at trial.

71. Rampart has suffered, and will continue to suffer, irreparable harm as a result of Defendant's infringement of the '609 Patent for which there is no adequate remedy at law, unless Defendant's infringement is enjoined by this Court.

COUNT IV
(Infringement of the '311 Patent)

72. Paragraphs 1 through 23 are incorporated by reference as if fully set forth herein.

73. Rampart has not licensed or otherwise authorized Defendant to make, use, offer for sale, sell, or import any products that embody the inventions of the ’311 Patent.

74. Defendant has and continues to directly infringe the ’311 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products including, but not limited to, products supporting the DDR3 and DDR3L external memories and a x32 or x64 bus, such as the TI DRA780, DRA781, DRA782, DRA783, DRA784, DRA785, DRA786, DRA787, DRA788, TMS320C6655, TMS320C6657, 66AK2G12, 66AK2H06, 66AK2H12, 66AK2H14, DRA744P, DRA745P, DRA746P, DRA750P, DRA751P, DRA752P, DRA754P, DRA755P, DRA756P, DRA710, DRA712, DRA714, DRA716, DRA724, DRA722, DRA725, DRA767P, DRA77xP, DRA790, DRA791, DRA793, DRA797, TDA2P-ABZ, TDA2P-ACD, TDA2EG-17, TDA2EG, TDA2EGABC, TDA2HF, TDA2SX, TDA2SG, TDA2SA, TDA2HG, TDA2HV, TDA2LF, AM4372, AM4376, AM4377, AM4378, AM4379, AM5748, AM5749, AM5706, AM5708, AM5716, AM5718, AM5726, AM5728, and AM5729.

75. For example, Defendant has and continues to directly infringe at least Claim 26 of the ’311 Patent by making, using, offering to sell, selling, and/or importing into the United States products that include a memory controller that complies with the DDR3 and DDR3L standard. For example, the TI 66AK2H06 SoC includes DDR3 and DDR3L external memory controllers capable of controlling a memory subsystem consisting of DDR3 SDRAMs, each of which is compliant with the JEDEC standard JESD79-3.

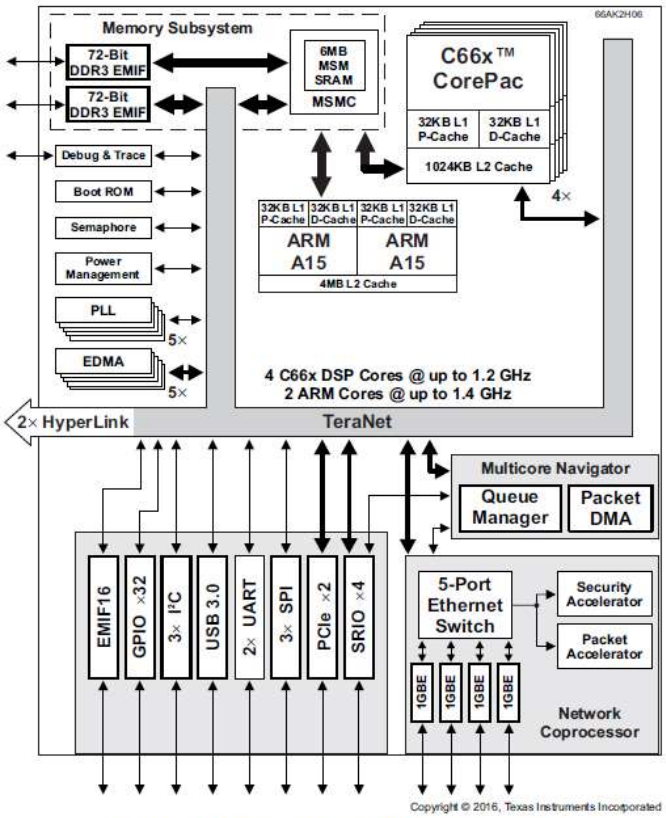


Figure 1-3. Functional Block Diagram for 66AK2H06

66AK2Hxx Multicore DSP+ARM® KeyStone™ II System-on-Chip (SoC), p. 5.

66AK2Hxx Multicore DSP+ARM® KeyStone™ II System-on-Chip (SoC)

1 Device Overview

1.1 Features

...

– Memory Protection Unit (MPU) for Both MSM SRAM and DDR3_EMIF

– Two 72-Bit DDR3/DDR3L Interfaces With Speeds up to 1600 MHz

66AK2Hxx Multicore DSP+ARM® KeyStone™ II System-on-Chip (SoC), p. 1.

11.9 DDR3A and DDR3B Memory Controllers

The 72-bit DDR3 memory controller bus of the 66AK2Hxx is used to interface to JEDEC standard-compliant DDR3 SDRAM devices. The DDR3 external bus interfaces only to DDR3 SDRAM devices and does not share the bus with any other type of peripheral.

66AK2Hxx Multicore DSP+ARM® KeyStone™ II System-on-Chip (SoC), p. 278.

76. The Accused Products including DDR3 memory controllers include a first transmitter to output first control information synchronously with respect to a first transition of a timing signal and second control information synchronously with respect to a second transition of

the timing signal. DDR3 SDRAM memory controllers, connected to the TI 66AK2H06, include a collection of control signals which provide control information to the memory components to direct their operation. A first set of control information is sent synchronously with the memory clock signal, which is the timing signal. Subsequently, a second set of control information is sent along the same control information signal lines synchronously with respect to a second transition of the memory clock. For example, the following timing diagram from the DDR3 SDRAM standard (JESD79-3) shows two consecutive write operations as a result to two separate write commands (control information) being transmitted on the command bus from a first transmitter, each synchronous with to CK/CK# signal.

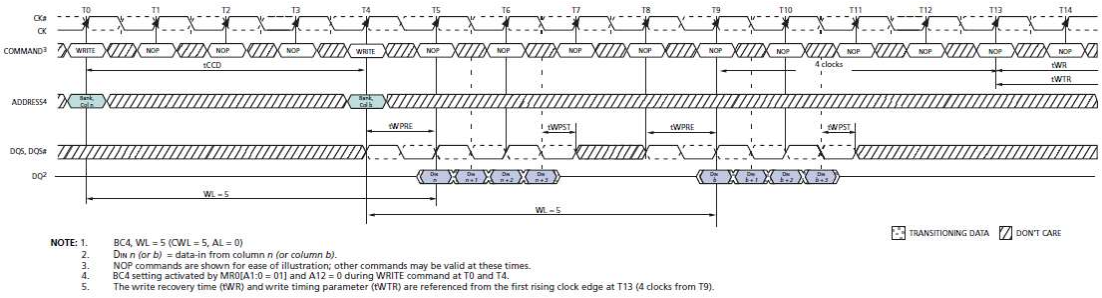


Figure 53 — WRITE (BC4) to WRITE (BC4) OTF

JESD79-3F, p. 73.

In DDR3 SDRAM memory systems, the command bus comprises the RAS#, CAS#, and WE# signals:

2.10 Pinout Description

Table 1 — Input/output functional description

Symbol	Type	Function
CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#.
CKE, (CKE0), (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK#, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS#, (CS0#), (CS1#), (CS2#), (CS3#)	Input	Chip Select: All commands are masked when CS# is registered HIGH. CS# provides for external Rank selection on systems with multiple Ranks. CS# is considered part of the command code.
ODT, (ODT0), (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, DQS# and DM/TDQS, NU/TDQS# (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x4/x8 configurations. For x16 configuration, ODT is applied to each DQ, DQSU, DQSU#, DQSL, DQSL#, DMU, and DML signal. The ODT pin will be ignored if MR1 and MR2 are programmed to disable RTT.
RAS#. CAS#. WE#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.

JESD79-3F, p. 13.

The TI 66AK2H06 SoC includes transmitter circuits that drive command signals onto output pins.

Table 4-2. Terminal Functions — Signals and Control by Function (continued)

SIGNAL NAME	BALL NO.	TYPE	IPD/IPU	DESCRIPTION
				...
DDR3ACAS	C13	OZ		DDR3A EMIF column address strobe
DDR3ARAS	A14	OZ		DDR3A EMIF row address strobe
DDR3AWE	F12	OZ		DDR3A EMIF write enable
DDR3ACKE0	G12	OZ		DDR3A EMIF clock enable0
DDR3ACKE1	A11	OZ		DDR3A EMIF clock enable1

66AK2Hxx Multicore DSP+ARM® KeyStone™ II System-on-Chip (SoC), p. 19.

77. Additionally, the Accused Products including DDR3 memory controllers send first control information indicating a first write operation to a first memory device, such that the first memory device samples first data in response to the first control information. A DDR3 SDRAM memory system comprises a bus width of 32 or 64 bits and comprise at least a first and second memory device attached to different ones of the 32 or 64 data bus lines.

66AK2Hxx Multicore DSP+ARM® KeyStone™ II System-on-Chip (SoC)

1 Device Overview

1.1 Features

- Memory Protection Unit (MPU) for Both MSM SRAM and DDR3_EMIF
- Two 72-Bit DDR3/DDR3L Interfaces With Speeds up to 1600 MHz

66AK2Hxx Multicore DSP+ARM® KeyStone™ II System-on-Chip (SoC), p. 1.

11.9 DDR3A and DDR3B Memory Controllers

The 72-bit DDR3 memory controller bus of the 66AK2Hxx is used to interface to JEDEC standard-compliant DDR3 SDRAM devices. The DDR3 external bus interfaces only to DDR3 SDRAM devices and does not share the bus with any other type of peripheral.

11.9.1 DDR3 Memory Controller Device-Specific Information

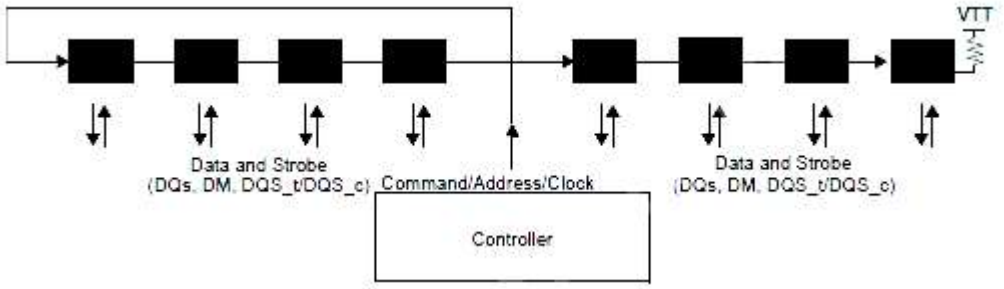
The 66AK2Hxx includes one 64-bit wide, 1.35-V / 1.5-V DDR3 SDRAM EMIF interface. The DDR3 interface can operate at 800 mega transfers per second (MTS), 1033 MTS, 1333 MTS, and 1600 MTS.

Due to the complicated nature of the interface, a limited number of topologies are supported to provide a 16-bit, 32-bit, or 64-bit interface.

The DDR3 electrical requirements are fully specified in the DDR JEDEC specification JESD79-3C. Standard DDR3 SDRAMs are available in 8-bit and 16-bit versions allowing for the following bank topologies to be supported by the interface:

- **72-bit:** Five 16-bit SDRAMs (including 8 bits of ECC)
- **72-bit:** Nine 8-bit SDRAMs (including 8 bits of ECC)
- **36-bit:** Three 16-bit SDRAMs (including 4 bits of ECC)
- **36-bit:** Five 8-bit SDRAMs (including 4 bits of ECC)
- **64-bit:** Four 16-bit SDRAMs
- **64-bit:** Eight 8-bit SDRAMs
- **32-bit:** Two 16-bit SDRAMs
- **32-bit:** Four 8-bit SDRAMs
- **16-bit:** One 16-bit SDRAM
- **16-bit:** Two 8-bit SDRAMs

66AK2Hxx Multicore DSP+ARM® KeyStone™ II System-on-Chip (SoC), p. 278.



JEDEC DDR3 SDRAM UDIMM Design Specification, Revision 1.06, pp. 4.20.19-35.

6.6 Net Structure Routing for Address/Command

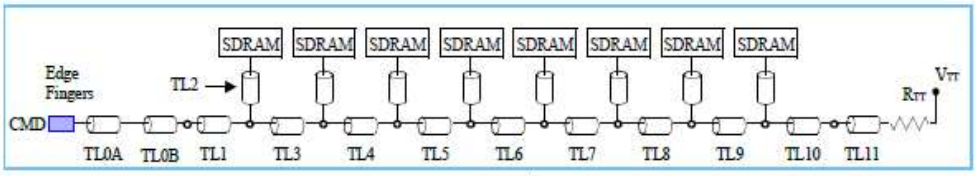


Figure 33 — Net Structure Routing for Address and Command (Raw Card Version A)

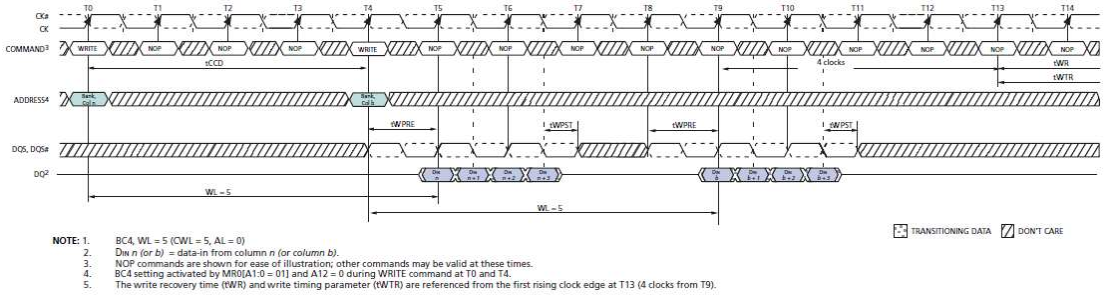
JEDEC DDR3 SDRAM UDIMM Design Specification, Revision 1.06, pp. 4.20.19-49.

If the first control information specifies a write operation, the first memory device will, at the appropriate time, sample first data arriving on a set of data signal lines from the memory controller.

Table 6 — Command Truth Table

Function	Abbreviation	CKE		CS#	RAS#	CAS#	WE#	BA0-BA2	A13-A15	A12-BC#	A10-AP	A0-A9, A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	7,8,9, 12
				L	H	H	H	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	

JESD79-3F, p. 33.

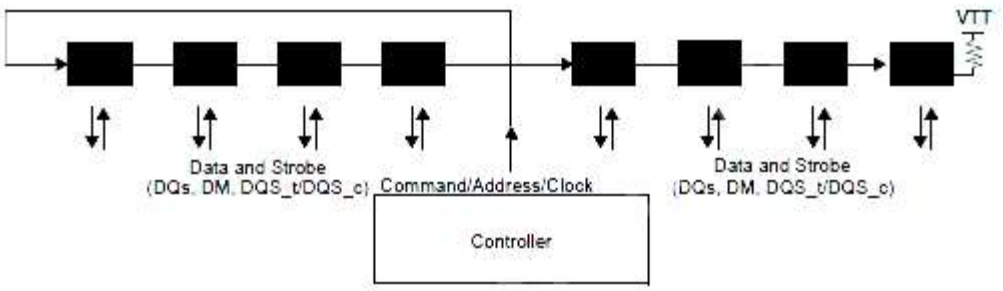


NOTE: 1. BC4, WL = 5 (CWL = 5, AL = 0)
2. Dxn (or bx) = data-in from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during WRITE command at T0 and T4.
5. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge at T13 (4 clocks from T9).

Figure 53 — WRITE (BC4) to WRITE (BC4) OTF

JESD79-3F, p. 73.

78. Additionally, the Accused Products including DDR3 memory controllers send second control information indicating a second write operation to a second memory device, such that the second memory device samples second data in response to the second control information. DDR3 SDRAM memory controllers connected to the TI 66AK2H06, send a second write to the same rank of memory devices causing a second memory device in the same rank to sample the second data in response to the second control information.



JEDEC DDR3 SDRAM UDIMM Design Specification, Revision 1.06, pp. 4.20.19-35.

6.6 Net Structure Routing for Address/Command

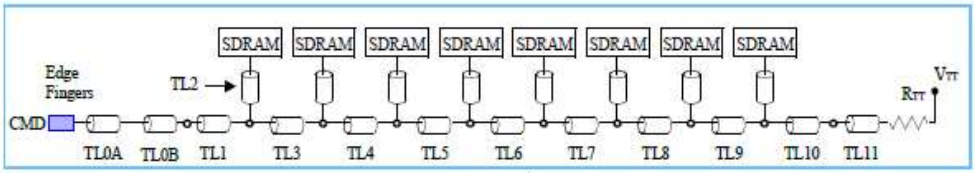


Figure 33 — Net Structure Routing for Address and Command (Raw Card Version A)

JEDEC DDR3 SDRAM UDIMM Design Specification, Revision 1.06, pp. 4.20.19-49.

79. Additionally, the Accused Products including DDR3 memory controllers include a second transmitter to output the first data using a first timing offset that is based on a first time that the first control information takes to propagate from the first transmitter to the first memory device. The DDR3 SDRAM controller is connected to the plurality of data signal conductors connecting the TI 66AK2H06 SoC memory controller to the first memory device for transmitting a first data to the first memory component.

6.6 Net Structure Routing for Address/Command

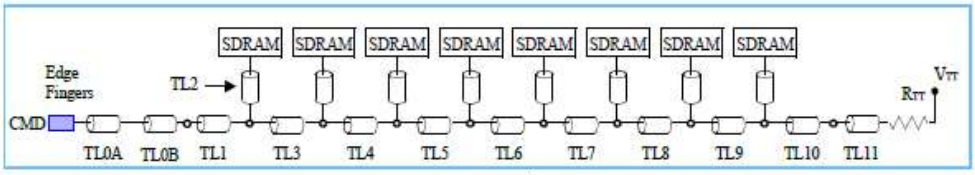
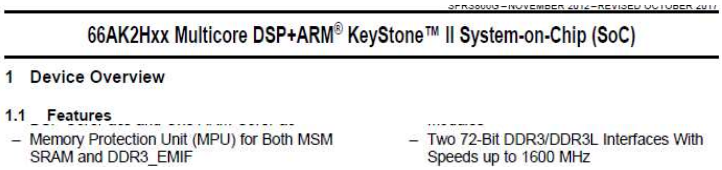


Figure 33 — Net Structure Routing for Address and Command (Raw Card Version A)

JEDEC DDR3 SDRAM UDIMM Design Specification, Revision 1.06, pp. 4.20.19-49.



66AK2Hxx Multicore DSP+ARM® KeyStone™ II System-on-Chip (SoC)

1 Device Overview

1.1 Features

– Memory Protection Unit (MPU) for Both MSM SRAM and DDR3_EMIF

– Two 72-Bit DDR3/DDR3L Interfaces With Speeds up to 1600 MHz

66AK2Hxx Multicore DSP+ARM® KeyStone™ II System-on-Chip (SoC), p. 1.

Table 4-2. Terminal Functions — Signals and Control by Function (continued)

SIGNAL NAME	BALL NO.	TYPE	IPD/IPU	DESCRIPTION
DDR3AD00	G1	IOZ		DDR3A EMIF data bus
DDR3AD01	H2	IOZ		
DDR3AD02	F1	IOZ		
DDR3AD03	G2	IOZ		
DDR3AD04	H1	IOZ		
DDR3AD05	E2	IOZ		
DDR3AD06	F2	IOZ		
DDR3AD07	D2	IOZ		
DDR3AD08	E4	IOZ		
DDR3AD09	F4	IOZ		
DDR3AD10	G3	IOZ		
DDR3AD11	A4	IOZ		
DDR3AD12	B4	IOZ		
DDR3AD13	H3	IOZ		
DDR3AD14	D3	IOZ		
DDR3AD15	D4	IOZ		

66AK2Hxx Multicore DSP+ARM® KeyStone™ II System-on-Chip (SoC), p. 18.

80. DDR3 SDRAM memory controllers connected to the TI 66AK2H06 employ write leveling to adjust the timing of write data being sent to the respective DDR3 SDRAM memory devices to compensate for the differing propagation delay of the control information and clock from the memory controller to the respective memory devices. Post write leveling during initialization of the memory subsystem, the second transmitter outputs the first data using a first timing offset that is based on a first time that the first control information takes to propagate from the first transmitter to the first memory device:

3.4.3.5 Write leveling

For better signal integrity, DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has the benefit of reducing the number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR3 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew. See 4.8 "Write Leveling" on page 42 for more details.

JESD79-3F. p.28.

4.8 Write Leveling

For better signal integrity, the DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR3 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew.

The memory controller can use the 'write leveling' feature and feedback from the DDR3 SDRAM to adjust the DQS - DQS# to CK - CK# relationship. The memory controller involved in the leveling must have adjustable delay setting on DQS - DQS# to align the rising edge of DQS - DQS# with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK - CK#, sampled with the rising edge of DQS - DQS#, through the DQ bus. The controller repeatedly delays DQS - DQS# until a transition from 0 to 1 is detected. The DQS - DQS# delay established though this exercise would ensure tDQSS specification. Besides tDQSS, tDSS and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS - DQS# signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in the chapter "AC Timing Parameters" in order to satisfy tDSS and tDSH specification. A conceptual timing of this scheme is shown in Figure 17.

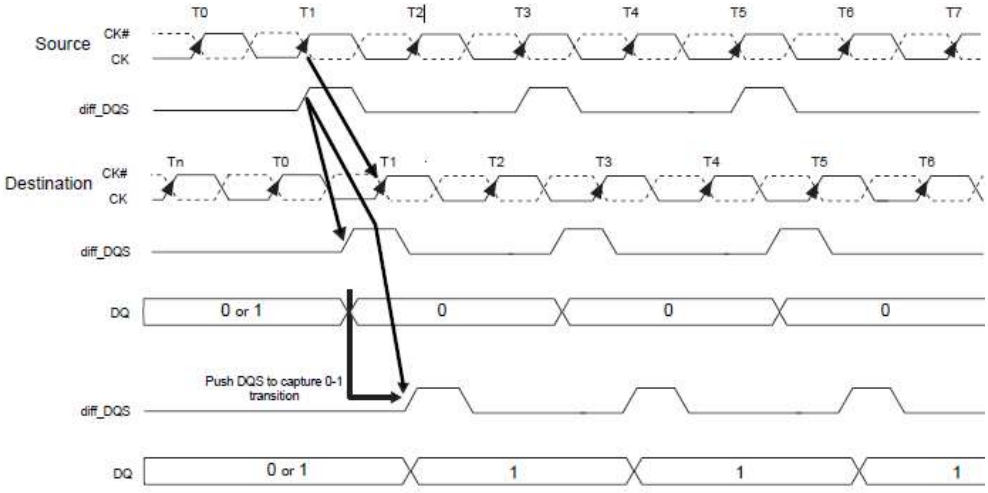


Figure 17 — Write Leveling Concept

JESD79-3F, p. 42.

2.12 Leveling

The DDR3 controller supports leveling to compensate for the command and DQS skew as a result of the fly-by topology. Leveling compensates the skew for both reads and writes. Unlike Keystone I devices, the controller in Keystone II devices does not require the user to program initial leveling values (INIT_RATIOs) to establish the starting point of the search window before triggering hardware leveling. The logic inside the DDR PHY is able to automatically search for and determine the optimal starting point when leveling and training sequence is triggered by writing to the PHY Initialization Register (PIR). Please refer to the DDR3 initialization application note for software programming sequence to initialize DDR3 on Keystone II devices.

Keystone II Architecture DDR3 Memory Controller, p. 30.

81. Additionally, the Accused Products including DDR3 SDRAM memory controllers include a third transmitter to output the second data using a second timing offset that is based on

a second time that the second control information takes to propagate from the first transmitter to the second memory device, the second time being longer than the first time. A DDR3 SDRAM memory system, such as one built using a DDR3 SDRAM UDIMM, comprises control information following the same path as the memory clock, so that the timing offset for sending the second data is based on both the propagation delay of the memory clock and the control information. In the DDR3 SDRAM memory system, the propagation delay of clock and control information travelling together are different to different memory devices as a result of the fly-by memory system configuration. Therefore, the second memory device is one of the pair such that the second time is longer than the first time.

6.6 Net Structure Routing for Address/Command

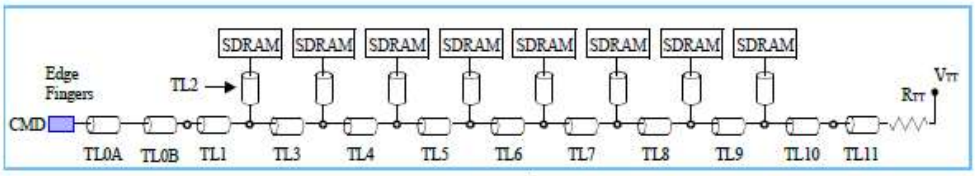


Figure 33 — Net Structure Routing for Address and Command (Raw Card Version A)

JEDEC DDR3 SDRAM UDIMM Design Specification, Revision 1.06, p. 4.20.19-49.

Table 4-2. Terminal Functions — Signals and Control by Function (continued)

SIGNAL NAME	BALL NO.	TYPE	IPD/IPU	DESCRIPTION
DDR3AD49	B20	IOZ		
DDR3AD50	D20	IOZ		
DDR3AD51	G20	IOZ		
DDR3AD52	C21	IOZ		
DDR3AD53	E20	IOZ		
DDR3AD54	F20	IOZ		
DDR3AD55	G21	IOZ		
DDR3AD56	C23	IOZ		DDR3A EMIF data bus
DDR3AD57	G22	IOZ		
DDR3AD58	D23	IOZ		
DDR3AD59	F22	IOZ		
DDR3AD60	E22	IOZ		
DDR3AD61	B22	IOZ		
DDR3AD62	F21	IOZ		
DDR3AD63	D22	IOZ		

66AK2Hxx Multicore DSP+ARM® KeyStone™ II System-on-Chip (SoC), p. 18.

Post write leveling during initialization of the memory subsystem, the third transmitter outputs the second data using a second timing offset that is based on a second time that the second control information takes to propagate from the first transmitter to the second memory device:

3.4.3.5 Write leveling

For better signal integrity, DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has the benefit of reducing the number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR3 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew. See 4.8 "Write Leveling" on page 42 for more details.

JESD79-3F, p. 28.

4.8 Write Leveling

For better signal integrity, the DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR3 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew.

The memory controller can use the 'write leveling' feature and feedback from the DDR3 SDRAM to adjust the DQS - DQS# to CK - CK# relationship. The memory controller involved in the leveling must have adjustable delay setting on DQS - DQS# to align the rising edge of DQS - DQS# with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK - CK#, sampled with the rising edge of DQS - DQS#, through the DQ bus. The controller repeatedly delays DQS - DQS# until a transition from 0 to 1 is detected. The DQS - DQS# delay established though this exercise would ensure tDQSS specification. Besides tDQSS, tDSS and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS - DQS# signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in the chapter "AC Timing Parameters" in order to satisfy tDSS and tDSH specification. A conceptual timing of this scheme is shown in Figure 17.

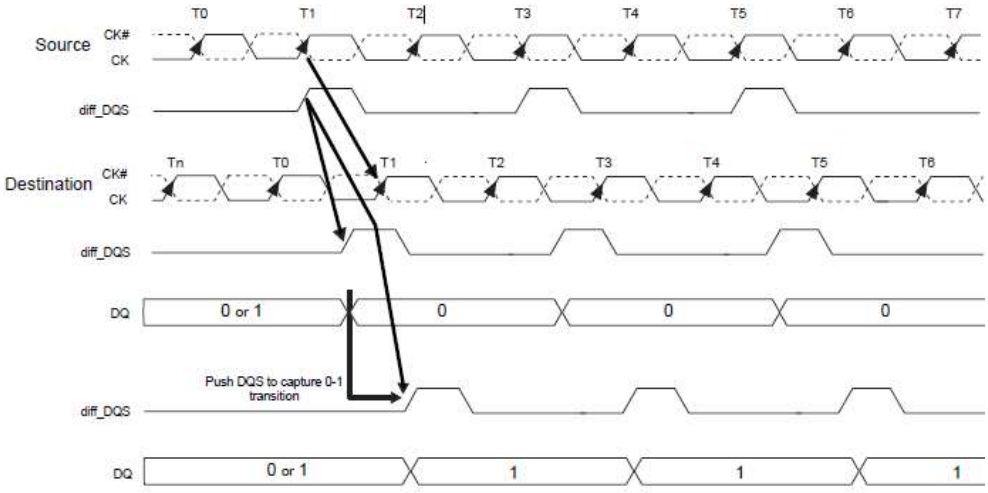


Figure 17 — Write Leveling Concept

JESD79-3F, p. 42.

2.12 Leveling

The DDR3 controller supports leveling to compensate for the command and DQS skew as a result of the fly-by topology. Leveling compensates the skew for both reads and writes. Unlike Keystone I devices, the controller in Keystone II devices does not require the user to program initial leveling values (INIT_RATIOs) to establish the starting point of the search window before triggering hardware leveling. The logic inside the DDR PHY is able to automatically search for and determine the optimal starting point when leveling and training sequence is triggered by writing to the PHY Initialization Register (PIR). Please refer to the DDR3 initialization application note for software programming sequence to initialize DDR3 on Keystone II devices.

Keystone II Architecture DDR3 Memory Controller, p. 30.

82. Defendant has and continues to indirectly infringe one or more claims of the ’311 Patent by knowingly and intentionally inducing others, including TI customers and end-users, to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products.

83. Upon information and belief, with knowledge and intent, or with willful blindness, Defendant encourages and facilitates infringement of one or more claims of the ’311 Patent by others, including at least Claim 26. For example, Rambus Inc. notified TI in April 2013 that the ’311 Patent was a member of the Ware 2001 Patent Family that Rambus was offering to license. Rambus notified TI at that time that TI was infringing patents in the Ware 2001 family, including U.S. Patent No. 7,177,998 based on its manufacture and sale of DDR3 memory controllers. In June 2015, Rambus notified TI that it was infringing the’616 Patent, U.S. Patent No. 8,537,601 (the “’601 Patent”), U.S. Patent No. 8,395,951 (the “’951 Patent”), and U.S. Patent No. 7,210,016 (the “’016 Patent”) by making, using, selling, offering to sell, and/or importing products practicing the DDR3 standard, including the TMS320C6654 DSP, TMS320DM64x DaVinci Digital Media Series DSP SoC, OM APX3530 Series Mobile Applications Processor, Keystone Multicore Family, Sitara AM389x ARM MPU Family, TMS320C6a81 6x C6-Integra DSP+ARM Processors, TMS320DM81xx DaVinci Digital Media Processors, and TMS320TC1 66xx/xx SoCs. The ’616 Patent, ’601 Patent, ’951 Patent, and ’016 Patent are all continuations of the ’311

Patent and are part of the same patent family. Based on these disclosures, TI was notified or willfully blind to the fact that the '311 Patent is infringed by TI products practicing the DDR3 standard.

84. Defendant, with knowledge that these products, or the use thereof, infringe the '311 Patent at least as of April 2013 and June 2015, knowingly and intentionally induced, and continues to knowingly and intentionally induce, direct infringement of the '311 Patent by providing these products to end-users for use in an infringing manner.

85. Defendant induced infringement by others, including end-users, with the intent to cause infringing acts by others or, in the alternative, with the belief that there was a high probability that others, including end-users, infringe the '311 Patent, but while remaining willfully blind to the infringement.

86. Rampart has suffered damages as a result of Defendant's direct and indirect infringement of the '311 Patent in an amount to be proved at trial.

87. Rampart has suffered, and will continue to suffer, irreparable harm as a result of Defendant's infringement of the '311 Patent, for which there is no adequate remedy at law, unless Defendant's infringement is enjoined by this Court.

88. TI has committed and continues to commit acts of infringement that TI actually knew or should have known constituted an unjustifiably high risk of infringement of at least one valid and enforceable claim of the '311 Patent. TI's direct and indirect infringement of the '311 Patent has been and continues to be willful, intentional, deliberate, and/or in conscious disregard of Rampart's rights under the patent. Rampart is entitled to an award of treble damages, reasonable attorney fees, and costs in bringing this action.

COUNT V
(Infringement of the '616 Patent)

89. Paragraphs 1 through 23 are incorporated by reference as if fully set forth herein.

90. Rampart has not licensed or otherwise authorized Defendant to make, use, offer for sale, sell, or import any products that embody the inventions of the '616 Patent.

91. Defendant has and continues to directly infringe the '616 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products including, but not limited to, products supporting DDR3 and DDR3L external memories and a x32 or x64 bus such as the TI DRA780, DRA781, DRA782, DRA783, DRA784, DRA785, DRA786, DRA787, DRA788, TMS320C6655, TMS320C6657, 66AK2G12, 66AK2H06, 66AK2H12, 66AK2H14, DRA744P, DRA745P, DRA746P, DRA750P, DRA751P, DRA752P, DRA754P, DRA755P, DRA756P, DRA710, DRA712, DRA714, DRA716, DRA724, DRA722, DRA725, DRA767P, DRA77xP, DRA790, DRA791, DRA793, DRA797, TDA2P-ABZ, TDA2P-ACD, TDA2EG-17, TDA2EG, TDA2EGABC, TDA2HF, TDA2SX, TDA2SG, TDA2SA, TDA2HG, TDA2HV, TDA2LF, AM4372, AM4376, AM4377, AM4378, AM4379, AM5748, AM5749, AM5706, AM5708, AM5716, AM5718, AM5726, AM5728, and AM5729.

92. For example, Defendant has and continues to directly infringe at least Claim 36 of the '616 Patent by making, using, offering to sell, selling, and/or importing into the United States products that include a memory controller that complies with the DDR3 standard. For example, the TI 66AK2H06 includes DDR3 and DDR3L memory controllers capable of controlling a memory system consisting of DDR3 SDRAMs, each of which is compliant with the JEDEC standard JESD79-3.

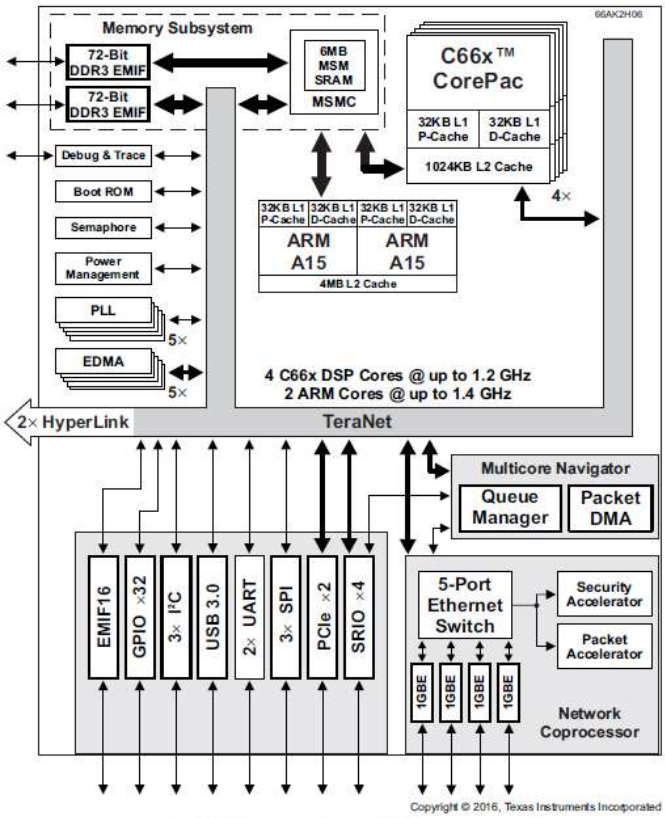


Figure 1-3. Functional Block Diagram for 66AK2H06

66AK2Hxx Multicore DSP+ARM® KeyStone™ II System-on-Chip (SoC), p. 5.

66AK2Hxx Multicore DSP+ARM® KeyStone™ II System-on-Chip (SoC)

1 Device Overview

1.1 Features

– Memory Protection Unit (MPU) for Both MSM SRAM and DDR3_EMIF

– Two 72-Bit DDR3/DDR3L Interfaces With Speeds up to 1600 MHz

66AK2Hxx Multicore DSP+ARM® KeyStone™ II System-on-Chip (SoC), p. 1.

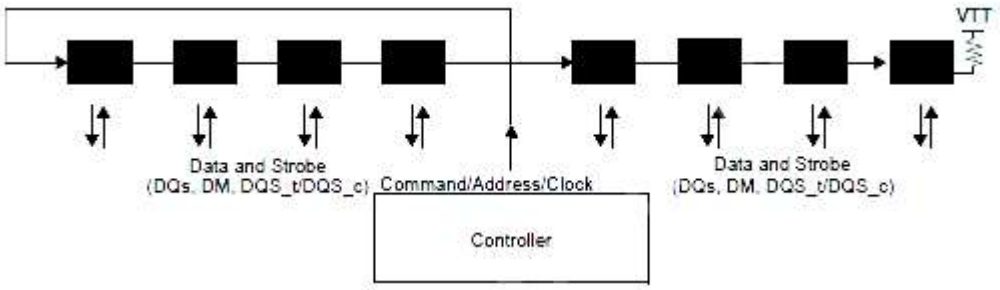
11.9 DDR3A and DDR3B Memory Controllers

The 72-bit DDR3 memory controller bus of the 66AK2Hxx is used to interface to JEDEC standard-compliant DDR3 SDRAM devices. The DDR3 external bus interfaces only to DDR3 SDRAM devices and does not share the bus with any other type of peripheral.

66AK2Hxx Multicore DSP+ARM® KeyStone™ II System-on-Chip (SoC), p. 278.

93. The Accused Products including DDR3 memory controllers, including the TI 66AK2H06, include a clock buffer to provide a clock signal to an external clock line routed in succession to a first and second memory component. DDR3 SDRAM memory controllers, connected to the 66AK2H06, include a buffer that drives the memory clock signal onto the external

clock line toward the plurality of DDR3 SDRAMs that necessarily include a first and second memory components. DDR3 memory systems generally incorporate a fly-by clock distribution topology, whereby the clock is routed in succession to the first and second memory components.



JEDEC DDR3 SDRAM UDIMM Design Specification, Revision 1.06, pp. 4.20.19-35.

6.4 Clock Net Structures

SDRAM clock signals must be carefully routed to meet the following requirements:
- Signal quality (slew rate and crossing point)
- Rise/fall time
- SDRAM component edge skew

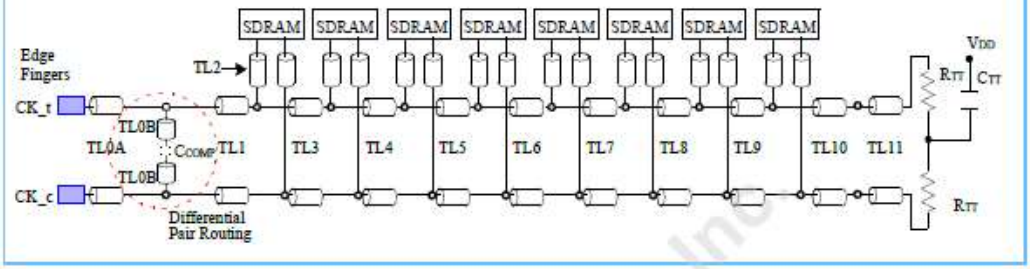


Figure 21 — Clock Net Structures (Raw Card Version A) CK0_t, CK0_c

JEDEC DDR3 SDRAM UDIMM Design Specification, Revision 1.06, pp. 4.20.19-39.

The same would be the case if the DDR3 SDRAMs are mounted directly on the same printed circuit board as the TI 66AK2H06 SoC if a comparable clock distribution strategy was used within the memory subsystem.

	11	12	13	14	15	16	17	18	19	20
AW	HYP0RXP0	VSS	RSV167	RSV168	VSS	RSV161	RSV162	VSS	XFIRXP1	XFIRXN1
AV	VSS	RSV171	RSV172	VSS	RSV165	RSV166	VSS	XFIRXP0	XFIRXN0	VSS
AU	HYP0RXP1	VSS	RSV169	RSV170	VSS	RSV163	RSV164	VSS	XFICLKP	XFICLKN
AT	VSS	RSV183	RSV184	VSS	RSV177	RSV178	VSS	XFITXP0	XFITXN0	VSS
AR	HYP0TXP1	VSS	RSV181	RSV182	VSS	RSV175	RSV176	VSS	XFITXP1	XFITXN1
AP	HYP0TXN0	HYP0TXP0	VSS	RSV179	RSV180	VSS	RSV173	RSV174	VSS	VSS
AN	VSS	VSS	VSS	VSS	VSS	XFIREFRES0	VSS	VSS	RSV026	VSS
AM	RSV099	VSS	VSS	RSV025	RSV185	RSV024	VSS	VSS	XFIREFRES1	VSS
AL	VSS	VDDAHV	VSS	VDDAHV	VSS	VDDAHV	VSS	VDDAHV	VSS	VDDAHV
AK	VDDAHV	VSS	VDDAHV	VSS	VDDAHV	VSS	VDDAHV	VSS	VDDAHV	VSS
AJ	VSS	VDDALV	VSS	VDDALV	VSS	VDDALV	VSS	VDDALV	VSS	VDDALV
AH	VDDALV	VSS	VDDALV	VSS	VDDALV	VSS	VDDALV	VSS	VDDALV	VSS
AG	VSS	VDDALV	VSS	VDDALV	VSS	VDDALV	VSS	VDDALV	VSS	VDDALV
AF	AVDDA1	VSS	VDDALV	VSS	VDDALV	VSS	VDDALV	VSS	VDDALV	VSS
AE	VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS	CVDD
AD	VNWA2	VSS	CVDD	VSS	CVDD	VSS	CVDD1	VSS	CVDD1	VSS
AC	VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS	CVDD1	VSS	CVDD
AB	CVDD	VSS	VDDUSB	VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS
AA	VSS	VP	VSS	DVDD33	VSS	CVDD	VSS	CVDD	VSS	CVDD
Y	VPTX	VSS	VPH	VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS
W	VSS	CVDD	VSS	CVDD	VSS	CVDD1	VSS	CVDD	VSS	CVDD
V	VNWA4	VSS	CVDD1	VSS	CVDD	VSS	CVDD1	VSS	CVDD	VSS
U	VSS	CVDD	VSS	CVDD1	VSS	CVDD1	VSS	CVDD	VSS	CVDD1
T	CVDD	VSS	CVDD1	VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS
R	VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS	CVDD
P	AVDDA6	VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS
N	VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS	CVDD	VSS	AVDDA2
M	DVDD15	VSS	AVDDA7	VSS	AVDDA8	VSS	DVDD15	AVDDA9	DVDD15	AVDDA10
L	VSS	DVDD15	VSS	DVDD15	VSS	DVDD15	VSS	DVDD15	VSS	DVDD15
K	DVDD15	VSS	DVDD15	VSS	DVDD15	VSS	DVDD15	VSS	DVDD15	VSS
J	VSS	DVDD15	VSS	DVDD15	VSS	DVDD15	VSS	DVDD15	VSS	DVDD15
H	DVDD15	VSS	DVDD15	VSS	DVDD15	DDR3ARQ0	DVDD15	VSS	DVDD15	VSS
G	DDR3ABA2	DDR3ACKE0	DDR3AODT1	DDR3AVREFSSTL	DDR3ACB07	DDR3AD33	DDR3AD35	DDR3AD42	DDR3AD44	DDR3AD51
F	DDR3ACE1	DDR3AWE	RSV029	DDR3ACB05	DDR3ACB03	DDR3AD34	DDR3AD38	DDR3AD47	DDR3AD43	DDR3AD54
E	VSS	DDR3AODT0	VSS	DDR3ADQM6	VSS	DDR3AD32	VSS	DDR3AD39	VSS	DDR3AD53
D	DDR3ACE0	RSV027	RSV028	DDR3ACB06	DDR3ACB04	DDR3AD36	DDR3AD37	DDR3AD46	DDR3AD41	DDR3AD50
C	DDR3ABA1	VSS	DDR3ACAS	VSS	DDR3ACB01	VSS	DDR3ADQM4	VSS	DDR3AD40	VSS
B	DDR3ABA0	DDR3ACLKOUTN0	DDR3ACLKOUTN1	DDR3ARESET	DDR3ADQS8P	DDR3ACB02	DDR3ADQS4N	DDR3AD45	DDR3ADQS5P	DDR3AD49
A	DDR3ACKE1	DDR3ACLKOUTP0	DDR3ACLKOUTP1	DDR3ARAS	DDR3ADQS8N	DDR3ACB00	DDR3ADQS4P	DDR3ADQM5	DDR3ADQS5N	DDR3AD48
	11	12	13	14	15	16	17	18	19	20

Figure 4-4. 66AK2Hxx Pin Map Left Center Panel (B) — Bottom View

66AK2Hxx Multicore DSP+ARM® KeyStone™ II System-on-Chip (SoC), p. 12.

Table 4-2. Terminal Functions — Signals and Control by Function (continued)

SIGNAL NAME	BALL NO.	TYPE	IPD/IPU	DESCRIPTION
DDR3A_REMAP_EN†	A36	I	Down	Control ARM remapping of DDR3A address space in the lower 4GB (32b space) Mode select. Secondary function. Pin shared with GPIO16.
LENDIAN†	F29	I	Up	Little-endian configuration pin. Pin shared with GPIO00.
MAINPLLODSEL†	E32	I	Down	Main PLL Output divider select. Pin shared with GPIO14.
Clock / Reset				
ALTCORECLKN	AL2	I		Alternate clock input to Main PLL
ALTCORECLKP	AM2	I		
ARMCLKN	B37	I		Reference clock to drive ARM CorePac PLL
ARMCLKP	C37	I		
CORECLKSEL	AL4	I	Down	Core clock select to select between SYSCLK(N)p and ALTCORECCLK to the main PLL
CORESEL0	F24	I	Down	Select for the target core for LRESET and NMI
CORESEL1	E24	I	Down	
CORESEL2	D24	I	Down	
CORESEL3	G24	I	Down	
DDR3ACLKN	A25	I		DDR3A reference clock input to DDR PLL
DDR3ACLKP	B25	I		
DDR3BCLKN	AR39	I		DDR3B reference clock input to DDR PLL
DDR3BCLKP	AR38	I		

66AK2Hxx Multicore DSP+ARM® KeyStone™ II System-on-Chip (SoC), p. 16.

94. Additionally, the Accused Products including DDR3 memory controllers include a memory controller component wherein a first propagation time required for the clock signal to propagate on the clock line from the memory controller component to the first memory component

is shorter than a second propagation time required for the clock signal to propagate on the clock line from the memory controller component to the second memory component. In DDR3 SDRAM UDIMMs, the clock signal traverses the DIMM from one SDRAM near one edge to the last SDRAM near the opposite edge. Those edges are specified to be 133 mm apart. Based on this or any comparable clock distribution topology, the first propagation time required for the clock to propagate from the memory controller to the first memory component will be shorter than the second clock propagation time from the memory controller to the second memory component.

6.4 Clock Net Structures

SDRAM clock signals must be carefully routed to meet the following requirements:
- Signal quality (slew rate and crossing point)
- Rise/fall time
- SDRAM component edge skew

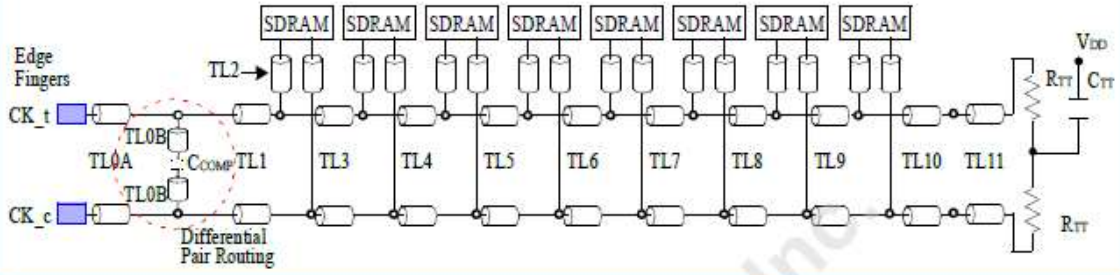


Figure 21 — Clock Net Structures (Raw Card Version A) CK0_t, CK0_c

JEDEC DDR3 SDRAM UDIMM Design Specification, Revision 1.06, pp. 4.20.19-39.

Table 16 — Trace Lengths for Clock Net Structures (Raw Card Version A) CK0_t, CK0_c

RC	Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	First DRAM Compensated[2]	Last DRAM Compensated[3]	TL10	TL11	CCOMP	RTT	CTT
		MS	MS	SL	MS	SL	SL	SL	SL	SL	SL	SL			SL	MS			
A0/A1	MIN	4.2	1.1	94.0	1.0	15.3	15.3	15.3	24.8	15.3	15.3	15.3	98.9	215.5	11.7	0.7	2.2pF	36Ω	0.1µF
	MAX	4.3	1.2	94.1	1.1	15.4	15.4	15.4	24.9	15.4	15.4	15.4	99.0	215.6	11.8	0.8	2.2pF	36Ω	0.1µF

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
Note 2 Equivalent stripline length to first DRAM [TL0A/1.1 + TL1 + TL2/1.1].
Note 3 Equivalent stripline length to last DRAM [TL0A/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5 + TL6 + TL7 + TL8 + TL9].
Note 4 The pair CK1_t and CK1_c is routed to a 75Ω, termination resistor but is not connected to any DRAM.

JEDEC DDR3 SDRAM UDIMM Design Specification, Revision 1.06, pp. 4.20.19-39.

Table 1 — Product Family Attributes

DIMM Organization	x64, x72 ECC	Notes
DIMM Dimensions (NOM)	133.35 mm x 30.00 mm x 4 mm	Refer to MO 269
	133.35 mm x 18.75 mm x 4 mm	Refer to MO 269
Pin Count	240	
DDR3 SDRAMs Supported	512Mb, 1Gb, 2Gb, 4Gb, 8Gb	78/106-ball FBGA package for x8 and 96/112-ball FBGA for x16 devices.

JEDEC DDR3 SDRAM UDIMM Design Specification, Revision 1.06, pp. 4.20.19-9.

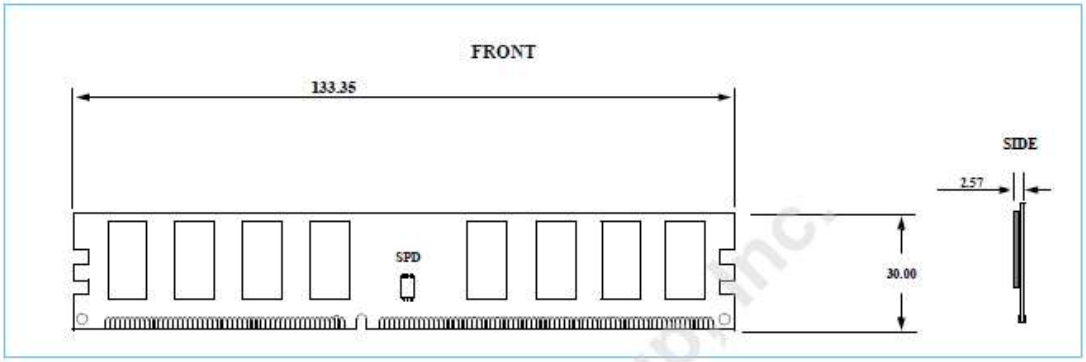


Figure 11 — Example Component Placement (Raw Card Version A)

JEDEC DDR3 SDRAM UDIMM Design Specification, Revision 1.06, pp. 4.20.19-30.

95. Additionally, the Accused Products including DDR3 memory controllers include a first transmitter to transmit first data along a first dedicated data bus to the first memory component. The Accused Products, including the TI 66AK2H06 SoC, include DDR3 SDRAM memory controllers connected to the plurality of data signal conductors that connect to the first memory component for transmitting a first data to the first memory component.

66AK2Hxx Multicore DSP+ARM® KeyStone™ II System-on-Chip (SoC)

1 Device Overview

1.1 Features

– Memory Protection Unit (MPU) for Both MSM SRAM and DDR3_EMIF
– Two 72-Bit DDR3/DDR3L Interfaces With Speeds up to 1600 MHz

66AK2Hxx Multicore DSP+ARM® KeyStone™ II System-on-Chip (SoC), p. 1.

Table 4-2. Terminal Functions — Signals and Control by Function (continued)

SIGNAL NAME	BALL NO.	TYPE	IPD/IPU	DESCRIPTION
DDR3AD00	G1	IOZ		DDR3A EMIF data bus
DDR3AD01	H2	IOZ		
DDR3AD02	F1	IOZ		
DDR3AD03	G2	IOZ		
DDR3AD04	H1	IOZ		
DDR3AD05	E2	IOZ		
DDR3AD06	F2	IOZ		
DDR3AD07	D2	IOZ		
DDR3AD08	E4	IOZ		
DDR3AD09	F4	IOZ		
DDR3AD10	G3	IOZ		
DDR3AD11	A4	IOZ		
DDR3AD12	B4	IOZ		
DDR3AD13	H3	IOZ		
DDR3AD14	D3	IOZ		
DDR3AD15	D4	IOZ		

66AK2Hxx Multicore DSP+ARM® KeyStone™ II System-on-Chip (SoC), p. 18.

Pin Name	Description
A0–A15	SDRAM address bus
BA0–BA2	SDRAM bank select
RAS_n	SDRAM row address strobe
CAS_n	SDRAM column address strobe
WE_n	SDRAM write enable
S0_n–S1_n	DIMM Rank Select Lines
CKE0–CKE1	SDRAM clock enable lines
ODT0–ODT1	On-die termination control lines
DQ0–DQ63	DIMM memory data bus
CB0–CB7	DIMM ECC check bits
DQS0_t–DQS8_t	SDRAM data strobes (positive line of differential pair)
DQS0_c–DQS8_c	SDRAM data strobes (negative line of differential pair)
DM0–DM8	SDRAM data masks/high data strobes (x8-based x72 DIMMs)
CK0_t–CK1_t	SDRAM clocks (positive line of differential pair)
CK0_c–CK1_c	SDRAM clocks (negative line of differential pair)

JEDEC DDR3 SDRAM UDIMM Design Specification, Revision 1.06, pp. 4.20.19-11.

2.10 Pinout Description

Table 1 — Input/output functional description

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus.

JESD79-3F, p. 13.

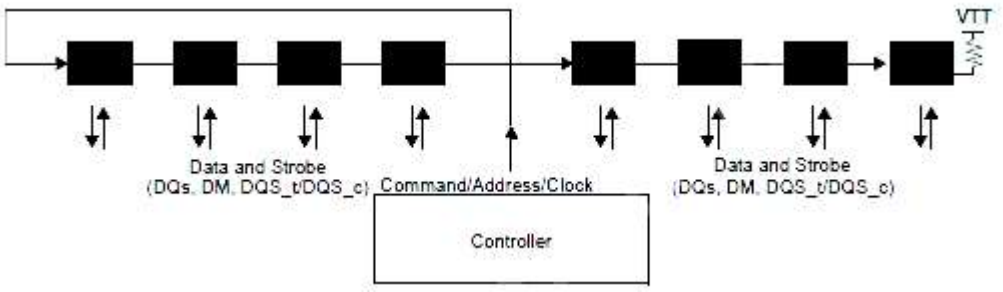
96. Additionally, the Accused Products including DDR3 memory controllers include a second transmitter to transmit second data along a second dedicated data bus to the second memory component. The Accused Products, including the TI 66AK2H06 SoC, include DDR3 SDRAM memory controllers, connected to the plurality of data signal conductors that connect to the second memory component for transmitting a second data to the second memory component.

Table 4-2. Terminal Functions — Signals and Control by Function (continued)

SIGNAL NAME	BALL NO.	TYPE	IPD/IPU	DESCRIPTION
DDR3AD49	B20	IOZ		
DDR3AD50	D20	IOZ		
DDR3AD51	G20	IOZ		
DDR3AD52	C21	IOZ		
DDR3AD53	E20	IOZ		
DDR3AD54	F20	IOZ		
DDR3AD55	G21	IOZ		
DDR3AD56	C23	IOZ		DDR3A EMIF data bus
DDR3AD57	G22	IOZ		
DDR3AD58	D23	IOZ		
DDR3AD59	F22	IOZ		
DDR3AD60	E22	IOZ		
DDR3AD61	B22	IOZ		
DDR3AD62	F21	IOZ		
DDR3AD63	D22	IOZ		

66AK2Hxx Multicore DSP+ARM® KeyStone™ II System-on-Chip (SoC), p. 18.

The JEDEC DDR3 SDRAM UDIMM Design Specification shows parallel data buses from the controller to each of the memory components in a rank of the memory subsystem.



JEDEC DDR3 SDRAM UDIMM Design Specification, Revision 1.06, pp. 4.20.19-35.

97. Additionally, the Accused Products including DDR3 memory controllers comprise a memory controller component wherein the time at which the second data is transmitted is offset from a time at which the first data is transmitted based, at least in part, on the difference between the first and second propagation times. In the DDR3 SDRAM memory systems, including the TI

66AK2H06, write leveling is applied to adjust the time that write data is transmitted towards each respective memory component so that the data arrives approximately coincidently with the clock signal arriving at each of the respective SDRAMs. Thus, after write leveling has been performed as part of memory system initialization, the time the second data is sent toward the second memory component is offset from the time the first data by an amount approximately equal to the difference in the clock propagation times.

3.4.3.5 Write leveling

For better signal integrity, DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has the benefit of reducing the number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR3 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew. See 4.8 "Write Leveling" on page 42 for more details.

JESD79-3F, p. 28.

4.8 Write Leveling

For better signal integrity, the DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR3 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew.

The memory controller can use the 'write leveling' feature and feedback from the DDR3 SDRAM to adjust the DQS - DQS# to CK - CK# relationship. The memory controller involved in the leveling must have adjustable delay setting on DQS - DQS# to align the rising edge of DQS - DQS# with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK - CK#, sampled with the rising edge of DQS - DQS#, through the DQ bus. The controller repeatedly delays DQS - DQS# until a transition from 0 to 1 is detected. The DQS - DQS# delay established though this exercise would ensure tDQSS specification. Besides tDQSS, tDSS and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS - DQS# signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in the chapter "AC Timing Parameters" in order to satisfy tDSS and tDSH specification. A conceptual timing of this scheme is shown in Figure 17.

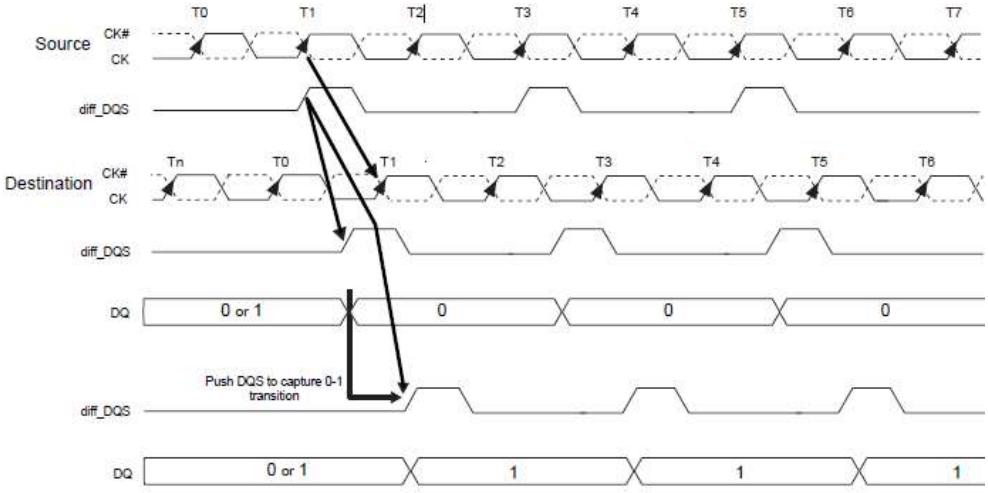
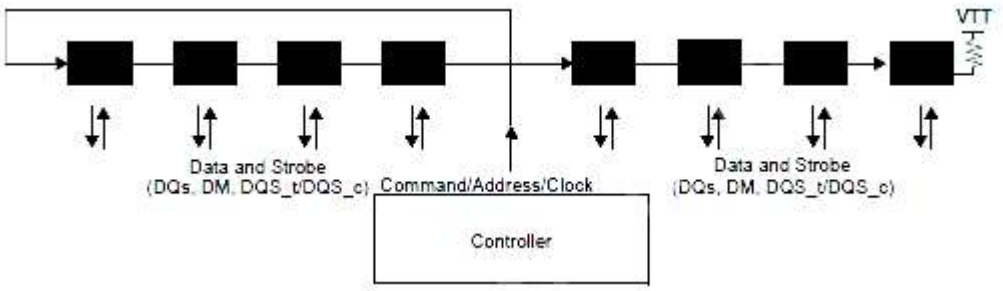


Figure 17 — Write Leveling Concept

JESD79-3F, p. 42.

98. Additionally, the Accused Products including DDR3 memory controllers include a third transmitter to transmit a first strobe signal along a first dedicated strobe signal line to the first memory component, wherein the first memory component receives the first strobe signal to sample the first data. In DDR3 SDRAM memory systems, each 8 data lines has associated with them a single differential data strobe signal. The DDR3 external memory controller part of the TI 66AK2H06 SoC includes a transmitter for sending a first dedicated data strobe signal on a first dedicated strobe signal line that is associated with the data signals/lines going to the first memory

component. The first DDR3 SDRAM memory component uses the received strobe signal to sample the first data.



JEDEC DDR3 SDRAM UDIMM Design Specification, Revision 1.06, pp. 4.20.19-35.

2.10 Pinout Description

Table 1 — Input/output functional description

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus.
DQU, DQL, DQS, DQS#, DQSU, DQSU#, DQSL, DQSL#	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobes DQS, DQSL, and DQSU are paired with differential signals DQS#, DQSL#, and DQSU#, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.

JESD79-3F, p. 13.

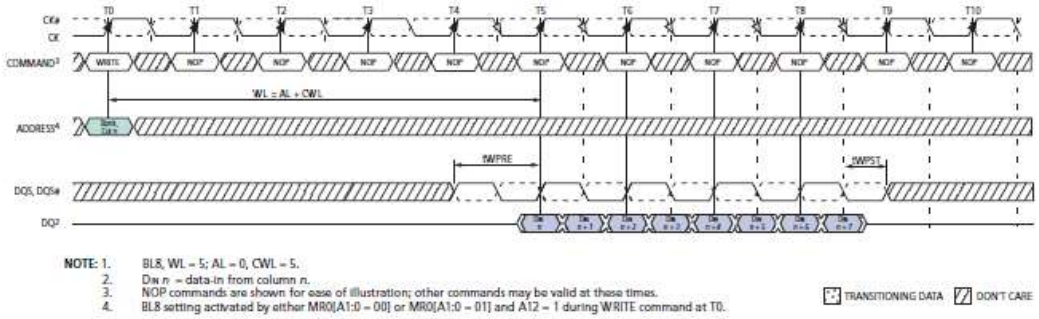


Figure 47 — WRITE Burst Operation WL = 5 (AL = 0, CWL = 5, BL8)

JESD79-3F, p. 71.

Table 4-2. Terminal Functions — Signals and Control by Function (continued)

SIGNAL NAME	BALL NO.	TYPE	IPD/IPU	DESCRIPTION
DDR3A				
DDR3ADQM0	C2	OZ		DDR3A EMIF data masks
DDR3ADQM1	F3	OZ		
DDR3ADQM2	A6	OZ		
DDR3ADQM3	E6	OZ		
DDR3ADQM4	C17	OZ		
DDR3ADQM5	A18	OZ		
DDR3ADQM6	D21	OZ		
DDR3ADQM7	A22	OZ		
DDR3ADQM8	E14	OZ		
DDR3ADQS0P	E1	IOZ		DDR3A EMIF data strobe
DDR3ADQS0N	D1	IOZ		
DDR3ADQS1P	B3	IOZ		
DDR3ADQS1N	C3	IOZ		
DDR3ADQS2P	A5	IOZ		
DDR3ADQS2N	B5	IOZ		
DDR3ADQS3P	B7	IOZ		
DDR3ADQS3N	A7	IOZ		
DDR3ADQS4P	A17	IOZ		
DDR3ADQS4N	B17	IOZ		
DDR3ADQS5P	B19	IOZ		
DDR3ADQS5N	A19	IOZ		
DDR3ADQS6P	A21	IOZ		
DDR3ADQS6N	B21	IOZ		
DDR3ADQS7P	A23	IOZ		
DDR3ADQS7N	B23	IOZ		
DDR3ADQS8P	B15	IOZ		
DDR3ADQS8N	A15	IOZ		

66AK2Hxx Multicore DSP+ARM® KeyStone™ II System-on-Chip (SoC), p. 17.

99. Additionally, the Accused Products including DDR3 memory controllers include a fourth transmitter to transmit a second strobe signal along a second dedicated strobe signal line to the second memory component, wherein the second memory component receives the second strobe signal to sample the second data. DDR3 SDRAM memory systems, including the TI 66AK2H06, include data lines, wherein each 8 data lines has associated with them a single differential data strobe signal. The DDR3 external memory controller part of the TI 66AK2H06 SoC includes a transmitter for sending a second data strobe signal on a second dedicated strobe signal line that is associated with the data signals/lines going to the second memory component. The second DDR3 SDRAM memory component uses the received strobe signal to sample the second data.

2.10 Pinout Description

Table 1 — Input/output functional description

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus.
DQU, DQL, DQS, DQS#, DQSU, DQSU#, DQSL, DQSL#	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobes DQS, DQSL, and DQSU are paired with differential signals DQS#, DQSL#, and DQSU#, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.

JESD79-3F, p. 13.

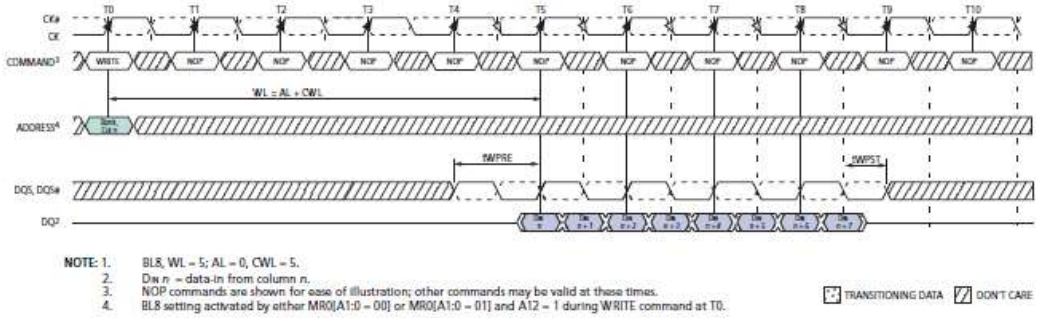


Figure 47 — WRITE Burst Operation WL = 5 (AL = 0, CWL = 5, BL8)

JESD79-3F, p. 71.

100. Additionally, the Accused Products including DDR3 memory controllers transmit the second strobe signal at a time that is offset from a time at which the first strobe signal is transmitted based, at least in part, on the difference between the first and second propagation times. In DDR3 SDRAM memory systems, including the TI 66AK2H06 SoC, the time the second strobe signal is sent is offset from the time the first strobe is sent, comparably to the offset between when the first data is sent and when the second data is sent.

3.4.3.5 Write leveling

For better signal integrity, DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has the benefit of reducing the number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR3 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew. See 4.8 "Write Leveling" on page 42 for more details.

JESD79-3F, p. 28.

4.8 Write Leveling

For better signal integrity, the DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR3 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew.

The memory controller can use the 'write leveling' feature and feedback from the DDR3 SDRAM to adjust the DQS - DQS# to CK - CK# relationship. The memory controller involved in the leveling must have adjustable delay setting on DQS - DQS# to align the rising edge of DQS - DQS# with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK - CK#, sampled with the rising edge of DQS - DQS#, through the DQ bus. The controller repeatedly delays DQS - DQS# until a transition from 0 to 1 is detected. The DQS - DQS# delay established though this exercise would ensure tDQSS specification. Besides tDQSS, tDSS and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS - DQS# signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in the chapter "AC Timing Parameters" in order to satisfy tDSS and tDSH specification. A conceptual timing of this scheme is shown in Figure 17.

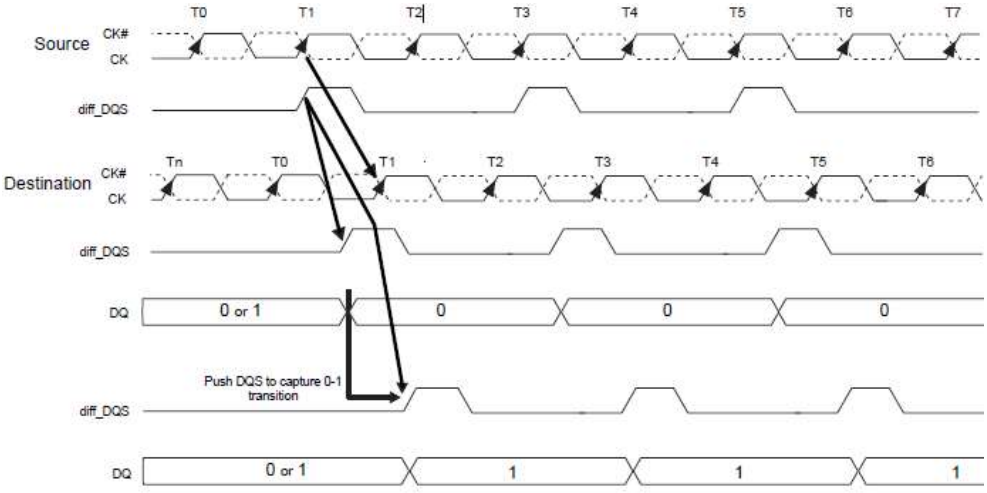


Figure 17 — Write Leveling Concept

JESD79-3F, p. 42.

4.8.2 Procedure Description

The Memory controller initiates Leveling mode of all DRAMs by setting bit 7 of MR1 to 1. When entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only NOP or DESELECT commands are allowed, as well as an MRS command to change Qoff bit (MR1[A12]) and an MRS command to exit write leveling (MR1[A7]). Upon exiting write leveling mode, the MRS command performing the exit (MR1[A7]=0) may also change MR1 bits of A12-A11, A9, A6-A5, and A2-A1. Since the controller levels one rank at a time, the output of other ranks must be disabled by setting MR1 bit A12 to 1. The Controller may assert ODT after tMOD, at which time the DRAM is ready to accept the ODT signal.

The Controller may drive DQS low and DQS# high after a delay of tWLDQSEN, at which time the DRAM has applied on-die termination on these signals. After tDQSL and tWLMRD, the controller provides a single DQS, DQS# edge which is used by the DRAM to sample CK - CK# driven from controller. tWLMRD(max) timing is controller dependent.

DRAM samples CK - CK# status with rising edge of DQS - DQS# and provides feedback on all the DQ bits asynchronously after tWLO timing. Either one or all data bits ("prime DQ bit(s)") provide the leveling feedback. The DRAM's remaining DQ bits are driven Low statically after the first sampling procedure. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits. The tWLOE period is defined from the transition of the earliest DQ bit to the corresponding transition of the latest DQ bit. There are no read strobes (DQS/DQS#) needed for these DQs. Controller samples incoming DQ and decides to increment or decrement DQS - DQS# delay setting and launches the next DQS/DQS# pulse after some time, which is controller dependent. Once a 0 to 1 transition is detected, the controller locks DQS - DQS# delay setting and write leveling is achieved for the device. Figure 18 describes the timing diagram and parameters for the overall Write Leveling procedure.

JESD79-3F, p. 43.

101. Defendant has and continues to indirectly infringe one or more claims of the ’616 Patent by knowingly and intentionally inducing others, including TI customers and end-users, to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling and/or importing into the United States the Accused Products.

102. Upon information and belief, with knowledge and intent, or with willful blindness, Defendant encourages and facilitates infringement of one or more claims of the ’616 Patent by others, including at least claim 36. For example, Rambus Inc. notified TI in May 2012 that TI was infringing the’616 Patent by making, using, selling, offering to sell and/or importing products that include controllers for DDR3 memories.

103. Defendant, with knowledge that these products, or the use thereof, infringes the ’616 Patent at least as of May 2012, knowingly and intentionally induced, and continues to

knowingly and intentionally induce, direct infringement of the ’616 Patent by providing these products to end-users for use in an infringing manner.

104. Defendant induced infringement by others, including end-users, with the intent to cause infringing acts by others or, in the alternative, with the belief that there was a high probability that others, including end-users, infringe the ’616 Patent, but while remaining willfully blind to the infringement.

105. Rampart has suffered damages as a result of Defendant’s direct and indirect infringement of the ’616 Patent in an amount to be proved at trial.

106. Rampart has suffered, and will continue to suffer, irreparable harm as a result of Defendant’s infringement of the ’616 Patent, for which there is no adequate remedy at law, unless Defendant’s infringement is enjoined by this Court.

107. TI has committed and continues to commit acts of infringement that TI actually knew or should have known constituted an unjustifiably high risk of infringement of at least one valid and enforceable claim of the ’616 Patent. TI’s direct and indirect infringement of the ’616 Patent has been and continues to be willful, intentional, deliberate, and/or in conscious disregard of Rampart’s rights under the patent. Rampart is entitled to an award of treble damages, reasonable attorney fees, and costs in bringing this action.

COUNT VI
(Infringement of the ’511 Patent)

108. Paragraphs 1 through 23 are incorporated by reference as if fully set forth herein.

109. Rampart has not licensed or otherwise authorized Defendant to make, use, offer for sale, sell, or import any products that embody the inventions of the ’511 Patent.

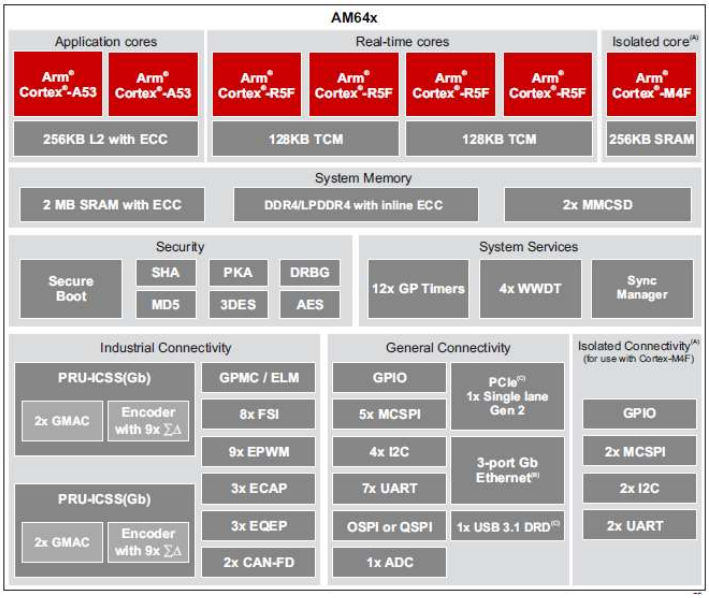
110. Defendant has and continues to directly infringe the ’511 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making,

using, offering to sell, selling, and/or importing into the United States the Accused Products including, but not limited to, products supporting DDR4 external memories, such as the TI AM6442, AM6441, AM6421, AM6412, and AM6411 Sitara Processors.

111. For example, Defendant has and continues to directly infringe at least Claim 1 of the '511 Patent by using products that include a memory controller that complies with the DDR4 standard. For example, the TI AM6442 includes DDR4 memory controllers capable of conducting memory operations in a memory system consisting of DDR4 SDRAMs, each of which is compliant with the JEDEC standard JESD79-4D.

112. The Accused Products including DDR4 memory controllers, including the TI AM6442, perform a method of setting a parameter in an integrated circuit receiver to a value selected from a set of possible values, the integrated circuit receiver to receive a signal from a conductive signal path. Products containing DDR4 memory controllers, including the TI AM6442, are connected to one or more DDR4 SDRAMs under their control in part via the DQ lines that are part of the memory bus, which are conductive signal paths. The DDR4 SDRAM(s) respond(s) to commands from the DDR4 memory controller in the AM6442. Part of the initialization of the memory system by the memory controller in the Accused Products including DDR4 memory controllers, including the AM6442, is a procedure called VrefDQ Training. In VrefDQ Training, memory controller iteratively causes the DDR4 SDRAMs to adjust, via writes to the SDRAM's mode registers, the SDRAM's internally generated VrefDQ voltage which is used in the DQ receivers in the SDRAMs during the capturing of data values arriving on the DQ signal lines from the memory controller. A DDR4 SDRAM in the memory system is an integrated circuit. The VrefDQ voltage is set in the SDRAM to a value set by the memory controller writing specific bit

patterns into Mode Register 6 (MR6) bits 7:0 (VrefDQ Training Range and VrefDQ Training Value).



AM64x Sitara Processors Datasheet, SPRSP56B, August 2021, p. 5.

Memory subsystem:

- Up to 2MB of On-chip RAM (OCSRAM) with SECDED ECC:
  - Can be divided into smaller banks in increments of 256KB for as many as 8 separate memory banks
  - Each memory bank can be allocated to a single core to facilitate software task partitioning
- DDR Subsystem (DDRSS)
  - Supports LPDDR4, DDR4 memory types
  - 16-Bit data bus with inline ECC
  - Supports speeds up to 1600 MT/s

AM64x Sitara Processors Datasheet, SPRSP56B, August 2021, p. 1.

Table 5-1. Device Comparison

FEATURES	REFERENCE NAME	AM6442	AM6441	AM6422	AM6421	AM6412	AM6411
CTRLMMR_WKUP_JTAG_DEVICE_ID[31:13] DEVICE_ID register bit field value[1]		D: 0x19464 E: 0x19465 F: 0x19466	D: 0x19264 E: 0x19265 F: 0x19266	C: 0x19423	D: 0x19224 E: 0x19225 F: 0x19226	C: 0x19403	C: 0x19203
PROCESSORS AND ACCELERATORS							
Speed Grades		See Table 7-1					
Arm Cortex-A53 Microprocessor Subsystem	Arm A53	Dual Core	Single Core	Dual Core	Single Core	Dual Core	Single Core
Arm Cortex-R5F	Arm R5F	2 x Dual Core	2 x Dual Core	1 x Dual Core	1 x Dual Core	Single Core	Single Core
Arm Cortex-M4F	Arm M4F	Single Core					
Device Management Security Controller	DMSC-L	Yes					
Cryto Accelerators	Security	Yes					
MCU domain with Arm Cortex-M4F	Safety	Yes					
PROGRAM AND DATA STORAGE							
On-Chip Shared Memory (RAM) in MAIN Domain	OCSRAM	2MB					
R5F Tightly Coupled Memory (TCM)	TCM	256KB	256KB	256KB	256KB	128KB	128KB
On-Chip Shared Memory (RAM) in M4F Domain	MCU_MSRAM	256KB					
DDR4/LPDDR4 DDR Subsystem	DDRSS	Up to 2GB (16-bit data) with inline ECC					

AM64x Sitara Processors Datasheet, SPRSP56B, August 2021, p. 7.

The required characteristics of DDR4 SDRAMs and memory systems and therefore of DDR4 memory controllers and their encompassing integrated circuits are defined by JEDEC in a collection of publicly available standards. In particular, standard JSD79-4 is the standard defining DDR4 SDRAMs, and JESD79-4D is the latest version of that standard, dated July 2021.

> This document defines the DDR4 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this Standard is to define the minimum set of requirements for JEDEC compliant 2 Gb through 16 Gb for x4, x8, and x16 DDR4 SDRAM devices. This standard was created based on the DDR3 standards (JESD79-3) and some aspects of the DDR and DDR2 standards (JESD79, JESD79-2).

JESD79-4D, p. 1.

The AM6442 is connected to the DDR4 SDRAM(s), in part, via the data lines of the memory bus, labelled DDR0_DQi at the AM6442 and DQ at the DDR4 SDRAM(s).

6.3.2 DDRSS

6.3.2.1 MAIN Domain

Table 6-3. DDRSS0 Signal Descriptions

SIGNAL NAME	PIN TYPE	DESCRIPTION	ALV
DDR0_DQ0	IO	DDRSS Data	A3
DDR0_DQ1	IO	DDRSS Data	A2
DDR0_DQ2	IO	DDRSS Data	B5
DDR0_DQ3	IO	DDRSS Data	A4
DDR0_DQ4	IO	DDRSS Data	B3
DDR0_DQ5	IO	DDRSS Data	C4
DDR0_DQ6	IO	DDRSS Data	C2
DDR0_DQ7	IO	DDRSS Data	B4
DDR0_DQ8	IO	DDRSS Data	N5
DDR0_DQ9	IO	DDRSS Data	L4
DDR0_DQ10	IO	DDRSS Data	L2
DDR0_DQ11	IO	DDRSS Data	M3
DDR0_DQ12	IO	DDRSS Data	N4
DDR0_DQ13	IO	DDRSS Data	N3
DDR0_DQ14	IO	DDRSS Data	M4
DDR0_DQ15	IO	DDRSS Data	N2

AM64x Sitara Processors Datasheet, SPRSP56B, August 2021, pp. 74-75.

Table 3 — Pinout Description (Cont'd)

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.

JESD79-4D, p. 6.

113. The Accused Products including DDR4 memory controllers, including the AM6442, cause the DDR4 SDRAMs to sample the conductive signal path with a sampling circuit of the integrated circuit receiver while iteratively setting the parameter to be different values in the set, to produce digital samples. As part of the VrefDQ Training procedure, each of the DDR4 SDRAMs that are part of the memory system receive write commands and sample the DQ conductive signal paths with the input receivers coupled to the conductive signal path. These receivers each include a sampling circuit that samples the DQ conductive signal path on the rising

and falling edges of DQS_t/DQS_c. These samplings produce digital samples, the accuracy of which are a function of the present VrefDQ range and value. As a result of testing the accuracy of that sampling, the memory controller iteratively sets the VrefDQ range and VrefDQ value in MR6 to adjust the VrefDQ in the DDR4 SDRAM.

4.13 DQ Vref Training (cont'd)

The Vref increment/decrement step times are defined by Vref_time. The Vref_time is defined from t0 to t1 as shown in the Figure 30 below where t1 is referenced to when the vref voltage is at the final DC level within the Vref valid tolerance (Vref_val_tol).

The Vref valid level is defined by Vref_val tolerance to qualify the step time t1 as shown in Figure 32 through Figure 35. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any Vref increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characterization.

Vref_time is the time including up to Vrefmin to Vrefmax or Vrefmax to Vrefmin change in Vref voltage

t0 - is referenced to MRS command clock
t1 - is referenced to the Vref_val_tol

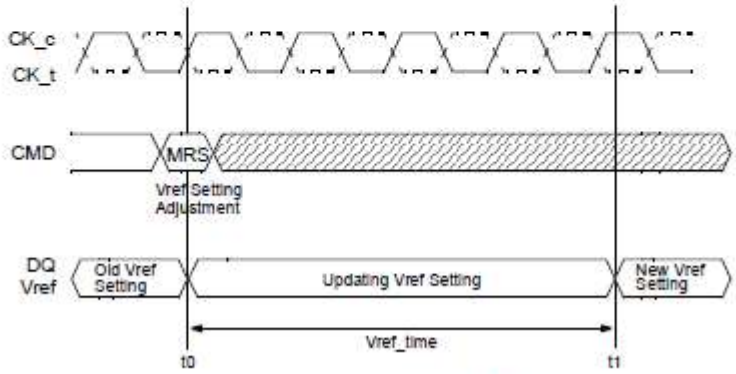
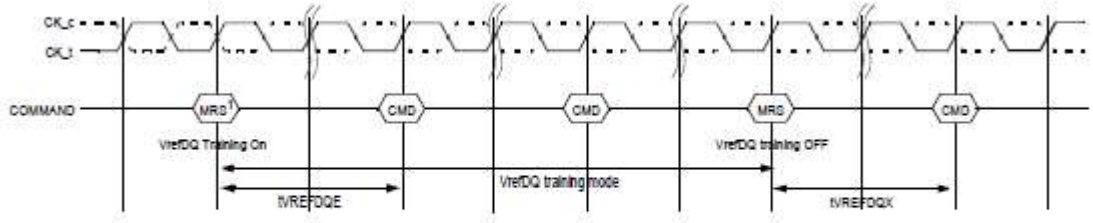


Figure 30 — Vref_time timing diagram

JESD79-4D, p. 59.

4.13 DQ Vref Training (cont'd)



NOTE 1 The MR command used to enter VrefDQ Calibration Mode treats MR6 A[5:0] as don't care while the next subsequent MR command sets VrefDQ values in MR6 A[5:0] .
NOTE 2 Depending on the step size of the latest programmed VREF value, Vref_time must be satisfied before disabling VrefDQ training mode.

Figure 31 — VrefDQ training mode entry and exit timing diagram

JESD79-4D, p. 60.

The Vref_DQ voltage is an internal reference voltage level that shall be set to the properly trained setting, which is generally Vcent_DQ(midpoint), in order to have valid Rx Mask values.

Vcent_DQ(midpoint) is defined as the midpoint between the largest Vref_DQ voltage level and the smallest Vref_DQ voltage level across all DQ pins for a given DDR4 DRAM component. Each DQ pin Vref level is defined by the center, i.e., widest opening, of the cumulative data input eye as depicted in Figure 229. This clarifies that any DDR4 DRAM component level variation must be accounted for within the DDR4 DRAM Rx mask.The component level Vref will be set by the system to account for Ron and ODT settings.

JESD79-4D, p. 250.

3.5 Mode Register (cont'd)

MR6

Table 31 — Mode Register 6

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13, A9, A8	RFU	
A12:A10	tCCD_L	(see Table 32)
A7	VrefDQ Training Enable	0 = Disable (Normal operation Mode) 1 = Enable (Training Mode)
A6	VrefDQ Training Range	(see Table 33)
A5:A0	VrefDQ Training Value	(see Table 34)

JESD79-4D, p. 27.

Table 34 — VrefDQ Training: Values

A5:A0	Range1	Range2	A5:A0	Range1	Range2
00 0000	60.00%	45.00%	01 1010	76.90%	61.90%
00 0001	60.65%	45.65%	01 1011	77.55%	62.55%
00 0010	61.30%	46.30%	01 1100	78.20%	63.20%
00 0011	61.95%	46.95%	01 1101	78.85%	63.85%
00 0100	62.60%	47.60%	01 1110	79.50%	64.50%
00 0101	63.25%	48.25%	01 1111	80.15%	65.15%
00 0110	63.90%	48.90%	10 0000	80.80%	65.80%
00 0111	64.55%	49.55%	10 0001	81.45%	66.45%
00 1000	65.20%	50.20%	10 0010	82.10%	67.10%
00 1001	65.85%	50.85%	10 0011	82.75%	67.75%
00 1010	66.50%	51.50%	10 0100	83.40%	68.40%
00 1011	67.15%	52.15%	10 0101	84.05%	69.05%
00 1100	67.80%	52.80%	10 0110	84.70%	69.70%
00 1101	68.45%	53.45%	10 0111	85.35%	70.35%
00 1110	69.10%	54.10%	10 1000	86.00%	71.00%
00 1111	69.75%	54.75%	10 1001	86.65%	71.65%
01 0000	70.40%	55.40%	10 1010	87.30%	72.30%
01 0001	71.05%	56.05%	10 1011	87.95%	72.95%
01 0010	71.70%	56.70%	10 1100	88.60%	73.60%
01 0011	72.35%	57.35%	10 1101	89.25%	74.25%
01 0100	73.00%	58.00%	10 1110	89.90%	74.90%
01 0101	73.65%	58.65%	10 1111	90.55%	75.55%
01 0110	74.30%	59.30%	11 0000	91.20%	76.20%
01 0111	74.95%	59.95%	11 0001	91.85%	76.85%
01 1000	75.60%	60.60%	11 0010	92.50%	77.50%
01 1001	76.25%	61.25%	11 0011 to 11 1111	Reserved	Reserved

JESD79-4D, p. 28.

114. The Accused Products including DDR4 memory controllers, including the TI AM6442, compare the digital samples with expected values to obtain pass/fail information for each of the different values. The memory controller compares the digital samples generated by the DQ receiver in the DDR4 SDRAMs with the values sent by the memory controller to obtain an indication of whether the DDR4 SDRAM accurately sampled the DQ signals on the DQ conductive signal paths. This is done for each of the attempted VrefDQ values.

4.13.1 Example scripts for VREFDQ Calibration Mode:

When MR6 [7] = 0 then MR6 [6:0] = XXXXXXX

Entering VREFDQ Calibration if entering range 1:
- MR6 [7:6]=10 & [5:0]=XXXXXX
- All subsequent VREFDQ Calibration MR setting commands are MR6 [7:6]=10 & MR6 [5:0]=VVVVVV {VVVVVV are desired settings for VrefDQ}
- Issue ACT/WR/RD looking for pass/fail to determine Vcent(midpoint) as needed
- Just prior to exiting VREFDQ Calibration mode:
- Last two VREFDQ Calibration MR commands are
- MR6 [7:6]=10, MR6 [5:0]=VVVVVV' where VVVVVV' = desired value for VREFDQ
- MR6 [7]=0, MR6 [6:0]=XXXXXXX to exit VREFDQ Calibration mode

Entering VREFDQ Calibration if entering range 2:
- MR6 [7:6]=11 & [5:0]=XXXXXX
- All subsequent VREFDQ Calibration MR setting commands are MR6 [7:6]=11 & MR6 [5:0]=VVVVVV {VVVVVV are desired settings for VrefDQ}
- Issue ACT/WR/RD looking for pass/fail to determine Vcent(midpoint) as needed
- Just prior to exiting VREFDQ Calibration mode:
- Last two VREFDQ Calibration MR commands are
- MR6 [7:6]=11, MR6 [5:0]=VVVVVV' where VVVVVV' = desired value for VREFDQ
- MR6 [7]=0, MR6 [6:0]=XXXXXXX to exit VREFDQ Calibration mode

JESD79-4D, p. 60.

115. The Accused Products including DDR4 memory controllers, including the TI AM6442, based on the pass/fail information for each of the different values, select one of the values from the set for use as the parameter. Based on the pass/fail indications of the data transmission tests for the different values of VrefDQ attempted, one value is selected for use during normal operation of the memory system after initialization and calibration is complete.

116. Additionally, the Accused Products including DDR4 memory controllers, including the TI AM6442, perform the aforementioned method wherein the parameter is one of a sampling phase offset, a voltage threshold offset, or an equalization setting used to produce sampled digital values from the signal. The parameter VrefDQ is a voltage threshold offset used in sampling digital DQ values from the DQ conductive signal path.

The Vref_DQ voltage is an internal reference voltage level that shall be set to the properly trained setting, which is generally Vcent_DQ(midpoint), in order to have valid Rx Mask values.
Vcent_DQ(midpoint) is defined as the midpoint between the largest Vref_DQ voltage level and the smallest Vref_DQ voltage level across all DQ pins for a given DDR4 DRAM component. Each DQ pin Vref level is defined by the center, i.e., widest opening, of the cumulative data input eye as depicted in Figure 229. This clarifies that any DDR4 DRAM component level variation must be accounted for within the DDR4 DRAM Rx mask.The component level Vref will be set by the system to account for Ron and ODT settings.

JESD79-4D, p. 250.

117. Defendant has and continues to indirectly infringe one or more claims of the ’511 Patent by knowingly and intentionally inducing others, including TI customers and end-users, to

directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products.

118. Defendant, with knowledge that these products, or the use thereof, infringe the '511 Patent at least as of the date of this Complaint, knowingly and intentionally induced, and continues to knowingly and intentionally induce, direct infringement of the '511 Patent by providing these products to end-users for use in an infringing manner.

119. Defendant induced infringement by others, including end-users, with the intent to cause infringing acts by others or, in the alternative, with the belief that there was a high probability that others, including end-users, infringe the '511 Patent, but while remaining willfully blind to the infringement.

120. Rampart has suffered damages as a result of Defendant's direct and indirect infringement of the '511 Patent in an amount to be proved at trial.

121. Rampart has suffered, and will continue to suffer, irreparable harm as a result of Defendant's infringement of the '511 Patent for which there is no adequate remedy at law, unless Defendant's infringement is enjoined by this Court.

DEMAND FOR JURY TRIAL

Plaintiff hereby demands a jury for all issues so triable.

PRAYER FOR RELIEF

WHEREFORE, Rampart prays for relief against Defendant as follows:

a. Entry of judgment declaring that Defendant has directly and/or indirectly infringed one or more claims of each of the Patents-in-Suit;

b. An order pursuant to 35 U.S.C. § 283 permanently enjoining Defendant, its officers, agents, servants, employees, attorneys, and those persons in active concert or

participation with them, from further acts of infringement of the Patents-in-Suit;

c. An order awarding damages sufficient to compensate Rampart for Defendant's infringement of the Patents-in-Suit, but in no event less than a reasonable royalty, together with interest and costs;

d. Entry of judgment declaring that this case is exceptional and awarding Rampart its costs and reasonable attorney fees under 35 U.S.C. § 285;

e. Entry of judgment awarding treble damages pursuant to 35 U.S.C. § 284 for Defendant's willful infringement of one or more of the Patents-in-Suit; and

f. Such other and further relief as the Court deems just and proper.

Dated: January 21, 2022

Respectfully submitted,

/s/ *Alfred R. Fabricant*

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