HIGHLY CONFIDENTIAL SUBJECT TO PROJECTIVE ORDER

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

TEXASLDPC INC., Plaintiff, v. BROADCOM INC., LSI CORPORATION, AVAGO TECHNOLOGIES U.S. INC. Defendants.	C.A. No. 18-1966-SB **JURY TRIAL DEMANDED** REDACTED [redacted]

THIRD AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff TexasLDPC Inc. (the "Plaintiff" or "TexasLDPC"), by and through its attorneys, for its Third Amended Complaint for patent and copyright infringement against Broadcom Inc., LSI Corporation, and Avago Technologies U.S. Inc. (collectively, the "Defendants"), hereby alleges as follows:

THE PARTIES

1. Plaintiff TexasLDPC Inc. is a Texas Corporation with its principal place of business located at 1920 W Villa Maria Rd #301, Bryan, Texas 77807.

2. TexasLDPC designs and markets LDPC solutions for use in the Flash, Hard Disk, Wi-Fi, 5G, and NVM technologies under the name Symbyon Systems (www.symbyon.com).

3. TexasLDPC has received funding from the National Science Foundation (both SBIR Phase 1 and Phase 2 funding) to apply LDPC technology to Flash Memory storage systems.

4. On information and belief, Broadcom Inc. is a Delaware corporation with its principal place of business located at 1320 Ridder Park Drive San Jose, California 95131.

5. On information and belief, Broadcom Inc. conducts business operations throughout the United States, including in the State of Delaware.

6. On information and belief, LSI Corporation ("LSI") is a Delaware corporation headquartered at 1320 Ridder Park Drive, San Jose, California 95131. LSI designs, develops, and supplies storage and networking integrated circuits.

7. On information and belief, LSI conducts business operations throughout the United States, including in the State of Delaware.

8. On information and belief Avago Technologies U.S. Inc. ("Avago U.S.") is a Delaware corporation headquartered at 1320 Ridder Park Drive, San Jose, California 95131. Since March 2015, Avago U.S. has handled the U.S. sale and distribution of LSI products.

9. On information and belief, Avago U.S. conducts business operations throughout the United States, including in the State of Delaware.

10. On information and belief, LSI was formed as a result of the merger of LSI Logic Corporation and Agere Systems Inc. in 2007. Avago Technologies Limited then acquired LSI in 2014.

11. On information and belief, LSI and Avago U.S. are both wholly owned indirect subsidiaries of holding company Avago Technologies Limited.

12. On information and belief, Avago Technologies Limited is a wholly owned indirect subsidiary of holding company Broadcom Inc. (formerly known as Broadcom Limited).

13. On information and belief, LSI was acquired by Avago Technologies Ltd. ("Avago"), a Singapore Corporation, in 2014.

14. On information and belief, Avago acquired Broadcom Corporation, a California Corporation, in 2016, and adopted the name Broadcom Limited. On information and belief, Broadcom Limited was redomiciled in the United States as Broadcom Inc. in 2018. Broadcom

Inc. is a designer, developer, and global supplier of products based on analog and digital semiconductor technologies.

15. Defendants Broadcom Inc., LSI, and Avago U.S. will be referred to herein as the Defendants, which shall be understood to refer to them collectively or individually as supported by the context of any particular statement or allegation.

16. On information and belief, Defendants, alone or through other subsidiaries as agents, collectively operate a worldwide design, manufacturing, and sales operation that operates collectively to design, engineer, market, and sell Accused Products.

17. On information and belief, Defendants, alone or through other subsidiaries as agents, market and sell Accused Products to customers both in the United States and elsewhere around the world.

18. On information and belief, Defendants, alone or through other subsidiaries as agents, mostly manufacturing the Accused Products in Asia.

19. On information and belief, a majority of the Accused Products sold by Defendants, alone or through other subsidiaries as agents, outside of the United States are sold with Defendants' knowledge and intention of those Accused Products being incorporated as components within customers' end-user products.

20. On information and belief, a majority of the Accused Products sold by Defendants, alone or through other subsidiaries as agents, outside of the United States are sold with Defendants' knowledge that their customers' end-user products containing the Accused Products will be imported into the United States to be used in an infringing manner in the United States.

21. LSI Logic Corporation, Agere Systems Inc., Avago Technologies Limited, and Broadcom Limited will be referred to herein as the Broadcom Predecessor Entities, which shall be understood to refer to them collectively or individually, along with the Defendants, as supported by the context of any particular statement or allegation.

JURISDICTION AND VENUE

22. Plaintiff's patent infringement claims arise under the Patent Laws of the United States, 35 U.S.C. §§ 100 *et seq*. This Court has jurisdiction over the subject matter of this action under 28 U.S.C. §§ 1331 and 1338(a).

23. Plaintiff's copyright infringement claims arise under the Copyright Laws of the United States, 17 U.S.C. §§ 101, *et seq*. This Court has exclusive subject matter jurisdiction over the copyright claims under 28 U.S.C. § 1331 and 1338 and 17 U.S.C. § 501(a).

24. This Court has personal jurisdiction over Defendants Avago Technologies U.S. Inc., LSI Corporation, and Broadcom, Inc. ("Defendants") because the Defendants are Delaware corporations.

25. Defendants are registered to do business in the State of Delaware.

26. Corporation Service Company, 251 Little Falls Drive, Wilmington, DE 19808, serves as Defendants' Registered Agent in the State of Delaware.

27. The Court has personal jurisdiction over Defendants because Defendants are incorporated in this judicial district and because, on information and belief, Defendants have regularly and systematically transacted business in this judicial district, directly or through intermediaries, and/or committed acts of infringement in this judicial district. Defendants have also placed infringing products into the stream of commerce by shipping those products into this district or knowing that the products would be shipped into this District.

28. Affiliates and subsidiaries of Defendants provide a distribution channel of infringing products within this Judicial District and the U.S. nationally.

29. Affiliates and subsidiaries of Defendants place infringing products into the stream of commerce knowing they will be sold and used in the State of Delaware and elsewhere in the United States and economically benefits from the retail sale of infringing products in the State of Delaware.

30. Defendants alone or through other subsidiaries as agents, make the Accused Products and supplies and/or make available the Accused Products to companies that further market and sell the Accused Products and products containing the Accused Products.

31. The division of labor between making, manufacturing, marketing and sales amongst all of the Defendants and their distributors amounts to an organized association, establishing a distribution channel for the Accused Products in the United States.

32. Defendants know or can reasonably foresee that a termination point of the distribution channel targeted to the United States includes this Judicial District (as further described below).

33. Venue is proper in this judicial district pursuant to 28 U.S.C. §1400(b) for the Defendants.

34. As noted above, Defendants (individually or in concert with one another) have committed and continue to commit acts of infringement under Fed. R. Civ. P. 4(k)(2) and within this Judicial District giving rise to this action.

PATENTS-IN-SUIT

35. On August 9, 2013, United States Patent No. 8,418,023 ("the '023 Patent"), entitled "Low Density Parity Check Decoder For Irregular LDPC Codes," was duly and legally

issued by the United States Patent and Trademark Office ("PTO"). A true and correct copy of the '023 Patent is attached hereto as **Exhibit A**.

36. On October 8, 2013, United States Patent No. 8,555,140 ("the '140 Patent"), entitled "Low Density Parity Check Decoder For Irregular LDPC Codes," was duly and legally issued by the PTO. A true and correct copy of the '140 Patent is attached hereto as **Exhibit B**.

37. On August 18, 2015, United States Patent No. 9,112,530 ("the '530 Patent"), entitled "Low Density Parity Check Decoder," was duly and legally issued by the PTO. A true and correct copy of the '530 Patent is attached hereto as **Exhibit C**.

38. On January 22, 2013, United States Patent No. 8,359,522 ("the '522 Patent"), entitled "Low Density Parity Check Decoder For Regular LDPC Codes," was duly and legally issued by the PTO. A true and correct copy of the '522 Patent is attached hereto as **Exhibit D**.

39. On February 18, 2014, United States Patent No. 8,656,250 ("the '250 Patent"), entitled "Low Density Parity Check Decoder For Irregular LDPC Codes," was duly and legally issued by the PTO. A true and correct copy of the '250 Patent is attached hereto as **Exhibit E**.

40. On November 27, 2018, United States Patent No. 10,141,950 ("the '950 Patent"), entitled "Low Density Parity Check Decoder," was duly and legally issued by the PTO. A true and correct copy of the '950 Patent is attached hereto as **Exhibit F**.

41. The '023, '140, '530, '522, '250, and '950 Patents are collectively referred to herein as the "Patents-in-Suit."

42. The Patents-in-Suit are each assigned by their named inventors, Dr. Kiran Gunnam ("Dr. Gunnam"), and Dr. Gwan S. Choi, to the Texas A&M University System (TAMUS).

43. Plaintiff is the exclusive licensee of each of the Patents-in-Suit pursuant to a license agreement between TAMUS and Plaintiff, executed on June 18, 2015 (the "TAMUS License Agreement"). Pursuant to the TAMUS License Agreement, Plaintiff has the exclusive and sole right (subject a pre-existing license) to practice the Patents-in-Suit, grant sub-licenses thereto, and sue and recover damages for the past, present, and future infringement of the Patents-in-Suit.

COPYRIGHTS-IN-SUIT

44. Dr. Gunnam, while an employee of Texas A&M Engineering Experiment Station ("TEES"), a subdivision of TAMUS, working under the guidance and review from Dr. Choi, an employee of TEES, expended time, intellectual effort, and capital to create a computer program work entitled "Source Code for Certain Low Density Parity Check Algorithms" (the "LDPC Algorithms Source Code Work").

Title

Title of Work: Source Code for Certain Low Density Parity Check Algorithms

Completion/Publication

Year of Completion: 2007

Author

- **Author:** The Texas A&M University System

Author Created: computer program

Work made for hire: Yes

Domiciled in: United States

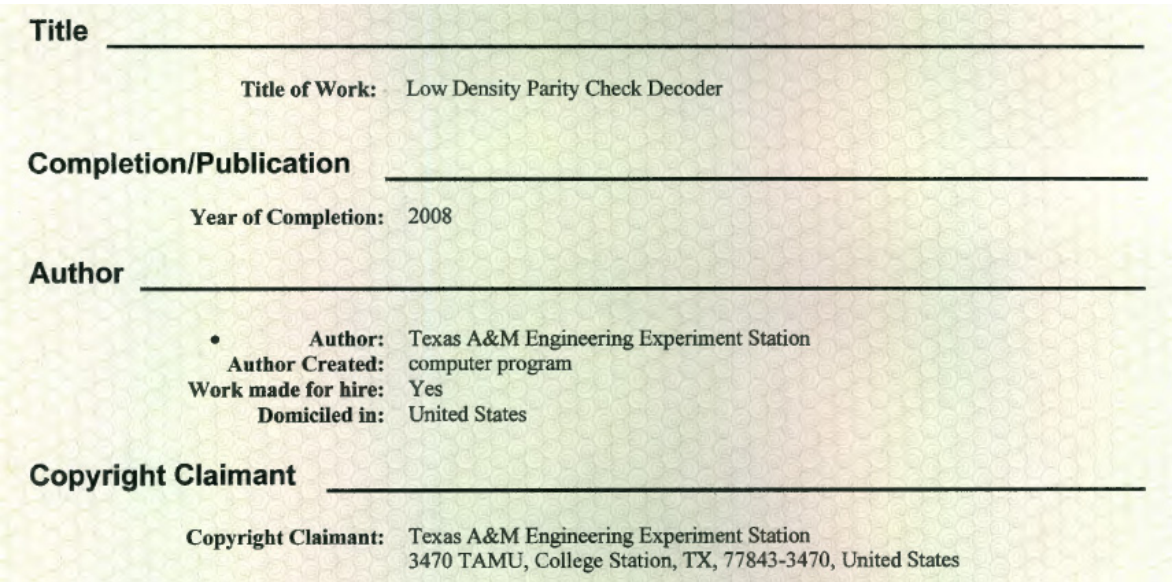
Copyright claimant

Copyright Claimant: The Texas A&M University System

301 Tarrow, John B. Connally Bldg., College Station, TX, 77840-7896, United States

45. As shown above, TAMUS registered its copyright in and to the LDPC Algorithms Source Code Work with the United States Copyright Office, and was granted U.S. Copyright Registration No. TXu 1-842-620, which issued on February 11, 2013. Attached hereto as **Exhibit G** is a copy of Registration No. TXu 1-842-620.

46. Dr. Gunnam, while an employee of TEES, a subdivision of TAMUS, working under the guidance and review from Dr. Choi, an employee of TEES, expended time, intellectual effort, and capital to create a computer program work entitled "Low Density Parity Check Decoder" (the "LDPC Decoder Program Work").



Title

Title of Work: Low Density Parity Check Decoder

Completion/Publication

Year of Completion: 2008

Author

- **Author:** Texas A&M Engineering Experiment Station
  Author Created: computer program
  Work made for hire: Yes
  Domiciled in: United States

Copyright Claimant

Copyright Claimant: Texas A&M Engineering Experiment Station
3470 TAMU, College Station, TX, 77843-3470, United States

47. As shown above, TEES registered its copyright in and to the LDPC Decoder Program Work with the United States Copyright Office, and was granted U.S. Copyright Registration No. TXu 2-001-020, which issued on October 12, 2015. Attached hereto as **Exhibit H** is a copy of Registration No. TXu 2-001-020.

48. Dr. Gunnam, while an employee of TEES, a subdivision of TAMUS, working under the guidance and review from Dr. Choi, an employee of TEES, expended time, intellectual effort, and capital to create a computer program work entitled "Source Code for Low Density Parity Check Decoder and Its Modules" (the "LDPC Decoder Source Code Work").

Title

Title of Work: Source Code for Low Density Parity Check Decoder and Its Modules

Completion/Publication

Year of Completion: 2007

Author

- **Author:** Texas A&M Engineering Experiment Station
  Author Created: computer program
  Work made for hire: Yes
  Domiciled in: United States

Copyright Claimant

Copyright Claimant: Texas A&M Engineering Experiment Station
3369 TAMU, College Station, TX, 77843-3369, United States

49. As shown above, TEES registered its copyright in and to the LDPC Decoder Source Code Work with the United States Copyright Office, and was granted U.S. Copyright Registration No. TXu 2-033-302, which issued on November 29, 2016. Attached hereto as **Exhibit I** is a copy of Registration No. TXu 2-033-302.

50. Collectively TAMUS' LDPC Algorithms Source Code Work, LDPC Decoder Program Work, and LDPC Decoder Source Code Work constitute the "TAMUS Copyrighted Works." Pursuant to the TAMUS License Agreement, Plaintiff has been granted by TAMUS an exclusive license and right to reproduce, distribute, publicly display and perform, and make derivative works from the TAMUS Copyrighted Works, grant sublicenses thereto, and to sue for infringement of the copyrights in the TAMUS Copyrighted Works, including the exclusive right to collect damages for past, present, and future infringement of those copyrights.

51. The TAMUS Copyrighted Works were marked with copyright notifications informing any reader that the works were copyrighted – thus making any copying by Defendants willful.

52. Defendant LSI was also notified by Dr. Gunnam that the TAMUS Copyrighted Works were property of TAMUS and could not be copied or used without a license.

FACTUAL BACKGROUND

Development of the Patented Technology

53. Each of the Patents-in-Suit is directed to improved designs and methods for using low-density parity check code ("LDPC") decoders.

54. LDPC decoders decode data that has been encoded using an LDPC code, a type of error correcting code. By encoding data in this fashion, digital electronic devices can transmit data over a noisy channel, while being able to detect and correct errors. As a result, such devices are able to operate at substantially higher data rates than would otherwise be possible.

55. The Patents-in-Suit improve upon prior LDPC decoder technology by providing decoder designs and techniques that are faster, more compact, and more energy efficient than prior art designs. These designs were developed by Dr. Kiran Gunnam, then a doctoral student at Texas A&M University (TAMU), working under the supervision of his thesis advisor, Prof. Gwan Choi. Dr. Gunnam and Prof. Choi discovered techniques to optimize the then-conventional algorithms and circuit architectures for LDPC decoders so that they used less memory and avoided redundant calculations. Dr. Gunnam and Prof. Choi first described aspects of their new design in a technical report entitled "A Low Power Architecture for Min-Sum Decoding of LDPC Codes," TAMU-ECE-2006-02 (the "Low Power Architecture" report), which is available at https://cesg.tamu.edu/techreports/, and issued in May, 2006.

56. Subsequent to the issuance of the Low Power Architecture report, Dr. Gunnam and Prof. Choi published and presented extensively about aspects and applications of their new LDPC decoder designs, including in the following publications and presentations:

- Gunnam, *et al.*, "VLSI Architectures for Layered Decoding for Irregular LDPC Codes of WiMax," 2007 IEEE International Conference on Communications (Glasgow, UK, June 2007).
- Gunnam, *et al.*, "Decoding of Quasi-cyclic LDPC Codes Using an On-the-Fly Computation," 2006 Asilomar Conference on Signals, Systems and Computers (Pacific Grove, CA, October 2006).
- Gunnam, "Area and Energy Efficient VLSI Architectures for Low-Density Party-Check Decoders Using On-the-Fly Computation, Ph.D Thesis, Texas A&M University, December, 2006.
- Gunnam, *et al.*, "VLSI Architectures for Turbo Decoding Message Passing Using Min-Sum for Rate-Compatible Array LDPC Codes," 2007 2nd Int'l Symposium on Wireless Pervasive Computing, (San Juan, PR, Feb. 2007).
- Gunnam, *et al.*, "Multi-Rate Layered Decoder Architecture for Block LDPC Codes of the IEEE 802.11n Wireless Standard." 2007 IEEE International Symposium on Circuits and Systems, (New Orleans, LA, May 2007).

57. On May 1, 2007, less than one year after the issuance of the Low Power Architecture report, Dr. Gunnam and Prof. Choi filed a provisional patent application with the United States Patent and Trademark Office ("USPTO"), bearing application number 60/915,320 (the "'320 provisional application"). Each of the Patents-in-Suit claims priority to the '320 provisional application, and at least some of the claims therein therefore entitled to a priority date of at least as early as May 1, 2007.

Development of the Copyrighted Works

58. During the course of his doctoral research, Dr. Gunnam built and tested specific decoding algorithms, decoder scheduling algorithms, decoder hardware architecture, micro-architecture, and circuit designs that implement the teachings of the Patents-in-Suit. Dr. Gunnam created simulation models for these designs in MATLAB code, and design descriptions in RTL code, a hardware description language. Each of the TAMUS Copyrighted Works comprise and share much of the same or substantially the same core Register Transfer Level (RTL) and MATLAB code reflecting Dr. Gunnam's circuit designs decoding algorithms, decoder scheduling algorithms, decoder hardware architecture, micro-architecture, and circuit designs. RTL and MATLAB code provides chip designers with tool for modelling LDPC decoder designs and for describing the physical implementation of LDPC decoders in integrated circuit chips. The TAMUS RTL code – written in Verilog Hardware Description Language (HDL) language – can be input into a logic synthesis tool which in turn creates the gate-level abstraction of the design that is used for all downstream physical chip implementation. The TAMUS MATLAB code can be generally broken into two categories for performing two unique functions: (1) MATLAB code related to RTL source code including (a) micro-code generation and scheduling parameters that provides information on decoder scheduling for TAMUS RTL designs and (b) automated RTL code generation to support the desired parallelization, pipelining and LDPC matrices; and (2) MATLAB code related to modeling including: (a) reference bit accurate verification models and (b) higher level simulation models to verify the performance of the decoder. The TAMUS Copyrighted Works thus represent a collection of directly written RTL source code that can be synthesized into gate level netlists for physical integrated circuit implementation, MATLAB source code that generates additional synthesizable RTL source code to support specific LDPC matrices, desired parallelization and throughput, micro-code and

scheduling parameters for decoder, MATLAB models that serve as reference for verification of RTL code and for error correction performance, all for uniquely implementing Dr. Gunnam's LDPC decoder designs.

Dr. Gunnam's Employment with LSI and LSI's Willful Infringement of the Patents-in-Suit and the TAMUS Copyrighted Works

59. Dr. Gunnam completed his doctoral work at TAMU in December, 2006. In January, 2008, Dr. Gunnam was hired by LSI to work on advanced LDPC decoder designs for the next generation of LSI's TrueStore hard disk drive (HDD) controller chips. LSI was aware of Dr. Gunnam's prior work on advanced designs in this area, and specifically hired him so that he could help them evaluate those designs for possible incorporation into their next generation of HDD controller chips.

60. Prior to and immediately upon arriving at LSI, Dr. Gunnam informed LSI that the advanced LDPC decoder designs that he had developed while at TAMU represented the intellectual property of TAMUS, and that LSI would need to obtain a license from TAMUS if LSI wished to exploit Dr. Gunnam's designs in a commercial product. At the time Dr. Gunnam joined LSI, the decoder design for the newest generation of HDD controllers, code named Mamba, had been frozen, and Dr. Gunnam was eventually invited to work on a subsequent generation design, code named McLaren.

61. In order to help LSI evaluate whether his advanced LDPC decoder designs were suitable for use in the McLaren design, Dr. Gunnam provided LSI with simulation models and circuit design files that he had created while at TAMU, and which are components of the TAMUS Copyrighted Works. Dr. Gunnam provided these files to LSI with the express understanding that if LSI decided to use these designs, it would need to obtain a license from TAMUS.

62. Although LSI held licensing discussions with TAMUS in the 2008 time period, LSI refused TAMUS' licensing terms and did not obtain a license from TAMUS for Dr. Gunnam's advanced LDPC decoder designs.

63. Despite not having obtained a license, LSI continued to investigate using Dr. Gunnam's LDPC decoder designs. In early 2009, Dr. Gunnam was assigned to work on the design of the McLaren LDPC decoder as the architect, under the supervision of Dr. Shaohua Yang ("Dr. Yang") and working closely with a design team led by Yen Johnson ("Mr. Johnson"). Also working under Mr. Johnson was Mr. Madhu Kalluri ("Mr. Kalluri"), a circuit designer and Ms. Lei Chen ("Ms. Chen"), a circuit designer. As part of the design process for the McLaren LDPC decoder, Mr. Kalluri and Ms. Chen worked with TAMUS RTL hardware design files and MATLAB design and simulation files that had been provided to LSI by Dr. Gunnam, and that were part of the TAMUS Copyrighted Works. Mr. Johnson, Mr. Kalluri, Ms. Chen and Dr. Gunnam were all aware that the hardware design files and simulation files were copyrighted by TAMUS and that LSI would need to obtain a license to use them.

64. Despite this knowledge, Mr. Kalluri and Ms. Chen were directed to superficially modify the RTL and MATLAB code that had been provided by Dr. Gunnam, while maintaining the same basic program structure sequence and organization as the original works. Specifically, Mr. Kalluri and Ms. Chen copied substantially line-by-line the program modules common to the TAMUS Copyrighted Works, changing only variable names to disguise the blatant infringement. Mr. Kalluri and Ms. Chen copied, for example, core RTL modules such as LDPC_Decoder_Top.v, Layered_Update_Module.v, Q_Computation_Module.v, P_Computation_Module.v, R_Selection.v, and Convergence_Check_2C_delta_hd.v, LUM_Control.v and MATALAB files such as Gen_LDPC_Decoder_parameters_header.m,

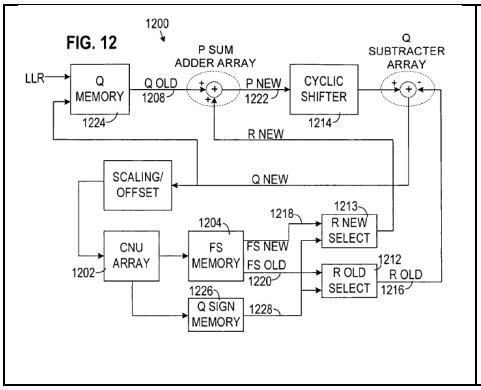
Gen_decoder_verilog_WiMax_Sc96_rcs_C2.m, Shifter4x_Model.m, and premux_switch_expander.m, while making only trivial changes to variable names. The supposed rewrite made to much of the RTL and MATLAB modules amounted to nothing more than changing, for example, the variable used to refer to the message from the check node from 'R' to some other variable. Indeed, the so-called LDPC decoder "top" was unchanged, the decoder control used the very same parameters, control signals and core logic were not changed, and numerous other unique and esoteric aspects of the TAMUS code were untouched. In addition, LSI designers' supposed rewrite of both the RTL and MATLAB code used the very same module hierarchy common to the TAMUS Copyrighted Works, again changing only the names of certain modules. In doing so, LSI created new simulation and design files that had in all material respects the very same, structure, sequence and organization as the TAMUS Copyrighted Works and are thus substantially similar to the TAMUS Copyrighted Works. There are many, if not limitless, ways that a circuit designer could construct the simulation and hardware design software to receive, assemble, calculate, retain, correlate, and produce useful information to carry out Dr. Gunnam's LDPC decoder designs, but LSI simply pirated the particular expression of those ideas as laid out in the TAMUS Copyrighted Works. The LSI "rewrite" therefore constituted unauthorized non-literal copies of the TAMUS Copyrighted Works and unauthorized derivative works derived from the TAMUS Copyrighted Works. Upon information and belief, LSI, and subsequently Broadcom Inc., continued to use the TAMUS Copyrighted Works, the initial LSI "rewrite", and further non-literal copies or derived works in their continuing research and development efforts concerning LDPC decoders used in HDD and SSD controllers and Wi-Fi products. For instance, Ms. Chen modified the TAMUS Copyrighted Works and LSI derived works for subsequent chip variations after McLaren. *See, e.g.*,

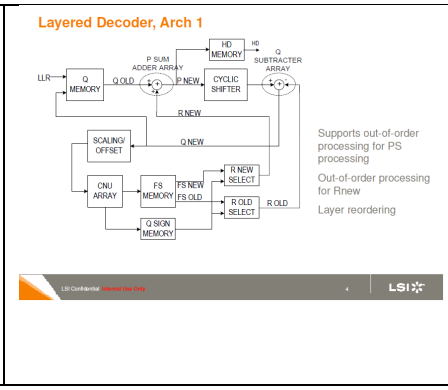
https://www.linkedin.com/in/lei-chen-5a3709b/ (Ms. Chen's Linkedin profile, noting that she implemented Dr. Gunnam's novel LDPC decoders in Verilog while at LSI) LSI, and subsequently Broadcom Inc. thereby infringed TAMUS' copyrights in the TAMUS Copyrighted Works by: (a) making further modifications of the TAMUS Copyrighted Works and or the LSI derived works (and thus making non-literal copies and derived works), and (b) copying the TAMUS Copyrighted Works, the LSI derived works, or further non-literal copies or derived works by loading said works into computer memories (and thereby making literal copies in said computer memories). Upon information and belief, such infringements continue up through the present day.

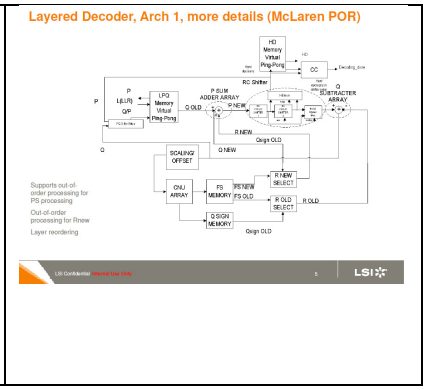
65. In 2009 and 2010, Dr. Gunnam continued to work at LSI on the architecture for the McLaren LDPC decoder and, with LSI's knowledge and approval, incorporated key features from his advanced design work at TAMU into the LSI design. During this period, Dr. Gunnum repeatedly reminded LSI management of its obligation to obtain a license from TAMUS if it wished to use his designs.

66. On August 21, 2009, Dr. Gunnam created an internal LSI presentation entitled "Layered Decoder for LDPC Codes with Zero Matrices" (the "Zero Matrices Presentation"). A copy of this presentation is available on the internet at https://www.scribd.com/document/367470390/read-channel-overview-part-1. Dr. Gunnam's Zero Matrices Presentation described Dr. Gunnam's advanced architectural design for an LDPC Decoder developed at TAMU, a design that was essentially identical to the design in the then-pending patent applications that had been filed by Dr. Gunnam and Prof. Choi, which had been published by the USPTO on November 6, 2008 (Publication No. 2008/0276156A1, the "156 Publication"). The table below shows Figure 12 from the '156 Publication, the basic decoder

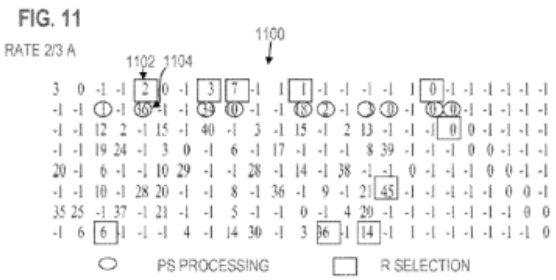
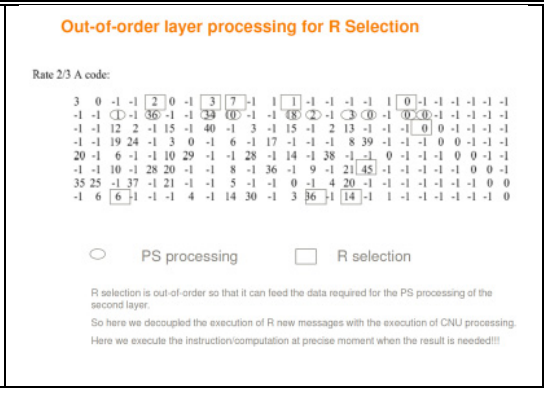
architecture described in Dr. Gunnam's Zero Matrices Presentation, and a further elaboration of that design labelled as McLaren "POR" (Plan of Record).





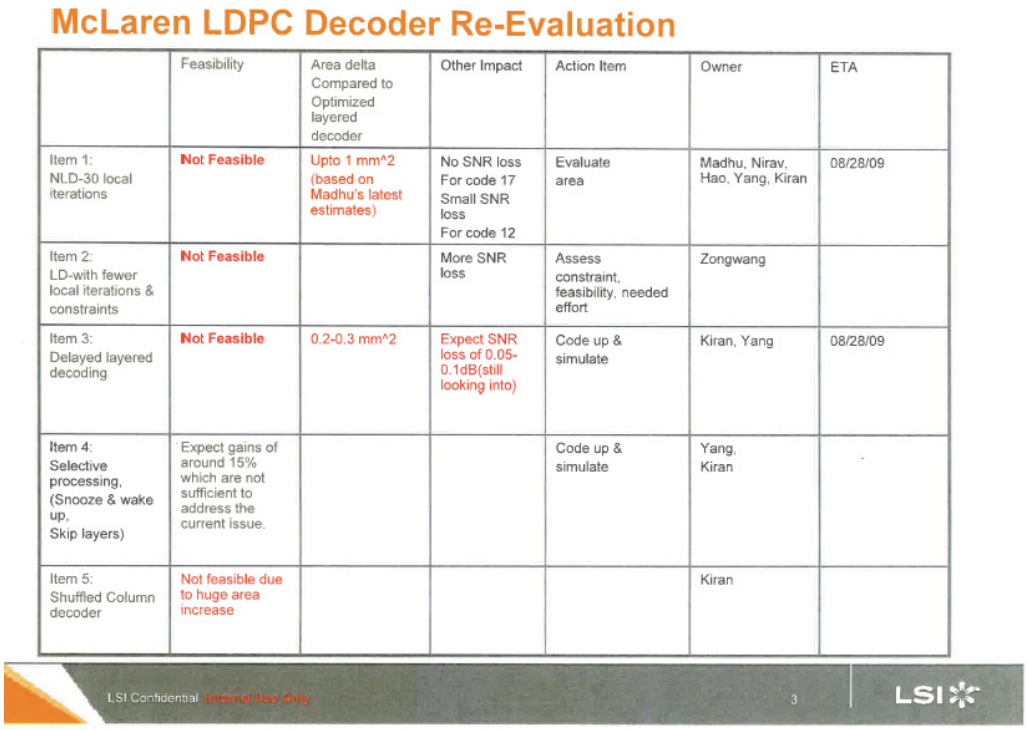


67. Dr. Gunnam's Zero Matrices Presentation included significant additional detail regarding the design of the LDPC decoder that was derived directly from the '156 Publication, as shown in the table below.

'156 Publication	Zero Matrices Presentation
	

68. On August 26, 2009, Dr. Gunnam, along with LSI colleagues Dr. Yan Hang and Mr. Kalluri, made a presentation entitled LDPC Decoder Reevaluation ("Reevaluation Presentation"). A copy of this presentation is available on the internet at https://www.scribd.com/document/367470390/read-channel-overview-part-1. The presentation explained that the "current option McLaren is the layered decoder with layer re-ordering and out-of-order processing," two key concepts from Dr. Gunnam's TAMU design. The presentation further stated that "we would like to re-evaluate the LDPC decoder options for McLaren due to non-technical issues." Upon information and belief, the "non-technical issues" that led to the re-evaluation of Dr. Gunnam's TAMU design was the understanding by LSI management that Dr. Gunnam's design was the subject of TAMUS pending patent applications and copyrights and that the use of that design would necessitate obtaining a license from TAMU.

69. The Reevaluation Presentation ("the presentation") described testing and modelling of five different alternatives to Dr. Gunnam's LDPC Decoder design. As shown in the table below, the presentation concluded that there were no viable alternatives to using Dr. Gunnam's design, and recommended staying with the existing design.



McLaren LDPC Decoder Re-Evaluation

	Feasibility	Area delta Compared to Optimized layered decoder	Other Impact	Action Item	Owner	ETA
Item 1: NLD-30 local iterations	Not Feasible	Upto 1 mm^2 (based on Madhu's latest estimates)	No SNR loss For code 17 Small SNR loss For code 12	Evaluate area	Madhu, Nirav, Hao, Yang, Kiran	08/28/09
Item 2: LD-with fewer local iterations & constraints	Not Feasible		More SNR loss	Assess constraint, feasibility, needed effort	Zongwang	
Item 3: Delayed layered decoding	Not Feasible	0.2-0.3 mm^2	Expect SNR loss of 0.05-0.1dB(still looking into)	Code up & simulate	Kiran, Yang	08/28/09
Item 4: Selective processing, (Snooze & wake up, Skip layers)	Expect gains of around 15% which are not sufficient to address the current issue.			Code up & simulate	Yang, Kiran	
Item 5: Shuffled Column decoder	Not feasible due to huge area increase				Kiran	

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70. In making its recommendation, the presentation noted that "other options have an area penalty of up to 1mm^2 or the SNR loss of more than 0.4dB." In other words, the other alternatives would take up more area, or would be less effective in correcting errors, than Dr. Gunnam's design. Upon information and belief, LSI considered those alternatives commercially unacceptable to Dr. Gunnam's design.

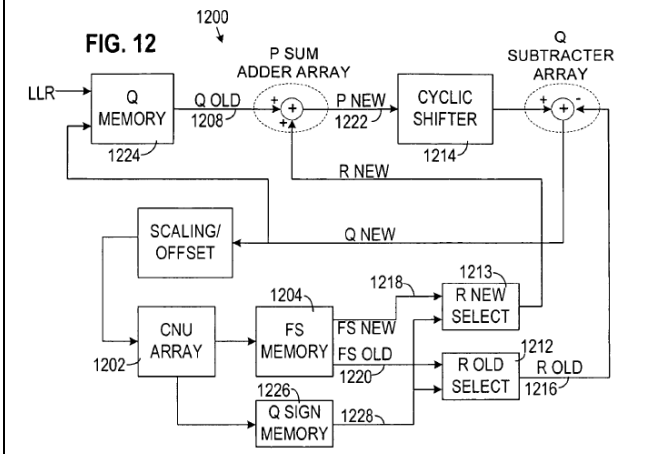
71. On October 13, 2009, an LSI team comprised of Dr. Gunnam, Dr. Yang, and Dr. Zongwang Li, made an internal presentation to LSI entitled "McLaren Client Server Architecture/Scheduling" ("Client Server Presentation"). A copy of this presentation is available on the internet at https://www.scribd.com/document/367470390/read-channel-overview-part-1. The Client Server Presentation, key features of the McLaren LDPC Decoder designs are discussed, and the decoder design is described as follows:

- New Decoder architecture: Use of layered decoder optimized based on "On-the-fly Computation" to minimize memory, logic requirements and remove the pipeline idle cycles and memory access conflicts associated with conventional layered/non-layered decoder designs. The decoder is highly optimized for area and high speed saving upto 1 mm^2 while compared to other implementations.

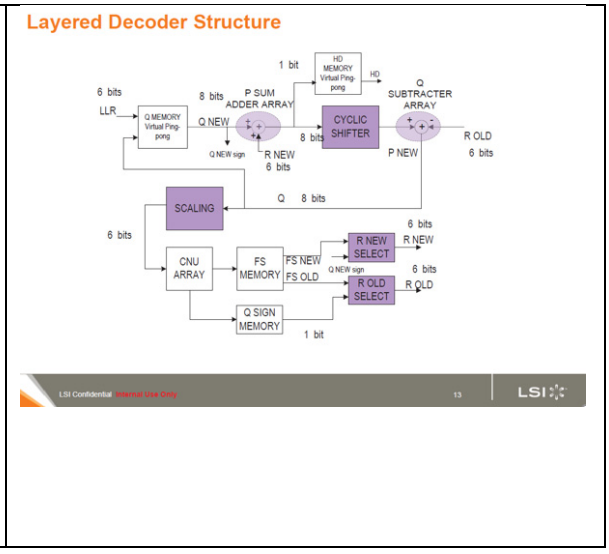
72. This description of the McLaren LDPC decoder included key features of the advanced decoder design developed by Dr. Gunnam at TAMU, including "on-the-fly computation to minimize memory, logic requirements and remove pipeline idle cycles and memory access conflicts associated with conventional layered/non-layered decoder designs."

73. Moreover, the architectural drawing included in the October 13, 2009 presentation was virtually identical to the corresponding drawing (FIG. 12) contained in specification of the Patents-in-Suit, a version of which had been published by the USPTO on November 6, 2008 (Publication No. 2008/0276156A1, the "'156 Publication").

'156 Publication at FIG. 12



LSI's Client Server Presentation



74. LSI management was extremely pleased with the work that Dr. Gunnam did on the LDPC decoder design for the McLaren chip. In his 2009 annual performance review, Dr.

Gunnam's manager, Dr. Yang, gave him an overall descriptor of "Exceeds Expectations," and stated as follows:

> Kiran is the team member who worked hardest literally in the team around the clock. He has demonstrated the highest level of innovation in hardware architecture and decoder algorithm. the Mclaren codec hardware architecture and algorithm is a very smart architecture which sizes ~1mm2 less than any alternative than we have evaluated for the same LDPC code matrix. Kiran innovated the whole read path architecture and half of the write path architecture. The key inventions are the local-global interleaver architecture, layered decoder architecture, and codec integration.
>
> Kiran also worked closely with more than 10 designers (in both Shanghai and Milpitas) on a hourly bases on various modules in the Mclaren channel. He has discovered hundreds of issues and addressed them during the early development stage.

75. Upon information and belief, LSI management finalized the design for the McLaren TrueStore HDD controller chip in 2010, and included patented features of Dr. Gunnam's LDPC decoder design in the final design. During 2010, Dr. Gunnam made repeated requests to LSI management to approach TAMUS to obtain a license for the TAMUS intellectual property that he knew to be incorporated into that design. LSI failed to act upon those requests and never obtained a license from TAMUS, despite its awareness at the time that at its McLaren design incorporated TAMUS intellectual property. LSI's actions caused Dr. Gunnam to become increasingly frustrated with LSI's failure to properly license the TAMUS intellectual property it was using in the McLaren design.

76. On December 21, 2010, Dr. Gunnam wrote an e-mail to certain managers at LSI entitled: "Some important legal and ethical issues." The e-mail pointed out that the LDPC decoder design used in the McLaren design "reads on claims" in his and Dr. Choi's pending, published, patent applications, which, as discussed above, these certain managers were intimately familiar. Dr. Gunnam also stated that the layered decoder architecture proposed for Spyder, the code-name for the generation of HDD controller chips after McLaren, also read on claims in the pending applications. Dr. Gunnam's e-mail urged LSI to "look for a way to license the" pending patent applications. The email also notes that Dr. Gunnam had informed Dr. Yang

(now Director of Read Channel Backend Architecture at Broadcom) that LSI needed to attain a license from Texas A&M. The December 2010 email also stated that Dr. Yang had informed Dr. Gunnam to refrain from listing the Texas A&M patent applications on LSI's internal wiki system related to the McLaren product.

77. In March of 2011, Dr. Gunnam was given his performance review for 2010. In this review, he was reprimanded for the December 21, 2010 e-mail because the e-mail supposedly "compromis[ed] the competitiveness of LSI's recent read channel [i.e., HDD controller] products by putting all possible/suspected IP infringements on record."

78. Shortly after receiving this review, Dr. Gunnam decided to leave his employment with LSI, and resigned in March, 2011.

79. After leaving LSI, Dr. Gunnam continued to be concerned that LSI was using TAMUS intellectual property without a license.

80. On April 27, 2012, Dr. Gunnam contacted Dr. Yuan Xing Lee ("Dr. Lee"), Dr. George Mathew ("Dr. Mathew"), and Mr. Johnson Yen ("Mr. Yen") at their official LSI email addresses to inform them of the pending patent applications for the '023 and '522 Patents.

81. At the time, Dr. Lee was a Vice President in charge of engineering at LSI, Dr. Mathew was a manager at LSI, and Mr. Yen was a senior engineering manager at LSI.

82. As part of this email, Dr. Gunnam again informed LSI that "claims read on several features of non-layered decoder and significant design of layered decoders (for the products I directly worked on as well as the products that are/being made based on my earlier work)."

83. Dr. Lee, Dr. Mathew, and Mr. Yen all received Dr. Gunnam's April 27, 2012 e-mail.

84. On information and belief, Dr. Lee called a meeting at LSI to discuss LSI's use of TAMUS' intellectual property in its products after receiving Dr. Gunnam's April 27, 2012 email. On information and belief, at least Dr. Lee and Mr. Kalluri attended this meeting.

85. On information and belief, LSI took no actions to stop LSI's infringement of the Patents-in-Suit after receiving Dr. Gunnam's April 27, 2012 email.

86. Thereafter, when the '522 Patent issued on January 22, 2013, Dr. Gunnam wrote an e-mail to Dr. Lee, Dr. Mathew, and Mr. Yen, notifying them the patent had issued, and that it covered several features of several implemented LSI decoders, including McLaren and Spyder.

87. Dr. Lee, Dr. Mathew, and Mr. Yen received Dr. Gunnam's January 22, 2013 e-mail.

88. None of these individuals acknowledged Dr. Gunnam's email, nor, upon information and belief, did they take any actions to ensure that the McLaren and Spyder chips were not infringing the '522 Patent.

89. On information and belief, LSI took no actions to stop LSI's infringement of the Patents-in-Suit after receiving Dr. Gunnam's January 22, 2013 email.

90. On January 31, 2014, Dr. Gunnam wrote again to Dr. Lee, informing him that the '023 and '140 Patents had issued, and that the '250 Patent was about to issue on February 18, 2014.

91. In that January 31, 2014 email, Dr. Gunnam reminded Dr. Lee that he had repeatedly discussed with him and other LSI managers over the years that the TAMUS patents disclose key features of LDPC decoders that had been incorporated into LSI's designs, that those decoder designs were "based on the material from these patents and patent applications," and that "the issued and pending patents cover several features of several implemented and planned

layered and non-layered decoders as part of the read channel ICs [i.e., the McLaren and Spyder disk controller chips].” Dr. Gunnam specifically identified claims 1-98 of the ’522 Patent, claims 1-30 of the ’023 Patent, claims 1-22 of the ’140 Patent, and claims 1-54 of the soon-to-issue ’250 Patent as covering features in the McLaren and Spyder products.

92. In the January 21, 2014 email to Dr. Lee, Dr. Gunnam also informed him that RTL code used by LSI to develop its LDPC decoder designs was based on TAMUS RTL code (which is a part of the TAMUS Copyrighted Works) and had similar structure, sequence, organization, and variables to that code. Dr. Gunnam advised Dr. Lee that this use of TAMUS RTL code could create a “copyright issue” for LSI.

93. Dr. Lee took no actions to stop LSI’s use of Texas A&M’s source code after receiving Dr. Gunnam’s January 21, 2014 email.

94. Dr. Lee received Dr. Gunnam’s January 31, 2014 e-mail.

95. On information and belief, LSI took no actions to stop LSI’s infringement of the Patents-in-Suit after receiving Dr. Gunnam’s January 31, 2014 email.

96. On information and belief, LSI, Avago, and now Broadcom Inc. have taken no efforts to cease or mitigate infringement of the Patents-in-Suit or the TAMUS Copyrighted Works.

Defendants apply the Texas A&M Technology to SSD Controller Products

97. In January 2012, LSI acquired SandForce, Inc, a maker of solid state drive (“SSD”) controller products.

98. In 2014, LSI introduced Sandforce controllers using LSI’s SHIELD technology.

99. In 2014, Mr. Kent Smith ("Mr. Smith"), an employee of LSI's Flash Components Division gave an interview (available at https://www.electronicdesign.com/memory/interview-kent-smith-addresses-error-correction-and-flash-storage-technology).

100. While being interviewed in 2014, Mr. Smith stated the following: "LSI's first implementation of LDPC codes was to correct errors in the magnet media of hard disk drives. LSI TrueStore read channels with LDPC iterative decoding technology have been shipping in high volume for HDDs since 2010. This experience and engineering expertise are leveraged in SHIELD error correction technology."

101. On information and belief, LSI incorporated features of the McLaren LDPC decoder design that are derived from, and covered by, the TAMUS Patents-in-Suit into Sandforce Controllers at least by 2013, including at least the SandForce SF3700 flash controller family and other SandForce controllers with SHEILD technology ("the Accused SandForce Products").

102. On information and belief, LSI sold its SandForce line to Seagate in late 2014.

103. Sales of the SandForce SF3700 prior to this sale of the SandForce line to Seagate were made after LSI received notice of at least the '522 Patent and had knowledge of their infringement of it.

104. On information and belief, Broadcom Inc. acquired Densbits, Inc. in December 2015.

105. On information and belief, Densbits designs and manufactures SSD controller products.

106. On information and belief, following Broadcom Inc.'s acquisition of Densbits, Broadcom Inc. assigned several individuals associated with the development of LSI's TrueStore products to work on improving the SSD controller technology purchased from Densbits.

107. On information and belief, Defendants and/or the Broadcom Predecessor Entities have incorporated features of the McLaren LDPC decoder design that are covered by the TAMUS Patents-in-Suit into Densbits' SSD controllers (the "Accused Densbits Products") and sold them to customers.

Defendants apply the Texas A&M Technology to Wi-Fi Products

108. Andrew J. Blanksby holds the title of Distinguished Engineer at Broadcom Inc., and his LinkedIn page states that he "lead[s] development of Low-Density Parity-Check (LDPC) technology for WLAN used in all major smart phones, tablets, and access points by companies such as Apple, Samsung, and LG."

109. In litigation between the California Institute of Technology and Broadcom concerning Broadcom's infringement of other LDPC technology, Dr. Blanksby stated that he has been employed by Broadcom since 2005 and that he leads the development of the LDPC technology used in Broadcom's products. *See California Institute of Technology v. Broadcom Limited et al.*, No. 2:16-cv-03714, D.I. 707-3 (Declaration of Dr. Andrew Blanksby), filed October 1, 2018, at paragraph 4. In that Declaration, Dr. Blanskby also noted that he is the named inventor on multiple LDPC patents and that at least some of his LDPC patents relate to Broadcom's products. *See id* at paragraph 5 ("As a lead developer of LDPC technologies for Broadcom, I have become familiar with patents and patent claims. I am a named inventor on more than twenty issued United States patents, the majority of which relate to LDPC encoder and

decoder technology, and it is within my normal responsibility to understand how such patents may (or may not) relate to Broadcom's products.").

110. Alvin L. Lin holds the title of Design Engineer at Broadcom and has been employed by Broadcom since 2006. Public information from the aforementioned *California Technical Institute v. Broadcom* litigation notes that Mr. Lin was also involved in the design of Broadcom products that use LDPC technology.

111. Andrew Blanksby and Alvin Lin are the named co-named inventors on multiple patents that are directed towards LDPC technology and originally assigned to Broadcom Corporation, one of the Broadcom Predecessor Entities. These patents issued from applications filed while both named co-inventors worked at Broadcom.

112. Blanksby and Lin are named as co-inventors on United States Patent No. 8,341,488, entitled "Accumulating LDPC (Low Density Parity Check) Decoder" ("the '488 patent"), which issued to Broadcom Corp. on December 25, 2012. The '488 patent claims priority to two provisional applications, provisional application No. 61/086,081, filed on August 4, 2008 ("the '081 application") and provisional application No. 61/086,097, filed on August 4, 2008 ("the '097 application"), while both named co-inventors were employed at Broadcom.

113. The '488 patent describes an LDPC decoder architecture that would, if operated, practice the inventions described in at least Claim 18 of the '140 Patent.

114. Blanksby and Lin are also co-inventors on United States Patent No. 8,341,489, entitled "Permuted Accelerated LDPC (Low Density Parity Check) Decoder" ("the '489 patent"), which also issued to Broadcom Corp. on December 25, 2012. The '489 patent, like the '488 patent, claims priority to the '081 application and the '097 application.

115. The ’489 patent describes an LDPC decoder architecture that would, if operated, practice the inventions described in at least Claim 85 of the ’522 Patent and Claim 17 of the ’250 Patent.

116. Broadcom boasts that it incorporates its patented technology into its products. *See, e.g.*, https://investors.broadcom.com/static-files/f81d3fbb-755c-44a7-ab4d-8b5fe16633fb, exemplary 2019 Broadcom From 10-K, at page 11 (“We focus our patent application program to a greater extent on those inventions and improvements that we believe are likely to be incorporated into our products, as contrasted with more basic research”).

117. Wi-Fi IEEE standards 802.11ac and 802.11ad support LDPC coding and decoding, and Wi-Fi chipsets sold by Broadcom must support LDPC decoding.

118. Broadcom advertises Wi-Fi products, like the exemplary BCM4350 “5G WiFi 802.11ac Client” as both compliant with IEEE Wi-Fi standards and supporting LDPC decoding. *See, e.g.*, https://www.broadcom.com/products/wireless/wireless-lan-infrastructure/bcm4350/ (“802.11ac-compliant . . . low-density parity check codes (LDPC)”).

119. Based on Broadcom’s public representations in its 10-K filings, in the previous LDPC-related litigation with the California Institute of Technology, in its promotional literature, and upon information and belief, Broadcom chipsets that support 802.11ac, 802.11ad, 802.11ax (to include Wi-Fi6 and 6e) and incorporate LDPC decoder designs, including the exemplary BCM4350 and all other 802.11ac- 802.11ad, 802.11ax-compliant, Wi-Fi6, or WiFi6E compliant Broadcom products that have an LDPC decoder (hereinafter the “Accused Wi-Fi Products”), incorporate designs described in the ’488 patent and the ’489 patent, and therefore infringe at least Claim 85 of the ’522 Patent, Claim 17 of the ’250 Patent, and Claim 18 of the ’140 Patent. Accused Wi-Fi Products include but are not limited to BCM6710, BCM6755, BCM47622,

BCM6752, BCM6750, BCM43684, BCM43694, BCM47452, BCM43525, BCM4366, BCM4350, BCM43162, BCM61755, BCM4335, BCM43460, BCM43526, BCM4360, BCM4389, BCM43456, BCM4375, BCM43516, BCM43556, BCM43558, BCM43566, BCM43569, BCM43462, BCM43465, BCM4352, BCM43520, BCM4356, BCM43567, BCM43570, BCM4358, BCM43598, BCM43602, BCM4365E, BCM4366E, BCM20130, BCm6705, BCm43692, BCm43693, BCM43698, BCM43751, BCM43752, BCM4378, BCM4391, BCM43353, BCM4339, BCM4345, BCM43455, BCM4354, BCM43572, BCM4359, BCM4361, BCM4371, BCM4373, BCM4377, BCM47189, BCM53573, and BCM43142.

120. For the avoidance of doubt, the Accused Wi-Fi Products in this case include each of [redacted] On information and belief, each of these [redacted] are believed to use the infringing LDPC decoder technology as set forth below in this Complaint. Indeed, initial discovery provided on the roughly 60 products for which Defendants have thus far provided some of the required disclosures, indicates that [redacted]. On information and belief, the other [redacted] Defendants' WiFi products sharing these characteristics [redacted] infringe Asserted Claims in the same manner.

121. The Accused Hard Disk Controller Products, the Accused SandForce Products, the Accused Densbits Products, and the Accused Wi-Fi Products are collectively referred to as the "Accused Products."

COUNT I
(Infringement under 35 U.S.C. § 271 of U.S. Patent No. 8,418,023)

122. Plaintiff repeats and re-alleges the paragraphs above as if fully set forth herein.

123. The '023 Patent is valid, enforceable, and was duly issued on August 9, 2013 in full compliance with Title 35 of the United States Code.

124. On information and belief, in violation of 35 U.S.C. § 271, Defendants and/or the Broadcom Predecessor Entities have infringed, contributed to the infringement of, and/or induced others to infringe the '023 Patent, either literally or under the doctrine of equivalents, by, among other things, making, using, offering for sale, selling, selling infringing products abroad with knowledge and intent that the infringing products be imported into the United States by others, and/or importing into the United States unlicensed systems and/or products in a manner that infringes Claims 1-30 of the '023 Patent.

125. On information and belief, Defendants and/or the Broadcom Predecessor Entities have directly infringed the '023 Patent, for example, by making, using, selling, offering to sell, and/or importing into the United States the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products, which meet each and every limitation of at least Claim 1 of the '023 Patent, in violation of Plaintiff's patent rights and without Plaintiff's license or authority. Non-limiting examples of such infringement are provided below, based on the limited information currently available to Plaintiff.

126. Claim 1 of the '023 Patent recites as follows:

1. A low density parity check code decoder, comprising:

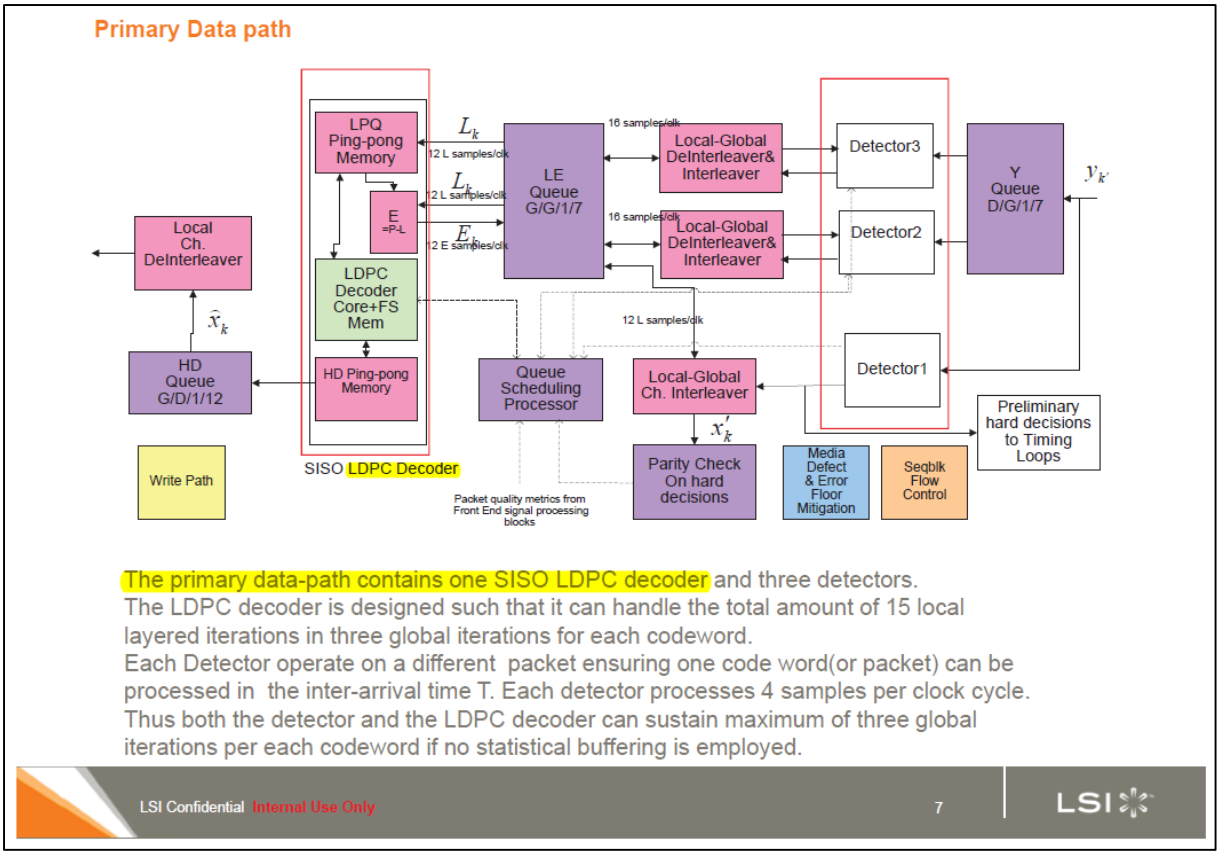
a control unit that controls decoder processing, the control unit configured to:

cause the decoder to process blocks of a low density parity check ("LDPC") matrix out of order; and

schedule computation of R messages for a first non-zero block and computation of P messages and Q messages for a second non-zero block such that R messages for the first non-zero block are generated while processing the second non-zero block based on a determination of need for the R messages for the computation of P and Q messages for the second non-zero block;

wherein the first non-zero block and the second non-zero block are in a same column of the matrix.

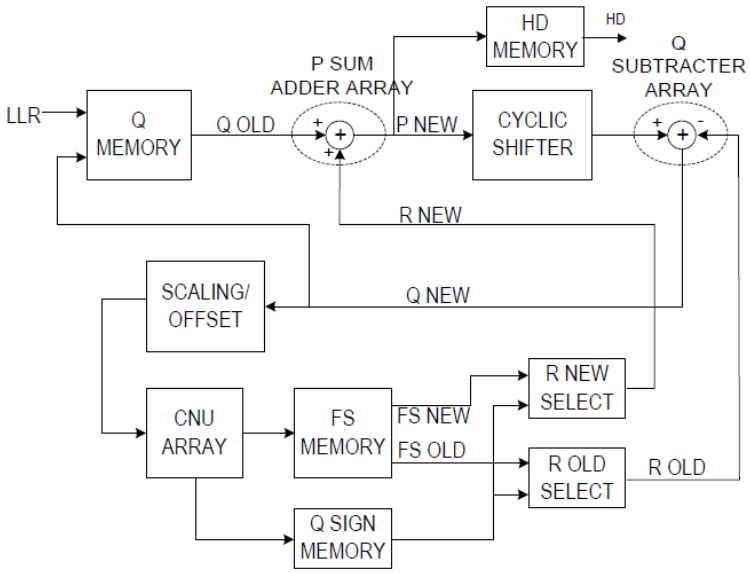
127. On information and belief, the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products satisfy each and every limitation of Claim 1 of the '023 Patent. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include a low density parity check code decoder. For example, an LSI presentation dated October 13, 2009 entitled: "Mclaren Client Server Architecture/Scheduling" (hereinafter, the "McLaren Architecture Presentation") references the LDPC decoder.



128. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include a control unit that controls decoder processing, and as set forth below, that control unit is configured to perform the actions required of the claimed control unit.

129. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products cause the decoder to process blocks of an LDPC matrix out of order. For example, an LSI presentation dated August 21, 2009 entitled: "Layered Decoder for LDPC Codes with Zero Matrices" (hereinafter, the "Layered Decoder Presentation") references out of order processing and includes many figures taken directly from the '023 Patent.

Layered Decoder, Arch 1

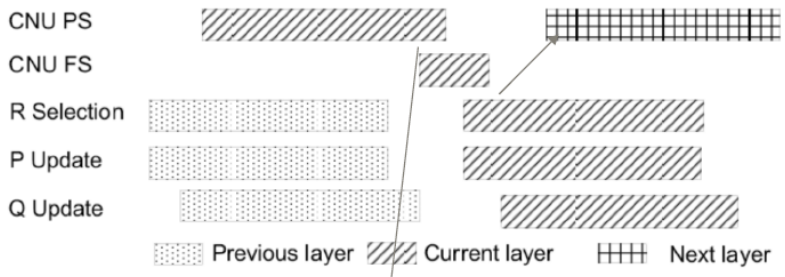


Supports out-of-order processing for PS processing

Out-of-order processing for Rnew

Layer reordering

Out-of-order processing for PS processing



The circulants in each layers can be processed out-of-order

Out-of-order layer processing for R Selection

Rate 2/3 A code:

3	0	-1	-1	2	0	-1	3	7	-1	1	1	-1	-1	-1	-1	1	0	-1	-1	-1	-1	-1	-1
-1	-1	1	-1	36	-1	-1	34	10	-1	-1	18	2	-1	3	0	-1	0	0	-1	-1	-1	-1	-1
-1	-1	12	2	-1	15	-1	40	-1	3	-1	15	-1	2	13	-1	-1	-1	0	0	-1	-1	-1	-1
-1	-1	19	24	-1	3	0	-1	6	-1	17	-1	-1	-1	8	39	-1	-1	-1	0	0	-1	-1	-1
20	-1	6	-1	-1	10	29	-1	-1	28	-1	14	-1	38	-1	-1	0	-1	-1	-1	0	0	-1	-1
-1	-1	10	-1	28	20	-1	-1	8	-1	36	-1	9	-1	21	45	-1	-1	-1	-1	-1	0	0	-1
35	25	-1	37	-1	21	-1	-1	5	-1	-1	0	-1	4	20	-1	-1	-1	-1	-1	-1	-1	0	0
-1	6	6	-1	-1	-1	4	-1	14	30	-1	3	36	-1	14	-1	1	-1	-1	-1	-1	-1	-1	0

PS processing R selection

R selection is out-of-order so that it can feed the data required for the PS processing of the second layer.

So here we decoupled the execution of R new messages with the execution of CNU processing.

Here we execute the instruction/computation at precise moment when the result is needed!!!

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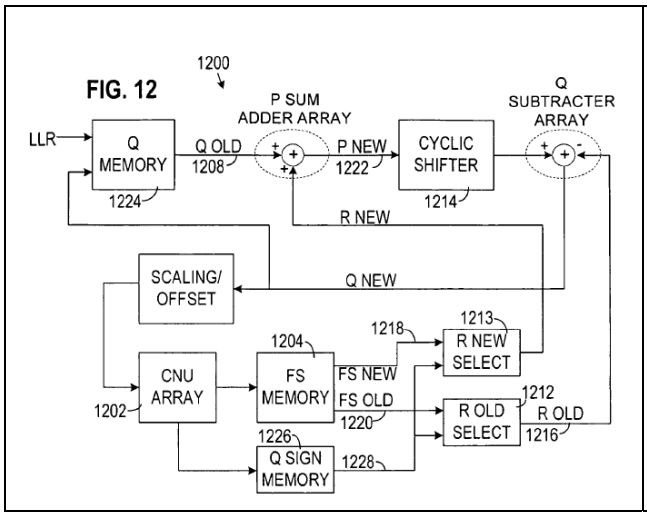
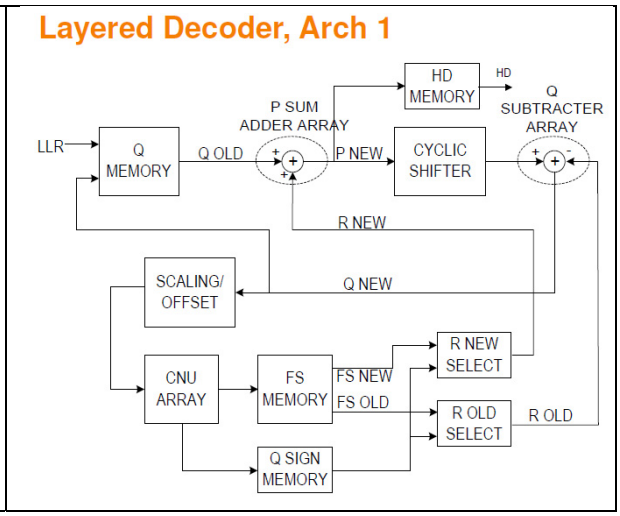
130. The layered decoder architecture of the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products is identical in relevant respects to what is set forth in the '023 Patent.

'023 Patent at FIG. 12

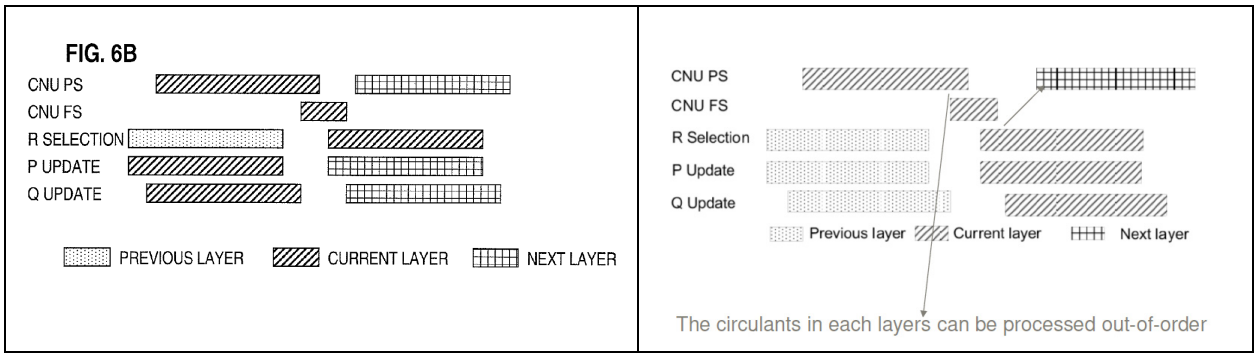


Layered Decoder Presentation at 4



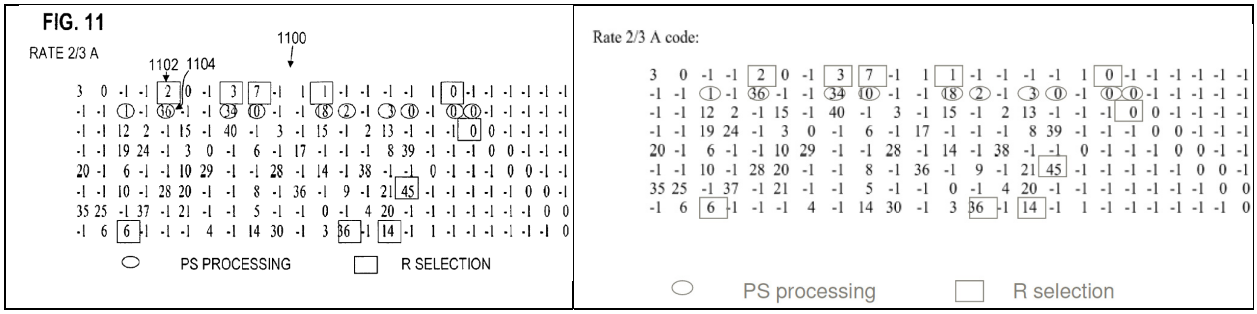
131. The pipeline architecture of the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products is similar to what is set forth in the ’023 Patent.

’023 Patent at FIG. 6B | **Layered Decoder Presentation at 8**



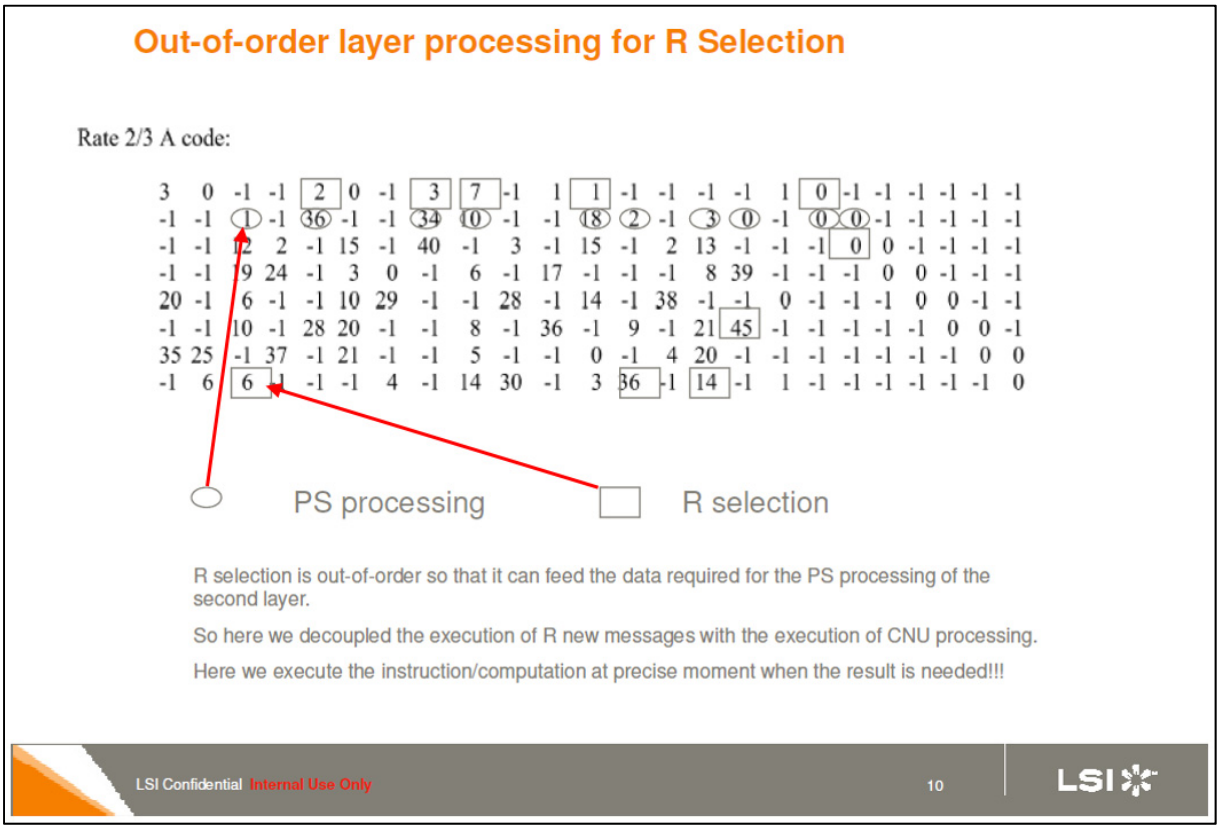
132. The exemplary Rate 2/3 A code of the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products is identical to what is set forth in the ’023 Patent.

’023 Patent at FIG. 11 | **Layered Decoder Presentation at 10**

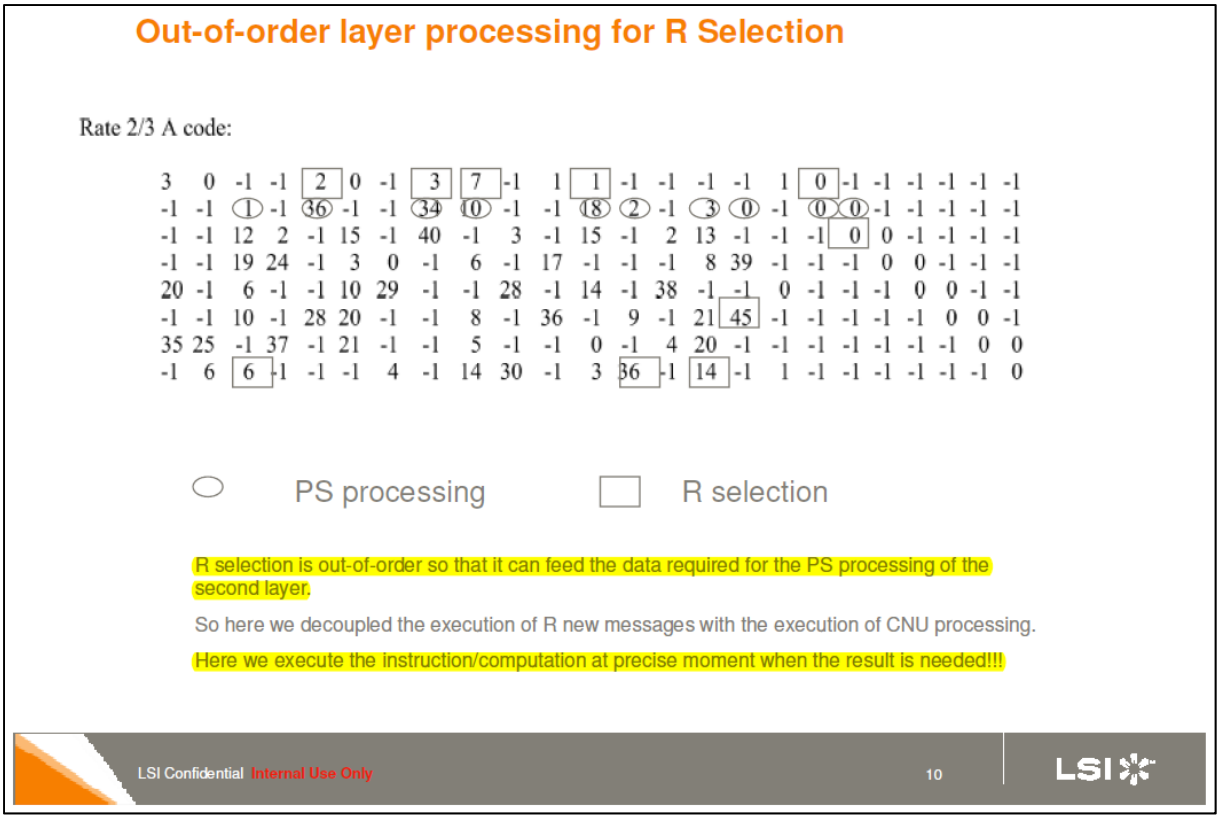


133. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products schedule computation of R messages for a first non-zero block and computation of P messages and Q messages for a second non-zero block. For example, the Layered Decoder Presentation discloses that the computation of the R messages (“R

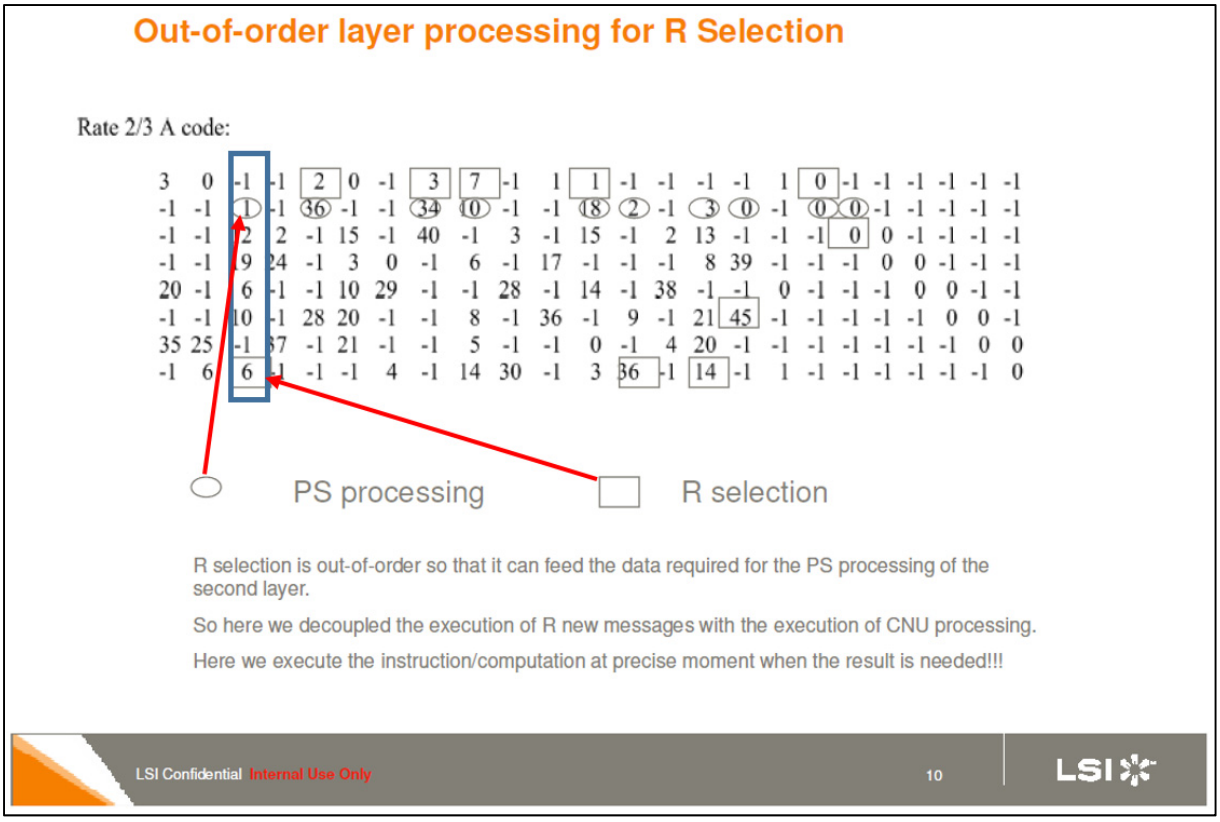
SELECTION") are for a first non-zero block and the computation of the P messages and the Q messages are for a second non-zero block.



134. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products schedule computations such that R messages for the first non-zero block are generated while processing the second non-zero block, based on a determination of need for the R messages for the computation of P and Q messages for the second non-zero block. For example, the Layered Decoder Presentation discloses that the R selection is out-of-order so that it can feed the data required for the P and Q message computation of the second layer.



135. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include wherein the first non-zero block and the second non-zero block are in a same column of the matrix. For example, the Layered Decoder Presentation discloses a matrix wherein the first non-zero block and the second non-zero block are in a same column.



136. Claim 18 of the '023 Patent recites as follows:

> 18. A method for decoding a low density parity check code, comprising:
> processing blocks of a low density parity check ("LDPC") matrix out of order; and
> scheduling computation of R messages for a first non-zero block and computation of P messages and Q messages for a second non-zero block such that R messages for the first non-zero block are generated while processing the second non-zero block based on a determination of need for the R messages for the computation of P and Q messages for the second non-zero block;
> wherein the first non-zero block and the second non-zero block are in a same column of the matrix.

137. On information and belief, the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products satisfy each and every limitation of Claim 18. The Accused Hard Disk Controller Products, the Accused SandForce

Products, and the Accused Densbits Products decode a low density parity check code. *See* ¶¶ 112, 113, *supra*.

138. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products process blocks of a LDPC matrix out of order. *See* ¶¶ 112, 115, *supra*.

139. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products schedule computation of R messages for a first non-zero block and computation of P messages and Q messages for a second non-zero block. *See* ¶¶ 112, 119, *supra*.

140. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products schedule computations such that R messages for the first non-zero block are generated while processing the second non-zero block based on a determination of need for the R messages for the computation of P and Q messages for the second non-zero block. *See* ¶¶ 112, 119-20, *supra*.

141. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products schedule computations wherein the first non-zero block and the second non-zero block are in a same column of the matrix. *See* ¶¶ 112, 121, *supra*.

142. In view of the foregoing, the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products directly infringe at least Claims 1-30 of the ’023 Patent at least through Defendants’ and/or the Broadcom Predecessor Entities’ sale, offer for sale, importation, use, and/or testing of the Accused Products.

143. On information and belief, Defendants and/or the Broadcom Predecessor Entities have taken active steps to induce infringement by others of at least Claims 1-30 of the ’023

Patent in violation of 35 U.S.C. §271(b), including, for example, by (a) inducing manufacturers to practice the claimed inventions when testing the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products, and (b) inducing end users to practice the claimed inventions when using the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products. Such active steps include, but are not limited to, selling Accused Hard Disk Controller Products, Accused SandForce Products, and Accused Densbits Products with the knowledge and intent that the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products will be operated by such manufacturers and their customers in accordance with the claimed inventions, as set forth in the Section "EXAMPLES OF DIRECT AND INDIRECT INFRINGEMENT" below.

144. On information and belief, Defendants and/or the Broadcom Predecessor Entities have known or should have known that such activities induce others to directly infringe one or more of at least Claims 1-30 of the '023 Patent. For example, Defendants and/or the Broadcom Predecessor Entities should have known that their actions induced others to directly infringe as of the date it became aware of the issuance of the '023 Patent on or about April 9, 2013, and in any event no later than the date it was advised of the issuance of the '023 Patent by Dr. Gunnam on January 31, 2014. Defendants and/or the Broadcom Predecessor Entities were further informed that the technology in the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products infringed the '023 Patent, and Defendants and/or the Broadcom Predecessor Entities have knowingly and purposefully continued to exploit the patented technology, despite knowing that it was covered by the '023

Patent, as set forth in the Section "EXAMPLES OF DIRECT AND INDIRECT INFRINGEMENT" below.

145. On information and belief, Defendants and/or the Broadcom Predecessor Entities have contributed to the infringement of at least Claims 1-30 of the '023 Patent by others, including consumer/end-user use of the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products, in violation of 35 U.S.C. § 271(c). Acts by Defendants and/or the Broadcom Predecessor Entities that have contributed to the infringement of others include, but are not limited to, the sale, offer for sale, and/or import by Defendants of the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products. Such Accused Hard Disk Controller Products, Accused SandForce Products, and Accused Densbits Products are especially made for or adapted for use to infringe, and are not a staple article of commerce and are not suitable for substantial non-infringing use. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products are apparatuses for use in practicing the inventions patented in Claims 1-30 of the '023 Patent, and are at least a material part of those claimed inventions, as set forth in the Section "EXAMPLES OF DIRECT AND INDIRECT INFRINGEMENT" below.

146. As also described above, Defendants and/or the Broadcom Predecessor Entities have, on information and belief, been on notice of the '023 Patent since it issued on April 9, 2013 and in any event were on notice as of no later than January 31, 2014.

147. In addition, Defendants and/or the Broadcom Predecessor Entities have been on notice since the filing and/or service of Plaintiff's original Complaint. (*See* D.I. 1, 5) Defendants have further been aware that use of the Accused Hard Disk Controller Products, the Accused

SandForce Products, and the Accused Densbits Products necessarily practice the inventions in Claims 1-30 of the ’023 Patent.

148. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products are especially made for or adapted for use to infringe, and are not a staple article of commerce, and are not suitable for substantial non-infringing use. By way of example, the use of the LDPC decoders included in the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products is necessary to use the accused products for their intended purpose (decoding data from a hard disk drive, solid state drive, or wireless digital transmission), and the LDPC decoders necessarily practice the claimed inventions when they decode data. Accordingly, the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products do not have a substantial use that does not entail practicing the claimed inventions. On information and belief, the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products cannot be used but to infringe the ’023 Patent.

149. Despite Defendants’ and/or the Broadcom Predecessor Entities’ knowledge and notice of the ’023 Patent and their ongoing infringement, Defendants and/or the Broadcom Predecessor Entities have continued to manufacture, use, sell, offer for sale, and/or import the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products in a manner that willfully infringes the ’023 Patent, and on information and belief, continue to sell and/or offer for sale the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products to the United States market. On information and belief, nearly all of Dr. Gunnam’s work, *inter alia*, at LSI was centered on the TAMUS’ ’320 provisional application. On information and belief, LSI recognized its

competitive disadvantage from not having acquired the rights to the Patents-in-Suit for itself, and embarked on a course of action where it filed and prosecuted numerous patents, based on Dr. Gunnam's work concerning the TAMUS '320 provisional application.

See https://www.google.com/search?tbm=pts&ei=lR4QXM-pHrm40PEP_s6YwAE&q=Ser.+No.+12%2F113%2C729+filed+on+May+1%2C+2008&oq=Ser.+No.+12%2F113%2C729+filed+on+May+1%2C+2008&gs_l=psy-ab.3...95601.99862.0.100208.3.3.0.0.0.0.128.258.2j1.3.0....0...1c.1.64.psy-ab..0.0.0....0.OmH6jRmYHJo; *see also* https://www.google.com/search?tbm=pts&ei=jB4QXODdHdC60PEP0qC4-A4&q=Ser.+No.+12%2F113%2C755+filed+on+May+1%2C+2008&oq=Ser.+No.+12%2F113%2C755+filed+on+May+1%2C+2008&gs_l=psy-ab.3...7529.7728.0.8111.2.2.0.0.0.0.81.149.2.2.0....0...1c.1.64.psy-ab..0.0.0....0.UBEXLdczJgA. On information and belief, LSI filed and prosecuted these patents despite Dr. Gunnam's repeated requests to LSI management for LSI to obtain a license for the TAMUS intellectual property. Defendants' and/or the Broadcom Predecessor Entities' infringement of the '023 Patent has thus been willful, as set forth above. Defendants and/or the Broadcom Predecessor Entities lacked a justifiable belief that they do not infringe the '023 Patent, or that the '023 Patent is invalid or unenforceable, and have acted recklessly in their infringing activity, justifying an increase in the damages to be awarded to Plaintiff up to three times the amount found or assessed, in accordance with 35 U.S.C. § 284.

150. On information and belief, Defendants and/or the Broadcom Predecessor Entities have had actual or constructive knowledge of the '023 Patent since at least April 9, 2013, and in any event no later than January 31, 2014.

151. Defendants and/or the Broadcom Predecessor Entities further have had knowledge of the '023 Patent at least as early as the filing and/or service of the original Complaint. (*See* D.I. 1, 5) Defendants and/or the Broadcom Predecessor Entities know or should know as of the date of filing and/or service of Plaintiff's original Complaint that their actions induced others to directly infringe the '023 Patent and contributed to infringement of the '023 Patent. (*See id.*)

152. This case is rendered an exceptional case at least in light of Defendants' and/or the Broadcom Predecessor Entities' willful infringement of the '023 Patent, justifying an award to Plaintiff of its reasonable attorney fees, in accordance with 35 U.S.C. § 285.

153. Plaintiff has no adequate remedy at law for Defendants' and/or the Broadcom Predecessor Entities' acts of infringement. As a direct and proximate result of Defendants' and/or the Broadcom Predecessor Entities' acts of infringement, Plaintiff has suffered and continues to suffer damages and irreparable harm. Unless Defendants' and/or the Broadcom Predecessor Entities' acts of infringement are enjoined by this Court, Plaintiff will continue to be damaged and irreparably harmed.

154. Defendants' and/or the Broadcom Predecessor Entities' infringement of the '023 Patent have damaged and continue to damage Plaintiff in an amount yet to be determined, of at least a reasonable royalty and/or lost profits that Plaintiff would have made but for Defendants' and/or the Broadcom Predecessor Entities' infringement acts.

COUNT II
(Infringement under 35 U.S.C. § 271 of U.S. Patent No. 8,555,140)

155. Plaintiff repeats and re-alleges the paragraphs above as if fully set forth herein.

156. The '140 Patent is valid, enforceable, and was duly issued on October 8, 2013 in full compliance with Title 35 of the United States Code.

157. On information and belief, in violation of 35 U.S.C. § 271, Defendants and/or the Broadcom Predecessor Entities have infringed, contributed to the infringement of, and/or induced others to infringe the '140 Patent, either literally or under the doctrine of equivalents, by, among other things, making, using, offering for sale, selling, selling infringing products abroad with knowledge and intent that the infringing products be imported into the United States by others, and/or importing into the United States unlicensed systems and/or products in a manner that infringes at least Claims 7-12 and 18-22 of the '140 Patent.

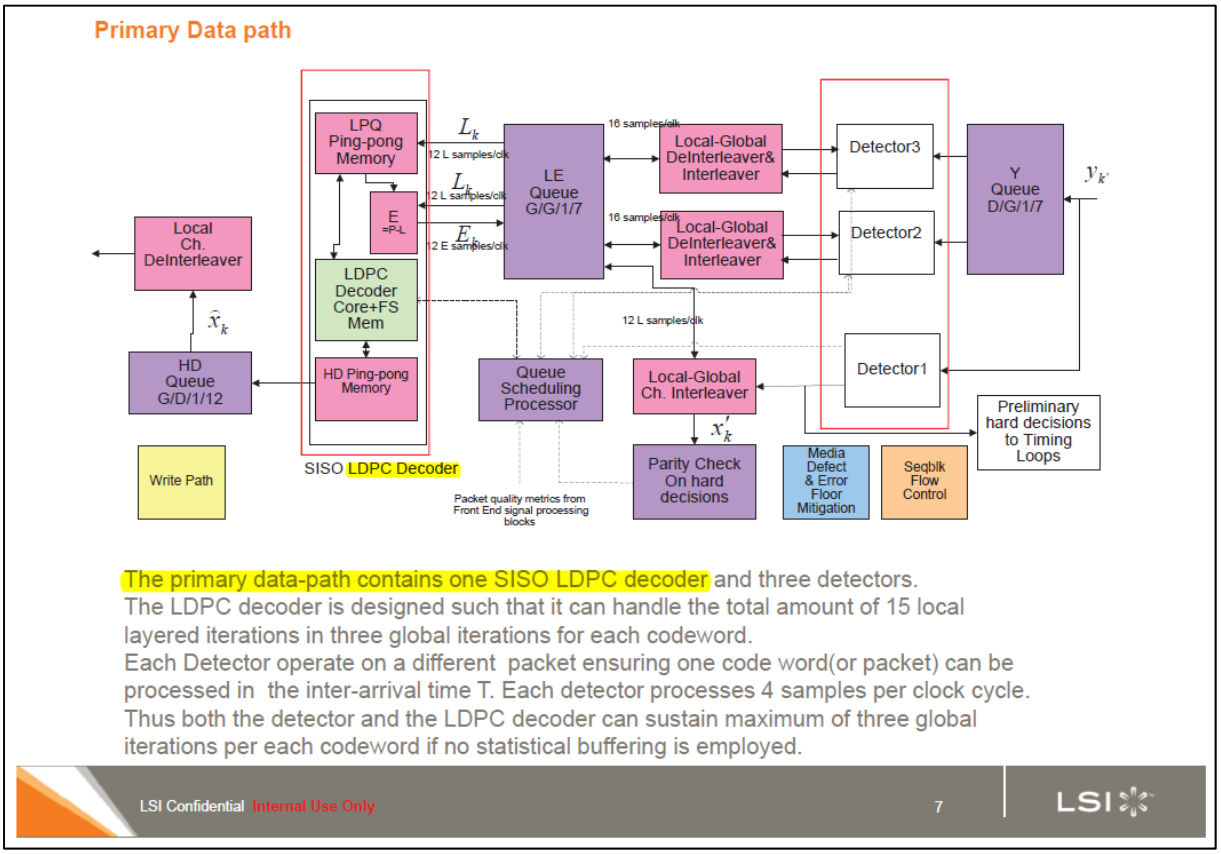
158. On information and belief, Defendants and/or the Broadcom Predecessor Entities have directly infringed the '140 Patent, for example, by making, using, selling, offering to sell, and/or importing into the United States the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products, which meet each and every limitation of at least Claim 7 of the '140 Patent, in violation of Plaintiff's patent rights and without Plaintiff's license or authority. Non-limiting examples of such infringement are provided below, based on the limited information currently available to Plaintiff.

159. Claim 7 of the '140 Patent recites as follows:

> 7. A method for decoding a low density parity check (LDPC) code, comprising:
> processing blocks of an LDPC matrix in a first sequence; computing R messages for the blocks in a second sequence that is different from the first sequence; specifying, via the first sequence, a first set of blocks of a given layer to be processed at a given time and a second set of blocks of the given layer to be processed after the first set of

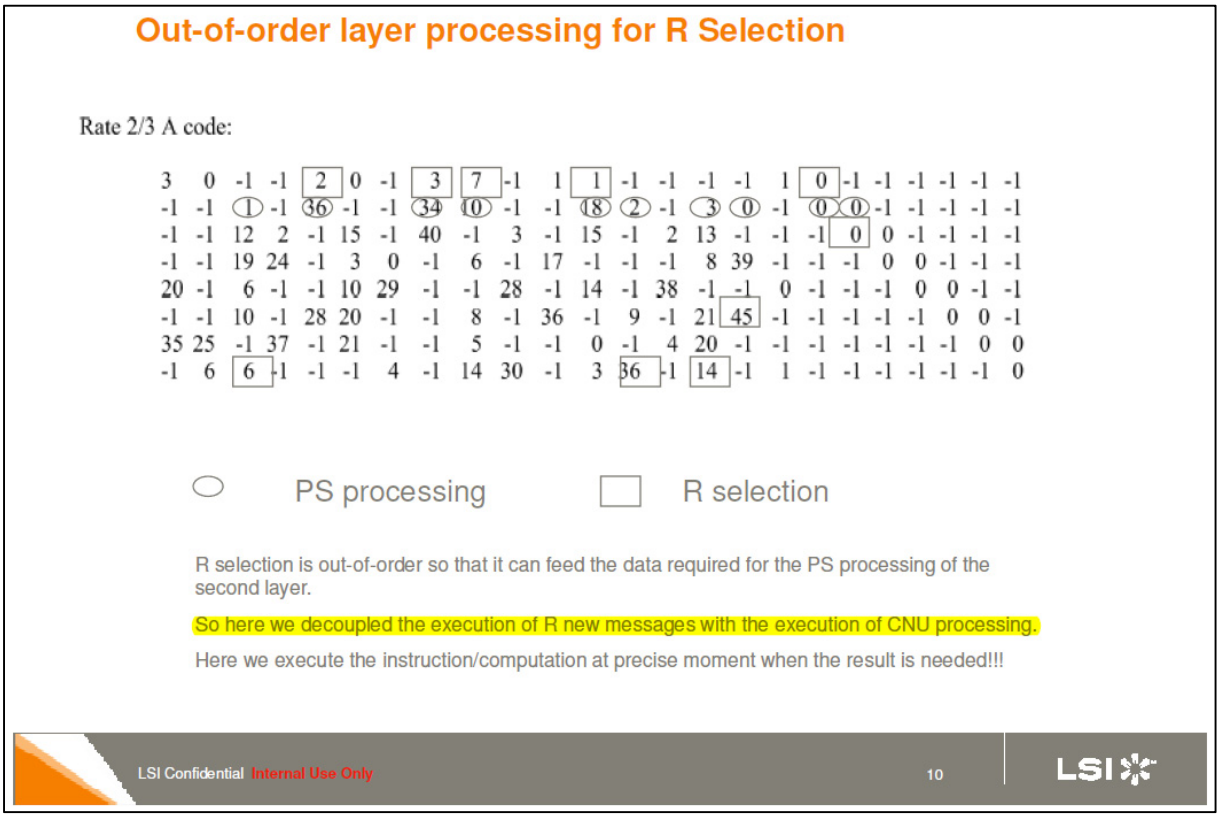
blocks; wherein the first set specifies only blocks of the given layer that are not dependent on a result of a previously processed layer and the second set specifies blocks of the given layer that are dependent on a result of the previously processed layer.

160. On information and belief, the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products satisfy each and every limitation of Claim 7. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products decode an LDPC code. For example, the McLaren Architecture Presentation references the LDPC decoder.



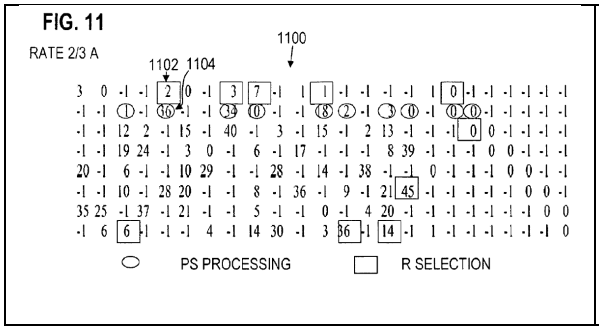
161. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products process blocks of an LDPC matrix in a first sequence and compute R messages for the blocks in a second sequence that is different from the first sequence. For example, the Layered Decoder Presentation indicates that the Accused Products process

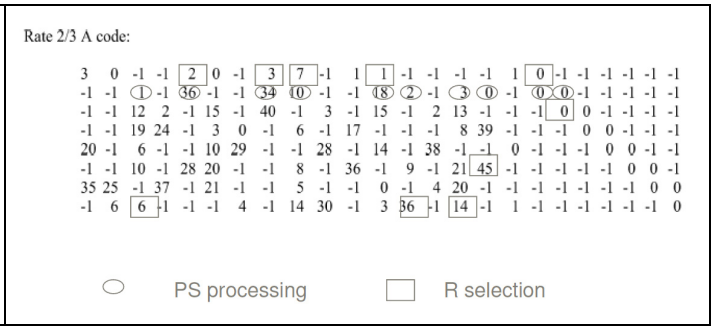
blocks of an LDPC matrix in a first sequence and compute R messages for the blocks in a different sequence.



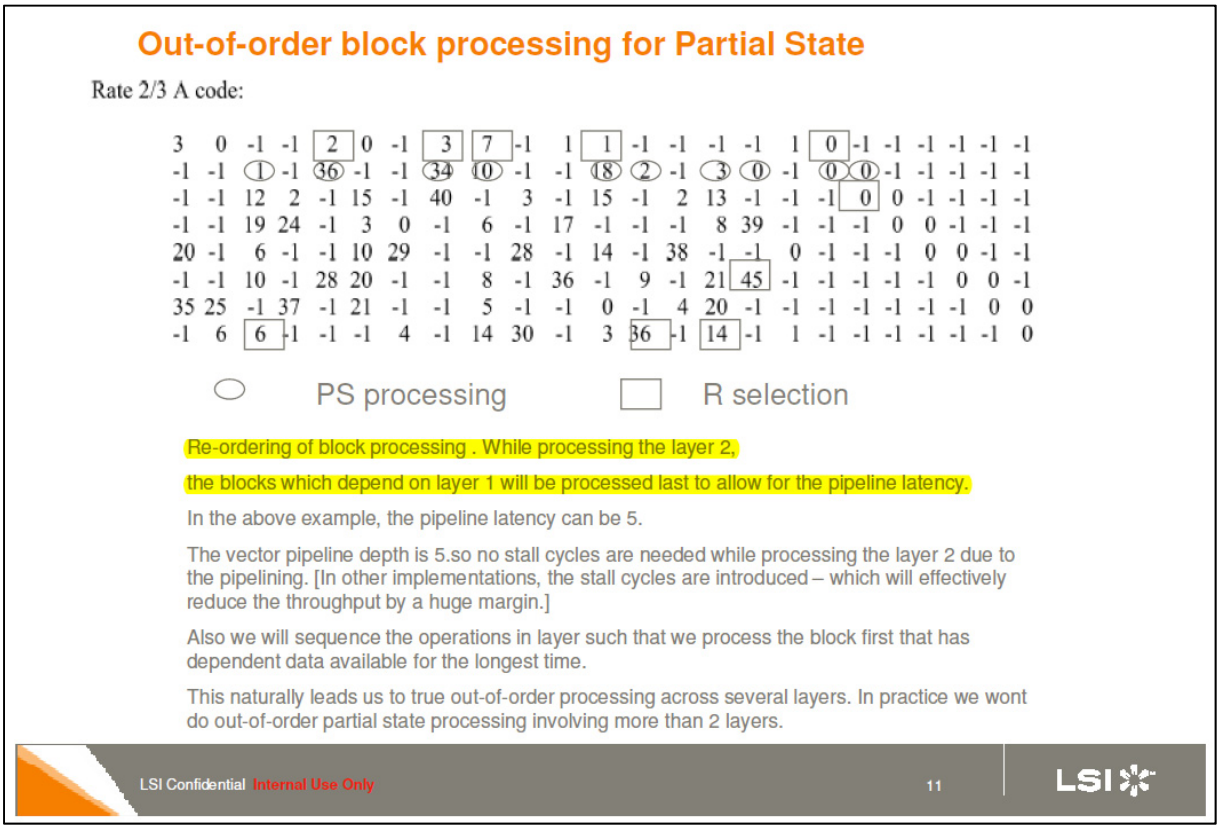
162. The exemplary Rate 2/3 A code of the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products is identical to what is set forth in the '140 Patent.

'140 Patent at FIG. 11 | **Layered Decoder Presentation at 10**





163. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products specify, via the first sequence, a first set of blocks of a given layer to be processed at a given time and a second set of blocks of the given layer to be processed after the first set of blocks, wherein the first set specifies only blocks of the given layer that are not dependent on a result of a previously processed layer and the second set specifies blocks of the given layer that are dependent on a result of the previously processed layer. For example, the Layered Decoder Presentation discloses that while processing the second layer, the blocks which depend on layer 1 will be processed last.



Out-of-order block processing for Partial State

Rate 2/3 A code:

3	0	-1	-1	2	0	-1	3	7	-1	1	1	-1	-1	-1	-1	1	0	-1	-1	-1	-1	-1	-1
-1	-1	1	-1	36	-1	-1	34	10	-1	-1	18	2	-1	3	0	-1	0	0	-1	-1	-1	-1	-1
-1	-1	12	2	-1	15	-1	40	-1	3	-1	15	-1	2	13	-1	-1	-1	0	0	-1	-1	-1	-1
-1	-1	19	24	-1	3	0	-1	6	-1	17	-1	-1	-1	8	39	-1	-1	-1	0	0	-1	-1	-1
20	-1	6	-1	-1	10	29	-1	-1	28	-1	14	-1	38	-1	-1	0	-1	-1	-1	0	0	-1	-1
-1	-1	10	-1	28	20	-1	-1	8	-1	36	-1	9	-1	21	45	-1	-1	-1	-1	-1	0	0	-1
35	25	-1	37	-1	21	-1	-1	5	-1	-1	0	-1	4	20	-1	-1	-1	-1	-1	-1	-1	0	0
-1	6	6	-1	-1	-1	4	-1	14	30	-1	3	36	-1	14	-1	1	-1	-1	-1	-1	-1	-1	0

PS processing R selection

Re-ordering of block processing . While processing the layer 2,

the blocks which depend on layer 1 will be processed last to allow for the pipeline latency.

In the above example, the pipeline latency can be 5.

The vector pipeline depth is 5.so no stall cycles are needed while processing the layer 2 due to the pipelining. [In other implementations, the stall cycles are introduced – which will effectively reduce the throughput by a huge margin.]

Also we will sequence the operations in layer such that we process the block first that has dependent data available for the longest time.

This naturally leads us to true out-of-order processing across several layers. In practice we wont do out-of-order partial state processing involving more than 2 layers.

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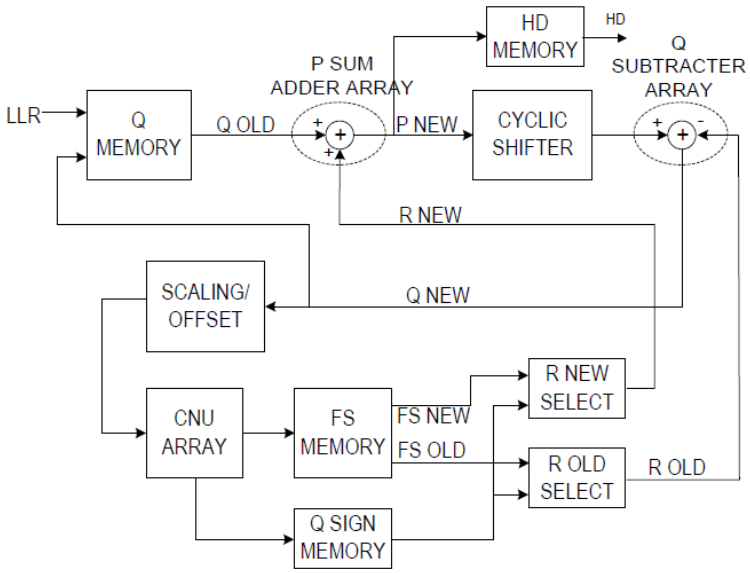
164. Claim 18 of the '140 Patent recites as follows:

> 18. A method for decoding a low density parity check (LDPC) code, comprising:
> processing blocks of an LDPC matrix out of order; and
> processing each block of the matrix in processing substeps comprising:
> an R new update substep that produces an R new message for a block of a different layer of the matrix from a layer containing a block currently being processed;
> an R old update substep that selects an R old message for a layer of the matrix currently being processed;
> a P message substep that generates updated P messages; and
> a Q message substep that computes variable node messages (Q messages);
> permuting a P message, wherein the permuting comprises permuting the P message by the difference of the permutation of a block currently being processed and the permutation of a block previously processed; wherein the block currently being processed and the block previously processed are in a same block column.

165. On information and belief, the Accused Products satisfy each and every limitation of Claim 18. The Accused Products decode an LDPC code. For example, with respect to the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products decode an LDPC code. *See* ¶ 146, *supra*. With respect to the Accused Wi-Fi Products, the '488 patent describes "a novel LDPC decoder architecture" for decoding LDPC code.

166. The Accused Products process blocks of an LDPC matrix out of order. For example, with respect to the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products, the Layered Decoder Presentation references out of order processing and includes many figures taken directly from the '140 Patent.

Layered Decoder, Arch 1

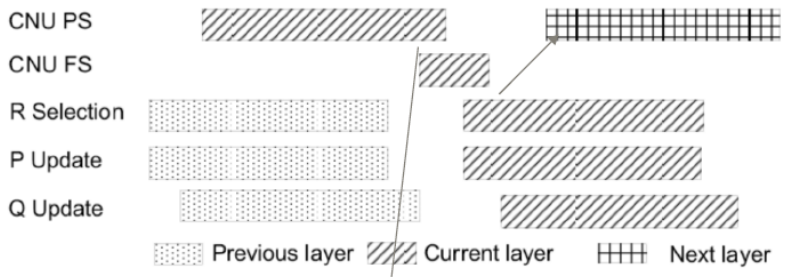


Supports out-of-order processing for PS processing

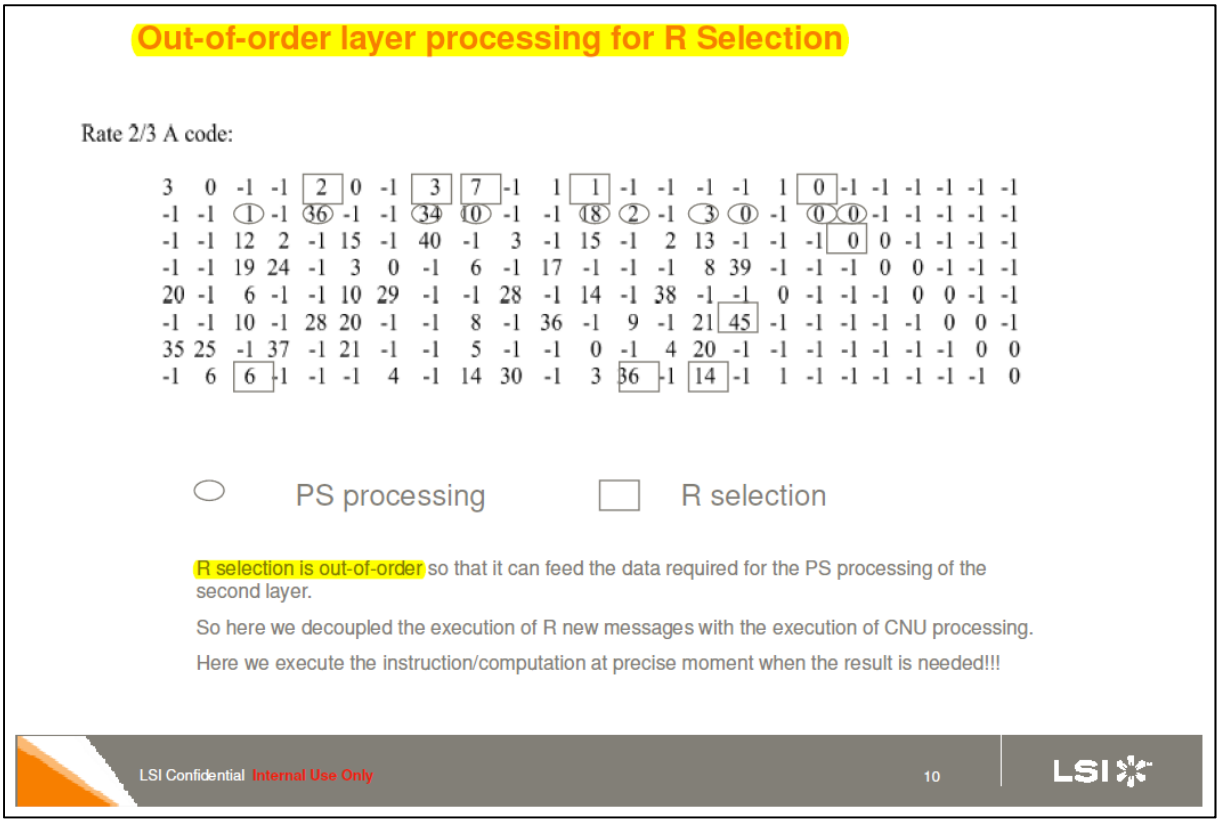
Out-of-order processing for Rnew

Layer reordering

Out-of-order processing for PS processing



The circulants in each layers can be processed out-of-order



With respect to the Accused Wi-Fi Products, they perform the LDPC decoding method described in the '488 patent in which multiple rows from different layers are processed at the same time, for example as shown in FIG. 9 (reproduced below) and the accompanying disclosure, and thus the blocks of the LDPC matrix are processed out of order.

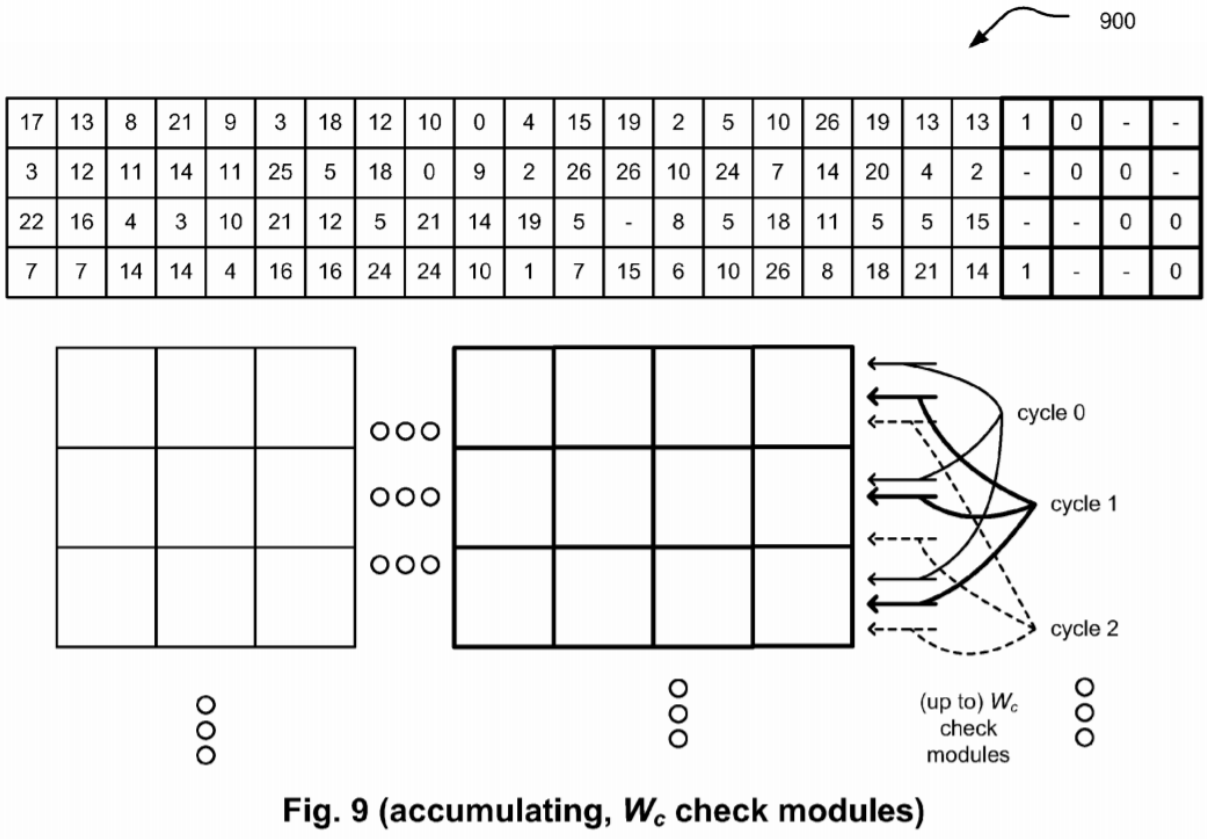
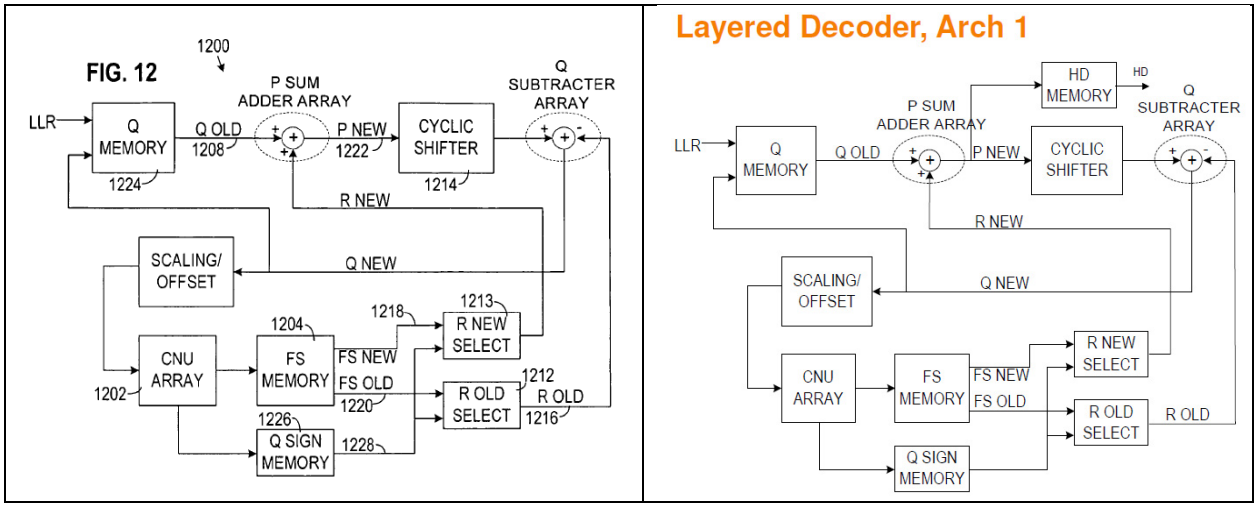


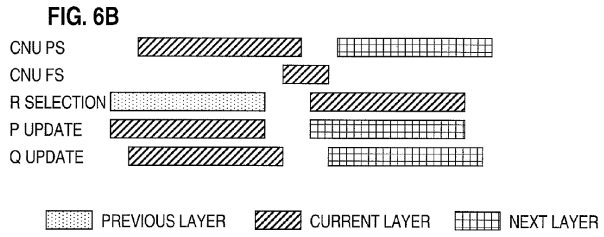
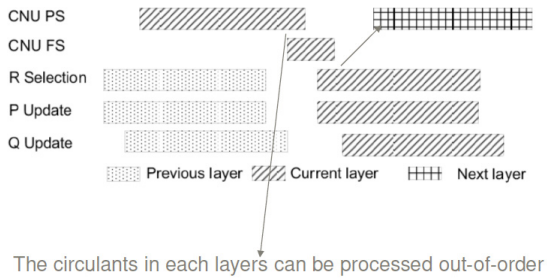
Fig. 9 (accumulating, W_c check modules)

167. The layered decoder architecture of the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products is identical to what is set forth in the '140 Patent.

'140 Patent at FIG. 12 | **Layered Decoder Presentation at 4**

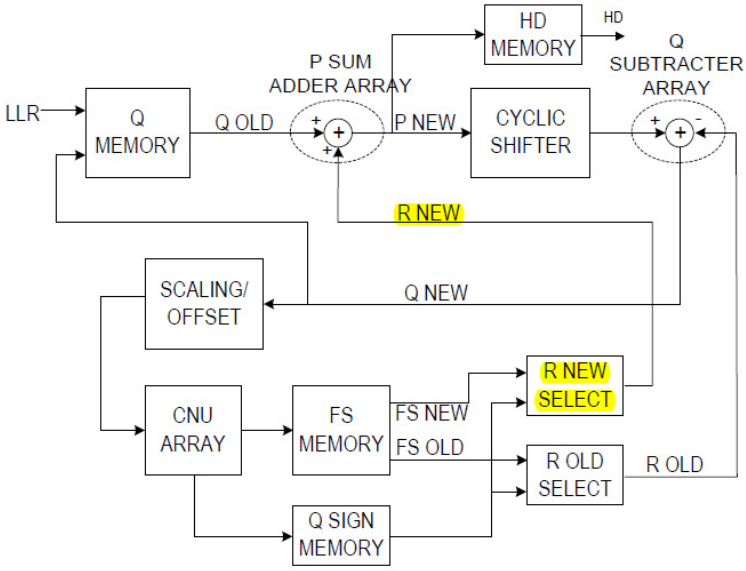


168. The pipeline architecture of the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products is similar to what is set forth in the '140 Patent.

'140 Patent at FIG. 6B	**Layered Decoder Presentation at 8**
	

169. The Accused Products process each block of the matrix in processing substeps comprising an R new update substep that produces an R new message for a block of a different layer of the matrix from a layer containing a block currently being processed. For example, with respect to the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products, the Layered Decoder Presentation discloses an R NEW SELECT unit that produces an R new message for a block of a different layer of the matrix from a layer containing a block currently being processed.

Layered Decoder, Arch 1

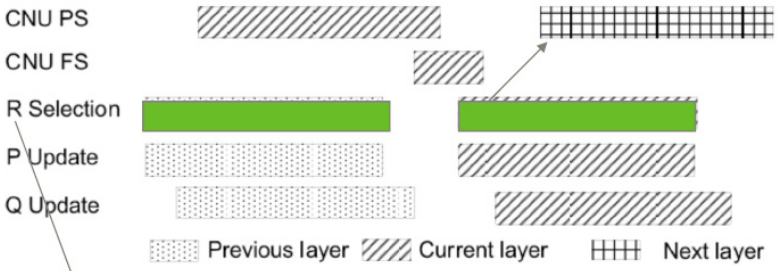


Supports out-of-order processing for PS processing

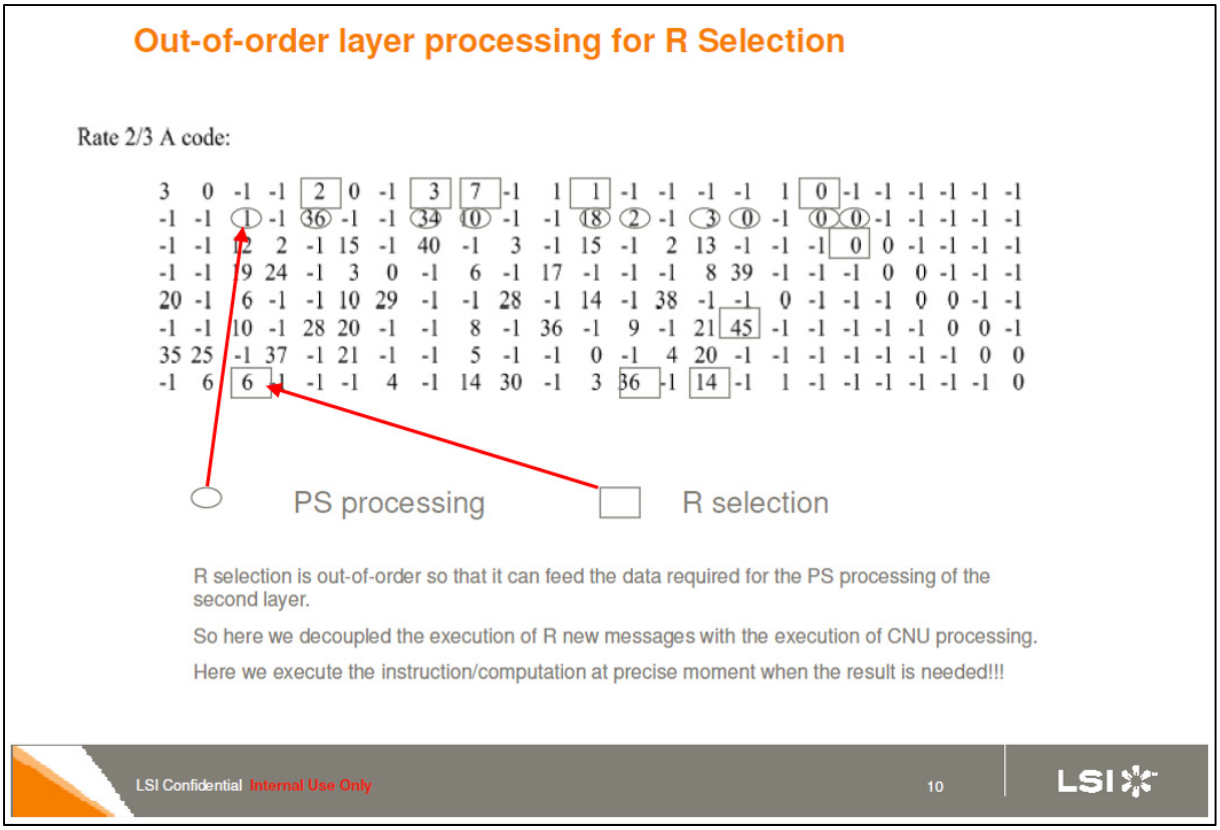
Out-of-order processing for Rnew

Layer reordering

Out-of-order processing of R_{new}



R selection for R_{new} operates out-of-order to feed the data for PS processing of next layer



With respect to the Accused Wi-Fi Products, they perform the LDPC decoding method described in the '488 patent which includes a decoding substep whereby an updated check edge message (λ) value [*i.e.,* updated R message] is produced for a block of a different layer of the matrix from a layer containing a block currently being processed, such as described, for example, in FIG. 15 (reproduced below) and the accompanying disclosure of method 1500 for performing an APP value update using first through fourth check edge messages (shown as λ1 – λ4). The Broadcom '488 patent and '489 patents use a different convention to refer to the R, P, and Q messages which are referred to in the Patents-in-Suit. In the '488 and '489 patents, the so-called check edge message (λ) value corresponds to R messages, the APP (or gamma(γ)) value corresponds to P messages, and the difference of (γ–λ) (i.e., a difference between a check edge message (λ) and an APP (or gamma(γ)) value) corresponds to Q messages.

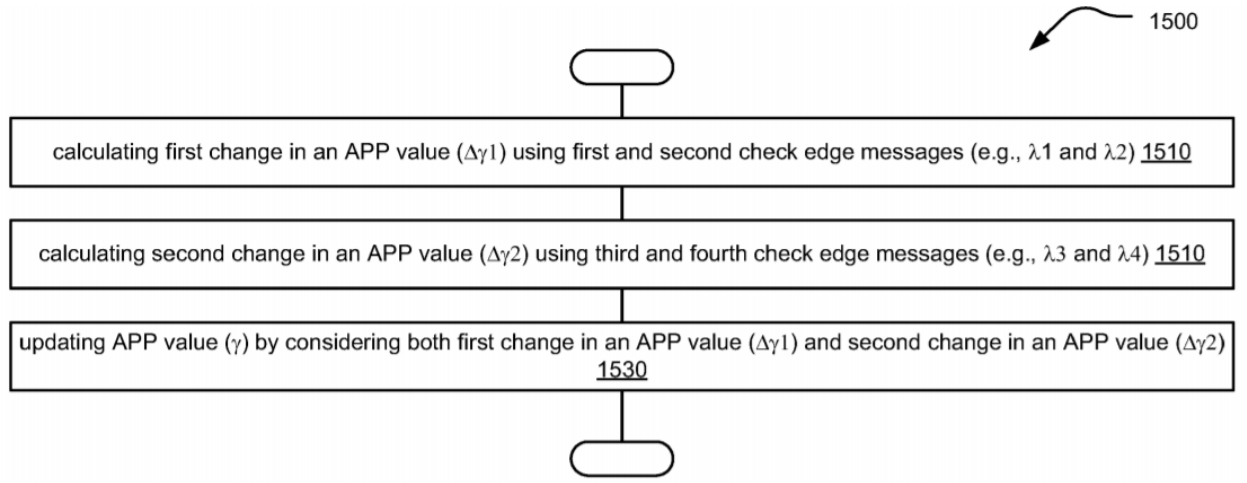
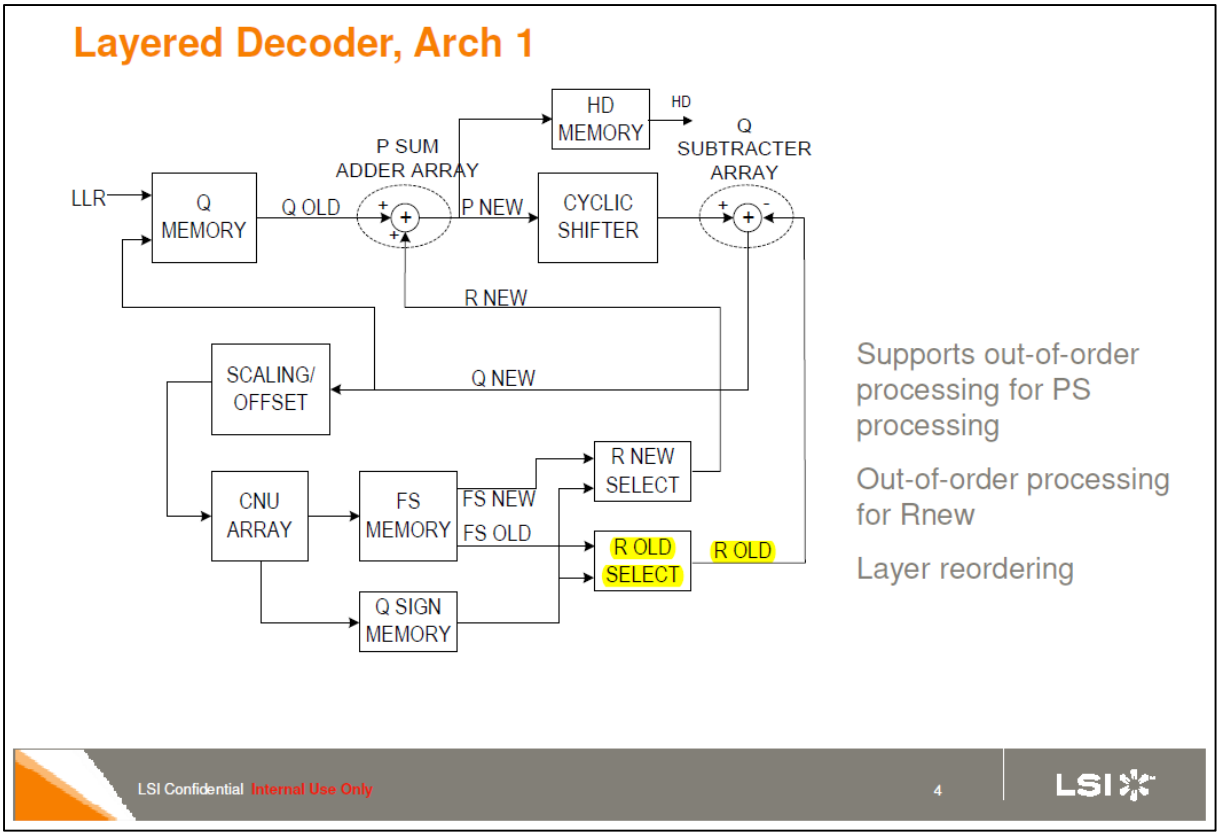


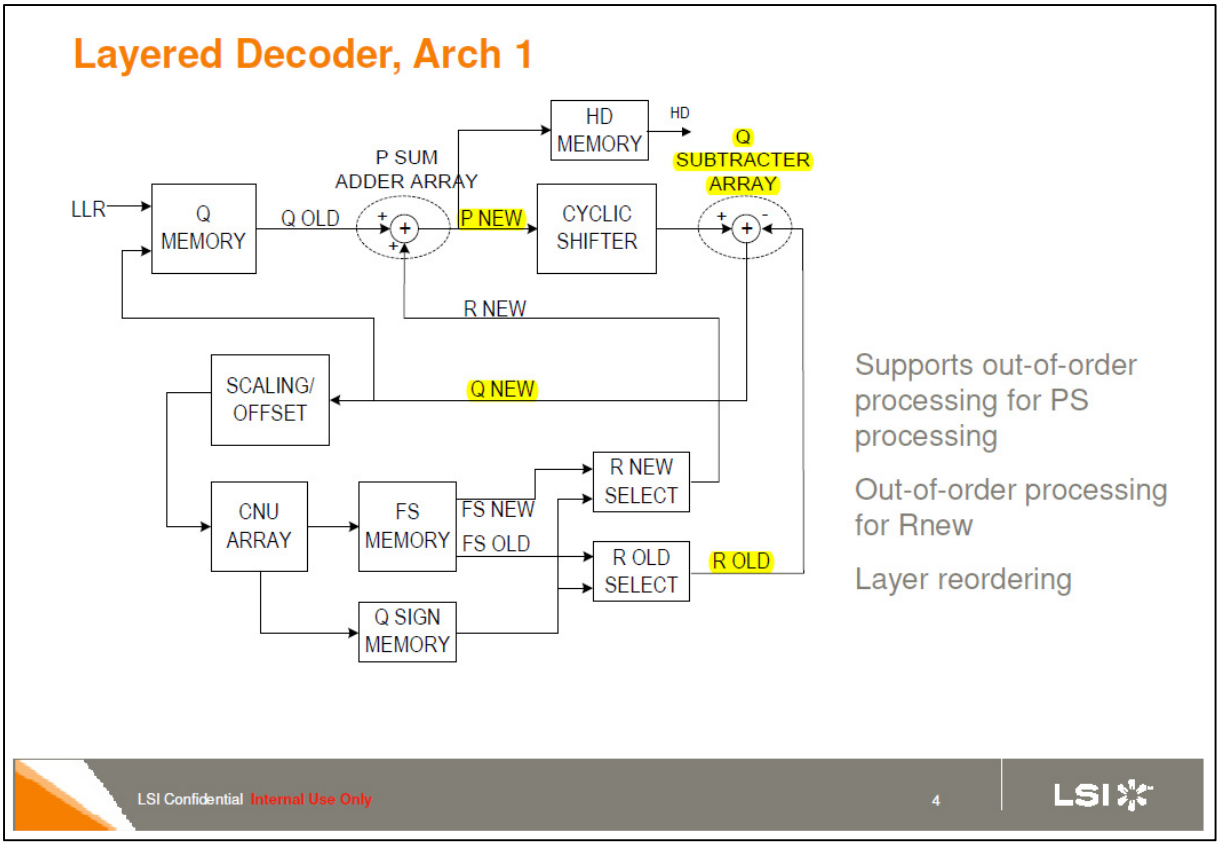
Fig. 15

170. The Accused Products process each block of the matrix in processing substeps comprising an R old update substep that selects an R old message for a layer of the matrix currently being processed. For example, with respect to the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products, the Layered Decoder Presentation discloses an R OLD SELECT unit that selects an R old message for a layer of the matrix currently being processed.

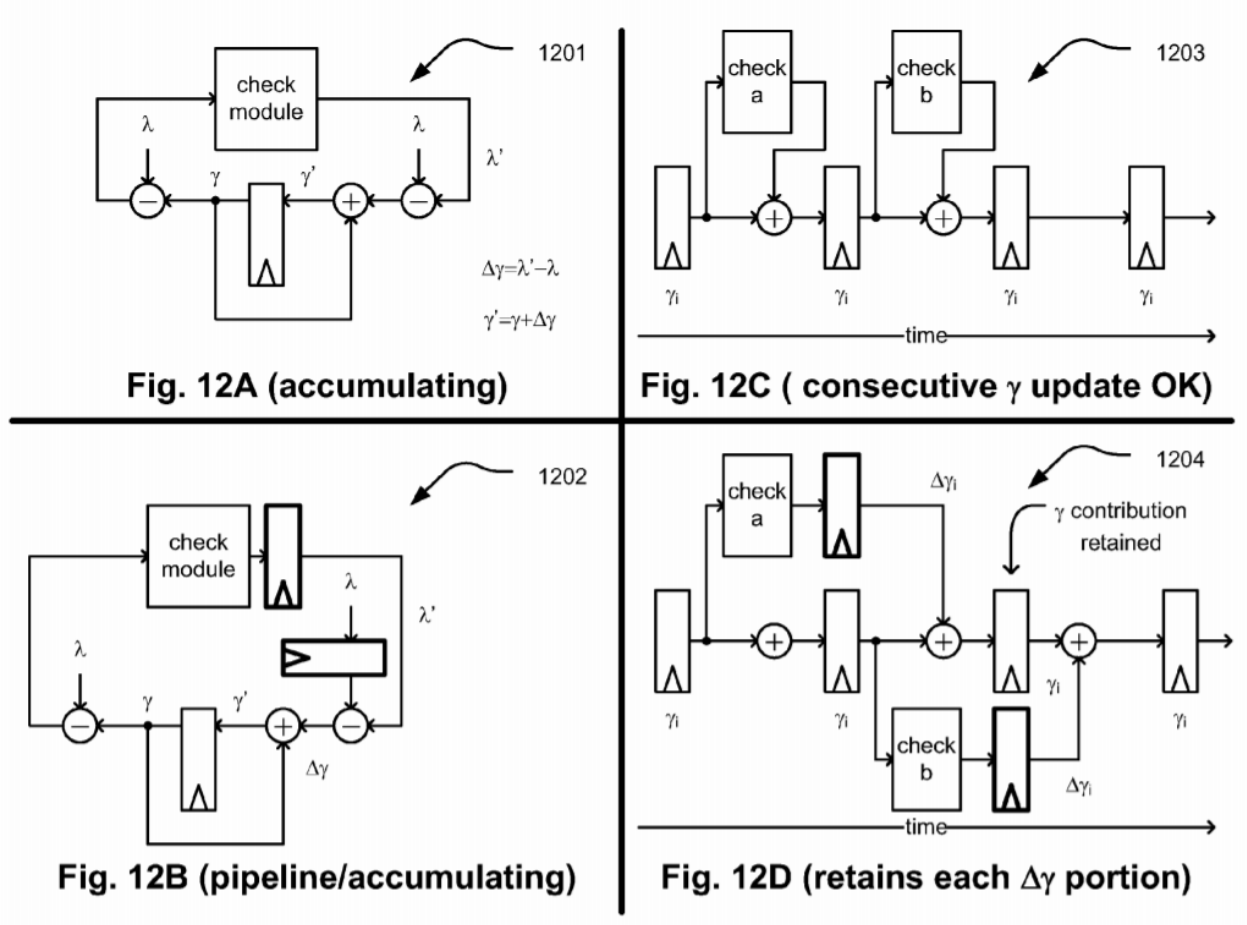


With respect to the Accused Wi-Fi Products, they perform the LDPC decoding method described in the '488 patent which includes an accumulating decoding substep whereby an old check edge message (λ) value is selected for a layer of the matrix currently being processed, such as described, for example, in FIG. 15 (reproduced at ¶ 155, *supra*) and the accompanying disclosure of method 1500 for performing an APP value update using first through fourth check edge messages (shown as λ1 – λ4).

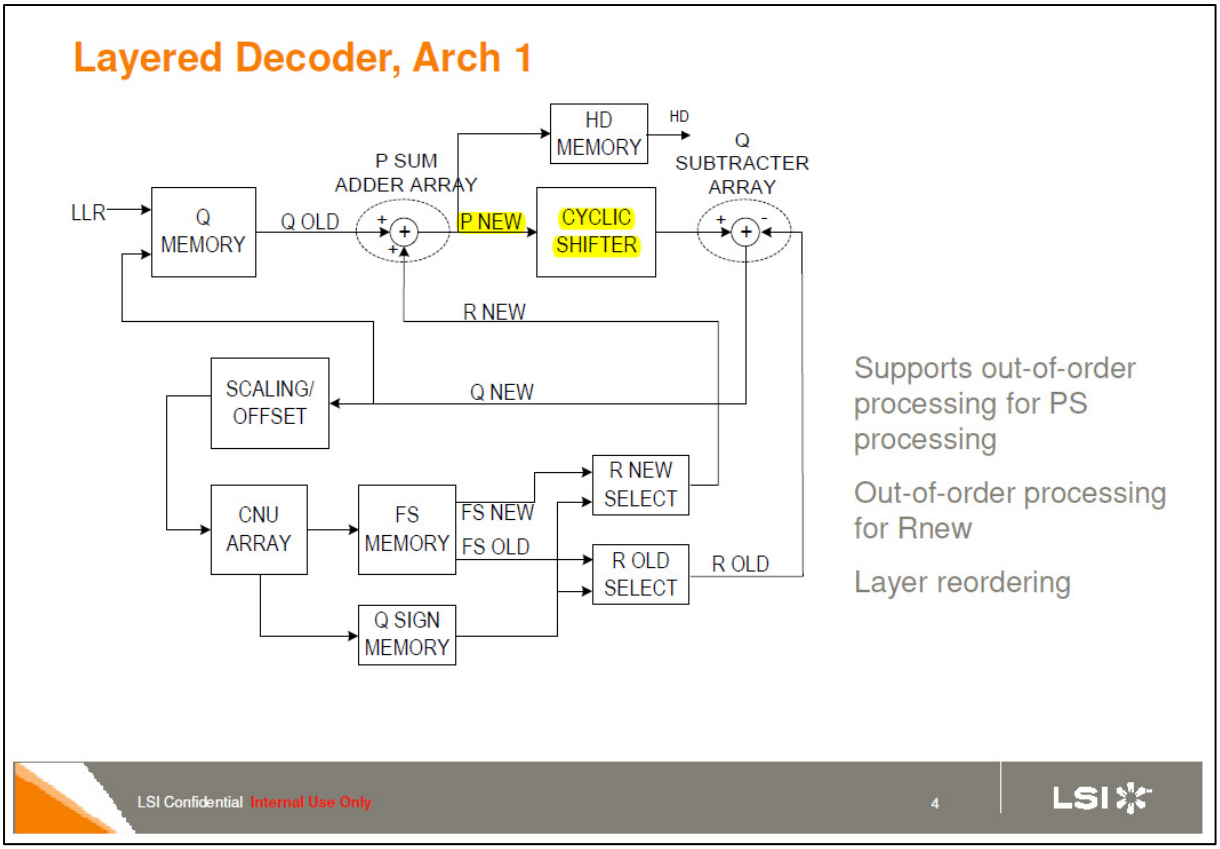
171. The Accused Products process each block of the matrix in processing substeps comprising a Q message substep that computes variable node messages (Q messages). For example, with respect to the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products, the Layered Decoder Presentation discloses a Q SUBTRACTER ARRAY that computes variable node messages (Q messages).



With respect to the Accused Wi-Fi Products, they perform the LDPC decoding method described in the '488 patent which includes a decoding substep whereby a check module receives a value that is a difference of (γ–λ) (*i.e.*, a difference between a check edge message (λ) and an APP (or gamma(γ)) value, such as described, for example, in FIG. 12B (reproduced below), and the accompanying disclosure.



172. The Accused Products permute a P message, wherein the permuting comprises permuting the P message by the difference of the permutation of a block currently being processed and the permutation of a block previously processed. For example, with respect to the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products, the Layered Decoder Presentation discloses the presence of CYCLIC SHIFTER configured to permute a P message by the difference of the permutation of a block currently being processed and the permutation of a block previously processed.



With respect to the Accused Wi-Fi Products, they perform the LDPC decoding method described in the '488 patent which includes using an accumulating LDPC pipeline using daisy chain registers that permutes an APP (or gamma(γ)) value by the difference of the permutation of a block currently being processed and the permutation of a block previously processed, such as described, for example, in FIG. 14 (reproduced below) and the corresponding disclosure.

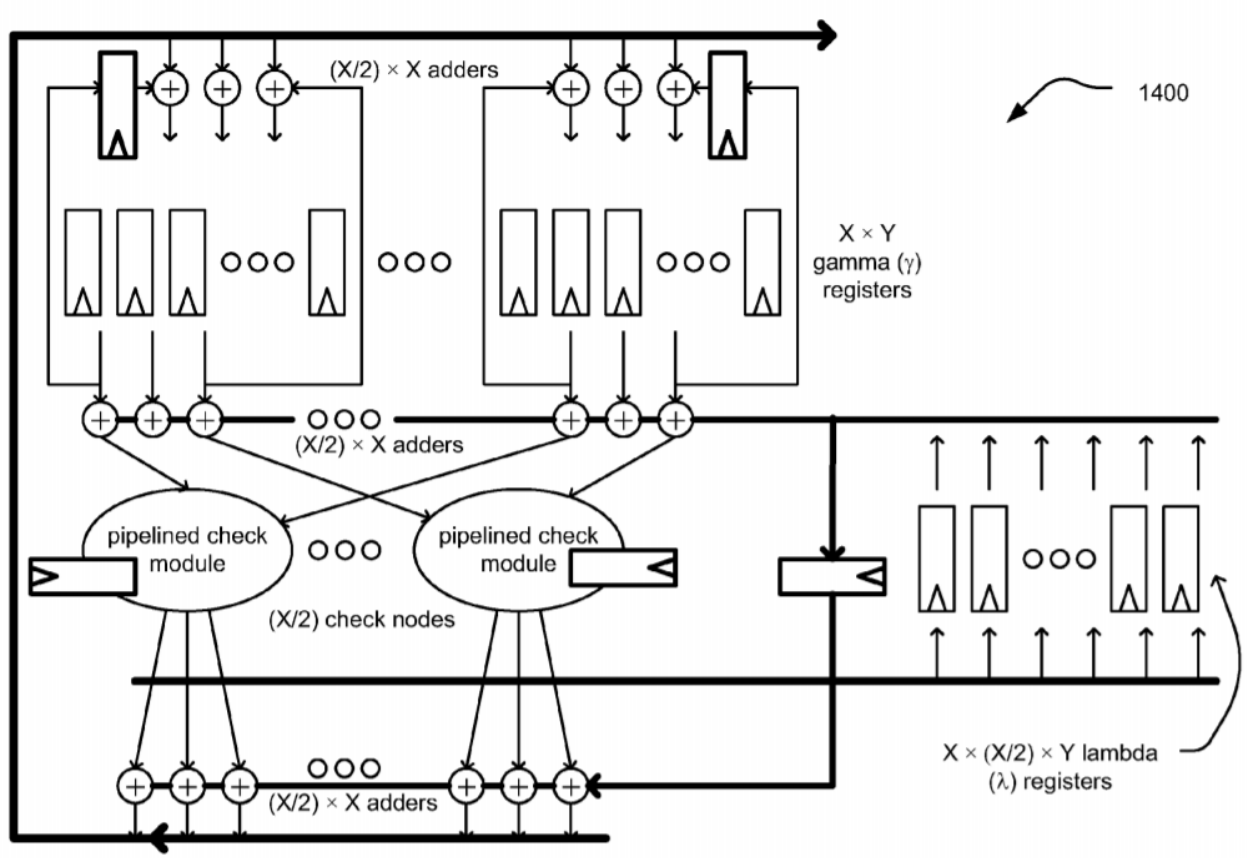
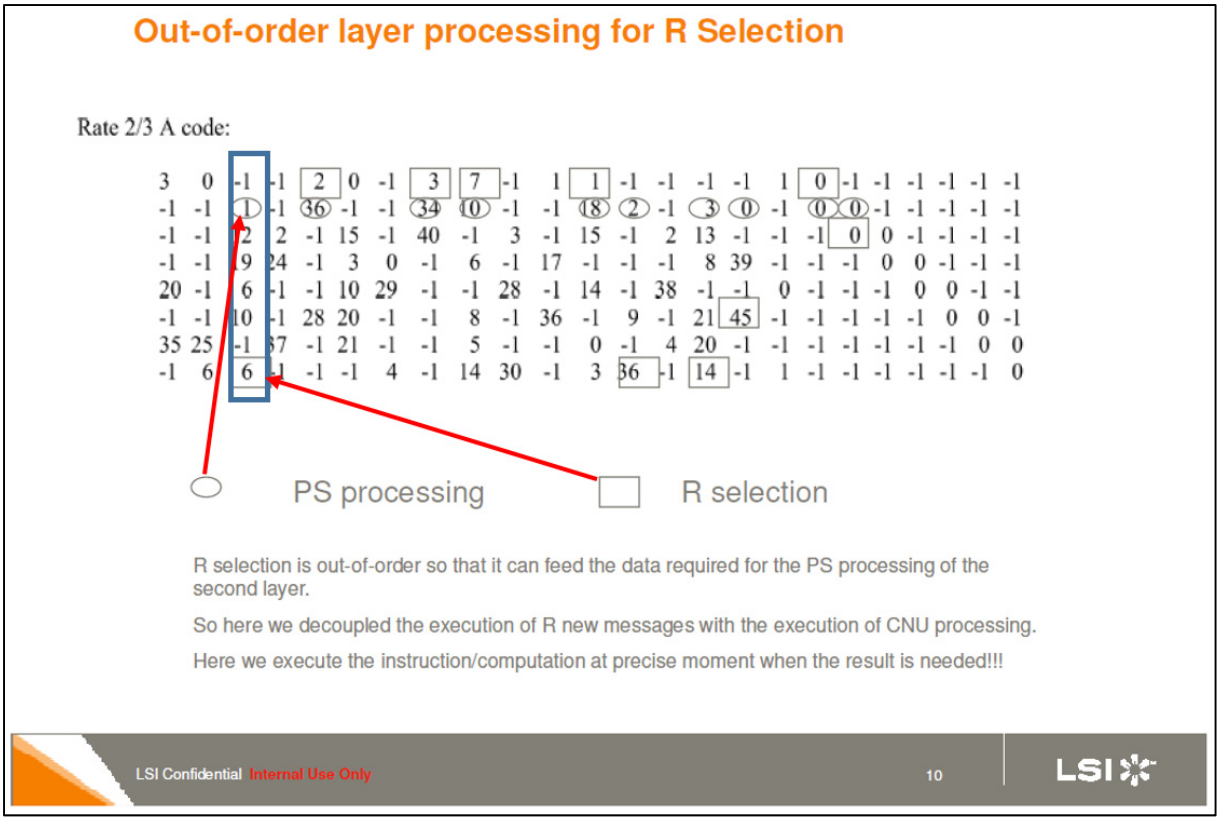


Fig. 14 (pipeline/accumulating)

173. The Accused Products permute a P message wherein the block currently being processed and the block previously processed are in a same block column. For example, with respect to the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products, the Layered Decoder Presentation discloses that the computation of the R messages ("R SELECTION") for a first non-zero block are generated while processing the second non-zero block ("PS PROCESSING"), and these two blocks are in a same block column of an LDPC matrix.



With respect to the Accused Wi-Fi Products, they perform the LDPC decoding method described in the '488 patent which includes maintaining for each column of the matrix corresponding to the best estimate of the log-likelihood ratio (LLR) of each codeword bit (i.e., APP (or gamma(Y)), considering incremental changes in APP value contributions from different check nodes that are in the same column, permuting LLR value (i.e. APP (or gamma (γ) value) using daisy chain and the block currently being processed and the block previously processed are in a same block column of an LDPC matrix, such as described in FIG. 9 (reproduced at ¶ 152, *supra*) and FIG. 15 (reproduced at ¶ 155, *supra*) and their corresponding disclosures.

174. In view of the foregoing, Defendants and/or the Broadcom Predecessor Entities have directly infringed at least Claims 7-12 and 18-22 of the '140 Patent through their internal testing, use, and operation of the Accused Products.

175. On information and belief, Defendants and/or the Broadcom Predecessor Entities have had actual or constructive knowledge of the '140 Patent since at least January 22, 2013, as noted above.

176. Defendants further have had knowledge of the '140 Patent at least as early as the filing and/or service of Plaintiff's original Complaint. (*See* D.I. 1, 5)

177. On information and belief, Defendants and/or the Broadcom Predecessor Entities have taken active steps to induce infringement by others of at least Claims 7-12 and 18-22 of the '140 Patent in violation of 35 U.S.C. §271(b), including, for example, by (a) inducing manufacturers to perform the claimed inventions when testing the Accused Products, and (b) inducing end users to perform the claimed inventions when using the Accused Products. Such active steps include, but are not limited to, selling Accused Products with the knowledge and intent that the Accused Products will be operated by such manufacturers and their customers in accordance with the claimed inventions, as set forth in the Section "EXAMPLES OF DIRECT AND INDIRECT INFRINGEMENT" below.

178. On information and belief, Defendants and/or the Broadcom Predecessor Entities have known or should have known that such activities induce others to directly infringe one or more of at least Claims 7-12 and 18-22 of the '140 Patent. For example, Defendants and/or the Broadcom Predecessor Entities should have known that their actions induced others to directly infringe as of the date it became aware of the issuance of the '140 Patent on or about October 8, 2013, and in any event no later than the date they were advised of the issuance of the '140 Patent by Dr. Gunnam on January 31, 2014. Defendants and/or the Broadcom Predecessor Entities were further informed that the technology in the Accused Products infringed the '140 Patent, and Defendants and/or the Broadcom Predecessor Entities have knowingly and purposefully

continued to exploit the patented technology despite knowing that it was covered by the '140 Patent, as set forth in the Section "EXAMPLES OF DIRECT AND INDIRECT INFRINGEMENT" below.

179. On information and belief, Defendants and/or the Broadcom Predecessor Entities have contributed to the infringement of at least Claims 7-12 and 18-22 of the '140 Patent by others, including consumer/end-user use of the Accused Products, in violation of 35 U.S.C. § 271(c). Acts by Defendants and/or the Broadcom Predecessor Entities that contribute to the infringement of others include, but are not limited to, the sale, offer for sale, and/or import by Defendants and/or the Broadcom Predecessor Entities of the Accused Products. Such Accused Products are especially made for or adapted for use to infringe, and are not a staple article of commerce and are not suitable for substantial non-infringing use. The Accused Products are apparatuses for use in practicing the inventions patented in Claims 7-12 and 18-22 of the '140 Patent, and are at least a material part of those claimed inventions, for example, as described above with respect to Claims 7 and 18 and as set forth in the Section "EXAMPLES OF DIRECT AND INDIRECT INFRINGEMENT" below.

180. On information and belief, the steps recited in Claim 7, for example, are performed by the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products and the steps recited in Claim 18, for example, are performed by the Accused Products. As also described above, Defendants and/or the Broadcom Predecessor Entities have, on information and belief, been on notice of the '140 Patent since it issued on October 8, 2013, and in any event no later than January 31, 2014.

181. In addition, Defendants and/or the Broadcom Predecessor Entities have been aware of the '140 Patent since filing and/or service of Plaintiff's original Complaint, and

Defendants and/or the Broadcom Predecessor Entities have further been aware that use of the Accused Products necessarily practice the inventions in Claims 7-12 and 18-22 of the '140 Patent. (*See* D.I. 1, 5)

182. The Accused Products are especially made for or adapted for use to infringe, and are not a staple article of commerce and are not suitable for substantial non-infringing use. By way of example, the use of the LDPC decoders included in the Accused Products is necessary to use the accused products for their intended purpose (decoding data from a hard disk drive, solid state drive, or wireless digital transmission), and the LDPC decoders necessarily perform the claimed inventions when they decode data. Accordingly, the Accused Products do not have a substantial use that does not entail practicing the claimed inventions. On information and belief, the Accused Products cannot be used but to infringe the '140 Patent.

183. Despite Defendants' and/or the Broadcom Predecessor Entities' knowledge and notice of the '140 Patent and their ongoing infringement, Defendants and/or the Broadcom Predecessor Entities continue to test or use the Accused Products in a manner that willfully infringes the '140 Patent, and on information and belief continue to sell and/or offer for sale the Accused Products to the United States market for customers / end users to infringe. On information and belief, nearly all of Dr. Gunnam's work, *inter alia*, at LSI was centered on the TAMUS' '320 provisional application. On information and belief, LSI recognized its competitive disadvantage from not having acquired the rights to the Patents-in-Suit for itself, and embarked on a course of action where it filed and prosecuted numerous patents, based on Dr. Gunnam's work concerning the TAMUS '320 provisional application. *See* https://www.google.com/search?tbm=pts&ei=lR4QXMpHrm40PEP_s6YwAE&q=Ser.+No.+12%2F113%2C729+filed+on+May+1%2C+2008&oq=Ser.+No.+12%2F113%2C729+filed+on+M

ay+1%2C+2008&gs_l=psyab.3...95601.99862.0.100208.3.3.0.0.0.0.128.258.2j1.3.0....0...1c.1.64.psy-ab..0.0.0....0.OmH6jRmYHJo; *see also* https://www.google.com/search?tbm=pts&ei=jB4QXODdHdC60PEP0qC4A4&q=Ser.+No.+12%2F113%2C755+filed+on+May+1%2C+2008&oq=Ser.+No.+12%2F113%2C755+filed+on+May+1%2C+2008&gs_l=psy-ab.3...7529.7728.0.8111.2.2.0.0.0.0.81.149.2.2.0....0...1c.1.64.psy-ab..0.0.0....0.UBEXLdczJgA. On information and belief, LSI filed and prosecuted these patents despite Dr. Gunnam's repeated requests to LSI management for LSI to obtain a license for the TAMUS intellectual property. Defendants' and/or the Broadcom Predecessor Entities' infringement of the '140 Patent is thus willful, as set forth above. Defendants and/or the Broadcom Predecessor Entities lacked a justifiable belief that they do not infringe the '140 Patent, or that the '140 Patent is invalid or unenforceable, and have acted recklessly in their infringing activity, justifying an increase in the damages to be awarded to Plaintiff up to three times the amount found or assessed, in accordance with 35 U.S.C. § 284.

184. This case is rendered an exceptional case at least in light of Defendants' and/or the Broadcom Predecessor Entities' willful infringement of the '140 Patent, justifying an award to Plaintiff of its reasonable attorney fees, in accordance with 35 U.S.C. § 285.

185. Plaintiff has no adequate remedy at law for Defendants' and/or the Broadcom Predecessor Entities' acts of infringement. As a direct and proximate result of Defendants' and/or the Broadcom Predecessor Entities' acts of infringement, Plaintiff has suffered and continues to suffer damages and irreparable harm. Unless Defendants' and/or the Broadcom Predecessor Entities' acts of infringement are enjoined by this Court, Plaintiff will continue to be damaged and irreparably harmed.

186. Defendants' and/or the Broadcom Predecessor Entities' infringement of the '140 Patent has damaged and continues to damage Plaintiff in an amount yet to be determined, of at least a reasonable royalty and/or lost profits that Plaintiff would have made but for Defendants' and/or the Broadcom Predecessor Entities' infringement acts.

COUNT III
(Infringement under 35 U.S.C. § 271 of U.S. Patent No. 9,112,530)

187. Plaintiff repeats and re-alleges the paragraphs above as if fully set forth herein.

188. The '530 Patent is valid, enforceable, and was duly issued on August 18, 2015 in full compliance with Title 35 of the United States Code.

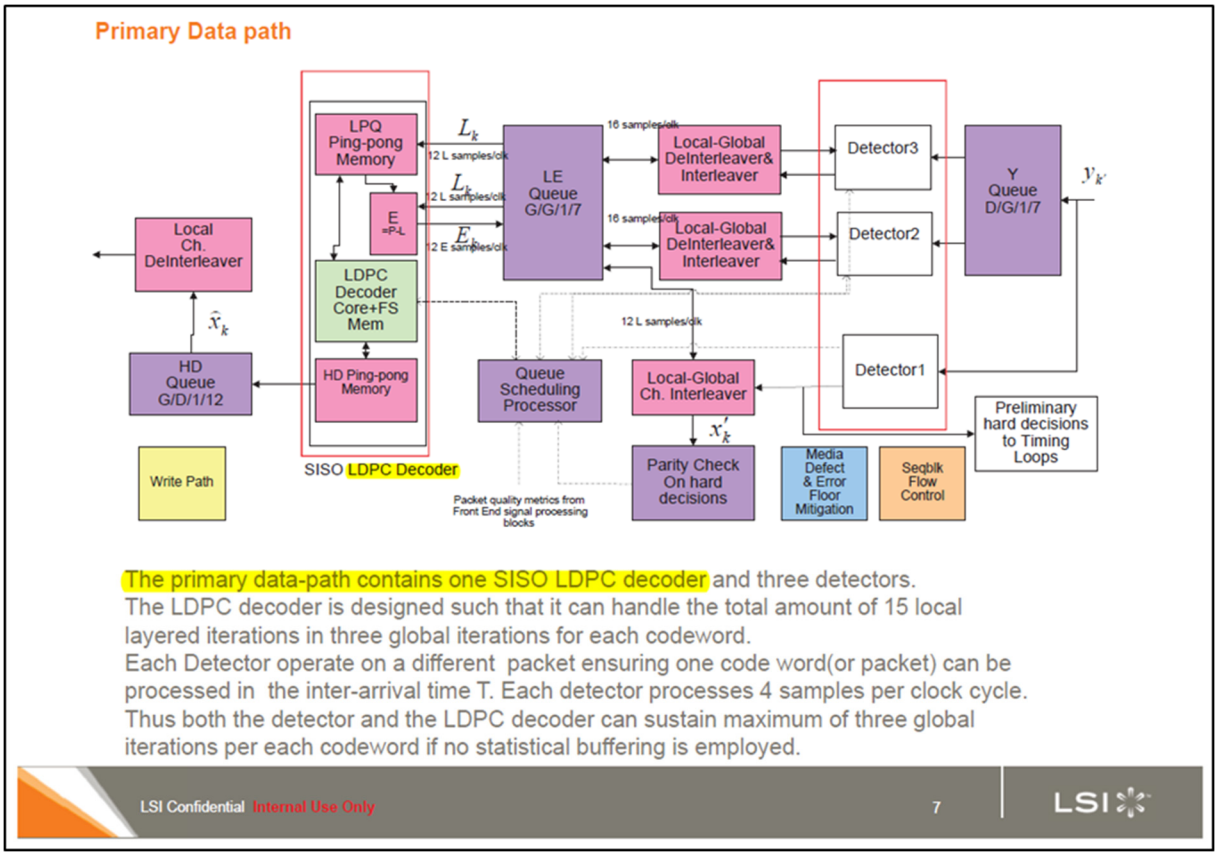
189. On information and belief, in violation of 35 U.S.C. § 271, Defendants and/or the Broadcom Predecessor Entities have infringed, contributed to the infringement of, and/or induced others to infringe the '530 Patent, either literally or under the doctrine of equivalents, by, among other things, making, using, offering for sale, selling, selling infringing products abroad with knowledge and intent that the infringing products be imported into the United States by others, and/or importing into the United States unlicensed systems and/or products in a manner that infringes at least Claims 13-20, 22-23, and 25-31 of the '530 Patent.

190. On information and belief, Defendants and/or the Broadcom Predecessor Entities have directly infringed the '530 Patent, for example, by making, using, selling, offering to sell, and/or importing into the United States the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products, which meet each and every limitation of at least Claims 13-20, 22-23, and 25-31 of the '530 Patent in violation of Plaintiff's patent rights and without Plaintiff's license or authority. Non-limiting examples of such infringement are provided below, based on the limited information currently available to Plaintiff.

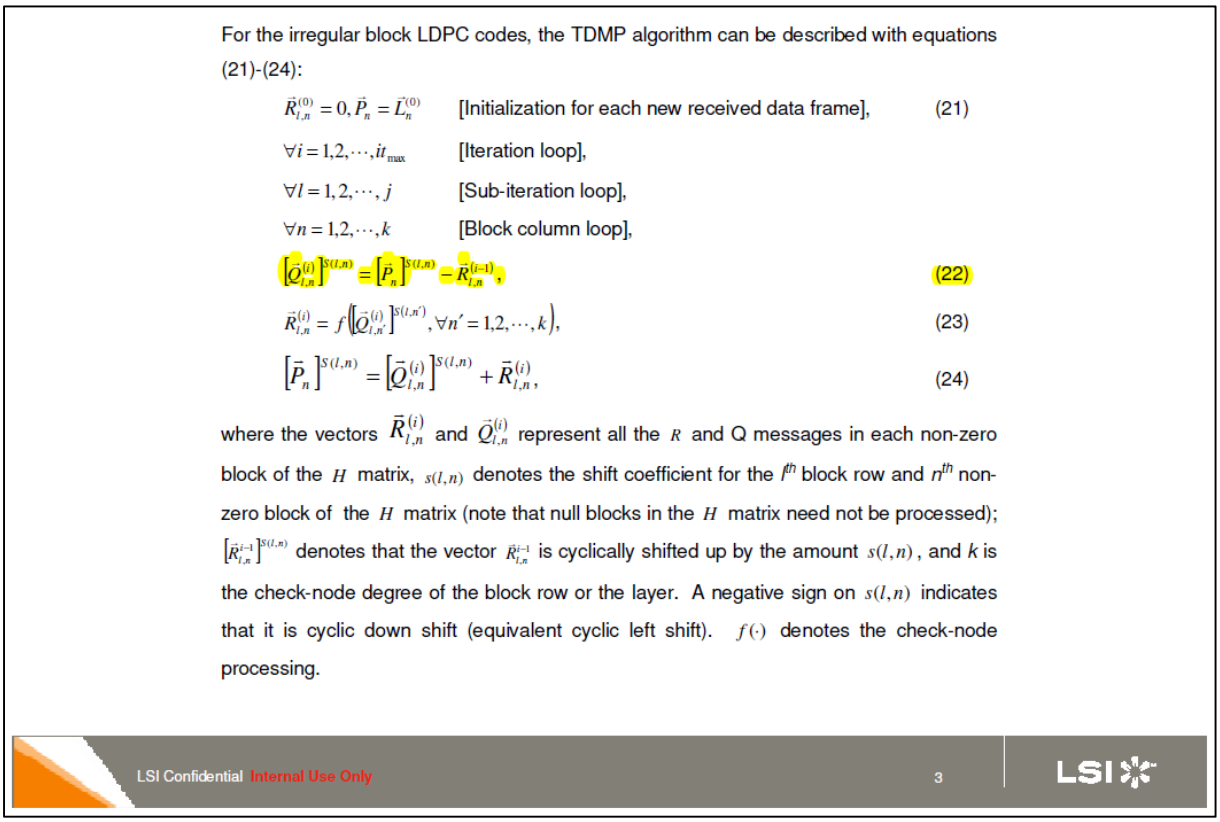
191. Claim 13 of the '530 Patent recites as follows:

13. A low density parity check (LDPC) code decoder, comprising:
a Q message generator configured to combine an R message with a P message to produce a Q message;
logic configured to reduce the magnitude a Q message provided to a check node unit of the decoder; and
a permuter configured to permute the P message by a difference of permutation of a block currently being processed and permutation of a block previously processed; wherein the block currently being processed and the block previously processed are in a same block column of an LDPC matrix.

192. On information and belief, the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products satisfy each and every limitation of Claim 13. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include an LDPC code decoder. For example, the McLaren Architecture Presentation references the LDPC decoder.



193. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include a Q message generator configured to combine an R message with a P message to produce a Q message. For example, the Layered Decoder Presentation uses equations and figures taken directly from the '530 Patent to disclose the presence of a Q SUBTRACTER ARRAY configured to combine an R message with a P message to produce a Q message.



For the irregular block LDPC codes, the TDMP algorithm can be described with equations (21)-(24):

$\vec{R}_{l,n}^{(0)} = 0, \vec{P}_n = \vec{L}_n^{(0)}$ [Initialization for each new received data frame], (21)

$\forall i = 1,2,\cdots,it_{\max}$ [Iteration loop],

$\forall l = 1,2,\cdots,j$ [Sub-iteration loop],

$\forall n = 1,2,\cdots,k$ [Block column loop],

$$\left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n)} = \left[\vec{P}_n\right]^{S(l,n)} - \vec{R}_{l,n}^{(i-1)}, \quad (22)$$

$$\vec{R}_{l,n}^{(i)} = f\left(\left[\vec{Q}_{l,n'}^{(i)}\right]^{S(l,n')}, \forall n' = 1,2,\cdots,k\right), \quad (23)$$

$$\left[\vec{P}_n\right]^{S(l,n)} = \left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n)} + \vec{R}_{l,n}^{(i)}, \quad (24)$$

where the vectors $\vec{R}_{l,n}^{(i)}$ and $\vec{Q}_{l,n}^{(i)}$ represent all the R and Q messages in each non-zero block of the H matrix, $s(l,n)$ denotes the shift coefficient for the l^{th} block row and n^{th} non-zero block of the H matrix (note that null blocks in the H matrix need not be processed); $\left[\vec{R}_{l,n}^{i-1}\right]^{S(l,n)}$ denotes that the vector $\vec{R}_{l,n}^{i-1}$ is cyclically shifted up by the amount $s(l,n)$, and k is the check-node degree of the block row or the layer. A negative sign on $s(l,n)$ indicates that it is cyclic down shift (equivalent cyclic left shift). $f(\cdot)$ denotes the check-node processing.

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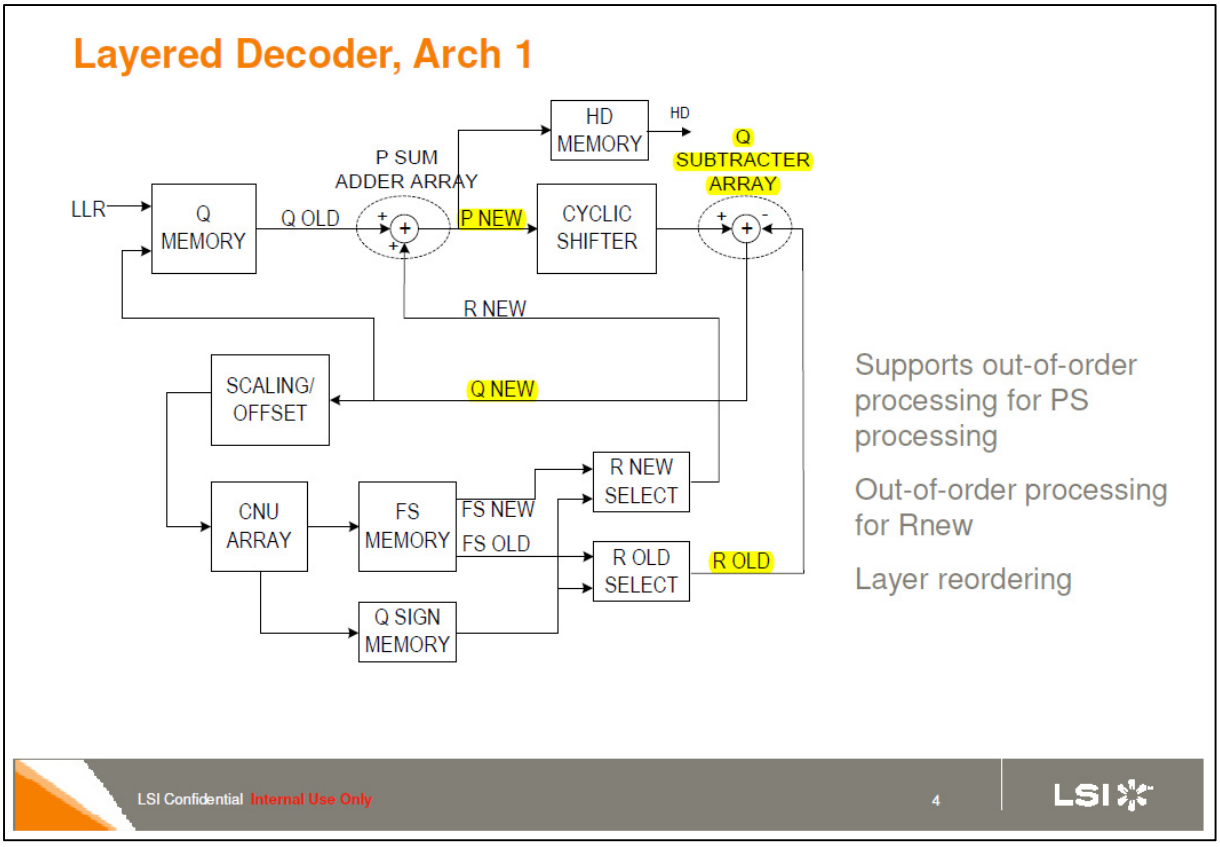


194. The TDMP algorithm equations of the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products are substantially identical to what is set forth in the '530 Patent.

'530 Patent at 15:35–62	**Layered Decoder Presentation at 3**
For the irregular block LDPC codes, the TDMP algorithm can be described with equations (21)-(24): $\vec{R}_{l,n}^{(0)}=0, \vec{P}_n=\vec{L}_n^{(0)}$ [Initialization for each new received data frame], $\forall i=1,2,\ldots,it_{max}$ [Iteration loop], $\forall l=1,2,\ldots,j$ [Sub-iteration loop], $\forall n=1,2,\ldots,k$ [Block column loop], (21) $[\vec{Q}_{l,n}^{(i)}]^{S(l,n)}=[\vec{P}_n]^{S(l,n)}-\vec{R}_{l,n}^{(i-1)}$ (22) $\vec{R}_{l,n}^{(i)}=f([\vec{Q}_{l,n'}^{(i)}]^{S(l,n')}), \forall n'=1,2,\ldots,k).$ (23) $[\vec{P}_n]^{S(l,n)}=[\vec{Q}_{l,n}^{(i)}]^{S(l,n)}+\vec{R}_{l,n}^{(i)}$, (24) where the vectors and $\vec{R}_{l,n}^{(i)}$ and $\vec{Q}_{l,n}^{(i)}$ represent all the R and Q messages in each non-zero block of the H matrix, s(l,n) denotes the shift coefficient for the i^{th} block row and n^{th} non-zero block of the H matrix (note that null blocks in the H matrix need not be processed); $[\vec{R}_{l,n}^{i-1}]^{S(l,n)}$ denotes that the vector is cyclically shifted up by the amount s(l,n) and k is the check-node degree of the block row or the layer. A negative sign on s(l,n) indicates that it is cyclic down shift (equivalent cyclic left shift). $f(\cdot)$ denotes the check-node processing, which can be performed using BCJR, SP or MS.	

For the irregular block LDPC codes, the TDMP algorithm can be described with equations (21)-(24):

$\vec{R}_{l,n}^{(0)} = 0, \vec{P}_n = \vec{L}_n^{(0)}$ [Initialization for each new received data frame], (21)

$\forall i = 1,2,\cdots, it_{\max}$ [Iteration loop],

$\forall l = 1,2,\cdots, j$ [Sub-iteration loop],

$\forall n = 1,2,\cdots, k$ [Block column loop],

$$\left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n)} = \left[\vec{P}_n\right]^{S(l,n)} - \vec{R}_{l,n}^{(i-1)}, \quad (22)$$

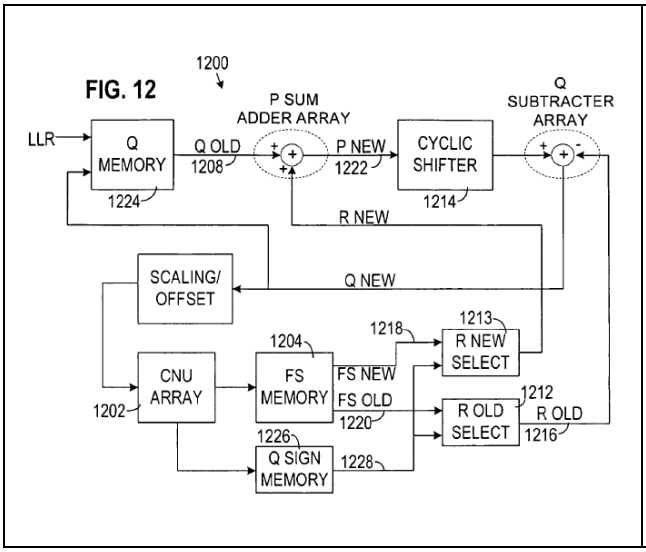
$$\vec{R}_{l,n}^{(i)} = f\left(\left[\vec{Q}_{l,n'}^{(i)}\right]^{S(l,n')}, \forall n' = 1,2,\cdots,k\right), \quad (23)$$

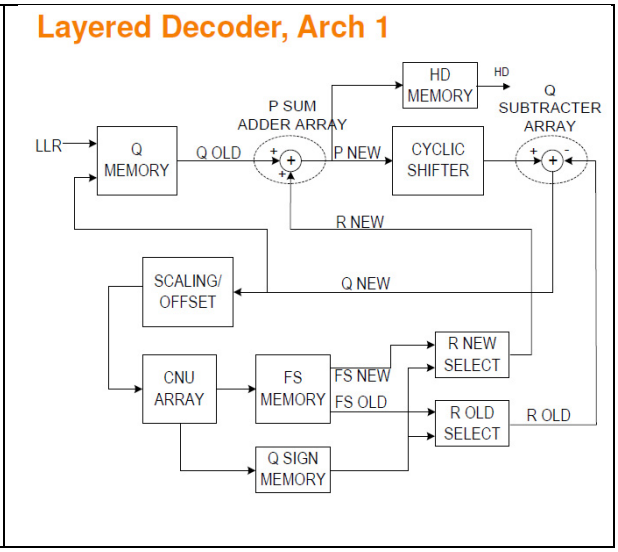
$$\left[\vec{P}_n\right]^{S(l,n)} = \left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n)} + \vec{R}_{l,n}^{(i)}, \quad (24)$$

where the vectors $\vec{R}_{l,n}^{(i)}$ and $\vec{Q}_{l,n}^{(i)}$ represent all the R and Q messages in each non-zero block of the H matrix, $s(l,n)$ denotes the shift coefficient for the l^{th} block row and n^{th} non-zero block of the H matrix (note that null blocks in the H matrix need not be processed); $\left[\vec{R}_{l,n}^{i-1}\right]^{S(l,n)}$ denotes that the vector $\vec{R}_{l,n}^{i-1}$ is cyclically shifted up by the amount $s(l,n)$, and k is the check-node degree of the block row or the layer. A negative sign on $s(l,n)$ indicates that it is cyclic down shift (equivalent cyclic left shift). $f(\cdot)$ denotes the check-node processing.

195. The layered decoder architecture of the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products is substantially identical to what is set forth in the '530 Patent.

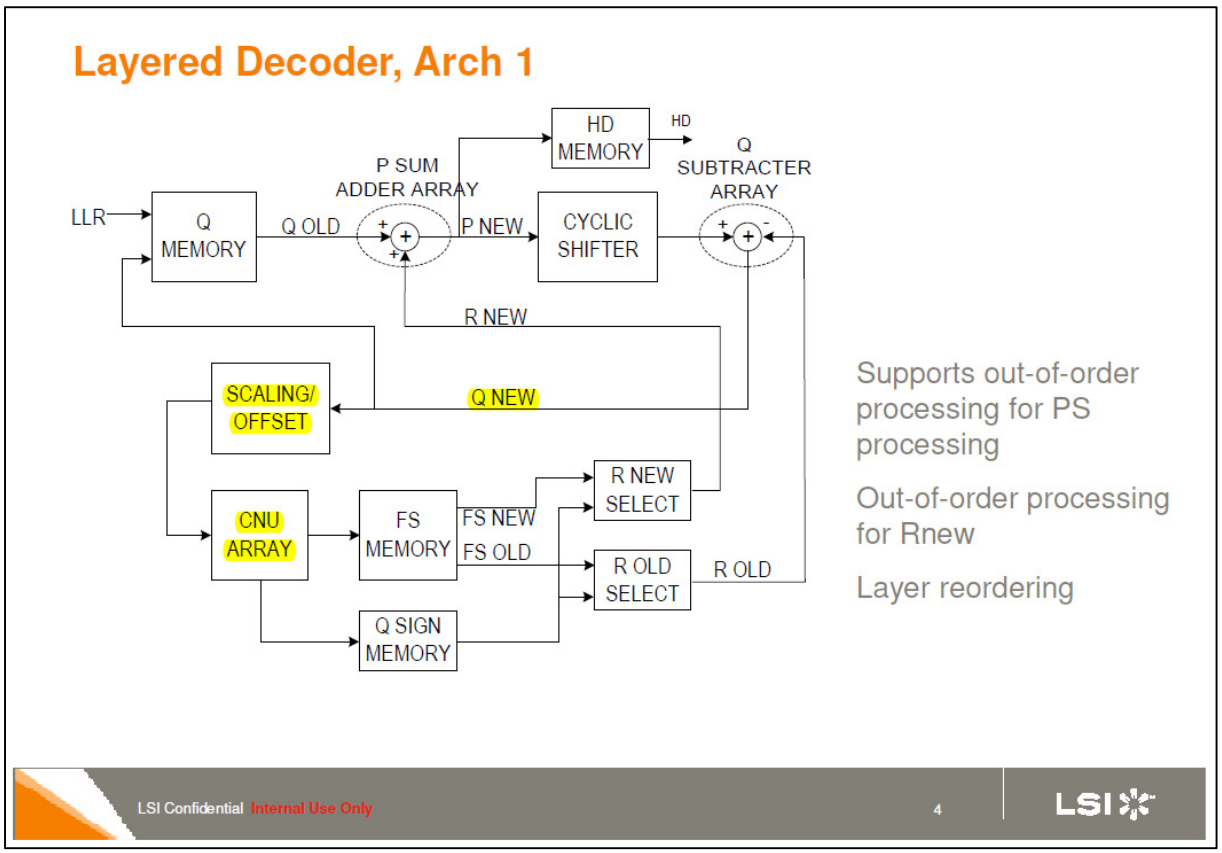
'530 Patent at FIG. 12 **Layered Decoder Presentation at 4**



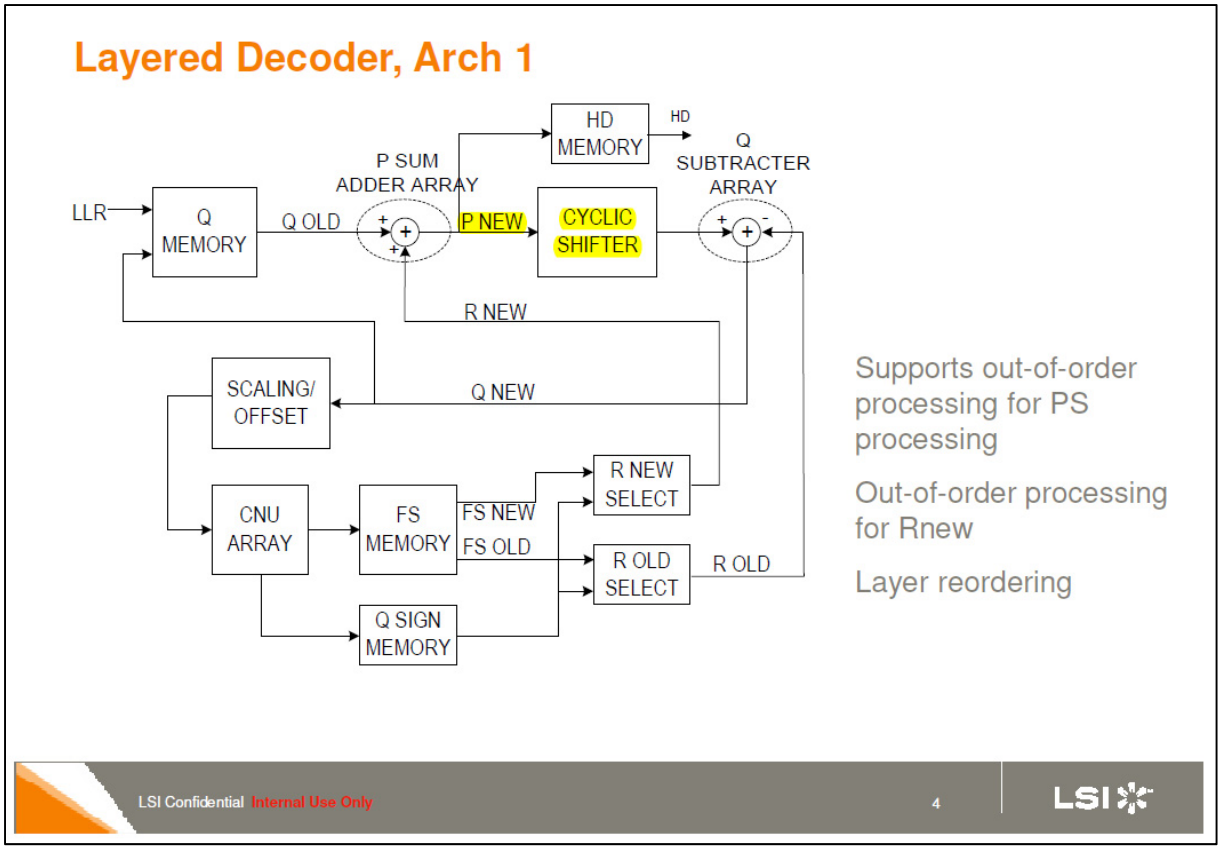


196. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include logic configured to reduce the magnitude a Q message provided to a check node unit of the decoder. For example, the Layered Decoder

Presentation discloses the presence of a SCALING/OFFSET unit configured to reduce the magnitude of a Q message provided to a check node unit of the decoder.



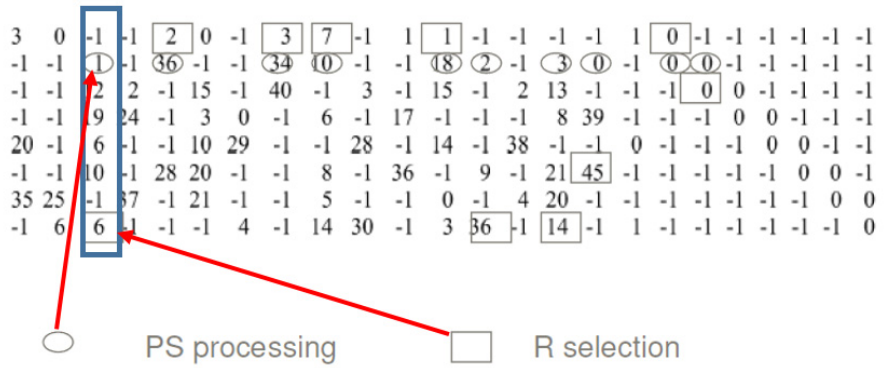
197. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include a permuter configured to permute the P message by a difference of permutation of a block currently being processed and permutation of a block previously processed. For example, the Layered Decoder Presentation discloses the presence of CYCLIC SHIFTER configured to permute the P message by a difference of permutation of a block currently being processed and permutation of a block previously processed.



198. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include wherein the block currently being processed and the block previously processed are in a same block column of an LDPC matrix. For example, the Layered Decoder Presentation discloses that the computation of the R messages ("R SELECTION") for a first non-zero block are generated while processing the second non-zero block ("PS PROCESSING"), and these two blocks are in a same block column of an LDPC matrix.

Out-of-order layer processing for R Selection

Rate 2/3 A code:



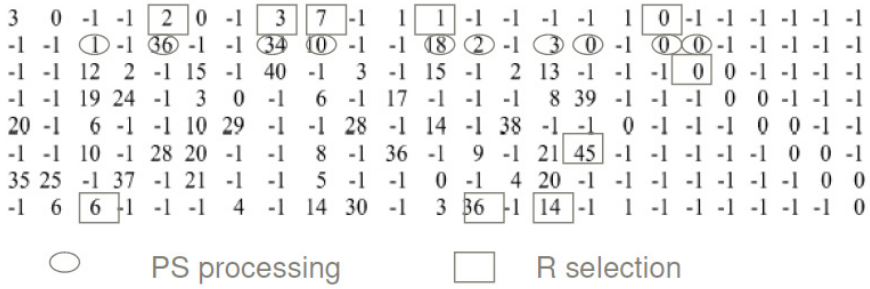
R selection is out-of-order so that it can feed the data required for the PS processing of the second layer.

So here we decoupled the execution of R new messages with the execution of CNU processing.

Here we execute the instruction/computation at precise moment when the result is needed!!!

Out-of-order block processing for Partial State

Rate 2/3 A code:



Re-ordering of block processing . While processing the layer 2,

the blocks which depend on layer 1 will be processed last to allow for the pipeline latency.

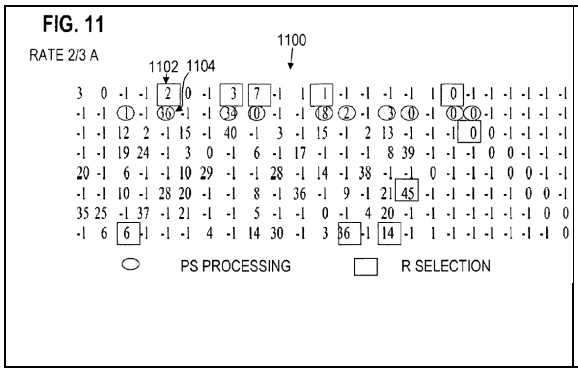
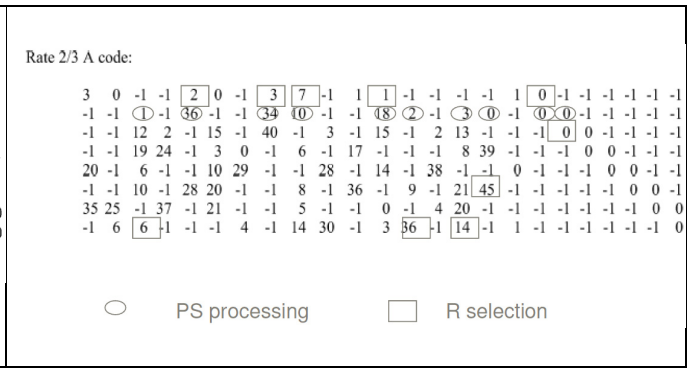
In the above example, the pipeline latency can be 5.

The vector pipeline depth is 5.so no stall cycles are needed while processing the layer 2 due to the pipelining. [In other implementations, the stall cycles are introduced – which will effectively reduce the throughput by a huge margin.]

Also we will sequence the operations in layer such that we process the block first that has dependent data available for the longest time.

This naturally leads us to true out-of-order processing across several layers. In practice we wont do out-of-order partial state processing involving more than 2 layers.

199. The exemplary Rate 2/3 A code of the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products is identical to what is set forth in the '530 Patent.

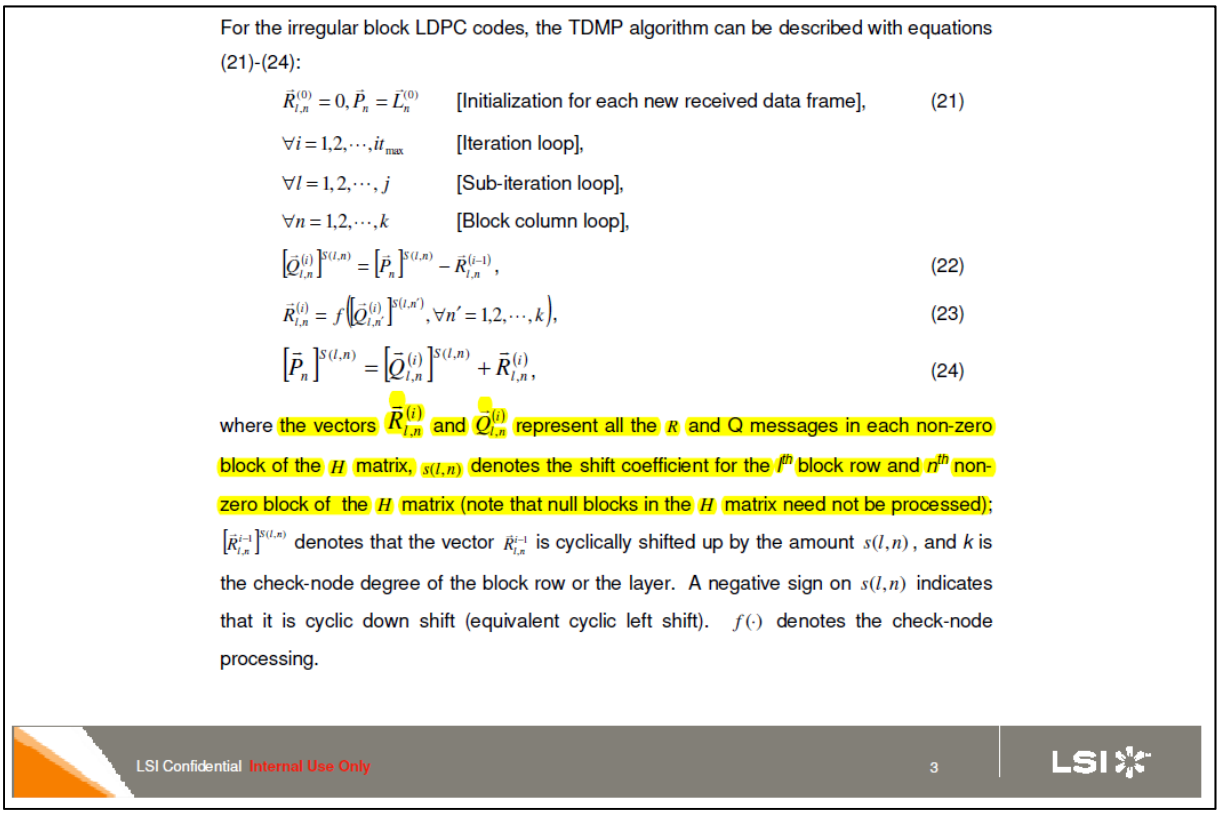
'530 Patent at FIG. 11	**Layered Decoder Presentation at 10**
	

200. Claim 25 of the '530 Patent recites as follows:

> 25. A low density parity check (LDPC) code decoder, comprising:
> a control unit that controls decoder processing, the control unit configured to cause the decoder to process blocks of an LDPC matrix in a sequence defined by an order of non-zero blocks of a given layer of the LDPC matrix;
> wherein the LDPC matrix comprises a plurality of layers, each layer having a plurality of blocks ordered such that the sequence of non-zero blocks of the given layer of the LDPC matrix specifies a first set of non-zero blocks of the given layer to be processed at a given time and a second set of non-zero blocks of the given layer to be processed after the first set of non-zero blocks; wherein the first set specifies only non-zero blocks of the given layer that are not dependent on a result of a previously processed layer and the second set specifies non-zero blocks of the given layer that are dependent on a result of the previously processed layer.

201. On information and belief, the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products satisfy each and every limitation of Claim 25. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include an LDPC code decoder. *See* ¶ 170, *supra*.

202. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include a control unit that controls decoder processing and that is configured to cause the decoder to process blocks of an LDPC matrix in a sequence defined by an order of non-zero blocks of a given layer of the LDPC matrix. For example, using disclosures taken directly from the '530 Patent, the Layered Decoder Presentation indicates that the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products process blocks of an LDPC matrix in a sequence defined by an order of non-zero blocks of a given layer of the LDPC matrix.



For the irregular block LDPC codes, the TDMP algorithm can be described with equations (21)-(24):

$\vec{R}_{l,n}^{(0)} = 0, \vec{P}_n = \vec{L}_n^{(0)}$ [Initialization for each new received data frame], (21)

$\forall i = 1,2,\cdots,it_{\max}$ [Iteration loop],

$\forall l = 1,2,\cdots,j$ [Sub-iteration loop],

$\forall n = 1,2,\cdots,k$ [Block column loop],

$$\left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n)} = \left[\vec{P}_n\right]^{S(l,n)} - \vec{R}_{l,n}^{(i-1)}, \quad (22)$$

$$\vec{R}_{l,n}^{(i)} = f\left(\left[\vec{Q}_{l,n'}^{(i)}\right]^{S(l,n')}, \forall n' = 1,2,\cdots,k\right), \quad (23)$$

$$\left[\vec{P}_n\right]^{S(l,n)} = \left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n)} + \vec{R}_{l,n}^{(i)}, \quad (24)$$

where the vectors $\vec{R}_{l,n}^{(i)}$ and $\vec{Q}_{l,n}^{(i)}$ represent all the R and Q messages in each non-zero block of the H matrix, $s(l,n)$ denotes the shift coefficient for the l^{th} block row and n^{th} non-zero block of the H matrix (note that null blocks in the H matrix need not be processed); $\left[\vec{R}_{l,n}^{i-1}\right]^{S(l,n)}$ denotes that the vector $\vec{R}_{l,n}^{i-1}$ is cyclically shifted up by the amount $s(l,n)$, and k is the check-node degree of the block row or the layer. A negative sign on $s(l,n)$ indicates that it is cyclic down shift (equivalent cyclic left shift). $f(\cdot)$ denotes the check-node processing.

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203. The TDMP algorithm equations of the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products are identical to what is set forth in the '530 Patent.

'530 Patent at 15:35–62

For the irregular block LDPC codes, the TDMP algorithm can be described with equations (21)-(24):

$\vec{R}_{l,n}^{(0)}=0, \vec{P}_n=\vec{L}_n^{(0)}$ [Initialization for each new received data frame],

$\forall i=1,2,\ldots,it_{max}$ [Iteration loop],

$\forall l=1,2,\ldots,j$ [Sub-iteration loop],

$\forall n=1,2,\ldots,k$ [Block column loop], (21)

$[\vec{Q}_{l,n}^{(i)}]^{S(l,n)}=[\vec{P}_n]^{S(l,n)}-\vec{R}_{l,n}^{(i-1)}$ (22)

$\vec{R}_{l,n}^{(i)}=f([\vec{Q}_{l,n'}^{(i)}]^{S(l,n')}), \forall n'=1,2,\ldots,k).$ (23)

$[\vec{P}_n]^{S(l,n)}=[\vec{Q}_{l,n}^{(i)}]^{S(l,n)}+\vec{R}_{l,n}^{(i)},$ (24)

where the vectors and $\vec{R}_{l,n}^{(i)}$ and $\vec{Q}_{l,n}^{(i)}$ represent all the R and Q messages in each non-zero block of the H matrix, s(l,n) denotes the shift coefficient for the i^{th} block row and n^{th} non-zero block of the H matrix (note that null blocks in the H matrix need not be processed); $[\vec{R}_{l,n}^{i-1}]^{S(l,n)}$ denotes that the vector is cyclically shifted up by the amount s(l,n) and k is the check-node degree of the block row or the layer. A negative sign on s(l,n) indicates that it is cyclic down shift (equivalent cyclic left shift). $f(\cdot)$ denotes the check-node processing, which can be performed using BCJR, SP or MS.

Layered Decoder Presentation at 3

For the irregular block LDPC codes, the TDMP algorithm can be described with equations (21)-(24):

$\vec{R}_{l,n}^{(0)}=0, \vec{P}_n=\vec{L}_n^{(0)}$ [Initialization for each new received data frame], (21)

$\forall i=1,2,\cdots,it_{max}$ [Iteration loop],

$\forall l=1,2,\cdots,j$ [Sub-iteration loop],

$\forall n=1,2,\cdots,k$ [Block column loop],

$[\vec{Q}_{l,n}^{(i)}]^{S(l,n)}=[\vec{P}_n]^{S(l,n)}-\vec{R}_{l,n}^{(i-1)}$, (22)

$\vec{R}_{l,n}^{(i)}=f([\vec{Q}_{l,n'}^{(i)}]^{S(l,n')}, \forall n'=1,2,\cdots,k)$, (23)

$[\vec{P}_n]^{S(l,n)}=[\vec{Q}_{l,n}^{(i)}]^{S(l,n)}+\vec{R}_{l,n}^{(i)}$, (24)

where the vectors $\vec{R}_{l,n}^{(i)}$ and $\vec{Q}_{l,n}^{(i)}$ represent all the R and Q messages in each non-zero block of the H matrix, $s(l,n)$ denotes the shift coefficient for the l^{th} block row and n^{th} non-zero block of the H matrix (note that null blocks in the H matrix need not be processed); $[\vec{R}_{l,n}^{i-1}]^{S(l,n)}$ denotes that the vector $\vec{R}_{l,n}^{i-1}$ is cyclically shifted up by the amount $s(l,n)$, and k is the check-node degree of the block row or the layer. A negative sign on $s(l,n)$ indicates that it is cyclic down shift (equivalent cyclic left shift). $f(\cdot)$ denotes the check-node processing.

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204. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include wherein the LDPC matrix comprises a plurality of layers, each layer having a plurality of blocks ordered such that the sequence of non-zero blocks of the given layer of the LDPC matrix specifies a first set of non-zero blocks of the given layer to be processed at a given time and a second set of non-zero blocks of the given layer to be processed after the first set of non-zero blocks. For example, upon information and belief, the Spyder product includes a layered decoder wherein each layer of the LDPC matrix is constructed such that non-zero blocks that are not dependent on the previous layer occur at earlier locations in the layer than non-zero blocks that are dependent on the previous layer. Further, upon information and belief, non-zero blocks of a given layer of the LDPC matrix in the layered decoder of the Spyder product are processed in the order in which they occur in the layer.

205. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include wherein the first set specifies only non-zero blocks of the given layer that are not dependent on a result of a previously processed layer and the second

set specifies non-zero blocks of the given layer that are dependent on a result of the previously processed layer. For example, upon information and belief, the Spyder product includes a layered decoder wherein each layer of the LDPC matrix is constructed such that non-zero blocks that are not dependent on the previous layer occur at earlier locations in the layer than non-zero blocks that are dependent on the previous layer.

206. In view of the foregoing, the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products directly infringe at least Claims 13-20, 22-23, and 25-31 of the '530 Patent.

207. On information and belief, Defendants and/or the Broadcom Predecessor Entities have had actual or constructive knowledge of the '530 Patent since at least August 18, 2015.

208. Defendants and/or the Broadcom Predecessor Entities further have had knowledge of the '530 Patent at least as early as the filing and/or service of Plaintiff's original Complaint. (*See* D.I. 1, 5) Defendants and/or the Broadcom Predecessor Entities have further been aware that use of the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products necessarily practice the inventions in Claims 13-20, 22-23, and 25-31 of the '530 Patent.

209. On information and belief, Defendants and/or the Broadcom Predecessor Entities have taken active steps to induce infringement by others of at least Claims 13-20, 22-23, and 25-31 of the '530 Patent in violation of 35 U.S.C. §271(b), including, for example, by (a) inducing manufacturers to practice the claims, and (b) inducing end users to practice the claims. Such active steps include, but are not limited to, selling Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products with the knowledge and intent that the Accused Products will be used, imported, or operated in violation of the '530 Patent, as

set forth in the Section "EXAMPLES OF DIRECT AND INDIRECT INFRINGEMENT" below.

210. On information and belief, Defendants and/or the Broadcom Predecessor Entities have known or should have known that such activities induce others to directly infringe one or more of at least Claims 13-20, 22-23, and 25-31 of the '530 Patent. For example, Defendants and/or the Broadcom Predecessor Entities should have known that their actions induced others to directly infringe as of the date it became aware of the issuance of the '530 Patent on or about August 18, 2015, and in any event no later than the date of service of Plaintiff's original complaint, as set forth in the Section "EXAMPLES OF DIRECT AND INDIRECT INFRINGEMENT" below. (*See* D.I. 1, 5)

211. Defendants and/or the Broadcom Predecessor Entities were further informed that the technology in the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products infringed the '530 Patent, and Defendants and/or the Broadcom Predecessor Entities have knowingly and purposefully continued to exploit the patented technology despite knowing that it was covered by the '530 Patent. Defendants and/or the Broadcom Predecessor Entities are further aware that the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products necessarily practice Claims 13-20, 22-23, and 25-31 of the '530 Patent.

212. On information and belief, Defendants and/or the Broadcom Predecessor Entities have contributed to the infringement of at least Claims 13-20, 22-23, and 25-31 of the '530 Patent by others, including consumer/end-user sale, importation, or use of the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products, in violation of 35 U.S.C. § 271(c). Acts by Defendants and/or the Broadcom Predecessor Entities

that contribute to the infringement by others include, but are not limited to, the sale, offer for sale, and/or import by Defendants and/or the Broadcom Predecessor Entities of the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products. Such Accused Hard Disk Controller Products, Accused SandForce Products, and Accused Densbits Products are especially made for or adapted for use to infringe, and are not a staple article of commerce and are not suitable for substantial non-infringing use. As also described above, Defendants and/or the Broadcom Predecessor Entities have, on information and belief, been on notice of the '530 Patent since at least the filing of Plaintiff's original Complaint and likely at or near its issuance in view of the knowledge set forth above regarding the '530 Patents' related patents. (*See* D.I. 1, 5) Defendants and/or the Broadcom Predecessor Entities are further aware that the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products necessarily practice Claims 13-20, 22-23, and 25-31 of the '530 Patent.

213. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products are especially made for or adapted for use to infringe, and are not a staple article of commerce and are not suitable for substantial non-infringing use. By way of example, the use of the LDPC decoders included in the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products is necessary to use the accused products for their intended purpose (decoding data from a hard disk drive, solid state drive, or wireless digital transmission), and the LDPC decoders necessarily perform the claimed inventions when they decode data. Accordingly, the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products do not have a substantial use that does not entail practicing the claimed inventions. On information and belief,

the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products cannot be used but to infringe the ’530 Patent.

214. Despite Defendants’ and/or the Broadcom Predecessor Entities’ knowledge, notice, and ongoing infringement of the ’530 Patent, Defendants and/or the Broadcom Predecessor Entities continue to sell, offer for sale, important, test, or use the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products in a manner that willfully infringes the ’530 Patent, and on information and belief continue to sell and/or offer for sale the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products to the United States market for customers / end users to infringe. Defendants’ and/or the Broadcom Predecessor Entities’ infringement of the ’530 Patent is willful, as set forth above. Defendants and/or the Broadcom Predecessor Entities lacked a justifiable belief that they do not infringe the ’530 Patent, or that the ’530 Patent is invalid or unenforceable, and have acted recklessly in its their infringing activity, justifying an increase in the damages to be awarded to Plaintiff up to three times the amount found or assessed, in accordance with 35 U.S.C. § 284.

215. This case is rendered an exceptional case at least in light of Defendants’ and/or the Broadcom Predecessor Entities’ willful infringement of the ’530 Patent, justifying an award to Plaintiff of its reasonable attorney fees, in accordance with 35 U.S.C. § 285.

216. Plaintiff has no adequate remedy at law for Defendants’ and/or the Broadcom Predecessor Entities’ acts of infringement. As a direct and proximate result of Defendants’ and/or the Broadcom Predecessor Entities’ acts of infringement, Plaintiff has suffered and continues to suffer damages and irreparable harm. Unless Defendants’ and/or the Broadcom

Predecessor Entities' acts of infringement are enjoined by this Court, Plaintiff will continue to be damaged and irreparably harmed.

217. Defendants' and/or the Broadcom Predecessor Entities' infringement of the '530 Patent has damaged and continues to damage Plaintiff in an amount yet to be determined, of at least a reasonable royalty and/or lost profits that Plaintiff would have made but for Defendants' and/or the Broadcom Predecessor Entities' infringement acts.

COUNT IV
(Infringement under 35 U.S.C. § 271 of U.S. Patent No. 8,359,522)

218. Plaintiff repeats and re-alleges the paragraphs above as if fully set forth herein.

219. The '522 Patent is valid, enforceable, and was duly issued on January 22, 2013 in full compliance with Title 35 of the United States Code.

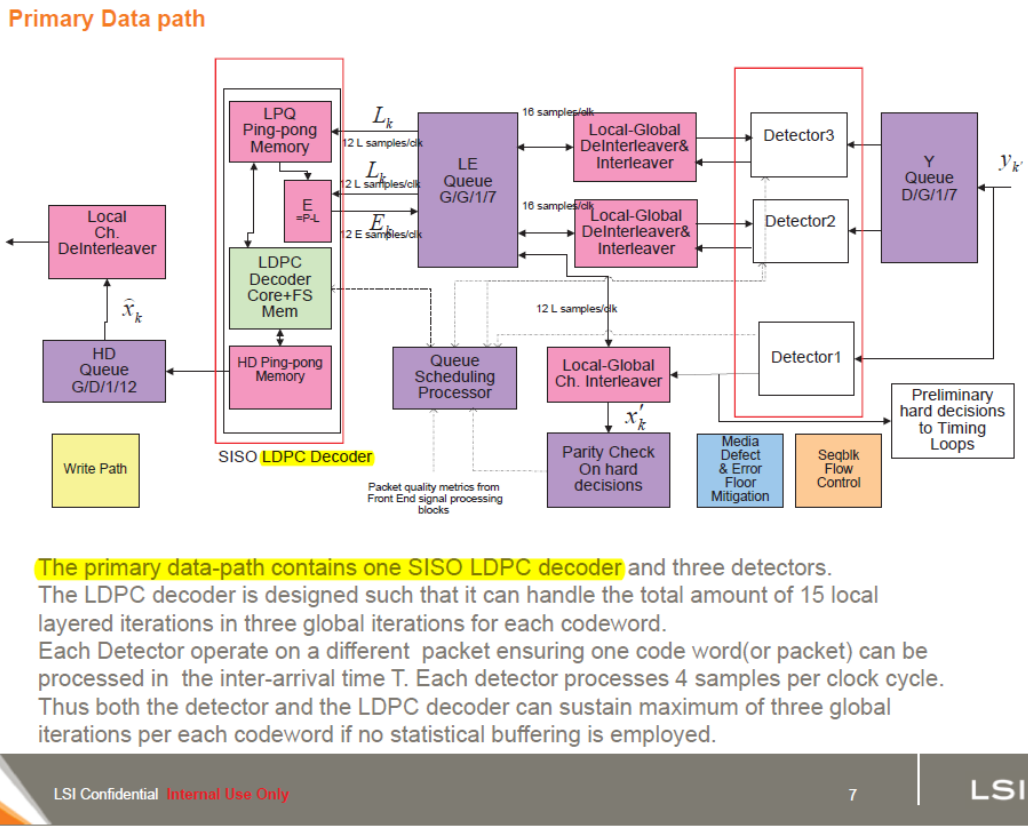
220. On information and belief, in violation of 35 U.S.C. § 271, Defendants and/or the Broadcom Predecessor Entities have infringed, contributed to the infringement of, and/or induced others to infringe the '522 Patent, either literally or under the doctrine of equivalents, by, among other things, making, using, offering for sale, selling, selling infringing products abroad with knowledge and intent that the infringing products be imported into the United States by others, and/or importing into the United States unlicensed systems and/or products in a manner that infringes at least Claims 85-97 of the '522 Patent.

221. On information and belief, Defendants and/or the Broadcom Predecessor Entities have directly infringed the '522 Patent, for example, by making, using, selling, offering to sell, and/or importing into the United States the Accused Products, which meet each and every limitation of at least Claim 85 of the '522 Patent, in violation of Plaintiff's patent rights and without Plaintiff's license or authority. Non-limiting examples of such infringement are provided below, based on the limited information currently available to Plaintiff.

222. Claim 85 of the '522 Patent recites as follows:

> 85. A method for decoding a low density parity check code, comprising:
> selecting a first R message from a plurality of previously generated possible R messages based on at least a message index value and a sign bit;
> generating a Q message by combining the first R message with a P message;
> cyclically shifting the P message; and
> updating the P message responsive to determination of a final state for each block row.

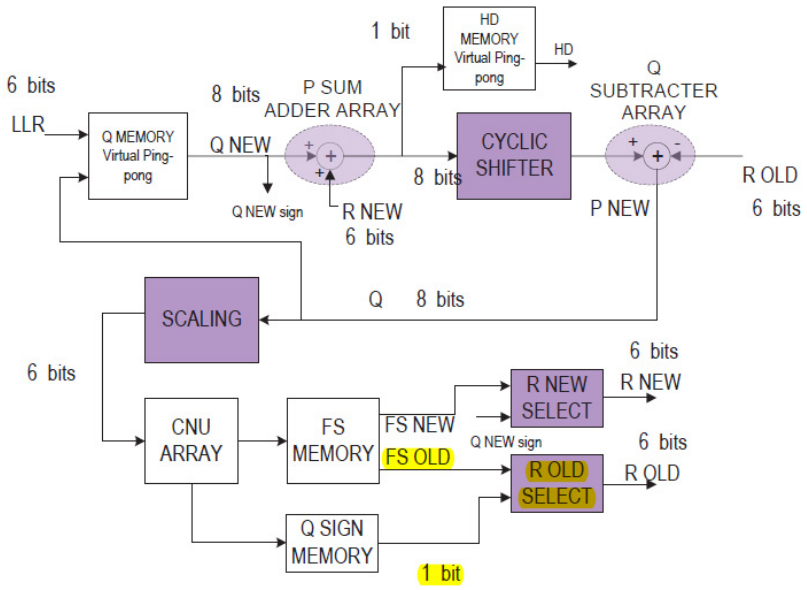
223. On information and belief, the Accused Products satisfy each and every limitation of Claim 85. The Accused Products decode a low density parity check code. For example, with respect to the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products, the McLaren Architecture Presentation references the LDPC decoder.

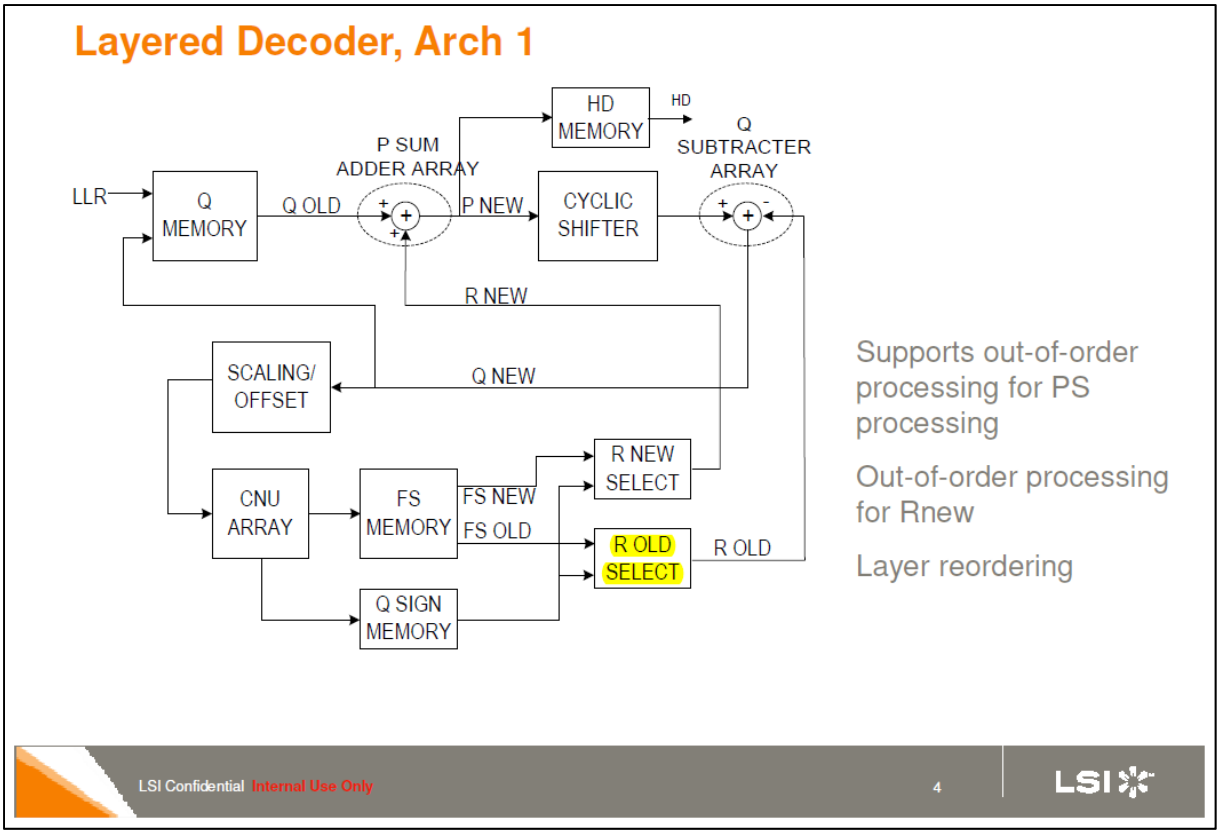


With respect to the Accused Wi-Fi Products, the '489 patent, titled "Permuted Accelerated LDPC (Low Density Parity Check) Decoder," discloses that its "decoding approach operates by processing, in parallel, selected rows for multiple individual LDPC matrix rows from various sub-matrix rows (e.g., first group of rows from a first sub-matrix row, second group of rows from a second sub-matrix row, etc.)."

224. The Accused Products select a first R message from a plurality of previously generated possible R messages based on at least a message index value and a sign bit. For example, with respect to the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products, the McLaren Architecture Presentation and the Layered Decoder Presentation each disclose the presence of an R OLD SELECT unit that selects a first R message from a plurality of previously generated possible R messages based on at least a message index value and a sign bit.

Layered Decoder Structure





With respect to the Accused Wi-Fi Products, they perform the LDPC decoding method described in the '489 patent which includes, for example, generating updated check edge message (λ) values from prior values, such as described, for example, in FIG. 10 (reproduced below) and the accompanying disclosure. Upon information and belief, those updated check edge message (λ) values are based on at least a message index value and a sign bit. *See also* ¶ 155, *supra*, describing correlation between variables λ, γ, and (γ−λ) in the Broadcom '488 and '489 patents with R, P, and Q messages in Patents-in-Suit.

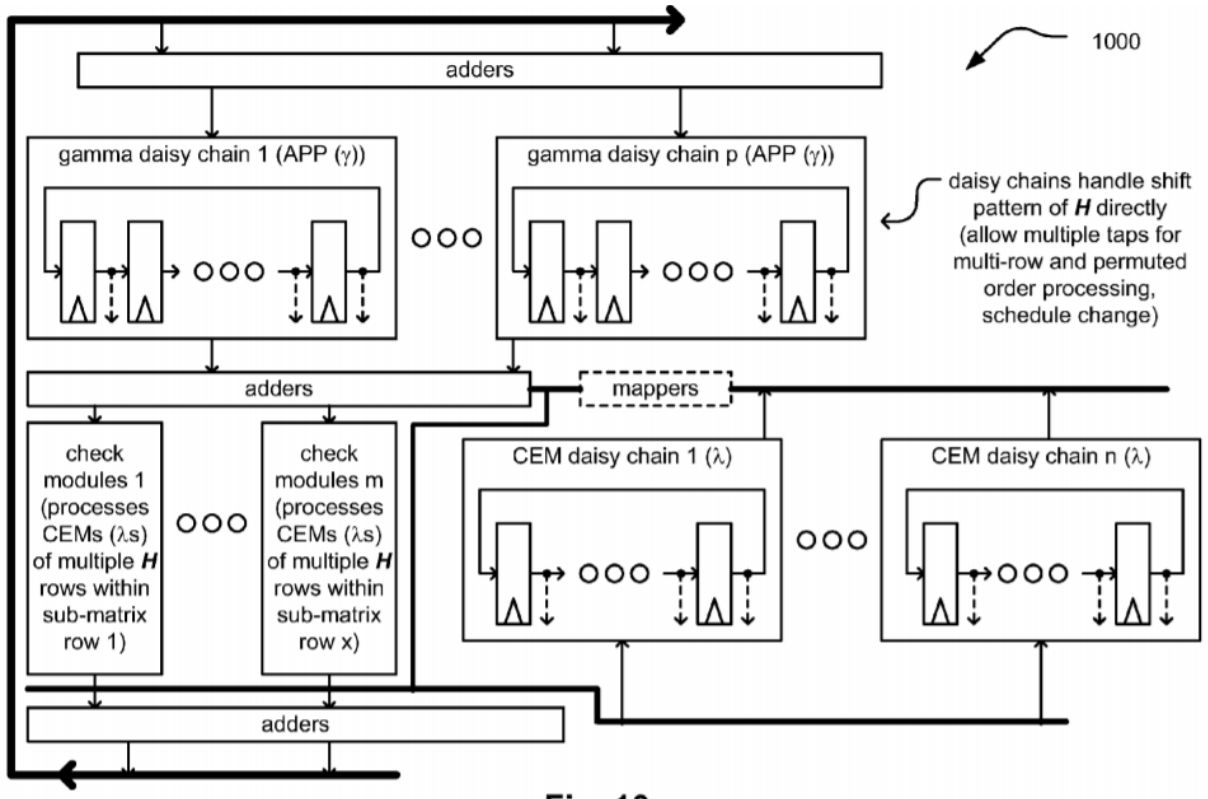
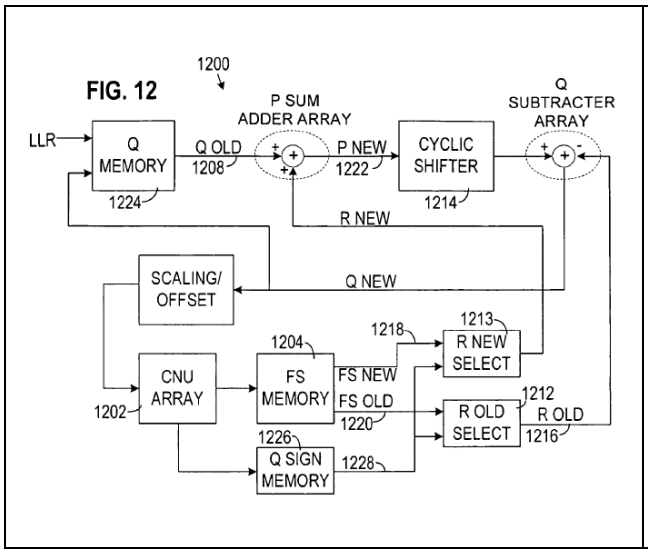
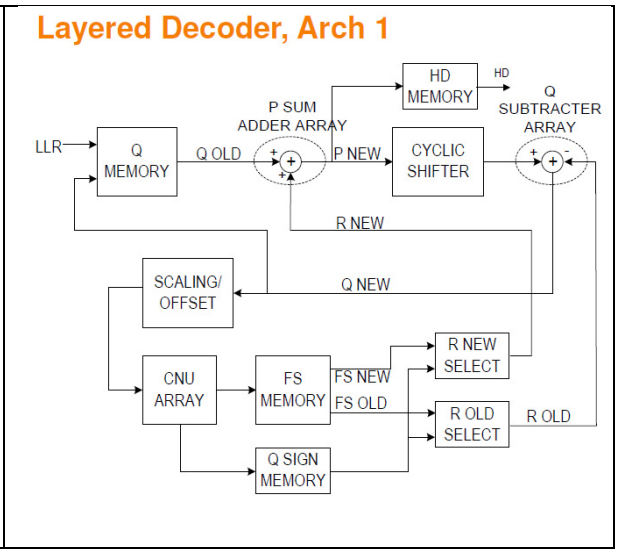


Fig. 10

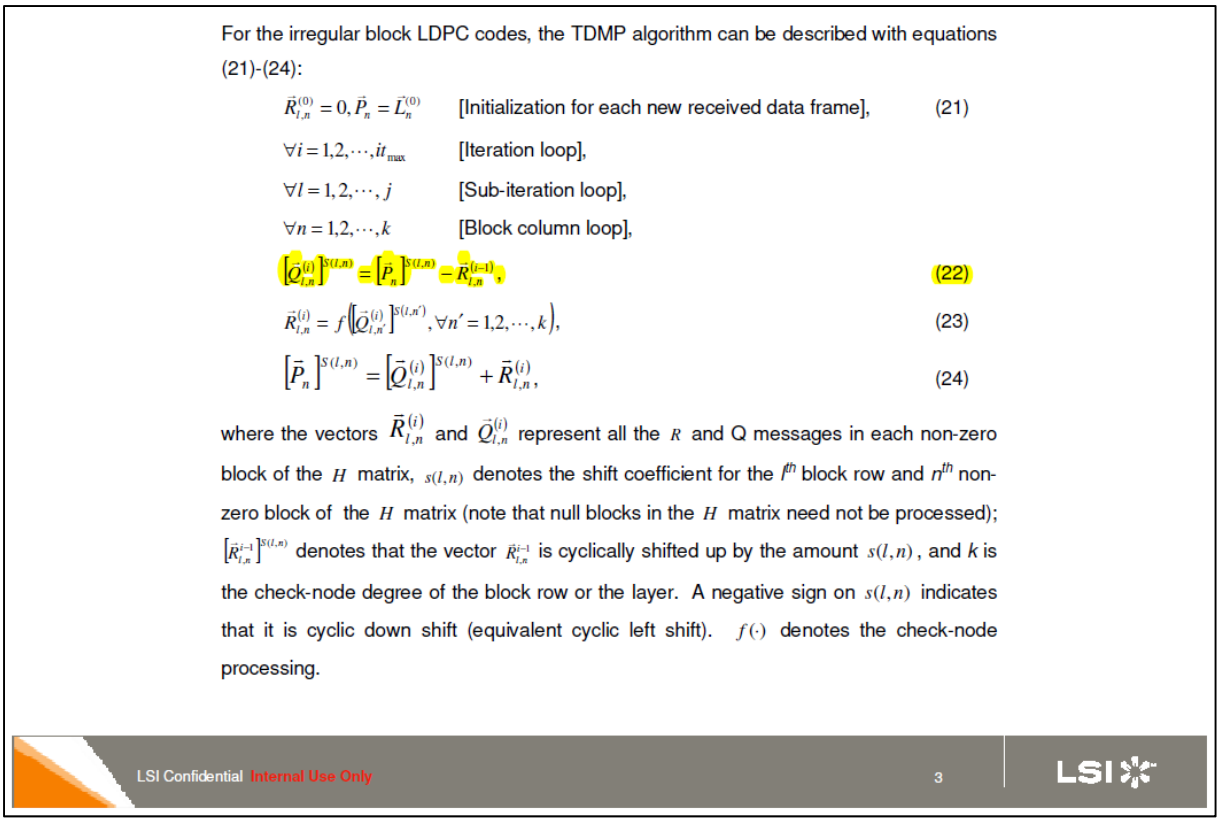
225. The layered decoder architecture of the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products is identical to what is set forth in the '522 Patent.

'522 Patent at FIG. 12 | **Layered Decoder Presentation at 4**





226. The Accused Products generate a Q message by combining the first R message with a P message. For example, with respect to the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products, the Layered Decoder Presentation discloses a Q SUBTRACTER ARRAY that generates a Q message by combining the first R message with a P message.



For the irregular block LDPC codes, the TDMP algorithm can be described with equations (21)-(24):

$\vec{R}_{l,n}^{(0)} = 0, \vec{P}_n = \vec{L}_n^{(0)}$ [Initialization for each new received data frame], (21)

$\forall i = 1,2,\cdots,it_{\max}$ [Iteration loop],

$\forall l = 1,2,\cdots,j$ [Sub-iteration loop],

$\forall n = 1,2,\cdots,k$ [Block column loop],

$$\left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n)} = \left[\vec{P}_n\right]^{S(l,n)} - \vec{R}_{l,n}^{(i-1)}, \quad (22)$$

$$\vec{R}_{l,n}^{(i)} = f\left(\left[\vec{Q}_{l,n'}^{(i)}\right]^{S(l,n')}, \forall n' = 1,2,\cdots,k\right), \quad (23)$$

$$\left[\vec{P}_n\right]^{S(l,n)} = \left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n)} + \vec{R}_{l,n}^{(i)}, \quad (24)$$

where the vectors $\vec{R}_{l,n}^{(i)}$ and $\vec{Q}_{l,n}^{(i)}$ represent all the R and Q messages in each non-zero block of the H matrix, $s(l,n)$ denotes the shift coefficient for the l^{th} block row and n^{th} non-zero block of the H matrix (note that null blocks in the H matrix need not be processed); $\left[\vec{R}_{l,n}^{i-1}\right]^{S(l,n)}$ denotes that the vector $\vec{R}_{l,n}^{i-1}$ is cyclically shifted up by the amount $s(l,n)$, and k is the check-node degree of the block row or the layer. A negative sign on $s(l,n)$ indicates that it is cyclic down shift (equivalent cyclic left shift). $f(\cdot)$ denotes the check-node processing.

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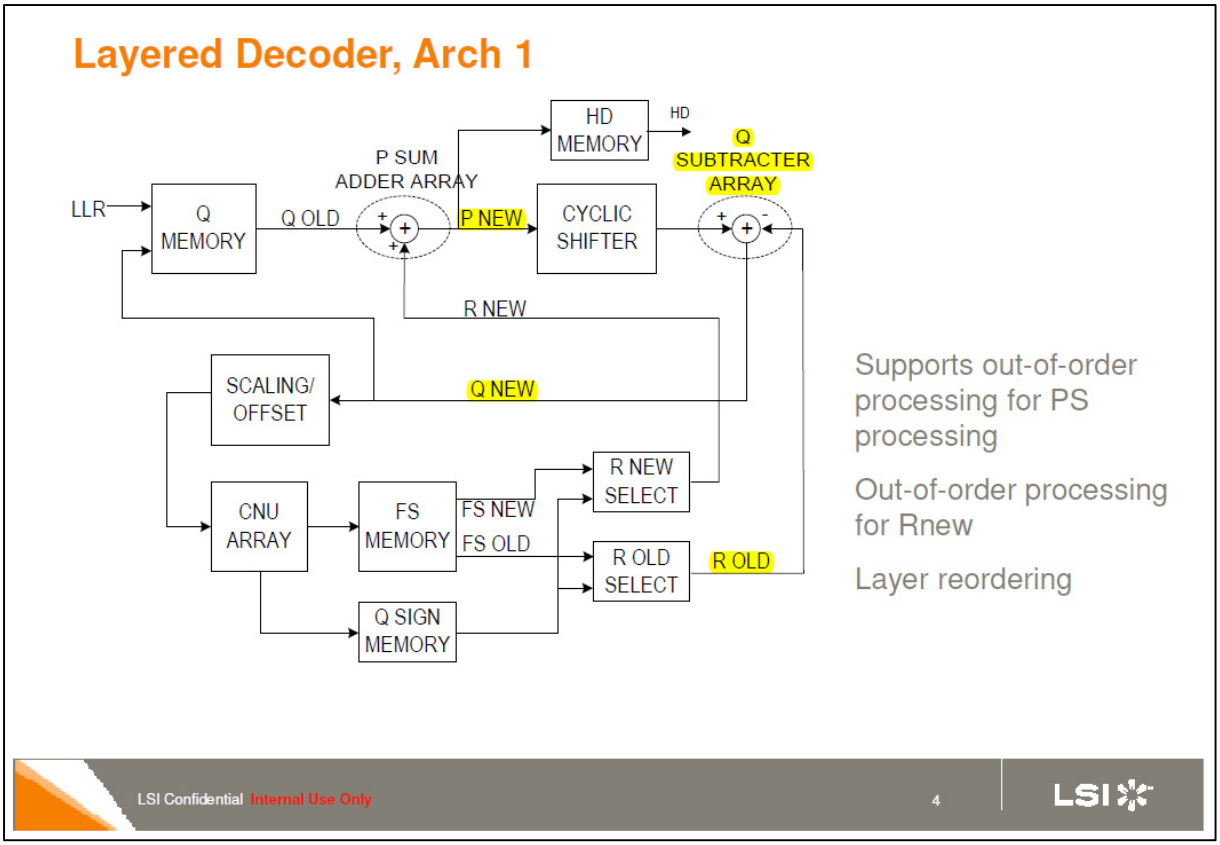


With respect to the Accused Wi-Fi Products, they perform the LDPC decoding method described in the '489 patent which provides, for example, that input values to the check modules are generated by combining the check edge message/intrinsic information (λ) values with APP (or gamma(γ)) values in accordance with the permuted accelerated decoding architecture such as described in FIG. 10 (reproduced at ¶ 208, *supra*) and the accompanying disclosure.

227. The TDMP algorithm equations of the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products are identical to what is set forth in the '522 Patent.

'522 Patent at 15:23–50

For the irregular block LDPC codes, the TDMP algorithm can be described with equations (21)-(24):

$\vec{R}_{l,n}^{(0)}=0, \vec{P}_n=\vec{L}_n^{(0)}$ [Initialization for each new received data frame],

$\forall i=1,2,\ldots,it_{max}$ [Iteration loop],

$\forall l=1,2,\ldots,j$ [Sub-iteration loop],

$\forall n=1,2,\ldots,k$ [Block column loop], (21)

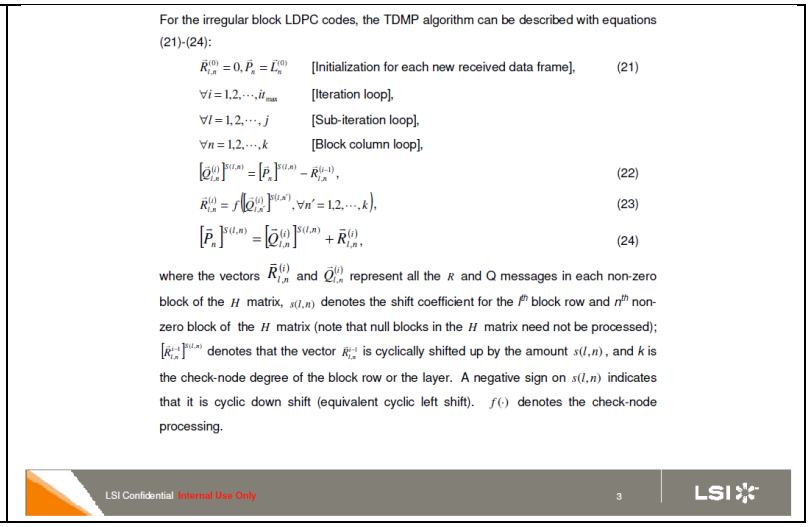
$[\vec{Q}_{l,n}^{(i)}]^{S(l,n)}=[\vec{P}_n]^{S(l,n)}-\vec{R}_{l,n}^{(i-1)}$, (22)

$\vec{R}_{l,n}^{(i)}=f([\vec{Q}_{l,n}^{(i)}]^{S(l,n')}), \forall n'=1,2,\ldots,k)$, (23)

$[\vec{P}_n]^{S(l,n)}=[\vec{Q}_{l,n}^{(i)}]^{S(l,n)}+\vec{R}_{l,n}^{(i)}$, (24)

where the vectors $\vec{R}_{l,n}^{(i)}$ and $\vec{Q}_{l,n}^{(i)}$ represent all the R and Q messages in each non-zero block of the H matrix, s(l,n) denotes the shift coefficient for the l^{th} block row and n^{th} non-zero block of the H matrix (note that null blocks in the H matrix need not be processed); $[\vec{R}_{l,n}^{i-1}]^{S(l,n)}$ denotes that the vector $\vec{R}_{l,n}^{i-1}$ is cyclically shifted up by the amount s(l,n), and k is the check-node degree of the block row or the layer. A negative sign on s(l,n) indicates that it is cyclic down shift (equivalent cyclic left shift). f(•) denotes the check-node processing, which can be performed using BCJR, SP or MS.

Layered Decoder Presentation at 3



For the irregular block LDPC codes, the TDMP algorithm can be described with equations (21)-(24):

$\vec{R}_{l,n}^{(0)}=0, \vec{P}_n=\vec{L}_n^{(0)}$ [Initialization for each new received data frame], (21)

$\forall i=1,2,\cdots,it_{max}$ [Iteration loop],

$\forall l=1,2,\cdots,j$ [Sub-iteration loop],

$\forall n=1,2,\cdots,k$ [Block column loop],

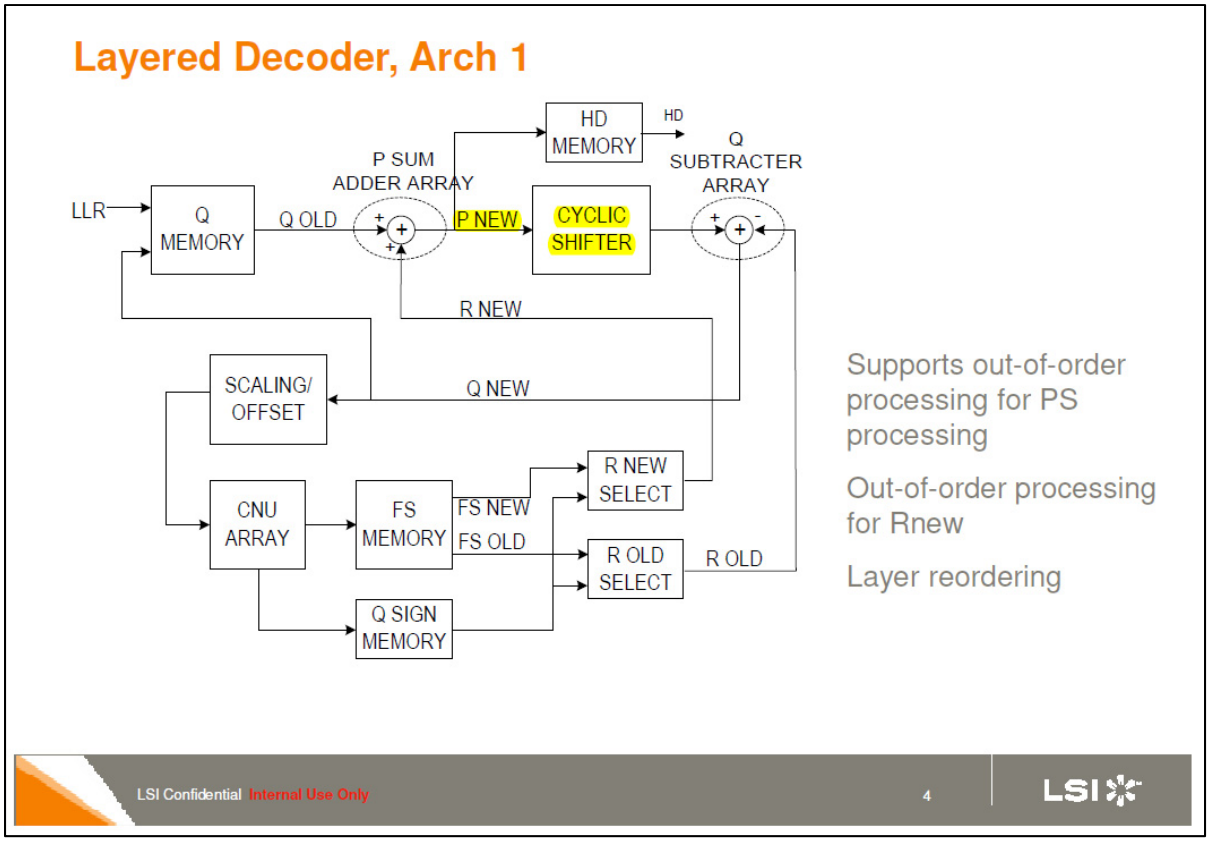
$\left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n)}=\left[\vec{P}_n\right]^{S(l,n)}-\vec{R}_{l,n}^{(i-1)}$, (22)

$\vec{R}_{l,n}^{(i)}=f\left(\left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n')}, \forall n'=1,2,\cdots,k\right)$, (23)

$\left[\vec{P}_n\right]^{S(l,n)}=\left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n)}+\vec{R}_{l,n}^{(i)}$, (24)

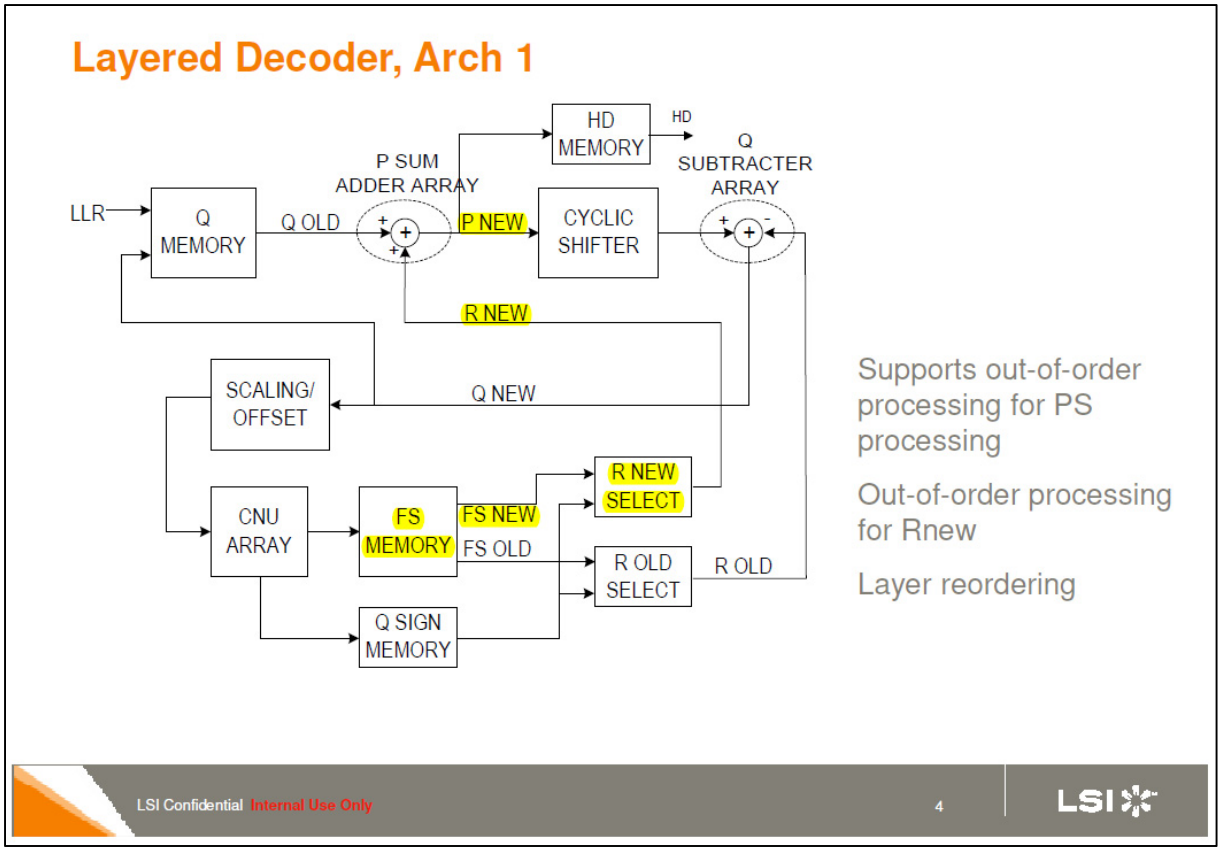
where the vectors $\vec{R}_{l,n}^{(i)}$ and $\vec{Q}_{l,n}^{(i)}$ represent all the R and Q messages in each non-zero block of the H matrix, $s(l,n)$ denotes the shift coefficient for the l^{th} block row and n^{th} non-zero block of the H matrix (note that null blocks in the H matrix need not be processed); $[\vec{R}_{l,n}^{i-1}]^{S(l,n)}$ denotes that the vector $\vec{R}_{l,n}^{i-1}$ is cyclically shifted up by the amount $s(l,n)$, and k is the check-node degree of the block row or the layer. A negative sign on $s(l,n)$ indicates that it is cyclic down shift (equivalent cyclic left shift). $f(\cdot)$ denotes the check-node processing.

228. The Accused Products cyclically shift the P message. For example, with respect to the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products, the Layered Decoder Presentation discloses a CYCLIC SHIFTER that shifts the P Message.



With respect to the Accused Wi-Fi Products, they perform the LDPC decoding method described in the '489 patent in which the APP (or gamma(γ)) values are cyclically shifted via APP (or gamma(γ)) daisy chains (shown as gamma daisy chain 1 (APP(γ)) to gamma daisy chain p (APP(γ)) as described, for example, in FIG. 10 (reproduced at ¶ 208, *supra*) and the corresponding disclosure. FIG. 10 notes specifically that "daisy chains handle shift pattern of *H* directly (allow multiple taps for multi-row and permuted order processing, schedule change)."

229. The Accused Products update the P message responsive to determination of a final state for each block row. For example, with respect to Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products, the Layered Decoder Presentation discloses that for each block row, each P message is a function of R NEW, and R NEW is based on a determination of a final state for the row.



With respect to the Accused Wi-Fi Products, they perform the LDPC decoding method described in the '489 patent in which the APP (or gamma(γ)) values are computed based on check edge message/intrinsic information (λ) values of sub-matrix rows of the LDPC matrix (which in turn depend on the final state for each block row), such as described, for example, in FIG. 10 (reproduced at ¶ 208, *supra*) and the corresponding disclosure.

230. In view of the foregoing, the Accused Products directly infringe at least Claims 85-97 of the '522 Patent through Defendants' and/or the Broadcom Predecessor Entities' internal use and testing of the Accused Products.

231. On information and belief, Defendants and/or the Broadcom Predecessor Entities had actual or constructive knowledge of the '522 Patent since at least January 22, 2013.

232. Defendants and/or the Broadcom Predecessor Entities further have had knowledge of the '522 Patent at least as early as the filing and/or service of Plaintiff's original Complaint. (*See* D.I. 1, 5) Defendants and/or the Broadcom Predecessor Entities are further aware that the Accused Products necessarily practice Claims 85-97 of the '522 Patent.

233. On information and belief, Defendants and/or the Broadcom Predecessor Entities have taken active steps to induce infringement by others of at least Claims 85-97 of the '522 Patent in violation of 35 U.S.C. §271(b), including, for example, by (a) inducing manufacturers to perform the claimed inventions when testing the Accused Products, and (b) inducing end users to perform the claimed inventions when using the Accused Products. Such active steps include, but are not limited to, selling Accused Products with the knowledge and intent that the Accused Products will be operated by such manufacturers and their customers in accordance with the claimed inventions, as set forth in the Section "EXAMPLES OF DIRECT AND INDIRECT INFRINGEMENT" below.

234. On information and belief, Defendants and/or the Broadcom Predecessor Entities knew or should have known that such activities induce others to directly infringe one or more of at least Claims 85-97 of the '522 Patent. For example, Defendants and/or the Broadcom Predecessor Entities should have known that their actions induced others to directly infringe as of the date LSI became aware of the issuance of the '522 Patent on or about January 22, 2013, the date LSI was advised of the issuance of the '522 Patent by Dr. Gunnam. Defendants and/or the Broadcom Predecessor Entities were further informed that the technology in the Accused Products infringed the '522 Patent, and Defendants and/or the Broadcom Predecessor Entities knowingly and purposefully continued to exploit the patented technology despite knowing that it

was covered by the '522 Patent, as set forth in the Section "EXAMPLES OF DIRECT AND INDIRECT INFRINGEMENT" below.

235. On information and belief, Defendants and/or the Broadcom Predecessor Entities have contributed to the infringement of at least Claims 85-97 of the '522 Patent by others, including consumer/end-user use of the Accused Products, in violation of 35 U.S.C. § 271(c). Acts by Defendants and/or the Broadcom Predecessor Entities that contribute to the infringement of others include, but are not limited to, the sale, offer for sale, and/or import by Defendants and/or the Broadcom Predecessor Entities of the Accused Products. Such Accused Products are especially made for or adapted for use to infringe, and are not a staple article of commerce and are not suitable for substantial non-infringing use. The Accused Products are apparatuses for use in practicing the inventions patented in Claims 85-97 of the '522 Patent, and are at least a material part of those claimed inventions, for example, as described above with respect to Claim 85. On information and belief, the steps recited in Claim 85, for example, are performed by the Accused Products and as set forth in the Section "EXAMPLES OF DIRECT AND INDIRECT INFRINGEMENT" below..

236. As also described above, Defendants and/or the Broadcom Predecessor Entities have, on information and belief, been on notice of the '522 Patent since January 22, 2013 and in addition since filing and/or service of Plaintiff's original Complaint. (*See* D.I. 1, 5) Defendants and/or the Broadcom Predecessor Entities have further been aware that use of the Accused Products necessarily practice the inventions in Claims 85-97 of the '522 Patent.

237. The Accused Products are especially made for or adapted for use to infringe, and are not a staple article of commerce and are not suitable for substantial non-infringing use. By way of example, the use of the LDPC decoders included in the Accused Products is necessary to

use the accused products for their intended purpose (decoding data from a hard disk drive, solid state drive, or wireless digital transmission), and the LDPC decoders necessarily perform the claimed inventions when they decode data. Accordingly, the Accused Products do not have a substantial use that does not entail practicing the claimed inventions. On information and belief, the Accused Products cannot be used but to infringe the '522 Patent.

238. Despite Defendants' and/or the Broadcom Predecessor Entities' knowledge, notice, and ongoing infringement of the '522 Patent, Defendants and/or the Broadcom Predecessor Entities continue to test or use the Accused Products in a manner that willfully infringes the '522 Patent, and on information and belief continue to sell and/or offer for sale the Accused Products to the United States market for customers / end users to infringe. Defendants' and/or the Broadcom Predecessor Entities' infringement of the '522 Patent is willful, as set forth above. Defendants and/or the Broadcom Predecessor Entities lacked a justifiable belief that they do not infringe the '522 Patent, or that the '522 Patent is invalid or unenforceable, and have acted recklessly in their infringing activity, justifying an increase in the damages to be awarded to Plaintiff up to three times the amount found or assessed, in accordance with 35 U.S.C. § 284.

239. This case is rendered an exceptional case at least in light of Defendants' and/or the Broadcom Predecessor Entities' willful infringement of the '522 Patent, justifying an award to Plaintiff of its reasonable attorney fees, in accordance with 35 U.S.C. § 285.

240. Plaintiff has no adequate remedy at law for Defendants' and/or the Broadcom Predecessor Entities' acts of infringement. As a direct and proximate result of Defendants' and/or the Broadcom Predecessor Entities' acts of infringement, Plaintiff has suffered and continues to suffer damages and irreparable harm. Unless Defendants' and/or the Broadcom

Predecessor Entities' acts of infringement are enjoined by this Court, Plaintiff will continue to be damaged and irreparably harmed.

241. Defendants' and/or the Broadcom Predecessor Entities' infringement of the '522 Patent has damaged and continues to damage Plaintiff in an amount yet to be determined, of at least a reasonable royalty and/or lost profits that Plaintiff would have made but for Defendants' and/or the Broadcom Predecessor Entities' infringing acts.

COUNT V
(Infringement under 35 U.S.C. § 271 of U.S. Patent No. 8,656,250)

242. Plaintiff repeats and re-alleges the paragraph above as if fully set forth herein.

243. The '250 Patent is valid, enforceable, and was duly issued on February 18, 2014 in full compliance with Title 35 of the United States Code.

244. On information and belief, in violation of 35 U.S.C. § 271, Defendants and/or the Broadcom Predecessor Entities have infringed, contributed to the infringement of, and/or induced others to infringe the '250 Patent, either literally or under the doctrine of equivalents, by, among other things, making, using, offering for sale, selling, selling infringing products abroad with knowledge and intent that the infringing products be imported into the United States by others, and/or importing into the United States unlicensed systems and/or products in a manner that infringes at least Claims 1-20, 25, 27-28, 31-35, 37, 38, 41, 44, and 46 of the '250 Patent.

245. On information and belief, Defendants and/or the Broadcom Predecessor Entities have directly infringed the '250 Patent, for example, by making, using, selling, offering to sell, and/or importing into the United States the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products, which meet each and every limitation of at least Claim 1 of the '250 Patent, in violation of Plaintiff's patent rights and without

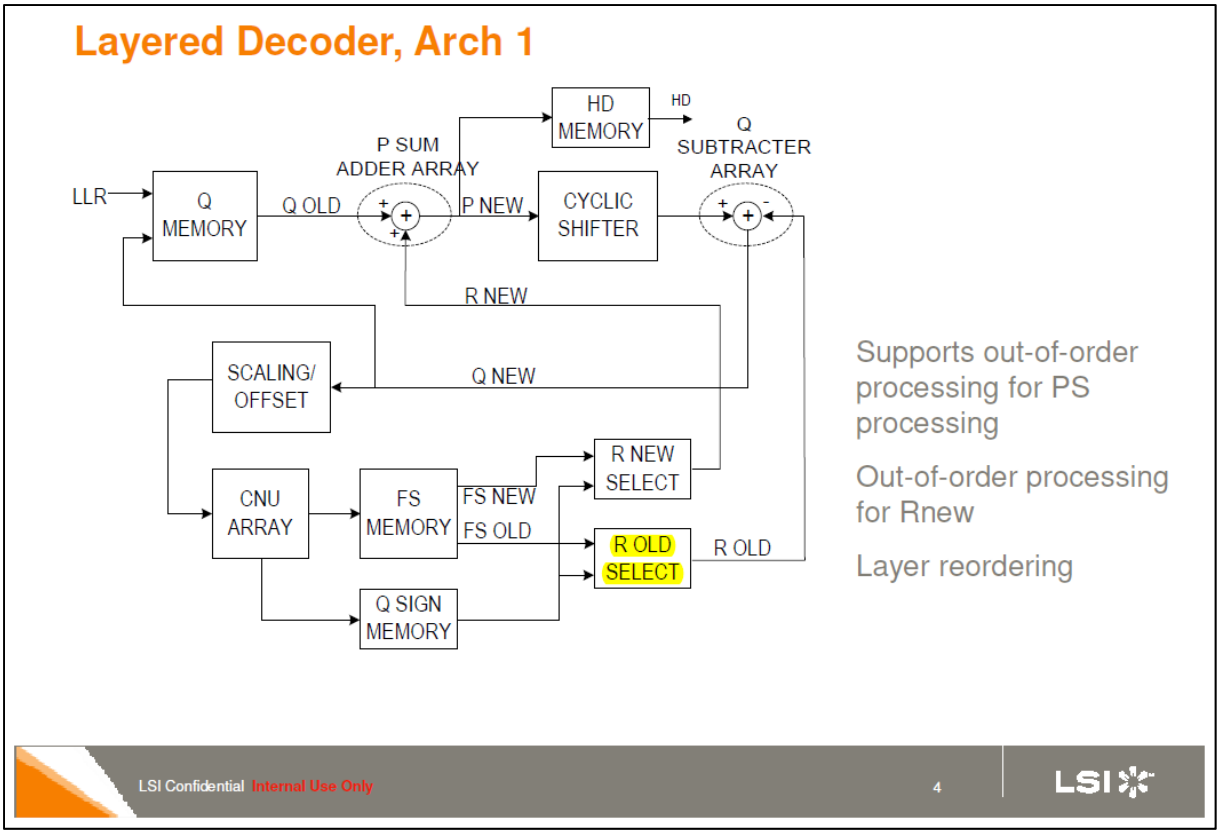
Plaintiff's license or authority. Non-limiting examples of such infringement are provided below, based on the limited information currently available to Plaintiff.

246. Claim 1 of the '250 Patent recites as follows:

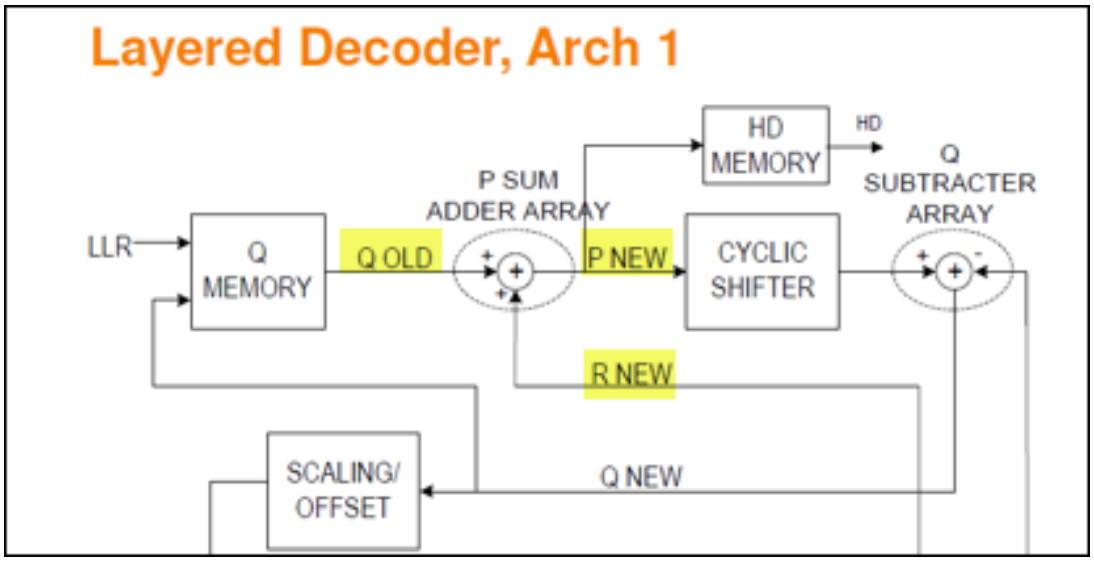
> A low density parity check (LDPC) code decoder, comprising:
> an R select unit that provides an R message by selecting from a plurality of possible R message values;
> a Q message memory that stores a Q message until an R message is generated by the R select unit, the Q message and the R message are combined to provide a P message; and
> a permuter that permutes the P message;
> wherein the permuter permutes the P message by the difference of the permutation of a block currently being processed and the permutation of a block previously processed; wherein the block currently being processed and the block previously processed are in a same block column.

247. On information and belief, the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products satisfy each and every limitation of Claim 1. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products decode a low density parity check code. For example, the McLaren Architecture Presentation references the LDPC decoder, as set forth above.

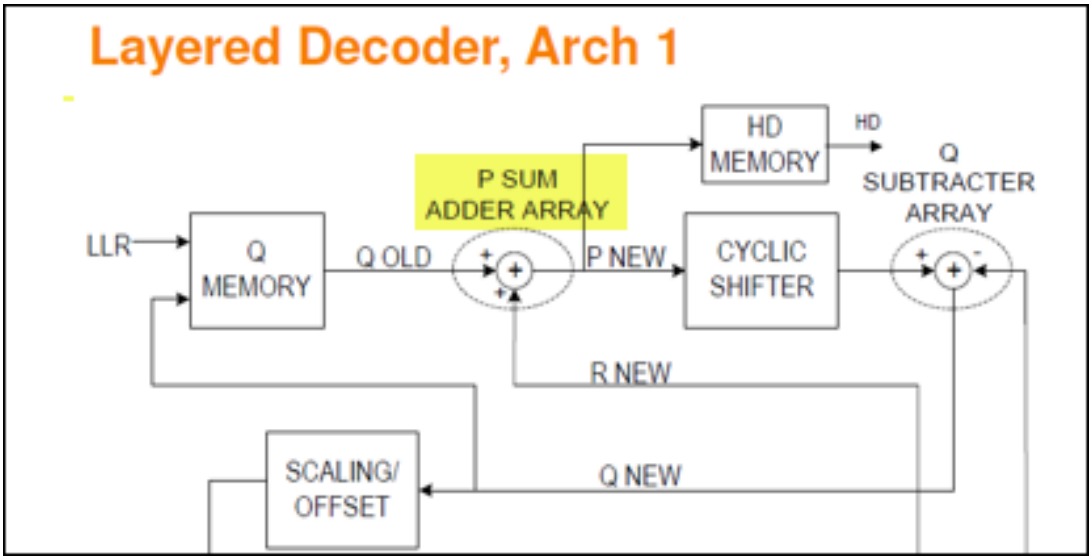
248. On information and belief, the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include an R select unit that provides an R message by selecting from a plurality of possible R message values. For example, the McLaren Architecture Presentation and the Layered Decoder Presentation each disclose the presence of an R NEW SELECT unit that selects a first R message from a plurality of previously generated possible R messages based on at least a message index value and a sign bit.



249. On information and belief, the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include a Q message memory (shown above) that stores a Q message until an R message is generated by the R select unit, the Q message and the R message are combined to provide a P message:

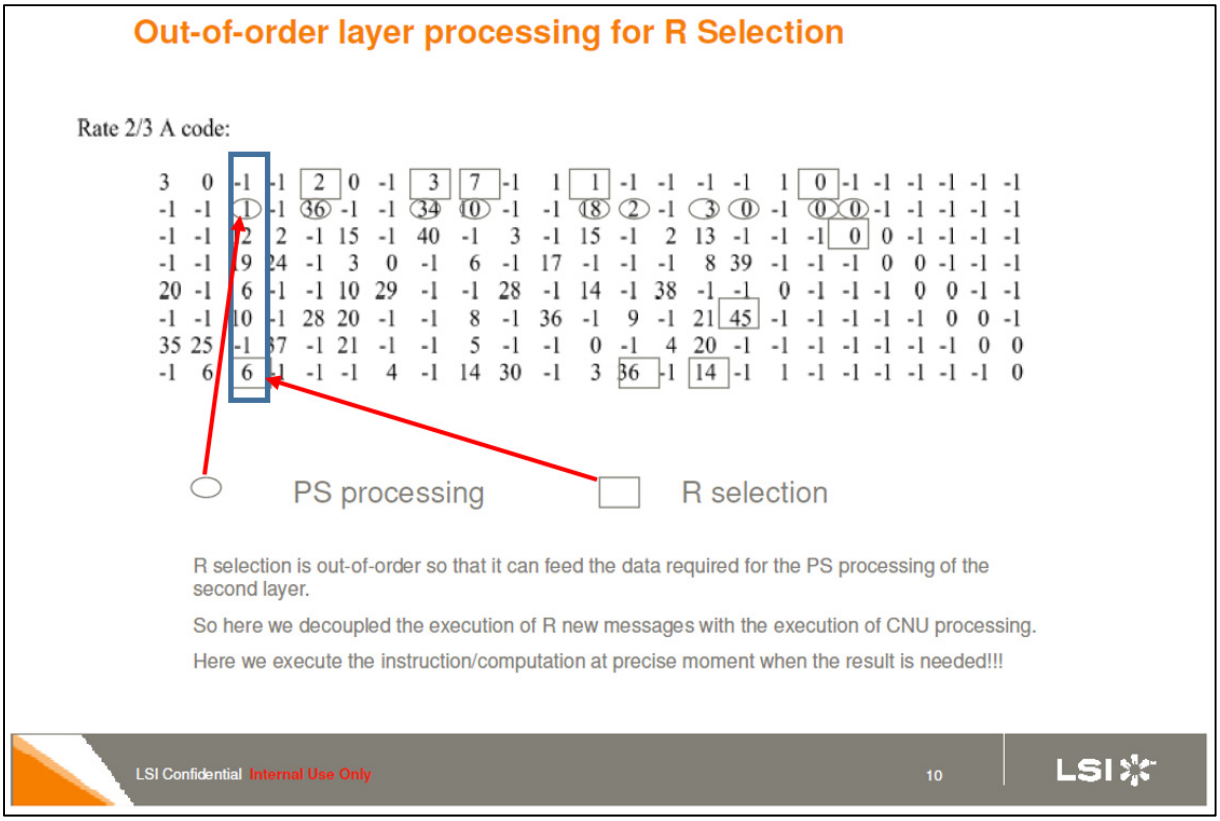


250. As shown below, the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products also includes a permuter (i.e., a cyclic shifter) that permutes the P message:



251. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include a permuter that permutes the P message by the difference of the permutation of a block currently being processed and the permutation of a block

previously processed (*see* above); wherein the block currently being processed and the block previously processed are in a same block column (*see* below):

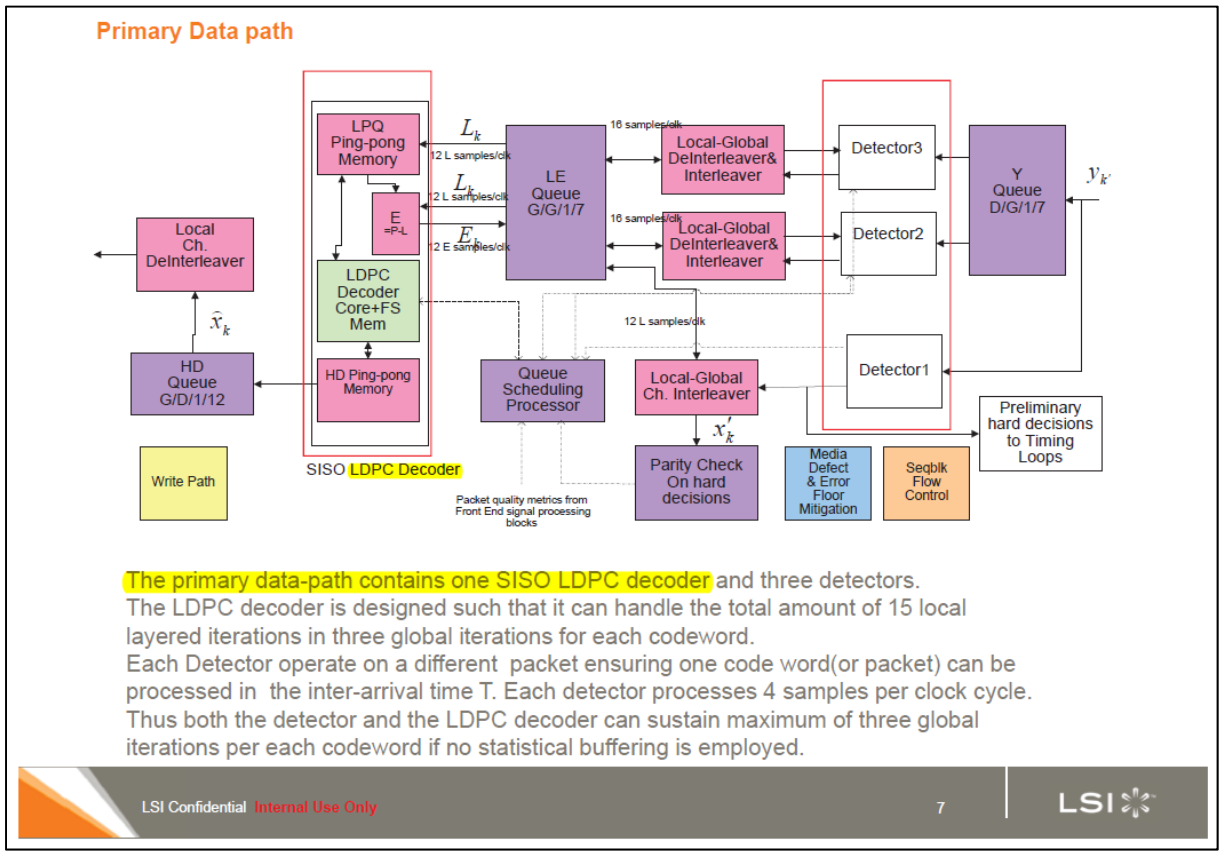


252. The method of Claim 10 is practiced by the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products for the same reasons set forth above with regard to the corresponding limitations of Claim 1.

253. Claim 17 of the '250 Patent recites as follows:

> 17. A low density parity check (LDPC) code decoder, comprising:
> a first R select unit that provides an R message by selecting from a plurality of possible R message values,
> a Q message generator that combines the R message with a P message to produce a Q message; and
> a first permuter that permutes the P message;
> wherein the decoder is configured to update the P message based on determination of a final state for each block row.

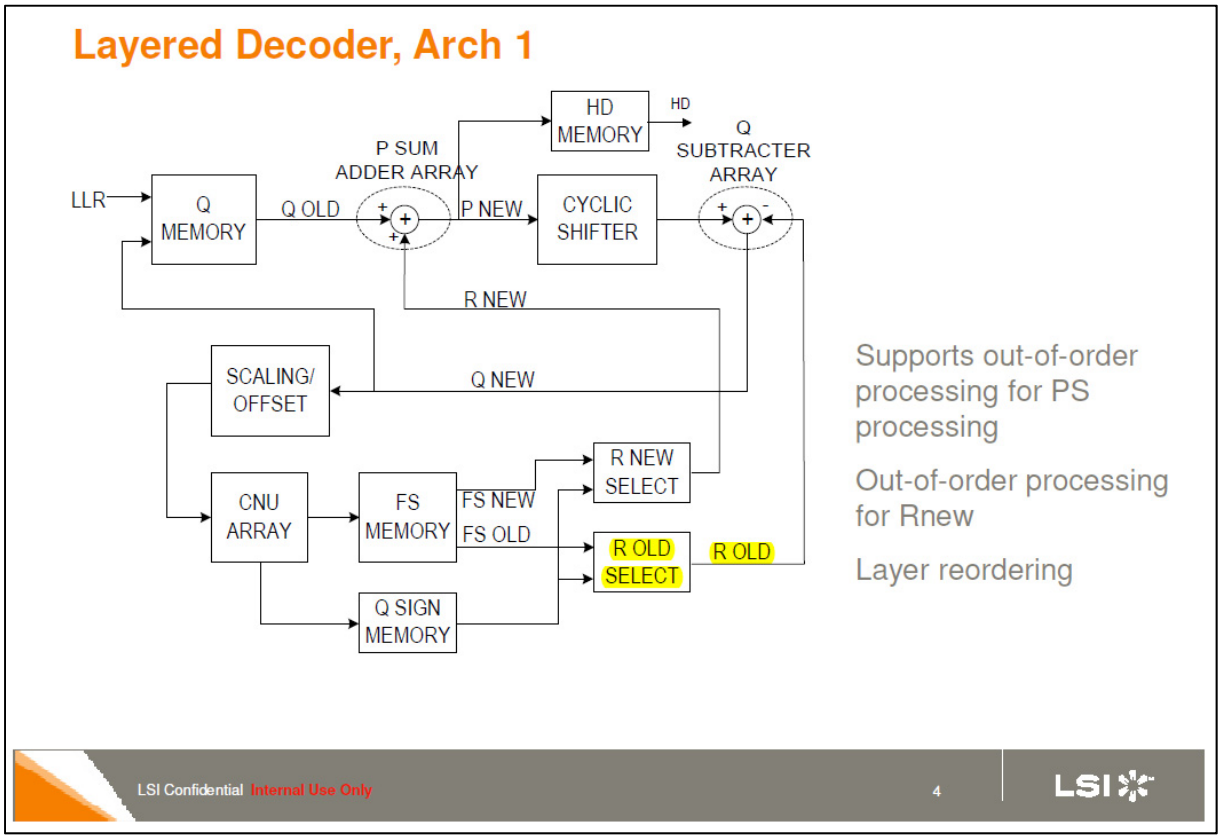
254. On information and belief, the Accused Products satisfy each and every limitation of Claim 17. The Accused Products include an LDPC code decoder. For example, with respect to Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products, the McLaren Architecture Presentation references the LDPC decoder.



With respect to the Accused Wi-Fi Products, they perform the LDPC decoding method described in the '489 patent which "operates by processing, in parallel, selected rows for multiple individual LDPC matrix rows from various sub-matrix rows (e.g., first group of rows from a first sub-matrix row, second group of rows from a second sub-matrix row, etc.)."

255. The Accused Products include a first R select unit that provides an R message by selecting from a plurality of possible R message values. For example, with respect to Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits

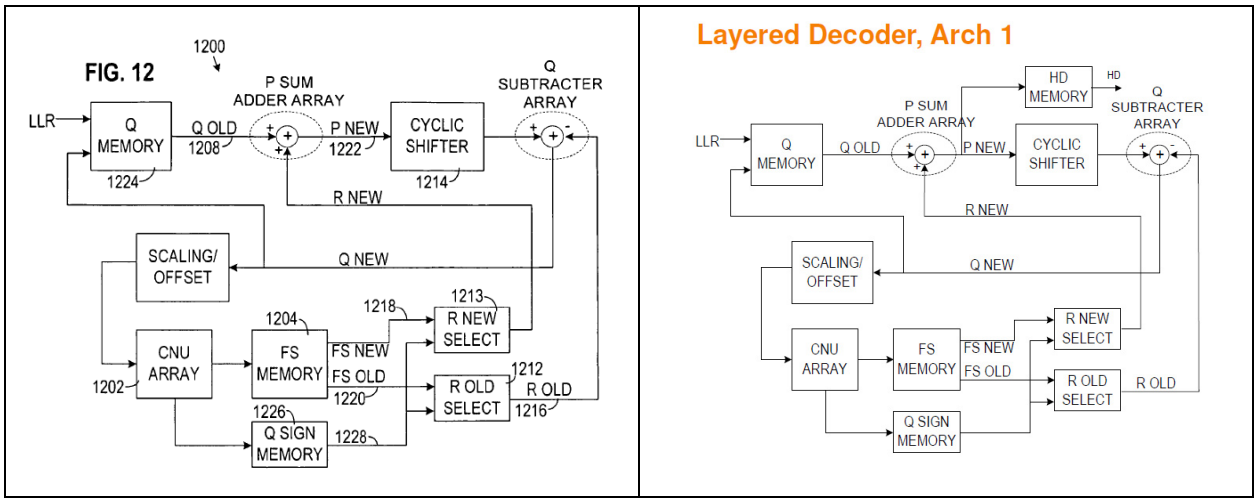
Products, the Layered Decoder Presentation discloses the presence of an R OLD SELECT unit that provides an R message by selecting from a plurality of possible R message values.



With respect to the Accused Wi-Fi Products, they perform the LDPC decoding method described in the '489 patent which utilizes, for example, CEM (check edge message) daisy chains for generating updated check edge message (λ) values from prior values, such as described, for example, in FIG. 10 (reproduced at ¶ 208, *supra*) and the accompanying disclosure. *See also* ¶ 155, *supra*, describing correlation between variables λ, γ, and (γ−λ) in the Broadcom '488 and '489 patents with R, P, and Q messages in Patents-in-Suit.

256. The layered decoder architecture of the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products is identical to what is set forth in the '250 Patent.

'250 Patent at FIG. 12 | **Layered Decoder Presentation at 4**



257. The Accused Products include a Q message generator that combines the R message with a P message to produce a Q message. For example, with respect to the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products, the Layered Decoder Presentation discloses a Q SUBTRACTER ARRAY that combines the R message with a P message to produce a Q message.

For the irregular block LDPC codes, the TDMP algorithm can be described with equations (21)-(24):

$$\vec{R}_{l,n}^{(0)} = 0, \vec{P}_n = \vec{L}_n^{(0)} \quad \text{[Initialization for each new received data frame]}, \tag{21}$$

$$\forall i = 1,2,\cdots,it_{\max} \quad \text{[Iteration loop]},$$

$$\forall l = 1,2,\cdots,j \quad \text{[Sub-iteration loop]},$$

$$\forall n = 1,2,\cdots,k \quad \text{[Block column loop]},$$

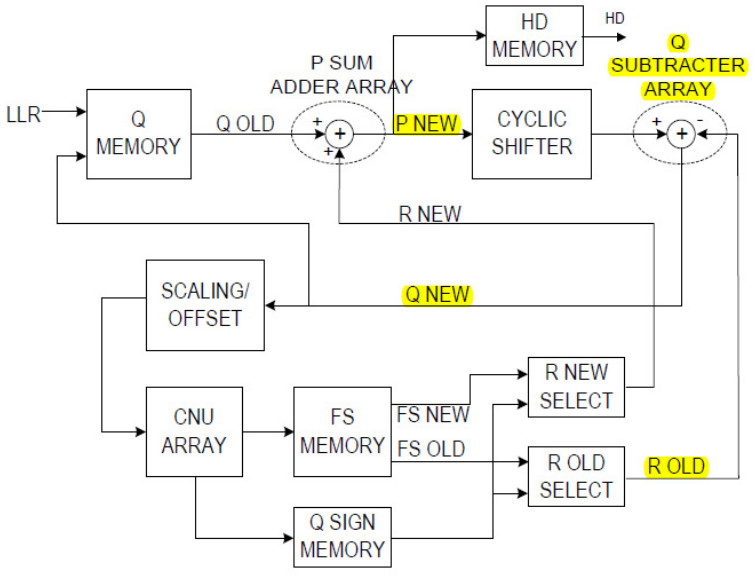
$$\left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n)} = \left[\vec{P}_n\right]^{S(l,n)} - \vec{R}_{l,n}^{(i-1)}, \tag{22}$$

$$\vec{R}_{l,n}^{(i)} = f\left(\left[\vec{Q}_{l,n'}^{(i)}\right]^{S(l,n')}, \forall n' = 1,2,\cdots,k\right), \tag{23}$$

$$\left[\vec{P}_n\right]^{S(l,n)} = \left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n)} + \vec{R}_{l,n}^{(i)}, \tag{24}$$

where the vectors $\vec{R}_{l,n}^{(i)}$ and $\vec{Q}_{l,n}^{(i)}$ represent all the R and Q messages in each non-zero block of the H matrix, $s(l,n)$ denotes the shift coefficient for the l^{th} block row and n^{th} non-zero block of the H matrix (note that null blocks in the H matrix need not be processed); $\left[\vec{R}_{l,n}^{i-1}\right]^{S(l,n)}$ denotes that the vector $\vec{R}_{l,n}^{i-1}$ is cyclically shifted up by the amount $s(l,n)$, and k is the check-node degree of the block row or the layer. A negative sign on $s(l,n)$ indicates that it is cyclic down shift (equivalent cyclic left shift). $f(\cdot)$ denotes the check-node processing.

Layered Decoder, Arch 1



Supports out-of-order processing for PS processing

Out-of-order processing for Rnew

Layer reordering

With respect to the Accused Wi-Fi Products, they perform the LDPC decoding method described in the '489 patent which utilizes, for example, adders that that generate input values to the check modules by combining the check edge message/intrinsic information (λ) values with APP (or gamma(γ)) values in accordance with the permuted accelerated decoding architecture such as described in FIG. 10 (reproduced at ¶ 208, *supra*) and the accompanying disclosure.

258. The TDMP algorithm equations of the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products are identical to what is set forth in the '250 Patent.

'250 Patent at 15:23–50

For the irregular block LDPC codes, the TDMP algorithm can be described with equations (21)-(24):

$\vec{R}_{l,n}^{(0)}=0, \vec{P}_n=\vec{L}_n^{(0)}$ [Initialization for each new received data frame],

$\forall i=1,2,\ldots,it_{max}$ [Iteration loop],

$\forall l=1,2,\ldots,j$ [Sub-iteration loop],

$\forall n=1,2,\ldots,k$ [Block column loop], (21)

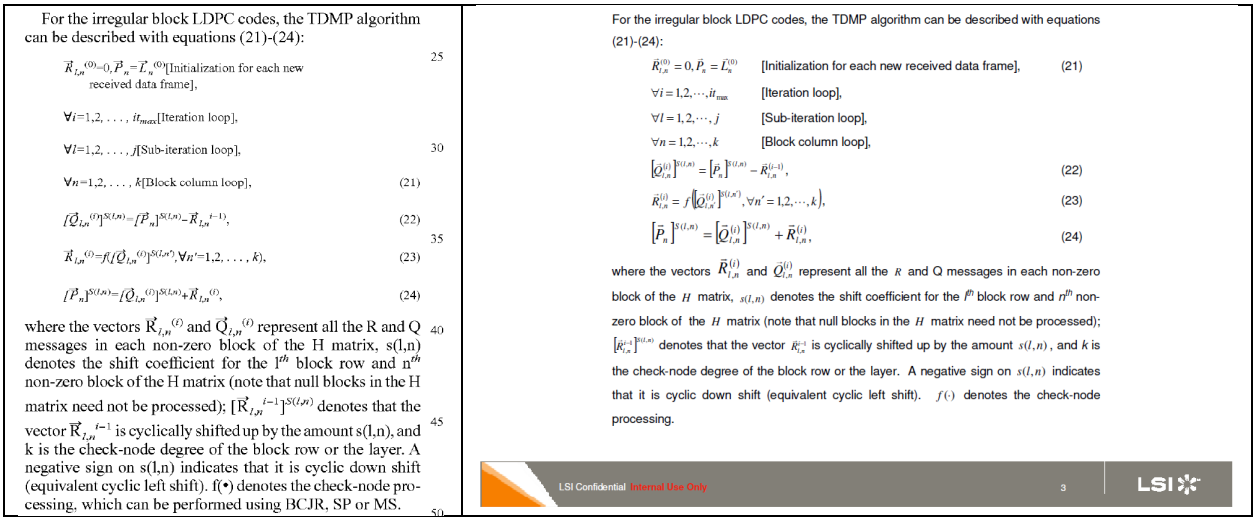
$[\vec{Q}_{l,n}^{(i)}]^{S(l,n)}=[\vec{P}_n]^{S(l,n)}-\vec{R}_{l,n}^{i-1)}$, (22)

$\vec{R}_{l,n}^{(i)}=f([\vec{Q}_{l,n}^{(i)}]^{S(l,n')}), \forall n'=1,2,\ldots,k)$, (23)

$[\vec{P}_n]^{S(l,n)}=[\vec{Q}_{l,n}^{(i)}]^{S(l,n)}+\vec{R}_{l,n}^{(i)}$, (24)

where the vectors $\vec{R}_{l,n}^{(i)}$ and $\vec{Q}_{l,n}^{(i)}$ represent all the R and Q messages in each non-zero block of the H matrix, s(l,n) denotes the shift coefficient for the l^{th} block row and n^{th} non-zero block of the H matrix (note that null blocks in the H matrix need not be processed); $[\vec{R}_{l,n}^{i-1}]^{S(l,n)}$ denotes that the vector $\vec{R}_{l,n}^{i-1}$ is cyclically shifted up by the amount s(l,n), and k is the check-node degree of the block row or the layer. A negative sign on s(l,n) indicates that it is cyclic down shift (equivalent cyclic left shift). f(•) denotes the check-node processing, which can be performed using BCJR, SP or MS.

Layered Decoder Presentation at 3



For the irregular block LDPC codes, the TDMP algorithm can be described with equations (21)-(24):

$\vec{R}_{l,n}^{(0)}=0, \vec{P}_n=\vec{L}_n^{(0)}$ [Initialization for each new received data frame], (21)

$\forall i=1,2,\cdots,it_{max}$ [Iteration loop],

$\forall l=1,2,\cdots,j$ [Sub-iteration loop],

$\forall n=1,2,\cdots,k$ [Block column loop],

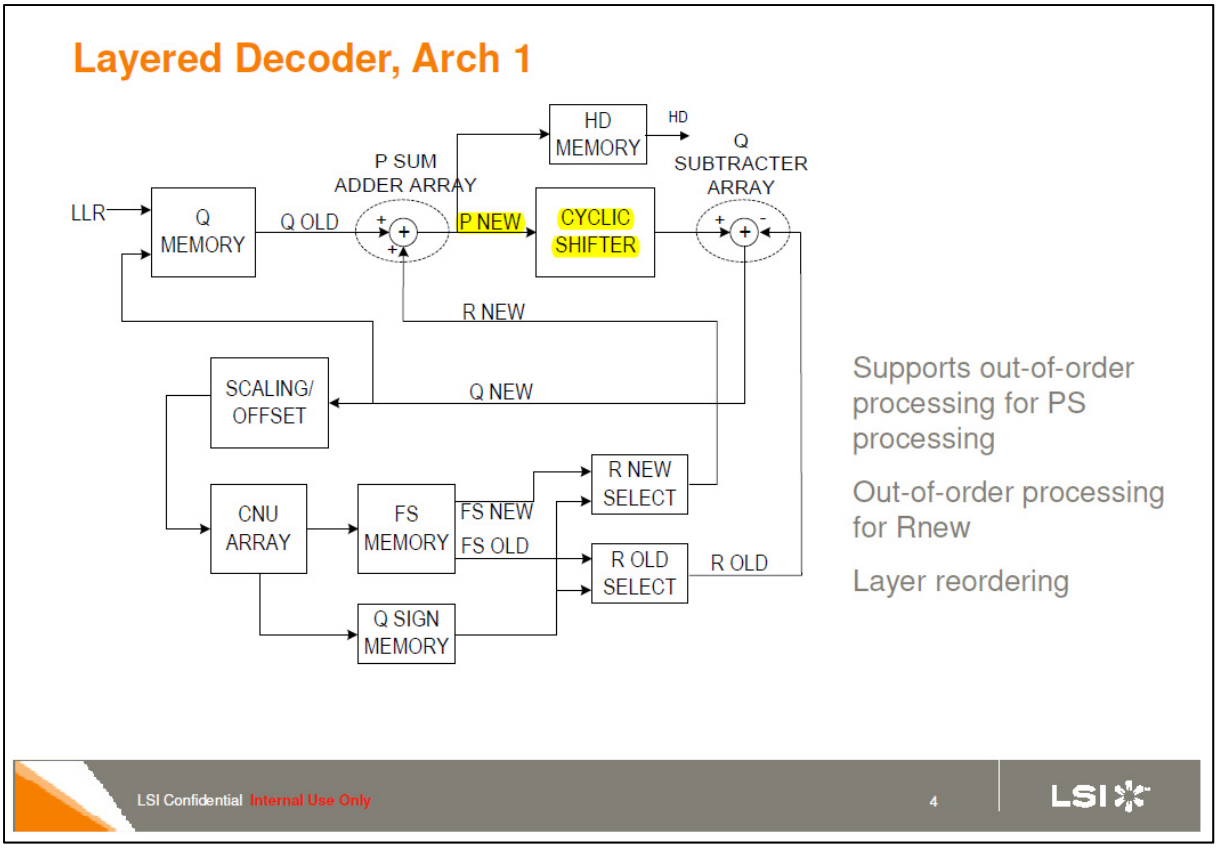
$\left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n)}=\left[\vec{P}_n\right]^{S(l,n)}-\vec{R}_{l,n}^{(i-1)}$, (22)

$\vec{R}_{l,n}^{(i)}=f\left(\left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n')}, \forall n'=1,2,\cdots,k\right)$, (23)

$\left[\vec{P}_n\right]^{S(l,n)}=\left[\vec{Q}_{l,n}^{(i)}\right]^{S(l,n)}+\vec{R}_{l,n}^{(i)}$, (24)

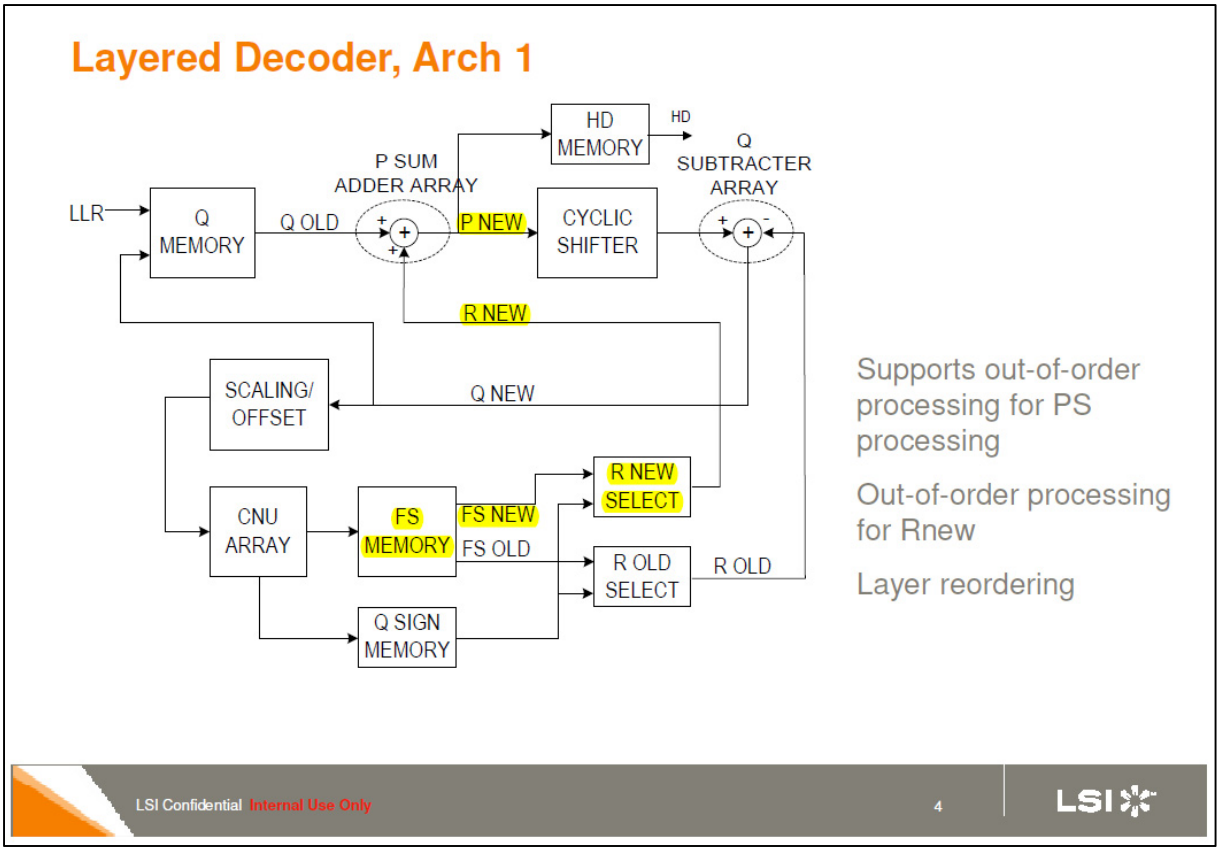
where the vectors $\vec{R}_{l,n}^{(i)}$ and $\vec{Q}_{l,n}^{(i)}$ represent all the R and Q messages in each non-zero block of the H matrix, $s(l,n)$ denotes the shift coefficient for the l^{th} block row and n^{th} non-zero block of the H matrix (note that null blocks in the H matrix need not be processed); $\left[\vec{R}_{l,n}^{i-1}\right]^{S(l,n)}$ denotes that the vector $\vec{R}_{l,n}^{i-1}$ is cyclically shifted up by the amount $s(l,n)$, and k is the check-node degree of the block row or the layer. A negative sign on $s(l,n)$ indicates that it is cyclic down shift (equivalent cyclic left shift). $f(\cdot)$ denotes the check-node processing.

259. The Accused Products include a first permuter that permutes the P message. For example, with respect to the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products, the Layered Decoder Presentation discloses a CYCLIC SHIFTER that permutes the P message.



With respect to the Accused Wi-Fi Products, they perform the LDPC decoding method described in the '489 patent which utilizes for example, APP (or gamma(γ)) daisy chains (shown as gamma daisy chain 1 (APP(γ)) to gamma daisy chain p (APP(γ)) that permute the APP (or gamma(γ)) values as described, for example, in FIG. 10 (reproduced at ¶ 208, *supra*) and the corresponding disclosure. FIG. 10 notes specifically that "daisy chains handle shift pattern of *H* directly (allow multiple taps for multi-row and permuted order processing, schedule change)."

260. The Accused Products include wherein the decoder is configured to update the P message based on determination of a final state for each block row. For example, with respect to the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products, the Layered Decoder Presentation discloses that the P message is a function of R NEW, and R NEW is based on a determination of a final state for each block row.



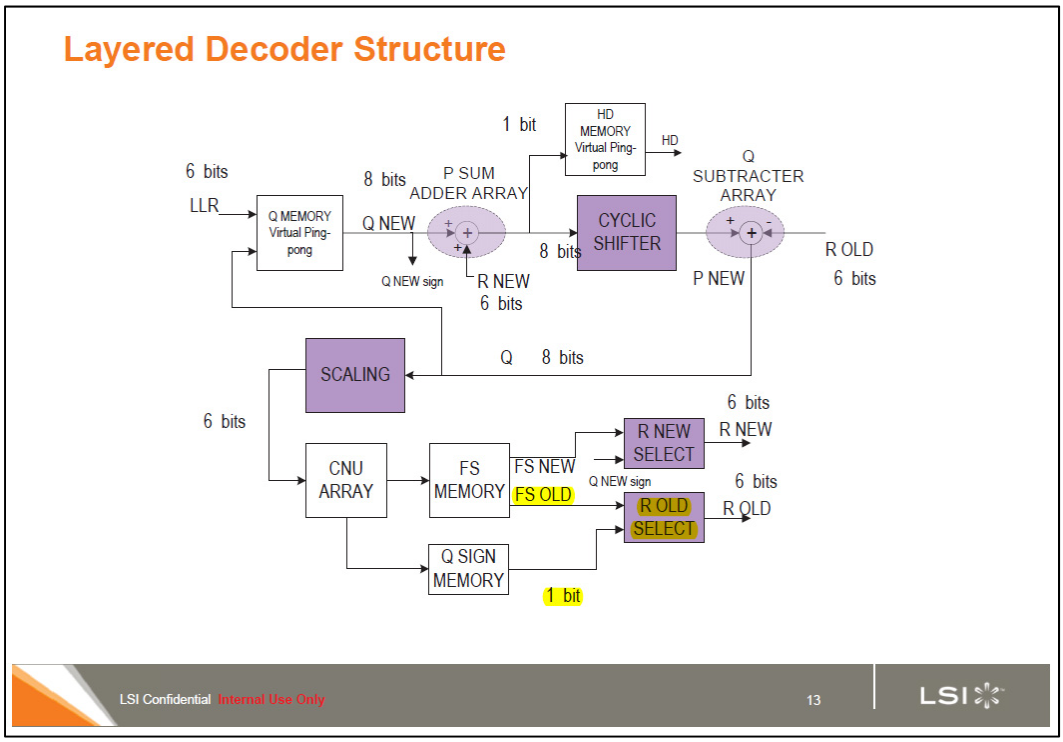
With respect to the Accused Wi-Fi Products, they perform the LDPC decoding method described in the '489 patent in which a decoder computes the APP (or gamma(γ)) values based on check edge message/intrinsic information (λ) values of sub-matrix rows of the LDPC matrix (which in turn depend on the final state for each block row), such as described, for example, in FIG. 10 (reproduced at ¶ 208, *supra*) and the corresponding disclosure.

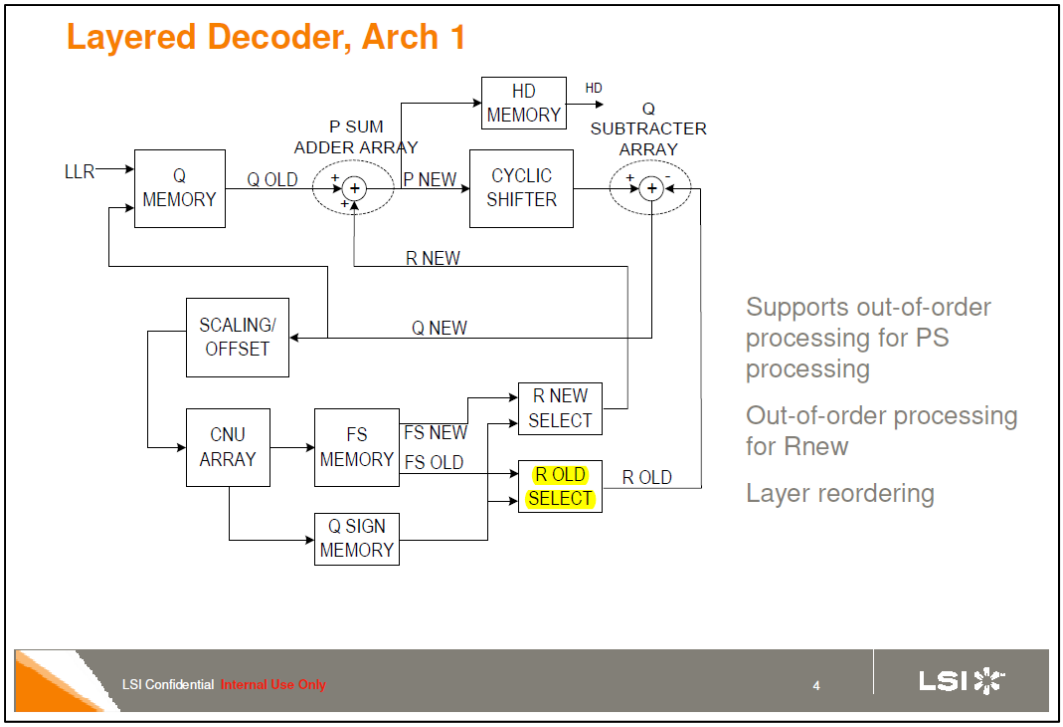
261. Claim 32 of the '250 Patent recites as follows:

> 32. A method for decoding a low density parity check code, comprising:
> selecting a first R message from a plurality of previously generated possible R messages based on at least a message index value and a sign bit;
> generating a Q message by combining the first R message with a P message;
> permuting the P message; and
> updating the P message responsive to determination of a final state for each block row.

262. On information and belief, the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products satisfy each and every limitation of Claim 32. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products decode an LDPC code. *See* ¶¶ 238, 241, *supra*.

263. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products select a first R message from a plurality of previously generated possible R messages based on at least a message index value and a sign bit. For example, the McLaren Architecture Presentation and the Layered Decoder Presentation each disclose the presence of an R OLD SELECT unit that selects a first R message from a plurality of previously generated possible R messages based on at least a message index value and a sign bit.





264. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products generate a Q message by combining the first R message with a P message. *See* ¶¶ 210, 241, *supra*.

265. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products permute the P message. *See* ¶¶ 234, 243, *supra*.

266. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products update the P message responsive to determination of a final state for each block row. *See* ¶¶ 213, 244, *supra*.

267. Claim 41 of the ’250 Patent recites as follows:

> 41. A low density parity check code decoder, comprising:
> a check node unit (CNU); the CNU comprising:
> a set of comparators for comparing stored minimum values to a received variable message Q, wherein:
> a total number of comparators in the set is less than the check node degree;

a first comparator of the set determines a first minimum value, M1, by comparing a first stored minimum value, $M1_{PS}$, and the received variable message Q; and

a second comparator of the set determines a second minimum value, M2, by comparing a second stored minimum value, $M2_{PS}$, and the received variable message Q; and

final state storage that stores:

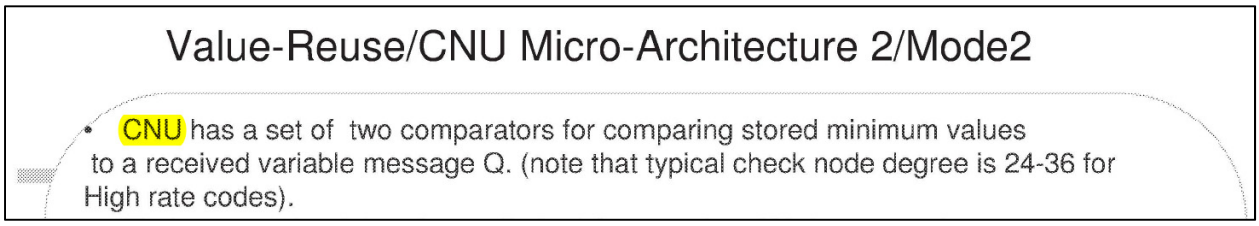
$M1_{PS}$, and

$M2_{PS}$; and

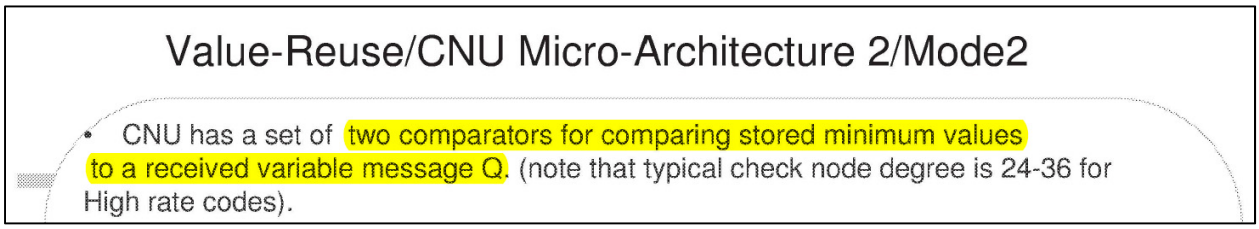
a computation unit that computes a message transferred from the check node to a variable node based on the values of $M1_{PS}$ and $M2_{PS}$ stored in the final state storage.

268. On information and belief, the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products satisfy each and every limitation of Claim 41. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include a low density parity check code decoder. For example, the McLaren Architecture Presentation references the LDPC decoder. *See* ¶¶ 146, 207 238, *supra*.

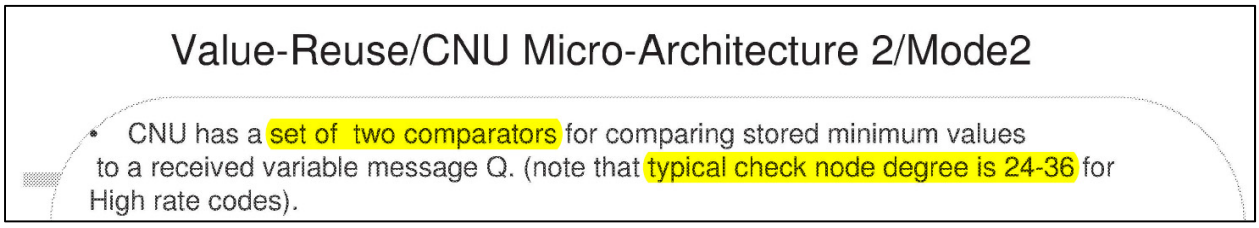
269. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include a check node unit (CNU). For example, a presentation given by LSI engineers at the 42nd Asilomar Conference on Signals, Systems, and Computers on October 28, 2008 is titled "Next Generation Iterative LDPC Solutions for Magnetic Recording Storage" (hereinafter, the "Asilomar Presentation") and discloses a check node unit.



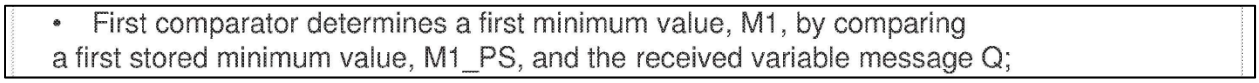
270. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include a set of comparators for comparing stored minimum values to a received variable message Q. For example, the "Asilomar Presentation" discloses a check node unit.



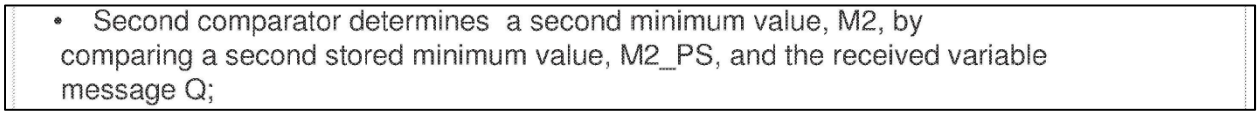
271. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include wherein a total number of comparators in the set is less than the check node degree. For example, the Asilomar Presentation discloses that the total number of comparators in the set is two, which is less than the disclosed typical check node degree of 24-36.



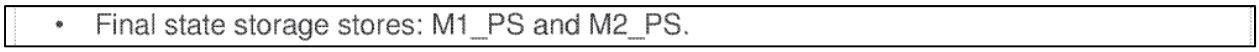
272. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include wherein a first comparator of the set determines a first minimum value, M1, by comparing a first stored minimum value, $M1_{PS}$, and the received variable message Q. For example, the Asilomar Presentation discloses that a first comparator determines a first minimum value, M1, by comparing a first stored minimum value, M1_PS, and the received variable message Q.



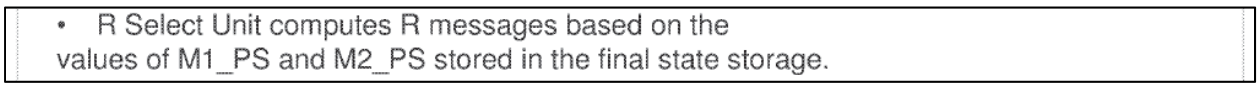
273. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include wherein a second comparator of the set determines a second minimum value, M2, by comparing a second stored minimum value, $M2_{PS}$, and the received variable message Q. For example, the Asilomar Presentation discloses that a second comparator determines a second minimum value, M2, by comparing a second stored minimum value, M2_PS, and the received variable message Q.



274. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include final state storage that stores $M1_{PS}$, and $M2_{PS}$. For example, the Asilomar Presentation discloses that final state storage stores M1_PS and M2_PS.



275. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include a computation unit that computes a message transferred from the check node to a variable node based on the values of $M1_{PS}$ and $M2_{PS}$ stored in the final state storage. For example, the Asilomar Presentation discloses that the R Select Unit computes R messages based on the values of M1_PS and M2_PS stored in the final state storage.



276. In view of the foregoing, the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products directly infringe at least Claims 1-20, 25, 27-28, 31-35, 37, 38, 41, 44, and 46 of the '250 Patent at least through Defendants' and/or the Broadcom Predecessor Entities' sale, offer for sale, importation, use, and/or testing of the Accused Hard Disk Controller Products, the Accused SandForce Products,

and the Accused Densbits Products and the Accused Wi-Fi Products directly infringe at least Claim 17 of the '250 Patent at least through Defendants' and/or the Broadcom Predecessor Entities' sale, offer for sale, importation, use, and/or testing of the Accused Wi-Fi Products.

277. On information and belief, Defendants and/or the Broadcom Predecessor Entities should have known that they directly infringe as of the date LSI became aware of the issuance of the '250 Patent, and in any event no later than the date LSI was advised of the issuance of impending issuance the '250 Patent by Dr. Gunnam on January 31, 2014, and in any event on or about February 18, 2014 when the '250 Patent issued.

278. Defendants and/or the Broadcom Predecessor Entities further have knowledge of the '250 Patent at least as early as the filing and/or service of Plaintiff's original Complaint. (*See* D.I. 1, 5) Defendants and/or the Broadcom Predecessor Entities are further aware that the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products necessarily practice Claims 1-20, 25, 27-28, 31-35, 37, 38, 41, 44, and 46 of the '250 Patent and the Accused Wi-Fi Products necessarily practice Claim 17 of the '250 Patent.

279. On information and belief, Defendants and/or the Broadcom Predecessor Entities take active steps to induce infringement by others of at least Claims 1-20, 25, 27-28, 31-35, 37, 38, 41, 44, and 46 of the '250 Patent in violation of 35 U.S.C. §271(b), including, for example, by (a) inducing manufacturers to perform the claimed inventions when testing the Accused Products, and (b) inducing end users to perform the claimed inventions when using the Accused Products. Such active steps include, but are not limited to, selling Accused Products with the knowledge and intent that the Accused Products will be operated by such manufacturers and their customers in accordance with the claimed inventions, as set forth in the Section "EXAMPLES OF DIRECT AND INDIRECT INFRINGEMENT" below.

280. On information and belief, Defendants and/or the Broadcom Predecessor Entities knew or should have known that such activities induce others to directly infringe one or more of at least Claims 1-20, 25, 27-28, 31-35, 37, 38, 41, 44, and 46 of the ’250 Patent. For example, Defendants and/or the Broadcom Predecessor Entities should have known that their actions induced others to directly infringe as of the date LSI became aware of the issuance of the ’250 Patent no later than the date LSI was advised of the issuance of impending issuance the ’250 Patent by Dr. Gunnam on January 31, 2014, and in any event on or about February 18, 2014 when the ’250 Patent issued. Defendants and/or the Broadcom Predecessor Entities were further informed that the technology in the Accused Products infringed the ’250 Patent, and Defendants and/or the Broadcom Predecessor Entities knowingly and purposefully continued to exploit the patented technology despite knowing that it was covered by the ’250 Patent, as set forth in the Section “EXAMPLES OF DIRECT AND INDIRECT INFRINGEMENT” below..

281. On information and belief, Defendants and/or the Broadcom Predecessor Entities have contributed to the infringement of at least Claims 1-20, 25, 27-28, 31-35, 37, 38, 41, 44, and 46 of the ’250 Patent by others, including consumer/end-user use of the Accused Products, in violation of 35 U.S.C. § 271(c). Acts by Defendants and/or the Broadcom Predecessor Entities that contribute to the infringement of others include, but are not limited to, the sale, offer for sale, and/or import by Defendants and/or the Broadcom Predecessor Entities of the Accused Products, as set forth in the Section “EXAMPLES OF DIRECT AND INDIRECT INFRINGEMENT” below. Such Accused Products are especially made for or adapted for use to infringe, and are not a staple article of commerce and are not suitable for substantial non-infringing use. The Accused Products are apparatuses for use in practicing Claims 1-20, 25, 27-

28, 31-35, 37, 38, 41, 44, and 46 of the '250 Patent and are at least a material part of those claimed inventions, for example, as described above with respect to Claim 1.

282. As also described above, Defendants and/or the Broadcom Predecessor Entities have, on information and belief, been on notice of the '250 Patent since it issued on February 18, 2014, and in addition since filing and/or service of Plaintiff's original Complaint, and Defendants and/or the Broadcom Predecessor Entities have further been aware that use of the Accused Products necessarily practice Claims 1-20, 25, 27-28, 31-35, 37, 38, 41, 44, and 46 of the '250 Patent. (*See* D.I. 1, 5)

283. The Accused Products are especially made for or adapted for use to infringe, and are not a staple article of commerce and are not suitable for substantial non-infringing use. By way of example, the use of the LDPC decoders included in the Accused Products is necessary to use the accused products for their intended purpose (decoding data from a hard disk drive, solid state drive, or wireless digital transmission), and the LDPC decoders necessarily perform the claimed inventions when they decode data. Accordingly, the Accused Products do not have a substantial use that does not entail practicing the claimed inventions. On information and belief, the Accused Products cannot be used but to infringe the '250 Patent.

284. Despite Defendants' and/or the Broadcom Predecessor Entities' knowledge, notice, and infringement of the '250 Patent, Defendants and/or the Broadcom Predecessor Entities continue to manufacture, use, sell, offer for sale, and/or import the Accused Products in a manner that willfully infringes the '250 Patent, and on information and belief continue to sell and/or offer for sale the Accused Products to the United States market. Defendants' and/or the Broadcom Predecessor Entities' infringement of the '250 Patent is willful, as set forth above. Defendants and/or the Broadcom Predecessor Entities lacked a justifiable belief that they do not

infringe the '250 Patent, or that the '250 Patent is invalid or unenforceable, and have acted recklessly in their infringing activity, justifying an increase in the damages to be awarded to Plaintiff up to three times the amount found or assessed, in accordance with 35 U.S.C. § 284.

285. On information and belief, Defendants and/or the Broadcom Predecessor Entities had actual or constructive knowledge of the '250 Patent since at least February 18, 2014.

286. Defendants and/or the Broadcom Predecessor Entities further have had knowledge of the '250 Patent at least as early as the filing and/or service of Plaintiff's original Complaint. (*See* D.I. 1, 5) Defendants and/or the Broadcom Predecessor Entities know or should know as of the date of filing and/or service of Plaintiff's original Complaint that their actions induced others to directly infringe the '250 Patent and contributed to infringement of the '250 Patent. (*See Id.*)

287. This case is rendered an exceptional case at least in light of Defendants' and/or the Broadcom Predecessor Entities' willful infringement of the '250 Patent, justifying an award to Plaintiff of its reasonable attorney fees, in accordance with 35 U.S.C. § 285.

288. Plaintiff has no adequate remedy at law for Defendants' and/or the Broadcom Predecessor Entities' acts of infringement. As a direct and proximate result of Defendants' and/or the Broadcom Predecessor Entities' acts of infringement, Plaintiff has suffered and continues to suffer damages and irreparable harm. Unless Defendants' and/or the Broadcom Predecessor Entities' acts of infringement are enjoined by this Court, Plaintiff will continue to be damaged and irreparably harmed.

289. Defendants' and/or the Broadcom Predecessor Entities' infringement of the '250 Patent has damaged and continues to damage Plaintiff in an amount yet to be determined, of at

least a reasonable royalty and/or lost profits that Plaintiff would have made but for Defendants' and/or the Broadcom Predecessor Entities' infringement acts.

COUNT VI
(Infringement under 35 U.S.C. § 271 of U.S. Patent No. 10,141,950)

290. Plaintiff repeats and re-alleges the paragraphs above as if fully set forth herein.

291. The '950 Patent is valid, enforceable, and was duly issued on November 27, 2018 in full compliance with Title 35 of the United States Code.

292. On information and belief, in violation of 35 U.S.C. § 271, Defendants and/or the Broadcom Predecessor Entities have infringed, contributed to the infringement of, and/or induced others to infringe the '950 Patent, either literally or under the doctrine of equivalents, by, among other things, making, using, offering for sale, selling, selling infringing products abroad with knowledge and intent that the infringing products be imported into the United States by others, and/or importing into the United States unlicensed systems and/or products in a manner that infringes at least Claims 1-16 of the '950 Patent.

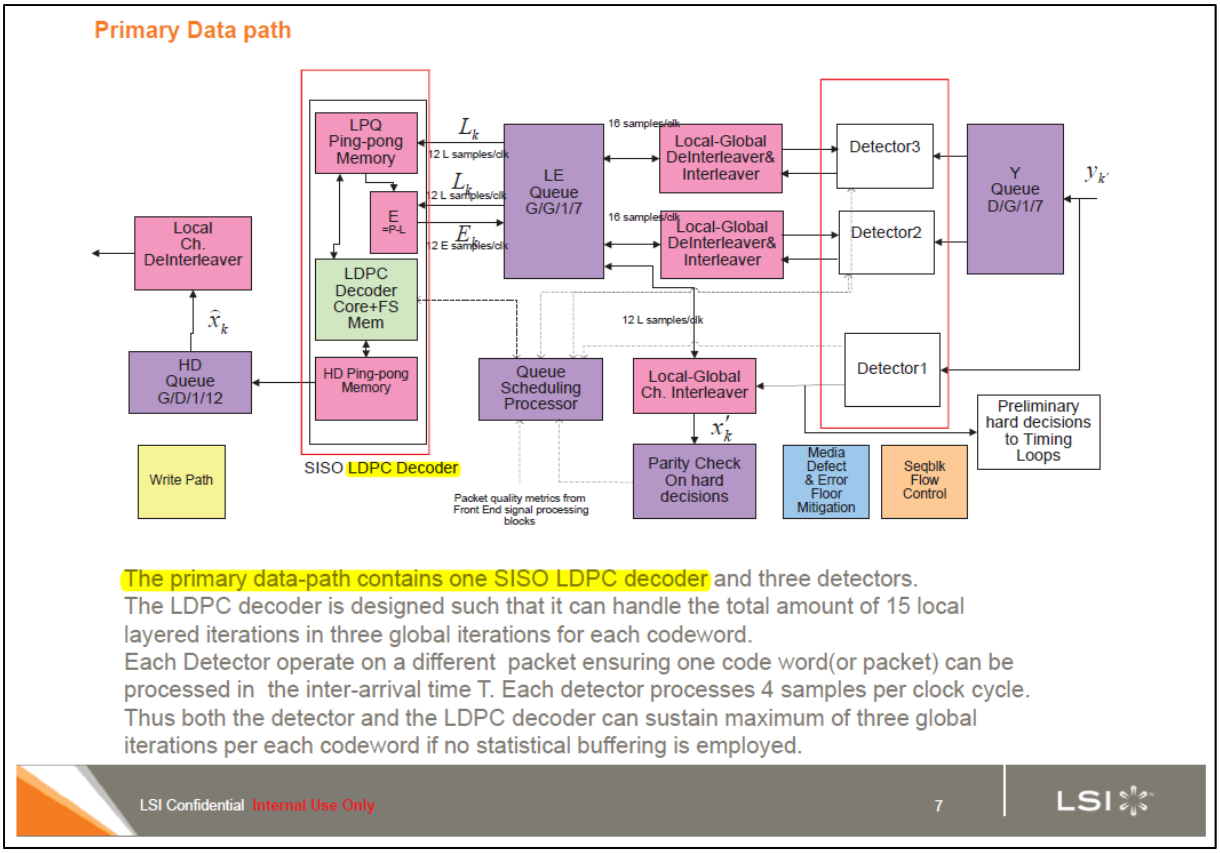
293. On information and belief, Defendants and/or the Broadcom Predecessor Entities have directly infringed the '950 Patent, for example, by making, using, selling, offering to sell, and/or importing into the United States the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products, which meet each and every limitation of at least Claim 1 of the '950 Patent, in violation of Plaintiff's patent rights and without Plaintiff's license or authority. Non-limiting examples of such infringement are provided below, based on the limited information currently available to Plaintiff.

294. Claim 1 of the '950 Patent recites as follows:

> 1. A low density parity check (LDPC) code decoder, comprising:
> decoding circuitry configured to process blocks of an LDPC matrix,
> the decoding circuitry comprising:

> a control unit that controls processing by the decoding circuitry, the control unit configured to cause the decoding circuitry to process blocks of a layer of the LDPC matrix out of order, wherein the control unit is configured to cause the decoding circuitry to process each block of the LDPC matrix in processing substeps comprising:
>
> an R new update substep that provides an R new message, wherein the R new message is produced for a block of a different layer of the matrix from a layer containing a block currently being processed;
>
> an R old update substep that selects an R old message, wherein the R old message is produced for a layer of the matrix currently being processed;
>
> a P message substep that generates updated P messages;
>
> a Q message substep that computes variable node messages (Q messages); and
>
> a partial state substep that updates partial state of a block row based on Q messages computed for the block (check node unit (CNU) Partial state processing).

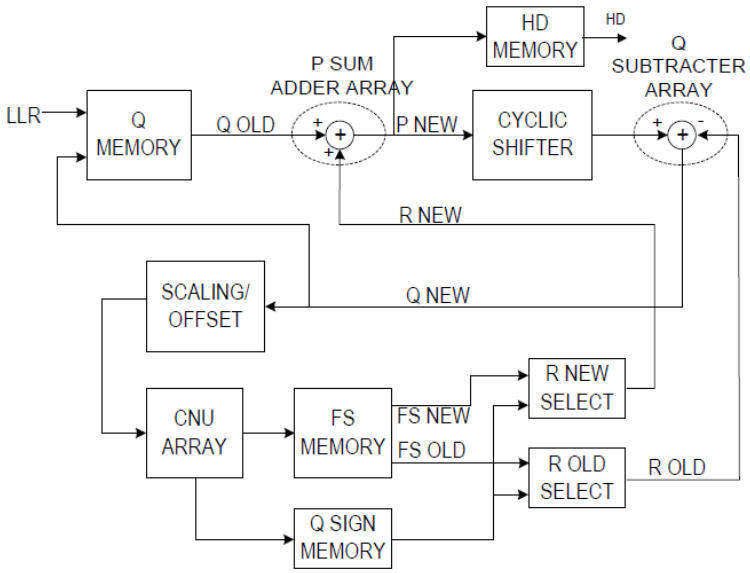
295. On information and belief, the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products satisfy each and every limitation of Claim 1. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products comprise an LDPC code decoder. For example, the McLaren Architecture Presentation references the LDPC decoder.



296. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include decoding circuitry, and as set forth below, that decoding circuitry is configured to process blocks of an LDPC matrix.

297. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include a control unit that controls processing by the decoding circuitry, the control unit configured to cause the decoding circuitry to process blocks of a layer of the LDPC matrix out of order. For example, the Layered Decoder Presentation references out of order processing and includes many figures taken directly from the '950 Patent.

Layered Decoder, Arch 1

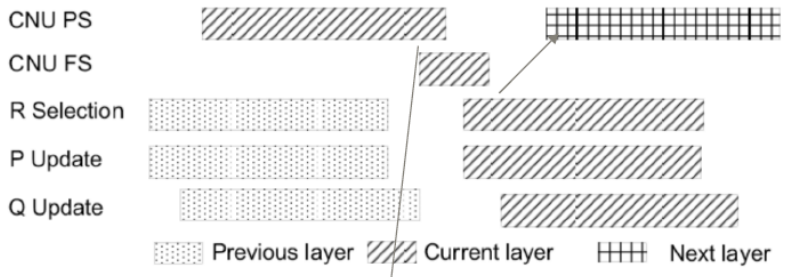


Supports out-of-order processing for PS processing

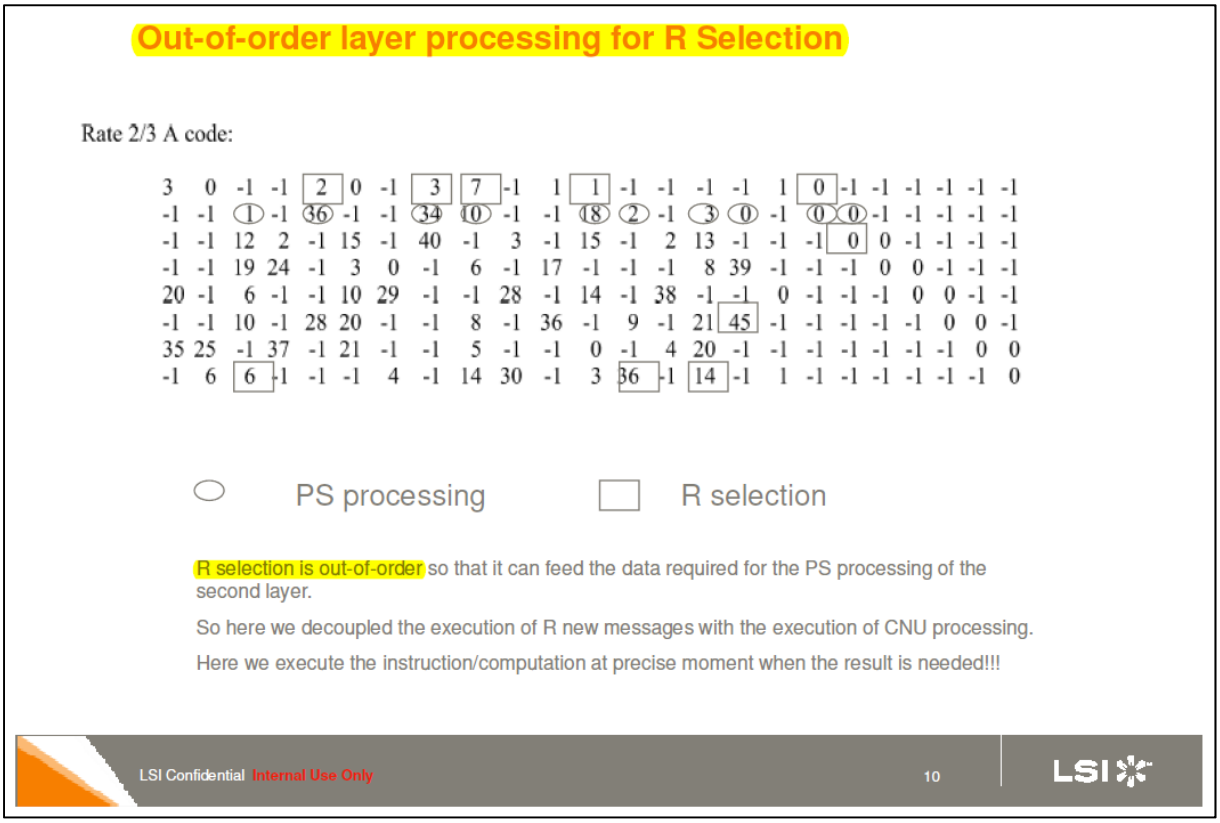
Out-of-order processing for Rnew

Layer reordering

Out-of-order processing for PS processing

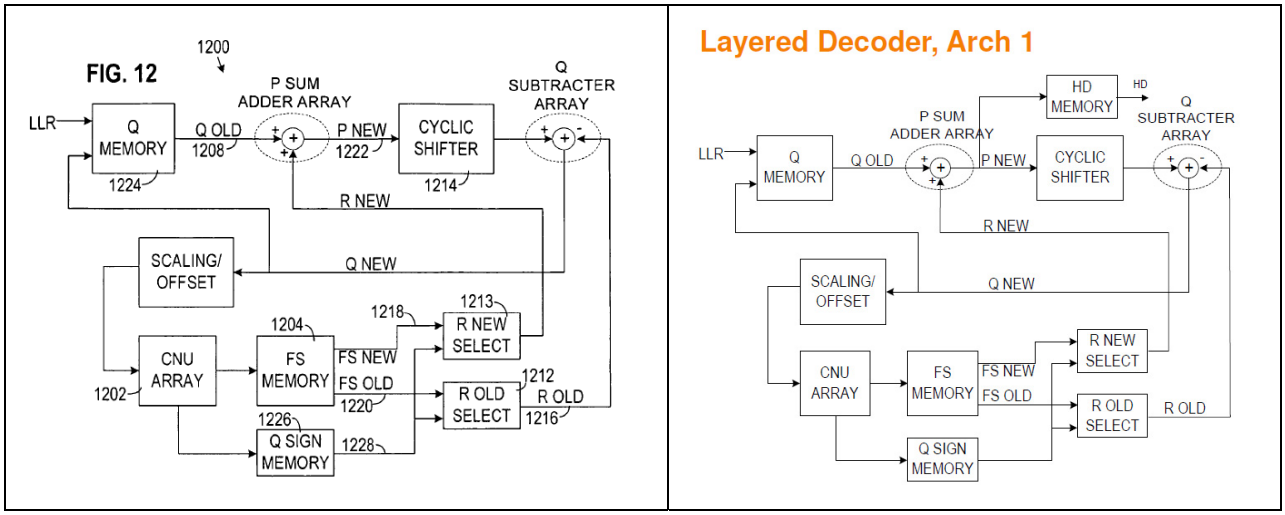


The circulants in each layers can be processed out-of-order



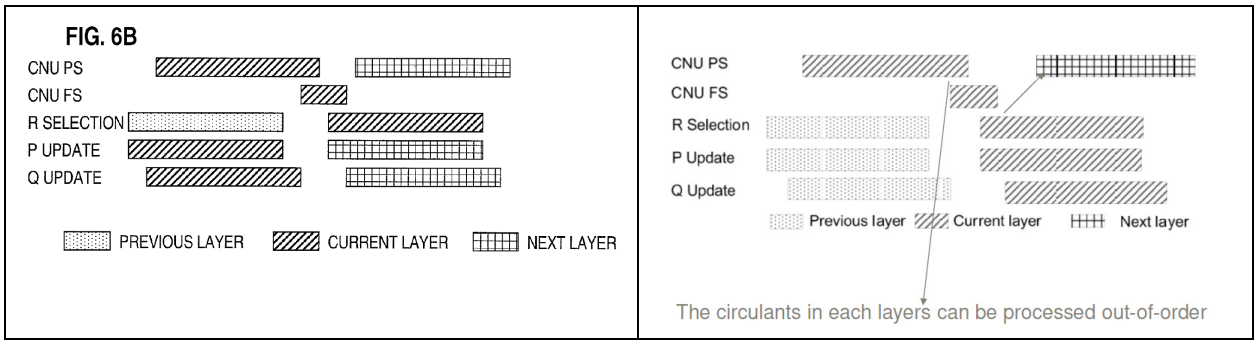
298. The layered decoder architecture of the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products is identical to what is set forth in the '950 Patent.

'950 Patent at FIG. 12 | **Layered Decoder Presentation at 4**



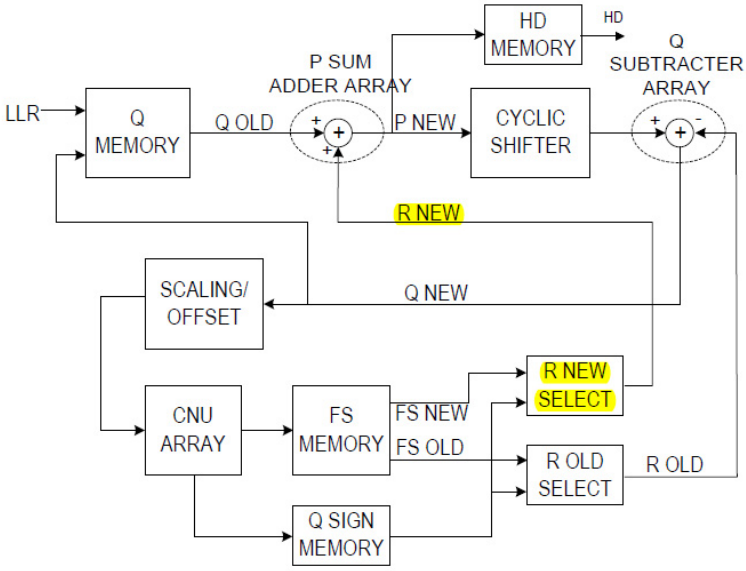
299. The pipeline architecture of the Accused Products is similar to what is set forth in the '950 Patent.

'950 Patent at FIG. 6B | **Layered Decoder Presentation at 8**



300. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include a control unit configured to cause the decoding circuitry to process each block of the LDPC matrix in processing substeps comprising an R new update substep that provides an R new message, wherein the R new message is produced for a block of a different layer of the matrix from a layer containing a block currently being processed. For example, the Layered Decoder Presentation discloses an R NEW SELECT unit that produces an R new message for a block of a different layer of the matrix from a layer containing a block currently being processed.

Layered Decoder, Arch 1

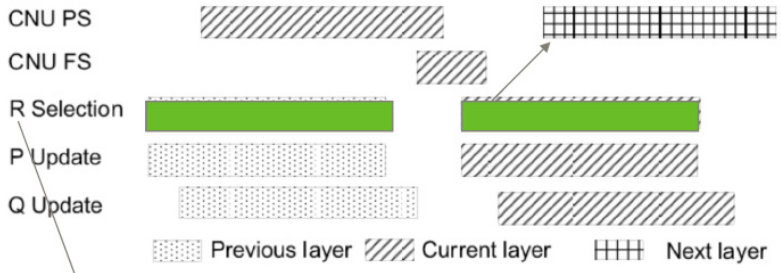


Supports out-of-order processing for PS processing

Out-of-order processing for Rnew

Layer reordering

Out-of-order processing of R_{new}



R selection for R_{new} operates out-of-order to feed the data for PS processing of next layer

Out-of-order layer processing for R Selection

Rate 2/3 A code:

3	0	-1	-1	2	0	-1	3	7	-1	1	1	-1	-1	-1	-1	1	0	-1	-1	-1	-1	-1	-1
-1	-1	1	-1	36	-1	-1	34	10	-1	-1	18	2	-1	3	0	-1	0	0	-1	-1	-1	-1	-1
-1	-1	12	2	-1	15	-1	40	-1	3	-1	15	-1	2	13	-1	-1	-1	0	0	-1	-1	-1	-1
-1	-1	19	24	-1	3	0	-1	6	-1	17	-1	-1	-1	8	39	-1	-1	-1	0	0	-1	-1	-1
20	-1	6	-1	-1	10	29	-1	-1	28	-1	14	-1	38	-1	-1	0	-1	-1	-1	0	0	-1	-1
-1	-1	10	-1	28	20	-1	-1	8	-1	36	-1	9	-1	21	45	-1	-1	-1	-1	-1	0	0	-1
35	25	-1	37	-1	21	-1	-1	5	-1	-1	0	-1	4	20	-1	-1	-1	-1	-1	-1	-1	0	0
-1	6	6	-1	-1	-1	4	-1	14	30	-1	3	36	-1	14	-1	1	-1	-1	-1	-1	-1	-1	0

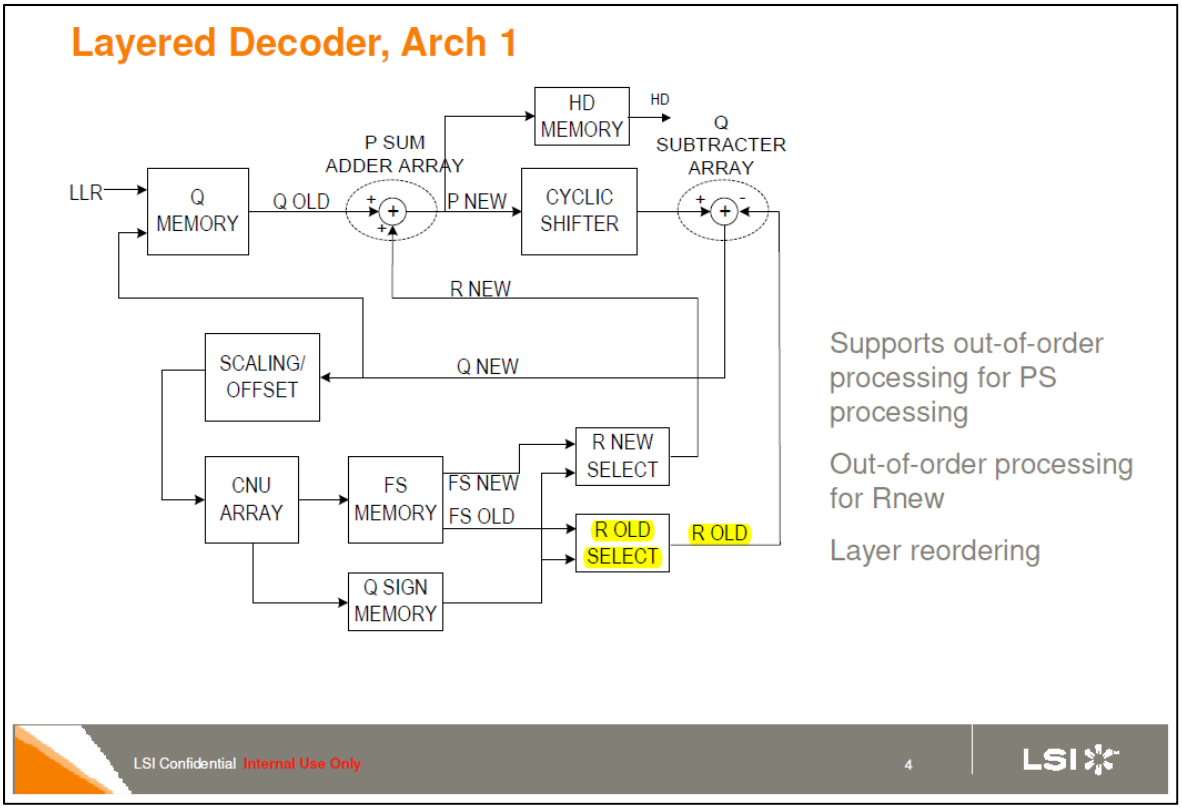
PS processing R selection

R selection is out-of-order so that it can feed the data required for the PS processing of the second layer.

So here we decoupled the execution of R new messages with the execution of CNU processing.

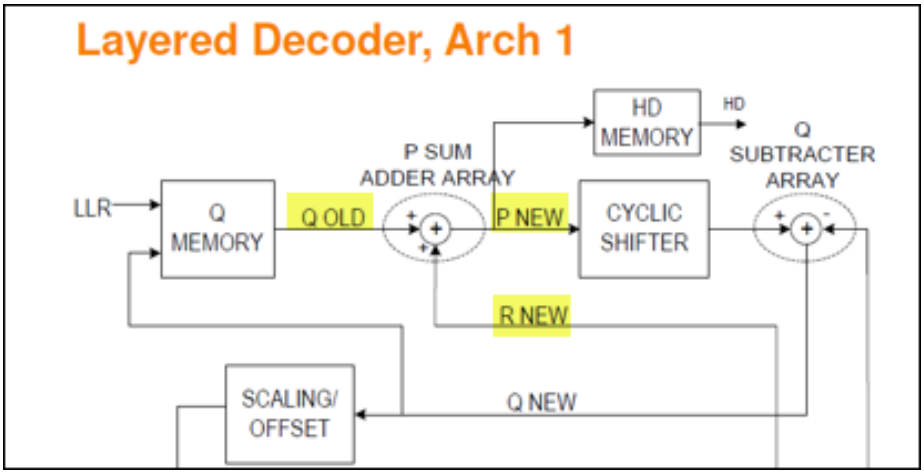
Here we execute the instruction/computation at precise moment when the result is needed!!!

301. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include a control unit configured to cause the decoding circuitry to process each block of the LDPC matrix in processing substeps comprising an R old update substep that selects an R old message, wherein the R old message is produced for a layer of the matrix currently being processed. For example, the Layered Decoder Presentation discloses an R OLD SELECT unit that selects an R old message for a layer of the matrix currently being processed.

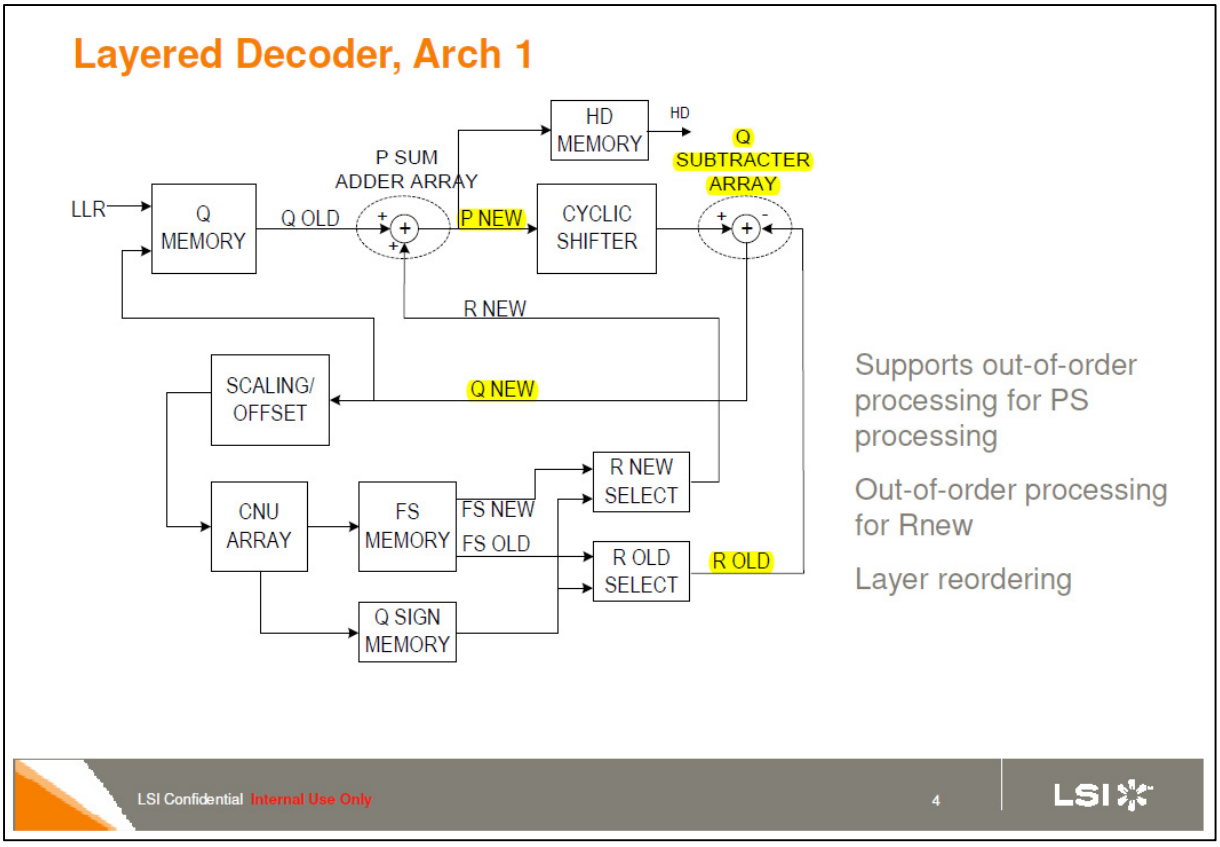


302. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include a control unit configured to cause the decoding circuitry to process each block of the LDPC matrix in processing substeps comprising a P message substep that generates updated P messages. For example, the Layered Decoder

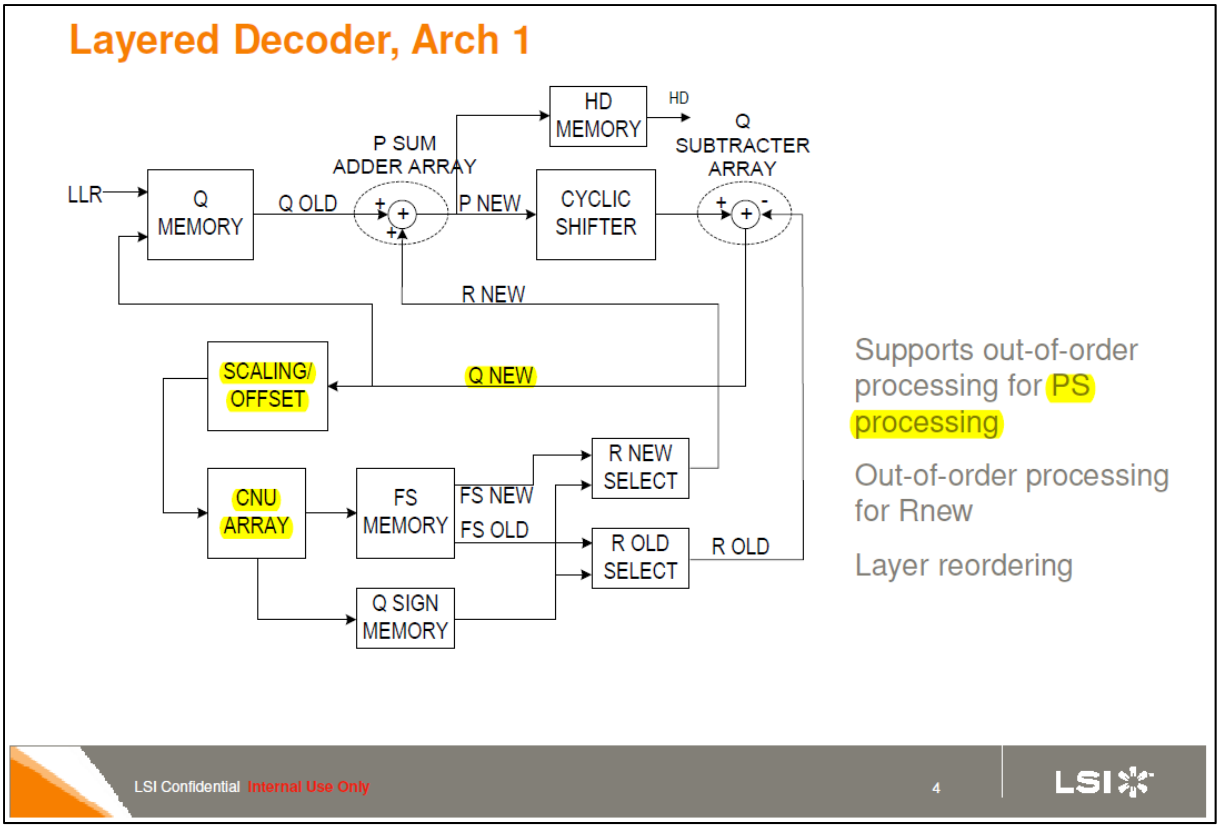
Presentation discloses a P NEW message created by combining the Q OLD message and the R NEW message together.



303. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include a control unit configured to cause the decoding circuitry to process each block of the LDPC matrix in processing substeps comprising a Q message substep that computes variable node messages (Q messages). For example, the Layered Decoder Presentation discloses a Q SUBTRACTER ARRAY that computes variable node messages (Q messages).



304. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products include a control unit configured to cause the decoding circuitry to process each block of the LDPC matrix in processing substeps comprising a partial state substep that updates partial state of a block row based on Q messages computed for the block (check node unit (CNU) Partial state processing). For example, the Layered Decoder Presentation discloses a partial state substep that updates the partial state of a block row based on Q messages computed for the block (check node unit (CNU) Partial state processing).



305. Claim 9 of the '950 Patent recites as follows:

9. A method comprising:
processing blocks of a layer of a low density parity check (LDPC) matrix out of order, the processing of each of the blocks comprising:
an R new update step comprising providing an R new message, the R new message produced for a block of a different layer of the matrix from a layer containing a block currently being processed;
an R old update step comprising selecting an R old message, the R old message produced for a layer of the matrix currently being processed;
a P message step comprising generating updated P messages;
a Q message step comprising computing variable node messages (Q messages); and
a partial state step comprising updating partial state of a block row based on Q messages computed for the block (check node unit (CNU) Partial state processing).

306. On information and belief, the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products satisfy each and every limitation of Claim 9. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products process blocks of a layer of an LDPC matrix out of order. *See* ¶¶ 115, 152, 280, *supra*.

307. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products process each of the blocks comprising an R new update step comprising providing an R new message, the R new message produced for a block of a different layer of the matrix from a layer containing a block currently being processed. *See* ¶¶ 155, 283, *supra*.

308. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products process each of the blocks comprising an R old update step comprising selecting an R old message, the R old message produced for a layer of the matrix currently being processed. *See* ¶¶ 156, 284, *supra*.

309. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products process each of the blocks comprising a P message step comprising generating updated P messages. *See* ¶ 285, *supra*.

310. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products process each of the blocks comprising a Q message step comprising computing variable node messages (Q messages). *See* ¶¶ 157, 286, *supra*.

311. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products process each of the blocks comprising a partial state step

comprising updating partial state of a block row based on Q messages computed for the block (check node unit (CNU) Partial state processing). *See* ¶ 287, *supra*.

312. In view of the foregoing, Defendants and/or the Broadcom Predecessor Entities directly infringe at least Claims 1-16 of the '950 Patent through their internal testing, use, and operation of the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products.

313. On information and belief, Defendants and/or the Broadcom Predecessor Entities should have known that they directly infringe as of the date the '950 Patent issued on or about November 27, 2018, and in any event at least as early as the filing and/or service of Plaintiff's original Complaint. (*See* D.I. 1, 5) Defendants and/or the Broadcom Predecessor Entities are further aware that the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products necessarily practice Claims 1-16 of the '950 Patent.

314. On information and belief, Defendants and/or the Broadcom Predecessor Entities take active steps to induce infringement by others of at least Claims 1-16 of the '950 Patent in violation of 35 U.S.C. §271(b), including, for example, by (a) inducing manufacturers to perform the claimed inventions when testing the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products, and (b) inducing end users to perform the claimed inventions when using the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products. Such active steps include, but are not limited to, selling Accused Hard Disk Controller Products, Accused SandForce Products, and Accused Densbits Products with the knowledge and intent that the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products will be operated

by such manufacturers and their customers in accordance with the claimed inventions, as set forth in the Section "EXAMPLES OF DIRECT AND INDIRECT INFRINGEMENT" below.

315. On information and belief, Defendants and/or the Broadcom Predecessor Entities know or should know that such activities induce others to directly infringe one or more of at least Claims 1-16 of the '950 Patent. For example, Defendants and/or the Broadcom Predecessor Entities should have known that their actions induced others to directly infringe as of the date it became aware of the issuance of the '950 Patent on or about November 27, 2018. Defendants and/or the Broadcom Predecessor Entities were further informed that the technology in the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products infringed the '950 Patent, and Defendants and/or the Broadcom Predecessor Entities knowingly and purposefully continued to exploit the patented technology despite knowing that it was covered by the '950 Patent, as set forth in the Section "EXAMPLES OF DIRECT AND INDIRECT INFRINGEMENT" below.

316. On information and belief, Defendants and/or the Broadcom Predecessor Entities contribute to the infringement of at least Claims 1-16 of the '950 Patent by others, including consumer/end-user use of the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products, in violation of 35 U.S.C. § 271(c). Acts by Defendants and/or the Broadcom Predecessor Entities that contribute to the infringement of others include, but are not limited to, the sale, offer for sale, and/or import by Defendants and/or the Broadcom Predecessor Entities of the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products, and as set forth in the Section "EXAMPLES OF DIRECT AND INDIRECT INFRINGEMENT" below.

317. Such Accused Hard Disk Controller Products, Accused SandForce Products, and Accused Densbits Products are especially made for or adapted for use to infringe, and are not a staple article of commerce and are not suitable for substantial non-infringing use. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products are apparatuses for use in practicing Claims 1-16 of the '950 Patent and are at least a material part of those claimed inventions, for example, as described above with respect to Claim 9. On information and belief, the steps recited in Claim 9, for example, are performed by the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products. As also described above, Defendants and/or the Broadcom Predecessor Entities have, on information and belief, been on notice of the '950 Patent since it issued on November 27, 2018, and in addition since filing and/or service of Plaintiff's original Complaint, and Defendants and/or the Broadcom Predecessor Entities have further been aware that use of the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products necessarily practice the inventions in Claims 1-16 of the '950 Patent. (*See* D.I. 1, 5)

318. The Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products are especially made for or adapted for use to infringe, and are not a staple article of commerce and are not suitable for substantial non-infringing use. By way of example, the use of the LDPC decoders included in the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products is necessary to use the accused products for their intended purpose (decoding data from a hard disk drive, solid state drive, or wireless digital transmission), and the LDPC decoders necessarily perform the claimed inventions when they decode data. Accordingly, the Accused Hard Disk Controller

Products, the Accused SandForce Products, and the Accused Densbits Products do not have a substantial use that does not entail practicing the claimed inventions. On information and belief, the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products cannot be used but to infringe the '950 Patent.

319. Despite Defendants' and/or the Broadcom Predecessor Entities' knowledge, notice, and ongoing infringement of the '950 Patent, Defendants and/or the Broadcom Predecessor Entities continue to test or use the Accused Products in a manner that willfully infringes the '950 Patent, and on information and belief continue to sell and/or offer for sale the Accused Hard Disk Controller Products, the Accused SandForce Products, and the Accused Densbits Products to the United States market for customers / end users to infringe. Defendants' and/or the Broadcom Predecessor Entities' infringement of the '950 Patent is willful, as set forth above. Defendants and/or the Broadcom Predecessor Entities lacked a justifiable belief that they do not infringe the '950 Patent, or that the '950 Patent is invalid or unenforceable, and have acted recklessly in their infringing activity, justifying an increase in the damages to be awarded to Plaintiff up to three times the amount found or assessed, in accordance with 35 U.S.C. § 284.

320. On information and belief, Defendants and/or the Broadcom Predecessor Entities had actual or constructive knowledge of the '950 Patent since at least November 27, 2018, and in any event no later than the filing and/or service of Plaintiff's original Complaint. (*See* D.I. 1, 5) Defendants and/or the Broadcom Predecessor Entities know or should know as of the date of filing and/or service of Plaintiff's original Complaint that their actions induced others to directly infringe the '950 Patent and contributed to infringement of the '950 Patent. (*See* D.I. 1, 5)

321. This case is rendered an exceptional case at least in light of Defendants' and/or the Broadcom Predecessor Entities' willful infringement of the '950 Patent, justifying an award to Plaintiff of its reasonable attorney fees, in accordance with 35 U.S.C. § 285.

322. Plaintiff has no adequate remedy at law for Defendants' and/or the Broadcom Predecessor Entities' acts of infringement. As a direct and proximate result of Defendants' and/or the Broadcom Predecessor Entities' acts of infringement, Plaintiff has suffered and continues to suffer damages and irreparable harm. Unless Defendants' and/or the Broadcom Predecessor Entities' acts of infringement are enjoined by this Court, Plaintiff will continue to be damaged and irreparably harmed.

323. Defendants' and/or the Broadcom Predecessor Entities' infringement of the '950 Patent has damaged and continues to damage Plaintiff in an amount yet to be determined, of at least a reasonable royalty and/or lost profits that Plaintiff would have made but for Defendants' and/or the Broadcom Predecessor Entities' infringement acts.

COUNT VII

(Copyright Infringement under 17 U.S.C. §§ 106 and 501, *et seq.* of "Low Density Parity Check Decoder", U.S. Copyright Registration No. TXu 2-001-020)

324. Plaintiff repeats and re-alleges the paragraphs above as if fully set forth herein.

325. TAMUS is the owner of the copyright in the LDPC Decoder Program Work, which is the subject of U.S. Copyright Registration No. TXu 2-001-020. TAMUS has granted Plaintiff an exclusive licensee to reproduce, distribute, publicly display and perform, and make derivative works from the LDPC Decoder Program Work, grant sublicenses thereto, and to sue for infringement of the copyrights in the LDPC Decoder Program Work.

326. Upon information and belief, Defendants and/or the Broadcom Predecessor Entities have violated and are continuing to violate Plaintiff's exclusive rights in the LDPC

Decoder Program Work by, for example, making and using, and continuing to make and use copies of the LDPC Decoder Program Work, or copies of works that are derivative works of the LDPC Decoder Program Work, in their ongoing engineering and design of the Accused Products, as explained for example in detail in ¶ 51, *supra*, thereby violating Plaintiff's exclusive rights to (a) make reproductions of the LDPC Decoder Program Work or parts thereof, and (b) make derivative works from the LDPC Decoder Program Work. As explained above, LSI substantially copied line-by-line core program modules of the LDPC Decoder Program Work, making only superficial changes to file names and variables, while retaining the work's unique structure, sequence and organization. The LSI "rewrite" therefore constituted unauthorized non-literal copies of the LDPC Decoder Program Work and unauthorized derivative works derived from the LDPC Decoder Program Work. Upon information and belief, LSI, and subsequently Broadcom Inc., continued to use the LDPC Decoder Program Work, the initial LSI "rewrite", and further non-literal copies or derived works in their continuing research and development efforts concerning LDPC decoders used in HDD and SSD controllers and Wi-Fi products. Upon information and belief, such making and using of copies continues to the present day.

327. The acts of Defendants and/or the Broadcom Predecessor Entities constitute copyright infringement under 17 U.S.C. §§ 106 and 501, *et seq.*

328. Defendants and/or the Broadcom Predecessor Entities will continue to infringe Plaintiff's exclusive rights with respect to the LDPC Decoder Program Work unless permanently enjoined by this Court.

329. Defendants' and/or the Broadcom Predecessor Entities' infringement has been willful and purposeful.

330. Plaintiff has been and continues to be damaged by Defendants' and/or the Broadcom Predecessor Entities' acts of infringement, and Plaintiff is entitled to a permanent injunction and an award of its actual damages and any profits of Defendants and/or the Broadcom Predecessor Entities under 17 U.S.C. §§ 502, 504(a)(1), and 504(b).

331. Upon information and belief, the infringing acts of Defendants and/or the Broadcom Predecessor Entities were undertaken and/or continue with knowledge of the Plaintiff's rights and without any good faith basis in law or fact that Defendants' and/or the Broadcom Predecessor Entities' actions were legal, thus Defendants' and/or the Broadcom Predecessor Entities' infringing acts were committed willfully and with reckless disregard of Plaintiff's known rights.

COUNT VIII
(Copyright Infringement under 17 U.S.C. §§ 106 and 501, *et seq.* of "Source Code for Low Density Parity Check Decoder and Its Modules", U.S. Copyright Registration No. TXu 2-033-302)

332. Plaintiff repeats and re-alleges the paragraphs above as if fully set forth herein.

333. TAMUS is the owner of the copyright in the LDPC Decoder Source Code Work, which is the subject of U.S. Copyright Registration No. TXu 2-033-302. TAMUS has granted Plaintiff an exclusive licensee to reproduce, distribute, publicly display and perform, and make derivative works from the LDPC Decoder Source Code Work, grant sublicenses thereto, and to sue for infringement of the copyrights in the LDPC Decoder Source Code Work.

334. Upon information and belief, Defendants and/or the Broadcom Predecessor Entities have violated Plaintiff's exclusive rights in the LDPC Decoder Source Code Work by, for example, making and using and continuing to make and use copies of the LDPC Decoder Source Code Work, or copies of works that are derivative works of the LDPC Decoder Source Code Work, in their ongoing engineering and design of the Accused Products, as explained for

example in detail in ¶ 51, *supra*, thereby violating Plaintiff's exclusive rights to (a) make reproductions of the LDPC Decoder Source Code Work or parts thereof, and (b) make derivative works from the LDPC Decoder Source Code Work. As explained above, LSI substantially copied line-by-line core program modules of the LDPC Decoder Source Code Work, making only superficial changes to file names and variables, while retaining the work's unique structure, sequence and organization. The LSI "rewrite" therefore constituted unauthorized non-literal copies of the LDPC Decoder Source Code Work and unauthorized derivative works derived from the LDPC Decoder Source Code Work. Upon information and belief, LSI, and subsequently Broadcom Inc., continued to use the LDPC Decoder Source Code Work, the initial LSI "rewrite", and further non-literal copies or derived works in their continuing research and development efforts concerning LDPC decoders used in HDD and SSD controllers and Wi-Fi products. Upon information and belief, such making and using of copies continues to the present day.

335. The acts of Defendants and/or the Broadcom Predecessor Entities constitute copyright infringement under 17 U.S.C. §§ 106 and 501, *et seq.*

336. Defendants and/or the Broadcom Predecessor Entities will continue to infringe Plaintiff's exclusive rights with respect to the LDPC Decoder Source Code Work unless permanently enjoined by this Court.

337. Defendants' and/or the Broadcom Predecessor Entities' infringement has been willful and purposeful.

338. Plaintiff has been and continues to be damaged by Defendants' and/or the Broadcom Predecessor Entities' acts of infringement, and Plaintiff is entitled to a permanent

injunction and an award of its actual damages and any profits of Defendants and/or the Broadcom Predecessor Entities under 17 U.S.C. §§ 502, 504(a)(1), and 504(b).

339. Upon information and belief, the infringing acts of Defendants and/or the Broadcom Predecessor Entities were undertaken and/or continue with knowledge of the Plaintiff's rights and without any good faith basis in law or fact that Defendants' and/or the Broadcom Predecessor Entities' actions were legal, thus Defendants' and/or the Broadcom Predecessor Entities' infringing acts were committed willfully and with reckless disregard of Plaintiff's known rights.

COUNT IX
(Copyright Infringement under 17 U.S.C. §§ 106 and 501, *et seq.* of "Source Code for Certain Low Density Parity Check Algorithms", U.S. Copyright Registration No. TXu 1-842-620)

340. Plaintiff repeats and re-alleges the paragraphs above as if fully set forth herein.

341. TAMUS is the owner of the copyright in the LDPC Algorithms Source Code Work, which is the subject of U.S. Copyright Registration No. TXu 1-842-620. TAMUS has granted Plaintiff an exclusive licensee to reproduce, distribute, publicly display and perform, and make derivative works from the LDPC Algorithms Source Code Work, grant sublicenses thereto, and to sue for infringement of the copyrights in the LDPC Algorithms Source Code Work.

342. Upon information and belief, Defendants and/or the Broadcom Predecessor Entities have violated Plaintiff's exclusive rights in the LDPC Algorithms Source Code Work by, for example, making and using, and continuing to make and use copies of the LDPC Algorithms Source Code Work, or copies of works that are derivative works of the LDPC Algorithms Source Code Work, in their its ongoing engineering and design of the Accused Products, as explained for example in detail in ¶ 51, *supra*, thereby violating Plaintiff's exclusive rights to (a) make

reproductions of the LDPC Algorithms Source Code Work or parts thereof, and (b) make derivative works from the LDPC Algorithms Source Code Work. As explained above, LSI substantially copied line-by-line core program modules of the LDPC Algorithms Source Code Work, making only superficial changes to file names and variables, while retaining the work's unique structure, sequence and organization. The LSI "rewrite" therefore constituted unauthorized non-literal copies of the LDPC Algorithms Source Code Work and unauthorized derivative works derived from the LDPC Algorithms Source Code Work. Upon information and belief, LSI, and subsequently Broadcom Inc., continued to use the LDPC Algorithms Source Code Work, the initial LSI "rewrite", and further non-literal copies or derived works in their continuing research and development efforts concerning LDPC decoders used in HDD and SSD controllers and Wi-Fi products. Upon information and belief, such making and using of copies continues to the present day.

343. The acts of Defendants and/or the Broadcom Predecessor Entities constitute copyright infringement under 17 U.S.C. §§ 106 and 501, *et seq.*

344. Defendants' and/or the Broadcom Predecessor Entities' infringement has been willful and purposeful.

345. Defendants and/or the Broadcom Predecessor Entities will continue to infringe Plaintiff's exclusive rights with respect to the LDPC Algorithms Source Code Work unless permanently enjoined by this Court.

346. Plaintiff has been and continues to be damaged by Defendants' and/or the Broadcom Predecessor Entities' acts of infringement, and Plaintiff is entitled to a permanent injunction and an award of its actual damages and any profits of Defendants and/or the Broadcom Predecessor Entities under 17 U.S.C. §§ 502, 504(a)(1), and 504(b).

347. Upon information and belief, the infringing acts of Defendants and/or the Broadcom Predecessor Entities were undertaken and/or continue with knowledge of the Plaintiff's rights and without any good faith basis in law or fact that Defendants' and/or the Broadcom Predecessor Entities' actions were legal, thus Defendants' and/or the Broadcom Predecessor Entities' infringing acts were committed willfully and with reckless disregard of Plaintiff's known rights.

EXAMPLES OF DIRECT AND INDIRECT INFRINGING BEHAVIOR

348. Plaintiff repeats and re-alleges the paragraphs above as if fully set forth herein.

349. On information and belief, Defendants have committed direct and indirect patent infringement (both inducement and contributory infringement) as set forth above in several ways, including the exemplary ways set forth in this section.

350. First, with respect to direct infringement, Defendants have [redacted] Accused Products in or from the United States.

351. Defendants' sales [redacted].

352. On information and belief, Defendants [redacted] have sold products throughout the world from their U.S.-based locations and involving sales and support employees in the U.S.

353. [redacted]

354. [redacted]

355. [redacted]

356. [redacted]

357. [redacted]

358. [redacted]

[redacted]

359. [redacted] Defendants know and encourage the sale of Accused Products contained within other products directed (hereinafter, "End Products") sold in the U.S.

360. On information and belief, Defendants are aware of, track, and maintain a database of customers and End Products containing an Accused Product.

361. Further, Defendants know that Accused Products [redacted].

362. Defendants further know or are willfully blind to the fact that [redacted]

363. Accordingly, when Defendants or a related entity sells an Accused Product to a customer for incorporation into and use in an End Product that Defendants know or are willfully blind to the fact that such End Product is sold in the United States, Defendants are knowingly encouraging acts of infringement in the United States.

364. Because Defendants have committed these acts involving sales of Accused Products and sales of End Products containing Accused Products in the U.S. with knowledge of the Asserted Patents and the fact that their Accused Products infringe them (as set forth above), these actions constitute inducement and contributory infringement.

365. One exemplary sales technique for Defendants includes Defendants [redacted].

366. On information and belief, Defendants [redacted]

367. On information and belief, the identity of some or all End Customers [redacted]

368. Defendants also indirectly infringe by providing [redacted]

369. As noted above, on information and belief, Defendants seek to [redacted] (hereafter referred to as "Overseas Entities that Target the U.S. Market") [redacted]

370. On information and belief, Defendants have technical information showing which Accused Products are sold to Overseas Entities that Target the U.S. Market [redacted]

371. On information and belief, Defendants have marketing information showing which Accused Products are sold to Overseas Entities that Target the U.S. Market [redacted]

372. On information and belief, Defendants have financial information showing which products are sold to Overseas Entities that Target the U.S. Market [redacted]

373. [redacted]

374. [redacted]

375. [redacted]

[redacted]

376. The end result of this scheme is that Defendants knowingly [redacted] to infringe the Patents-in-Suit.

377. Defendants' knowledge of this infringement can be seen from their promotion of Accused Products made overseas to U.S. businesses and consumers.

378. For example, on March 4, 2021 Broadcom posted a press release available at https://www.broadcom.com/blog/wi-fi-6-milestone-to-celebrate celebrating the shipment of over 500 million Accused Products that are Wi-Fi 6-compatible chips.

379. As part of this March 4, 2021 press release, Broadcom touted that Accused Products are used in "MLB, NBA, and NFL stadiums across the United States."

380. On information and belief, Broadcom does not sell Accused Products directly to the stadiums hosting MLB, NBA, or NFL games, but rather sells Accused Products to an Overseas Entities that Target the U.S. Market, who incorporates Accused Products into End Products imported into the U.S. Defendants, however, know that the Accused Products are imported back into the United States by others for use in the stadiums hosting MLB, NBA, and NFL games, and other venues around the U.S., and encourage the importation, as this March 4, 2021 press release, indicates.

381. Indeed, on September 24, 2021, Extreme Networks, a Broadcom customer posted an interview with Vijay Nagarajan, Vice President of Mobile Connectivity at Broadcom, Inc. (available at https://www.youtube.com/watch?v=oNPWMy_1uJU). Mr. Nagarajan, on behalf of Broadcom, Inc., described Extreme Networks as an "important Broadcom partner." The video

was part of a series called "Connected by Broadcom." The interview was conducted with Ed Meyercord of Extreme Networks:

382. During the interview referenced in the preceding paragraph of this Complaint, Mr. Meyercord states that numerous U.S. large institutions are "running on Broadcom." Mr. Meyercord informs Broadcom that the Accused Products are used or will soon be used to provide WiFi service to stadiums in the NFL, NBA, and MLB. Mr. Meyercord further notes that the first "all-digital Superbowl…ran on Broadcom."

383. As noted above, Broadcom was already aware that the Accused Products are sold in the United States by Overseas Entities that Target the U.S. Market or their customers. *See* https://www.broadcom.com/blog/wi-fi-6-milestone-to-celebrate (stating that "Our chips are also an integral part of Wi-Fi 6 installations in major MLB, NBA, and NFL stadiums across the United States").

384. On information and belief, Broadcom markets the Accused Products specifically to Overseas Entities that Target the U.S. Market with the knowledge and intent that those companies sell End Products containing the Accused Products within the United States.

385. The Extreme Network's website touts sales of End Products including the Accused Products to "50,000 leading organizations" including many large organizations within the U.S. On October 14, 2021, Broadcom retweeted a posting from Extreme Networks saying that "Broadcom is the backbone of our new AP4000 access points." On information and belief, the Country of Origin for the AP4000 is China.

386. Extreme Networks even uses Broadcom's trademark on their website for products:

387. On information and belief, Defendants authorized Extreme Networks to use their "Built on BROADCOM" mark to advertise products for the U.S. market, and are thus knowingly encouraging and assisting in the sale of Accused Products in the United States.

388. The AP4000 shown above is one of numerous End Products that Defendants know of and intend to be sold to End Customers in the United States containing the Accused

Products. *See* https://www.cdw.com/product/extreme-networks-6e-2.4-5ghz-tri-radio-wireless-access-point/6679166.

389. On information and belief, Defendants are aware and intend for products sold for use in Extreme Networks products to be resold by Extreme Networks to U.S. businesses and consumers.

390. Additionally, on information and belief, Defendants provide technical support to Extreme Networks and other Overseas Entities that Target the U.S. Market in the design and deployment of Accused Products within the U.S.

391. Defendants' activities in support of Overseas Entities that Target the U.S. Market provide further knowledge to Defendants that the Accused Products conveyed overseas are being imported into and sold in the United States. For at least these reasons, Defendants partner with and encourage infringement of the Patents-in-Suit within the United States by Overseas Entities that Target the U.S. Market.

392. On information and belief, Extreme Networks [redacted]

393. To the extent, that Defendants have authorized any other U.S. sellers to use the "Built on BROADCOM" mark, Defendants are encouraging infringement by those companies in the United States.

394. In further example, Broadcom has issued press releases in which they touted that companies such as Aerohive, Netgear, and Linksys incorporate Accused Products into End Products that are sold in the United States.

395. For example, in a March 4, 2021 press release touting the fact that over 500 million Accused Products had been shipped by that date, Broadcom specifically highlighted End Product routers from customer Netgear. See https://www.broadcom.com/blog/wi-fi-6-milestone-to-celebrate.

396. David Henry, Netgear's senior vice president of connected home products, stated that "Netgear is excited to partner with Broadcom to build a portfolio of Wi-Fi 6E enabled products." https://www.cnet.com/home/internet/broadcom-jumps-in-with-wi-fi-6e-chipsets-for-better-more-capable-routers/.

397. Defendants advertise that Accused Products "are being deployed by NETGEAR with its Nighthawk product line." See https://www.broadcom.com/company/news/product-releases/41051. This advertisement describes "Broadcom's close collaboration with NETGEAR" on the Accused Products. Broadcom then directs customers to the NETGEAR website at https://www.Netgear.com/AX-WIFI. This website is an e-commerce site for U.S. customers to purchase End Products containing and employing the Accused products, such as the Nighthawk product line.

398. On information and belief, the NETGEAR Nighthawk product line is manufactured in [redacted] for sale in the US.

399. Broadcom also directs customers to industry review website for imported End Products that include the Accused Products. *See* https://www.broadcom.com/blog/broadcom-ships-one-billion-wi-fi-6-and-6e-chips (providing a link to review of the NETGEAR routers along with links to purchase them). Broadcom obviously knows that NETGEAR sells End Products containing the Accused Products to customers in the United States and sells Accused

Products to NETGEAR or parties partnering with NETGEAR with the intention and design that they be resold in the United States.

400. On information and belief, NETGEAR [redacted]

401. On information and belief, Defendants' business model for the Accused Products relies on such partnerships with Overseas Entities that Target the U.S. Market to account for the bulk of its sales.

402. Further, Defendants have advertised a plan to distribute the Accused Product to U.S. customers, entitled "Connecting America: Broadband is critical infrastructure." *See* https://www.broadcom.com/blog/connecting-america-broadband-as-critical-infrastructure. This article evidences a plan by Defendants to increase broadband use in the United States.

403. Given that Defendants themselves are not believed to manufacture Wi-Fi End Products, on information and belief, Defendants' intention is to encourage U.S. consumers to purchase End Products containing the Accused Products in order to "Connect America" using the Accused Products.

404. Without the technology set forth in the Patents-in-Suit, Defendants' goals of "Connect[ing] America" would not be possible.

405. Defendants also produce a video series entitled "Connected by Broadcom" where they have asked companies that sell Accused Products in the United States to discuss and advertise their resale of the Accused Products within End Products.

406. In one of these "Connected by Broadcom" interviews, Broadcom, Inc. Vice President Vijay Nagarajan stated that "many of the Broadband modems in the US Homes" are built by companies believed to integrate the Accused Products into their product overseas for importation into the U.S. This series contains numerous interviews with executives at companies that Broadcom knows and encourages to the import Accused Products into the U.S. for the purpose of infringing.

407. Beyond this, on information and belief, Broadcom has sought and obtained FCC approval for the Accused Wi-Fi Products to be sold and used in the United States. *See, e.g.,* https://www.broadcom.com/blog/bcm4389-worlds-first-fcc-certified-wi-fi-6e-chip#:~:text=On%20December%207%2C%202020%2C%20the,a%20gratifying%20moment%20for%20Broadcom (touting FCC approval of the Accused BCM4389 product).

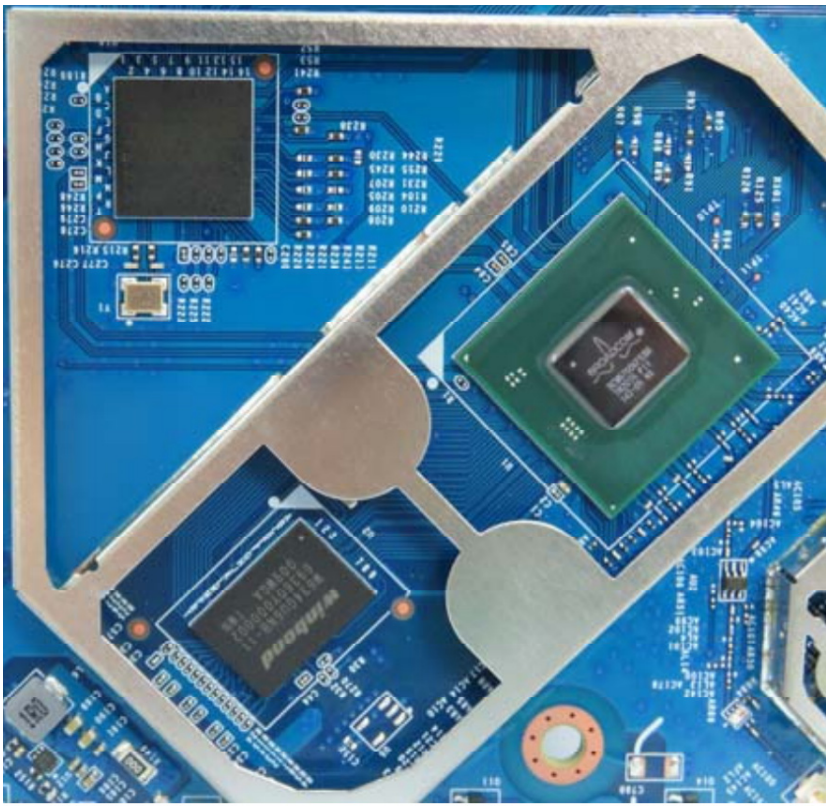
408. Defendants have similarly sought FCC clearance for most (if not all) of the Accused Wi-Fi products.

409. Defendants have similarly received FCC clearance for most (if not all) of the Accused Wi-Fi products.

410. On information and belief, Defendants have sought and continue to seek FCC approval for the Accused Wi-Fi Products because they market those products to Overseas Entities that Target the U.S. Market as preapproved for sale in the United States. These actions by Defendants show knowledge and intent that sales of Accused Products to be incorporated into End Products overseas will be imported into the United States for sale and use in the United States.

411. Moreover, on information and belief, Defendants know that their customers file approval requests with the FCC prior to selling End Products containing Accused Products in the

United States. These approval documents, which are publicly available, show that customers of Defendants are selling or intending to sell End Products containing Accused Products within the United States. *See, e.g.*, https://fcc.report/FCC-ID/PY320100480/4876159.pdf (showing an Accused Product within an End Product router intended for U.S. sale):



412. On information and belief, Defendants' marketing personnel track many of the End Products of their customers and know/intend that the Accused Products will be included in End Products sold in the U.S.

413. Independent industry estimates place the North American share of the global Wi-Fi chip market at roughly 25%. See https://markets.businessinsider.com/news/stocks/wi-fi-6-and-wi-fi-6e-market-technology-and-competition-assessment-2020-2026-featuring-profiles-of-broadcom-qualcomm-on-semiconductor-intel-and-more-1030225071.

414. On information and belief, the U.S. makes up the majority of the Defendants' North American sales.

415. On information and belief, Defendants have marketing information that shows the approximate U.S. share of their sales.

416. Defendants recently advertised the sale of their one-billionth WiFi6 compatible Accused Product chip. Wifi6 chips containing LDPC decoders are Accused Products in this case. While Defendants have not, as of the filing of this Complaint, provided any U.S. sales data figures, those U.S. sales figures should align with the industry trends and geography.

JURY TRIAL DEMAND

Pursuant to Federal Rule of Civil Procedure 38(b), Plaintiff hereby demands a trial by jury of all issues so triable.

REQUESTED RELIEF

Plaintiff respectfully seeks the following relief:

a) The entry of judgment holding that Defendants have infringed each of the '023, '140, '530, '522, '250, and '950 Patents;

b) The entry of a permanent injunction pursuant to 35 U.S.C. § 283 enjoining Defendants, its officers, agents, attorneys, and employees, and those acting or attempting to act in active concert with them or acting on their behalf, from infringing any of the '023, '140, '530,'522, '250, and '950 Patents by engaging in any commercial manufacture, use, offer to sell, or sale within the United States, or importation into the United States, or engaging in any effort to sell to Overseas Customers that Target the U.S. Market, of any product covered by the '023, '140, '530, '522, '250, and '950 Patents for the full terms thereof or any additional period of

exclusivity to which Plaintiff and/or such Patents are, or become, entitled, and from inducing or contributing to such activities;

c) The entry of an order declaring that Plaintiff be awarded damages in an amount sufficient to compensate it for Defendants' infringement of the '023, '140,'530, '522, '250, and '950 Patents, together with prejudgment and post-judgment interest and costs;

d) The entry of an order declaring that Plaintiff be awarded enhanced damages pursuant to 35 U.S.C. § 284 for Defendants' willful patent infringement;

e) That Defendants be ordered to provide an accounting for the damages resulting from infringement of the Patents-in-Suit, together with interests and costs, and all other damages permitted by 35 U.S.C. § 284 (2012), including an accounting for infringing acts not presented at trial and an award by the court of additional damages for any such infringing acts;

f) The entry of an injunction, pursuant to 17 U.S.C. § 502, permanently enjoining Defendants from reproducing, publishing, posting, copying, offering to copy, or otherwise distributing, and from making any derivative works of, the TAMUS Copyrighted Works, including all versions thereof;

g) Award Plaintiff its damages, in addition to Defendants' profits, as a result of Defendants' acts of copyright infringement;

h) That Defendants be ordered to provide an accounting for the damages resulting from infringement of the of the TAMUS Copyrighted Works, and all other damages permitted by 17 U.S.C. § 504, including an accounting for infringing acts not presented at trial and an award by the court of additional damages for any such infringing acts;

i) In the alternative, and if Plaintiff so elects, award Plaintiff statutory damages pursuant to 17 U.S.C. § 504, *et seq.* per each of the TAMUS Copyrighted Works infringed by

Defendants, including damages on account of Defendants' willful infringement of the TAMUS Copyrighted Works;

j) The entry of an order declaring that this is an exceptional case and awarding Plaintiff its costs, expenses, and reasonable attorney fees under 35 U.S.C. § 285 and 17 U.S.C. § 505 and all other applicable statutes, rules, and common law;

k) The taxation of all allowable costs against Defendants; and

l) An award to Plaintiff of any other relief that the Court deems just and proper under the circumstances.

Dated: April 27, 2022

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