UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
WACO DIVISION

MIMO RESEARCH, LLC, ***Plaintiff,*** v. **INTEL CORPORATION,** ***Defendant.***	**Civil Action No. 6:22-cv-542** **JURY TRIAL DEMANDED**

COMPLAINT FOR PATENT INFRINGEMENT

MIMO Research, LLC ("MIMO Research" or "Plaintiff") brings this action and makes the following allegations of patent infringement relating to U.S. Patent Nos.: 7,091,854 (the "'854 patent") and 7,200,166 (the "'166 patent") (collectively, the "patents-in-suit"). Defendant Intel Corporation ("Intel" or "Defendant") infringes the patents-in-suit in violation of the patent laws of the United States of America, 35 U.S.C. § 1 *et seq*.

THE PARTIES

1. Plaintiff MIMO Research, LLC ("Plaintiff" or "MIMO Research") is a New York limited liability company established in 2017. MIMO Research owns a portfolio of patents that cover Multiple Input Multiple Output ("MIMO") wireless communication, powerline networking, and ultra-wideband ("UWB") technology. MIMO Research is the owner of all rights, title, and interest in and to the patents-in-suit.

2. Highlighting the importance of the patents-in-suit is the fact that the MIMO Research's patent portfolio has been cited by over 800 U.S. and international patents and patent applications assigned to a wide variety of the largest companies operating in the wireless integrated circuit field. MIMO Research's patents have been cited by companies such as:

- Apple Inc.[1]
- Samsung Electronics Co., Ltd. [2]
- Broadcom Inc.[3]
- STMicroelectronics N.V. [4]
- Sony Group Corporation[5]
- Nokia Corporation[6]
- Qualcomm, Inc.[7]
- Siemens AG[8]
- Fujitsu Limited[9]

3. Defendant Intel Corporation ("Intel") is a corporation organized and existing under the laws of the state of Delaware. Intel has regular and established places of business in this District, including at 1300 S. Mopac Expressway, Austin, Texas 78746 and at 9442 N Capital of Texas Hwy, Bldg. 2, Suite 600, Austin, Texas 78759.

4. Intel states that it is "Innovating and Investing in Texas" and "We're proud to call Texas home."[10] Intel's facilities in the Western District of Texas include a research and

[1] *See, e.g.*, U.S. Patent Nos. 7,548,577; 8,279,913; 8,705,641; 8,743,852; 8,958,760; 9,490,864; and 9,614,578.

[2] *See, e.g.*, U.S. Patent Nos. 8,478,271; 7,929,995; 7,305,250; 7,392,012; 7,969,859; 9,002,304; and 9,306,616.

[3] *See, e.g.*, U.S. Patent Nos. 7,885,323; 8,520,715; 7,680,083; 7,725,096; 7,795,973; 7,808,985; 7,860,146; 7,873,324; 7,877,078; 7,899,436; 7,956,689; 8,160,127; 8,213,895; 8,406,239; 8,437,387; 8,509,707; 8,750,362; 8,750,392; 8,885,814; 9,042,436; 9,065,465; 9,313,828; and 9,936,439.

[4] *See, e.g.*, U.S. Patent Nos. 7,660,342; 7,656,932; 7,660,341; 7,817,763; and 8,817,935.

[5] *See, e.g.*, U.S. Patent Nos. 9,265,004; 7,542,728; 7,545,787; 7,567,820; 7,688,784; 7,822,436; 7,881,252; 8,045,447; 8,121,144; 8,160,001; 8,259,823; 8,462,746; 9,036,569; 9,237,572; 9,258,833; 8,660,196; and 9,276,649.

[6] *See, e.g.*, U.S. Patent Nos. 7,499,674; 7,643,811; 7,697,893; 7,782,894; and 9,913,248.

[7] *See, e.g.*, U.S. Patent Nos. 8,767,812; 9,300,491; 7,916,081; 8,009,775; 8,054,223; 8,401,503; 8,452,294; 8,467,331; 8,472,551; 8,743,903; 8,745,137; 8,745,695; 8,774,334; and 8,824,477.

[8] *See, e.g.*, U.S. Patent Nos. 7,378,980; 7,382,271; 7,408,839; 8,155,664; and 10,051465.

[9] *See, e.g.*, U.S. Patent Nos. 7,702,022; 7,995,680; 8,761,275; and 8,938,017.

[10] *Intel in Texas,* INTEL WEBSITE (last visited May 2022), *available at*: https://www.intel.com/content/www/us/en/corporate-responsibility/intel-in-texas.html

development center where roughly 1,800 employees are employed in "experienced positions across hardware, software, and more."[11]

JURISDICTION AND VENUE

5. This action arises under the patent laws of the United States, Title 35 of the United States Code. Accordingly, this Court has exclusive subject matter jurisdiction over this action under 28 U.S.C. §§ 1331 and 1338(a).

6. This Court has personal jurisdiction over Intel in this action because Intel has committed acts within the Western District of Texas giving rise to this action and has established minimum contacts with this forum such that the exercise of jurisdiction over Intel would not offend traditional notions of fair play and substantial justice. Defendant Intel, directly and/or through subsidiaries or intermediaries (including distributors, retailers, and others), has committed and continues to commit acts of infringement in this District by, among other things, offering to sell and selling products and/or services that infringe the patents-in-suit. Moreover, Intel is registered to do business in the State of Texas, has offices and facilities in the State of Texas, and actively directs its activities to customers located in the State of Texas.

7. Venue is proper in this district under 28 U.S.C. §§ 1391(b)-(d) and 1400(b). Defendant Intel is registered to do business in the State of Texas, has offices in the State of Texas, has transacted business in the Western District of Texas and has committed acts of direct and indirect infringement in the Western District of Texas.

8. Intel has a regular and established place of business in this District and has committed acts of infringement in this District. Intel has also committed acts of infringement in

[11] *Id.*

this District by commercializing, marketing, selling, distributing, testing, and servicing certain Accused Products.

9. This Court has personal jurisdiction over Intel. Intel has conducted and does conduct business within the State of Texas. Intel, directly or through subsidiaries or intermediaries (including distributors, retailers, and others), ships, distributes, makes, uses, offers for sale, sells, imports, and/or advertises (including by providing an interactive web page) its products and/or services in the United States and the Western District of Texas and/or contributes to and actively induces its customers to ship, distribute, make, use, offer for sale, sell, import, and/or advertise (including the provision of an interactive web page) infringing products and/or services in the United States and the Western District of Texas. Intel, directly and through subsidiaries or intermediaries (including distributors, retailers, and others), has purposefully and voluntarily placed one or more of its infringing products and/or services, as described below, into the stream of commerce with the expectation that those products will be purchased and used by customers and/or consumers in the Western District of Texas. These infringing products and/or services have been and continue to be made, used, sold, offered for sale, purchased, and/or imported by customers and/or consumers in the Western District of Texas. Intel has committed acts of patent infringement within the Western District of Texas. Intel interacts with customers in Texas, including through visits to customer sites in Texas. Through these interactions and visits, Intel directly infringes the patents-in-suit. Intel also interacts with customers who sell the Accused Products into Texas, knowing that these customers will sell the Accused Products into Texas, either directly or through intermediaries.

10. Intel has minimum contacts with this District such that the maintenance of this action within this District would not offend traditional notions of fair play and substantial justice. Thus, the Court therefore has both general and specific personal jurisdiction over Intel.

THE ASSERTED PATENTS

U.S. PATENT NO. 7,091,854

11. U.S. Patent No. 7,091,854 (the "'854 patent") entitled, *Multiple-Input Multiple-Output Wireless Sensor Networks Communications,* was filed on April 9, 2004. The '854 patent is subject to a 35 U.S.C. § 154(b) term extension of 187 days. MIMO Research, LLC is the owner by assignment of the '854 patent. A true and correct copy of the '854 patent is attached hereto as Exhibit A.

12. The '854 patent claims specific systems for wireless multiple-input multiple-output communication devices.

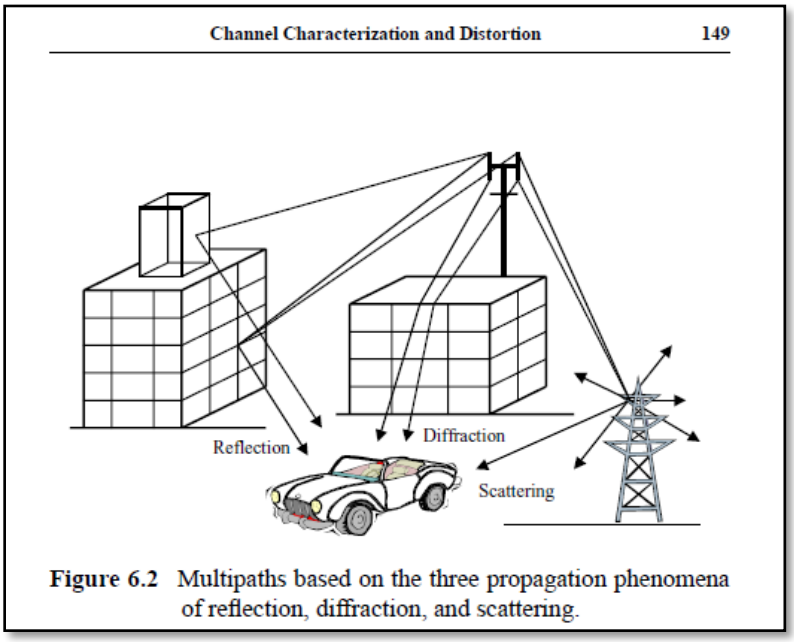
13. The '854 patent teaches the use of a MIMO sensor transmitter that improves array gain, diversity, and reduces channel interference and inter-symbol interference.

14. The '854 patent teaches the use of a sensor array unit coupled to an analog-to-digital converter which is coupled to a signal processing and data computing unit. The signal processing and data computing unit are coupled to a MIMO transceiver containing multiple antennas. This system improves average signal power, mitigates fading, and reduces channel interference and intersymbol interference. The reduction in channel and intersymbol interference allows the systems claimed in the '854 patent to significantly improve the capacity, coverage, and quality of wireless communication.

15. The inventions taught in the '854 patent boost the data rate not only on uplink channels but also on downlink channels, which allows for better communication and control between wireless devices.

16. The '854 patent teaches the use of a MIMO transceiver to overcome multipath propagation. Multipath propagation arises from scattering, reflection, refraction or diffraction of the radiated energy off objects in the environment. Thus, received signals are much weaker than transmitted signals due to mean propagation loss. In addition to a mean path loss, the received signals exhibit fluctuations in a signal level that is referred to as fading.

17. The '854 patent is directed to overcoming problems attendant to multipath propagation which occurs through the reflection, diffraction, and scattering of a wireless signal. "The multipath propagation arises from scattering, reflection, refraction or diffraction of the radiated energy off objects in the environment." '854 patent, col. 2:43-45. The inventor of the '854 patent illustrated the problem of multipath propagation in a subsequent textbook on signal processing.



George J. Maio, SIGNAL PROCESSING IN DIGITAL COMMUNICATIONS at 149 (2006).

18. The '854 patent teaches the use of a MIMO transceiver which turns multipath propagation into a benefit. By combining the use of the transmitter antennas at one end and receiver antennas, the systems taught in the '854 patent enhance wireless transmission over the MIMO channel.

19. The inventor of '854 patent described the problem of multipath propagation in a 2006 textbook on signal processing:

> Wireless channels experience multipath propagation due to reflection, diffraction, and/or scattering of radiated energy off of objects located in the environment. Signals at the receiver are much feebler than transmitted signals because of propagation path loss. In addition, received signals may display fading over traveling distance from the transmitter. The fading includes large-scale fading and small-scale fading.

George J. Maio, SIGNAL PROCESSING IN DIGITAL COMMUNICATIONS at 184-85 (2006).

20. The '854 patent has been cited by 61 United States and international patents and patent applications as relevant prior art. Specifically, patents issued to the following companies and research institutions have cited the '854 patent as relevant prior art:

- Qualcomm, Inc.
- NEC Corporation
- Samsung Electronics Co., Ltd.
- Allied Telesis Holdings K.k.
- University Of Virginia
- Texas Instruments Incorporated
- Honeywell International Inc.
- Shanghai Jiaotong University
- Zebra Technologies Corp.
- The Boeing Company
- Chinese Academy of Sciences
- Itron, Inc.
- HBX Control Systems, Inc.

U.S. PATENT NO. 7,200,166

21. U.S. Patent No. 7,200,166 ("the '166 patent") entitled, *Dual-Mode Transceiver For Indoor And Outdoor Ultra Wideband Communications,* was filed on July 10, 2003. The '166

patent is subject to a 35 U.S.C. § 154(b) term extension of 768 days. MIMO Research, LLC is the owner by assignment of the '166 patent. A true and correct copy of the '166 patent is attached hereto as Exhibit B.

22. The '166 patent claims specific systems for a dual-mode digital lowpass shaping finite impulse response (FIR) filter.

23. The '166 patent is directed to enabling a communication device to operate in a dual mode where each mode has different emission masks and/or frequency bands.

24. The '166 patent is directed to allowing a single communication device to operate in a dual mode by employing a dual-mode architecture through digital transmission-shaping filters and receiver filters for two modes of operations.

25. The '166 patent teaches use of a digital lowpass-shaping FIR transmission filter to enable a dual-mode system. Further, the '166 patent teaches a FIR transmission filter wherein the filter is a filter whose impulse response is of a finite duration as the filter settles to zero after a period of time.

26. The '166 patent teaches improvements to communication devices where operating in two or more modes is required where the modes include different masks of emissions limitations.

27. The '166 patent is directed to addressing the continuing need for a communication transceiver employing a dual-mode architecture of digital transmission-shaping filters and receiver filters for operating in two modes.

28. The '166 patent has been cited by 15 United States and international patents and patent applications as relevant prior art. Specifically, patents issued to the following companies and research institutions have cited the '166 patent as relevant prior art:

- Samsung Electronics Co., Ltd.
- Qualcomm, Inc.
- Tata Sons Ltd.
- Interuniversity Microelectronics Centre
- Shandong Academy of Science Institute of Automation

COUNT I
INFRINGEMENT OF U.S. PATENT NO. 7,091,854

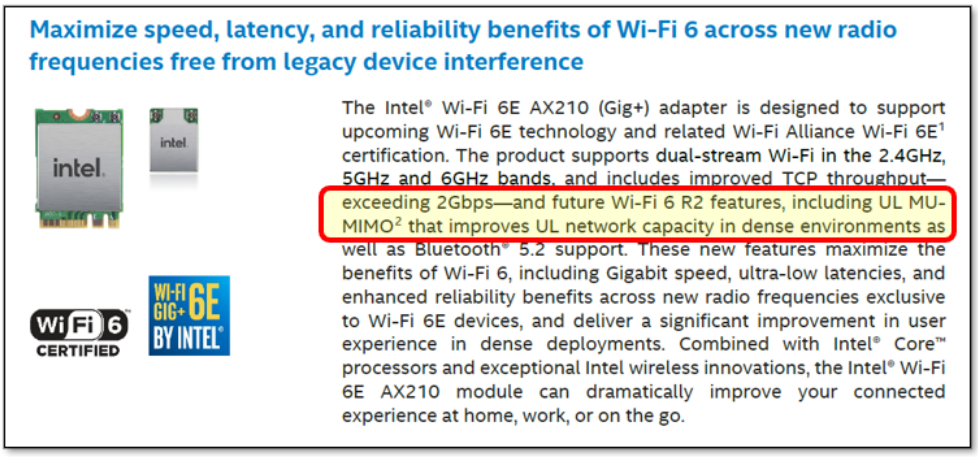
29. Plaintiff references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

30. Intel designs, makes, uses, sells, and/or offers for sale in the United States products comprising a MIMO wireless sensor and transceiver system.

31. Intel designs, makes, sells, offers to sell, imports, and/or uses the following products: Intel Wi-Fi 6 Series Products (AX200, AX201, AX210, AX1675, AX1650 i/s, AX1650 x/w) (the "Intel '854 Product(s)").

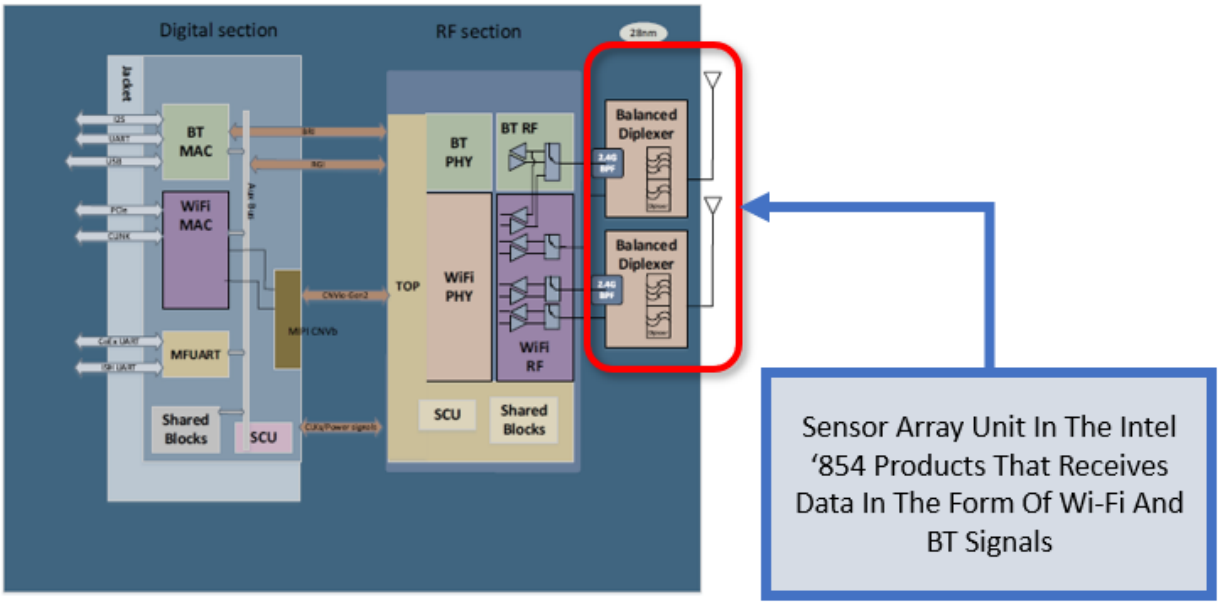
32. One or more Intel subsidiaries and/or affiliates use the Intel '854 Products in regular business operations.

33. One or more of the Intel '854 Products include technology for a wireless multiple-input multiple-output sensor node and transceiver system.



Intel Wi-Fi 6E AX210 (Gig+) Module, INTEL PRODUCT BRIEF AT 2 (May 27, 2021) (emphasis added).

34. One or more of the Intel '854 Products include a sensor array unit coupled to an analog-to-digital converter unit. Specifically, the Intel '854 Products include a sensor array unit that receives data in the form of Wi-Fi and BT signals



Intel Wi-Fi 6 AX200 (Cyclone Peak 2) External Product Specification (EPS), INTEL DOCUMENTATION at 12 (March 2019) (annotation added).

35. The Intel '854 Products enable dynamic frequency selection ("DFS") for detecting radar pulses when operating in the 5 GHz band. Specifically, the below FCC report shows that the Intel '854 Products enable and have been verified as performing dynamic frequency selection.

B.2 Test results for Dynamic Frequency Selection (DFS)

Test procedure

The conducted setup shown on *Section A.1* was used to measure the Channel Closing Transmission Time and Channel Move Time.

The *Client Device* (UUT) is set up to associate with the *Master Device*. The channel loading test file is streamed from the *Master Device* to the *Client Device*. Radar test waveforms generated with the vector signal generator are injected into the *Master* on the operating channel above the DFS detection threshold. Observations are done on the transmissions of the UUT at the end of the radar burst on the Operating Channel for a duration greater than 10 seconds. We measured the transmissions from the UUT during the observation time, after radar detection occurs the Channel Move Time and Channel Closing Transmission Time are recorded.

Results tables

Tested Channel: 56, Frequency: 5280 MHz

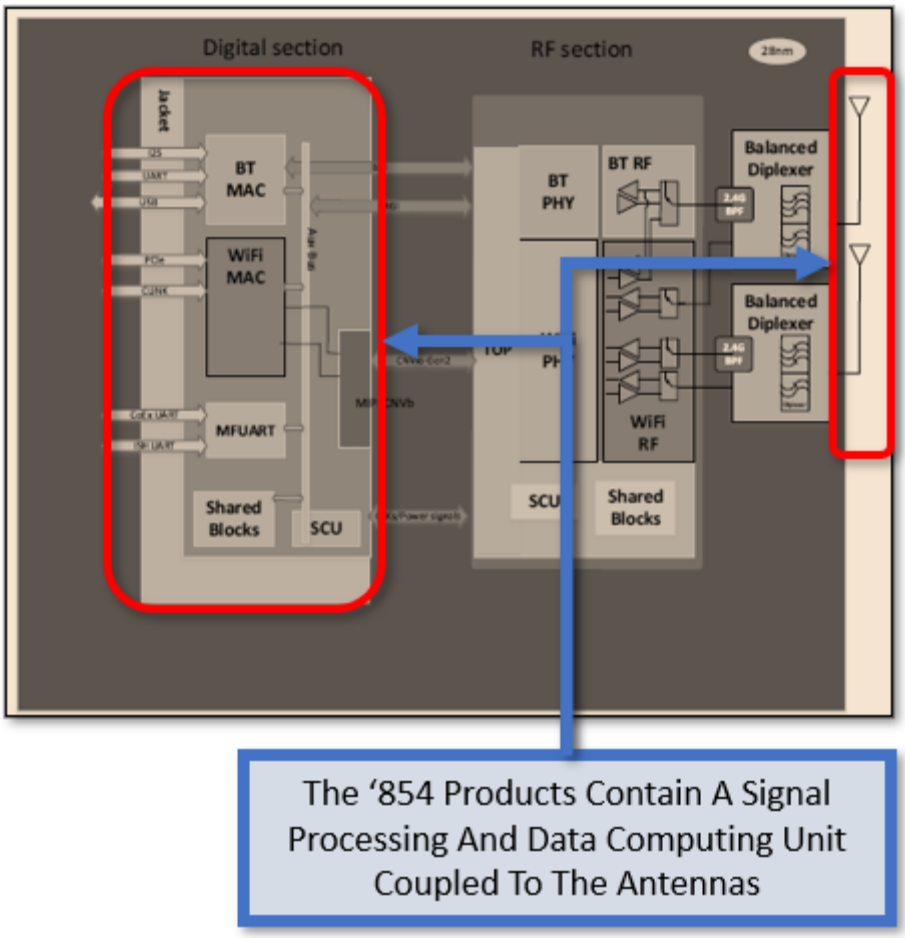
Test item	Results	Limit
Channel Closing Transmission Time	< 0.3 ms	200 ms + an aggregate of 60ms over remaining 10 seconds period.
Channel Move Time	0.3 ms	10 seconds
Non-Occupancy Period	> 30 minutes	30 minutes

Intel Wi-Fi 6 AX201 Federal Communications Test Report, REPORT NO. 180717-04.TR06 at 7 (October 16, 2018).

36. One or more of the Intel '854 Products comprise technology for an analog-to-digital converter unit coupled to a signal processing and data computing unit. For example, the Intel '854 Products contain integrated circuits that perform signal processing and data computing. These integrated circuits are connected to the transmission systems of the Intel '854 Products that comprise technology to convert signals from analog to digital signals.

37. The Intel '854 Products contain an analog-to-digital (ADC) converter unit coupled to a signal processing and data computing unit. Specifically, the Intel '854 Products contain processing unit(s) to perform signal processing and data computing.

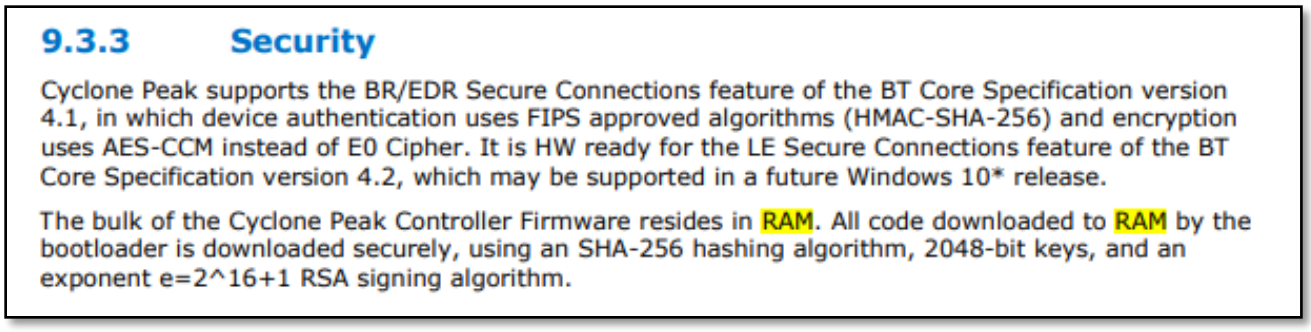
38. One or more of the Intel '854 Products include a signal processing and data computing unit that is coupled to a multiple-input multiple-output space-time transceiver that is connected to two or more antennas. The below diagram shows one example of the infringing functionality wherein Wi-Fi antennas are coupled to the signal processing and data computing unit.



Intel Wi-Fi 6 AX200 (Cyclone Peak 2) External Product Specification (EPS), INTEL DOCUMENTATION at 12 (March 2019) (annotation added).

39. One or more of the Intel '854 Products include a signal processing and data computing unit that is coupled to a multiple-input multiple-output space-time transceiver that is connected to two or more antennas.

40. One or more of the Intel '854 Products include memory that is coupled to the analog-to-digital converter unit, the signal processing and data computing unit, and the multiple-input multiple-output space-time transceiver.



9.3.3 Security

Cyclone Peak supports the BR/EDR Secure Connections feature of the BT Core Specification version 4.1, in which device authentication uses FIPS approved algorithms (HMAC-SHA-256) and encryption uses AES-CCM instead of E0 Cipher. It is HW ready for the LE Secure Connections feature of the BT Core Specification version 4.2, which may be supported in a future Windows 10* release.

The bulk of the Cyclone Peak Controller Firmware resides in RAM. All code downloaded to RAM by the bootloader is downloaded securely, using an SHA-256 hashing algorithm, 2048-bit keys, and an exponent e=2^16+1 RSA signing algorithm.

Intel Wi-Fi 6 AX200 (Cyclone Peak 2) External Product Specification (EPS), INTEL DOCUMENTATION at 12 (March 2019) (emphasis added).

41. One or more of the Intel '854 Products include a power generator coupled to a power unit.

42. One or more of the Intel '854 Products include a power unit that is connected to the sensor array unit, the analog-to-digital converter unit, the signal processing and data computing unit, and the multiple-input multiple-output space-time transceiver.

43. Intel has directly infringed and continues to directly infringe the '854 patent by, among other things, making, using, offering for sale, and/or selling technology for MIMO wireless sensor networks, including but not limited to the Intel '854 Products.

44. The Intel '854 Products are available to businesses and individuals throughout the United States.

45. The Intel '854 Products are provided to businesses and individuals located in the Western District of Texas.

46. By making, using, testing, offering for sale, and/or selling products and services that comprise a MIMO wireless sensor, including but not limited to the Intel '854 Products, Intel has injured Plaintiff and is liable to Plaintiff for directly infringing one or more claims of the '854 patent, including at least claim 15 pursuant to 35 U.S.C. § 271(a).

47. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '854 patent.

48. As a result of Intel's infringement of the '854 patent, Plaintiff has suffered monetary damages, and seeks recovery in an amount adequate to compensate for Intel's infringement, but in no event less than a reasonable royalty for the use made of the invention by Intel together with interest and costs as fixed by the Court.

COUNT II
INFRINGEMENT OF U.S. PATENT NO. 7,200,166

49. Plaintiff references and incorporates by reference the preceding paragraphs of this Complaint as if fully set forth herein.

50. Intel designs, makes, uses, sells, and/or offers for sale in the United States products comprising a dual-mode system containing a transmission filter.

51. Intel designs, makes, sells, offers to sell, imports, and/or uses the following products: Intel FPGA IP Cores, Intel FPGA IP Base Suite, Intel Quartus Prime Pro Edition, and Intel Quartus Prime Standard Edition that include the FIR II Intel FPGA IP Core (the "Intel '166 Product(s)").

52. One or more Intel subsidiaries and/or affiliates use the Intel '166 Products in regular business operations.

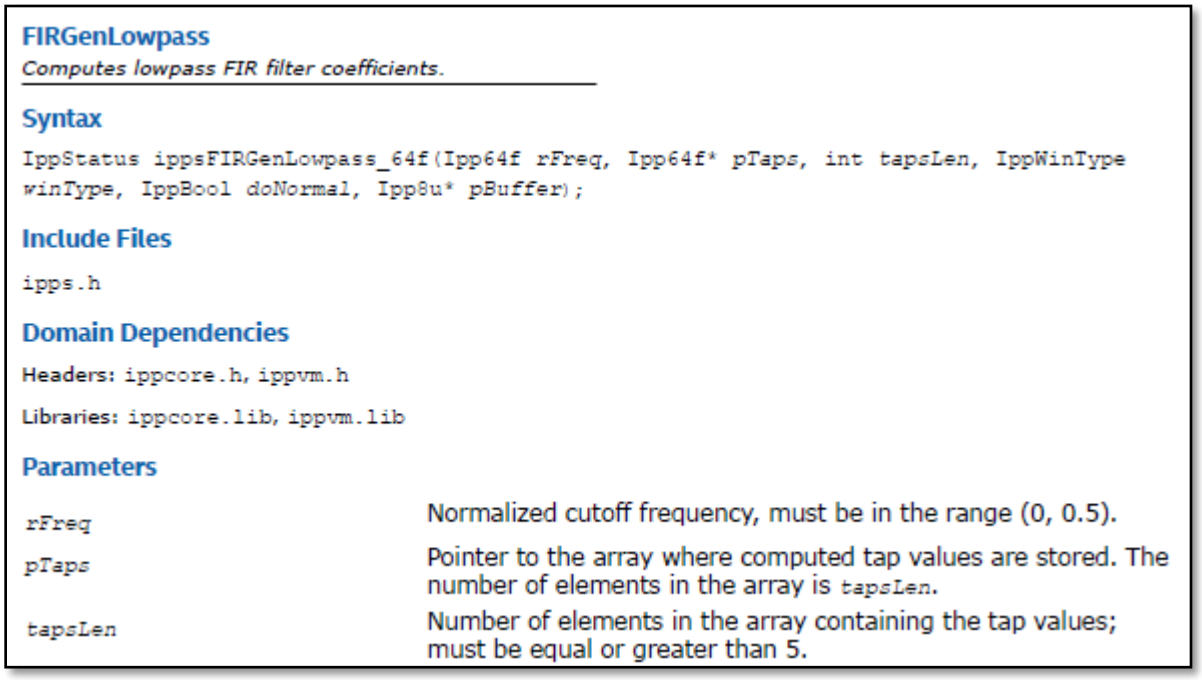
53. One or more of the Intel '166 Products comprise a dual-mode implementation system of a digital lowpass-shaping FIR transmission filter. Specifically, the Intel '166 Products comprise a FIR filter engine that enables a digital lowpass-shaping FIR transmission filter.

> The Altera® FIR II IP core provides a fully-integrated finite impulse response **(FIR) filter** function optimized for use with Altera FPGA devices. The II IP core has an interactive parameter editor that allows you to easily create custom **FIR filters**. The parameter editor outputs IP functional simulation model files for use with Verilog HDL and VHDL simulators. You can use the parameter editor to implement a variety of filter types, including single rate, decimation, interpolation,

> and fractional rate filters. Many digital systems use signal filtering to remove unwanted noise, to provide spectral shaping, or to perform signal detection or analysis. FIR filters and infinite impulse response (IIR) filters provide these functions. Typical filter applications include signal preconditioning, band selection, and **low-pass filtering**.

Intel FIR II IP CORE USER GUIDE AT PAGE 4 (May 2016) (emphasis added).

54. One or more of the Intel '166 Products contain a digital lowpass shaping FIR filter that enables the removal of the high frequency to get the low frequency from a mixed signal. The following excerpt from Intel documentation shows an example of an implementation of the digital lowpass FIR filter.



FIRGenLowpass

Computes lowpass FIR filter coefficients.

Syntax

```
IppStatus ippsFIRGenLowpass_64f(Ipp64f rFreq, Ipp64f* pTaps, int tapsLen, IppWinType
winType, IppBool doNormal, Ipp8u* pBuffer);
```

Include Files

ipps.h

Domain Dependencies

Headers: ippcore.h, ippvm.h

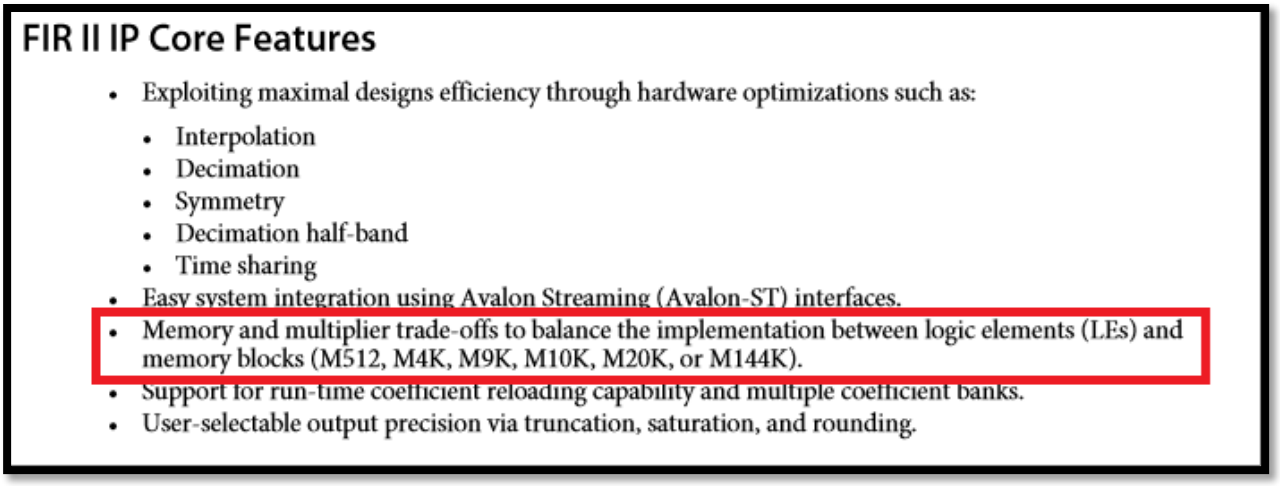
Libraries: ippcore.lib, ippvm.lib

Parameters

rFreq	Normalized cutoff frequency, must be in the range (0, 0.5).
pTaps	Pointer to the array where computed tap values are stored. The number of elements in the array is *tapsLen*.
tapsLen	Number of elements in the array containing the tap values; must be equal or greater than 5.

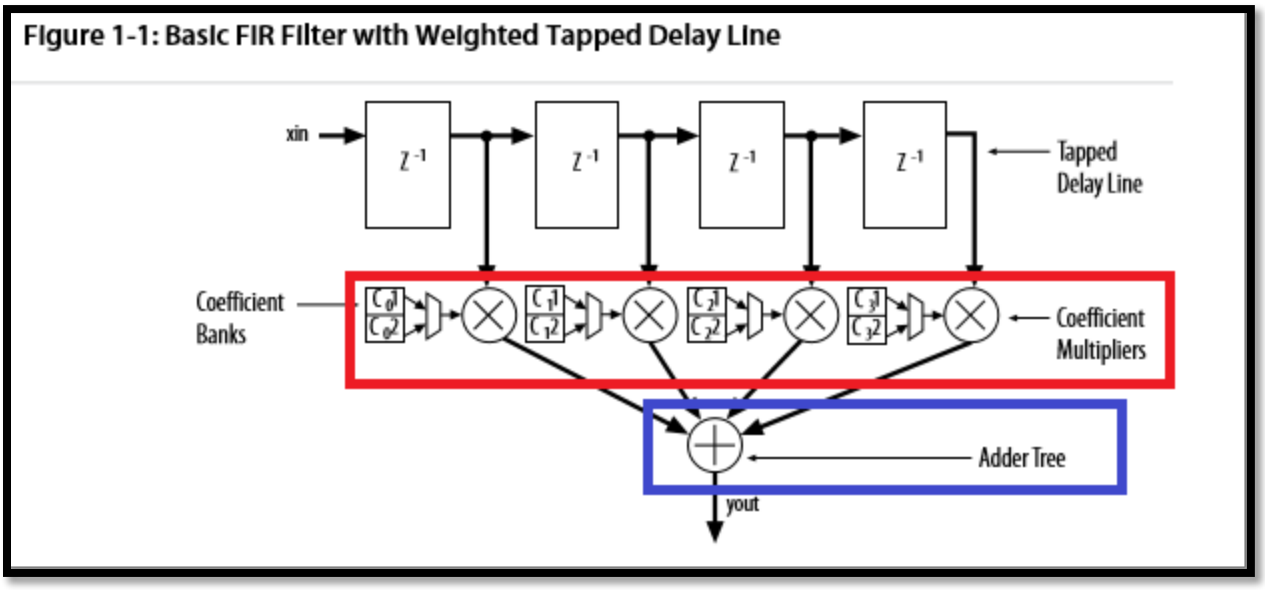
INTEL INTEGRATED PERFORMANCE PRIMITIVES – VOLUME 1: SINGAL PROCESSING at 219.

55. One or more of the Intel '166 Products include a set of memory banks. Specifically, the memory banks in the Intel '166 Products can be used to store the FIR filter coefficients. Specifically, Intel '166 Product documentation states that the product comprises memory blocks identified as "M512, M4K, M9K, M10K, M20K and M144K."



FIR II IP CORE USER GUIDE AT PAGE 5 (May 2016) (the red box identifying the memory banks in the Intel '166 Products).

56. One or more of the Intel '166 Products include a set of multiply and accumulate (MAC) units. Specifically, the Intel '166 Products contain multiply and accumulate units that enable the multiplying of a coefficient by a corresponding delayed data sample and accumulating the result. The Intel '166 Products comprise functionality whereby the systems compute the product of two numbers and adds that product to an accumulator. The figure below shows the multiply portion in a red box and the accumulate (addition or adder) portion in a blue box.



INTEL FIR II IP CORE USER GUIDE AT PAGE 4 (May 2016) (the red box identifies the coefficient multipliers that are added to the "adder tree" which is identified in the blue box).

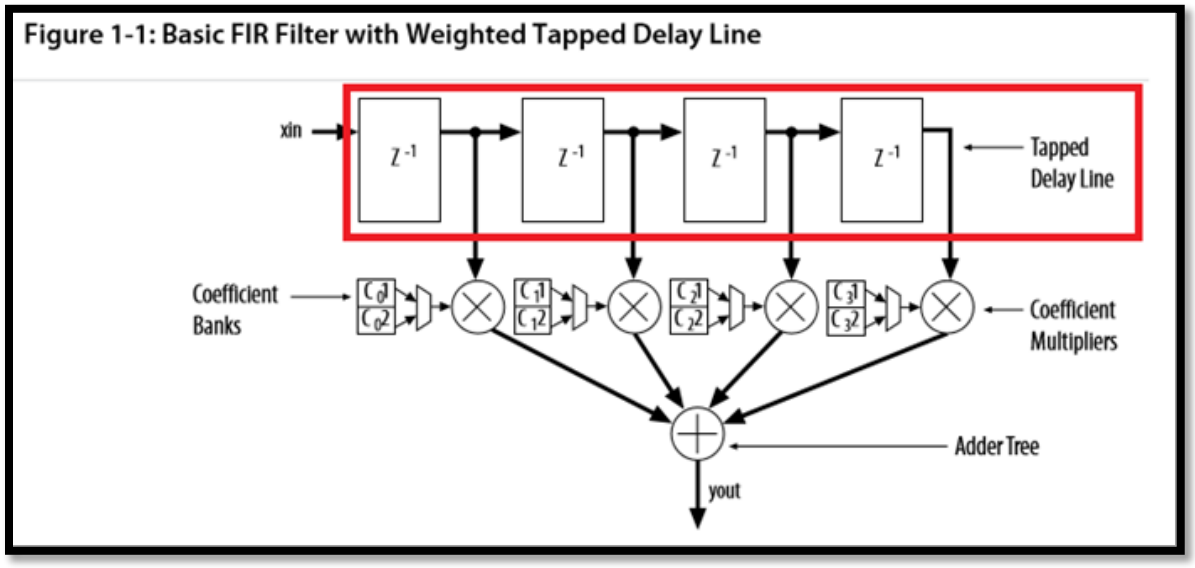
57. One or more of the Intel '166 Products include a set of counter units. Specifically, the Intel '166 Products comprise a lowpass-shaping FIR transmission filter in which the counter units are identified in Intel's documentation as "ChanCycleCount" and contain functionality for counting the number of channels carried per wire. Further, the ChanCycleCount is calculated by "dividing the number of channels by the number of channels per wire." The channel signal counts from zero to ChanCycleCount minus one.

- ChanCycleCount is the number of channels carried per wire. It is calculated by dividing the number of channels by the number of channels per wire. The channel signal counts from 0 to ChanCycleCount–1. More specifically:
  - ChansPerPhyIn = Number of channels per input wire
  - ChansPerPhyOut = Number of channels per output wire

FIR II IP CORE USER GUIDE AT PAGE 39 (May 2016) **(**the red underline identifies the mechanism by which the counter unit operates**).**

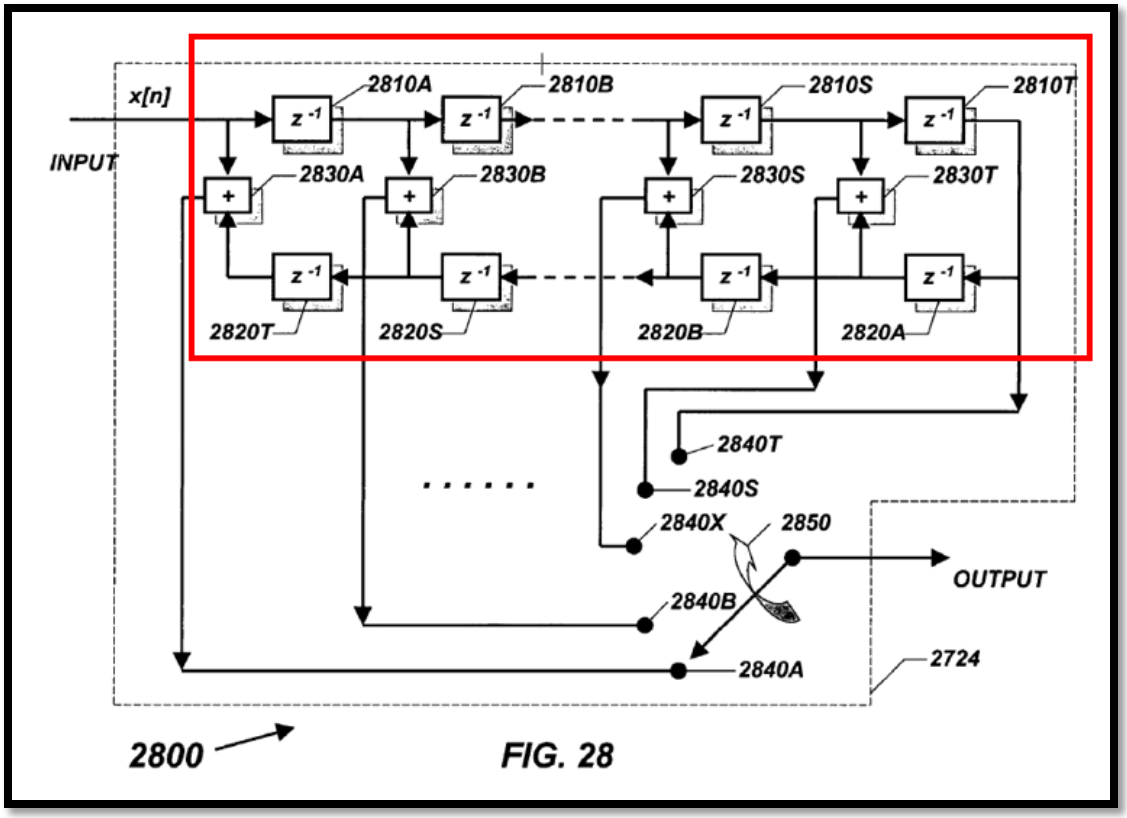
58. One or more of the Intel '166 Products comprise a pre-addition unit which includes a "Weighted Tapped Delay Line." The Weighted Tapped Delay Line (aka pre-addition unit) extracts a signal output from within the delay line and scales the extracted signal output with the

other taps to form an output signal. The below excerpt from Intel's documentation shows that the Tapped Delay Line in the Intel '166 Products take the signal output and perform a symmetric addition operation. The output signal of the pre-addition unit is stored into the data memory bank.



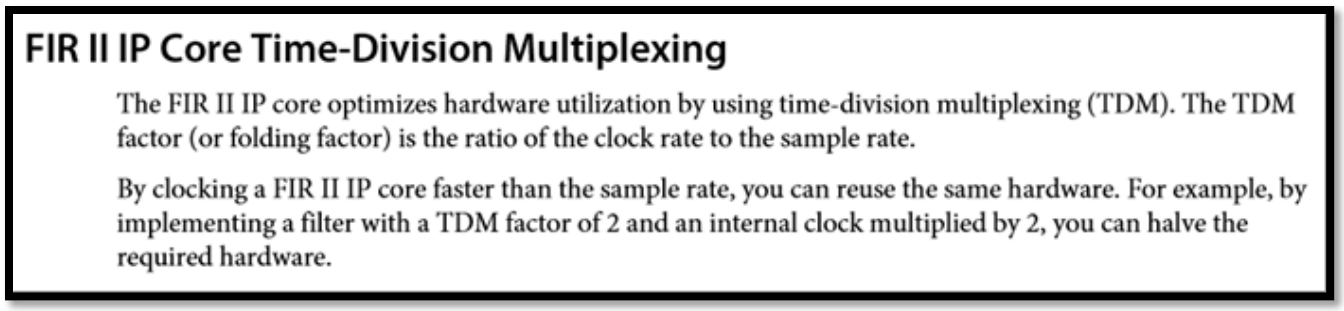
FIR II IP CORE USER GUIDE AT PAGE 4 (May 2016) (the red box identifying the pre-addition unit in the Intel '166 Products).

59. The specification of the '166 patent provides further support substantiating the "Tapped Delay Line" in the Intel '166 Products comprise a pre-addition unit. The '166 patent specification describes as one embodiment of the pre-addition element as "[t]he input samples are passed through a pre-addition to perform a symmetric addition operation. The output samples of the pre-addition are stored into the data memory bank." '166 patent, Col. 11:15-17. The below figure from the '166 patent specification shows one exemplar embodiment of the pre-addition unit with the red box identifying that "[t]he units 2810A-2810T and units 2820A-2820T are called one sample delay unit. . . . The units 2830A-2830T are referred to as the addition operation unit. . . . The input samples x[n] are passed through the delay and addition operation units to produce the output samples." '166 patent, Col. 14:37-45. The Intel '166 Products' "Tapped Delay Line" performs an identical function.



'166 PATENT, FIG. 28 (the red box annotation identifies the pre-addition unit in a figure of the '166 patent specification).

60. One or more of the Intel '166 Products include a multiplexer (MUX) unit. Specifically, the Intel '166 Products use time-division multiplexing (TDM). The TDM implemented in the Intel '166 Products is a form of multiplexing where signals are transmitted and received over a common signal path by synchronized switches to that each signal appears on the line only a fraction of a time in an alternating pattern. The below excerpt from Intel's documentation identifies that the Intel '166 Products "optimize[] hardware utilization by using time-division multiplexing."



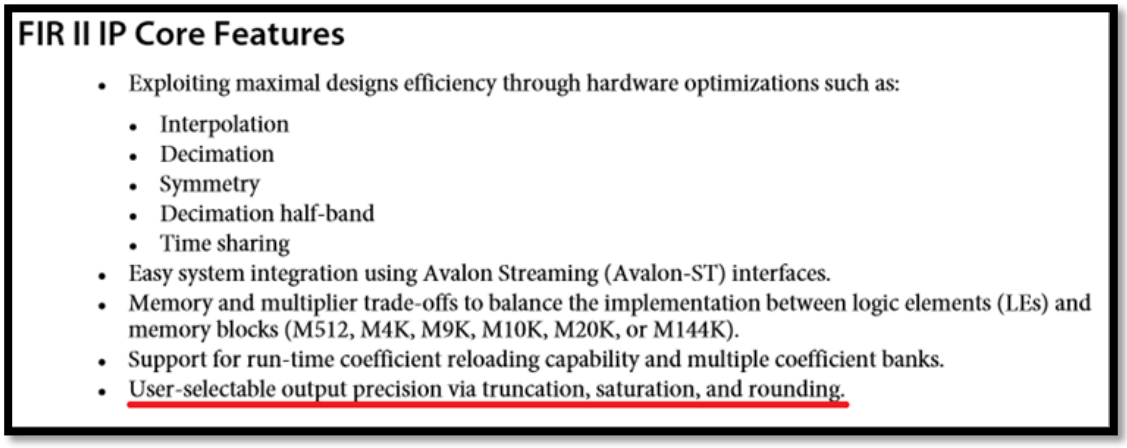
FIR II IP Core Time-Division Multiplexing

The FIR II IP core optimizes hardware utilization by using time-division multiplexing (TDM). The TDM factor (or folding factor) is the ratio of the clock rate to the sample rate.

By clocking a FIR II IP core faster than the sample rate, you can reuse the same hardware. For example, by implementing a filter with a TDM factor of 2 and an internal clock multiplied by 2, you can halve the required hardware.

FIR II IP Core User Guide at Page 36 (May 2016).

61. One or more of the Intel '166 Products comprise a selectable unit. The selectable unit in the Intel '166 Products enables a user to select different outputs via "truncation, saturation, and rounding."



FIR II IP Core Features

- Exploiting maximal designs efficiency through hardware optimizations such as:
  - Interpolation
  - Decimation
  - Symmetry
  - Decimation half-band
  - Time sharing
- Easy system integration using Avalon Streaming (Avalon-ST) interfaces.
- Memory and multiplier trade-offs to balance the implementation between logic elements (LEs) and memory blocks (M512, M4K, M9K, M10K, M20K, or M144K).
- Support for run-time coefficient reloading capability and multiple coefficient banks.
- User-selectable output precision via truncation, saturation, and rounding.

FIR II IP CORE USER GUIDE AT PAGE 5 (May 2016) (the red annotation identifies the selectable unit allows a user to select the output based via truncation, saturation, and rounding).

62. Intel has directly infringed and continues to directly infringe the '166 patent by, among other things, making, using, offering for sale, and/or selling technology comprising a dual-mode system containing a transmission filter, including but not limited to the Intel '166 Products.

63. The Intel '166 Products are available to businesses and individuals throughout the United States.

64. The Intel '166 Products are provided to businesses and individuals located in the Western District of Texas.

65. By making, using, testing, offering for sale, and/or selling products and services comprising a dual-mode system containing a transmission filter, including but not limited to the Intel '166 Products, Intel has injured Plaintiff and is liable to Plaintiff for directly infringing one or more claims of the '166 patent, including at least claim 11 pursuant to 35 U.S.C. § 271(a).

66. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the '166 patent.

67. As a result of Intel's infringement of the '166 patent, Plaintiff has suffered monetary damages, and seek recovery in an amount adequate to compensate for Intel's infringement, but in no event less than a reasonable royalty for the use made of the invention by Intel together with interest and costs as fixed by the Court.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff MIMO Research, LLC respectfully requests that this Court enter:

A. A judgment in favor of Plaintiff that Intel has infringed, either literally and/or under the doctrine of equivalents, the '854 and '166 patents;

B. An award of damages resulting from Intel's acts of infringement in accordance with 35 U.S.C. § 284;

C. A judgment and order finding that Intel's infringement was willful, wanton, malicious, bad-faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate within the meaning of 35 U.S.C. § 284 and awarding to Plaintiff enhanced damages.

D. A judgment and order finding that this is an exceptional case within the meaning of 35 U.S.C. § 285 and awarding to Plaintiff reasonable attorneys' fees against Intel.

E. Any and all other relief to which Plaintiff may show themselves to be entitled.

JURY TRIAL DEMANDED

Pursuant to Rule 38 of the Federal Rules of Civil Procedure, Plaintiff MIMO Research, LLC requests a trial by jury of any issues so triable by right.

Dated: May 27, 2022

Respectfully submitted,

/s/ Daniel P. Hipskind

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