IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

BiTMICRO LLC, Plaintiff, v. KIOXIA AMERICA, INC. and KIOXIA CORPORATION, Defendants.	Case No. 6:22-cv-00331-ADA **JURY TRIAL DEMANDED**

AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff BiTMICRO LLC ("Plaintiff" or "BiTMICRO"), through its attorneys, for its Amended Complaint against KIOXIA America, Inc. and KIOXIA Corporation (collectively, "Defendants" or "KIOXIA"), demands a trial by jury and alleges as follows:

FACTUAL INTRODUCTION

1. The novel inventions disclosed in the Asserted Patents in this matter were invented by BiTMICRO Networks, Inc. ("BNI"). BNI was founded in 1995 and was a leader in enterprise storage for mission-critical computing, particularly for military applications. BNI's storage devices are best known for exceeding the extreme performance and data integrity required for enterprise, industrial, and military environments.

2. BNI made critical advances in the solid state drive ("SSD") and integrated circuit technology that is embodied in the Asserted Patents. The Asserted Patents in this case are the result of the work from 10 different BNI engineers and developers, spanning a period of over a decade.

3. Innovation was one of the keys to the success at BNI. The company was involved with research and development projects in the SSD industry for about 20 years, over which time it accumulated over 50 U.S. patents, all of which are now owned by BiTMICRO.

THE PARTIES

4. BiTMICRO is the current owner and assignee of the Asserted Patents and holds all rights necessary to bring this action.

5. BiTMICRO is a Delaware limited liability company with its principal place of business located at 11921 Freedom Drive, Suite 550, Reston, Virginia 20190.

6. Defendant KIOXIA America, Inc. is a corporation organized and existing under the laws of California that maintains an established place of business at 801 E. Old Settlers Blvd., Suite 110, Round Rock, Texas 78664. Prior to around October 2019, KIOXIA America, Inc. operated under the name Toshiba Memory America, Inc.

7. KIOXIA America, Inc. is registered to do business in the State of Texas and has been since at least October 2017. KIOXIA America, Inc. may be served by serving its registered agent, C T Corporation System, 1999 Bryan St., Ste. 900, Dallas, TX 75201-3136.

8. Defendant KIOXIA Corporation is a corporation organized and existing under the laws of Japan that maintains an established place of business at 3-1-21, Shibaura, Minato-ku, Tokyo 108-0023, Japan. Prior to around October 2019, KIOXIA Corporation operated under the name Toshiba Memory Corporation.

9. KIOXIA Corporation may be served pursuant to Rule 4(h) of the Federal Rules of Civil Procedure, including but not limited to the means authorized by the Hague Convention on the Service Abroad of Judicial and Extrajudicial Documents in Civil or Commercial Matters.

10. KIOXIA America, Inc. is a wholly-owned subsidiary of KIOXIA Corporation.

JURISDICTION AND VENUE

11. This action arises under the patent laws of the United States, Title 35 of the United States Code. Subject matter jurisdiction is proper in this Court pursuant to 28 U.S.C. §§ 1331 and 1338(a).

12. This Court has personal jurisdiction over KIOXIA in accordance with due process and/or the Texas Long Arm Statute because, in part, KIOXIA "recruits Texas residents, directly or through an intermediary located in this state, for employment inside or outside this state." *See* Tex. Civ. Prac. & Rem. Code § 17.042.

13. This Court also has personal jurisdiction over KIOXIA because it has committed and continues to commit acts of direct and/or indirect infringement in this judicial district in violation of at least 35 U.S.C. §§ 271(a) and (b). In particular, on information and belief, KIOXIA has made, used, offered to sell, and/or sold the accused products in this judicial district, and has induced others to use the accused products in this judicial district.

14. This Court also has personal jurisdiction over KIOXIA because, *inter alia*, KIOXIA (1) has substantial, continuous, and systematic contacts with this State and this judicial district; (2) owns, manages, and operate facilities in this State and this judicial district; (3) enjoys substantial income from its operations and sales in this State and this judicial district; (4) employs Texas residents in this State and this judicial district; and (5) solicits business and markets products, systems and/or services in this State and judicial district including, without limitation, those related to the infringing accused products.

15. Venue is proper in this District pursuant to at least 28 U.S.C. §1319(b)-(c) and §1400(b), at least because KIOXIA, either directly or through its agents, has committed acts within

this judicial district giving rise to this action, and continues to conduct business in this district, and/or has committed acts of patent infringement within this District giving rise to this action.

FACTUAL ALLEGATIONS

BiTMICRO Patents

16. The BiTMICRO inventions contained in the Asserted Patents in this case relate to groundbreaking improvements to memory controllers, mapping tables for memory devices, and memory saving during power loss as will be further described below.

U.S. Patent No. 9,135,190

17. On September 15, 2015, the U.S. Patent and Trademark Office duly and lawfully issued United States Patent No. 9,135,190 ("the '190 Patent"), entitled "Multi-profile memory controller for computing devices." A true and correct copy of the '190 Patent is attached hereto as **Exhibit A.**

18. BiTMICRO is the owner and assignee of all right, title, and interest in and to the '190 Patent, including the right to assert all causes of action arising under said patent and the right to any remedies for infringement of it.

19. The '190 Patent describes, among other things, a multi-profile memory controller for computing devices. Specifically, the '190 Patent describes a memory controller that can operate with memory locations, memory devices, or both which are associated with different memory attributes, different attribute qualifiers, or the like. For example, a non-volatile memory storage device may be portioned to allow a memory controller to treat a portion of the memory device as a temporary cache memory to store data prior to writing the data to a permanent storage location. This eliminates the need for a separate memory cache, often composed of volatile memory. This

has the additional advantage of maintaining the temporary data in the non-volatile cache partition in the event of an unexpected power loss.

20. Prior to the invention of the '190 Patent, memory controllers were designed to operate with memory locations and memory devices that all shared the same set of memory device characteristics, such as block size. Due to this limitation, there was no way of varying how a memory controller performed read and write operations on different memory locations or memory devices. The '190 Patent overcame this limitation by disclosing a novel multi-profile memory controller with the ability to operate differently with memory locations and memory devices based on differences between the attributes of particular memory locations and memory devices. (*See* Ex. A, at 1:20-60).

21. As described in the '190 Patent, a memory store includes multiple addressable memory locations, and each location is associated with a set of memory attributes, which can include, for example, the type of memory device in which the memory location is located, the data size used by the memory device, or the memory protocol of the device. (*See* Ex. A, at 2:63-3:13). These attributes are organized into device profiles that can be used by a memory controller connected to the memory store to determine how memory transactions are to be performed with each memory location. (*See* Ex. A, at 3:14-4:25). By analyzing the requirements of the requested memory transaction and comparing those requirements to the device profiles, the memory controller selects the appropriate memory location for the memory transaction. The criteria used by the controller to select the optimal memory location for the memory transaction based on the stored attributes within the device profiles can be programmed in any number of ways. (*See* Ex. A, at 7:60-9:48).

22. The novel features of the invention are recited in the claims. For example, claim 59 of the '190 Patent recites:

> A memory controller comprising:
>
> an interface controller coupled to a memory device interface and an input/output (IO) device interface;
>
> a memory store;
>
> wherein the memory device interface is directly coupled to the memory store;
>
> said interface controller disposed to perform a memory transaction by addressing a first memory location in the memory store,
>
> said first memory location and a second memory location respectively associated with a first device profile and a second device profile;
>
> wherein said first device profile is optimal for a data type subject to the memory transaction, wherein said data type comprises one of a random data type or a sequential data type;
>
> said interface controller identifies command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device;
>
> said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles;
>
> said interface controller obtaining the first set of attributes after identifying the command details; and said addressing of said first memory location includes using said attributes from said first device profile;
>
> and said addressing of said first memory location includes selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.

(Ex. A at 18:34-65). Claim 59 of the '190 Patent describes claim elements individually or as an ordered combination, that were non-routine and unconventional at the time of the invention in 2009 and an improvement over prior art, as it provided a memory controller (not previously available)

with an interface controller capable of performing memory transactions with different transfer sizes on different memory locations based on attributes associated with the different memory locations as defined in differing device profiles for those memory locations. (*See* Ex. A at Abstract, 1:20-60, 2:41-62).

U.S. Patent No. 8,010,740

23. On August 30, 2011, the U.S. Patent and Trademark Office duly and lawfully issued United States Patent No. 8,010,740 ("the '740 Patent"), entitled "Optimizing memory operations in an electronic storage device." A true and correct copy of the '740 Patent is attached hereto as Exhibit B.

24. BiTMICRO is the owner and assignee of all right, title, and interest in and to the '740 Patent, including the right to assert all causes of action arising under said patent and the right to any remedies for infringement of it.

25. The '740 Patent describes, among other things, a mapping table for optimizing memory operations in an electronic storage device. Prior to the inventions in the '740 Patent, memory operations in solid state storage devices were subject to a number of inefficiencies. As described in the '740 specification, SSDs such as those that include NAND flash memory "suffer from write cycle limitations and to a certain degree, bad blocks. In addition, flash drives use block addressing rather than byte addressing, and these flash drives use block addresses that are usually much larger than the block address used by the host. Block addressing may impose an additional level of complexity and additional processing cycles when performing a write operation, and which in turn, may increase write operation latency. This additional level of complexity may include performing a read-modify-write transaction to complete the write operation." (Ex. B at 1:42-53).

26. To address these issues and increase the speed and efficiency of memory operations in their products, SSD manufacturers tried solutions such as adding complex algorithms to handle the management of memory operations and adding more powerful processing devices to run these complex algorithms. (*See id.* at 1:54-2:10). These solutions, however, increased both the cost and design complexity of the SSDs. (*See id.*).

27. The '740 Patent overcame this problem by providing a solution that optimizes memory operations in a solid state storage device while minimizing the amount of additional cost and complexity to the design of the device. (*See id.* at 2:11-14). The '740 Patent achieves this through an improved mapping table that "increas[es] the likelihood that, in response to an I/O transaction initiated by a host, the operational load imposed on the storage device by these memory operations will be optimally distributed across different storage device resources, such as by interleaving or parallel memory operations, reducing memory operation latency, increasing operational device efficiency, or both." (*Id.* at 2:14-21; *see also id.* at 3:12-31). For example, the '740 Patent describes a mapping table that includes a set of logical fields that represent a plurality of logical block address (LBA) sets. The mapping table also includes a set of physical block address (PBA) fields that represent a set of PBAs and access parameters for the PBAs, as well as information that associates the LBA sets with the PBA sets in a highly efficient manner. The mapping table enables the storage device to perform optimized memory operations on memory locations based on the information in the table regarding the relationship between the LBA and PBA sets and the access parameters. (*See id.* at 2:27-49).

28. The novel features of the '740 inventions are recited in the claims. For example, claim 1 of the '740 Patent recites:

> A mapping table for optimizing memory operations performed by an electronic storage device in response to receiving an I/O transaction request initiated by a host, said mapping table comprising:
>
> a set of logical fields, including a first logical field and a second logical field, and said logical fields respectively disposed for representing a plurality of LBA sets, including said first logical field disposed for representing a first LBA set and said second logical field disposed for representing a second LBA set, said first and second LBA sets each representing a set of consecutive LBAs;
>
> a set of PBA fields, including a first PBA field and a second PBA field, said set of PBA fields respectively disposed for representing a set of PBAs, including a first PBA disposed for representing a first set of access parameters and a second PBA disposed for representing a second set of access parameters, said PBAs each associated with a physical memory location in a memory store, said set of logical fields and said set of PBA fields disposed to associate said first and second LBA sets with said first and second PBAs;
>
> and wherein, in response to receiving the I/O transaction request, said mapping table causes the electronic storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first and second LBA sets.

(Ex. B at 9:64-10:24). Claim 1 of the '740 Patent describes claim elements individually or as an ordered combination, that were non-routine and unconventional at the time of the inventions in 2006 and an improvement over prior art, as it provided a mapping table (not previously available) that enables optimized memory operations in an electronic storage device through information stored in a mapping table regarding logical fields, PBA fields, access parameters, and relationships between LBA and PBA sets. (*See id.* at Abstract, 2:27-49).

U.S. Patent No. 6,496,939

29. On December 17, 2002, the U.S. Patent and Trademark Office duly and lawfully issued United States Patent No. 6,496,939 ("the '939 Patent"), entitled "Method and system for controlling data in a computer system in the event of a power failure." A true and correct copy of the '939 Patent is attached hereto as **Exhibit C**.

30. BiTMICRO is the owner and assignee of all right, title, and interest in and to the '939 Patent, including the right to assert all causes of action arising under said patent and the right to any remedies for infringement of it.

31. The '939 Patent describes, among other things, systems and methods for controlling data in a computer or memory system when the system loses external power. (*See* Ex. C at Abstract). Specifically, the '939 Patent describes a plurality of capacitors configured to supply power to the computer or memory system, activating those capacitors to supply power in the event of a sudden loss of external power, and reconfiguring the data in the computer or memory system while that auxiliary power is supplied. (*Id.*). Through the use of the systems and methods described by the '939 Patent, newly written and/or modified data can be stored (or flushed) from the volatile memory to the non-volatile memory in the event of a sudden power loss, and/or enable the data to be erased automatically or manually—in all cases, preserving the security of the stored data. (*Id.*).

32. Prior to the inventions in the '939 Patent, computing systems utilized various types of memory for storing and managing data, including volatile memory for main memory and cache, as well as mechanical disk drives for longer term storage. (*Id.* at 1:14-33). One disadvantage of volatile memory, however, is that it requires a constant source of power, or the data stored thereon will be lost. Consequently, when there is a sudden loss of power, there is insufficient time to safely write all the newly written and/or modified data from the volatile memory to the hard disk drive before the system shuts down – resulting in data loss and insecurity. (*Id.* at 1:34-45). Batteries could be coupled to the internal power system, but those have a number of disadvantages, including a limited number of charge-drain cycles, large internal resistance, size, and weight. A battery-backed uninterruptable power supply (UPS) could be coupled to the external power supply of the

computer system, but those systems suffer from the same or similar disadvantages. (*Id.* at 1:46-58). In addition, prior to the inventions of the '939 Patent, computing systems did not have a means for ensuring that the data to be securely erased when the system loses power. (*Id.* at 1:59-2:21).

33. The '939 Patent overcame these various limitations by disclosing novel systems and methods for controlling data in a computer system when the system loses power, comprised of a plurality of capacitors configured to supply power to the computer system, activating those capacitors to supply power in the event of a sudden loss of external power, and reconfiguring the data in the computer system while that auxiliary power is supplied. (*Id.* at 2:24-37). In addition, these systems and methods allow the computing system to rapidly erase data from a non-volatile memory automatically, in the event of a sudden loss of power, and/or manually. (*Id.* at 2:37-43).

34. The novel features of the inventions of the '939 Patent are recited in the claims. For example, claim 10 of the '939 Patent recites:

> 1. A system for controlling data in a computer system when the computer system loses power, the computer system comprising a computer engine, comprising:
>
> means for activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system;
>
> means for reconfiguring the data in the computing engine; and
>
> means for deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level.

(Ex. C at 7:20-31). Claim 10 of the '939 Patent describes claim elements individually or as an ordered combination, that were non-routine and unconventional at the time of the inventions in or before 1999 and an improvement over prior art, as it used a plurality of capacitors configured to supply power to the computer system when the system loses power, thereby preserving the security of the data stored in volatile memory therein. (*See* Ex. C at Abstract, 1:14-2:21, 2:24-43).

KIOXIA's Use of the Patented Technology

35. KIOXIA is a worldwide supplier of flash memory and solid state drives (SSDs). KIOXIA was formerly a business unit focused on memory products within the Japanese multinational conglomerate Toshiba Corporation, and which was spun off into a separate company in 2017. Specific examples of KIOXIA's infringing products made, sold, and/or offered for sale in the United States, and/or imported into the United States are discussed in further detail below.

36. KIOXIA makes, uses, sells, and/or offers to sell in the United States, and/or imports into the United States (or has made, used, sold, offered for sale, and/or imported into the United States) SSDs with SLC caching capabilities, which infringe one or more claims of the '190 Patent. Such SSDs include, for example, at least KIOXIA's XG5, XG6, BG3, and BG4 Series SSDs, as well as the Toshiba Q300, TR200, OCZ RC100, OCZ TL100, OCZ TR150, OCZ Trion 100, OCZ Trion 150, and OCZ VX500 Series SSDs.

37. KIOXIA makes, uses, sells, and/or offers to sell in the United States, and/or imports into the United States (or has made, used, sold, offered for sale, and/or imported into the United States) Non-Volatile Memory Express (NVMe) SSDs, which infringe one or more claims of the '740 Patent. Such products include, for example, at least KIOXIA's XG5, XG5-P, XG6, BG1, BG3, BG4, RC100, CD5, CD6-V, CD6-R, CD7-V, CD7-R, XD5, XD6, FL6, CM5-V, CM6-V, CM5-R, and CM6-R Series SSDs as well as the Toshiba OCZ RC100 and RD400 Series SSDs.

38. KIOXIA makes, uses, sells, and/or offers to sell in the United States, and/or imports into the United States (or has made, used, sold, offered for sale, and/or imported into the United States) SSDs with power loss protection, which infringe one or more claims of the '939 Patent. Such SSDs include, for example, at least the KIOXIA FL, CM, PM, CD, and XD Series products.

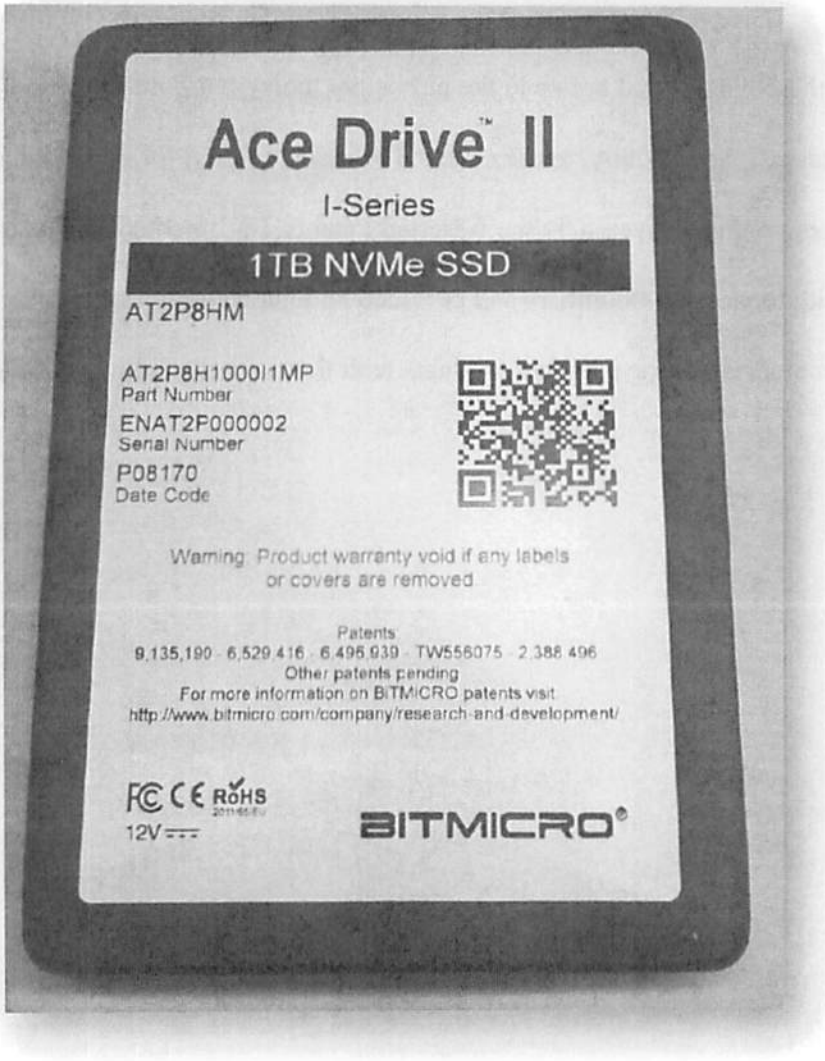
Notice and Marking

39. As set forth below, KIOXIA has been on constructive and/or actual notice of the Asserted Patents.

40. BiTMICRO has complied with 35 U.S.C. § 287 with respect to the Asserted Patents.

41. The previous owner of the Asserted Patents, BNI, also complied with 35 U.S.C. § 287, and thereby provided notice to the public, including but not limited to KIOXIA, of the Asserted Patents. Specifically, to the extent BNI made, offered for sale, sold, or imported into the United States products covered by the Asserted Patents, BNI marked substantially all of such products with those patent numbers and provided an internet address at which BNI posted information associating the patented products with their corresponding patent numbers in compliance with 35 U.S.C. § 287.

42. For example, BNI's Ace Drive II products, which BNI contended were covered by the '190 and '939 Patents, were sold by BNI with a label affixed on the products listing the '190 and '939 Patents, as well as an internet address at which BNI posted a listing of additional patents it contended were practiced by that product, as shown below:



43. BNI's other products similarly included product labels identifying specific patents by number and/or an internet address at which BNI posted a listing of the patents it contended were associated with each product, including but not limited to the '190, '740, and '939 Patents.

44. BNI's product documentation, which was provided to customers and available to the general public, also identified by number specific patents that BNI contended were practiced by the products and included an internet address at which BNI posted a listing of other patents it contended were associated with the products, pursuant to 35 U.S.C. § 287.

45. BiTMICRO has not made, offered for sale, sold, or imported into the United States any products that are covered by any of the Asserted Patents. Thus, there are no BiTMICRO products that would require marking under 35 U.S.C. § 287.

46. The Asserted Patents have been widely cited by the industry and by the USPTO during the prosecution of other patents. For example, the '190 Patent has been cited in patents and/or applications by Western Digital, SanDisk, Micron, Huawei, Microsoft, and other well-known industry participants. The '740 Patent has been cited in patents and/or patent applications by Seagate and other well-known industry participants. And the '939 Patent has been cited in patents and/or applications by Western Digital, Qualcomm, Samsung, SK hynix, HTC, IBM, Google, Avaya, and other well-known industry participants.

47. Indeed, the Asserted Patents have been used by the USPTO as a basis to reject patent applications filed by well-known industry participants under 35 U.S.C. § 102 and/or § 103. For example, the '190 Patent has served as the basis for § 102/103 rejections at least three times, including against SanDisk. The '740 Patent has served as the basis for § 102/103 rejections at least four times, including against Seagate and Samsung. And the '939 Patent has served as the basis for § 102/103 rejections at least ten times, including against Amazon, Marvell, and other well-known industry participants.

48. In addition, as set forth in greater detail below, KIOXIA has had actual notice of the '190 Patent and the rest of the Asserted Patents since at least September 5, 2018 by virtue of its participation in a proceeding before the International Trade Commission involving those patents.

FIRST COUNT

(INFRINGEMENT OF U.S. PATENT NO. 9,135,190)

49. BiTMICRO incorporates by reference the allegations set forth in paragraphs 1-48 as though fully set forth herein.

50. On information and belief, KIOXIA has directly infringed and continues to directly infringe one or more claims of the '190 Patent, including at least claim 59 of the '190 Patent, in the state of Texas, in this judicial district, and elsewhere in the United States by, among other things, making, using, selling, offering for sale, and/or importing into the United States products that embody one or more of the inventions claimed in the '190 Patent, including but not limited to the above-identified SSDs with SLC caching, and all reasonably similar products ("the '190 Accused Products"), in violation of 35 U.S.C. § 271(a).

51. As an example, the XG6 Series SSDs include "a memory controller." Specifically, the XG6 Series SSDs includes a memory controller for handling read and write operations on the NAND memory cells on the drive. "The XG6 series utilizes KIOXIA's latest 96-layer, 3D TLC (3-bit-per-cell) flash memory. With 4th generation BiCS FLASH™ and SLC cache features, XG6 SSDs reach up to sequential read/write speeds of 3180 MB/s and 2960 MB/s respectively and deliver up to 355,000 random read and 365,000 random write IOPS.")." (*See* XG6 Product Brief).[1]

[1] Available at https://business.kioxia.com/content/dam/kioxia/shared/business/ssd/doc/cSSD-XG6-product-brief.pdf

52. The XG6 Series SSDs include "an interface controller coupled to a memory device interface and an input/output (IO) device interface." For example, the XG6 Series SSDs include a TC58NCP090GSD controller chip that serves as an interface controller:

Specifications

Product	Toshiba XG6 256GB	Toshiba XG6 512GB	Toshiba XG6 1TB
Pricing	N/A	N/A	N/A
Capacity (User / Raw)	256GB / 256GB	512GB / 512GB	1024GB / 1024GB
Form Factor	M.2 2280 S2 (Single-sided)	M.2 2280 S2 (Single-sided)	M.2 2280 S2 (Single-sided)
Interface / Protocol	PCIe 3.1 x4 / NVMe 1.3a	PCIe 3.1 x4 / NVMe 1.3a	PCIe 3.1 x4 / NVMe 1.3a
Controller	TC58NCP090GSD	TC58NCP090GSD	TC58NCP090GSD
DRAM	NANYA LPDDR3	NANYA LPDDR3	NANYA LPDDR3
Memory	Toshiba BiCS FLASH 96-layer 3D TLC	Toshiba BiCS FLASH 96-layer 3D TLC	Toshiba BiCS FLASH 96-layer 3D TLC
Sequential Read	Up to 3,180 MB/s	Up to 3,180 MB/s	Up to 3,180 MB/s
Sequential Write	Up to 2,960 MB/s	Up to 2,960 MB/s	Up to 2,960 MB/s
Random Read	Up to 355,000 IOPS	Up to 355,000 IOPS	Up to 355,000 IOPS
Random Write	Up to 365,000 IOPS	Up to 365,000 IOPS	Up to 365,000 IOPS
Encryption	TCG Pyrite and OPAL 2.01 as an option (TCG Pyrite: x = 0, TCG OPAL: x = A)		
Endurance	N/A	N/A	N/A
Part Number	KXG6xZNV256G	KXG6xZNV512G	KXG6xZNV1T02
Warranty	5-Years	5-Years	5-Years

(Toshiba XG6 M.2 NVMe SSD Review: Higher Density and Improved Efficiency).[2]

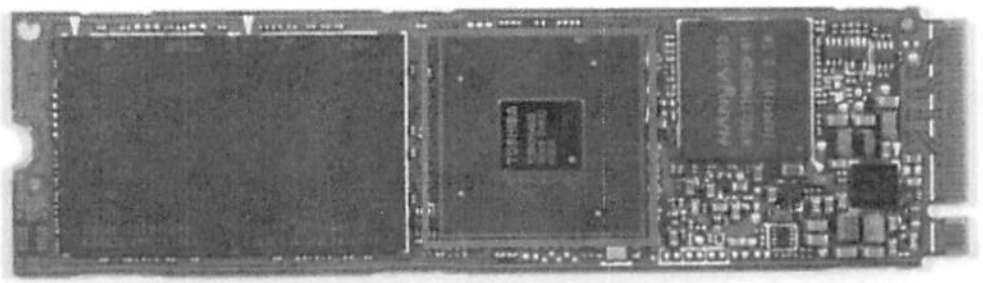
53. The TC58NCP090GSD controller chip is connected to at least one memory bus, which serves as a memory device interface. The controller chip is also connected to a PCIe interface, which serves as an input/output interface with a computing device:

[2] Available at https://www.tomshardware.com/reviews/toshiba-xg6-nvme-ssd,5782.html

Specifications

Product	Toshiba XG6 256GB	Toshiba XG6 512GB	Toshiba XG6 1TB
Pricing	N/A	N/A	N/A
Capacity (User / Raw)	256GB / 256GB	512GB / 512GB	1024GB / 1024GB
Form Factor	M.2 2280 S2 (Single-sided)	M.2 2280 S2 (Single-sided)	M.2 2280 S2 (Single-sided)
Interface / Protocol	PCIe 3.1 x4 / NVMe 1.3a	PCIe 3.1 x4 / NVMe 1.3a	PCIe 3.1 x4 / NVMe 1.3a
Controller	TC58NCP090GSD	TC58NCP090GSD	TC58NCP090GSD
DRAM	NANYA LPDDR3	NANYA LPDDR3	NANYA LPDDR3
Memory	Toshiba BiCS FLASH 96-layer 3D TLC	Toshiba BiCS FLASH 96-layer 3D TLC	Toshiba BiCS FLASH 96-layer 3D TLC
Sequential Read	Up to 3,180 MB/s	Up to 3,180 MB/s	Up to 3,180 MB/s
Sequential Write	Up to 2,960 MB/s	Up to 2,960 MB/s	Up to 2,960 MB/s
Random Read	Up to 355,000 IOPS	Up to 355,000 IOPS	Up to 355,000 IOPS
Random Write	Up to 365,000 IOPS	Up to 365,000 IOPS	Up to 365,000 IOPS
Encryption	TCG Pyrite and OPAL 2.01 as an option (TCG Pyrite: x = 0, TCG OPAL: x = A)		
Endurance	N/A	N/A	N/A
Part Number	KXG6xZNV256G	KXG6xZNV512G	KXG6xZNV1T02
Warranty	5-Years	5-Years	5-Years

(*Id.*).



(The Toshiba XG6 1TB SSD Review: Our First 96-Layer 3D NAND SSD).[3]

54. The XG6 Series SSDs include "a memory store." For example, the XG6 Series SSDs include 96-layer 3D TLC NAND memory, which constitutes a memory store. As advertised

[3] Available at https://www.anandtech.com/show/13254/the-toshiba-xg6-1tb-ssd-review-first-96l-3d-nand

by KIOXIA, "[t]he XG6 series utilizes KIOXIA's latest 96-layer, 3D TLC (3-bit-per-cell) flash memory." (XG6 Product Brief,[4] at 1).

55. In the XG6 Series SSDs, "the memory device interface is directly coupled to the memory store." For example, the memory bus connected to the controller chip is directly coupled to the TLC NAND memory store, thereby enabling the controller to handle read and write operations to the memory store.

56. In the XG6 Series SSDs, "said interface controller [is] disposed to perform a memory transaction by addressing a first memory location in the memory store." For example, in the XG6 Series SSDs, a portion of the TLC NAND memory store is reserved to act as an SLC cache. Data can be written to the SLC cache at a faster rate than to other portions of the TLC NAND memory store. As advertised by KIOXIA, "[w]ith 4th generation BiCS FLASH™ and SLC cache features, XG6 SSDs reach up to sequential read/write speeds of 3180 MB/s and 2960 MB/s respectively and deliver up to 355,000 random read and 365,000 random write IOPS." (XG6 Product Brief,[5] at 1). For write operations to the SLC cache, the controller chip performs a memory transaction by addressing a first memory location within the SLC cache.

57. In the XG6 Series SSDs, "said first memory location and a second memory location [are] respectively associated with a first device profile and a second device profile." For example, a second memory location within the TLC NAND memory store is a TLC cell that is not a part of the SLC cache. The first memory location and second memory location are associated with a first

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[4] Available at https://business.kioxia.com/content/dam/kioxia/shared/business/ssd/doc/cSSD-XG6-product-brief.pdf

[5] Available at https://business.kioxia.com/content/dam/kioxia/shared/business/ssd/doc/cSSD-XG6-product-brief.pdf

device profile and a second device profile, respectively, that define how data is to be stored in those locations.

58. In the XG6 Series SSDs, "said first device profile is optimal for a data type subject to the memory transaction, wherein said data type comprises one of a random data type or a sequential data type." For example, as advertised by KIOXIA, the SLC cache allows the XG6 SSDs to "reach up to sequential read/write speeds of 3180 MB/s and 2960 MB/s respectively and deliver up to 355,000 random read and 365,000 random write IOPS." (XG6 Product Brief,[6] at 1).

59. In the XG6 Series SSDs, "said interface controller identifies command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device." For example, for memory transactions with the first memory device such as writing data to the SLC cache, the controller chip identifies command details for causing the memory transaction to be performed in the first memory device.

60. In the XG6 Series SSDs, "said device profile represent[s] a first set of attributes of said first memory location, and said second device profile represent[s] a second set of attributes of said second memory location, and a difference exists between said first and second device profiles." For example, the first device profile (*e.g.*, the profile for the SLC cache) represents a first set of attributes (*e.g.*, data size, memory protocol, device type) associated with the first memory location (*e.g.*, a location within the SLC cache). The second device profile (*e.g.*, the profile for the non-cache portion of the TLC NAND memory store) represents a second set of attributes (*e.g.*, data size, memory protocol, device type) associated with the second memory location (*e.g.*, a location within the non-cache portion of the TLC NAND memory store). The first and second device profiles are

[6] Available at https://business.kioxia.com/content/dam/kioxia/shared/business/ssd/doc/cSSD-XG6-product-brief.pdf

different because the SLC cache has attributes associated with a write protocol of one bit per cell, whereas the non-cache portion of the TLC NAND memory store has attributes associated with a write protocol of three bits per cell.

61. In the XG6 Series SSDs, "said interface controller obtain[s] the first set of attributes after identifying the command details; and said addressing of said first memory location includes using said attributes from said first device profile." For example, after identifying command details specifying that data is to be written to the SLC cache, the controller chip obtains the first set of attributes (*e.g.*, data size, memory protocol, device type) associated with the memory location in the SLC cache.

62. In the XG6 Series SSDs, "said addressing of said first memory location includes selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes." As advertised by KIOXIA, "[o]ne important practice that can enable greater endurance of MLC or TLC based managed NAND is to partition a portion to act as SLC flash memory, or what is known as pseudo SLC (pSLC) NAND. In combination with a refresh policy, pSLC mode can improve automotive data retention even further as it stores only one bit of data (like SLC) within MLC or TLC based managed NAND, and delivers more P/E cycles of cell endurance. The consequence is a reduction of bits that are available for storage. . . . Although NAND density may be reduced by 50% in MLC and 66.6% in TLC, storing a single bit per cell in both can improve write endurance by up to ten times. To implement pSLC mode requires a sophisticated controller with firmware that is optimized for the specific NAND that is used. KIOXIA (formerly Toshiba Memory) embedded Multi-Media Card (e-MMC) and Universal Flash Storage (UFS) solutions support an enhanced data area based on pSLC mode, delivering cost benefits of using MLC or TLC based managed NAND with higher

reliability, especially in extreme temperature environments." (Kioxia White Paper, "Why Data Retention is Becoming More Critical in Automotive Applications").[7] Thus, for example, after receiving a write transaction command, the controller chip obtains the attributes of the SLC cache profile and determines whether there is sufficient capacity within the SLC cache to write the data to the cache. The controller will select a transfer size to the SLC cache based on an analysis of the size of the data to be written, the remaining memory capacity within the SLC cache, and the attributes of the SLC cache profile.

63. By making, using, offering for sale, and/or selling products in the United States and/or importing products into the United States, including but not limited to the '190 Accused Products, KIOXIA has injured BiTMICRO and is liable to BiTMICRO for directly infringing one or more claims of the '190 Patent, including without limitation claim 59 pursuant to 35 U.S.C. § 271(a).

64. On information and belief, KIOXIA has had knowledge of the '190 Patent since at least September 2018, when BiTMICRO served a subpoena on KIOXIA (then known as Toshiba Memory America, Inc. in connection with a proceeding before the International Trade Commission, *In the Matter of Certain Solid State Storage Drives, Stacked Electronics Components, and Products Containing Same*, Inv. No. 337-TA-1097 ("the ITC Action"). In the ITC Action, BiTMICRO alleged that various solid state computer drives ("SSDs") and electronic devices that incorporate stacked electronics components sold by Samsung Electronics, SK Hynix, and other electronic device manufacturers infringed four BiTMICRO patents, including the '190 Patent.

[7] Available at https://business.kioxia.com/content/dam/kioxia/shared/business/memory/doc/KIOXIA_Automotive_NAND_Data_Retention_White_Paper.pdf

65. In response to the subpoena, counsel for KIOXIA conferred with BiTMICRO's ITC counsel regarding the subpoena and its scope. BiTMICRO eventually decided to withdraw the subpoena due to insufficient time left in the fact discovery period in the ITC Action.

66. On information and belief, through its participation in the ITC Action as described above, KIOXIA had knowledge of the '190 Patent and its relevance to the '190 Accused Products. Despite this knowledge, KIOXIA has continued to directly infringe one or more claims of the '190 Patent as described above. Thus, on information and belief, KIOXIA's infringement of the '190 Patent has been willful.

67. On information and belief, KIOXIA is also inducing and/or has induced infringement of one or more claims of the '190 Patent, including at least claim 59, as a result of, amongst other activities, instructing, encouraging, and directing its customers on the use of the '190 Accused Products in an infringing manner in violation of 35 U.S.C. § 271(b). Through its website, instructional guides, and manuals, KIOXIA provides its customers with detailed explanations, instructions, and information on how to use and implement the '190 Accused Products which demonstrate active steps taken to encourage direct infringement. (*See, e.g.*, XG6 Product Brief;[8] Kioxia White Paper, "Why Data Retention is Becoming More Critical in Automotive Applications"[9]). On information and belief, KIOXIA has had knowledge of the '190 Patent since at least September 2018 as set forth above, and also as of the filing and/or service date of the original Complaint in this action. Despite this knowledge, KIOXIA has continued to engage in activities to encourage and assist its customers in the use of the '190 Accused Products. Thus, on information

[8] Available at https://business.kioxia.com/content/dam/kioxia/shared/business/ssd/doc/cSSD-XG6-product-brief.pdf

[9] Available at https://business.kioxia.com/content/dam/kioxia/shared/business/memory/doc/KIOXIA_Automotive_NAND_Data_Retention_White_Paper.pdf

and belief, KIOXIA (1) had actual knowledge of the patent; (2) knowingly induced its customers to infringe the patent; and (3) had specific intent to induce the patent infringement.

68. On information and belief, by using the '190 Accused Products as encouraged and assisted by KIOXIA, KIOXIA's customers have directly infringed and continue to directly infringe one or more claims of the '190 Patent, including at least claim 59. On information and belief, KIOXIA knew or was willfully blind to the fact that its actions would induce its customers' direct infringement of the '190 Patent.

69. KIOXIA's infringement of the '190 Patent has been and continues to be deliberate and willful, and this is therefore an exceptional case warranting an award of enhanced damages and attorneys' fees and costs pursuant to 35 U.S.C. §§ 284-285.

70. On information and belief, KIOXIA will continue to infringe the '190 Patent unless enjoined by this Court.

71. As a result of KIOXIA's infringement of the '190 Patent, BiTMICRO has suffered monetary damages, and seeks recovery, in an amount to be proven at trial, adequate to compensate for KIOXIA's infringement, but in no event less than a reasonable royalty with interest and costs. KIOXIA's infringement of BiTMICRO's rights under the '190 Patent will continue to damage BiTMICRO, causing irreparable harm for which there is no adequate remedy at law, unless enjoined by this Court.

SECOND COUNT

(INFRINGEMENT OF U.S. PATENT NO. 8,010,740)

72. BiTMICRO incorporates by reference the allegations set forth in paragraphs 1-71 as though fully set forth herein.

73. On information and belief, KIOXIA has directly infringed and continues to directly infringe one or more claims of the '740 Patent, including at least claim 1 of the '740 Patent, in the state of Texas, in this judicial district, and elsewhere in the United States by, among other things, making, using, selling, offering for sale, and/or importing into the United States products that embody one or more of the inventions claimed in the '740 Patent, including but not limited to the above-identified NVMe SSDs and all reasonably similar products ("the '740 Accused Products"), in violation of 35 U.S.C. § 271(a).

74. As an example, KIOXIA's BG4 Series SSDs include "a mapping table for optimizing memory operations performed by an electronic storage device in response to receiving an I/O transaction request initiated by a host." Specifically, the SSDs include a mapping table located in DRAM or other memory to map logical block addresses (LBAs) to physical block addresses (PBAs) on the memory devices within the SSD. (*See* KIOXIA White Paper, "Delivering Improved Performance and Power Efficiency with Next-Generation BG4 Series Client NVMe™ SSDs,"[10] at 7 ("In support of the NVMe 1.3b specification, the BG4 Series supports namespace management commands that enable data to be organized as objects as opposed to traditional block or file-based approaches. . . . Specification support also enables the BG4 Series to delete the mapping table and erase all blocks that have been written to, using the Sanitize Command.")). KIOXIA sometimes refers to this mapping table as a "lookup table" or "LUT":

[10] Available at https://business.kioxia.com/content/dam/kioxia/shared/business/ssd/doc/whitepaper-cSSD-BG4.pdf

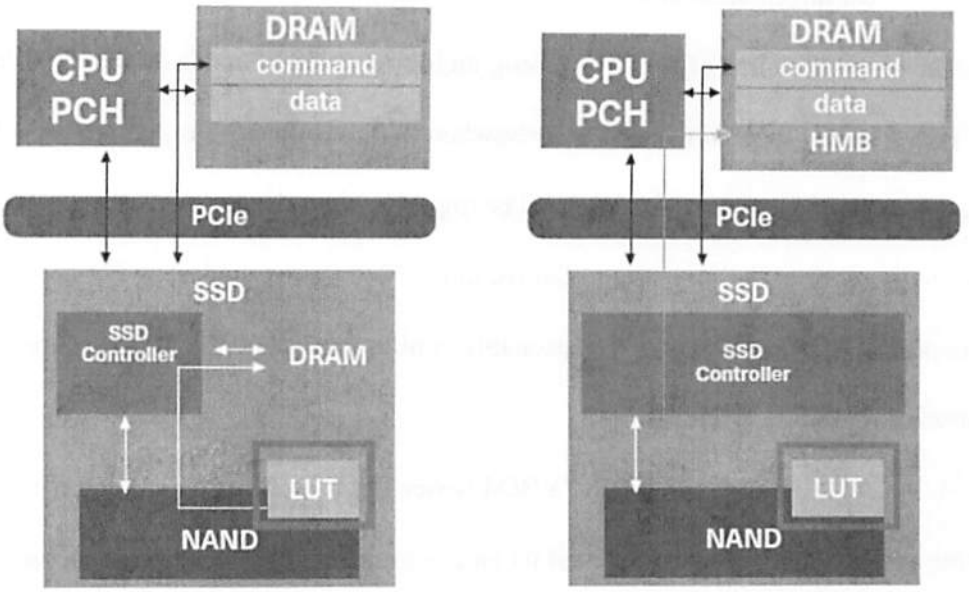

Figure 1 depicts a traditional client SSD and one with Host Memory Buffer (HMB) architecture

(*Id.* at 1).

75. Information in the indirection table is used by a controller in the BG4 Series SSDs to optimize memory operations, by for example allowing the controller to perform interleaving to optimally distribute data across multiple non-volatile memory channels, lanes, buses, devices, dies, planes, etc., thereby improving the speed and efficiency of storing and accessing the data. (*See, e.g.*, "Maximizing SSD Performance"[11] ("As one of the world's largest SSD manufacturers, KIOXIA has a great deal of expertise in NVMe and NVMe-oF technology . . . . Each NAND Flash die in recent generation SSDs can hold 32 or 64 Gigabytes of raw data. When using 32GB die, we need about 32 of them per Terabyte (TB). Flash die are typically divided into two or four planes, which are separate storage regions which operate somewhat independently, and can be treated for many purposes as if they were separate ICs. Each plane can process a single command (read, write,

[11] Available at https://kumoscale.kioxia.com/en/performance/ssd-performance

or erase) at a time. For a hypothetical one TB drive comprising 32 two-plane die, it can at most process 64 read, write, or erase commands simultaneously."); KIOXIA White Paper, "Delivering Improved Performance and Power Efficiency with Next-Generation BG4 Series Client NVMe™ SSDs,"[12] at 2 ("The BG4 Series is KIOXIA's fourth generation of single package BGA SSDs and announced to the industry in January 2019. BG4 utilizes 96-layer BiCS FLASH 3D technology and also leverages the HMB feature, but within the NVMe Revision 1.3b specification. This product doubles the lane count with support for PCIe Gen3 x4 lanes, and delivers more performance in the same power envelope when compared to other products.")).

76. The mapping table of the BG4 Series SSDs also includes "a set of logical fields, including a first logical field and a second logical field, and said logical fields respectively disposed for representing a plurality of LBA sets, including said first logical field disposed for representing a first LBA set and said second logical field disposed for representing a second LBA set, said first and second LBA sets each representing a set of consecutive LBAs." For example, the mapping table includes a set of logical fields that represent sets of consecutive LBAs:

5a Sequential Read

Sequential read is a data access pattern whereby large contiguous blocks of data, 128KiB[9] in this test case, are read from adjacent logical block addresses of flash memory in sequential order. The term is used mostly for benchmarking, and speed is measured in MB/s. This kind of performance testing is read-intensive (100% read and 0% write) at the application level (Table 1).

SSD Tested	Highest Result (5 runs)	BG4 Advantage
BG3 Series	1,635 MB/s	
BG4 Series	2,336 MB/s	+43%

Table 1: Sequential read comparison between BG3 Series and BG4 Series SSDs (higher is better)

[12] Available at https://business.kioxia.com/content/dam/kioxia/shared/business/ssd/doc/whitepaper-cSSD-BG4.pdf

(KIOXIA White Paper, "Delivering Improved Performance and Power Efficiency with Next-Generation BG4 Series Client NVMe™ SSDs,"[13] at 4).

77. The mapping table of the BG4 Series SSDs also includes "a set of PBA fields, including a first PBA field and a second PBA field, said set of PBA fields respectively disposed for representing a set of PBAs, including a first PBA disposed for representing a first set of access parameters and a second PBA disposed for representing a second set of access parameters, said PBAs each associated with a physical memory location in a memory store, said set of logical fields and said set of PBA fields disposed to associate said first and second LBA sets with said first and second PBAs." For example, the first and second PBAs can be associated with different non-volatile memory channels, lanes, buses, devices, dies, planes, etc. within the SSD. *See, e.g.*, "Maximizing SSD Performance"[14] ("As one of the world's largest SSD manufacturers, KIOXIA has a great deal of expertise in NVMe and NVMe-oF technology . . . . Each NAND Flash die in recent generation SSDs can hold 32 or 64 Gigabytes of raw data. When using 32GB die, we need about 32 of them per Terabyte (TB). Flash die are typically divided into two or four planes, which are separate storage regions which operate somewhat independently, and can be treated for many purposes as if they were separate ICs. Each plane can process a single command (read, write, or erase) at a time. For a hypothetical one TB drive comprising 32 two-plane die, it can at most process 64 read, write, or erase commands simultaneously."); KIOXIA White Paper, "Delivering Improved Performance and Power Efficiency with Next-Generation BG4 Series Client NVMe™

[13] Available at https://business.kioxia.com/content/dam/kioxia/shared/business/ssd/doc/whitepaper-cSSD-BG4.pdf

[14] Available at https://kumoscale.kioxia.com/en/performance/ssd-performance

SSDs,"[15] at 2 ("The BG4 Series is KIOXIA's fourth generation of single package BGA SSDs and announced to the industry in January 2019. BG4 utilizes 96-layer BiCS FLASH 3D technology and also leverages the HMB feature, but within the NVMe Revision 1.3b specification. This product doubles the lane count with support for PCIe Gen3 x4 lanes, and delivers more performance in the same power envelope when compared to other products."); KIOXIA Corporation's U.S. Pub. No. 2021/0303424, at [0002]-[0005] ("[L]arge capacity SSDs have begun introducing a number of disadvantages that counteract some of traditional advantages associated with SSDs. One set of disadvantages stems from the fact that as the capacity of SSDs increases so does the amount of data required to store the logical to physical mapping information for the SSD. . . . Moreover, larger amounts of physical to logical mapping information increases the amount of data that must be transferred to non-volatile memory during a power loss event. . . . Accordingly, there is a long felt need for large capacity SSDs that reduce the amount of data required to translate logical to physical addresses.").

78. The first and second PBA fields represent these first and second PBAs, respectively, in the mapping table. Each of the PBAs has a set of access parameters defined in the mapping table, such as identifying information that allows the PBA to be associated with one or more LBAs, and the first and second LBA sets are associated with the first and second PBAs, respectively. (*See* KIOXIA White Paper, "Delivering Improved Performance and Power Efficiency with Next-Generation BG4 Series Client NVMe™ SSDs,"[16] at 7 ("In support of the NVMe 1.3b specification, the BG4 Series supports namespace management commands that enable data to be organized as

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[15] Available at https://business.kioxia.com/content/dam/kioxia/shared/business/ssd/doc/whitepaper-cSSD-BG4.pdf

[16] Available at https://business.kioxia.com/content/dam/kioxia/shared/business/ssd/doc/whitepaper-cSSD-BG4.pdf

objects as opposed to traditional block or file-based approaches. . . . An identifier assigned to each object makes it easy to index or retrieve data, or find a specific object, such as a photo or video. Specification support also enables the BG4 Series to delete the mapping table and erase all blocks that have been written to, using the Sanitize Command.")).

79. Also, the mapping table of the BG4 Series SSDs, "in response to receiving the I/O transaction request, [] causes the electronic storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first and second LBA sets." For example, the interleaving function in the SSDs allows the products to perform optimized memory operations on memory locations associated with the first PBA and second PBA by distributing the reading and writing of data across those memory locations to increase the speed and efficiency of storing and accessing the data. This interleaving requires the use of the LBA-PBA mapping information in the indirection table by the memory controller within the SSD:

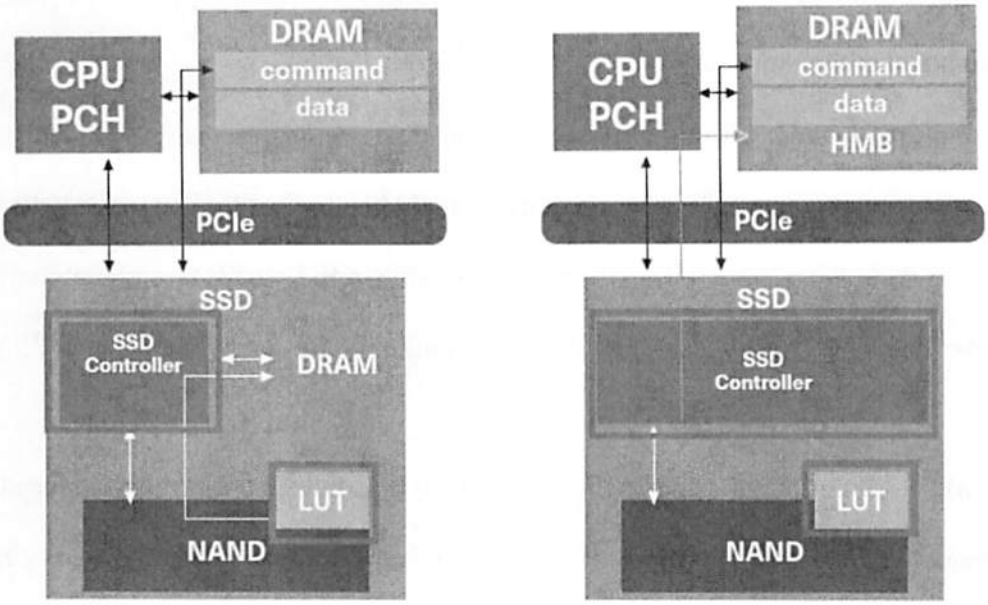

Figure 1 depicts a traditional client SSD and one with Host Memory Buffer (HMB) architecture

(KIOXIA White Paper, "Delivering Improved Performance and Power Efficiency with Next-Generation BG4 Series Client NVMe™ SSDs,"[17] at 1; *see also* "Maximizing SSD Performance"[18] ("As one of the world's largest SSD manufacturers, KIOXIA has a great deal of expertise in NVMe and NVMe-oF technology . . . . Each NAND Flash die in recent generation SSDs can hold 32 or 64 Gigabytes of raw data. When using 32GB die, we need about 32 of them per Terabyte (TB). Flash die are typically divided into two or four planes, which are separate storage regions which operate somewhat independently, and can be treated for many purposes as if they were separate ICs. Each plane can process a single command (read, write, or erase) at a time. For a

[17] Available at https://business.kioxia.com/content/dam/kioxia/shared/business/ssd/doc/whitepaper-cSSD-BG4.pdf

[18] Available at https://kumoscale.kioxia.com/en/performance/ssd-performance

hypothetical one TB drive comprising 32 two-plane die, it can at most process 64 read, write, or erase commands simultaneously.")).

80. By making, using, offering for sale, and/or selling products in the United States and/or importing products into the United States, including but not limited to the '740 Accused Products, KIOXIA has injured BiTMICRO and is liable to BiTMICRO for directly infringing one or more claims of the '740 Patent, including without limitation claim 1 pursuant to 35 U.S.C. § 271(a).

81. On information and belief, KIOXIA is also inducing and/or has induced infringement of one or more claims of the '740 Patent, including at least claim 1, as a result of, amongst other activities, instructing, encouraging, and directing its customers on the use of the '740 Accused Products in an infringing manner in violation of 35 U.S.C. § 271(b). Through its website, instructional guides, and manuals, KIOXIA provides its customers with detailed explanations, instructions, and information on how to use and implement the '740 Accused Products which demonstrate active steps taken to encourage direct infringement. (*See, e.g.,* KIOXIA White Paper, "Delivering Improved Performance and Power Efficiency with Next-Generation BG4 Series Client NVMe™ SSDs"[19]; "Maximizing SSD Performance"[20]).

82. On information and belief, KIOXIA has had knowledge of the '740 Patent at least as of the filing and/or service of the original Complaint in this action. Despite this knowledge, KIOXIA has continued to engage in activities to encourage and assist its customers in the use of the '740 Accused Products. Thus, on information and belief, KIOXIA (1) had actual knowledge of the

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[19] Available at https://business.kioxia.com/content/dam/kioxia/shared/business/ssd/doc/whitepaper-cSSD-BG4.pdf

[20] Available at https://kumoscale.kioxia.com/en/performance/ssd-performance

patent; (2) knowingly induced its customers to infringe the patent; and (3) had specific intent to induce the patent infringement.

83. On information and belief, by using the '740 Accused Products as encouraged and assisted by KIOXIA, KIOXIA's customers have directly infringed and continue to directly infringe one or more claims of the '740 Patent, including at least claim 1. On information and belief, KIOXIA knew or was willfully blind to the fact that its actions would induce its customers' direct infringement of the '740 Patent.

84. KIOXIA's infringement of the '740 Patent has been and continues to be deliberate and willful, and this is therefore an exceptional case warranting an award of enhanced damages and attorneys' fees and costs pursuant to 35 U.S.C. §§ 284-285.

85. On information and belief, KIOXIA will continue to infringe the '740 Patent unless enjoined by this Court.

86. As a result of KIOXIA's infringement of the '740 Patent, BiTMICRO has suffered monetary damages, and seeks recovery, in an amount to be proven at trial, adequate to compensate for KIOXIA's infringement, but in no event less than a reasonable royalty with interest and costs. KIOXIA's infringement of BiTMICRO's rights under the '740 Patent will continue to damage BiTMICRO, causing irreparable harm for which there is no adequate remedy at law, unless enjoined by this Court.

THIRD COUNT

(INFRINGEMENT OF U.S. PATENT NO. 6,496,939)

87. BiTMICRO incorporates by reference the allegations set forth in paragraphs 1-86 as though fully set forth herein.

88. KIOXIA has directly infringed one or more claims of the '939 Patent, including at least claim 10 of the '939 Patent, in the state of Texas, in this judicial district, and elsewhere in the United States by, among other things, making, using, selling, offering for sale, and/or importing into the United States products that embody one or more of the inventions claimed in the '939 Patent, including but not limited to the above-identified SSDs with Power Loss Protection, and all reasonably similar products ("the '939 Accused Products"), in violation of 35 U.S.C. § 271(a).

89. Each of the '939 Accused Products includes "a system for controlling data in a computer system when the computer system loses power." KIOXIA (and formerly Toshiba) referred to this feature as "Power Loss Protection" or "PLP." KIOXIA's product documentation for its CM and PM Enterprise SSDs explains that "PLP allows to record data in buffer memory to flash memory, utilizing back up power of solid capacitor in case of sudden supply shut down."[21]

90. The system of the '939 Accused Products further includes "means for activating a plurality of super capacitors to supply power to the computing engine based upon power being removed from the computer system." As noted above, KIOXIA's PLP utilizes "back up power of solid capacitor," which "in case of sudden supply shut down" are activated to supply power to the SSD. In addition, the '939 Accused Products further include means for "reconfiguring the data in the computing engine" in the event of a power loss, and "deactivating the plurality of super capacitors to cut off power to the computing engine based upon the plurality of super capacitors discharging to a predetermined level." As further noted above, "in case of sudden supply shut down," KIOXIA's PLP utilizes the "back up power of solid capacitor" to, *inter alia*, "record data in buffer memory to flash memory."

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[21] Available at https://business.kioxia.com/content/dam/kioxia/emea/en-gb/business/SSD/Support/dl/ KIOXIA%20Enterprise%20SSD_Data%20Sheet_E_Ver03.21_EMEA.pdf.

91. KIOXIA (and/or its predecessor) have applied and/or obtained a number of patents related to PLP that, on information and belief, describe the operation of KIOXIA's PLP and the value of PLP to KIOXIA and its customers. For example, U.S. Patent No. 10,139,884, which was applied for by Toshiba Memory Corp. and is currently assigned to KIOXIA, is entitled "Power loss protection for solid state drives" and "generally relates to power loss protection (PLP) for solid state drives (SSDs)." The Background of the Invention in that KIOXIA patent describes the PLP feature:

> As the solid state drive (SSD) plays an increasingly important role in computer and enterprise storage, there is a correlated increase in importance and reliance on the use of backup power sources, such as supercapacitors, to help prevent data loss in the SSD from occurring due to power outage or power loss. This feature is generally referred to as power loss protection (PLP). When a power outage or power loss occurs for a host device, such as a computer, with an SSD, the energy stored by the supercapacitor provides backup power to ensure that all pending commands are successfully completed by the SSD, all critical data is saved, and the SSD can shut down properly.

On information and belief, the PLP feature in the '939 Accused Products are designed and operate consistent with this description, confirming infringement of at least claim 10 of the '939 Patent.

92. As a result of KIOXIA's infringement of the '939 Patent, BiTMICRO has suffered monetary damages, and seeks recovery, in an amount to be proven at trial, adequate to compensate for KIOXIA's infringement, but in no event less than a reasonable royalty with interest and costs.

PRAYER FOR RELIEF

WHEREFORE, BiTMICRO prays for judgment and seeks relief against KIOXIA as follows:

A. For judgment that KIOXIA has infringed and/or continue to infringe one or more claims of the Asserted Patents, directly, and/or indirectly by way of inducement;

B. For a permanent injunction against KIOXIA and its respective officers, directors, agents, servants, affiliates, employees, divisions, branches, subsidiaries, parents, and

all other acting in active concert therewith from infringement of the Asserted Patents;

C. For an accounting of all damages sustained by BiTMICRO as the result of KIOXIA's acts of infringement;

D. For a mandatory future royalty payable on each and every future sale by KIOXIA of a product that is found to infringe one or more of the Asserted Patents and on all future products which are reasonably similar to those products found to infringe;

E. For a judgment and order finding that KIOXIA's infringement is willful and awarding to BiTMICRO enhanced damages pursuant to 35 U.S.C. § 284;

F. For a judgment and order requiring KIOXIA to pay BiTMICRO's damages, costs, expenses, and pre- and post-judgment interest for its infringement of the Asserted Patents as provided under 35 U.S.C. § 284;

G. For a judgment and order finding that this is an exceptional case within the meaning of 35 U.S.C. § 285 and awarding to BiTMICRO its reasonable attorneys' fees; and

H. For such other and further relief in law and in equity as the Court may deem just and proper.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure, BiTMICRO hereby demands a trial by jury of this action.

Dated: June 3, 2022

Respectfully submitted,

/s/ B. Russell Horton

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