IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

PROFESSOR MASAHIRO IIDA, Plaintiff, v. INTEL CORPORATION, Defendant.	Case No. 6:22-CV-00662 **JURY TRIAL DEMANDED**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff, Professor Masahiro Iida ("Professor Iida"), files this Complaint against Defendant, Intel Corporation ("Intel"), for infringement of U.S. Patent No. 6,812,737 in connection with its manufacture, use, offering for sale, and sale of programmable logic devices – Field Programmable Gate Array ("FPGA") chips and System-on-Chip ("SoC") chips – that employ Adaptive Logic Modules (the "Accused Products"), and alleges as follows:

PARTIES

1. Professor Iida is an adult individual and Japanese citizen residing at 7-chōme-11-6 Toroku Chūō-ku, Kumamoto, Japan. He holds a Doctorate of Engineering in Systems and Information Science from Kumamoto University, and is Chair of the Department of Computer Science and Electrical Engineering in the Faculty of Engineering at Kumamoto University located in Kumamoto, Japan.

2. Professor Iida is the inventor and owner of U.S. Patent No. 6,812,737 (the "'737 patent") entitled "PROGRAMMABLE LOGIC CIRCUIT DEVICE HAVING LOOK UP

TABLE ENABLING TO REDUCE IMPLEMENTATION AREA." A copy of the '737 patent is attached as Exhibit 1.

3. Intel is a corporation duly organized and existing under the laws of the State of Delaware, and has regular and established places of business in the Western District of Texas, including at 1300 S. Mopac Expressway, Austin, Texas 78746.

4. Intel can be served with process through its registered agent for service in Texas: CT Corporation System, 1999 Bryan Street, Suite 900, Dallas, Texas 75201.

5. Since at least April 1989, Intel has been registered to do business in the State of Texas under Texas Taxpayer No. 19416727436.

JURISDICTION

6. This action arises under the Patent Laws of the United States, 35 U.S.C. § 1, *et seq*., and this Court has subject matter jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and 1338(a).

7. The United States District Court for the Western District of Texas has general and specific personal jurisdiction over Intel because Intel has sufficient minimum contacts with this forum as a result of the business it regularly conducts within the State of Texas and in this District. In particular, this Court has personal jurisdiction over Intel because, *inter alia*, Intel, on information and belief: (1) has substantial, continuous, and systematic business contacts with this State and this District; (2) owns, manages, and/or operates facilities in this State and this District; (3) enjoys substantial income from its operations in this State and this District; (4) employs Texas residents in this State and this District; and (5) solicits business and markets goods, including the Accused Products, in this State and this District.

8. Intel has also purposefully and voluntarily availed itself of the privileges of conducting business in the State of Texas, and the Western District of Texas, by continuously and systematically placing goods, including the Accused Products, into the stream of commerce through an established distribution channel with the expectation that they will be purchased by consumers in Texas and in this District.

9. Intel is subject to this Court's personal jurisdiction in accordance with due process and/or the Texas Long Arm Statute because, in part, Intel "[r]ecruits Texas residents, directly or through an intermediary located in this state, for employment inside or outside this state." Tex. Civ. Prac. & Rem. Code § 17.042.

10. This Court also has personal jurisdiction over Intel because Intel (directly and/or through its subsidiaries, affiliates, or intermediaries) has committed and continues to commit acts of patent infringement in this judicial district in violation of at least 35 U.S.C. § 271(a).

11. Professor Iida's cause of action arises, at least in part, from Intel's contacts with and activities in the State of Texas and within this District. Upon information and belief, Defendant has committed acts of patent infringement within this District giving rise to this action, including offering to sell and/or selling the Accused Products to customers in this District.

12. Intel has committed, and continues to commit, acts of patent infringement within the United States, the State of Texas, and this District.

VENUE

13. Venue is proper in this District under 35 U.S.C. § 1400(b) because: (1) there is a physical place located in this District, (2) it is a regular and established place of business, and (3) it is the place of Intel. *See In re Cray Inc.*, 871 F.3d 1355, 1360 (Fed. Cir. 2017).

14. In touting its research and development facility in Austin, Intel declares that it is "proud to call Texas home."[1]

15. Intel maintains several facilities, which it refers to as campuses, in this District.[2]

16. Intel maintains a campus at 1300 S. Mopac Expressway, Austin Texas 78746 which it calls the Barton Skyway Campus.[3] This is a regular and established place of business within this District belonging to Intel.

17. Intel also maintains a campus at 9442 N. Capital of Texas Hwy., Bldg. 2, Suite 600, Austin, Texas 78759 which it calls the Austin FSO, Arboretum Campus.[4] This is a regular and established place of business within this District belonging to Intel.

18. Intel's Austin facilities include a research and development center with close to 1,800 employees.[5]

19. Intel's Austin facilities are focused on supporting innovations in, among other things, programmable logic devices.[6]

20. Intel's interest in programmable logic devices dates back at least to December 28, 2015, with its acquisition of Altera Corporation ("Altera"), one the largest designers and fabricators of FPGA products at that time.

21. Intel purchased Altera for approximately $16.7 billion.

[1] Intel in Texas, Intel Website (last visited June 2022), available at: https://www.intel.com/content/www/us/en/corporate-responsibility/intel-in-texas.html
[2] Contact Intel, Intel Website (last visited June 2022), available at: https://www.intel.com/content/www/us/en/support/contact-intel.html?tab=campus-locations#support-us-locations
[3] *Id*.
[4] *Id*.
[5] Intel in Texas, Intel Website (last visited June 2022), available at: https://www.intel.com/content/www/us/en/corporate-responsibility/intel-in-texas.html
[6] *Id*.

22. Intel acquired Altera, at least in part, because Altera was a "leading provider of field programmable gate array (FPGA) technology."[7]

23. The operations of Altera designing and selling FPGA products continued as a new business unit of Intel called the Programmable Solutions Group ("PSG").

24. From 2016 through 2021, the PSG was one of six separately reporting business units, called operating segments, through which Intel conducted and reported its operations.

25. As of the first quarter of 2022, Intel implemented a reorganization of its various business operations in which financial results were to be reported under six different operating segments. The operations of the PSG are now included as part of the Data Center and AI ("DCAI") Group, and revenues previously attributed to the PSG are now reported as part of the revenues for the DCAI Group.

26. Certain of Intel's operations within the PSG, including operations relating to design and sale of the Accused Products, have been planned and executed, and continue to be planned and executed, in this District.

27. Intel employees in this District have worked, and presently work, on the design, sale, and support of the Accused Products. Many of these employees are senior level software, firmware, and/or hardware engineers who worked on the Accused Products for Altera in this District and who continued to work on the Accused Products in the PSG for Intel in this District since its acquisition of Altera in 2015. *See* LinkedIn profile page screen captures attached, collectively, as Exhibit 2.[8]

---

[7] Press Release, Intel Website (last visited June 2022), available at: https://download.intel.com/newsroom/2021/archive/2015-12-28-news-releases-intel-completes-acquisition-of-altera.pdf

[8] Full profiles of the identified Intel employees are accessible on LinkedIn website (last visited June 2022) at: Bacrau: https://www.linkedin.com/in/radubacrau/

28. Intel is currently looking to fill positions within the PSG that are principally located in this District.[9]

29. Upon information and belief, Intel's records relating to the design and sales of the Accused Products are accessible in this District by employees within the PSG who work in this District.

THE ASSERTED PATENT

30. In 2001, Professor Iida was a doctoral student conducting research on FPGA architecture. During the course of his research, Professor Iida discovered a revolutionary way to flexibly configure large look up tables (LUTs), primitive logic elements used in programmable

---

Baumgartner: https://www.linkedin.com/in/yoanna-baumgartner-6327073/
Blake: https://www.linkedin.com/in/galen-blake-3b657b1b/
Brice: https://www.linkedin.com/in/bricedonaldn/
Cid: https://www.linkedin.com/in/alberto-cid-a944151/
Cozart: https://www.linkedin.com/in/sue-cozart-89a58224/
Ehrlich: https://www.linkedin.com/in/rehrlich/
Elias: https://www.linkedin.com/in/vinu-k-elias-a6424132/
Flores: https://www.linkedin.com/in/jpcf/
Howell: https://www.linkedin.com/in/richardwhowell/
Jackson: https://www.linkedin.com/in/andy-jackson-387b851/
Law: https://www.linkedin.com/in/sweehua/
Leong: https://www.linkedin.com/in/deam-ieong-49632557/
Lim: https://www.linkedin.com/in/kong-wai-lim-29234321/
Martin: https://www.linkedin.com/in/susannah-martin-b716422/
Mata: https://www.linkedin.com/in/luis-mata-04367646/
Nasirian: https://www.linkedin.com/in/nasimnasirian/
Nguyen: https://www.linkedin.com/in/dinh-nguyen-086b17/
Reipold: https://www.linkedin.com/in/tony-reipold-20153518/
Slockers: https://www.linkedin.com/in/shawn-slockers-52189b1a/
Song: https://www.linkedin.com/in/zhen-song-a4a72219/
Velagapudi: https://www.linkedin.com/in/supriya-velagapudi-a4375a/
Vyas: https://www.linkedin.com/in/neema-vyas-b1326181/
Williams: https://www.linkedin.com/in/kirtwilliams/
Wilson: https://www.linkedin.com/in/david-wilson-791897/
Zhou: https://www.linkedin.com/in/biyun-zhou-bb89999/

[9] Field Applications Engineer Job Posting, Intel Website (last visited June 2022), accessible at: https://jobs.intel.com/ShowJob/Id/3355235/Field-Applications-Engineer
Design for Test Engineer Job Posting, Intel Website (last visited June 2022), accessible at: https://jobs.intel.com/ShowJob/Id/3446865/Design-for-Test-Engineer-(DFT)

logic devices (such as FPGA chips), so that a single M-input N-output LUT can operate either as a single "whole" LUT or as a plurality of "fractured" LUTs.

31. This breakthrough in LUT architecture enabled a significant reduction in both implementation area and power consumption for chips utilizing this innovation.

32. For over 20 years, Professor Iida has remained at the forefront of his field by teaching, conducting research, presenting at conferences, and publishing hundreds of articles and other papers on various topics relating to programmable logic devices.

33. On June 29, 2001, a Japanese patent application was filed on Professor Iida's invention.

34. On June 28, 2002, a United States patent application was filed on Professor Iida's invention, claiming priority directly to the prior-filed Japanese patent application.

35. On November 2, 2004, the United States Patent and Trademark Office duly and legally issued the '737 patent.

36. Since October 1, 2014, Professor Iida has been, and is presently, the sole owner of all right, title, and interest in the '737 patent.

37. By virtue of the claim of priority directly to a foreign application under 35 U.S.C. § 119 (as opposed to a claim of priority through a PCT application), the 20-year term of the '737 patent is measured from its U.S. filing date. As a result, the '737 patent expires on June 28, 2022.

38. The '737 patent is presumed valid under 35 U.S.C. § 282.

THE ACCUSED PRODUCTS

39. The Accused Products are Intel's programmable logic devices – FPGA chips and SoC chips – that employ Adaptive Logic Modules (ALMs).

40. Altera first employed ALMs into their programmable logic devices with the introduction of the Stratix II line of FPGA chips in 2004.

41. Altera expanded its use of ALMs by incorporating them into later generations of Stratix chips (*i.e.*, Stratix III, Stratix IV, Stratix V, and Stratix 10) as well as certain of its Arria and Cyclone lines of FPGA and SoC chips.

42. With its acquisition of Altera in 2016, Intel continued the operations of Altera through its newly constituted business segment – the Programmable Solutions Group – which included the design, manufacture, sale, and support of Stratix, Arria, and Cyclone chips that employ ALMs.

43. In addition to continuing to make and sell Stratix, Arria, and Cyclone FPGA and SoC chips that employ ALMs, Intel introduced a new line of FPGA and SoC chips under the Agilex name that also employ ALMs.

44. Intel has made, used, offered for sale, and/or sold, and continues to make, use, offer for sale, and/or sell, the following FPGA and SoC chips that employ ALMs:

a. Stratix II FPGA products including EP2S15, EP2S30, EP2S60, EP2S90, EP2S130, and EP2S180;

b. Stratix III E FPGA products including EP3SE50, EP3SE80, EP3SE110, and EP3SE260;

c. Stratix III L FPGA products including EP3SL50, EP3SL70, EP3SL110, EP3SL150, EP3SL200, and EP3SL340;

d. Arria GX FPGA products including EP1AGX20, EP1AGX35, EP1AGX50, EP1AGX60 and EP1AGX90;

e. Stratix IV GT FPGA products including EP4S40G2, EP4S40G5, EP4S100G2, EP4S100G3, EP4S100G4, and EP4S100G5;

f. Stratix IV GX FPGA products including EP4SGX70, EP4SGX110, EP4SGX180, EP4SGX230, EP4SGX290, EP4SGX360, and EP4SGX530;

g. Stratix IV E FPGA products including EP4SE230, EP4SE360, EP4SE530, and EP4SE820;

h. Arria II GX FPGA products including EP2AGX45, EP2AGX65, EP2AGX95, EP2AGX125, EP2AGX190, and EP2AGX260;

i. Arria II GZ FPGA products including EP2AGZ225, EP2AGZ300, and EP2AGZ350;

j. Stratix V E FPGA products including 5SEE9 and 5SEEB;

k. Stratix V GS FPGA products including 5SGSD3, 5SGSD4, 5SGSD5, 5SGSD6, and 5SGSD8;

l. Stratix V GX FPGA products including 5SGXA3, 5SGXA4, 5SGXA5, 5SGXA7, 5SGXA9, 5SGXAB, 5SGXB5, 5SGXB6, 5SGXB9, and 5SGXBB;

m. Arria V GT FPGA products including 5AGTC3, 5AGTC7, 5AGTD3, and 5AGTD7;

n. Arria V GX FPGA products including 5AGXA1, 5AGXA3, 5AGXA5, 5AGXA7, 5AGXB1, 5AGXB3, 5AGXB5, and 5AGXB7;

o. Arria V GZ FPGA products including 5AGZE1, 5AGZE3, 5AGZE5, and 5AGZE7;

p. Arria V ST SoC products including 5ASTD3 and 5ASTD5;

q. Arria V SX SoC products including 5ASXB3 and 5ASXB5;

r. Cyclone V E FPGA products including 5CEA2, 5CEA4, 5CEA5, 5CEA7, and 5CEA9;

s. Cyclone V GT FPGA products including 5CGTD5, 5CGTD7, and 5CGTD9;

t. Cyclone V GX FPGA products including 5CGXC3, 5CGXC4, 5CGXC5, 5CGXC7, and 5CGXC9;

u. Cyclone V SE SoC products including 5CSEA2, 5CSEA4, 5CSEA5, and 5CSEA6;

v. Cyclone V ST SoC products including 5CSTD5 and 5CSTD6;

w. Cyclone V SX SoC products including 5CSXC2, 5CSXC4, 5CSXC5, and 5CSXC6;

x. Stratix 10 DX SoC FPGA products including DX 1100, DX 2100, and DX 2800;

y. Stratix 10 GX FPGA products including GX 400, GX 650, GX 850, GX 1100, GX 1650, GX 2100, GX 2500, GX 2800, GX 1660, GX 2110, and GX 10M;

z. Stratix 10 MX FPGA products including MX 1650 and MX 2100;

aa. Stratix 10 SX SoC products including SX 400, SX 650, SX 850, SX 1100, SX 1650, SX 2100, SX 2500, and SX 2800;

bb. Stratix 10 TX FPGA products including TX 400, TX 850, TX 1100, TX 1650, TX 2100, TX 2500, and TX 2800;

cc. Stratix NX FPGA products including NX 2100;

dd. Arria 10 GT FPGA products including GT 900 and GT 1150;

ee. Arria 10 GX FPGA products including GX 160, GX 220, GX 270, GX 320, GX 480, GX 570, GX 660, GX 900, and GX 1150;

ff. Arria 10 SX SoC products including SX 160, SX 220, SX 270, SX 320, SX 480, SX 570, and SX 660;

gg. Cyclone 10 GX FPGA products including 10CX085, 10CX105, 10CX150, and 10CX220;

hh. Agilex F-Series FPGA and SoC FPGA products including AGF 004, AGF 006, AGF 008, AGF 012, AGF 014, AGF 022, and AGF 027;

ii. Agilex I-Series SoC FPGA products including AGI 022 and AGI 027; and

jj. Agilex M-Series FPGA products including AGM 032 and AGM 039.

45. Upon information and belief, Intel's annual revenues over the past six years from the sale of the Accused Products constitute at least 80%, by dollar volume, of Intel's annual revenues from the sale of products attributed to the PSG over that same period.

46. Intel recognized revenues of approximately $425 million in Q3 of 2016 from the sale of products attributed to the PSG.

47. Intel recognized revenues of approximately $420 million in Q4 of 2016 from the sale of products attributed to the PSG.

48. Intel recognized revenues of approximately $1.902 billion in 2017 from the sale of products attributed to the PSG.

49. Intel recognized revenues of approximately $2.123 billion in 2018 from the sale of products attributed to the PSG.

50. Intel recognized revenues of approximately $1.987 billion in 2019 from the sale of products attributed to the PSG.

51. Intel recognized revenues of approximately $1.853 billion in 2020 from the sale of products attributed to the PSG.

52. Intel recognized revenues of approximately $1.934 billion in 2021 from the sale of products attributed to the PSG.

53. Assuming the historical demand for Intel's programmable logic devices has continued into 2022, Intel should recognize at least $900 million over the first half of 2022 from the sale of products that, prior to 2022, were attributed by Intel to its PSG (which are now reported within its DCAI Group).

54. Over the six-year period immediately preceding the filing of this Complaint, Intel will have recognized at least $11.5 billion from the sale of products attributed to the PSG. Upon information and belief, at least 80% of those revenues will have been associated with the sale of the Accused Products.

CLAIMS FOR RELIEF

COUNT I – Direct Infringement of '737 Patent

55. The allegations set forth above are re-alleged and incorporated by reference as if they were set forth fully here.

56. Intel has directly infringed (literally and/or under the doctrine of equivalents), and continues to infringe, at least claim 1 of the '737 patent by making, using, offering to sell, and selling the Accused Products without a license from Professor Iida.

57. Professor Iida is the sole owner of all right, title, and interest in the '737 patent with full rights to pursue recovery of damages for infringement.

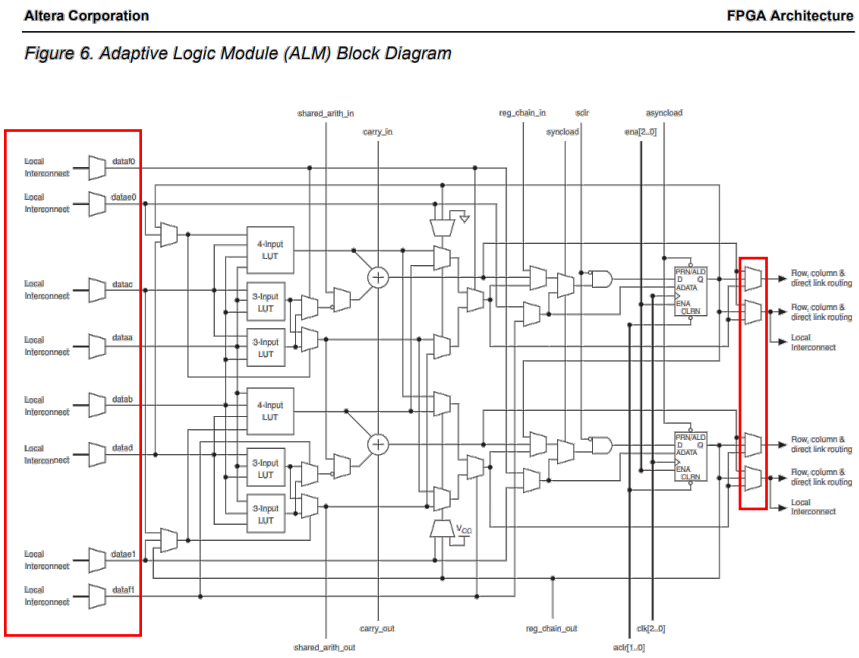
58. Each claim of the '737 patent is valid, enforceable, and patent-eligible.

59. Intel has never, either expressly or impliedly, been licensed under the '737 patent.

60. The Accused Products are Intel FPGA chips and SoC chips, as well as all other Intel products, that employ Adaptive Logic Modules (ALMs).

61. ALMs are radically different from any other FPGA logic block, offering a number of major innovations.[10]

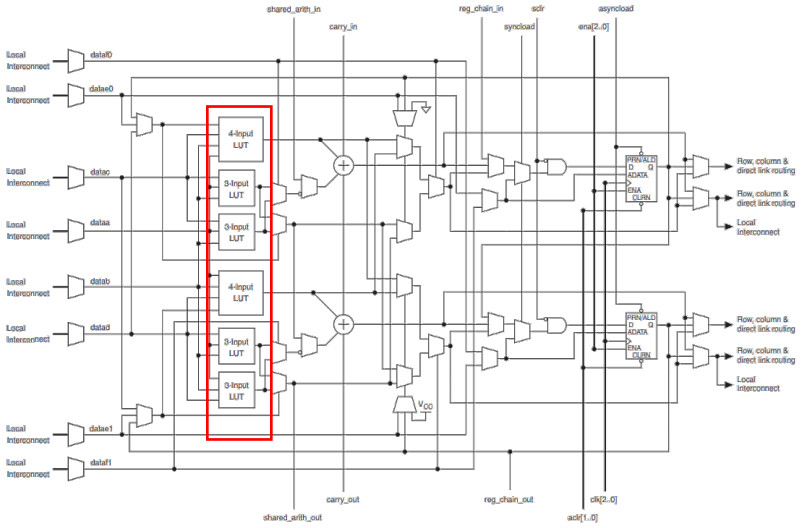
62. Intel's ALMs have look up tables (LUTs) that have M inputs and N outputs:[11]



[10] *See* Altera FPGA Architecture White Paper (attached as Exhibit 3) at p. 4.
[11] *Id.* at p. 7.

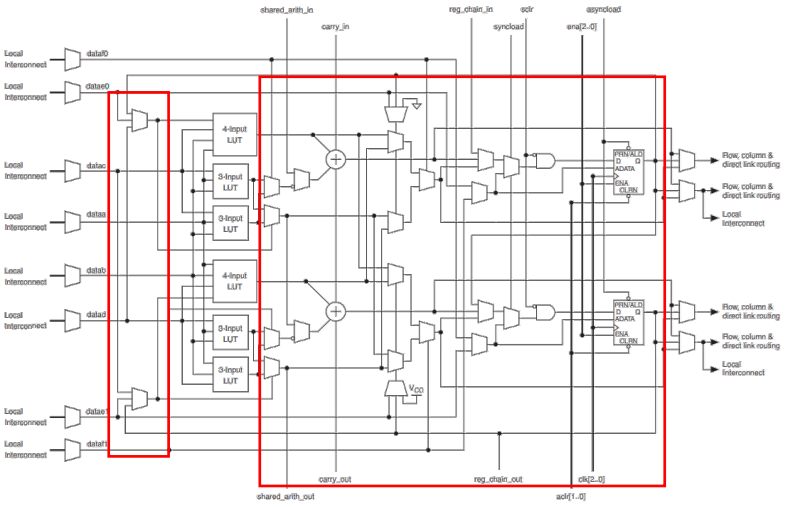
63. The LUTs in Intel's ALMs comprise a plurality of LUT units:[12]

Figure 6. Adaptive Logic Module (ALM) Block Diagram



64. The LUTs in Intel's ALMs also comprise an internal configuration control circuit:[13]

Figure 6. Adaptive Logic Module (ALM) Block Diagram

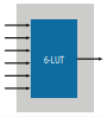
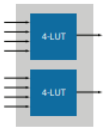
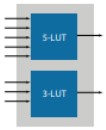
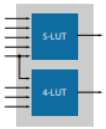
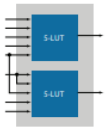
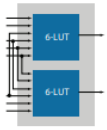
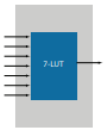


[12] *Id.*
[13] *Id.*

65. The internal configuration control circuit of the LUTs in Intel's ALMs controls the internal configuration of the plurality of LUT units. A summary of combinational logic configurations supported in an ALM are shown in the following table:[14]

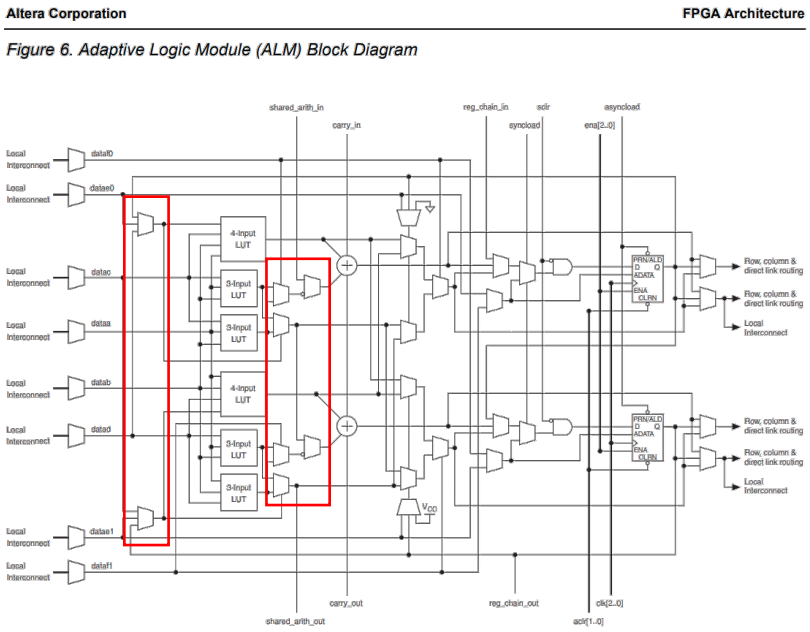
FPGA Architecture **Altera Corporation**

Table 1. ALM Flexibility

Configuration	Description
	One Stratix II ALM can input any 6-input function.
	One Stratix II ALM can be configured to implement 2 independent 4-input or smaller LUTs. This configuration can be viewed as the "backward-compatibility" mode. Designs that are optimized for the traditional 4-LUT FPGAs can easily be migrated to the Stratix II family.
	One Stratix II ALM can be configured to implement a 5-LUT and 3-LUT. The inputs to the two LUTs are independent of each other. The 3-LUT can be used to implement any logic function that has 3 or fewer inputs. Therefore, a 5-LUT/2-LUT combination is also available.
	One Stratix II ALM can be configured to implement a 5-LUT and a 4-LUT. One of the inputs is shared between the 2 LUTs. The 5-LUT has up to 4 independent inputs. The 4-LUT has up to 3 independent inputs. The sharing of inputs between LUTs is very common in FPGA designs, and the Quartus® II software automatically seeks logic functions that are structured in this manner.
	One Stratix II ALM can be configured to implement two 5-LUTs. Two of the inputs between the LUTs are common, and up to 3 independent inputs are allowed for each 5-LUT.
	If two 6-input functions have the same logic operation and 4 shared inputs, the two 6-input functions can be implemented in one Stratix II ALM. For example, a 4x2 crossbar switch with 4 data input lines and 2 sets of unique select signals requires four LEs in the Stratix family. In the Stratix II family, this function only requires one ALM. Another example is a 6-input AND gate. An ALM can implement two 6-input AND gates that have 4 common inputs. The same function would require 3 LEs if implemented in a Stratix device.
	One Stratix II ALM in the extended mode can implement a subset of a 7-variable function. The Quartus II sofware automatically recognizes the applicable 7-input function and fits it into an ALM. Refer to the *Stratix II Device Handbook* for detailed information about the types of 7-input functions that can be implemented in an ALM.

[14] *Id.* at p. 2.

66. The internal configuration control circuit of the LUTs in Intel's ALMs comprises a plurality of selectors selecting I/O signals of said plurality of LUT units:[15]



67. The internal configuration control circuit of the LUTs in Intel's ALMs also comprises a selector control circuit having a memory, controlling said plurality of selectors in accordance with data stored in said memory, and defining the internal configuration of said plurality of LUT units:[16]

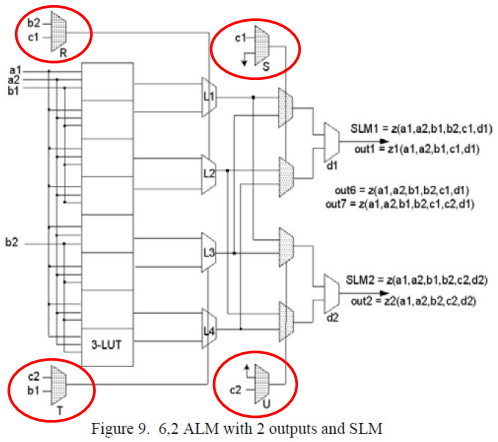


Figure 9. 6.2 ALM with 2 outputs and SLM

[15] *Id.* at p. 7.
[16] *Fracturable FPGA Logic Elements*, M. Hutton, et al. (2004) (attached as Exhibit 4) at p. 5.

68. The Accused Products infringe at least claim 1 of the ’737 patent.

69. Intel has been on actual notice of the ’737 patent, and of Professor Iida’s specific claims regarding Intel’s FPGA chips with ALMs, since at least February of 2018.

70. On February 19, 2018, counsel for Professor Iida sent a letter, via certified mail, to the General Counsel of Intel in which she advised him that her firm had become aware that Intel’s PSG “offers FPGAs with adaptive logic modules (ALMs) that appear to be claimed by our client’s US Patent No. 6,812,737 entitled ‘PROGRAMMABLE LOGIC CIRCUIT DEVICE HAVING LOOK UP TABLE ENABLING TO REDUCE IMPLEMENTATION AREA’ (enclosed).” A copy of this letter is attached as Exhibit 5.

71. Despite having been put on actual notice of the ’737 patent and of Professor Iida’s specific claims regarding Intel’s use of ALMs in its programmable logic devices, Intel nonetheless persisted in making, using, offering to sell, and selling the Accused Products.

72. Intel’s actual knowledge of the ’737 patent and of Professor Iida’s claims since February of 2018 has made its infringement of Professor Iida’s patent rights since that time deliberate and intentional.

73. Intel operates under a self-imposed Code of Conduct (the “Code”) which “applies to every employee, members of the Intel Board of Directors, and employees of Intel subsidiaries” as well as to “contingent workers, independent contractors, consultants, suppliers, and others who do business with Intel.”[17]

[17] Intel Code of Conduct at p. 6, Intel Website (last visited June 2022), available at: https://www.intel.com/content/www/us/en/policy/policy-code-conduct-corporate-information.html

74. The Code purports to exemplify Intel's "core values and its continuing commitment to corporate responsibility" by setting forth how its employees "work and win with integrity each day."[18]

75. According to the Code, all Intel employees are mandated to "respect the intellectual property rights of others."[19]

76. Intel has not respected the intellectual property rights of Professor Iida.

77. Professor Iida has been damaged by Intel's direct infringement of the '737 patent and is entitled to damages therefor as provided for in 35 U.S.C. § 284.

COUNT II – Indirect Infringement of '737 Patent

78. The allegations set forth above are re-alleged and incorporated by reference as if they were set forth fully here.

79. Intel's distributors and end customers directly infringe at least claim 1 of the '737 patent by offering for sale, selling, or using the Accused Products.

80. Intel has induced, and continues to induce, infringement of the '737 patent under 35 U.S.C. § 271(b) by actively and knowingly aiding and abetting direct infringement by its distributors and end customers.

81. Intel has been on actual notice of the '737 patent and of Professor Iida's claims with regard to the Accused Products since at least as early as February of 2018. *See* Exhibit 5.

82. Despite such actual notice, Intel has induced, and continues to induce, infringement of the '737 patent by actively encouraging others, including its distributors and end customers, to offer to sell, sell, or use the Accused Products. On information and belief, these

[18] *Id.* at p. 2.
[19] *Id.* at p. 14.

acts include providing the Accused Products to distributors; providing information and instructions to distributors and end customers on the use of the Accused Products; and providing information, education, and instructions supporting sales of the Accused Products by distributors. *See, e.g.*, roles and responsibilities of Intel employees as posted on their LinkedIn profile pages attached as Exhibit 2.

83. Professor Iida has been damaged by Intel's indirect infringement of the '737 patent and is entitled to damages therefor as provided for in 35 U.S.C. § 284.

JURY DEMAND

Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure, Professor Iida hereby requests a trial by jury on all issues so triable.

PRAYER FOR RELIEF

WHEREFORE, Professor Masahiro Iida respectfully requests that the Court grant the following relief:

A. A judgment in favor of Professor Iida that Intel has infringed the '737 patent, and that the '737 patent is valid and enforceable;

B. An award to Professor Iida of monetary damages adequate to compensate him for Intel's infringement but, in no event, less than a reasonable royalty for the use made of his invention by Intel, together with costs and pre- and post-judgment interest pursuant to 35 U.S.C. § 284;

C. An increase in the amount found by the jury and awarded to Professor Iida up to three times that amount for Intel's willful infringement pursuant to 35 U.S.C. § 284;

D. A finding that this case is exceptional under 35 U.S.C. § 285, and an award of Professor Iida's reasonable attorney's fees; and

E. Any other and further relief that the Court determines to be just and equitable.

Dated: June 24, 2022

Respectfully submitted,

Joshua R. Slavitt*
Pennsylvania State Bar No. 63139
SLAVITT IP LAW, LLC
535 Hamilton Road
Merion Station, PA 19066
Phone: (215) 880-2569
Email: josh@slavittiplaw.com

Travis C. Barton
Texas State Bar No. 00790276
Richard D. Milvenan
Texas State Bar No. 14171800
McGINNIS & LOCHRIDGE LLP
1111 W. 6th Street, Bldg. B, Suite 400
Austin, TX 78703
Phone: (512) 495-6005
Facsimile: (512) 505-6305
Email: tcbarton@mcginnislaw.com
Email: rmilvenan@mcginnislaw.com

By: /s/ *Travis C. Barton*

Jacob C. Cohn*
Pennsylvania State Bar No. 54139
Ilan Rosenberg*
Pennsylvania State Bar No. 89668
GORDON REES SCULLY MANSUKHANI LLP
1717 Arch Street, Suite 610
Philadelphia, PA 19103
Phone: (215) 561-2300
Email: jcohn@grsm.com
Email: irosenberg@grsm.com

**Pro hac vice to be filed*

Attorneys for Plaintiff,
Professor Masahiro Iida