

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

XUESHAN TECHNOLOGIES INC.,

Plaintiff,

v.

RENESAS ELECTRONICS
CORPORATION,

Defendant.

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CIVIL ACTION NO. 2:22-cv-00157

JURY TRIAL DEMANDED

PLAINTIFF’S FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Xueshan Technologies Inc. (“XTI”) files this First Amended Complaint against Defendant Renesas Electronics Corporation (“Renesas”) for infringement of U.S. Patent No. 7,038,695 (the “’695 Patent”); U.S. Patent No. 8,117,479 (the “’479 Patent”); U.S. Patent No. 8,643,659 (“the ’659 Patent”); and U.S. Patent No. 10,162,642 (the “’642 Patent), collectively, the “Asserted Patents.”

THE PARTIES

1. Xueshan Technologies Inc. is a Delaware corporation having a principal place of business in the Eastern District of Texas.
2. On information and belief, Renesas Electronics Corporation is a corporation organized under the laws of Japan, having a principal place of business at Toyosu Foresia, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan. Renesas is a leading manufacturer and seller of semiconductors, integrated circuits, microcontrollers (“MCUs”), microprocessors (“MPUs”), and System on a Chip products (“SoCs”) in the United States and the world, generally. Renesas conducts business in Texas and, particularly, the Eastern District of Texas, directly or through

intermediaries (including subsidiaries, distributors, affiliates, retailers, suppliers, integrators, customers, and others).

3. Renesas is engaged in making, using, selling, offering for sale, and/or importing products, such as semiconductors, integrated circuits, MCUs, MPUs, and SoCs, to and throughout the United States, including this District. Renesas also induces its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, and customers in the making, using, selling, offering for sale, and/or importing such products to and throughout the United States, including this District. To this end, Renesas and its foreign and U.S.-based subsidiaries—which act together as part of Renesas’ global network of sales and manufacturing emissaries—have operated as agents of, and for, one another and have otherwise acted vicariously for Renesas as elements of the same business group and/or enterprise. Indeed, they work in concert and in orchestrated fashion, subject to agreements that are far nearer than arm’s length, in order to implement a distribution channel of infringing products within this District and the United States.

4. Renesas maintains a substantial corporate presence in the United States via at least its U.S.-based sales subsidiaries, including Renesas Electronics America Inc. (“REA”). REA is a corporation organized under the laws of the State of California, having a principal place of business at 6024 Silver Creek Valley Road, San Jose, California 95138. REA is a wholly-owned subsidiary of Renesas. REA is responsible for Renesas’ domestic sales, offers for sale, importation, marketing, and support in North America. REA is Renesas’ agent, operating at Renesas’ direction and control. Subject to such direction and control, Renesas’ U.S.-based sales subsidiaries including, REA, import and sell infringing products, such as semiconductors, integrated circuits, MCUs, MPUs, and SoCs, in the United States and this District.

5. Alone and through at least the activities of its U.S.-based sales subsidiaries (e.g., REA), Renesas conducts business in the United States and this District, including importing, distributing, and selling semiconductors, integrated circuits, MCUs, MPUs, and SoCs that incorporate devices, systems, and processes that infringe the Asserted Patents. *See Trois v. Apple Tree Auction Center, Inc.*, 882 F.3d 485, 490 (5th Cir. 2018) (“A defendant may be subject to personal jurisdiction because of the activities of its agent within the forum state....”); *see also Cephalon, Inc. v. Watson Pharmaceuticals, Inc.*, 629 F. Supp. 2d 338, 348 (D. Del. 2009) (“The agency theory may be applied not only to parents and subsidiaries, but also to companies that are ‘two arms of the same business group,’ operate in concert with each other, and enter into agreements with each other that are nearer than arm’s length.”).

6. Through importation, offers to sell, sales, distributions, and related agreements to transfer ownership of Renesas’ products (e.g., semiconductors, integrated circuits, MCUs, MPUs, and SoCs) with distributors and customers operating in and maintaining significant business presences in the United States, Renesas conducts extensive business in the United States, this State, and this District.

JURISDICTION AND VENUE

7. This is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. §§ 1, *et seq.* This Court has jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and 1338(a) and 1367.

8. This Court has specific and personal jurisdiction over Renesas consistent with the requirements of the Due Process Clause of the United States Constitution and the Texas Long Arm Statute because, among other things: (i) Renesas has done and continues to do business in Texas; and (ii) Renesas has committed and continues to commit, directly or through intermediaries

(including subsidiaries, distributors, affiliates, retailers, suppliers, integrators, customers, and others), acts of patent infringement in this State. Such acts of infringement include making, using, offering to sell, and/or selling Accused Products (as more particularly identified and described throughout this First Amended Complaint) in this State and this District and/or importing Accused Products into this State and/or inducing others to commit acts of patent infringement in this State. Indeed, Renesas has purposefully and voluntarily placed, and is continuing to place, one or more Accused Products into the stream of commerce through established distribution channels (including the Internet) with the expectation and intent that such products will be sold to and purchased by consumers in the United States, this State, and this District; and with the knowledge and expectation that such products (whether in standalone form or as integrated in downstream products) will be imported into the United States, this State, and this District.

9. Renesas has derived substantial revenues from its infringing acts occurring within this State and this District. It has substantial business in this State and this District, including: (i) at least part of its infringing activities alleged herein; and (ii) regularly doing or soliciting business, engaging in other persistent conduct, and/or deriving substantial revenue from infringing goods offered for sale, sold, and imported, and services provided to Texas residents vicariously through and/or in concert with its alter egos, intermediaries, agents, distributors, importers, customers, subsidiaries, and/or consumers.

10. This Court has personal jurisdiction over Renesas, directly or through intermediaries (e.g., subsidiaries, distributors, affiliates, retailers, suppliers, integrators, customers, and others), including its U.S.-based sales subsidiaries, e.g., REA. Through direction and control of such subsidiaries, Renesas has committed acts of direct and/or indirect patent infringement within this State and elsewhere within the United States giving rise to this action and/or has

established minimum contacts with this forum such that the exercise of personal jurisdiction over Renesas would not offend traditional notions of fair play and substantial justice. REA is a wholly-owned subsidiary of Renesas. The primary business of REA is the marketing, support, and sale of Renesas' electronic products in the United States. Upon information and belief, Renesas compensates REA for marketing, support, and sales services in the United States. As such, Renesas has a direct financial interest in its U.S.-based subsidiaries, and vice versa.

11. Renesas controls and otherwise directs and authorizes all activities of its U.S.-based sales subsidiaries, including REA. Such directed and authorized activities include the U.S.-based subsidiaries using, offering for sale, selling, and/or importing the Accused Products, their components, and/or products containing the same that incorporate and/or perform the fundamental technologies covered by the Asserted Patents. Renesas' U.S.-based sales subsidiaries, including REA, are expressly authorized to import, distribute, offer to sell, and sell the Accused Products on behalf of Renesas. For example, Renesas researches, designs, develops, and manufactures semiconductors, integrated circuits, MCUs, MPUs, and SoCs, and then directs its U.S.-based sales subsidiaries to import, distribute, offer for sale, and sell the Accused Products in the United States. *See, e.g., United States v. Hui Hsiung*, 778 F.3d 738, 743 (9th Cir. 2015) (finding that the sale of infringing products to third parties rather than for direct import into the U.S. did not “place [defendants’] conduct beyond the reach of United States law [or] escape culpability under the rubric of extraterritoriality”). Renesas' U.S.-based sales subsidiaries also provide, on Renesas' behalf, marketing and technical support services for the Accused Products from their facilities in the United States. For example, REA helps maintain a website that advertises the Accused Products, including identifying the applications for which they can be used and providing related specifications. *See, e.g.,* <https://www.renesas.com/us/en/>. The referenced website also contains

user manuals, product documentation, and other materials related to Renesas' products. For example, the website includes: (i) reference designs (<https://www.renesas.com/us/en/products/software-tools/boards-and-kits/reference-designs.html>) spanning analog products, power management products, and microprocessor and microcontrollers; (ii) complimentary design review services such as EDA schematic symbols, PCB footprints, and simulation models in industry-standard formats to help shorten development time (<https://www.renesas.com/us/en/support/technical-resources/eda-data.html>); (iii) robust customer support through REA's online support platforms including REA's Synergy Platform (<https://www.renesas.com/us/en/support/contact.html>); and (iv) REA's Knowledgebase (<https://en-support.renesas.com/knowledgeBase>). Thus, Renesas' U.S.-based sales subsidiaries, including REA, conduct infringing activities on Renesas' behalf.

12. On information and belief, because Renesas' U.S.-based sales subsidiaries are authorized by Renesas to import, distribute, offer to sell, and sell Accused Products and/or to perform the fundamental technologies covered by the Asserted Patents, Renesas' U.S.-based sales subsidiaries' corporate presences in the United States give Renesas substantially the same business advantages it would enjoy if it conducted its business through its own offices and personnel.

13. In addition, Renesas has knowingly induced, and continues to knowingly induce, infringement within this District by advertising, marketing, offering for sale and/or selling Accused Products (such as semiconductors, integrated circuits, MCUs, MPUs, and SoCs) that incorporate the fundamental technologies covered by the Asserted Patents. Such advertising, marketing, offering for sale and/or selling of Accused Products is directed to manufacturers, integrators, suppliers, distributors, resellers, partners, consumers, customers, and/or end users, and this includes providing instructions, user manuals, advertising, and/or marketing materials

facilitating, directing and encouraging use of infringing functionality with Renesas' knowledge thereof.

14. Renesas has, thus, in the multitude of ways described above, availed itself of the benefits and privileges of conducting business in this State and willingly subjected itself to the exercise of this Court's personal jurisdiction. Indeed, Renesas has sufficient minimum contacts with this forum through its transaction of substantial business in this State and this District and its commission of acts of patent infringement as alleged in this First Amended Complaint that are purposefully directed towards this State and District.

15. Alternatively, the Court maintains personal jurisdiction over Renesas under Federal Rule of Civil Procedure 4(k)(2).

16. Venue is proper in this District pursuant to 28 U.S.C. § 1391 because, among other things, Renesas is not a resident of the United States, and thus may be sued in any judicial district, including this one, pursuant to 28 U.S.C. § 1391(c)(3). *See In re HTC Corp.*, 889 F.3d 1349, 1357 (Fed. Cir. 2018) (holding that "[t]he Court's recent decision in *TC Heartland* does not alter" the alien-venue rule).

THE PATENTS-IN-SUIT

17. XTI is the sole and exclusive owner of all right, title, and interest in the '695 Patent, the '479 Patent, the '659 Patent, and the '642 Patent and holds the exclusive right to take all actions necessary to enforce its rights in, and to, the Asserted Patents, including the filing of this patent infringement lawsuit. XTI also has the right to recover all damages for past, present, and future infringements of the Asserted Patents and to seek injunctive relief as appropriate under the law.

18. The '695 Patent is entitled, "User interface display apparatus using texture mapping method." The '695 Patent lawfully issued on May 2, 2006 and stems from U.S. Patent Application No. 10/812,173, which was filed on March 30, 2004.

19. The '479 Patent is entitled, "Electronic apparatus and auto wake-up circuit thereof." The '479 Patent lawfully issued on February 14, 2012 and stems from U.S. Patent Application No. 12/402,698, which was filed on March 12, 2009.

20. The '659 Patent is entitled, "Shader with global and instruction caches." The '659 Patent lawfully issued on February 4, 2014 and stems from U.S. Patent Application No. 10/958,758, which was filed on October 5, 2004.

21. The '642 Patent is entitled, "Shader with global and instruction caches." The '642 Patent lawfully issued on December 25, 2018 and stems from U.S. Patent Application No. 14/172,839, which was filed on February 4, 2014.

22. XTI and its predecessors complied with the requirements of 35 U.S.C. § 287, to the extent necessary, such that XTI may recover pre-suit damages.

23. The claims of the patents-in-suit are directed to patent eligible subject matter under 35 U.S.C. § 101. They are not directed to an abstract idea, and the technologies covered by the claims comprise systems and/or consist of ordered combinations of features and functions that, at the time of invention, were not, alone or in combination, well-understood, routine, or conventional.

DEFENDANT'S PRE-SUIT KNOWLEDGE OF ITS INFRINGEMENT

24. Prior to the filing of the Original Complaint, XTI repeatedly attempted to engage Renesas and/or its agents in licensing discussions related to the Asserted Patents:

- a) On March 25, 2021, XTI sent its first letter to Renesas headquarters addressed to Mr. Jason Hall (Renesas's Senior Vice President and CLO) to initiate patent licensing discussions. The letter identified certain Asserted Patents as being infringed by exemplary Renesas products, and further included claim charts

demonstrating how the identified products infringe the '659 and '642 Patents. The letter identified the following exemplary Renesas products as infringing:

Patent Infringed	Exemplary Products
'659 Patent	<ul style="list-style-type: none"> • Renesas R Car SoCs (including R-Car M3, R-Car H3, R-Car H2, R-Car D3, R-Car E2, R-Car V3U, R-Car M2, R-Car E2, R-Car V2H & R-Car D1); and • Renesas RZ MPU's (including RZ/G1H, RZ/G2E, RZ/G2H, RZ/G2M, RZ/G2N, RZ/G1C, RZ/G1E, RZ/G1M & RZ/G1N).
'642 Patent	<ul style="list-style-type: none"> • Renesas R Car SoCs (including R-Car M3, R-Car H3, R-Car H2, R-Car D3, R-Car E3, R-Car V3U, R-Car M2, R-Car E2, R-Car V2H & R-Car D1); and • Renesas RZ MPUs (including RZ/G1H, RZ/G2E, RZ/G2H, RZ/G2M, RZ/G2N, RZ/G1C, RZ/G1E, RZ/G1M & RZ/G1N).

- b) On May 20, 2021, XTI sent its second letter to Renesas headquarters addressed to Mr. Jason Hall (Renesas's Senior Vice President and CLO) to follow up on the initial letter since no response was received. The second letter further identified additional patents (including the '695 Patent) as being infringed by exemplary Renesas products. The letter included claim charts demonstrating how the identified Renesas products infringe the '695 Patent. The letter identified the following exemplary Renesas products as infringing:

Patent Infringed	Exemplary Products
'695 Patent	<ul style="list-style-type: none"> • Renesas Synergy MCUs S5 Series; and • Renesas Synergy MCUs S7 Series.

- c) On February 28, 2022, XTI sent a third letter to Renesas headquarters addressed to Mr. Jason Hall (Renesas's Senior Vice President and CLO) to follow up on XTI's first two letters since no responses were received. The letter identified additional

patents (including the '479 Patent) as being infringed by exemplary Renesas products. The letter included claim charts demonstrating how Renesas' products infringe the '479 Patent. The letter identified the following exemplary Renesas product as infringing:

Patent Infringed	Exemplary Products
'479 Patent	• Renesas RL78 MCU Family

25. Renesas ignored all attempts by XTI to communicate and open a licensing dialogue. As a result, XTI was left with no other choice but to seek relief through patent enforcement litigation.

26. The Accused Products include, but are not limited to, the exemplary products identified in XTI's letters to Renesas, and Renesas' past and continuing sales of the Accused Products: (i) willfully infringe the Asserted Patents; and (ii) impermissibly usurp the significant benefits of XTI's patented technologies without fairly compensating XTI.

COUNT I

(INFRINGEMENT OF U.S. PATENT NO. 7,038,695)

27. Plaintiff incorporates the preceding paragraphs herein by reference.

28. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq.*

29. XTI is the owner of all substantial rights, title, and interest in and to the '695 Patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

30. The '695 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on May 2, 2006, after full and fair examination.

31. Renesas has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the '695 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, Renesas products, their components and processes, and/or products containing the same that incorporate the fundamental technologies covered by the '695 Patent, including, but not limited to, the Renesas Synergy S5 Series MCUs and the Renesas Synergy S7 Series MCUs (collectively, the "'695 Accused Products").

Direct Infringement (35 U.S.C. § 271(a))

32. Renesas has directly infringed and continues to directly infringe one or more claims of the '695 Patent in this District and elsewhere in Texas and the United States.

33. Renesas has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 1 of the '695 Patent¹ as set forth under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing the '695 Accused Products. Furthermore, Renesas makes and sells the '695 Accused Products outside of the United States and either delivers those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivers the '695 Accused Products outside of the United States, it does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the '695 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013). Furthermore, Renesas directly infringes the '695 Patent through its direct involvements in, and

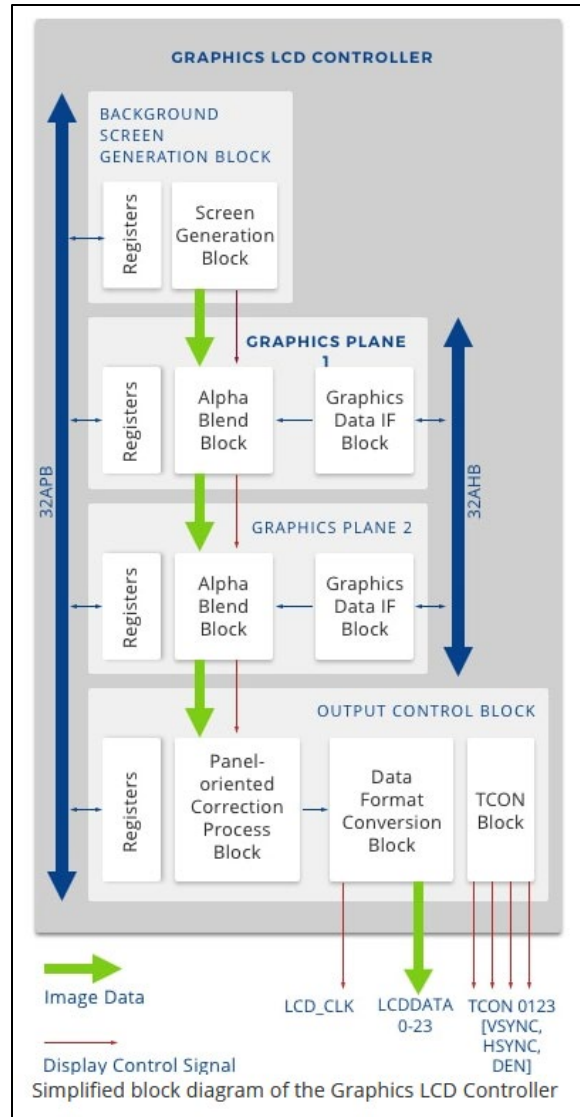
¹ Throughout this First Amended Complaint, wherever XTI identifies specific claims of the Asserted Patents infringed by Renesas, XTI expressly reserves the right to identify additional claims and products in its infringement contentions in accordance with applicable local rules and the Court's case management order. Specifically identified claims throughout this First Amended Complaint are provided for notice pleading only.

control of, the activities of its subsidiaries, including REA. Subject to Renesas' direction and control, such subsidiaries conduct activities that constitute direct infringement of the '695 Patent under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing '695 Accused Products. Renesas receives direct financial benefit from such infringements of its U.S.-based sales subsidiaries, including REA.

34. By way of illustration only, the '695 Accused Products include each and every element of claim 1 of the '695 Patent. The '695 Accused Products include “a user interface display apparatus.” For example, the '695 Accused Products include a “Graphics LCD Controller (‘GLCDC’)” component that is configured to “[d]rive[] a variety of color TFT LCD screens using the standard RGB and control signals.”² Specifically, “[t]he GLCDC outputs image data in either serial or parallel format, up to 24 bits. It can be used to superimpose two drawing planes and one background plane, and to perform enhancements such as alpha-blending, dither correction, brightness and contrast correction, and gamma correction,”³ as demonstrated by the block diagram of the Graphics LCD Controller below:

² See <https://www.renesas.com/us/en/products/microcontrollers-microprocessors/renesas-synergy-platform-mcus/components-synergy-mcus> (last visited March 28, 2022).

³ *Id.*



“Components of Synergy MCUs”⁴

35. The '695 Accused Products include “an image module unit for providing image patterns.” For example, the S5D9 Microcontroller Group User’s Manual provides that the Graphics LCD Controller (“GLCDC”) of the S5D9 Microcontroller further includes a “Graphics data IF block” [image module unit for providing image patterns] that is configured to “[c]onvert the graphics data/CLUT data read through the GPX bus into ARGB (8888) data for internal

⁴ *Id.*

processing, and transfer[ing] the clocks (PCLKA → PXCLK),”⁵ as demonstrated by the GLCDC block diagram below:

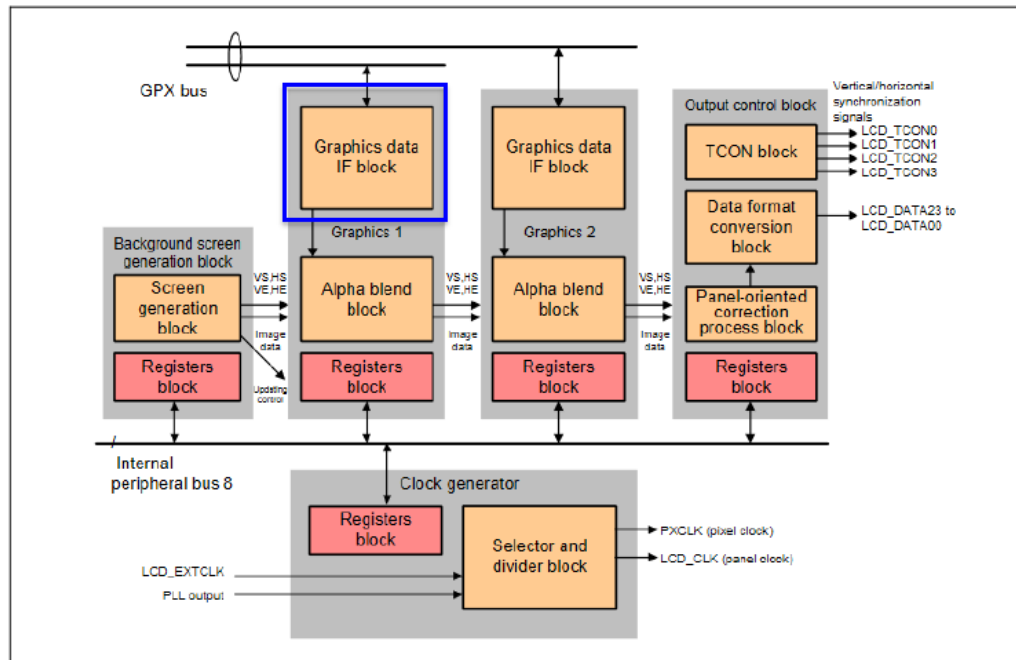


Figure 58.1—S5D9 Microcontroller Group User’s Manual, at p. 1948 (emphasis added).⁶

36. The '695 Accused Products include “a texture pattern unit for providing texture patterns.” For example, the S5D9 Microcontroller Group User’s Manual provides that the Graphics LCD Controller (“GLCDC”) of the S5D9 Microcontroller further includes a “Background screen generation block” [texture pattern unit for providing texture patterns] that is configured to “[g]enerat[e] the background screen (including the blanking interval), select[ing] the background color, and generat[ing] the synchronization signals for controlling the screens,”⁷ as demonstrated by the GLCDC block diagram below:

⁵ See <https://www.renesas.com/us/en/document/mah/s5d9-microcontroller-group-users-manual?r=1054626> (last visited March 28, 2022), at 1950.

⁶ *Id.* at 1948.

⁷ *Id.*

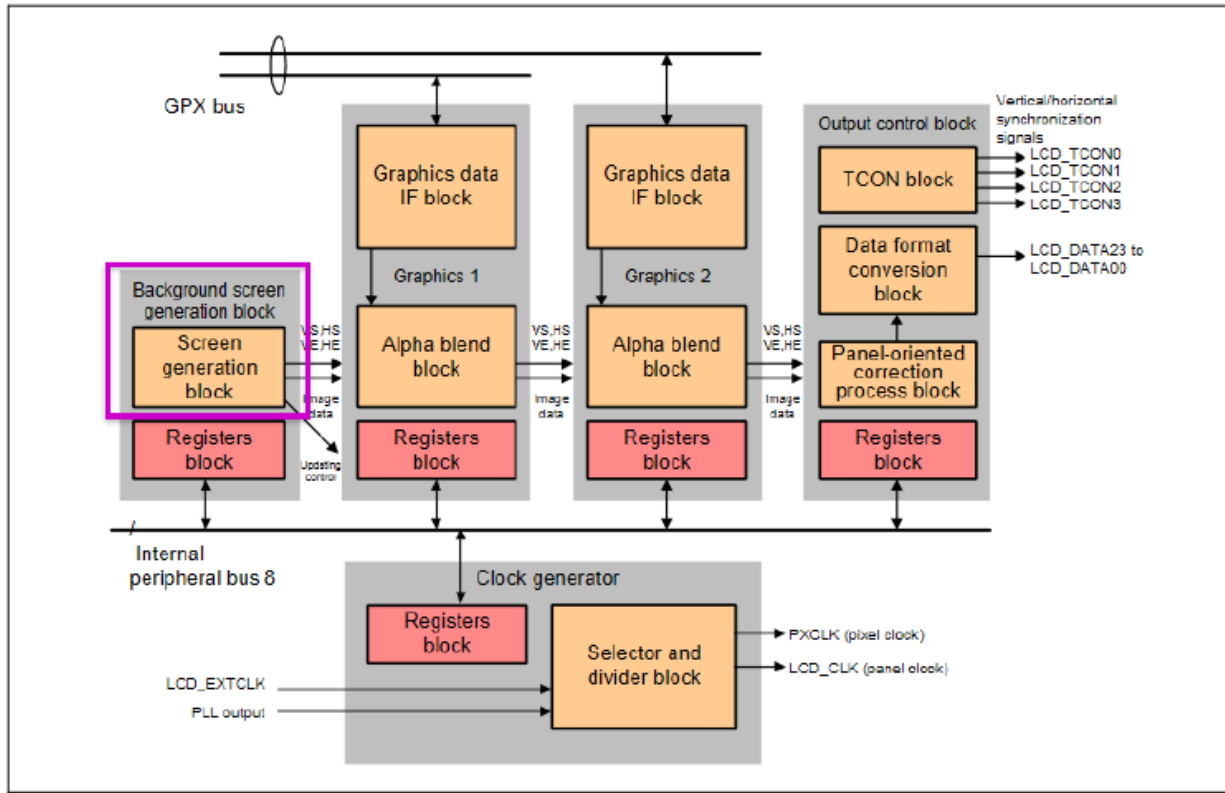


Figure 58.1—S5D9 Microcontroller Group User’s Manual, at p. 1948 (emphasis added).⁸

37. The '695 Accused Products include “a display code-buffer unit for arranging pattern codes which are associated with the image patterns and texture patterns to be displayed on a user interface display window.” For example, the S5D9 Microcontroller Group User’s Manual provides that the Graphics LCD Controller (“GLCDC”) of the S5D9 Microcontroller further includes a “Registers block” [display code-buffer unit for arranging pattern codes], as demonstrated by the GLCDC block diagram below:

⁸ *Id.*

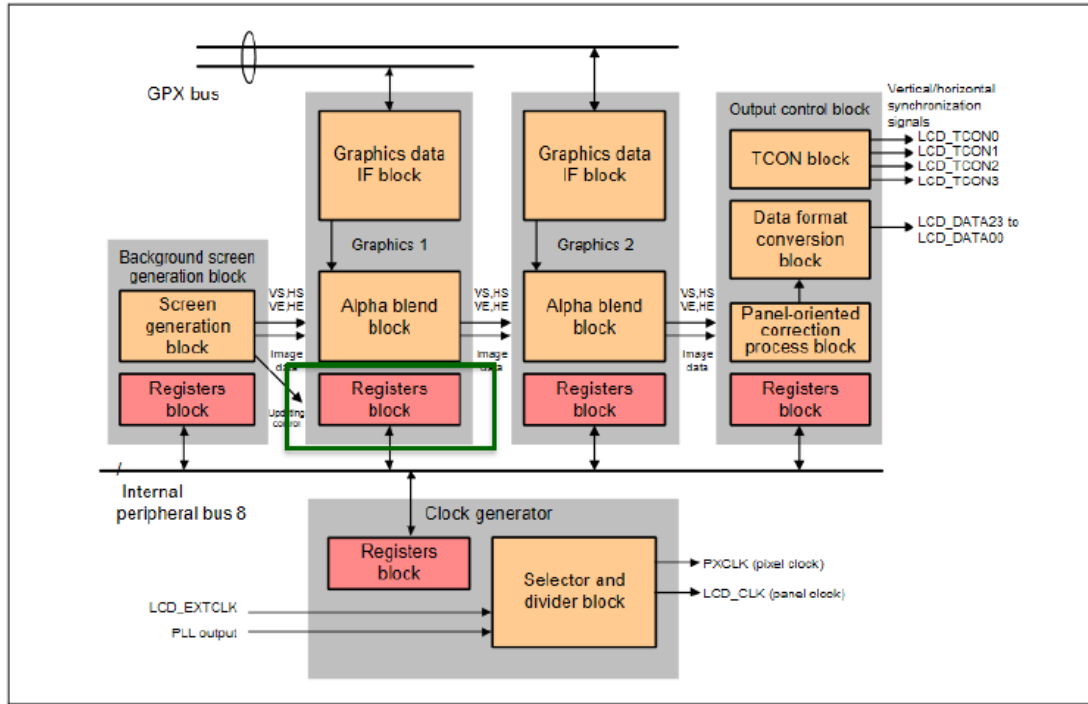


Figure 58.1—S5D9 Microcontroller Group User’s Manual, at p. 1948 (emphasis added).⁹

58.2.16 Graphics 1 Alpha Blending Control Register 1 (GR1_AB1)
Graphics 2 Alpha Blending Control Register 1 (GR2_AB1)

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	ARCO N	—	—	—	ARCDI SPON	—	—	—	GRCDI SPON	—	—	DISPSEL[1:0]	—
Value after reset: 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0															

Bit	Symbol	Bit name	Description	R/W															
b1, b0	DISPSEL[1:0]	Graphics Display Plane Control	<table border="0"> <tr> <td>b1</td> <td>b0</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>Background color display (value set in the GR_n_BASE register)</td> </tr> <tr> <td>0</td> <td>1</td> <td>Lower-layer graphics display</td> </tr> <tr> <td>1</td> <td>0</td> <td>Current graphics display</td> </tr> <tr> <td>1</td> <td>1</td> <td>Blended display of lower-layer graphics (input image from the previous stage) and current graphics (data read from the GPX bus).</td> </tr> </table>	b1	b0		0	0	Background color display (value set in the GR _n _BASE register)	0	1	Lower-layer graphics display	1	0	Current graphics display	1	1	Blended display of lower-layer graphics (input image from the previous stage) and current graphics (data read from the GPX bus).	R/W
b1	b0																		
0	0	Background color display (value set in the GR _n _BASE register)																	
0	1	Lower-layer graphics display																	
1	0	Current graphics display																	
1	1	Blended display of lower-layer graphics (input image from the previous stage) and current graphics (data read from the GPX bus).																	

DISPSEL[1:0] bits (Graphics Display Plane Control)

The DISPSEL[1:0] bits control the graphics display plane. When the plane is selected as the lower-layer graphics, the image input from the previous stage is displayed (the background plane for GR1, and output from GR1 for GR2); as the background color, the background color specified in the GLCDC registers is displayed; and as the current graphics, the ARGB8888 data obtained by expanding the graphics data read by the GLCDC from the GPX bus is displayed. When the current graphics display is selected (these bits are set to 10b), RGB888 data is displayed, regardless of the alpha blending value in the pixel. Table 58.8 and Figure 58.10 show the relationship between the register setting and display area.

S5D9 Microcontroller Group User’s Manual, at p. 1975 (emphasis added).¹⁰

⁹ *Id.*

¹⁰ *Id.* at 1975.

38. The '695 Accused Products include “a mixer unit for mixing the image patterns and the texture patterns, and output a mixed signal.” For example, the S5D9 Microcontroller Group User’s Manual provides that the Graphics LCD Controller (“GLCDC”) of the S5D9 Microcontroller further includes a “Alpha blend block” [mixer unit] that is configured to “[s]uperimpose graphics data on the lower-layer screen [texture patterns] and perform alpha blending based on the register settings and the alpha blending values for the current screen graphics data [image patterns],”¹¹ as demonstrated by the GLCDC block diagram below:

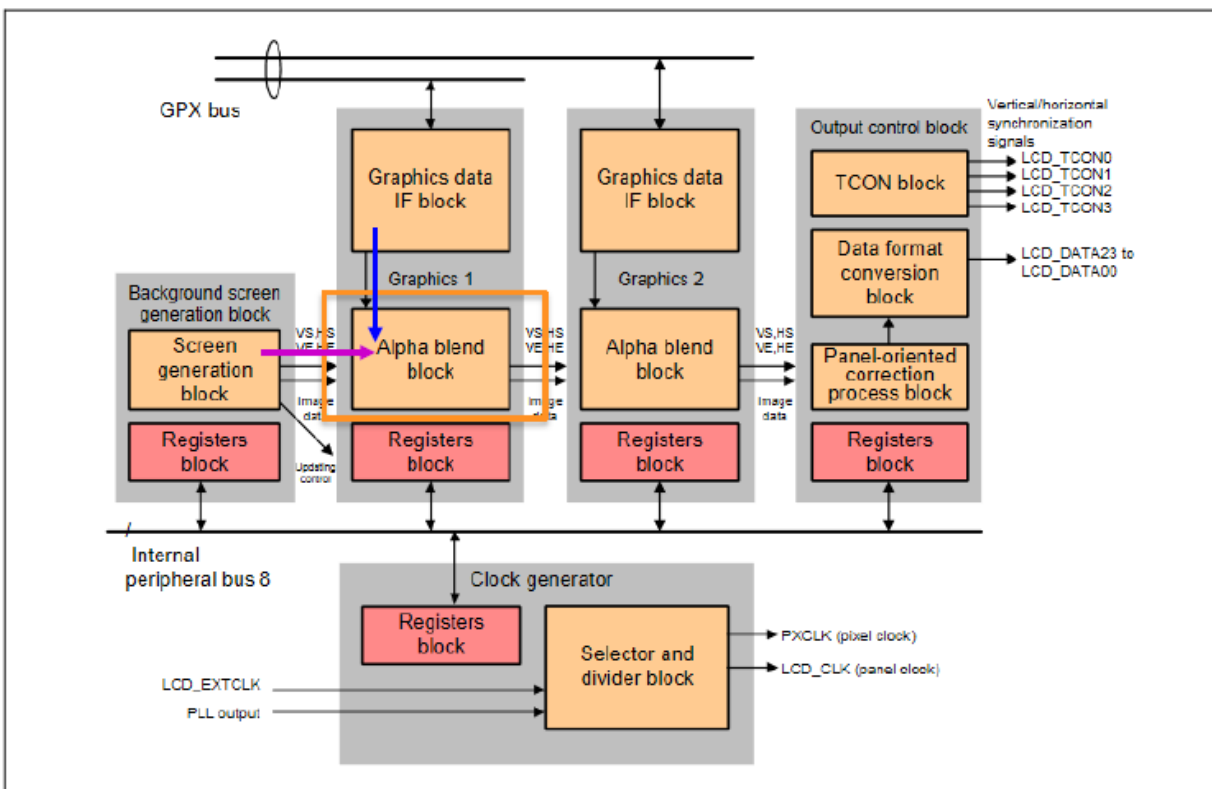


Figure 58.1—S5D9 Microcontroller Group User’s Manual, at p. 1948 (emphasis added).¹²

39. The '695 Accused Products satisfy the requirement that “wherein the mixer unit uses an alpha blending method, where $output = (pattern \text{ from said image module}$

¹¹ *Id.* at 1950.

¹² *Id.* at 1948.

unit) \times alpha+(pattern from said texture pattern unit) \times (1-alpha), and wherein the parameter alpha is a real number between 0 and 1.” For example, the S5D9 Microcontroller Group User’s Manual further provides the specific formula for its alpha blending—performed by the “Alpha blend block” [mixer unit]—of current graphics data [image patterns] and lower-layer graphics data [texture patterns]:

58.1.8 Blending

Alpha blending is based on the following formulas:

When A value = 255
Rout/Gout/Bout = current graphics data

When A value \neq 255

$$\text{Rout} = (\text{Rin1} \times A + \text{Rin0} \times (256 - A))/256$$

$$\text{Gout} = (\text{Gin1} \times A + \text{Gin0} \times (256 - A))/256$$

$$\text{Bout} = (\text{Bin1} \times A + \text{Bin0} \times (256 - A))/256$$

where,

A: alpha blending value
Rin1/Gin1/Bin1: current graphics data
Rin0/Gin0/Bin0: lower-layer graphics data

S5D9 Microcontroller Group User’s Manual, at p. 1961 (emphasis added).¹³

Indirect Infringement (Inducement – 35 U.S.C. § 271(b))

40. In addition and/or in the alternative to its direct infringements, Renesas has indirectly infringed and continues to indirectly infringe one or more claims of the ’695 Patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the ’695 Accused Products.

¹³ *Id.* at 1961.

41. At a minimum, Renesas has knowledge of the '695 Patent since being served with the Original Complaint and this First Amended Complaint. Renesas also has knowledge of the '695 Patent since receiving detailed correspondence from XTI dated May 20, 2021, alerting Renesas to its infringements. Since receiving notice of its infringements, Renesas has actively induced the direct infringements of its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Such inducements have been committed with the knowledge, or with willful blindness to the fact, that the acts induced constitute infringement of the '695 Patent. Indeed, Renesas has intended to cause, continues to intend to cause, and has taken, and continues to take, affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the '695 Accused Products;¹⁴ creating and/or maintaining established distribution channels for the '695 Accused Products into and within the United States; manufacturing the '695 Accused Products in conformity with U.S. laws and regulations; distributing or making available datasheets supporting use of the '695 Accused Products that promote their features, specifications, and applications;¹⁵ providing technical documentation and tools for the '695 Accused Products, including white papers, brochures, and

¹⁴ See, e.g., <https://www.renesas.com/us/en/products/microcontrollers-microprocessors/renesas-synergy-platform-mcus>; <https://www.renesas.com/us/en/products/microcontrollers-microprocessors/renesas-synergy-platform-mcus/s5d9-120-mhz-arm-cortex-m4-cpu>; <https://www.renesas.com/us/en/products/microcontrollers-microprocessors/renesas-synergy-platform-mcus/s7g2-240-mhz-arm-cortex-m4-cpu> (last visited March 28, 2022).

¹⁵ See, e.g., S5D9 Microcontroller Group Datasheet (2019), available at <https://www.renesas.com/us/en/document/dst/s5d9-microcontroller-group-datasheet-r01ds0303eu0130?language=en&r=1054626> (last visited March 28, 2022); S7G2 Microcontroller Group Datasheet (2018), available at <https://www.renesas.com/us/en/document/dst/s7g2-microcontroller-group-datasheet?Language=en&r=1054631> (last visited March 28, 2022).

manuals;¹⁶ promoting the incorporation of the '695 Accused Products into end-user products through the development of Renesas' Partner programs,¹⁷ complimentary design review services,¹⁸ automated utilities, calculators, and reference designs;¹⁹ testing and certifying features related to alpha blending in the '695 Accused Products;²⁰ and by providing technical support and/or related services for these products to purchasers in the United States through Renesas' online support platforms including RenesasRulz forum²¹ and Renesas Synergy Platform²² further explaining how to use Renesas' products.

Damages

42. On information and belief, despite having knowledge of the '695 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the '695 Patent, Renesas has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. Renesas' infringing activities relative to the '695 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant,

¹⁶ See, e.g., S7G2 Microcontroller Group User's Manual (2018), available at <https://www.renesas.com/us/en/document/man/s7g2-microcontroller-group-users-manual?language=en&r=1054631> (last visited March 28, 2022).

¹⁷ See <https://www.renesas.com/us/en/support/partners/preferred-partners> (last visited March 28, 2022).

¹⁸ See <https://www.renesas.com/us/en/support/clock-tree-design-service> (last visited March 28, 2022).

¹⁹ See, e.g., <https://www.renesas.com/us/en> (including Renesas' iSim:PE Offline Simulation Tool, Jitter Measurement Utility, Lab on the Cloud, PowerCompass Multi-Rail Design Tool, PowerNavigator; Timing Commander, and X-Microwave Modular Blocks) (last visited March 28, 2022).

²⁰ See, e.g., Renesas Electronics Quality Assurance System pp. 9-17 (2022), available at <https://www.renesas.com/us/en/document/ppt/renesas-electronics-quality-assurance-system?Language=en> (last visited March 28, 2022).

²¹ See <https://renesasrulz.com/> (last visited March 28, 2022).

²² See Renesas Synergy Platform Brochure, available at <https://www.renesas.com/us/en/document/bro/renesas-synergy-platform-brochure> (last visited March 28, 2022).

characteristic of a pirate, and an egregious case of misconduct beyond typical infringement such that XTI is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

43. XTI has been damaged as a result of Renesas' infringing conduct described in this Count. Renesas is, thus, liable to XTI in an amount that adequately compensates XTI for Renesas' infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

COUNT II

(INFRINGEMENT OF U.S. PATENT NO. 8,117,479)

44. Plaintiff incorporates the preceding paragraphs herein by reference.

45. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq.*

46. XTI is the owner of all substantial rights, title, and interest in and to the '479 Patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

47. The '479 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on February 14, 2012, after full and fair examination.

48. Renesas has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the '479 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, Renesas products, their components and processes, and/or products containing the same that incorporate the fundamental technologies covered by the '479 Patent, including, but not limited to, the Renesas RL78 MCU family (collectively, the "'479 Accused Products").

Direct Infringement (35 U.S.C. § 271(a))

49. Renesas has directly infringed and continues to directly infringe one or more claims of the '479 Patent in this District and elsewhere in Texas and the United States.

50. Renesas has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 1 of the '479 Patent as set forth under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing the '479 Accused Products. Furthermore, Renesas makes and sells the '479 Accused Products outside of the United States and either delivers those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivers the '479 Accused Products outside of the United States, it does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the '479 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013). Furthermore, Renesas directly infringes the '479 Patent through its direct involvements in, and control of, the activities of its subsidiaries, including REA. Subject to Renesas' direction and control, such subsidiaries conduct activities that constitute direct infringement of the '479 Patent under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing '479 Accused Products. Renesas receives direct financial benefit from such infringements of its U.S.-based sales subsidiaries, including REA.

51. By way of illustration only, the '479 Accused Products include each and every element of claim 1 of the '479 Patent.

52. The '479 Accused Products are a family of microcontrollers that employ features, such as the Renesas Snooze function. For example, the Renesas Snooze function allows the power

consumption of many typical MCU functions to be dramatically reduced by allowing common data acquisition or data transmission functions to operate without the need to wake-up the CPU.

53. To minimize power usage and consumption during intermittent operation, the '479 Accused Products are configured to implement three low power modes – “Halt,” “Stop,” and “Snooze,” as demonstrated below:

LOW POWER CONSUMPTION

SNOOZE mode for more power savings

In SNOOZE mode the CPU is halted while A/D conversion and data reception are enabled. By transitioning from STOP mode (clock stopped) to SNOOZE mode, it is possible to start the on-chip oscillator and operate peripheral functions while the CPU remains inactive.

SNOOZE mode

- It is not necessary to activate the CPU for data reception.
- Using the exclusive SNOOZE mode, peripheral functions such as the ADC, UART or CSI can operate when CPU is in standby mode.
- Power consumption is one-tenth of normal operation.
SNOOZE mode: 0.5 mA, RUN mode (ADC): 5 mA

HALT and STOP modes

- The standby function stops CPU operation, reducing overall microcontroller current consumption by 80%.
- The STOP mode disables the microcontroller’s on-chip functions, reducing power consumption to the lowest level possible.

Brochure of RL78 Family Microcontrollers at p. 2 (2021).²³

54. The '479 Accused Products are configured to transition from Normal Operation to Stop mode when a Stop instruction is executed via the MCU.²⁴ The '479 Accused Products are

²³ See <https://www.renesas.com/us/en/document/fly/rl78-family-microcontrollers-brochure?language=en&r=469291> (last visited March 28, 2022), at 2.

²⁴ See <https://www.renesas.com/us/en/document/apn/rl78f13-f14-standby-function-rev100?language=en> (last visited March 28, 2022), at 6-8.

configured such that when they enter a sleep mode (e.g., STOP mode), a control signal is generated to set the serial standby control register m (SSCm) (SNOOZE mode setting).

55. The '479 Accused Products are further configured such that in Stop mode, the high-speed system clock oscillator and internal high-speed oscillator are disabled.²⁵ While in Stop Mode, the serial standby control register 0 (SSC0) is configured to control the startup of reception (the Snooze Mode) when receiving CSI00 or UART0 serial data. For example, the SWCm bit of serial standby control register m (SSCm) is set to 1 immediately before switching to the STOP mode, as demonstrated below.²⁶

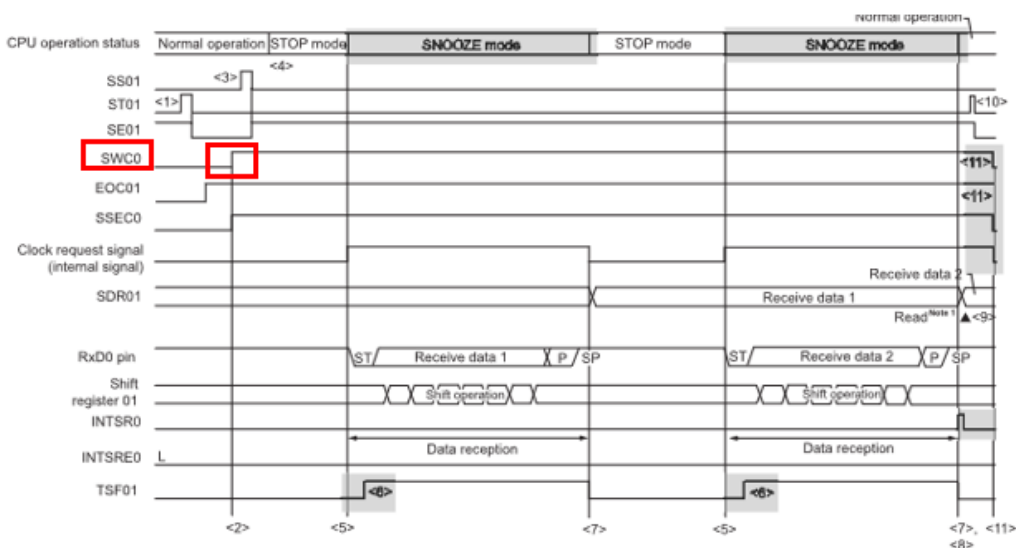


Figure 14-93. Renesas Technical Update at 9 (emphasis added).²⁷

56. The '479 Accused Products are further configured such that when a start trigger for the peripheral function is generated by an auxiliary module in Stop mode, the high-speed on-chip

²⁵ *Id.*

²⁶ See <https://www.renesas.com/us/en/document/mah/rl78f12-users-manual-hardware-rev111?r=1054251> (last visited March 28, 2022), at 478.

²⁷ See <https://www.renesas.com/us/en/document/tcu/correction-incorrect-description-notice-rl78l13?language=en> (last visited April 4, 2022), at 9.

oscillator starts oscillating and the MCU transitions from Stop mode to Snooze mode.²⁸ For example, while the MCU is in Stop mode, a change in the pin input (e.g., RxDn and SCKp pin inputs) will trigger a transition from Stop mode to Snooze mode, as demonstrated below:²⁹

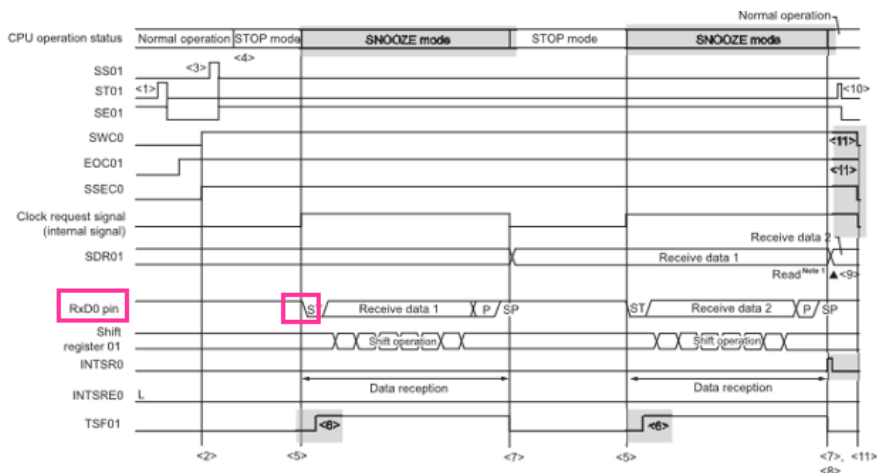


Figure 14-93. Renesas Technical Update at 9 (emphasis added).³⁰

57. The '479 Accused Products are further configured such that while the MCU is in Snooze mode, the clock request signal (internal signal) allows data reception from the synchronous or UART serial port, or a data conversion by the A/D converter to continue to operate, as demonstrated below:

²⁸ See <https://www.renesas.com/us/en/document/apn/rl78f13-f14-standby-function-rev100?language=en> (last visited March 28, 2022), at 10-11.

²⁹ See <https://www.renesas.com/us/en/document/mah/rl78f12-users-manual-hardware-rev111?r=1054251> (last visited March 28, 2022), at 566, 597.

³⁰ See <https://www.renesas.com/us/en/document/tcu/correction-incorrect-description-notice-rl78l13?language=en> (last visited April 4, 2022), at 9.

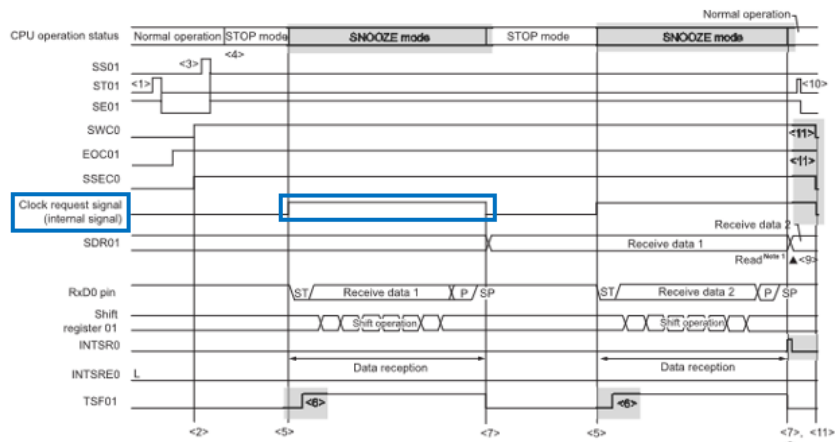


Figure 14-93. Renesas Technical Update at 9 (emphasis added).³¹

58. The '479 Accused Products comprise “an electronic apparatus.” For example, the '479 Accused Products are each a microcontroller containing electronic circuits.

59. The '479 Accused Products include “a main module, for performing a main function of the electronic apparatus, and generating a first control signal when the electronic apparatus enters a sleep mode.” For example, the '479 Accused Products include first circuitry and/or firmware (which may comprise the CPU) that are configured to provide functionality, such as data processing, in Normal Operation and to generate a control signal setting the serial standby control register m (SSCm).

60. The '479 Accused Products are configured to generate this signal when the '479 Accused Products enter Stop mode.³² For example, the SWCm bit of serial standby control register m (SSCm) is set to 1 immediately before switching to the STOP mode.

³¹ *Id.*

³² See <https://www.renesas.com/us/en/document/mah/r178f12-users-manual-hardware-rev111?r=1054251> (last visited March 28, 2022), at 653.

(14) **Serial standby control register 0 (SSCO)**
 The SSCO register is used to control the startup of reception (the SNOOZE mode) while in the STOP mode when receiving CSI00 or UART0 serial data.

Figure 13-21. Format of Serial Standby Control Register 0 (SSCO)

Address: F0138H, F0139H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSCO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SS EC0	Selection of whether to enable or stop the generation of transfer end interrupts
0	Enable the generation of error interrupts (INTSRE0). In the following cases, the clock request signal (an internal signal) to the clock generator is also cleared: • When the SWC bit is cleared to 0 • When the UART reception start bit is mistakenly detected
1	Stop the generation of error interrupts (INTSRE0). In the following cases, the clock request signal (an internal signal) to the clock generator is also cleared: • When the SWC bit is cleared to 0 • When the UART reception start bit is mistakenly detected • When the transfer end interrupt generation timing is based on a parity error or framing error

SWC 0	SNOOZE mode setting
0	SNOOZE mode function is not used.
1	SNOOZE mode function is used. • STOP mode is cancelled by the hardware trigger signal generated during STOP mode, and reception operation of the CSI/UART is performed without the CPU operation (SNOOZE mode). • The SNOOZE mode function can be set only when high-speed on-chip oscillator clock is selected for the CPU/peripheral hardware clock (f _{CLK}). Setting SNOOZE mode function is prohibited when any other clock is selected. • Even when SNOOZE mode is used, the SWC bit must be set to 0 in normal operation mode. Change the bit to 1 immediately before a transition to STOP mode. After a return from STOP mode to normal operation mode, be sure to clear the SWC bit to 0.

Figure 13-21. RL78/F12 User’s Manual at p. 478 (emphasis added).³³

This operation is further demonstrated by the Timing Chart of SNOOZE Mode Operation:

Correct:
 Figure 14-90. Timing Chart of SNOOZE Mode Operation (EOCm1 = 0, SSECm = 0/1)

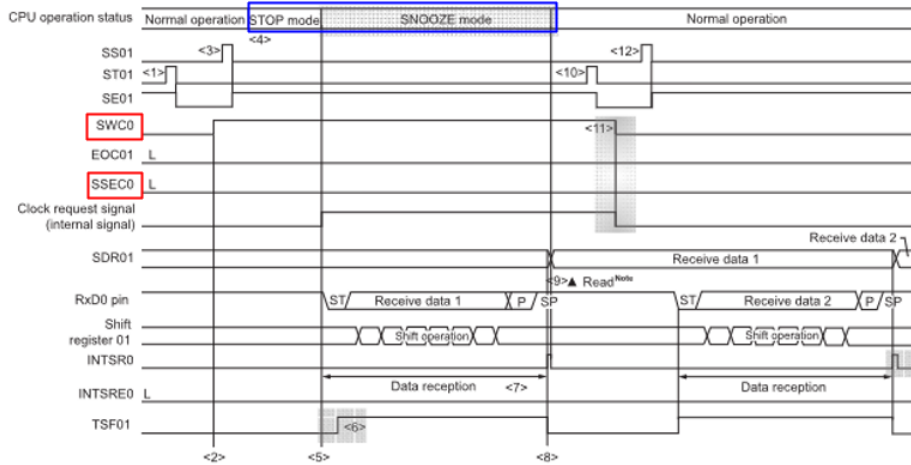


Figure 14-93. Renesas Technical Update at 9 (emphasis added).³⁴

³³ See <https://www.renesas.com/us/en/document/mah/rl78f12-users-manual-hardware-rev111?r=1054251> (last visited March 28, 2022), at 478.

³⁴ See <https://www.renesas.com/us/en/document/tcu/correction-incorrect-description-notice-rl78l13?language=en> (last visited April 4, 2022), at 9.

61. The '479 Accused Products are configured such that when the MCU is in Stop mode, the high-speed system clock oscillator and internal high-speed oscillator are disabled, stopping the whole system.³⁵ As explained by the RL78/F12 User's Manual, the "STOP instruction . . . stop[s] the whole system, thereby considerably reducing the CPU operating current."³⁶ "The STOP mode is set by executing the STOP instruction"³⁷ This STOP instruction stops the operation of the CPU [main module], as demonstrated by Table 20-2 below:

Table 20-2. Operating Statuses in STOP Mode

STOP Mode Setting		When STOP Instruction Is Executed While CPU Is Operating on Main System Clock		
		When CPU Is Operating on High-Speed On-Chip Oscillator Clock (f _{osc})	When CPU Is Operating on X1 Clock (f _{x1})	When CPU Is Operating on External Main System Clock (f _{ext})
System clock		Clock supply to the CPU is stopped		
Main system clock	f _{osc}	Stopped		
	f _{x1}			
	f _{ext}			
Subsystem clock	f _{osc}	Status before STOP mode was set is retained		
	f _{ext}			
f _{osc}		Set by bits 6 (WDSTBYON) and 4 (YDTON) of option byte (000C0H), and WUTMMCK0 bit of operation speed mode control register (OSMC) <ul style="list-style-type: none"> • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 1 and YDTON = 0: Stops • WUTMMCK0 = 1, YDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 1, YDTON = 1, and WDSTBYON = 0: Stops 		
CPU		Operation stopped		
Code flash memory				
Data flash memory		Operation stopped (Executing the STOP instruction is disabled during data flash programming)		
RAM		Operation stopped		

Table 20-2. RL78/F12 User's Manual at p. 895 (emphasis added).³⁸

62. The '479 Accused Products include "an auxiliary module, coupled to the main module, for providing an auxiliary function to the electronic apparatus, and generating a second control signal." For example, the '479 Accused Products include second circuitry and/or firmware that is coupled to the main module. The second circuitry and/or firmware are configured to provide

³⁵ See <https://www.renesas.com/us/en/document/apn/rl78f13-f14-standby-function-rev100?language=en> (last visited March 28, 2022), at 6-8.

³⁶ See <https://www.renesas.com/us/en/document/mah/rl78f12-users-manual-hardware-rev111?r=1054251> (last visited March 28, 2022), at 885.

³⁷ *Id.*

³⁸ *Id.* at 895.

data reception to the '479 Accused Products outside of Normal Operation mode. The second circuitry and/or firmware are configured to generate a signal on the RxDn pin (e.g., a RxD0 pin input) that is configured to transition the '479 Accused Products from the Stop mode to the Snooze mode.³⁹ For example, while the MCU is in Stop mode, a change in the RxDn pin (e.g., a RxD0 pin input) will trigger a transition from Stop mode to Snooze mode.⁴⁰ As explained by the RL78/F12 User's Manual, "UART0 reception (channel 1 of unit 0) [of the communication hardware] supports the SNOOZE mode. When RxD0 pin input [second control signal] is detected while in the STOP mode, the SNOOZE mode makes data reception that does not require the CPU possible."⁴¹ This operation is further demonstrated by the Timing Chart and the Flowchart of SNOOZE Mode Operation:

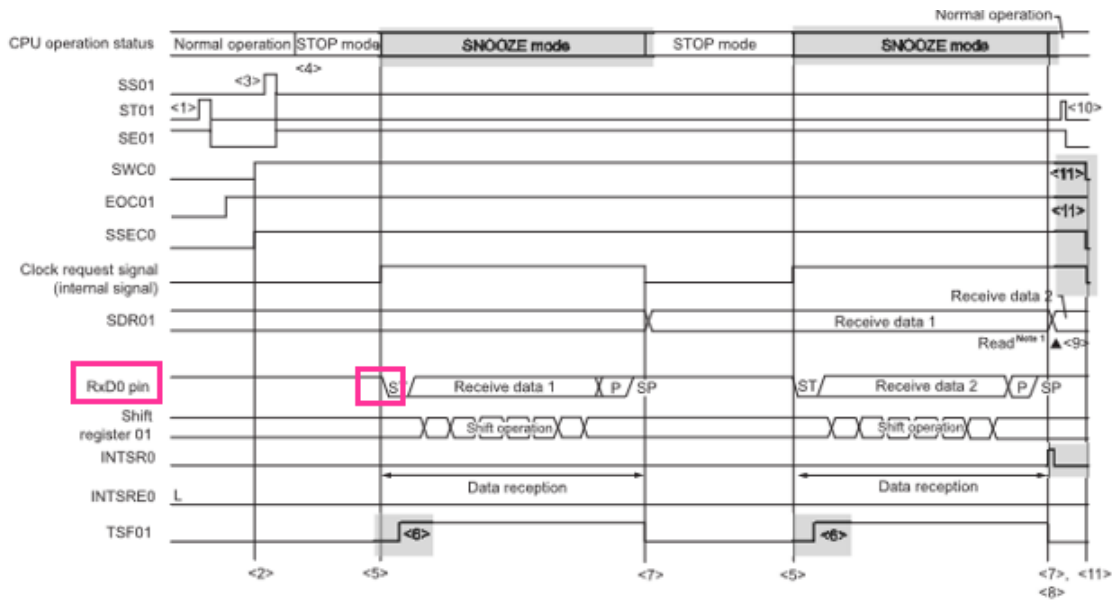


Figure 14-93. Renesas Technical Update at 9 (emphasis added).⁴²

³⁹ *Id.* at 566, 597.

⁴⁰ *Id.*

⁴¹ *Id.* at 594.

⁴² See <https://www.renesas.com/us/en/document/tcu/correction-incorrect-description-notice-rl78l13?language=en> (last visited April 4, 2022), at 9.

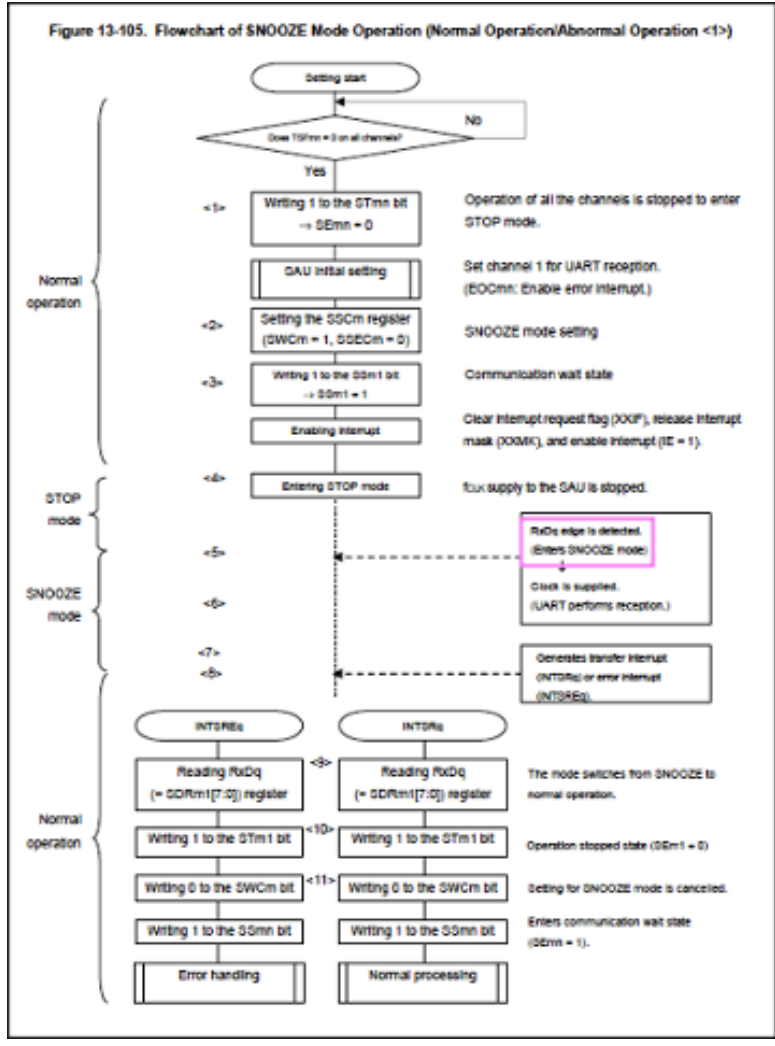


Figure 13-105-Flowchart. RL78/F12 User’s Manual at p. 595 (emphasis added).⁴³

63. The '479 Accused Products include “a wake-up circuit module, coupled to the main module and the auxiliary module, for generating a third control signal in accordance with the first control signal and the second control signal.” For example, the '479 Accused Products include third circuitry and/or firmware that is coupled to the main module and the auxiliary module. The third circuitry and/or firmware is configured to generate a clock request signal (internal signal) that allows the data reception from the synchronous or UART serial port to continue to operate

⁴³ See <https://www.renesas.com/us/en/document/mah/rl78f12-users-manual-hardware-rev111?r=1054251> (last visited March 28, 2022), at 595.

while the MCU is in Snooze mode. This operation is further demonstrated by the Timing Chart of SNOOZE Mode Operation:

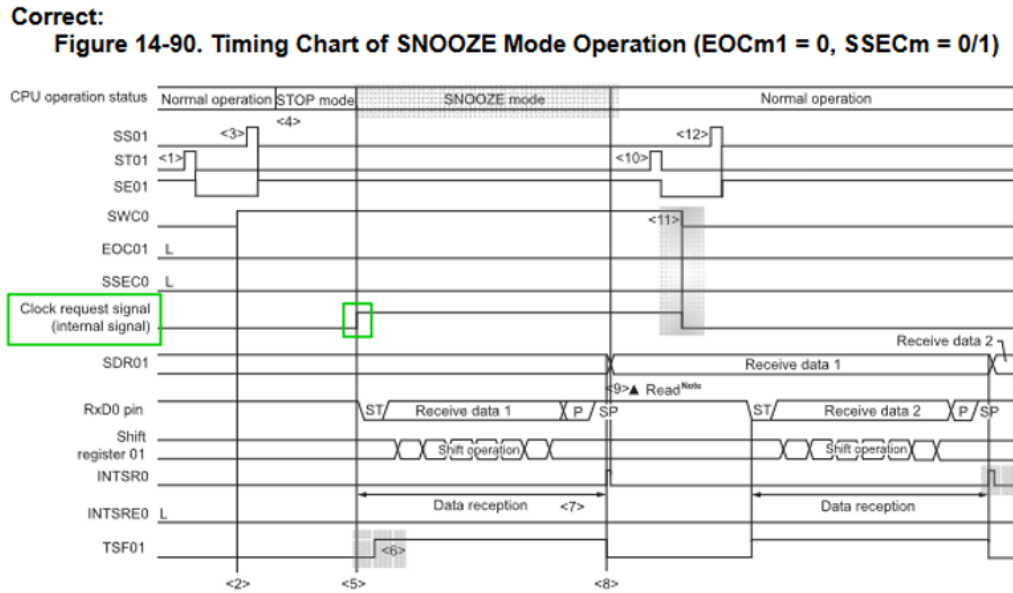


Figure 14-93. Renesas Technical Update at 9 (emphasis added).⁴⁴

64. The '479 Accused Products are configured such that “wherein, the auxiliary module maintains the auxiliary function in accordance with the third control signal in the sleep mode.” For example, the second circuitry and/or firmware is configured to maintain the auxiliary data reception function (UART function) in accordance with the clock request signal [the third control signal] while the MCU is in Snooze mode.

⁴⁴ See <https://www.renesas.com/us/en/document/tcu/correction-incorrect-description-notice-r178113?language=en> (last visited April 4, 2022), at 9.

Correct:

Figure 14-90. Timing Chart of SNOOZE Mode Operation (EOCm1 = 0, SSECM = 0/1)

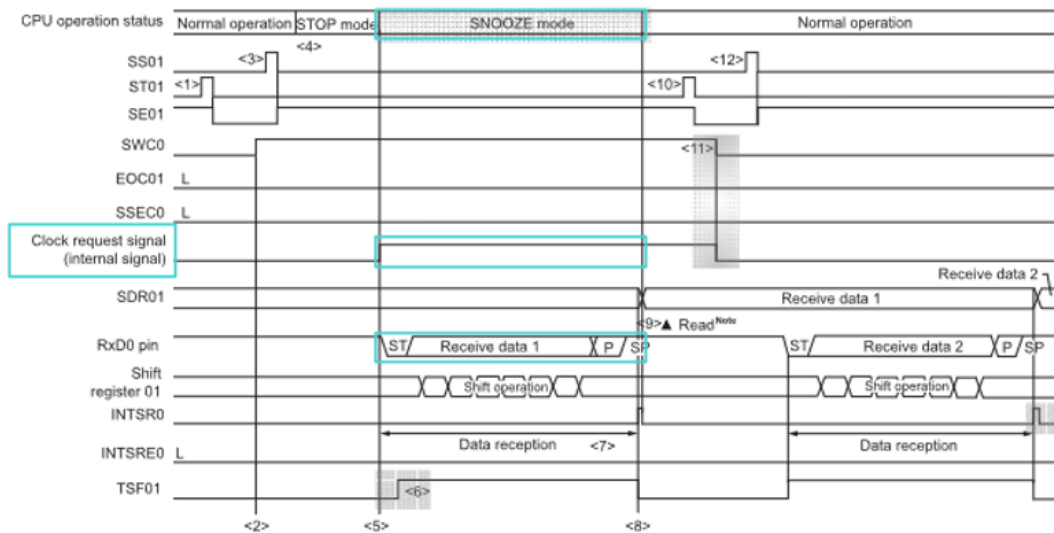


Figure 14-93. Renesas Technical Update at 9 (emphasis added).⁴⁵

Indirect Infringement (Inducement – 35 U.S.C. § 271(b))

65. In addition and/or in the alternative to its direct infringements, Renesas has indirectly infringed and continues to indirectly infringe one or more claims of the '479 Patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the '479 Accused Products.

66. At a minimum, Renesas has knowledge of the '479 Patent since being served with the Original Complaint and this First Amended Complaint. Renesas also has knowledge of the '479 Patent since receiving detailed correspondence from XTI dated February 28, 2022, alerting Renesas to its infringements. Since receiving notice of its infringements, Renesas has actively induced the direct infringements of its subsidiaries, distributors, affiliates, retailers, suppliers,

⁴⁵ *Id.*

integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Such inducements have been committed with the knowledge, or with willful blindness to the fact, that the acts induced constitute infringement of the '479 Patent. Indeed, Renesas has intended to cause, continues to intend to cause, and has taken, and continues to take, affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the '479 Accused Products; creating and/or maintaining established distribution channels for the '479 Accused Products into and within the United States; manufacturing the '479 Accused Products in conformity with U.S. laws and regulations; distributing or making available datasheets supporting use of the '479 Accused Products that promote their features, specifications, and applications; providing technical documentation and tools for the '479 Accused Products, including white papers, brochures, and manuals; promoting the incorporation of the '479 Accused Products into end-user products through the development of Renesas' Partner programs, complimentary design review services, automated utilities, calculators, and reference designs; testing and certifying features related to the "SNOOZE mode" [sleep mode] in the '479 Accused Products; and by providing technical support and/or related services for these products to purchasers in the United States through Renesas' online support platforms including RenesasRulz forum and Renesas Synergy Platform further explaining how to use Renesas' products.

Damages

67. On information and belief, despite having knowledge of the '479 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the '479 Patent, Renesas has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. Renesas' infringing activities relative to the '479 Patent have been, and

continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, characteristic of a pirate, and an egregious case of misconduct beyond typical infringement such that XTI is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

68. XTI has been damaged as a result of Renesas' infringing conduct described in this Count. Renesas is, thus, liable to XTI in an amount that adequately compensates XTI for Renesas' infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

COUNT III

(INFRINGEMENT OF U.S. PATENT NO. 8,643,659)

69. Plaintiff incorporates the preceding paragraphs herein by reference.

70. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq.*

71. XTI is the owner of all substantial rights, title, and interest in and to the '659 Patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

72. The '659 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on February 4, 2014, after full and fair examination.

73. Renesas has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the '659 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, Renesas products, their components and processes, and/or products containing the same that incorporate the fundamental technologies

covered by the '659 Patent, including, but not limited to, the Renesas R-Car Automotive System-on-Chips (SoCs) and the Renesas RZ MPU Family (collectively, the "'659 Accused Products").⁴⁶

Direct Infringement (35 U.S.C. § 271(a))

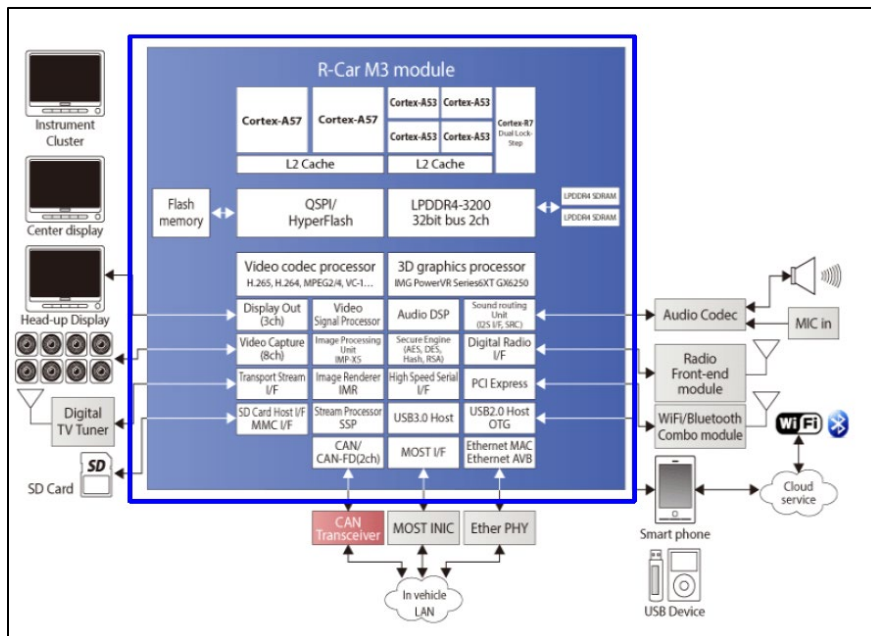
74. Renesas has directly infringed and continues to directly infringe one or more claims of the '659 Patent in this District and elsewhere in Texas and the United States.

75. Renesas has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 6 of the '659 Patent as set forth under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing the '659 Accused Products. Furthermore, Renesas makes and sells the '659 Accused Products outside of the United States and either, delivers those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivers the '659 Accused Products outside of the United States, it does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the '659 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013). Furthermore, Renesas directly infringes the '659 Patent through its direct involvements in, and control of, the activities of its subsidiaries, including REA. Subject to Renesas' direction and control, such subsidiaries conduct activities that constitute direct infringement of the '659 Patent under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing '659 Accused Products. Renesas receives direct financial benefit from such infringements of its U.S.-based sales subsidiaries, including REA.

⁴⁶ **Renesas R-Car Automotive System-on-Chips (SoCs)** – R-Car M3, R-Car M3e, R-Car M3Ne, R-Car H3, R-Car H3e, R-Car H3Ne, R-Car H2, R-Car D3, R-Car D3e, R-Car E2, R-Car E3e, R-Car V3U, R-Car M2, R-Car E2, R-Car V2H & R-Car D1; **Renesas RZ MPU Family** – RZ/G1H, RZ/G2E, RZ/G2H, RZ/G2M, RZ/G2N, RZ/G1C, RZ/G1E, RZ/G1M & RZ/G1N.

76. By way of illustration only, the '659 Accused Products include each and every element of claim 6 of the '659 Patent.

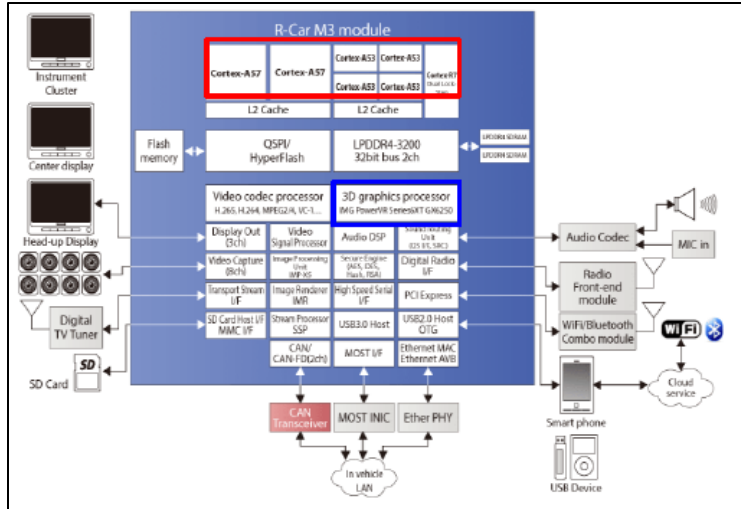
77. The '659 Accused Products include “[a] computer system for 3D graphics processing.” For example, the '659 Accused Products are comprised of a system of components that support the processing of 3D graphics, as demonstrated below:



R-Car M3 Block Diagram (emphasis added).⁴⁷

78. The '659 Accused Products include “a host processor” and [a] 3D graphics accelerator.” For example, the '659 Accused Products include a “CPU core” [host processor] and a “3D Graphics” card [3D graphics accelerator] as demonstrated below:

⁴⁷ See <https://www.renesas.com/sites/default/files/r-car-m3-block-diagram.png> (last visited March 28, 2022).



R-Car M3 Block Diagram (emphasis added).⁴⁸

Main Product Specifications of the R-Car M3 SoC			
Item	R-Car M3 Specifications		
Product No	R-Car M3 (R8J77960 (SiP), R8A77960 (SoC))		
Power supply voltage	3.3/1.8 V (IO), 1.1 V (LPDDR4), 0.9 V (core)		
CPU core	ARM® Cortex®-A57 Dual	ARM® Cortex®-A53 Quad	ARM® Cortex®-R7 Dual Lock-Step
Cache memory	L1 Instruction cache: 48 KB	L1 Instruction cache: 32 KB	L1 Instruction cache: 32 KB
	L1 Operand cache: 32 KB	L1 Operand cache: 32 KB	L1 Operand cache: 32 KB
	L2 cache: 1 MB	L2 cache: 512 KB	
External memory	• LPDDR4-SDRAM • Maximum operating frequency: 1600 MHz • Data bus width : 32 bits x 2 ch (12.8 GB/s x 2)		
3D Graphics	Imagination Technologies' PowerVR® Series 6XT GX6250 Display Out x 3 ch		

R-Car M3 Specifications (emphasis added).⁴⁹

79. The '659 Accused Products include “a fragment shading unit running multiple threads and including a first on chip cache that stores cached instructions to be executed by said fragment shading unit.” As demonstrated above, the '659 Accused Products are configured to

⁴⁸ *Id.*

⁴⁹ See <https://www.renesas.com/us/en/document/pre/main-product-specifications-r-car-m3-soc?r=1172516> (last visited March 28, 2022).

utilize at least the PowerVR GX6250 3D graphics card from Imagination Technologies. For example, the PowerVR GX6250 is comprised of a Graphics Core [fragment shading unit], as demonstrated below:

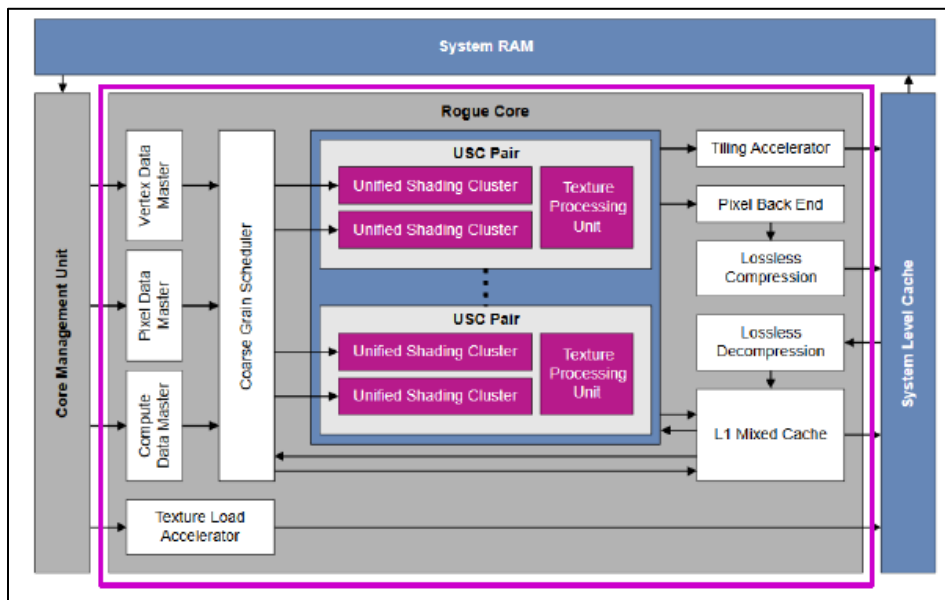
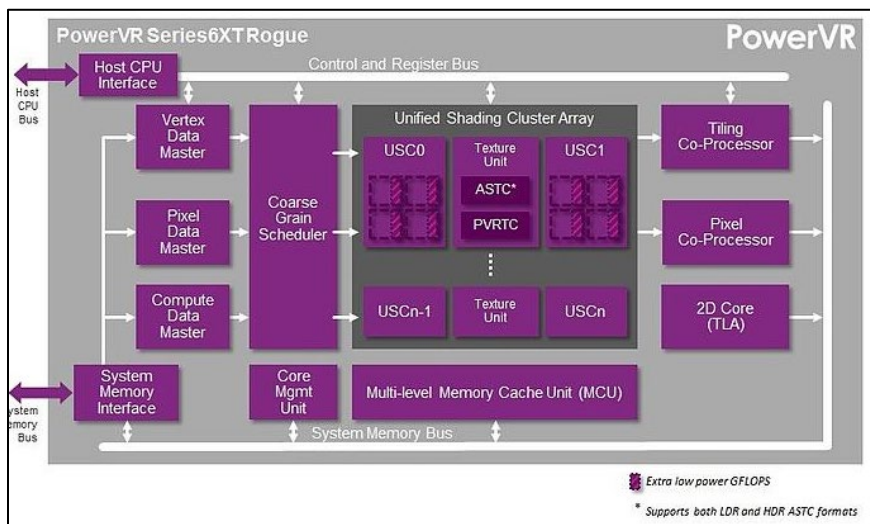


Figure 2: Rogue Architecture and Data Flow Overview at p. 10 (emphasis added).⁵⁰



Block Diagram of PowerVR Series6XT GPUs⁵¹

⁵⁰ See [https://cdn.imgtec.com/sdk-documentation/PowerVR%20Compute%20Development %20Recommendations.pdf](https://cdn.imgtec.com/sdk-documentation/PowerVR%20Compute%20Development%20Recommendations.pdf) (last visited March 28, 2022), at 10.

⁵¹ See <https://blog.imaginationtech.com/new-powervr-series6xt-gpus-go-rogue-ces-2014/> (last visited March 28, 2022).

80. The Graphics Core [fragment shading unit] is configured to execute threads together [running multiple threads].⁵² As explained by Imagination Technologies, “[e]ach work item of OpenCL, thread of OpenGL ES, or kernel invocation for RenderScript is handled as a thread of instructions in the hardware. These threads are executed together, in groups of up to 32, known as a task.” While “[t]asks are the grouping used by Rogue hardware for SIMD execution of threads, with each task treated as a unit of work.”⁵³

81. The Graphics Core [fragment shading unit] of the PowerVR GX6250 further includes residency slots [a first on-chip cache], as demonstrated below:

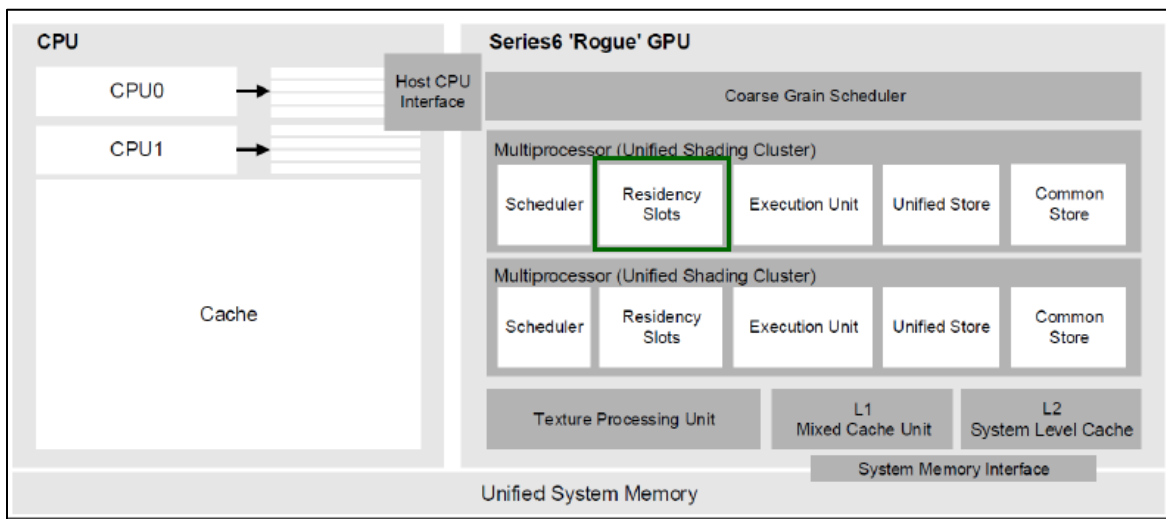


Figure of Rogue Architecture and Data Flow Overview (emphasis added).⁵⁴

⁵² See <https://cdn.imgtec.com/sdk-Documents/PowerVR%20Compute%20Development%20Recommendations.pdf> (last visited March 28, 2022), at 12.

⁵³ *Id.*

⁵⁴ See <https://blog.imaginationtech.com/a-quick-guide-to-writing-opencl-kernels-for-rogue/> (last visited March 28, 2022).

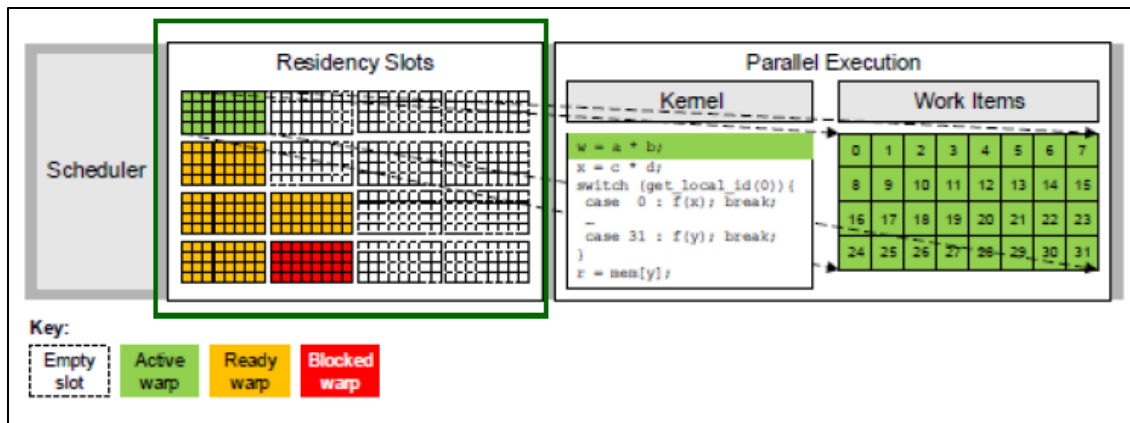


Figure of Parallel Execution (emphasis added).⁵⁵

82. As demonstrated above, each multiprocessor contains a number of residency slots that at any time are either empty (illustrated as a grid with a dotted line) or occupied by a warp (illustrated as a grid with a solid line and colour fill).⁵⁶ On information and belief, the residency slots [a first on-chip cache] is configured to store cached instructions to be executed by the Graphics Core [fragment shading unit]. As explained, “[e]ach warp can be in one of three states: active (green fill) which means it is currently running on the execution unit [of the Graphics Core]; ready (orange fill) which means the scheduler may run the warp on the execution unit [of the Graphics Core] after executing the active warp; and blocked (red fill) which means that one or more of the work items in the warp is awaiting a memory or barrier operation to complete.”⁵⁷

83. The ’659 Accused Products include “wherein the first cache is included within said fragment shading unit.” For example, the residency slots [first cache] are included within the Graphics Core [fragment shading unit] of the PowerVR GX6250, as demonstrated by at least Figures 2 and 8 above.⁵⁸

⁵⁵ *Id.*

⁵⁶ *Id.*

⁵⁷ *Id.*

⁵⁸ *Id.*

84. The '659 Accused Products include “wherein an external virtual memory stores a portion of the data used by said fragment shading unit.” For example, the Rogue architecture of the PowerVR GX6250 includes at least a “System Level Cache” [external virtual memory] that is outside of the Graphics Core. The System Level Cache [external virtual memory] is configured to interact directly with the System RAM and is the last chance for a data fetch to hit a cache. Data fetches that miss the System Level Cache are fetched from System RAM. On information and belief, the System Level Cache [external virtual memory] is further configured to store a portion of the data used by the Graphics Core [fragment shading unit], as demonstrated by the architecture and data flow below:

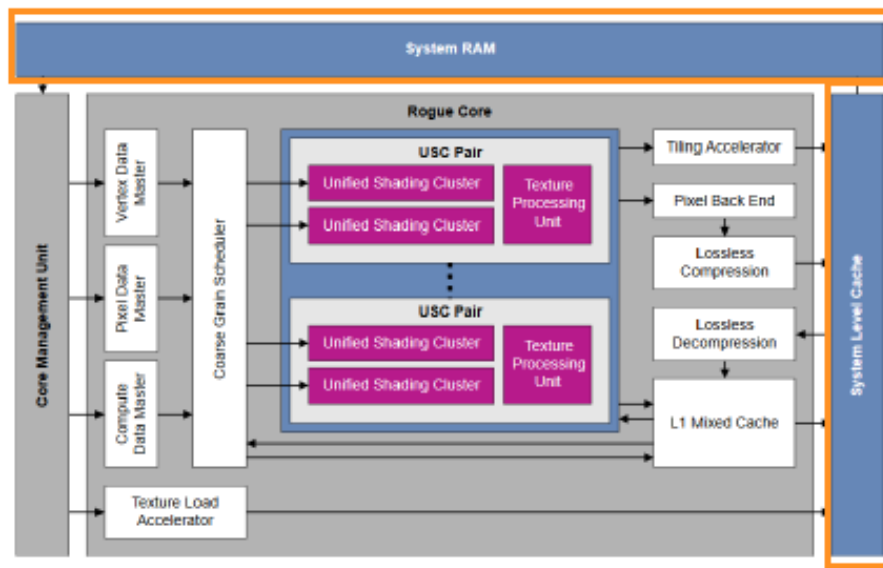


Figure 2: Rogue Architecture and Data Flow Overview at p. 10 (emphasis added).⁵⁹

85. As demonstrated above, the Rogue architecture of the PowerVR GX6250 further includes the L1 Mixed Cache and the System RAM.⁶⁰ The external Random Access Memory (RAM) is configured to serve as the system’s memory and to be used by all system components.

⁵⁹ See [https://cdn.imgtec.com/sdk-documentation/PowerVR%20Compute%20Development %20Recommendations.pdf](https://cdn.imgtec.com/sdk-documentation/PowerVR%20Compute%20Development%20Recommendations.pdf) (last visited March 28, 2022), at 10.

⁶⁰ *Id.* at 16-17.

⁶¹ The L1 Mixed Cache is configured to serve as the main cache used by the Rogue architecture and further configured such that all data transfers to and from memory go through the L1 Mixed Cache first.⁶² If the L1 Mixed Cache cannot serve a data fetch request, the request is passed to the System Level Cache [external virtual memory].⁶³

86. The '659 Accused Products include “wherein a second on chip cache is included within said fragment shading unit, the second cache storing global data which can affect multiple fragments being shaded by said fragment shading unit.” For example, the architecture of the PowerVR GX6250 includes at least a “L1 Mixed Cache” [second on-chip cache] within the Graphics Core, as demonstrated below:

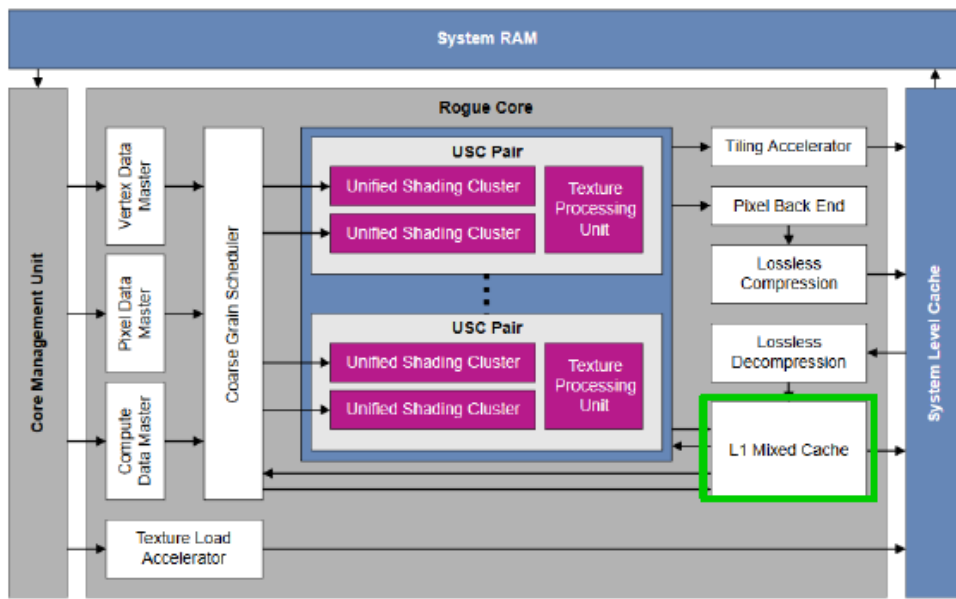


Figure 2: Rogue Architecture and Data Flow Overview at p. 10 (emphasis added).⁶⁴

87. The L1 Mixed Cache [second on-chip cache] is configured to serve as the main cache used by the Rogue architecture and further configured such that all data [global data]

⁶¹ *Id.*

⁶² *Id.*

⁶³ *Id.*

⁶⁴ *Id.* at 10.

transfers to and from memory go through the L1 Mixed Cache first.⁶⁵ If the L1 Mixed Cache cannot serve a data fetch request, the request is passed to the System Level Cache [external virtual memory].⁶⁶ On information and belief, all of the data [global data] stored by the L1 Mixed Cache [second on-chip cache] is configured to affect multiple fragments being shaded by Graphics Core [fragment shading unit].

88. The '659 Accused Products include “whereby said fragment shading unit can switch operations between threads in a lightweight manner.” For example, the Graphics Core [fragment shading unit] is further comprised of a Fine Grained Scheduler (FGS), as demonstrated below:

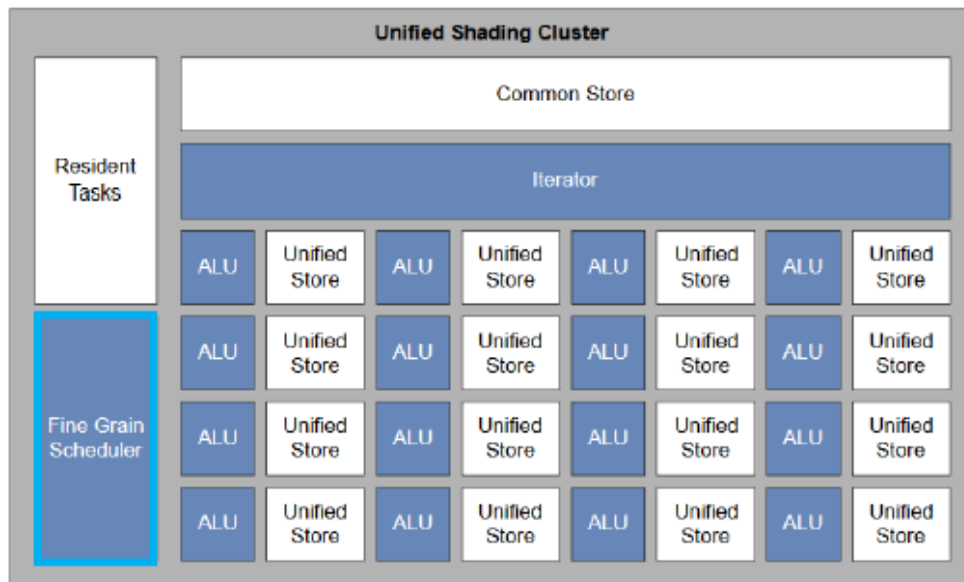


Figure 3: Rogue Unified Shading Cluster at p. 11 (emphasis added).⁶⁷

89. The Fine Grained Scheduler (FGS) is configured to schedule and deschedule a work on a per-task basis from a pool of resident tasks.⁶⁸ As previously discussed, “[t]asks are the

⁶⁵ *Id.* at 16-17.

⁶⁶ *Id.*

⁶⁷ *Id.* at 11.

⁶⁸ *Id.* at 12.

grouping used by Rogue hardware for SIMD execution of threads, with each task treated as a unit of work.⁶⁹ “Tasks that need to wait for any reason are switched out and a ready-to-execute task is scheduled in its place immediately” by the Fine Grained Scheduler (FGS) of the Graphics Core [fragment shading unit].

Indirect Infringement (Inducement – 35 U.S.C. § 271(b))

90. In addition and/or in the alternative to its direct infringements, Renesas has indirectly infringed and continues to indirectly infringe one or more claims of the ’659 Patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the ’659 Accused Product.

91. At a minimum, Renesas has knowledge of the ’659 Patent since being served with the Original Complaint and this First Amended Complaint. Renesas also has knowledge of the ’659 Patent since receiving detailed correspondence from XTI dated March 25, 2021, alerting Renesas to its infringements. Since receiving notice of its infringements, Renesas has actively induced the direct infringements of its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Such inducements have been committed with the knowledge, or with willful blindness to the fact, that the acts induced constitute infringement of the ’659 Patent. Indeed, Renesas has intended to cause, continues to intend to cause, and has taken, and continues to take, affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the ’659 Accused Products; creating and/or

⁶⁹ *Id.* at 12.

maintaining established distribution channels for the '659 Accused Products into and within the United States; manufacturing the '659 Accused Products in conformity with U.S. laws and regulations; distributing or making available datasheets supporting use of the '659 Accused Products that promote their features, specifications, and applications; providing technical documentation and tools for the '659 Accused Products, including white papers, brochures, and manuals; promoting the incorporation of the '659 Accused Products into end-user products through the development of Renesas' Partner programs, complimentary design review services, automated utilities, calculators, and reference designs; testing and certifying features related to 3D graphics processing in the '659 Accused Products; and by providing technical support and/or related services for these products to purchasers in the United States through Renesas' online support platforms including RenesasRulz forum and Renesas Synergy Platform further explaining how to use Renesas' products.

Damages

92. On information and belief, despite having knowledge of the '659 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the '659 Patent, Renesas has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. Renesas' infringing activities relative to the '659 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, characteristic of a pirate, and an egregious case of misconduct beyond typical infringement such that XTI is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

93. XTI has been damaged as a result of Renesas' infringing conduct described in this Count. Renesas is, thus, liable to XTI in an amount that adequately compensates XTI for Renesas'

infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

COUNT IV

(INFRINGEMENT OF U.S. PATENT NO. 10,162,642)

94. Plaintiff incorporates the preceding paragraphs herein by reference.

95. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq.*

96. XTI is the owner of all substantial rights, title, and interest in and to the '642 Patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

97. The '642 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on December 25, 2018, after full and fair examination.

98. Renesas has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the '642 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, Renesas products, their components and processes, and/or products containing the same that incorporate the fundamental technologies covered by the '642 Patent, including, but not limited to,, the Renesas R-Car Automotive System-on-Chips (SoCs) and the Renesas RZ MPU Family(collectively, the "'642 Accused Products").⁷⁰

⁷⁰ **Renesas R-Car Automotive System-on-Chips (SoCs)** – R-Car M3, R-Car M3e, R-Car M3Ne, R-Car H3, R-Car H3e, R-Car H3Ne, R-Car H2, R-Car D3, R-Car D3e, R-Car E2, R-Car E3e, R-Car V3U, R-Car M2, R-Car E2, R-Car V2H & R-Car D1; **Renesas RZ MPU Family** – RZ/G1H, RZ/G2E, RZ/G2H, RZ/G2M, RZ/G2N, RZ/G1C, RZ/G1E, RZ/G1M & RZ/G1N.

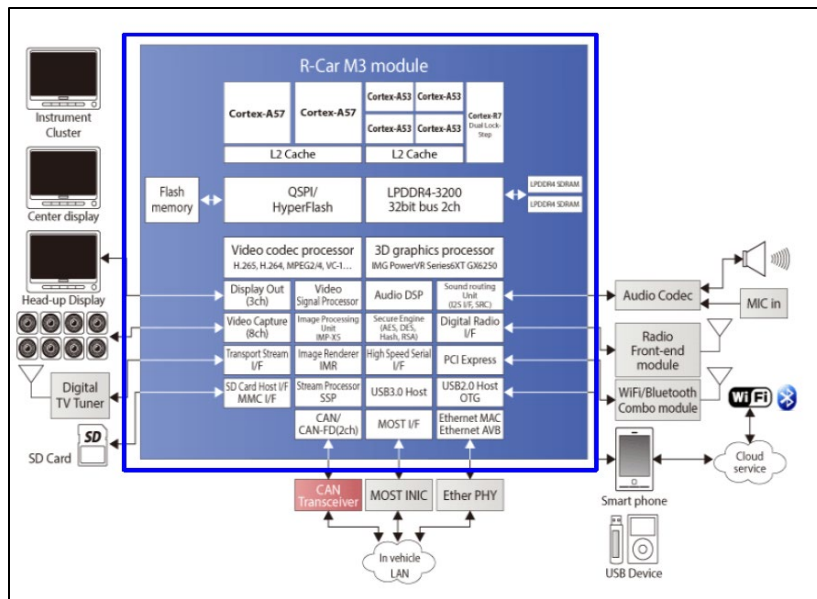
Direct Infringement (35 U.S.C. § 271(a))

99. Renesas has directly infringed and continues to directly infringe one or more claims of the '642 Patent in this District and elsewhere in Texas and the United States.

100. Renesas has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 1 of the '642 Patent as set forth under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing the '642 Accused Products. Furthermore, Renesas makes and sells the '642 Accused Products outside of the United States and either, delivers those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivers the '642 Accused Products outside of the United States, it does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the '642 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013). Furthermore, Renesas directly infringes the '642 Patent through its direct involvements in, and control of, the activities of its subsidiaries, including REA. Subject to Renesas' direction and control, such subsidiaries conduct activities that constitute direct infringement of the '642 Patent under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing '642 Accused Products. Renesas receives direct financial benefit from such infringements of its U.S.-based sales subsidiaries, including REA.

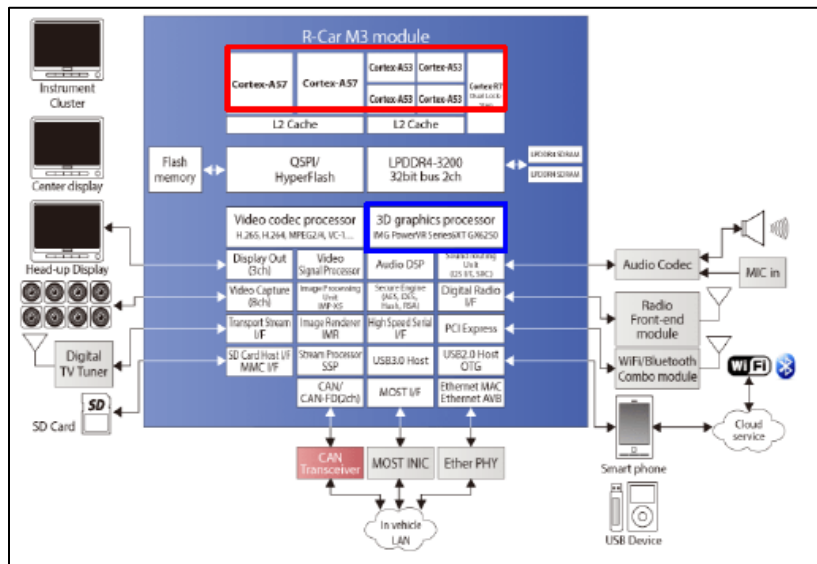
101. By way of illustration only, the '642 Accused Products include each and every element of claim 1 of the '642 Patent.

102. The '642 Accused Products include “[a] 3D graphics processing system.” For example, the '642 Accused Products are comprised of a system of components that support the processing of 3D graphics, as demonstrated below:



R-Car M3 Block Diagram (emphasis added).⁷¹

103. Key components of the Asserted Products that support 3D graphics processing include, but are not limited to, the CPU and the 3D Graphics Card (e.g., “the PowerVR GX6250 3D graphics card from Imagination Technologies”), as demonstrated below:



R-Car M3 Block Diagram (emphasis added).⁷²

⁷¹ See <https://www.renesas.com/sites/default/files/r-car-m3-block-diagram.png> (last visited March 28, 2022).

⁷² *Id.*

Main Product Specifications of the R-Car M3 SoC			
Item	R-Car M3 Specifications		
Product No	R-Car M3 (R8J77960 (SiP), R8A77960 (SoC))		
Power supply voltage	3.3/1.8 V (IO), 1.1 V (LPDDR4), 0.9 V (core)		
CPU core	ARM® Cortex®-A57 Dual	ARM® Cortex®-A53 Quad	ARM® Cortex®-R7 Dual Lock-Step
Cache memory	L1 Instruction cache: 48 KB L1 Operand cache: 32 KB L2 cache: 1 MB	L1 Instruction cache: 32 KB L1 Operand cache: 32 KB L2 cache: 512 KB	L1 Instruction cache: 32 KB L1 Operand cache: 32 KB
External memory	<ul style="list-style-type: none"> · LPDDR4-SDRAM · Maximum operating frequency: 1600 MHz · Data bus width : 32 bits x 2 ch (12.8 GB/s x 2) 		
3D Graphics	Imagination Technologies' PowerVR® Series 6XT GX6250		
	Display Out x 3 ch		

R-Car M3 Specifications (emphasis added).⁷³

104. The '642 Accused Products include “a fragment shading unit configured to perform shading operations, the fragment shading unit being further configured to run multiple shaders, each shader being run as a separate thread for a shading operation.” As demonstrated above, the '642 Accused Products are configured to utilize at least the PowerVR GX6250 3D graphics card from Imagination Technologies. For example, the PowerVR GX6250 is comprised of a Graphics Core [fragment shading unit], as demonstrated below:

⁷³ See <https://www.renesas.com/us/en/document/pre/main-product-specifications-r-car-m3-soc?r=1172516> (last visited March 28, 2022).

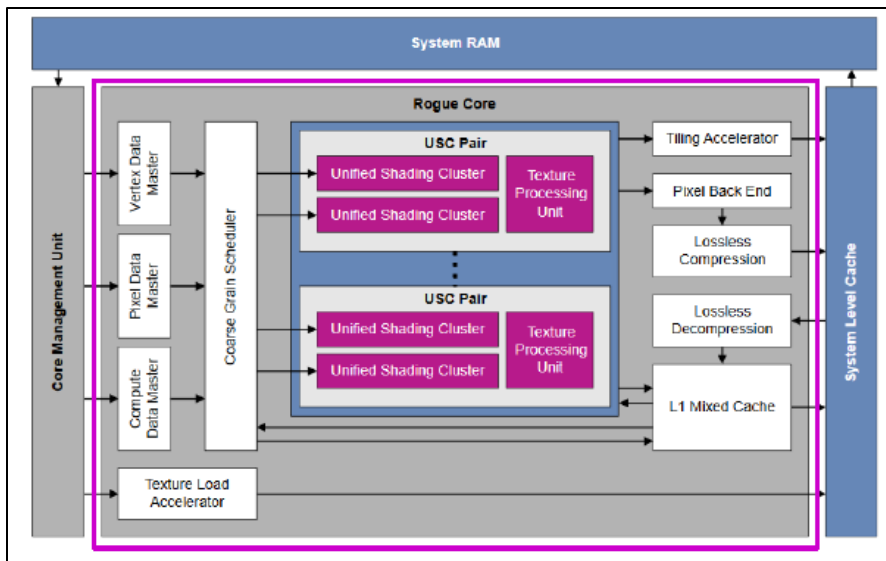
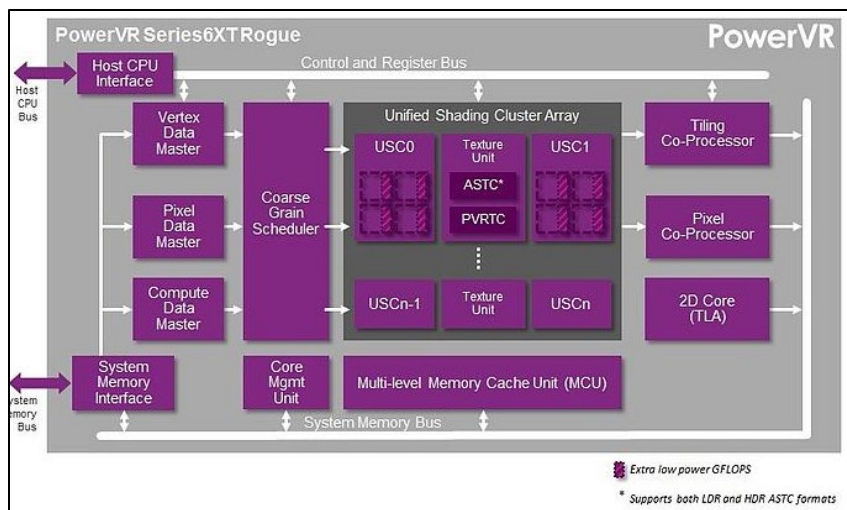


Figure 2: Rogue Architecture and Data Flow Overview at p. 10 (emphasis added).⁷⁴



Block Diagram of PowerVR Series6XT GPUs⁷⁵

105. On information and belief, the Graphics Core [fragment shading unit] is configured to run multiple Unified Shading Clusters (“USCs”) with each USC being run as a separate thread for a shading operation, as demonstrated by the architecture and data flow below:

⁷⁴ See [https://cdn.imgtec.com/sdk-documentation/PowerVR%20Compute%20Development %20Recommendations.pdf](https://cdn.imgtec.com/sdk-documentation/PowerVR%20Compute%20Development%20Recommendations.pdf) (last visited March 28, 2022), at 10.

⁷⁵ See <https://blog.imaginationtech.com/new-powervr-series6xt-gpus-go-rogue-ces-2014/> (last visited March 28, 2022).

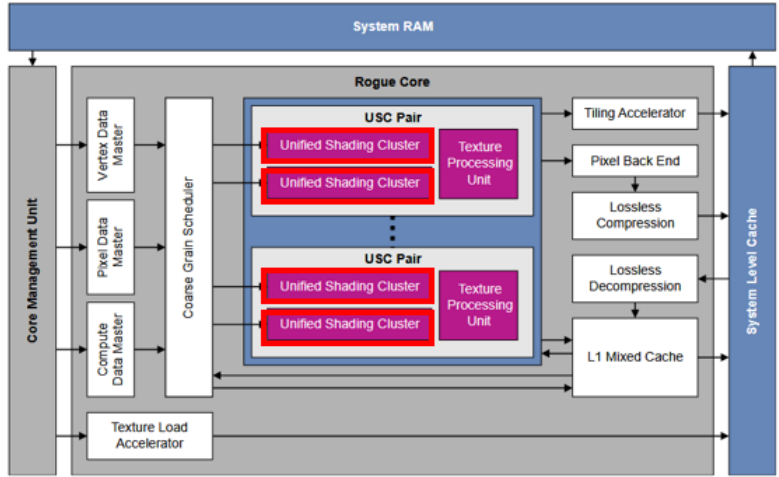


Figure 2: Rogue Architecture and Data Flow Overview at p. 10 (emphasis added).⁷⁶

106. As demonstrated above, the Graphics Core [fragment shading unit] is comprised of multiple Unified Shading Clusters (“USCs”). Each USC is configured to contain 16 Arithmetic Logic Units (“ALUs”), as demonstrated below:

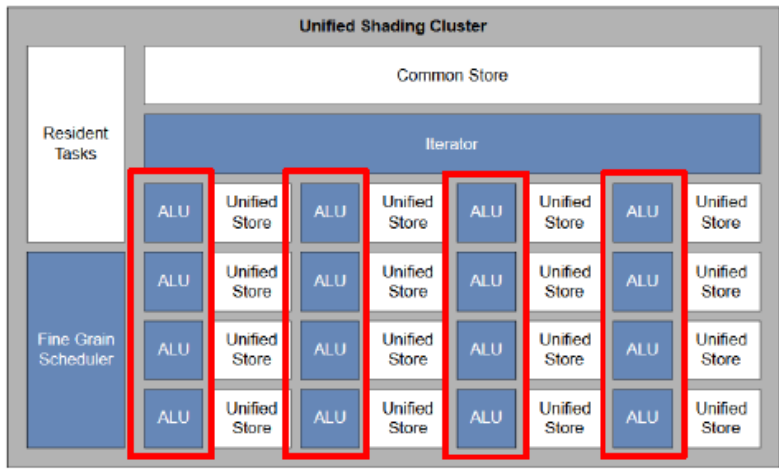


Figure 3: Rogue Unified Shading Cluster at p. 11 (emphasis added).⁷⁷

107. The ALUs of each USC are configured to process shader instructions.⁷⁸ As explained by Imagination Technologies, “[e]ach work item of OpenCL, thread of OpenGL ES, or

⁷⁶ See <https://cdn.imgtec.com/sdk-documentation/PowerVR%20Compute%20Development%20Recommendations.pdf> (last visited March 28, 2022), at 10.

⁷⁷ *Id.* at 11.

⁷⁸ *Id.* at 15.

kernel invocation for RenderScript is handled as a thread of instructions in the hardware. These threads are executed together, in groups of up to 32, known as a task. In any given cycle, 16 threads - one per ALU Pipe, will execute the same instruction. This means that half of a task runs in lockstep, with the other half staggered so that it executes one cycle behind.”⁷⁹

108. The '642 Accused Products include “a first on chip cache internal to the fragment shading unit and configured to store cached instruction used by the fragment shading unit.” For example, the Graphics Core [fragment shading unit] of the PowerVR GX6250 further includes internal residency slots [a first on-chip cache], as demonstrated below:

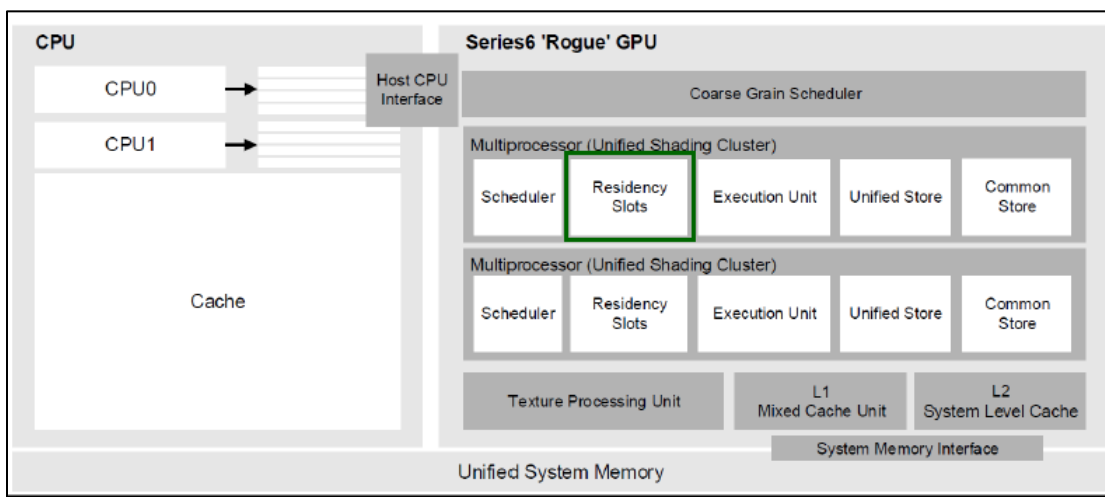


Figure of Rogue Architecture and Data Flow Overview (emphasis added).⁸⁰

⁷⁹ *Id.* at 12.

⁸⁰ See <https://blog.imaginationtech.com/a-quick-guide-to-writing-opengl-kernels-for-rogue/> (last visited March 28, 2022).

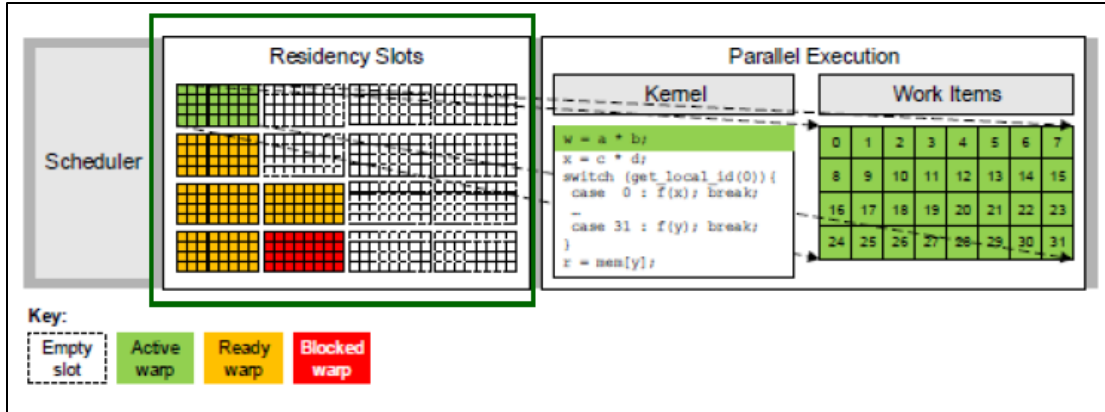


Figure of Parallel Execution (emphasis added).⁸¹

109. As demonstrated above, each multiprocessor contains a number of residency slots that at any time are either empty (illustrated as a grid with a dotted line) or occupied by a warp (illustrated as a grid with a solid line and color fill).⁸² On information and belief, the residency slots [a first on-chip cache] are configured to store cached instructions to be used by the Graphics Core [fragment shading unit]. As explained, “[e]ach warp can be in one of three states: active (green fill) which means it is currently running on the execution unit [of the Graphics Core]; ready (orange fill) which means the scheduler may run the warp on the execution unit [of the Graphics Core] after executing the active warp; and blocked (red fill) which means that one or more of the work items in the warp is awaiting a memory or barrier operation to complete.”⁸³

110. The '642 Accused Products include “a second on chip cache internal to the fragment shading unit and configured to store global data used by the fragment shading unit, wherein the global data is used by multiple shaders.” For example, the architecture of the PowerVR GX6250 includes at least an internal “L1 Mixed Cache” [second on-chip cache] within the Graphics Core, as demonstrated below:

⁸¹ *Id.*

⁸² *Id.*

⁸³ *Id.*

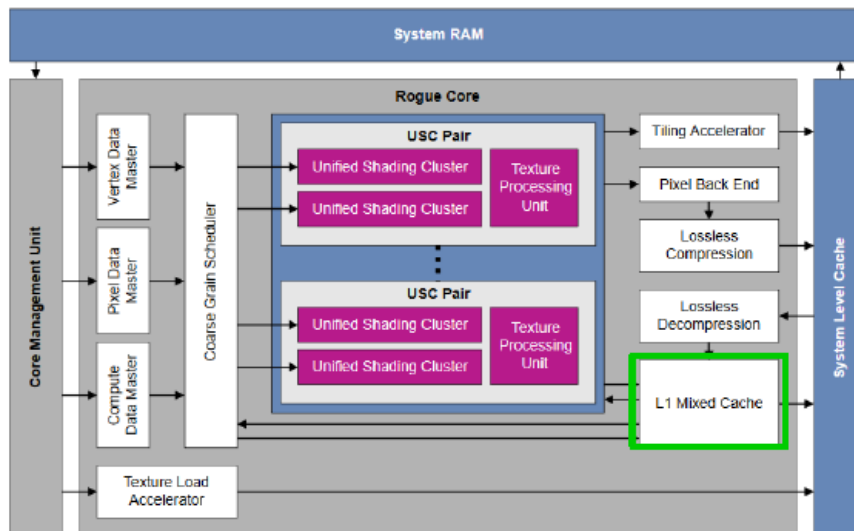


Figure 2: Rogue Architecture and Data Flow Overview at p. 10 (emphasis added).⁸⁴

111. On information and belief, the L1 Mixed Cache [second on-chip cache] is configured to store data transfers [global data] used by the Graphics Core [fragment shading unit]. The L1 Mixed Cache [second on-chip cache] is configured to serve as the main cache used by the Graphics Core [fragment shading unit] and further configured such that all data [global data] transfers to and from memory go through the L1 Mixed Cache first.⁸⁵ If the L1 Mixed Cache cannot serve a data fetch request, the request is passed to the System Level Cache [external virtual memory].⁸⁶

112. On information and belief, the data transfers [global data] is configured to be used by multiple USCs [multiple shaders]. The L1 Mixed Cache [second on-chip cache] is configured to serve the main cache used by the Graphics Core [fragment shading unit] and further configured

⁸⁴ See <https://cdn.imgtec.com/sdk-documentation/PowerVR%20Compute%20Development%20Recommendations.pdf> (last visited March 28, 2022), at 10.

⁸⁵ *Id.* at 16-17.

⁸⁶ *Id.*

such that all data [global data] transfers to and from memory go through the L1 Mixed Cache first.⁸⁷

113. The '642 Accused Products include “wherein the fragment shading unit is further configured to switch operations between the multiple threads upon the occurrence of a cache miss.” For example, the Graphics Core [fragment shading unit] is further comprised of a Fine Grained Scheduler (FGS), as demonstrated below:

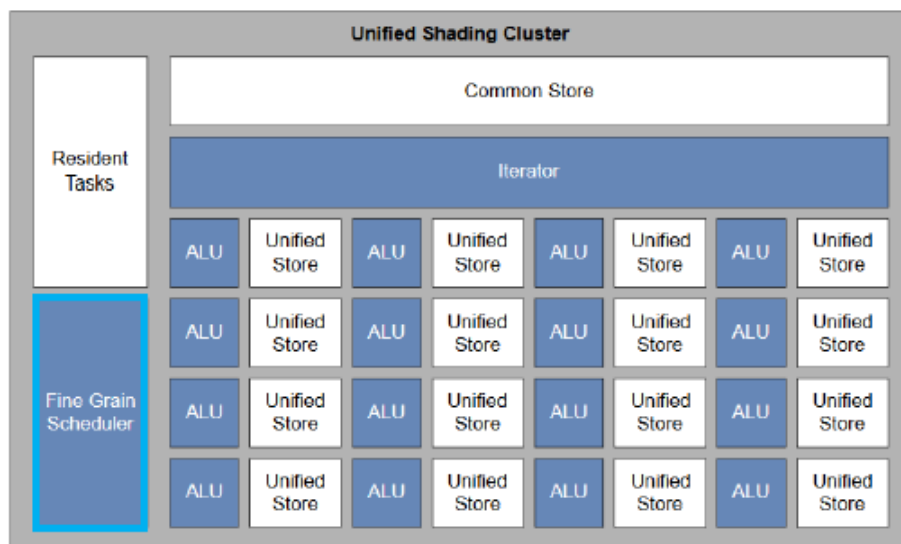


Figure 3: Rogue Unified Shading Cluster at p. 11 (emphasis added).⁸⁸

114. The Fine Grained Scheduler (FGS) is configured to schedule and deschedule a work on a per-task basis from a pool of resident tasks.⁸⁹ As previously discussed, “[t]asks are the grouping used by Rogue hardware for SIMD execution of threads, with each task treated as a unit of work.⁹⁰ “Tasks that need to wait for any reason are switched out and a ready-to-execute task is scheduled in its place immediately” by the Fine Grained Scheduler (FGS) of the Graphics Core [fragment shading unit]. As further explain by Imagination Technologies, “[w]henver a warp is

⁸⁷ *Id.*

⁸⁸ *Id.* at 11.

⁸⁹ *Id.* at 12.

⁹⁰ *Id.* at 12.

descheduled . . . the multiprocessor selects another resident warp that is ready to execute.”⁹¹ Therefore, “[w]henver the first warp has reached a statement that reads from an array allocated to system memory (mem), preventing it from continuing until some point in the future when the data has been fetched.” For example, “[t]he scheduler starts executing warp 0, which runs until it reaches a blocking operation such a read or write to system memory. At this time the scheduler deschedules warp 0 and starts executing warp 1.”⁹²

Indirect Infringement (Inducement – 35 U.S.C. § 271(b))

115. In addition and/or in the alternative to its direct infringements, Renesas has indirectly infringed and continues to indirectly infringe one or more claims of the ’642 Patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the ’642 Accused Products.

116. At a minimum, Renesas has knowledge of the ’642 Patent since being served with the Original Complaint and this First Amended Complaint. Renesas also has knowledge of the ’642 Patent since receiving detailed correspondence from XTI dated March 25, 2021, alerting Renesas to its infringements. Since receiving notice of its infringements, Renesas has actively induced the direct infringements of its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Such inducements have been committed with the knowledge, or with willful blindness to the fact, that the acts induced constitute infringement of the ’642 Patent. Indeed, Renesas has intended to cause,

⁹¹ See <https://blog.imaginationtech.com/a-quick-guide-to-writing-opencl-kernels-for-rogue/> (last visited March 28, 2022), at 642.

⁹² *Id.*

continues to intend to cause, and has taken, and continues to take, affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the '642 Accused Products; creating and/or maintaining established distribution channels for the '642 Accused Products into and within the United States; manufacturing the '642 Accused Products in conformity with U.S. laws and regulations; distributing or making available datasheets supporting use of the '642 Accused Products that promote their features, specifications, and applications; providing technical documentation and tools for the '642 Accused Products, including white papers, brochures, and manuals; promoting the incorporation of the '642 Accused Products into end-user products through the development of Renesas' Partner programs, complimentary design review services, automated utilities, calculators, and reference designs; testing and certifying features related to 3D graphics processing in the '642 Accused Products; and by providing technical support and/or related services for these products to purchasers in the United States through Renesas' online support platforms including RenesasRulz forum and Renesas Synergy Platform further explaining how to use Renesas' products.

Damages

117. On information and belief, despite having knowledge of the '642 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the '642 Patent, Renesas has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. Renesas' infringing activities relative to the '642 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, characteristic of a pirate, and an egregious case of misconduct beyond typical infringement such

that XTI is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

118. XTI has been damaged as a result of Renesas' infringing conduct described in this Count. Renesas is, thus, liable to XTI in an amount that adequately compensates XTI for Renesas' infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

CONCLUSION

119. XTI is entitled to recover from Renesas the damages sustained by XTI as a result of Renesas' wrongful acts and willful infringements in an amount subject to proof at trial, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court.

120. XTI has incurred and will incur attorneys' fees, costs, and expenses in the prosecution of this action. The circumstances of this dispute may give rise to an exceptional case within the meaning of 35 U.S.C. § 285, and XTI is entitled to recover its reasonable and necessary attorneys' fees, costs, and expenses.

JURY DEMAND

XTI hereby requests a trial by jury pursuant to Rule 38 of the Federal Rules of Civil Procedure.

PRAYER FOR RELIEF

XTI respectfully requests that the Court find in its favor and against Renesas, and that the Court grant XTI the following relief:

- (i) A judgment that one or more claims of the Asserted Patents have been infringed, either literally and/or under the doctrine of equivalents, by Renesas;

- (ii) A judgment that one or more claims of the Asserted Patents have been willfully infringed, either literally and/or under the doctrine of equivalents, by Renesas;
- (iii) A judgment that Renesas account for and pay to XTI all damages and costs incurred by XTI because of Renesas' infringing activities and other conduct complained of herein, including an accounting for any sales or damages not presented at trial;
- (iv) A judgment that Renesas account for and pay to XTI a reasonable, ongoing, post judgment royalty because of Renesas' infringing activities, including continuing infringing activities, and other conduct complained of herein;
- (v) A judgment that XTI be granted pre-judgment and post judgment interest on the damages caused by Renesas' infringing activities and other conduct complained of herein;
- (vi) A judgment that this case is exceptional under the provisions of 35 U.S.C. § 285 and award enhanced damages; and
- (vii) Such other and further relief as the Court deems just and equitable.

Dated: July 28, 2022

Respectfully submitted,

/s/ Edward R. Nelson III

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that on July 28, 2022 Defendant and its counsel are being served with a copy of this FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT via electronic mail.

/s/ Edward R. Nelson III