IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC. Plaintiff, v. **MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., MICRON TECHNOLOGY TEXAS LLC,** Defendants.	)	Civil Action No. 22-cv-00294 JURY TRIAL DEMANDED

FIRST AMENDED COMPLAINT

1. Plaintiff Netlist, Inc. ("Netlist"), by its undersigned counsel, for its First Amended Complaint against defendants Micron Technology, Inc. ("Micron Technology"), Micron Semiconductor Products, Inc. ("Micron Semiconductor"), and Micron Technology Texas, LLC ("Micron Texas") (collectively, "Micron" or "Defendants"), states as follows, with knowledge as to its own acts, and on information and belief as to the acts of others:

2. This action involves Netlist's U.S. Patent Nos. 7,619,912 (the "'912 patent," Exhibit 1), 11,093,417 (the "'417 patent," Exhibit 2), and 9,858,215 (the "'215 patent," Exhibit 3) (the "Patents-in-Suit").

I. THE PARTIES

3. Plaintiff Netlist is a corporation organized and existing under the laws of the State of Delaware, having a principal place of business at 111 Academy Drive, Suite 100, Irvine, CA 92617.

4. On information and belief, Micron makes dynamic random-access memory ("DRAM"), NAND Flash, and NOR Flash memory, and other memory products in semiconductor fabrication plants in the United States and other countries throughout the world. On information and belief, Micron sells its products to customers, including customers in this District, in the computer, networking and storage, consumer electronics, solid-state drives and mobile telecommunications markets.

5. On information and belief, Micron Technology is a corporation organized and existing under the laws of Delaware. On information and belief, Micron Technology has a regular and established place of business at 805 Central Expressway South, Suite 100, Allen, Texas 75013. On information and belief, Micron Technology is registered to do business in the State of Texas, and can be served through its registered agent, The Corporation Service Company, 211 E. 7th Street, Suite 620, Austin, Texas 78701-3218.

6. On information and belief, Micron Semiconductor is a corporation organized and existing under the laws of Idaho. On information and belief, Micron Semiconductor has a regular and established place of business at 805 Central Expressway South, Suite 100, Allen, Texas 75013. On information and belief, Micron Semiconductor is registered with the Texas Secretary of State to do business in Texas. On information and belief, Micron Semiconductor can be served through its registered agent, The Corporation Service Company, 211 E. 7th Street, Suite 620, Austin, Texas 78701-3218.

7. On information and belief, Micron Texas is a corporation organized and existing under the laws of Idaho. On information and belief, Micron Texas has a regular and established place of business at 805 Central Expressway South, Suite 100, Allen, Texas 75013. On information and belief, Micron Texas also has a regular and established place of business at 950 West Bethany Drive, Suite 120, Allen, Texas 75013-3837. On information and belief, Micron Texas is registered with the Texas Secretary of State to do business in Texas. On information and belief, Micron Texas can be served through its registered agent, The Corporation Service Company, 211 E. 7th Street, Suite 620, Austin, Texas, 78701-3218.

8. On information and belief, Micron Semiconductor and Micron Texas are wholly owned subsidiaries of Micron Technology. On information and belief, Micron Technology does not separately report revenue from Micron Semiconductor or Micron Texas in its filings to the Securities Exchange Commission, but rather reports combined revenue from its various products and subsidiaries.

9. On information and belief, Defendants have semiconductor fabrication plants in the United States and other countries throughout the world and manufacture memory products such as DRAM, NAND Flash, and NOR Flash at those plants. On information and belief, Defendants also use, sell, and offer for sale in the United States, import into the United States and/or export from the United States memory products, including DDR4 load reduced dual in-line memory modules ("LRDIMMs"), and DDR4 registered DIMMs ("RDIMMs"). On information and belief, Defendants have at least used, sold, or offered to sell products and services, including the Accused Instrumentalities, in this judicial district, *e.g.*, through sales and distribution channels managed by Micron Texas.

10. On information and belief, Defendants place, have placed, and contributed to placing Accused Instrumentalities into the stream of commerce via an established distribution

channel knowing or understanding that such products would be sold and used in the United States, including in this judicial district. On information and belief, Defendants have also derived substantial revenues from infringing acts in this judicial district, including from the sale and use of the Accused Instrumentalities.

II. JURISDICTION AND VENUE

11. The Court has subject matter jurisdiction under 28 U.S.C. § 1338, in that this action arises under federal statute, the patent laws of the United States (35 U.S.C. §§ 1, *et seq.*).

12. Each Defendant is subject to this Court's personal jurisdiction consistent with the principles of due process and/or the Texas Long Arm Statute.

13. Personal jurisdiction exists generally over the Defendants because each Defendant has sufficient minimum contacts and/or has engaged in continuous and systematic activities in the forum as a result of business conducted within the State of Texas and the Eastern District of Texas. Personal jurisdiction also exists over each Defendant because each, directly or through subsidiaries, makes, uses, sells, offers for sale, imports, advertises, makes available, and/or markets products within the State of Texas and the Eastern District of Texas that infringe one or more claims of the Patents-in-Suit. Further, on information and belief, Defendants have placed or contributed to placing infringing products into the stream of commerce knowing or understanding that such products would be sold and used in the United States, including in this District.

14. Venue is proper in this Court pursuant to 28 U.S.C. §§ 1391(b) and (c) and/or 1400(b) because Defendants (1) have committed and continue to commit acts of patent infringement in this District by, among other things, directly and/or indirectly making, using, selling, offering to sell, or importing products that infringe one or more claims of the Patents-in-Suit, and (2) have done and continue to do business in this District by maintaining regular and

established places of business, including at least at 805 Central Expressway South, Suite 100, Allen, Texas 75013.

III. FACTUAL ALLEGATIONS

Background

15. Since its founding in 2000, Netlist has been a leading innovator in high-performance memory module technologies. Netlist designs and manufactures a wide variety of high-performance products for the cloud computing, virtualization and high-performance computing markets. Netlist's technology enables users to derive useful information from vast amounts of data in a shorter period of time. These capabilities will become increasingly valuable as the volume of data continues to dramatically increase.

16. Netlist has a long history of being the first to market with disruptive new products such as the first LRDIMM, HyperCloud®, based on Netlist's distributed buffer architecture later adopted by the industry for DDR4 LRDIMM. Netlist was also the first to bring NAND flash to the memory channel with its NVvault® NVDIMM. These innovative products built on Netlist's early pioneering work in areas such as embedding passives into printed circuit boards to free up board real estate, doubling densities via quad-rank double data rate ("DDR") technology, and other off-chip technology advances that result in improved performance and lower costs compared to conventional memory.

17. The technologies disclosed and claimed in the Patents-in-Suit relate generally to memory modules. In many commercial products, a memory module is a printed circuit board that contains, among other components, a plurality of individual memory devices (such as DRAMs). The memory devices are typically arranged in "ranks," which are accessible by a processor or memory controller of the host system. A memory module is typically installed into a memory slot on a computer motherboard and serve as memory for computer systems.

18. Memory modules are designed for, among other things, use in servers such as those supporting cloud-based computing and other data-intensive applications (e.g. scaled data manipulation and aggregation, on-demand tracking, AI-based image analysis, weather patterning, etc.). The structure, function, and operation of memory modules is defined, specified, and standardized by the JEDEC Solid State Technology Association ("JEDEC"), the standard-setting body for the microelectronics industry. Memory modules are typically characterized by, among other things, the generation of DRAM on the module (*e.g.*, DDR4, DDR3) and the type of module (*e.g.*, RDIMM, LRDIMM).

19. Dual in-line memory modules ("DIMMs") are a type of memory module which generally includes SDRAMs mounted in a printed circuit board with other components, *e.g.*, serial presence detect ("SPD") and Hub with thermal sensors.

20. LRDIMMs are a type of memory module that generally include SDRAMs mounted on a printed circuit board. LRDIMMs typically also include an RCD for transmitting control and address signals to the SDRAMs and data buffers between the host controller and memory devices.

21. Netlist designs and manufactures a wide variety of high-performance products for the cloud computing, virtualization, and high-performance computing markets. Netlist's technology enables users to derive useful information from vast amounts of data in a shorter period of time. These capabilities will become increasingly valuable as the volume of data continues to dramatically increase.

The Asserted '912 Patent

22. The '912 patent is entitled "Memory Module Decoder." Netlist owns the '912 patent by assignment from the listed inventors Jayesh R. Bhakta and Jeffrey C. Solomon. The '912 patent was filed as Application No. 11/862,931 on September 27, 2007, issued as a patent on November 17, 2009, and claims priority to three provisional applications: Nos. 60/588,244 filed

on July 15, 2004 60/550,668 filed on March 5, 2004, and 60/575,595 filed on May 28, 2004. The '912 patent also claims priority to application, filed July 1, 2005, now U.S. Patent No. 7,289,386, which is a continuation-in-part of application No. 11/075,395, filed March 7, 2005, now U.S. Patent No. 7,286,436.

23. Micron has had actual knowledge of the '912 patent no later than April 28, 2021 via Exhibit A to Netlist's April 28, 2021 letter to Micron, and as of the filing of the original Complaint in this action.

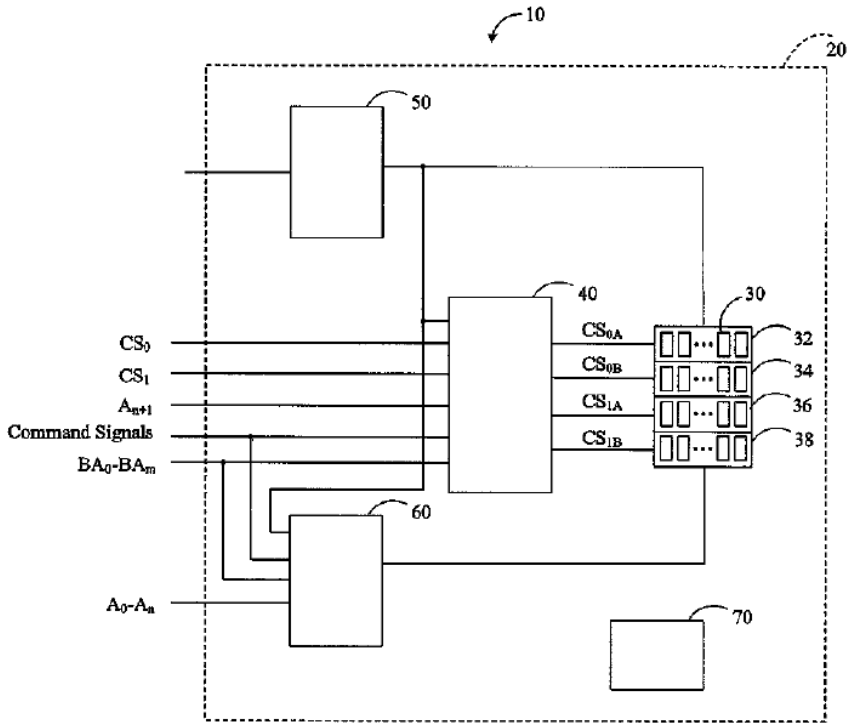
24. The '912 patent relates to memory module technology, and more specifically, to a concept called rank multiplication. A memory module is a device that contains individual memory devices arranged in "ranks" on a printed circuit board. At the time of the invention, most computer systems supported accessing only one or two ranks, limiting the number of ranks that can be added per memory module. Exhibit 1, 1:20-2:42.

25. The '912 patent teaches that one way to upgrade the memory capacity of a memory module is to use on-module logic to present a memory module with, *e.g.*, 2n physical ranks of memory devices, as a module with n (virtual) ranks to the computer system. *Id.*, 6:64-7:19. In this way, "even though the memory module 10 actually has the first number of [physical] ranks of memory devices 30, the memory module 10 simulates a virtual memory module by operating as having the second number of [logical or virtual] ranks of memory devices 30." *Id.*, 7:9-13. This technique is commonly referred to as "rank multiplication."

26. Rank multiplication allows a designer to expand the number of ranks and hence the total memory capacity on a memory module. It also enables them to construct a memory module of a given capacity using lower density memory devices that often cost less. *Id.*, 4:42-58, 22:5-14. For example, for the same 1 GB memory capacity, it could be more cost-effective to use thirty-

six 256-Mb DRAMs arranged in 4 ranks than eighteen 512-Mb DRAMs arranged in two ranks. *Id.*, 4:42-58, 4:59-5:5.

27. Figure 1A illustrates an example of a memory module with rank multiplication capability. The memory module has a register 60 and a logic element 40.



28. The logic element receives a set of input control signals from the computer system that include chip-select signals CS_0-CS_1, address signal A_{n+1}, and bank address signals BA_0-BA_m. *Id.*, 7:35-53; Fig. 1A. From the computer system's perspective, it is connected to only two ranks of memory devices, to be selected by CS_0 or CS_1, even though the memory devices are arranged in four physical ranks. *Id.*, 6:55-7:19. In response to the received input control signals, the logic element on the memory module generates a set of output control signals, corresponding to the four physical ranks of the memory devices. *Id.*, 6:61-63. The logic element 40 also receives command signals (such as read/write) from the computer system. *Id.*, 6:55-61, 7:46-53. In response to the command signal and the input signals, the logic element transmits the command signal to the

memory devices on the selected rank of the memory module. *Id.* In some embodiments, command signals are transmitted to only a single memory device on a multi-device rank at a time.

The Asserted '417 Patent

29. The '417 patent is entitled "Memory Module With Data Buffering." Netlist owns the '417 patent by assignment from the listed inventors Jayesh R. Bhakta and Jeffrey C. Solomon. The '417 patent was filed as Application No. 16/695,020 on November 25, 2019, issued as a patent on August 17, 2021, and claims priority to five provisional applications: Nos. 60/645,087, filed on January 19, 2005, 60/590,038, filed on July 21, 2004, 60/588,244 filed on July 15, 2004, 60/550,668 filed on March 5, 2004, and 60/575,595 filed on May 28, 2004.

30. Micron has had actual knowledge of the '417 patent at least as of the filing of the First Amended Complaint in this action.

31. The '417 patent relates to a memory module operable to communicate data with a memory controller via a N-bit wide memory bus, where the memory module includes memory devices arranged in a plurality of N-bit wide ranks, with logic that is configurable to receive a set of input address and control signals associated with a read or write memory command and output registered address and control signals and data buffer control signals. As summarized in the Abstract, the memory module further includes circuitry coupled between the memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, where the circuitry is configurable to "enable registered transfers of N-bit wide data signals associated with the memory read or write command between the N-bit wide memory bus and the memory devices in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module, which is greater than an actual operational CAS latency of the memory devices."

The Asserted '215 Patent

32. The '215 patent is entitled "Memory Module With Data Buffering." Netlist owns the '215 patent by assignment from the listed inventors Jayesh R. Bhakta and Jeffrey C. Solomon. The '215 patent was filed as Application No. 14/715,486 on May 18, 2015, issued as a patent on January 2, 2018, and claims priority to five provisional applications: Nos. 60/645,087, filed on January 19, 2005, 60/590,038, filed on July 21, 2004, 60/588,244 filed on July 15, 2004, 60/550,668 filed on March 5, 2004, and 60/575,595 filed on May 28, 2004.

33. Micron has had actual knowledge of the '215 patent no later than April 28, 2021 via Exhibit A to Netlist's April 28, 2021 letter to Micron, and as of the filing of the First Amended Complaint in this action.

34. The '215 patent relates to a memory module that is operable to communicate data with a memory controller via a memory bus in response to memory commands received from the memory controller. The memory module includes a plurality of memory integrated circuits arranged in ranks, at least one first memory integrated circuit in a first rank and at least one second memory integrated circuit in a second rank, and a buffer coupled between the at least one first memory integrated circuit and the memory bus and between the at least one second memory integrated circuit and the memory bus. As summarized in the Abstract, the "memory module further comprises logic providing first control signals to the buffer to enable communication of a first data burst between the memory controller and the at least one first memory integrated circuit through the buffer in response to a first memory command, and providing second control signals to the buffer to enable communication of a second data burst between the at least one second memory integrated circuit and the memory bus through the buffer in response to a second memory command."

Micron's Infringing Activities

35. Defendants are worldwide semiconductor solution providers that primarily manufacture semiconductor memory products such as DRAM, DIMMs, and MCP (Multi-Chip Package), such as HBM. Defendants develop, manufacture, sell, offer to sell, import into the United States and export from the United States memory components and memory modules (including semi-finished ones) designed for, among other things, use in servers such as those supporting cloud-based computing and other data-intensive applications as well as for use in consumer end products.

36. Netlist contacted Micron by letter dated April 28, 2021 requesting that it take a license; Micron has declined to take a license.

DDR4 Memory Modules

37. The accused DDR4 products include, without limitation, any Micron DDR4 LRDIMM and RDIMM products made in, sold in, offered for sale in, used in, exported from and/or imported into the United States by Micron. By way of non-limiting example, the accused DDR4 LRDIMM and RDIMM products include Micron products advertised on Micron's website that employ per DRAM addressability ("PDA"). As to the '912 patent, claim 16, the accused DDR4 LRDIMM and RDIMM products include all branded, alternatively branded and non-branded products by Micron that employ PDA. As to the other claims of the Patents-in-Suit, Micron is responsible for making, using, selling, offering to sell, and/or importing, without authority, infringing DDR4 LRDIMMS and other products that have materially the same structures and designs in relevant part. Collectively, these are the "Accused Products."

IV. FIRST CLAIM FOR RELIEF – '912 PATENT[1]

38. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this First Amended Complaint as if fully set forth herein.

39. On information and belief, Micron directly infringed and is currently infringing at least one claim of the '912 patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the Accused Products and other products with materially the same structures in relevant parts. An exemplary claim chart comparing claim 16 of the '912 patent to exemplary DDR4 LRDIMM and RDIMM Accused Products is attached hereto as Exhibit 4. As shown in Exhibit 4, accused DDR4 LRDIMMs and DDR4 RDIMMs, and other products with materially the same structures in relevant parts, infringe at least claim 16 of the '912 patent.

V. SECOND CLAIM FOR RELIEF – '417 PATENT

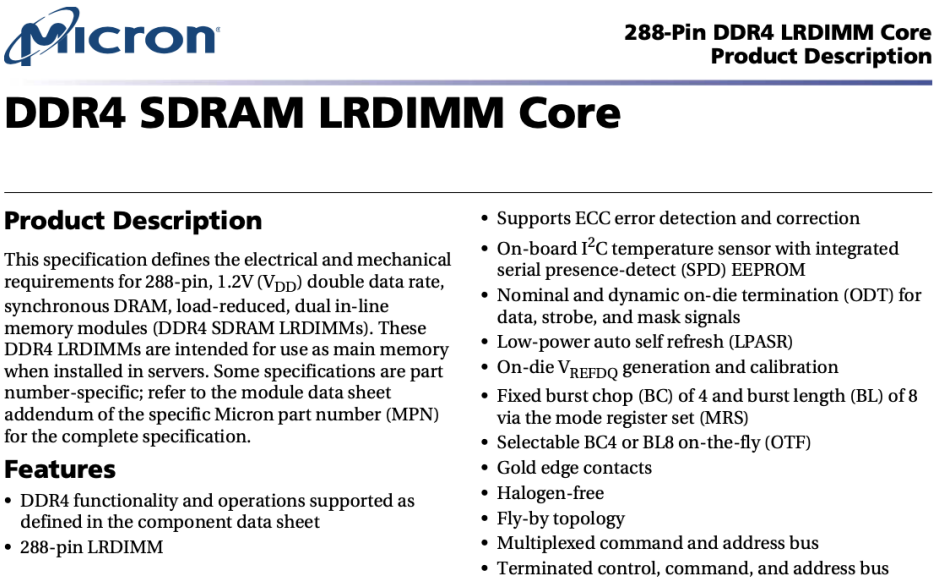
40. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this First Amended Complaint as if fully set forth herein.

41. On information and belief, Defendants directly infringed and are currently infringing at least one claim of the '417 patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the accused DDR4 LRDIMMs and other products with materially the same structures in relevant parts. For example and as shown below, the accused DDR4 LRDIMMs and other

[1] The claims asserted, and the theories set forth herein are based on Netlist's present understanding of Micron's Accused Instrumentality. Netlist reserves the right to supplement or amend these contentions as permitted by the Local Rules and any Orders of the Court as discovery progresses. Further, these contentions contain images and examples illustrating Netlist's infringement theories. As such, the images and examples are not intended, and should not be read, as narrowing or limiting the scope of these contentions.

products with materially the same structures in relevant parts infringe at least claim 1 of the '417 patent.

42. For example, to the extent the preamble is limiting, each of the accused DDR4 LRDIMMs comprise a memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide data bus in response to memory commands (e.g., read or write) received from the memory controller. *See* Micron Technologies, DRAM Modules, *available at* https://www.micron.com/products/dram-modules (last accessed: August 15, 2022). An example is depicted below.



Micron

288-Pin DDR4 LRDIMM Core
Product Description

DDR4 SDRAM LRDIMM Core

Product Description

This specification defines the electrical and mechanical requirements for 288-pin, 1.2V (V_{DD}) double data rate, synchronous DRAM, load-reduced, dual in-line memory modules (DDR4 SDRAM LRDIMMs). These DDR4 LRDIMMs are intended for use as main memory when installed in servers. Some specifications are part number-specific; refer to the module data sheet addendum of the specific Micron part number (MPN) for the complete specification.

Features

- DDR4 functionality and operations supported as defined in the component data sheet
- 288-pin LRDIMM
- Supports ECC error detection and correction
- On-board I^2C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- On-die V_{REFDQ} generation and calibration
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Multiplexed command and address bus
- Terminated control, command, and address bus

Exhibit 6 at 1 (Micron DDR4 SDRAM LRDIMM Core specification).

Table 5: Pin Descriptions

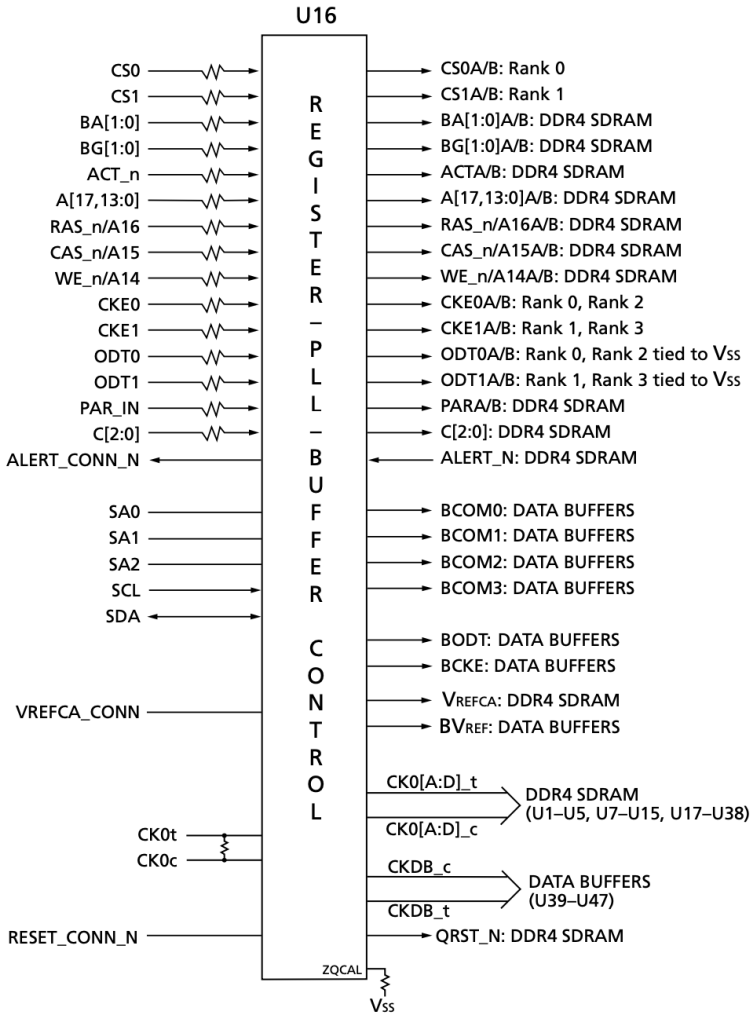
Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands in order to select one location out of the memory array in the respective bank (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, and RAS_n/A16 have additional functions; see individual entries in this table). The address inputs also provide the op-code during the MODE REGISTER SET command. A17 is only defined for x4 SDRAM.
A10/AP	Input	**Auto precharge:** A10 is sampled during READ and WRITE commands to determine whether an auto precharge should be performed on the accessed bank after a READ or WRITE operation (HIGH = auto precharge; LOW = no auto precharge). A10 is sampled during a PRECHARGE command to determine whether the precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	**Burst chop:** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH = no burst chop; LOW = burst chopped). See Command Truth Table in the DDR4 component data sheet.
ACT_n	Input	**Command input:** ACT_n defines the ACTIVATE command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 are considered as row address A16, A15, and A14. See Command Truth Table.
BAx	Input	**Bank address inputs:** Define the bank (with a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command.
BGx	Input	**Bank group address inputs:** Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. x16-based SDRAM only has BG0.
C0, C1, C2 (RDIMM/LRDIMM only)	Input	**Chip ID:** These inputs are used only when devices are stacked; that is, 2H, 4H, and 8H stacks for x4 and x8 configurations using through-silicon vias (TSVs). These pins are not used in the x16 configuration. Some DDR4 modules support a traditional DDP package, which uses CS1_n, CKE1, and ODT1 to control the second die. All other stack configurations, such as a 4H or 8H, are assumed to be single-load (initiator/target) type configurations where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT. Chip ID is considered part of the command code.
CKx_t CKx_c	Input	**Clock:** Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.
CKEx	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After V_{REFCA} has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET_n) are disabled during self refresh.
CSx_n	Input	**Chip select:** All commands are masked when CS_n is registered HIGH. CS_n provides external rank selection on systems with multiple ranks. CS_n is considered part of the command code (CS2_n and CS3_n are not used on UDIMMs).

Table 5: Pin Descriptions (Continued)

Symbol	Type	Description
ODTx	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT (R_{TT}) is applied only to each DQ, DQS_t, DQS_c, DM_n/DBI_n/TDQS_t, and TDQS_c signal for x4 and x8 configurations (when the TDQS function is enabled via the mode register). For the x16 configuration, R_{TT} is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, UDM_n, and LDM_n signal. The ODT pin will be ignored if the mode registers are programmed to disable R_{TT}.
PARITY	Input	**Parity for command and address:** This function can be enabled or disabled via the mode register. When enabled in MR5, the DRAM calculates parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG[1:0], BA[1:0], A[16:0]. Input parity should be maintained at the rising edge of the clock and at the same time as command and address with CS_n LOW.
RAS_n/A16 CAS_n/A15 WE_n/A14	Input	**Command inputs:** RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command and/or address being entered and have multiple functions. For example, for activation with ACT_n LOW, these are addresses like A16, A15, and A14, but for a non-activation command with ACT_n HIGH, these are command pins for READ, WRITE, and other commands defined in Command Truth Table.
RESET_n	CMOS Input	**Active LOW asynchronous reset:** Reset is active when RESET_n is LOW and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
SAx	Input	**Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I^2C bus.
DQx, CBx	I/O	**Data input/output and check bit input/output:** Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If cyclic redundancy checksum (CRC) is enabled via the mode register, the CRC code is added at the end of the data burst. Any one or all of DQ0, DQ1, DQ2, or DQ3 may be used for monitoring of internal V_{REF} level during test via mode register setting MR[4] A[4] = HIGH; training times change when enabled.
DM_n/DBI_n/ TDQS_t (DMU_n, DBIU_n), (DML_n/ DBIl_n)	I/O	**Input data mask and data bus inversion:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM is multiplexed with the DBI function by the mode register A10, A11, and A12 settings in MR5. For a x8 device, the function of DM or TDQS is enabled by the mode register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 device and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations (TDQS is not valid for UDIMMs).
SDA	I/O	**Serial Data:** Bidirectional signal used to transfer data in or out of the EEPROM or EEPROM/TS combo device.
DQS_t DQS_c DQSU_t DQSU_c DQSL_t DQSL_c	I/O	**Data strobe:** Output with read data, input with write data. Edge-aligned with read data, centered-aligned with write data. For x16 configurations, DQSL corresponds to the data on DQ[7:0], and DQSU corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0], respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.
ALERT_n	Output	**Alert output:** Possesses functions such as CRC error flag and command and address parity error flag as output signal. If a CRC error occurs, ALERT_n goes LOW for the period time interval and returns HIGH. If an error occurs during a command address parity check, ALERT_n goes LOW until the on-going DRAM internal recovery transaction is complete. During connectivity test mode, this pin functions as an input. Use of this signal is system-dependent. If not connected as signal, ALERT_n pin must be connected to V_{DD} on DIMMs.
EVENT_n	Output	**Temperature event:** The EVENT_n pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded. This pin has no function (NF) on modules without temperature sensors.

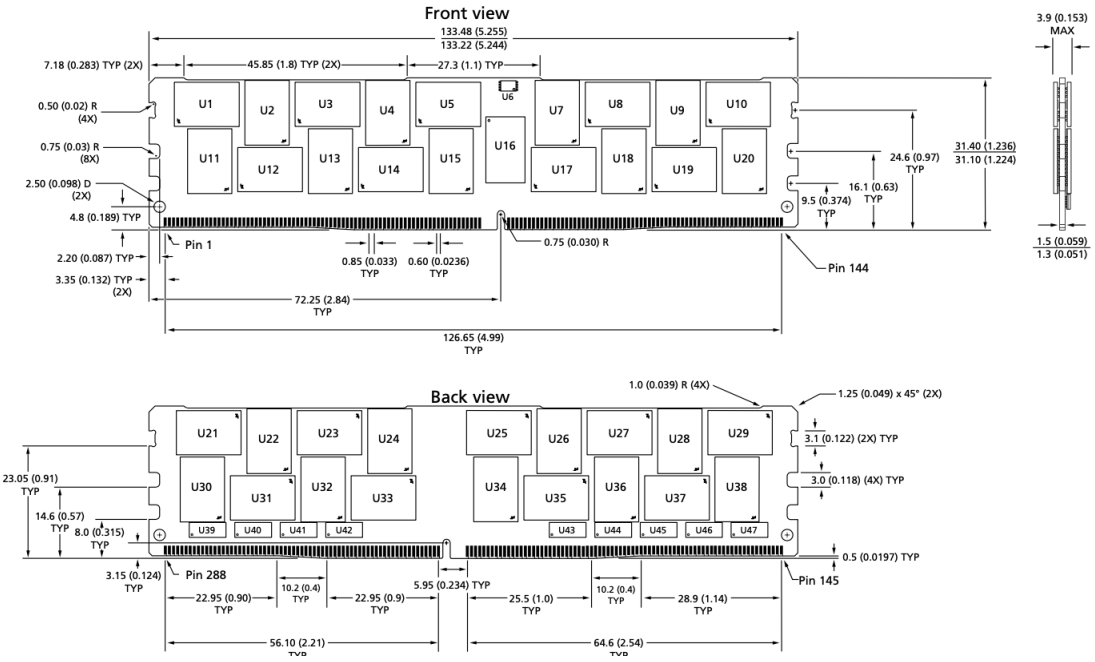
Id. at 6-7.

See also, e.g., Exhibit 5 (Micron MTA36ASF4G72LZ datasheet), at 9:



43. As shown above, the memory bus includes address (e.g., "Ax") and control signal lines (e.g., "CSx_n") and data signal lines (e.g., "DQx") connected via pins on the edge connection to the DIMM.

44. As shown above and below, the accused DDR4 LRDIMMs each comprise a printed circuit board ("PCB") having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system, with logic (e.g., DDR4 registering clock driver, or "RCD") coupled to the PCB.



Id. at 24 (depiction of a Micron DDR4 LRDIMM).

45. As shown below, the logic in each of the accused DDR4 LRDIMMs is configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals. The set of input address and control signals includes a plurality of input chip select signals and other input address and control signals. The plurality of input chip select signals include one chip select signal having an active signal value and one or more other input chip select signals each having a non-active signal value. The logic receives the chip select signals with one active value and one or more chip selects with a non-active value and outputs corresponding registered chip selects. As shown below, the set of registered address and control signals output by the logic include a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals and other registered address and control signals corresponding to respective ones of the other input address and control signals. The plurality of registered chip select signals include one registered chip select signal having an active signal value and one or more other registered chip select signals

each having a non-active signal value. *See, e.g.*, Exhibit 5 (Micron MTA36ASF4G72LZ datasheet), at 4-5 (depicted below) (input/output functional description for Micron DDR4 LRDIMMs, including input address and control signals associated with a read or write memory command); *see also, e.g.*, JEDEC DDR4 SDRAM Standard 79-4C (Exhibit 8), at 29 (Command Truth Table providing input address and control signals associated with memory commands)).

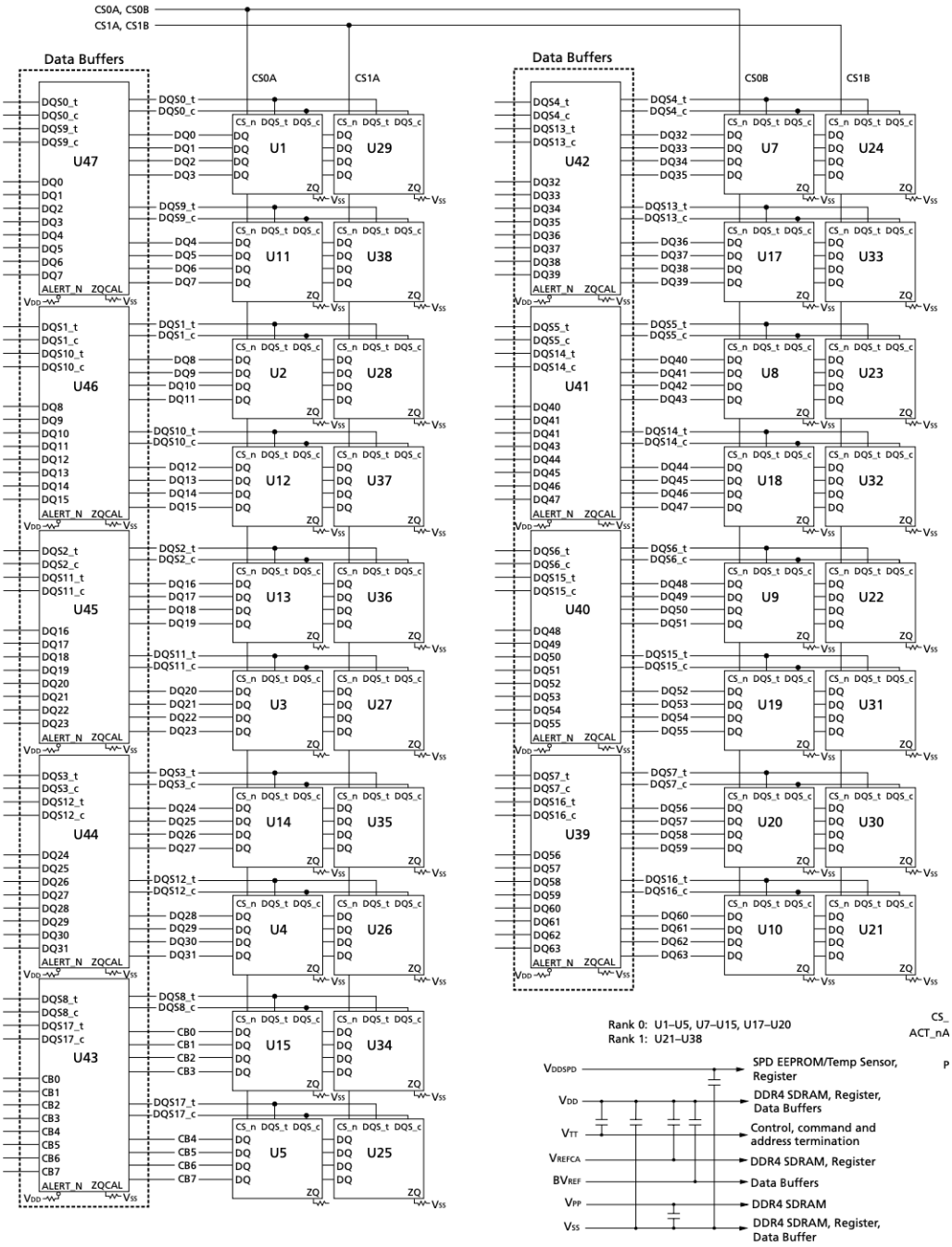
Table 5: Pin Descriptions

Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands in order to select one location out of the memory array in the respective bank (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, and RAS_n/A16 have additional functions; see individual entries in this table). The address inputs also provide the op-code during the MODE REGISTER SET command. A17 is only defined for x4 SDRAM.
A10/AP	Input	**Auto precharge:** A10 is sampled during READ and WRITE commands to determine whether an auto precharge should be performed on the accessed bank after a READ or WRITE operation (HIGH = auto precharge; LOW = no auto precharge). A10 is sampled during a PRECHARGE command to determine whether the precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	**Burst chop:** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH = no burst chop; LOW = burst- chopped). See Command Truth Table in the DDR4 component data sheet.
ACT_n	Input	**Command input:** ACT_n defines the ACTIVATE command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 are considered as row address A16, A15, and A14. See Command Truth Table.
BAx	Input	**Bank address inputs:** Define the bank (with a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command.
BGx	Input	**Bank group address inputs:** Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. x16-based SDRAM only has BG0.
C0, C1, C2 (RDIMM/LRDIMM only)	Input	**Chip ID:** These inputs are used only when devices are stacked; that is, 2H, 4H, and 8H stacks for x4 and x8 configurations using through-silicon vias (TSVs). These pins are not used in the x16 configuration. Some DDR4 modules support a traditional DDP package, which uses CS1_n, CKE1, and ODT1 to control the second die. All other stack configurations, such as a 4H or 8H, are assumed to be single-load (master/slave) type configurations where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT. Chip ID is considered part of the command code.
CKx_t CKx_c	Input	**Clock:** Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.
CKEx	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After V_{REFCA} has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET_n) are disabled during self refresh.
CSx_n	Input	**Chip select:** All commands are masked when CS_n is registered HIGH. CS_n provides external rank selection on systems with multiple ranks. CS_n is considered part of the command code (CS2_n and CS3_n are not used on UDIMMs).

Table 5: Pin Descriptions (Continued)

Symbol	Type	Description
ODTx	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT (R_{TT}) is applied only to each DQ, DQS_t, DQS_c, DM_n/DBI_n/TDQS_t, and TDQS_c signal for x4 and x8 configurations (when the TDQS function is enabled via the mode register). For the x16 configuration, R_{TT} is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, UDM_n, and LDM_n signal. The ODT pin will be ignored if the mode registers are programmed to disable R_{TT}.
PARITY	Input	**Parity for command and address:** This function can be enabled or disabled via the mode register. When enabled in MR5, the DRAM calculates parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG[1:0], BA[1:0], A[16:0]. Input parity should be maintained at the rising edge of the clock and at the same time as command and address with CS_n LOW.
RAS_n/A16 CAS_n/A15 WE_n/A14	Input	**Command inputs:** RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command and/or address being entered and have multiple functions. For example, for activation with ACT_n LOW, these are addresses like A16, A15, and A14, but for a non-activation command with ACT_n HIGH, these are command pins for READ, WRITE, and other commands defined in Command Truth Table.
RESET_n	CMOS Input	**Active LOW asynchronous reset:** Reset is active when RESET_n is LOW and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
SAx	Input	**Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I^2C bus.
DQx, CBx	I/O	**Data input/output and check bit input/output:** Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If cyclic redundancy checksum (CRC) is enabled via the mode register, the CRC code is added at the end of the data burst. Any one or all of DQ0, DQ1, DQ2, or DQ3 may be used for monitoring of internal V_{REF} level during test via mode register setting MR[4] A[4] = HIGH; training times change when enabled.
DM_n/DBI_n/ TDQS_t (DMU_n, DBIU_n), (DML_n/ DBIl_n)	I/O	**Input data mask and data bus inversion:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM is multiplexed with the DBI function by the mode register A10, A11, and A12 settings in MR5. For a x8 device, the function of DM or TDQS is enabled by the mode register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 device and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations (TDQS is not valid for UDIMMs).
SDA	I/O	**Serial Data:** Bidirectional signal used to transfer data in or out of the EEPROM or EEPROM/TS combo device.
DQS_t DQS_c DQSU_t DQSU_c DQSL_t DQSL_c	I/O	**Data strobe:** Output with read data, input with write data. Edge-aligned with read data, centered-aligned with write data. For x16 configurations, DQSL corresponds to the data on DQ[7:0], and DQSU corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0], respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.

Figure 2: Functional Block Diagram



Id. at 9.

See also, e.g., JEDEC 82-31A RCD Standard (Exhibit 9), at 2-3 (detailing the three basic modes of operation of the DDR4 RCD; as explained in the JEDEC 82-31A Standard, commands may be sent to a single rank, that is, one chip select has an active value, indicating that the selected rank is active, while the other one or more chip select signals have a non-active signal value):

Table 1 — Generic DCS - QxCS Mapping

Input CS	Output CS		
	Direct DualCS mode	Direct QuadCS mode	Encoded QuadCS mode
DCS0_n	QxCS0_n	QxCS0_n	QxCS0_n, QxCS1_n
DCS1_n	QxCS1_n	QxCS1_n	QxCS2_n, QxCS3_n
DCS2_n/DC0	n/a	QxCS2_n	n/a
DCS3_n/DC1	n/a	QxCS3_n	n/a

2.2.1 Direct CS Modes

Commands are sent to a single rank or multiple ranks, as determined by the DCS[n:0]_n and DC[n:0] inputs. The number of input chip selects matches the number of output chip selects in each of the two sets (A-outputs and B-outputs).

The number of input chip selects is two (in Direct DualCS mode) or four (in Direct QuadCS mode).

2.2.2 Quad CS Modes

For DIMMs using dual-die packages there is a need for four CS signals rather than the standard two. For these modules two modes are available where four CS outputs are available. The memory controller can select by programming the CS mode control bits which of the two modes it wants to utilize.

There are two ways of accomplishing this:

- by using four CS inputs from the host (DCS[3:0]_n). This is the Direct QuadCS mode. See Chapter 2.2.1, "Direct CS Modes," above.
- by using two CS inputs and one of the chip ID inputs from the host (DCS[1:0]_n and DC0). See Chapter 2.2.3, "Encoded QuadCS Mode," below.

2.2.3 Encoded QuadCS Mode

When F0RC0D DA[1:0] = 11 the DDR4 register decodes two sets of four QxCS_n outputs from two DCS_n inputs by using the DC0 as the encoding input.

Table 2 — DCS, DC - QxCS, QxC Mapping in Encoded QuadCS mode

DCS1_n	DCS0_n	DC0	DC2	QxCS[3:0]_n	QxC2
H	H	X	0	HHHH	No change
		X	1		
H	L	0	0	HHHL	0
		0	1		1
		1	0	HHLH	0
		1	1		1
L	H	0	0	HLHH	0
		0	1		1
		1	0	LHHH	0
		1	1		1
L	L	0	0	HLHL[1]	0
		0	1		1
		1	0	LHLH[1]	0
		1	1		1

1.Only one DCSx_n input can be asserted for DRAM MRS and DRAM read commands

46. The logic is further configurable to output data buffer control signals (e.g., BCOM[3:0]=1001 or BCOM[3:0]=1000) in response to the read or write memory command, e.g., via the data buffer control bus BCOM[3:0] bus. *See, e.g.*, JEDEC 82-32A Data Buffer Standard (Exhibit 7), at 3-4:

2.4 Data Buffer Control Bus

This section describes the signals used in the DDR4 LRDIMM control bus that connects the DDR4 Register with each of the nine DDR4 data buffers (DDR4DB02).

2.4.1 Control Bus Signals

Table 2 — List of Signals for Data Buffer control

Name	Description	Signal Count
BCOM[3:0]	Data buffer command signals	4
BCKE	Function of registered DCKE (dedicated non-encoded signal)	1
BODT	Function of registered DODT (dedicated non-encoded signal)	1
BCK_t, BCK_c	Input clock	2
BVrefCA	Reference voltage for command and control signals	1
	Total	9

2.4.2 Command List

Table 3 — DDR4 Data Buffer Command Table

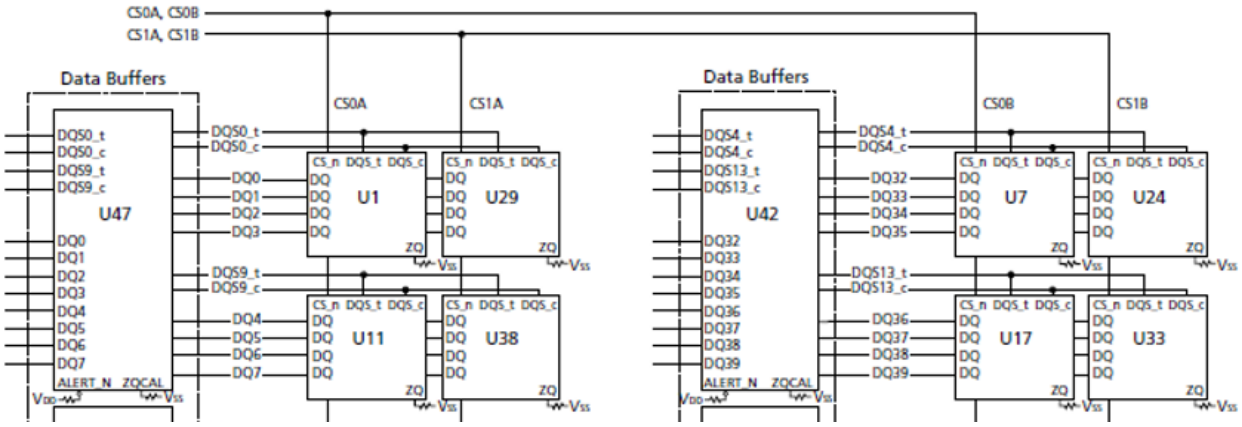
Command	Description	BCOM[3:0] Encoding
WR	Write BC4 or BC8 (fixed or on the fly) or BC10 (with CRC enabled) and send accessed rank ID and BL information in the next command time slot, followed by parity in the last command time slot.	1000
RD	Read BC4 or BC8 (fixed or on the fly) and send accessed rank ID and BL information in the next command time slot, followed by parity in the last command time slot.	1001
MRS Write	Send MRS Write bits snooped by DDR4 Register and the MRS ID in the following six command time slots, followed by parity in the last command time slot.	1011
BCW Write	Write buffer control word data in the next five command slots, followed by parity in the last command time slot.	1100
BCW Read	Read buffer control word address in the four command slots, followed by parity in the last command time slot.	1101
RFU[1]	Reserved for future use	1110
RFU[1]	Reserved for future use	1111
NOP	Idle, do nothing	1010

1. RFU commands are treated as NOP commands for command sequence error detection

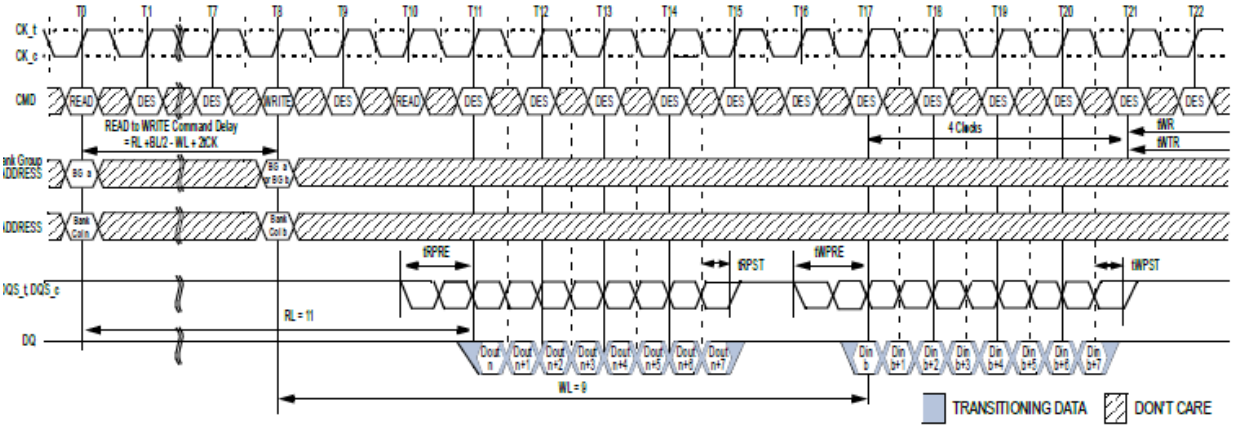
47. As shown above, the accused DDR4 LRDIMMs further comprise memory devices (e.g., SDRAMs) mounted on the PCB and arranged in a plurality of N-bit wide ranks, which correspond to respective ones of the plurality of registered chip select signals such that each of the

plurality of registered chip select signals is received by memory devices on respective N-bit wide ranks. *See, e.g.*, Exhibit 5 (Micron MTA36ASF4G72LZ datasheet), at 9:

Figure 2: Functional Block Diagram



See also, e.g., JEDEC DDR4 SDRAM Standard 79-4C (Exhibit 8), at 105, 122 (examples of read/write burst operations):

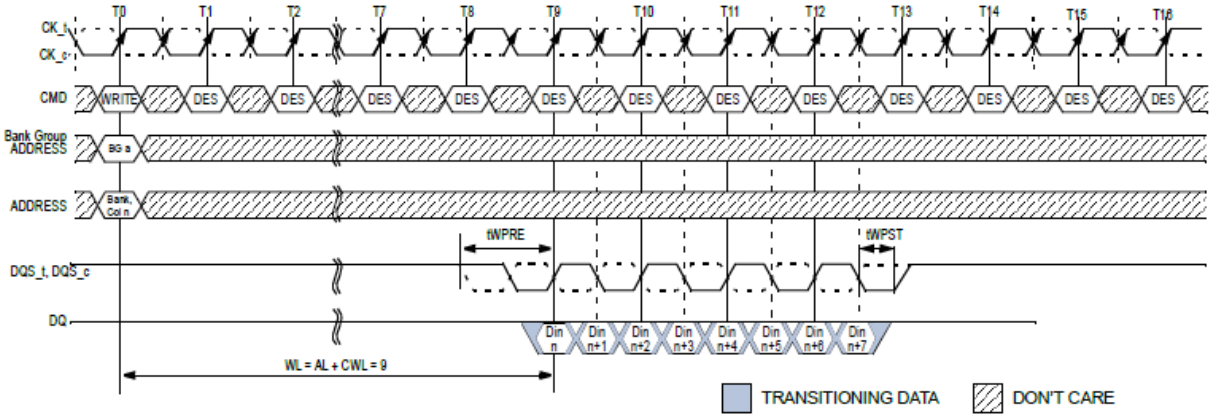


OTE 1 BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL =9 (CWL = 9, AL = 0), Write Preamble = 1tCK
OTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.
OTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
OTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and WRITE command at T8.
OTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 98 — READ (BL8) to WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group

4.25.5 Write Burst Operation

The following write timing diagram is to help understanding of each write parameter's meaning and just examples. The details of the definition of each parameter will be defined separately.
In these write timing diagram, CK and DQS are shown aligned and also DQS and DQ are shown center aligned for illustration purpose.



NOTE 1 BL = 8, WL = 9, AL = 0, CWL = 9, Preamble = 1tCK
NOTE 2 DIN n = data-in to column n.
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.
NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

Figure 128 — WRITE Burst Operation WL = 9 (AL = 0, CWL = 9, BL8)

48. The accused DDR4 LRDIMMs each include circuitry (e.g., DDR4 data buffers) coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks.

Figure 2: Functional Block Diagram

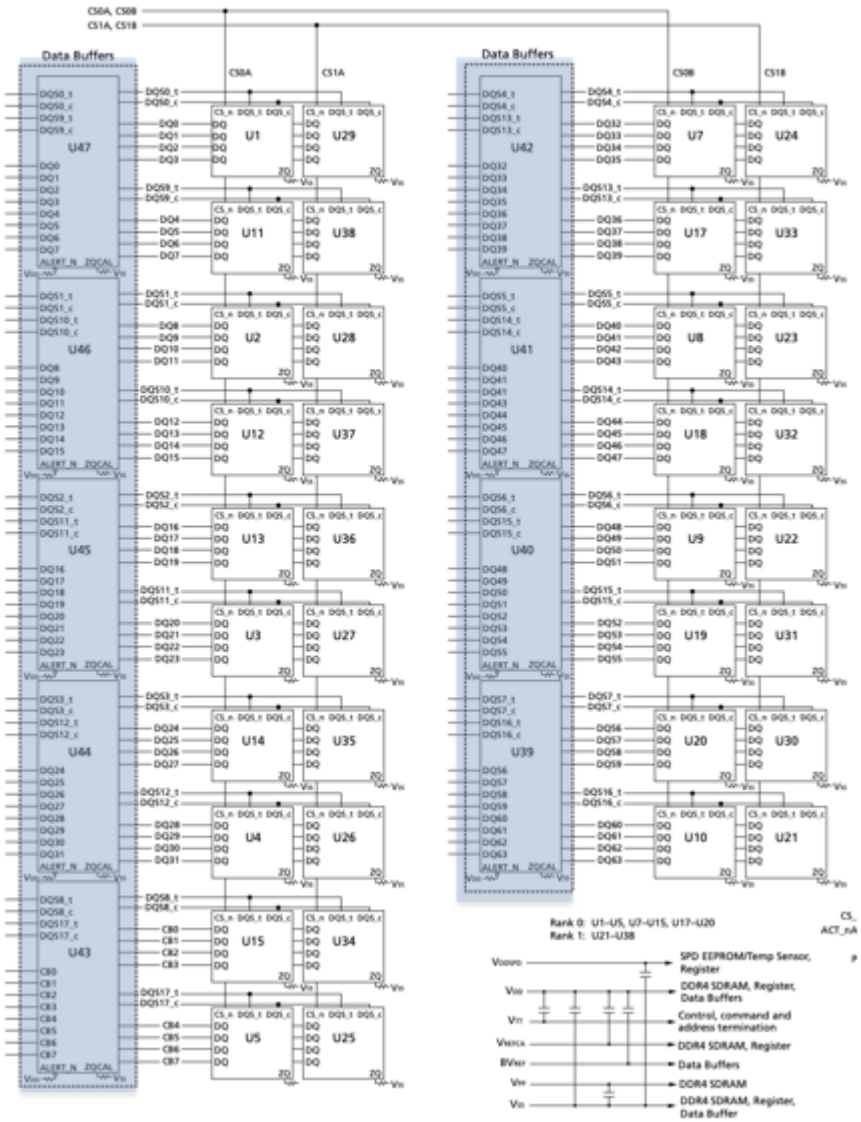


Exhibit 5 (Micron MTA36ASF4G72LZ datasheet), at 9.

4.61 Logic Diagram

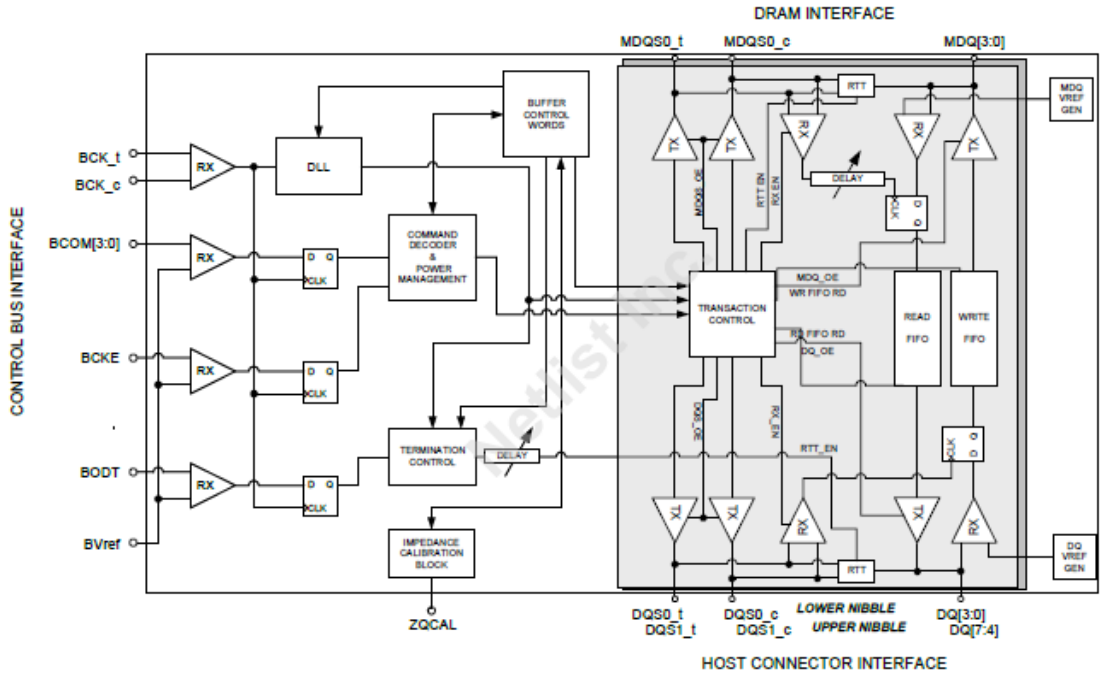


Figure 15 — Logic Diagram

JEDEC 82-32A Data Buffer Standard (Exhibit 7), at 95 (exemplary logic diagram of DDR4 data buffer circuitry).

49. In each of the accused DDR4 LRDIMMs, the circuitry (e.g., DDR4 data buffer) is configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals (e.g., BCOM[3:0]=1001 or BCOM[3:0]=1000) and in accordance with an overall CAS latency of the memory module. *See, e.g.*, JEDEC 82-32A Data Buffer Standard (Exhibit 7), at 12, 14:

Table 4 — Multicycle Sequence for Write Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	WR	Write command BCOM[3:0] = 1000
2	DAT0	Transfer the rank ID for write command BCOM[1:0] = {RANK_ID[1:0]} for DRAM writes Burst length information for Write data BCOM[3:2] = {0, 0} for BC4 BCOM[3:2] = {0, 1} for BC8
3	PAR[3:0]	Even parity bits for WR command and data PAR[x]: Parity bit for previous two BCOM[x] transfers
4	Next Cmd	Next Command

Table 5 — Multi-cycle Sequence for Read Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	RD	Read command BCOM[3:0] = 1001
2	DAT0	Transfer the rank ID for read command or the MPR selection ID in MPR override read mode BCOM[1:0] = {RANK_ID[1:0]} for DRAM reads BCOM[1:0] = {BA1, BA0} for MPR override reads Burst length information for Read data BCOM[3:0] = {0, 0} for BC4[1] BCOM[3:0] = {0, 1} for BC8
3	PAR[3:0]	Even parity bits for RD command and data PAR[x]: Parity bit for previous two BCOM[x] transfers
4	Next Cmd	Next Command

1. BC4 is not supported for MPR override reads

The overall CAS latency of the memory module may be expressed as shown below in the following equations:

2.5.4 Command Sequence Descriptions

The timing diagrams in this section show only the lower nibble of the DDR4RCD02. The same timing relationships apply independently also for the upper nibble. The timing diagrams only show the case of burst length = 8 and preamble = 1 nCK but equivalent timing relationships exist for burst length = 4 & 10 and preamble = 2 nCK.

For readability reasons, the timing diagrams use the abbreviations DB_RL and DB_WL for the latency between first cycle of RD command and the first rising edge of MDQS at DDR4DB02 inputs and for the latency between first cycle of WR command and the first rising edge of MDQS at DDR4DB02 outputs respectively. Both DB_RL and DB_WL include full cycle and fractional cycle delays. The equations for these latencies are as follows:

$DB\_WL(R)^1 = CWL + AL + PL + DWL(R)$

$DB\_RL(R)^2 = CL + AL + PL + MRE(R) + tRPRE/2$

tRPRE/2 exists in DB_RL since the host will adjust the receive enable delay MRE(R) to place it in the center of the read preamble.

For the detailed equations for DWL and MRE refer to the DDR4DB02 specification.

The DDR4RCD02 delays tPDM_RD and tPDM_WR are defined as the delay between first rising edge of MDQS and the first rising edge of DQS for a RD command and as the delay between first rising edge of DQS and the first rising edge of MDQS for a WR command respectively. By default these delays are constant per DDR4RCD02 for all ranks and nibbles.

---

1. This equation assumes that the DDR4 data buffer MDQ-MDQS Write Delay Control Words in F[3:0]BC8x/ F[3:0]BC9x are at their default power-on setting.
2. This equation assumes that the DDR4 data buffer MDQS Read Delay Control Words in F[3:0]BC4x/ F[3:0]BC5x are at their default power-on setting.

JEDEC 82-31A RCD Standard (Exhibit 9), at 15.

50. The data transfers through the circuitry (e.g., DDR4 data buffer) are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices. As an example, the overall CAS latency of the memory module may be expressed as shown below.

2.12 Command Sequence Descriptions

To accommodate the worst case DRAM CAS Latency, Additive Latency and Parity Latency, a DB is required to support a queue depth of 12 commands on the BCOM bus for data rates up to 2400MT/s.

The timing diagrams in this section show only the lower nibble of the DDR4DB02. The same timing relationships apply independently also for the upper nibble. The timing diagrams only show the case of burst length = 8 and preamble = 1 nCK but equivalent timing relationships exist for burst length = 4 & 10 and preamble = 2 nCK.

For readability reasons, the timing diagrams use the abbreviations DB_RL and DB_WL for the latency between first cycle of RD command and the first rising edge of MDQS at DDR4DB02 inputs and for the latency between first cycle of WR command and the first rising edge of MDQS at DDR4DB02 outputs respectively. Both DB_RL and DB_WL include full cycle and fractional cycle delays. The equations for these latencies are as follows:

$DB\_WL(R)^1 = CWL + AL + PL + DWL(R)$

$DB\_RL(R)^2 = CL + AL + PL + MRE(R) + tRPRE/2$

The equations for DWL and MRE for Ranks 0 to 3 are listed below.

where xxx[R].l and xxx[R].u are the equations for the lower and upper nibbles respectively

DWL[0].l = (F0BCDx[2:0] * 64 + F0BCAx[5:0]) * tCK/64

DWL[0].u = (F0BCDx[6:4] * 64 + F0BCBx[5:0]) * tCK/64

DWL[1].l = (F1BCDx[2:0] * 64 + F1BCAx[5:0]) * tCK/64

DWL[1].u = (F1BCDx[6:4] * 64 + F1BCBx[5:0]) * tCK/64

DWL[2].l = (F0BCFx[2:0] * 64 + F2BCAx[5:0]) * tCK/64

DWL[2].u = (F0BCFx[6:4] * 64 + F2BCBx[5:0]) * tCK/64

DWL[3].l = (F1BCFx[2:0] * 64 + F3BCAx[5:0]) * tCK/64

DWL[3].u = (F1BCFx[6:4] * 64 + F3BCBx[5:0]) * tCK/64

MRE[0].l = (F0BCCx[2:0] * 64 + F0BC2x[5:0]) * tCK/64

MRE[0].u = (F0BCCx[6:4] * 64 + F0BC3x[5:0]) * tCK/64

MRE[1].l = (F1BCCx[2:0] * 64 + F1BC2x[5:0]) * tCK/64

MRE[1].u = (F1BCCx[6:4] * 64 + F1BC3x[5:0]) * tCK/64

MRE[2].l = (F0BCEx[2:0] * 64 + F2BC2x[5:0]) * tCK/64

MRE[2].u = (F0BCEx[6:4] * 64 + F2BC3x[5:0]) * tCK/64

MRE[2].l = (F1BCEx[2:0] * 64 + F3BC2x[5:0]) * tCK/64

MRE[2].u = (F1BCEx[6:4] * 64 + F3BC3x[5:0]) * tCK/64

tRPRE/2 exists in DB_RL since the host will adjust the receive enable delay MRE(R) to place it in the center of the read preamble.

The DDR4DB02 delays tPDM_RD and tPDM_WR are defined as the delay between first rising edge of MDQS and the first rising edge of DQS for a RD command and as the delay between first rising edge of DQS and the first rising edge of MDQS for a WR command respectively. By default these delays are constant per DDR4DB02 for all ranks and nibbles.

JEDEC 82-32A Data Buffer Standard (Exhibit 7), at 11-12.

51. On information and belief, Micron also indirectly infringes the '417 patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as Micron's customers and end users, in this District and elsewhere in the United States. For example, on information

and belief, Micron has induced, and currently induces, the infringement of the '417 patent through its affirmative acts of selling, offering to sell, distributing, and/or otherwise making available the accused DDR4 LRDIMM products and other materially similar products that infringe the '417 patent. On information and belief, Micron provides specifications, datasheets, instruction manuals, and/or other materials that encourage and facilitate infringing use of the accused DDR4 LRDIMM products and other materially similar products by users in a manner that it knows or should have known would result in infringement and with the intent of inducing infringement.

52. On information and belief, Micron also indirectly infringes the '417 patent, as provided in 35 U.S.C. § 271(c), contributing to direct infringement committed by others, such as customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Micron has contributed to, and currently contributes to, Micron's customers and end-users infringement of the '417 patent through its affirmative acts of selling and offering to sell, in this District and elsewhere in the United States, the accused DDR4 LRDIMM products and other materially similar products that infringe the '417 patent. On information and belief, the accused DDR4 LRDIMM and other materially similar products have no substantial noninfringing use, and constitute a material part of the patented invention. On information and belief, Micron is aware that the product or process that includes the accused DDR4 LRDIMM products and other materially similar products would be covered by one or more claims of the '417 patent. On information and belief, the use of the product or process that includes the accused DDR4 LRDIMM products infringes at least one claim of the '417 patent.

53. Micron's infringement of the '417 patent has damaged and will continue to damage Netlist. Micron has had actual notice of the '417 patent at least as of the filing of the First Amended Complaint in this action. Micron's infringement of the '417 patent has been continuing and willful. Micron continues to commit acts of infringement despite a high likelihood that its actions

constitute infringement, and Micron knew or should have known that its actions constituted an unjustifiably high risk of infringement.

VI. THIRD CLAIM FOR RELIEF – '215 PATENT

54. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this First Amended Complaint as if fully set forth herein.

55. On information and belief, Defendants directly infringed and are currently infringing at least one claim of the '215 patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the accused DDR4 LRDIMMs and other products with materially the same structures in relevant parts. For example and as shown below, the accused DDR4 LRDIMMs and other products with materially the same structures in relevant parts infringe at least claim 1 of the '215 patent.

56. For example, to the extent the preamble is limiting, the accused DDR4 LRDIMMs comprise a memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller. *See* Micron Technologies, DRAM Modules, *available at* https://www.micron.com/products/dram-modules (last accessed: August 15, 2022). An example is depicted below.

DDR4 SDRAM LRDIMM Core

Product Description

This specification defines the electrical and mechanical requirements for 288-pin, 1.2V (V_{DD}) double data rate, synchronous DRAM, load-reduced, dual in-line memory modules (DDR4 SDRAM LRDIMMs). These DDR4 LRDIMMs are intended for use as main memory when installed in servers. Some specifications are part number-specific; refer to the module data sheet addendum of the specific Micron part number (MPN) for the complete specification.

Features

- DDR4 functionality and operations supported as defined in the component data sheet
- 288-pin LRDIMM
- Supports ECC error detection and correction
- On-board I^2C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- On-die V_{REFDQ} generation and calibration
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Multiplexed command and address bus
- Terminated control, command, and address bus

Exhibit 6 at 1 (Micron DDR4 SDRAM LRDIMM Core specification).

Table 5: Pin Descriptions

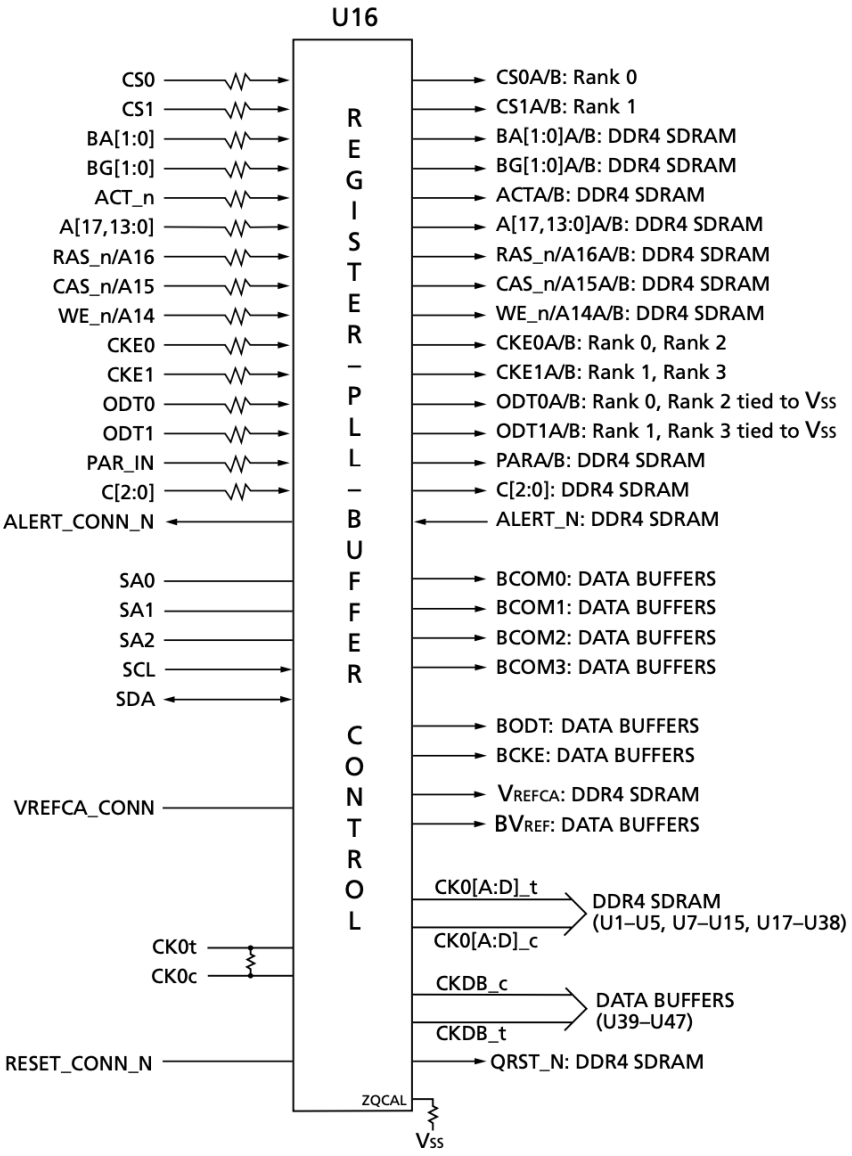
Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands in order to select one location out of the memory array in the respective bank (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, and RAS_n/A16 have additional functions; see individual entries in this table). The address inputs also provide the op-code during the MODE REGISTER SET command. A17 is only defined for x4 SDRAM.
A10/AP	Input	**Auto precharge:** A10 is sampled during READ and WRITE commands to determine whether an auto precharge should be performed on the accessed bank after a READ or WRITE operation (HIGH = auto precharge; LOW = no auto precharge). A10 is sampled during a PRECHARGE command to determine whether the precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	**Burst chop:** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH = no burst chop; LOW = burst chopped). See Command Truth Table in the DDR4 component data sheet.
ACT_n	Input	**Command input:** ACT_n defines the ACTIVATE command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 are considered as row address A16, A15, and A14. See Command Truth Table.
BAx	Input	**Bank address inputs:** Define the bank (with a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command.
BGx	Input	**Bank group address inputs:** Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. x16-based SDRAM only has BG0.
C0, C1, C2 (RDIMM/LRDIMM only)	Input	**Chip ID:** These inputs are used only when devices are stacked; that is, 2H, 4H, and 8H stacks for x4 and x8 configurations using through-silicon vias (TSVs). These pins are not used in the x16 configuration. Some DDR4 modules support a traditional DDP package, which uses CS1_n, CKE1, and ODT1 to control the second die. All other stack configurations, such as a 4H or 8H, are assumed to be single-load (initiator/target) type configurations where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT. Chip ID is considered part of the command code.
CKx_t CKx_c	Input	**Clock:** Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.
CKEx	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After V_{REFCA} has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET_n) are disabled during self refresh.
CSx_n	Input	**Chip select:** All commands are masked when CS_n is registered HIGH. CS_n provides external rank selection on systems with multiple ranks. CS_n is considered part of the command code (CS2_n and CS3_n are not used on UDIMMs).

Table 5: Pin Descriptions (Continued)

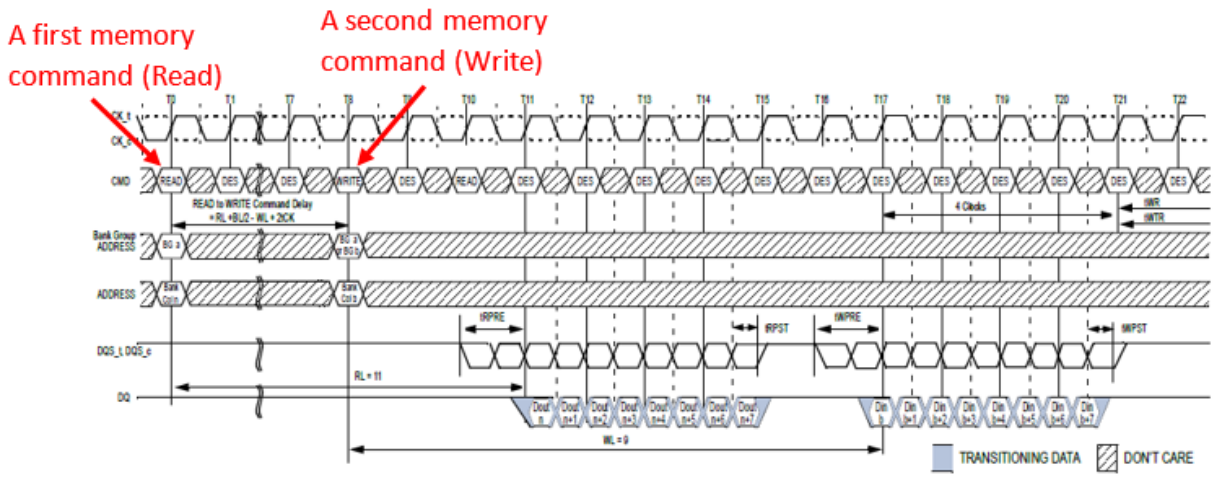
Symbol	Type	Description
ODTx	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT (R_{TT}) is applied only to each DQ, DQS_t, DQS_c, DM_n/DBI_n/TDQS_t, and TDQS_c signal for x4 and x8 configurations (when the TDQS function is enabled via the mode register). For the x16 configuration, R_{TT} is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, UDM_n, and LDM_n signal. The ODT pin will be ignored if the mode registers are programmed to disable R_{TT}.
PARITY	Input	**Parity for command and address:** This function can be enabled or disabled via the mode register. When enabled in MR5, the DRAM calculates parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG[1:0], BA[1:0], A[16:0]. Input parity should be maintained at the rising edge of the clock and at the same time as command and address with CS_n LOW.
RAS_n/A16 CAS_n/A15 WE_n/A14	Input	**Command inputs:** RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command and/or address being entered and have multiple functions. For example, for activation with ACT_n LOW, these are addresses like A16, A15, and A14, but for a non-activation command with ACT_n HIGH, these are command pins for READ, WRITE, and other commands defined in Command Truth Table.
RESET_n	CMOS Input	**Active LOW asynchronous reset:** Reset is active when RESET_n is LOW and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
SAx	Input	**Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I^2C bus.
DQx, CBx	I/O	**Data input/output and check bit input/output:** Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If cyclic redundancy checksum (CRC) is enabled via the mode register, the CRC code is added at the end of the data burst. Any one or all of DQ0, DQ1, DQ2, or DQ3 may be used for monitoring of internal V_{REF} level during test via mode register setting MR[4] A[4] = HIGH; training times change when enabled.
DM_n/DBI_n/ TDQS_t (DMU_n, DBIU_n), (DML_n/ DBIl_n)	I/O	**Input data mask and data bus inversion:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM is multiplexed with the DBI function by the mode register A10, A11, and A12 settings in MR5. For a x8 device, the function of DM or TDQS is enabled by the mode register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 device and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations (TDQS is not valid for UDIMMs).
SDA	I/O	**Serial Data:** Bidirectional signal used to transfer data in or out of the EEPROM or EEPROM/TS combo device.
DQS_t DQS_c DQSU_t DQSU_c DQSL_t DQSL_c	I/O	**Data strobe:** Output with read data, input with write data. Edge-aligned with read data, centered-aligned with write data. For x16 configurations, DQSL corresponds to the data on DQ[7:0], and DQSU corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0], respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.
ALERT_n	Output	**Alert output:** Possesses functions such as CRC error flag and command and address parity error flag as output signal. If a CRC error occurs, ALERT_n goes LOW for the period time interval and returns HIGH. If an error occurs during a command address parity check, ALERT_n goes LOW until the on-going DRAM internal recovery transaction is complete. During connectivity test mode, this pin functions as an input. Use of this signal is system-dependent. If not connected as signal, ALERT_n pin must be connected to V_{DD} on DIMMs.
EVENT_n	Output	**Temperature event:** The EVENT_n pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded. This pin has no function (NF) on modules without temperature sensors.

Id. at 6-7.

See also, e.g., Exhibit 5 (Micron MTA36ASF4G72LZ datasheet), at 9:



57. The memory commands may include a first memory command and a subsequent second memory command, where the first memory command causes the memory module to receive or output a first data burst, and the second memory command causes the memory module to receive or output a second data burst, for example, as illustrated in the exemplary waveform and timing diagrams below.



NOTE 1 BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL =9 (CWL = 9, AL = 0), Write Preamble = 1tCK
NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and WRITE command at T8.
NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 98 — READ (BL8) to WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group

JEDEC DDR4 SDRAM Standard 79-4C (Exhibit 8), at 105; *see also, e.g., id.*, §§ 4.24-4.25 (waveform and timing diagrams for JEDEC-standardized read and write operations). *See also, e.g.*, Exhibit 5 (Micron MTA36ASF4G72LZ datasheet), at 4-5 (depicted below) (input/output functional description for Micron DDR4 LRDIMMs, including input address and control signals associated with a read or write memory command); *see also, e.g.*, JEDEC DDR4 SDRAM Standard 79-4C (Exhibit 8), at 29 (Command Truth Table providing input address and control signals associated with memory commands)).

Table 5: Pin Descriptions

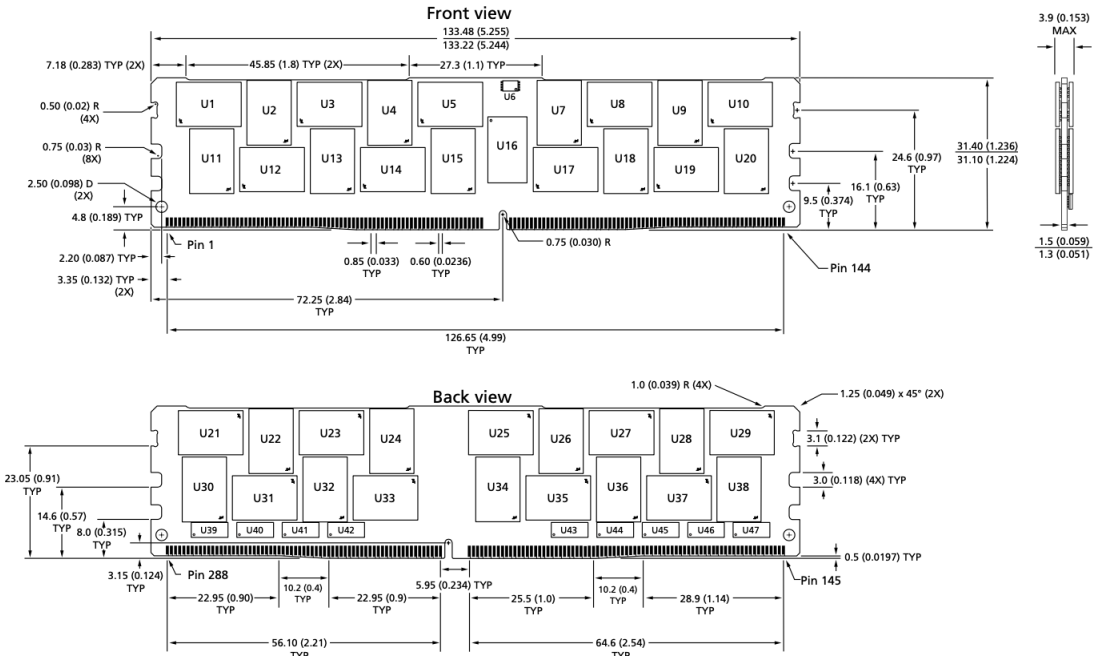
Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands in order to select one location out of the memory array in the respective bank (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, and RAS_n/A16 have additional functions; see individual entries in this table). The address inputs also provide the op-code during the MODE REGISTER SET command. A17 is only defined for x4 SDRAM.
A10/AP	Input	**Auto precharge:** A10 is sampled during READ and WRITE commands to determine whether an auto precharge should be performed on the accessed bank after a READ or WRITE operation (HIGH = auto precharge; LOW = no auto precharge). A10 is sampled during a PRECHARGE command to determine whether the precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	**Burst chop:** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH = no burst chop; LOW = burst- chopped). See Command Truth Table in the DDR4 component data sheet.
ACT_n	Input	**Command input:** ACT_n defines the ACTIVATE command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 are considered as row address A16, A15, and A14. See Command Truth Table.
BAx	Input	**Bank address inputs:** Define the bank (with a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command.
BGx	Input	**Bank group address inputs:** Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. x16-based SDRAM only has BG0.
C0, C1, C2 (RDIMM/LRDIMM only)	Input	**Chip ID:** These inputs are used only when devices are stacked; that is, 2H, 4H, and 8H stacks for x4 and x8 configurations using through-silicon vias (TSVs). These pins are not used in the x16 configuration. Some DDR4 modules support a traditional DDP package, which uses CS1_n, CKE1, and ODT1 to control the second die. All other stack configurations, such as a 4H or 8H, are assumed to be single-load (master/slave) type configurations where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT. Chip ID is considered part of the command code.
CKx_t CKx_c	Input	**Clock:** Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.
CKEx	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After V_{REFCA} has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET_n) are disabled during self refresh.
CSx_n	Input	**Chip select:** All commands are masked when CS_n is registered HIGH. CS_n provides external rank selection on systems with multiple ranks. CS_n is considered part of the command code (CS2_n and CS3_n are not used on UDIMMs).

Table 5: Pin Descriptions (Continued)

Symbol	Type	Description
ODTx	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT (R_{TT}) is applied only to each DQ, DQS_t, DQS_c, DM_n/ DBI_n/TDQS_t, and TDQS_c signal for x4 and x8 configurations (when the TDQS function is enabled via the mode register). For the x16 configuration, R_{TT} is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, UDM_n, and LDM_n signal. The ODT pin will be ignored if the mode registers are programmed to disable R_{TT}.
PARITY	Input	**Parity for command and address:** This function can be enabled or disabled via the mode register. When enabled in MR5, the DRAM calculates parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG[1:0], BA[1:0], A[16:0]. Input parity should be maintained at the rising edge of the clock and at the same time as command and address with CS_n LOW.
RAS_n/A16 CAS_n/A15 WE_n/A14	Input	**Command inputs:** RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command and/or address being entered and have multiple functions. For example, for activation with ACT_n LOW, these are addresses like A16, A15, and A14, but for a non-activation command with ACT_n HIGH, these are command pins for READ, WRITE, and other commands defined in Command Truth Table.
RESET_n	CMOS Input	**Active LOW asynchronous reset:** Reset is active when RESET_n is LOW and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
SAx	Input	**Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I^2C bus.
DQx, CBx	I/O	**Data input/output and check bit input/output:** Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If cyclic redundancy checksum (CRC) is enabled via the mode register, the CRC code is added at the end of the data burst. Any one or all of DQ0, DQ1, DQ2, or DQ3 may be used for monitoring of internal V_{REF} level during test via mode register setting MR[4] A[4] = HIGH; training times change when enabled.
DM_n/DBI_n/ TDQS_t (DMU_n, DBIU_n), (DML_n/ DBIl_n)	I/O	**Input data mask and data bus inversion:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM is multiplexed with the DBI function by the mode register A10, A11, and A12 settings in MR5. For a x8 device, the function of DM or TDQS is enabled by the mode register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/ output after inversion inside the DDR4 device and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations (TDQS is not valid for UDIMMs).
SDA	I/O	**Serial Data:** Bidirectional signal used to transfer data in or out of the EEPROM or EEPROM/TS combo device.
DQS_t DQS_c DQSU_t DQSU_c DQSL_t DQSL_c	I/O	**Data strobe:** Output with read data, input with write data. Edge-aligned with read data, centered-aligned with write data. For x16 configurations, DQSL corresponds to the data on DQ[7:0], and DQSU corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0], respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.

58. As shown above and below, the accused DDR4 LRDIMMs each include a PCB having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system, and a register coupled to the PCB.

See, *e.g.*, Exhibit 5 (Micron MTA36ASF4G72LZ datasheet), at 9:



59. The register of each of the accused DDR4 LRDIMMs is configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command. *See*, *e.g.*, *id.* at 4-5, *id.* at 9 (register block diagram depicted above), JEDEC DDR4 SDRAM Standard 79-4C (Exhibit 8), at 29.

60. The accused DDR4 LRDIMMs each include a plurality of memory integrated circuits (e.g., SDRAMs, highlighted in blue below) mounted on the PCB and arranged in a plurality of ranks including a first rank and a second rank. The plurality of memory integrated circuits include at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank.

Figure 2: Functional Block Diagram

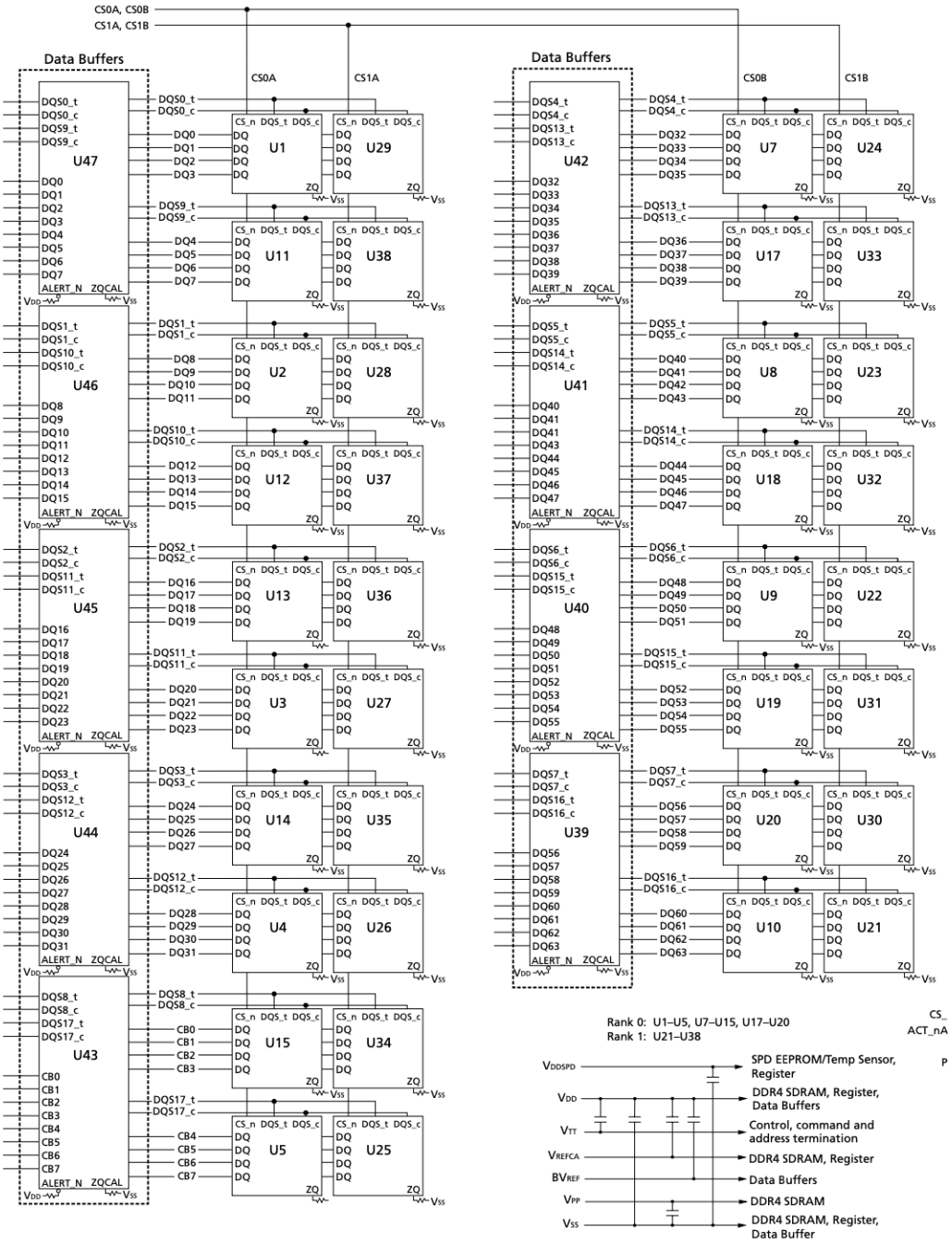
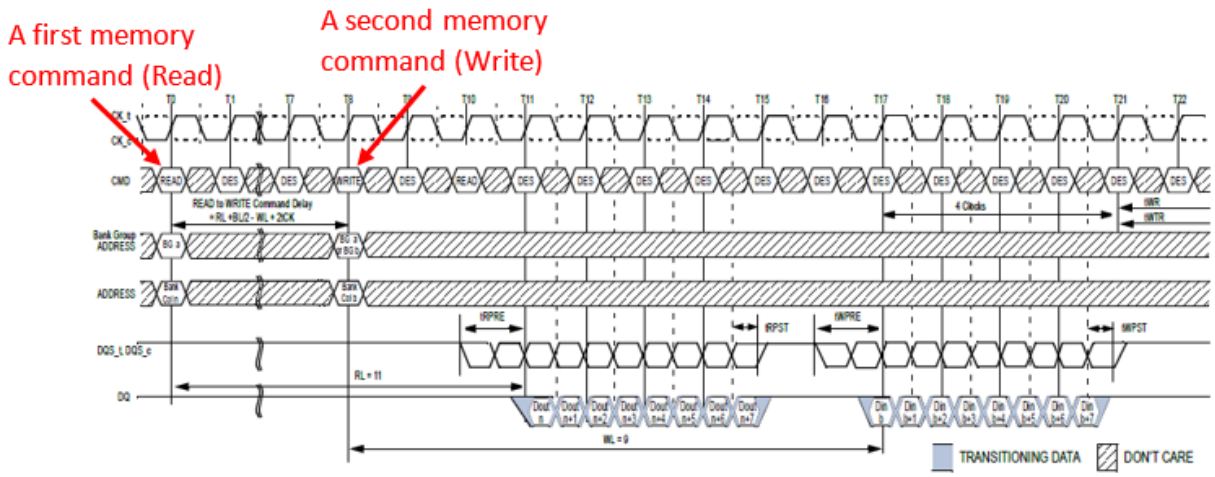


Exhibit 5 (Micron MTA36ASF4G72LZ datasheet), at 9.

61. As demonstrated in the exemplary waveform and timing diagram below, a first rank is selected to receive or output the first data burst in response to the first memory command, which is associated with a first chip-select signal, and is not selected to communicate data with the

memory controller in response to the second memory command. Similarly, the second rank is selected to receive or output the second data burst in response to the second memory command, which is associated with a second chip-select signal, and is not selected to communicate data with the memory controller in response to the first memory command. *See, e.g.*,



NOTE 1 BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL =9 (CWL = 9, AL = 0), Write Preamble = 1tCK
NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and WRITE command at T8.
NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 98 — READ (BL8) to WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group

JEDEC DDR4 SDRAM Standard 79-4C (Exhibit 8), at 105; *see also, e.g., id.*, §§ 4.24-4.25 (waveform and timing diagrams for JEDEC-standardized read and write operations); JEDEC 82-31A RCD Standard (Exhibit 9), at 2-3 (detailing the three basic modes of operation of the DDR4 RCD).

62. The accused DDR4 LRDIMMs further comprise a buffer (e.g. DDR4 data buffer) coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus.

Figure 2: Functional Block Diagram

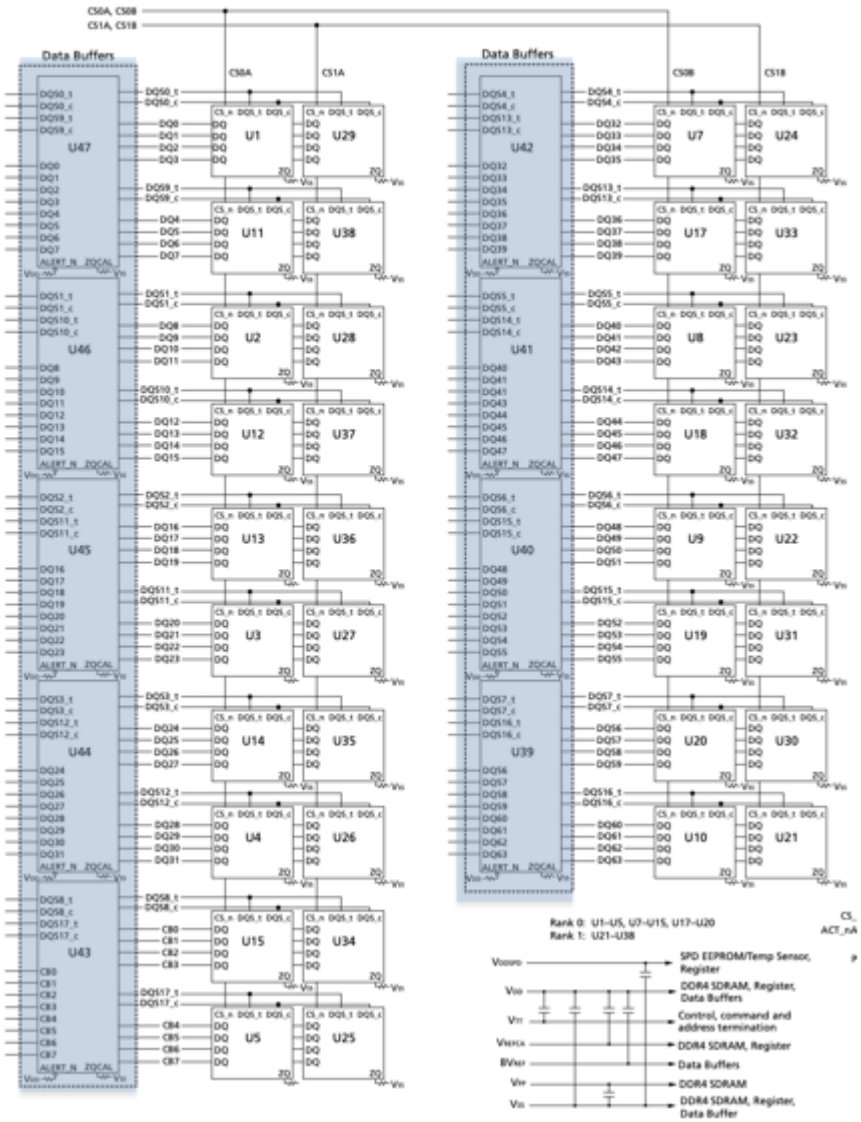


Exhibit 5 (Micron MTA36ASF4G72LZ datasheet), at 9.

4.61 Logic Diagram

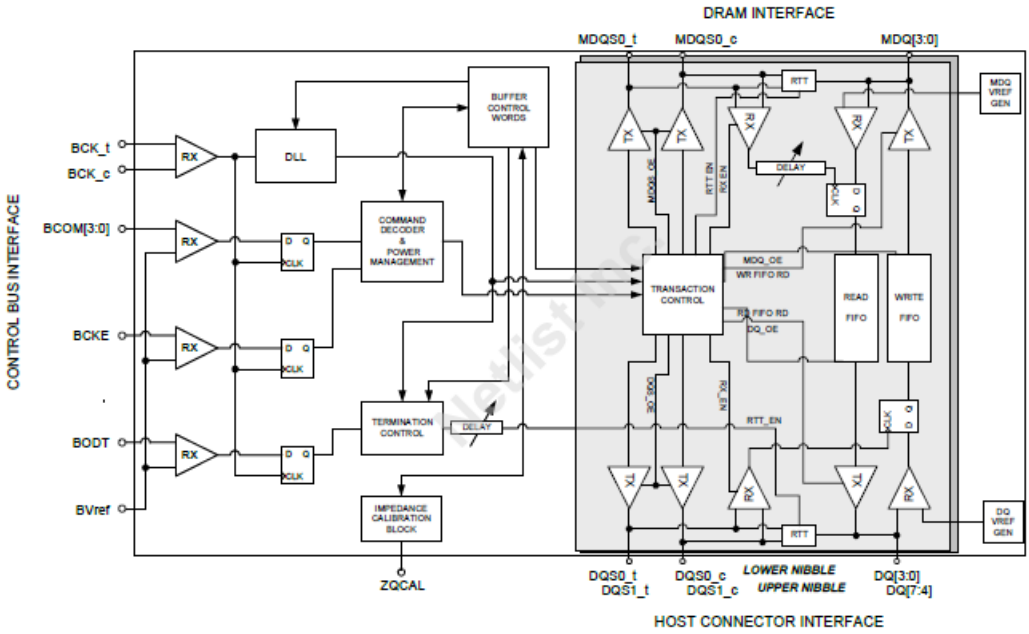


Figure 15 — Logic Diagram

JEDEC 82-32A Data Buffer Standard (Exhibit 7), at 95 (exemplary logic diagram of DDR4 data buffer circuitry).

63. As shown above and below, the buffer in each of the accused DDR4 LRDIMMs includes logic coupled to the buffer that is configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer. The logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.

2.4 Data Buffer Control Bus

This section describes the signals used in the DDR4 LRDIMM control bus that connects the DDR4 Register with each of the nine DDR4 data buffers (DDR4DB02).

2.4.1 Control Bus Signals

Table 2 — List of Signals for Data Buffer control

Name	Description	Signal Count
BCOM[3:0]	Data buffer command signals	4
BCKE	Function of registered DCKE (dedicated non-encoded signal)	1
BODT	Function of registered DODT (dedicated non-encoded signal)	1
BCK_t, BCK_c	Input clock	2
BVrefCA	Reference voltage for command and control signals	1
	Total	9

2.4.2 Command List

Table 3 — DDR4 Data Buffer Command Table

Command	Description	BCOM[3:0] Encoding
WR	Write BC4 or BC8 (fixed or on the fly) or BC10 (with CRC enabled) and send accessed rank ID and BL information in the next command time slot, followed by parity in the last command time slot.	1000
RD	Read BC4 or BC8 (fixed or on the fly) and send accessed rank ID and BL information in the next command time slot, followed by parity in the last command time slot.	1001
MRS Write	Send MRS Write bits snooped by DDR4 Register and the MRS ID in the following six command time slots, followed by parity in the last command time slot.	1011
BCW Write	Write buffer control word data in the next five command slots, followed by parity in the last command time slot.	1100
BCW Read	Read buffer control word address in the four command slots, followed by parity in the last command time slot.	1101
RFU[1]	Reserved for future use	1110
RFU[1]	Reserved for future use	1111
NOP	Idle, do nothing	1010

1. RFU commands are treated as NOP commands for command sequence error detection

JEDEC 82-32A Data Buffer Standard (Exhibit 7), at 3-4.

Table 4 — Multicycle Sequence for Write Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	WR	Write command BCOM[3:0] = 1000
2	DAT0	Transfer the rank ID for write command BCOM[1:0] = {RANK_ID[1:0]} for DRAM writes Burst length information for Write data BCOM[3:2] = {0, 0} for BC4 BCOM[3:2] = {0, 1} for BC8
3	PAR[3:0]	Even parity bits for WR command and data PAR[x]: Parity bit for previous two BCOM[x] transfers
4	Next Cmd	Next Command

Table 5 — Multi-cycle Sequence for Read Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	RD	Read command BCOM[3:0] = 1001
2	DAT0	Transfer the rank ID for read command or the MPR selection ID in MPR override read mode BCOM[1:0] = {RANK_ID[1:0]} for DRAM reads BCOM[1:0] = {BA1, BA0} for MPR override reads Burst length information for Read data BCOM[3:0] = {0, 0} for BC4[1] BCOM[3:0] = {0, 1} for BC8
3	PAR[3:0]	Even parity bits for RD command and data PAR[x]: Parity bit for previous two BCOM[x] transfers
4	Next Cmd	Next Command

1. BC4 is not supported for MPR override reads

Id. at 12, 14.

64. On information and belief, Micron also indirectly infringes the ’215 patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as Micron’s customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Micron has induced, and currently induces, the infringement of the ’215 patent through its affirmative acts of selling, offering to sell, distributing, and/or otherwise making available the accused DDR4 LRDIMM products and other materially similar products that infringe the ’215 patent. On information and belief, Micron provides specifications, datasheets, instruction

manuals, and/or other materials that encourage and facilitate infringing use of the accused DDR4 LRDIMM products and other materially similar products by users in a manner that it knows or should have known would result in infringement and with the intent of inducing infringement.

65. On information and belief, Micron also indirectly infringes the '215 patent, as provided in 35 U.S.C. § 271(c), contributing to direct infringement committed by others, such as customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Micron has contributed to, and currently contributes to, Micron's customers and end-users infringement of the '215 patent through its affirmative acts of selling and offering to sell, in this District and elsewhere in the United States, the accused DDR4 LRDIMM products and other materially similar products that infringe the '215 patent. On information and belief, the accused DDR4 LRDIMM and other materially similar products have no substantial noninfringing use, and constitute a material part of the patented invention. On information and belief, Micron is aware that the product or process that includes the accused DDR4 LRDIMM products and other materially similar products would be covered by one or more claims of the '215 patent. On information and belief, the use of the product or process that includes the accused DDR4 LRDIMM products infringes at least one claim of the '215 patent.

66. Micron's infringement of the '215 patent has damaged and will continue to damage Netlist. Micron has had actual notice of the '215 patent since at least April 28, 2021. Micron's infringement of the '215 patent has been continuing and willful. Micron continues to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Micron knew or should have known that its actions constituted an unjustifiably high risk of infringement.

VII. DEMAND FOR JURY TRIAL

67. Pursuant to Federal Rule of Civil Procedure 38(b), Netlist hereby demands a trial by jury on all issues triable to a jury.

VIII. PRAYER FOR RELIEF

WHEREFORE, Netlist respectfully requests that this Court enter judgment in its favor ordering, finding, declaring, and/or awarding Netlist relief as follows:

A. that Micron infringes the Patents-in-Suit;

B. all equitable relief the Court deems just and proper as a result of Micron's infringement;

C. an award of damages resulting from Micron's acts of infringement in accordance with 35 U.S.C. § 284;

D. enhanced damages pursuant to 35 U.S.C. § 284;

E. that Micron's infringement of the Patents-in-Suit is willful;

F. that this is an exceptional case and awarding Netlist its reasonable attorneys' fees pursuant to 35 U.S.C. § 285;

G. an accounting for acts of infringement and supplemental damages, without limitation, pre-judgment and post-judgment interest; and

H. such other equitable relief which may be requested and to which Netlist is entitled.

Dated: August 15, 2022

Respectfully submitted,

/s/ Jason Sheasby

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