# Exhibit B

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**UNITED STATES DISTRICT COURT**
**WESTERN DISTRICT OF TEXAS**
**WACO DIVISION**

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| OCEAN SEMICONDUCTOR LLC<br><br>Plaintiff,<br><br>v.<br><br>NVIDIA CORPORATION;<br><br>TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LIMITED; and<br><br>TSMC NORTH AMERICA,<br><br>Defendants. | Civil Action No. 6:22-cv-00200<br><br><br><br>JURY TRIAL DEMANDED |

## SECOND AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Ocean Semiconductor LLC ("Ocean Semiconductor" or "Plaintiff") files this Second Amended Complaint against NVIDIA Corporation ("NVIDIA"), Taiwan Semiconductor Manufacturing Company, Limited ("TSMC Ltd."), and TSMC North America ("TSMC NA") (TSMC Ltd. and TSMC NA collectively referred to as "TSMC") (collectively with NVIDIA, "Defendants"), seeking damages and other relief for patent infringement, and alleges with knowledge to its own acts, and on information and belief as to other matters, as follows:

## NATURE OF THE ACTION

1. This is an action for patent infringement arising under the Patent Laws of the United States, 35 U.S.C. § 1 *et seq*.

## THE PARTIES

2. Plaintiff Ocean Semiconductor is a limited liability company organized and existing under the laws of the State of Delaware, and its registered agent for service of process in Delaware is Rita Carnevale, 717 N. Union Street, Wilmington, DE 19805.

3. On information and belief, Defendant NVIDIA is a corporation organized and existing under the laws of Delaware, with its principal place of business at 2701 San Tomas Expressway, Santa Clara, CA 95050. NVIDIA is registered with the State of Texas and may be served with process through its registered agent, Corporation Service Company d/b/a CSC-Lawyers Incorporating Service Company, 211 E. 7th St., Suite 620, Austin, TX 78701. On information and belief, NVIDIA has a regional office in this District, including at least at 11001 Lakeline Blvd., Building 2, Suite 100, Austin, TX 78717.

4. On information and belief, Defendant NVIDIA sells, offers to sell, and/or uses products and services throughout the United States, including in this judicial District, and introduces infringing products and services into the stream of commerce knowing that they would be sold and/or used in this judicial District and elsewhere in the United States.

5. On information and belief, Defendant TSMC Ltd. is a corporation organized and existing under the laws of Taiwan. It has a principal place of business located at 8, Li-Hsin Rd. 6, Hsinchu Science Park, Hsinchu 300-78, Taiwan, R.O.C. TSMC engages in business in the State of Texas. Pursuant to §17.044 of the Texas Civil Practice & Remedies Code, TSMC has designated the Secretary of State as its agent for service of process and may be served with process through the Secretary of State. The Secretary of State may forward service to TSMC at its home office address located at 8, Li-Hsin Rd. 6, Hsinchu Science Park, Hsinchu 300-78,Taiwan, R.O.C.

6. On information and belief, Defendant TSMC Ltd. either itself and/or through the activities of its subsidiaries, makes, uses, sells, offers for sale, and/or imports throughout the

United States, including within this District, products, such as semiconductor devices and integrated circuits, that infringe the Asserted Patents, defined below. TSMC's customers, and in particular Defendant NVIDIA, incorporates these products into downstream products that are made, used, sold, offered for sale, and/or imported throughout the United States, including within this judicial District.

7. Defendant TSMC NA is a wholly-owned subsidiary of Defendant TSMC Ltd. TSMC NA is a California corporation headquartered in San Jose, California. TSMC NA has a physical place of business at 11921 North Mopac Expressway, Austin, Texas 78759. TSMC NA's Registered Agent for process of service is Steven A. Schulman, 2851 Junction Avenue, San Jose, California 95134.

8. TSMC's 2021 Annual Report lists the "Major Corporate Function" of TSMC NA as "[s]ales and market development, field technical solutions and business operations for customers in North America." https://investor.tsmc.com/static/annualReports/2021/english/index.html; *see also* https://investor.tsmc.com/static/annualReports/2021/english/pdf/e_all.pdf (p. 167); https://craft.co/tsmc-north-america (accessed July 21, 2022) ("TSMC North America is a supplier of semiconductor products. It sells and markets integrated circuits and other semiconductor devices. The company caters to the computer, communications, consumer, industrial, mobile devices, high-performance computing, automotive electronics, and the Internet of things (IoT) markets.").

9. According to TSMC's 2021 Annual Report, NVIDIA Corporation is one of TSMC's customers. https://investor.tsmc.com/static/annualReports/2021/english/pdf/e_all.pdf (p. 100).

10. Plaintiff Ocean Semiconductor is the assignee and owner of the patents at issue in this action: U.S. Patents Nos. 7,005,376; 7,307,322; and 7,629,211 (collectively, the "Asserted Patents"). Ocean Semiconductor holds all substantial rights, title, and interest in the Asserted Patents, including the exclusive right to sue NVIDIA for infringement and recover damages, including damages for past infringement.

11. Plaintiff Ocean Semiconductor seeks monetary damages and prejudgment interest for Defendant's past and ongoing direct and indirect infringement of the Asserted Patents.

12. Defendant NVIDIA is a semiconductor company that designs, develops, sells, offers to sell, and imports into the United States semiconductor products in the communications, internet of things, automotive, computer, and consumer electronics industries ("Accused Products").

13. Defendant NVIDIA, which has its own design centers in the United States (including a facility in Austin, Texas), contracts with third-party semiconductor fabricators or foundries ("NVIDIA Foundry Partners") that own, operate, and/or control semiconductor fabrication plants ("fabs") within and/or outside of the United States ("International Facilities") to produce the Accused Products. One such NVIDIA Foundry Partner is Taiwan Semiconductor Manufacturing Company Ltd.. *See*, *e.g.*, "NVIDIA and TSMC Ship One-Billionth GeForce Graphics Processor," available at https://www.chipestimate.com/NVIDIA-and-TSMC-Ship-One-Billionth-GeForce-Graphics-Processor/TSMC/news/8288 (last accessed February 24, 2022); "TSMC expects record revenue from NVIDIA Turing GPU production," available at https://hardwaresfera.com/en/noticias/hardware/tsmc-espera-ingresos-record-gracias-la-produccion-de-las-gpu-turing-de-nvidia/ (last accessed February 24, 2022); "NVIDIA Corp.'s Relationship With Taiwan Semiconductor Manufacturing Is Deepening," available at

https://www.fool.com/investing/2017/05/17/nvidia-corp-relationship-taiwan-semiconductor.aspx (last accessed February 24, 2022); "Nvidia: TSMC Remains Our Primary Manufacturing Partner for 16nm FinFETs and 10nm," available at https://wccftech.com/nvidia-tsmc-official-partner-16nm-finfet-10nm/ (last accessed February 24, 2022); "TSMC Gives NVIDIA Priority for 28 nm Manufacturing," available at https://www.techpowerup.com/165707/tsmc-gives-nvidia-priority-for-28-nm-manufacturing (last accessed February 24, 2022); "VIDIA's Next Gen 11 Series 'Turing' GPUs Driving Record Revenue Growth for TSMC Through Q4," available at https://wccftech.com/nvidias-next-gen-11-series-turing-gpus-driving-record-revenue-growth-for-tsmc-through-q4/ (accessed July 21, 2022); "NVIDIA Turing GPU Architecture" (white paper), available at https://images.nvidia.com/aem-dam/en-zz/Solutions/design-visualization/technologies/turing-architecture/NVIDIA-Turing-Architecture-Whitepaper.pdf (accessed July 21, 2022) ("NVIDIA Turing is the world's most advanced GPU architecture. The high-end TU102 GPU includes 18.6 billion transistors fabricated on TSMC's 12 nm FFN (FinFET NVIDIA) high-performance manufacturing process."); "Nvidia GTX 1630 leaks, an entry level Turing card," available at https://www.gsmarena.com/nvidia_gtx_1630_leaks_an_entry_level_turing_card-news-54822.php (accessed July 21, 2022) ("Turing chips are fabbed in TSMC's 12nm foundries, so there should be relatively little competition for capacity."); "AMD is launching first, but Nvidia has contracted TSMC for a 7nm GPU in 2019," available at https://www.pcgamesn.com/nvidia-7nm-gpu-tsmc (accessed July 21, 2022) ("The Nvidia Turing architecture is built upon the 12nm process node, although the company, which utilises TSMC for all its foundry needs, is already looking ahead to the next densest node: 7nm."); "NVIDIA Turing Architecture In-Depth," available at https://developer.nvidia.com/blog/nvidia-turing-architecture-in-depth/ (accessed July

21, 2022) ("NVIDIA Turing is the world's most advanced GPU architecture. The high-end TU102 GPU includes 18.6 billion transistors fabricated on TSMC's 12 nm FFN (FinFET NVIDIA) high-performance manufacturing process."). TSMC has a contractual partnership with NVIDIA to design, develop, or manufacture semiconductor products including integrated circuits for NVIDIA.

14. On information and belief, Defendant NVIDIA (directly or through one or more of its Foundry Partners such as TSMC) designs, develops and/or manufactures one or more systems, products, devices, and integrated circuits for importation into the United States for use, sale, and/or offer for sale in this District and throughout the United States, including, but not limited to, GEFORCE RTX 20 SERIES models (including, but not limited to, GEFORCE RTX 2060, 2060 SUPER, 2070, 2070 SUPER, 2080, 2080 SUPER, and 2080 Ti), GEFORCE GTX 16 SERIES models (including, but not limited to, GEFORCE GTX 1650, 1650 SUPER, 1650 Ti, 1660, 1660 Super, and 1660 Ti), TITAN models (including, but not limited to TITAN RTX models), QUADRO models (e.g., QUADRO T400, T500, T600, T1000, T4000, T5000, T8000, RTX 4000, RTX 5000, and RTX 8000 models), products incorporating NVIDIA's Turing architecture (*e.g.*, products incorporating TU102, TU104, TU106, TU116, or TU117), products manufactured using, for example, TSMC's 12nm FinFET manufacturing process, and similar products, devices, systems, components of systems, and/or integrated circuits ("NVIDIA Accused Products"). *See, e.g.*, https://www.nvidia.com/en-us/geforce/graphics-cards/compare/?section=compare-20 (last accessed February 24, 2022); https://images.nvidia.com/aem-dam/en-zz/Solutions/design-visualization/technologies/turing-architecture/NVIDIA-Turing-Architecture-Whitepaper.pdf (last accessed February 24, 2022); https://www.techpowerup.com/gpu-specs/geforce-rtx-2080-ti.c3305 (last accessed February 24, 2022); https://www.techpowerup.com/gpu-specs/geforce-rtx-2080-

super.c3439 (last accessed February 24, 2022); https://www.techpowerup.com/gpu-specs/geforce-rtx-2080.c3224 (last accessed February 24, 2022); https://www.techpowerup.com/gpu-specs/geforce-rtx-2070-super.c3440 (last accessed February 24, 2022); https://www.techpowerup.com/gpu-specs/nvidia-tu104.g854 (last accessed February 24, 2022); https://www.techpowerup.com/gpu-specs/geforce-rtx-2070.c3252 (last accessed February 24, 2022); https://www.techpowerup.com/gpu-specs/nvidia-tu106.g875 (accessed February 24, 2022); https://www.techpowerup.com/gpu-specs/nvidia-tu102.g813#:~:text=NVIDIA's%20TU102%20GPU%20uses%20the,Ultimate%20(Feature%20Level%2012_2) (last accessed February 24, 2022); https://www.techpowerup.com/review/nvidia-geforce-turing-geforce-rtx-architecture/2.html (last accessed February 24, 2022); https://www.techpowerup.com/gpu-specs/nvidia-tu117.g881#:~:text=NVIDIA's%20TU117%20GPU%20uses%20the,CUDA%207.5%20can%20be%20used (last accessed February 24, 2022); https://www.techpowerup.com/gpu-specs/geforce-gtx-1650.c3366 (last accessed February 24, 2022); https://www.techpowerup.com/gpu-specs/geforce-gtx-1650-super.c3411 (last accessed February 24, 2022); https://www.techpowerup.com/gpu-specs/geforce-gtx-1650-ti-mobile.c3512 (last accessed February 24, 2022); https://www.techpowerup.com/gpu-specs/geforce-gtx-1660.c3365 (last accessed February 24, 2022); https://www.techpowerup.com/gpu-specs/geforce-gtx-1660-super.c3458 (last accessed February 24, 2022); https://www.techpowerup.com/gpu-specs/geforce-gtx-1660-ti.c3364 (last accessed February 24, 2022); https://www.techpowerup.com/gpu-specs/titan-rtx.c3311 (last accessed February 24, 2022); https://www.techpowerup.com/gpu-specs/t400.c3808 (last accessed February 24, 2022); https://www.techpowerup.com/gpu-specs/t500-mobile.c3747 (last accessed February 24, 2022); https://www.techpowerup.com/gpu-

specs/t600.c3796 (last accessed February 24, 2022); https://www.techpowerup.com/gpu-specs/t1000.c3797 (last accessed February 24, 2022); https://www.techpowerup.com/gpu-specs/quadro-rtx-4000-mobile.c3430 (last accessed February 24, 2022); https://www.techpowerup.com/gpu-specs/quadro-rtx-5000-mobile.c3431 (last accessed February 24, 2022); https://www.techpowerup.com/gpu-specs/quadro-rtx-8000.c3306 (last accessed February 24, 2022); https://www.anandtech.com/show/13249/nvidia-announces-geforce-rtx-20-series-rtx-2080-ti-2080-2070 (last accessed February 24, 2022); https://www.pcgamer.com/rtx-2080-everything-you-need-to-know/ (last accessed February 24, 2022); https://images.nvidia.com/aem-dam/en-zz/Solutions/design-visualization/technologies/turing-architecture/NVIDIA-Turing-Architecture-Whitepaper.pdf (last accessed February 24, 2022); https://www.notebookcheck.net/NVIDIA-GeForce-GTX-1660-Ti-Laptop-Graphics-Card.386426.0.html (last accessed February 24, 2022); https://www.anandtech.com/show/15010/the-nvidia-geforce-gtx-1660-super-review-feat-evga (last accessed February 24, 2022); https://www.pcgamer.com/nvidia-geforce-gtx-1660-review/ (last accessed February 24, 2022).

## JURISDICTION AND VENUE

15. This is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. § 1, *et seq*., including 35 U.S.C. §§ 271, 281, 283, 284, and 285.

16. This Court has jurisdiction over the subject matter of this action under 28 U.S.C. §§ 1331 and 1338(a).

17. NVIDIA is subject to this Court's general personal jurisdiction at least because NVIDIA is a resident of Texas as defined by Texas law.

18. NVIDIA is additionally subject to this Court's general and specific personal jurisdiction because NVIDIA has sufficient minimum contacts within the State of Texas and this District, pursuant to due process and/or the Texas Long Arm Statute, Tex. Civ. Prac & Rem. Code § 17.042. On information and belief, NVIDIA committed the tort of patent infringement in the State of Texas and this District; NVIDIA purposefully availed itself of the privileges of conducting business in the State of Texas and this District; NVIDIA regularly conducts and solicits business within the State of Texas and this District; and NVIDIA designs, develops, manufactures, distributes, makes available, imports, sells, and offers to sell products and services throughout the United States, including in this District, and introduces infringing products and services into that stream of commerce knowing that they would be used and sold in this District and elsewhere in the United States.

19. TSMC Ltd. and TSMC NA are subject to this Court's general and specific personal jurisdiction because TSMC has sufficient minimum contacts within the State of Texas and this District, pursuant to due process and/or the Texas Long Arm Statute, Tex. Civ. Prac & Rem. Code § 17.042. On information and belief, TSMC committed the tort of patent infringement in the State of Texas and this District; TSMC purposefully availed itself of the privileges of conducting business in the State of Texas and this District; TSMC regularly conducts and solicits business within the State of Texas and this District; and TSMC distributes, makes available, imports, sells, and offers to sell products and services throughout the United States, including in this District, and introduces infringing products and services into that stream of commerce knowing that they would be used and sold in this District and elsewhere in the United States.

20. Venue is proper in this Court pursuant to 28 U.S.C. § 1391 and 1400(b). NVIDIA is subject to personal jurisdiction in this District and a substantial part of the events giving rise to

Ocean Semiconductor's claims against NVIDIA occurred and continue to occur in this District. NVIDIA has a regular and established place of business in this District—including at least its regional office at 11001 Lakeline Blvd., Building 2, Suite 100, Austin, TX 78717—and its acts of infringement have taken place and are continuing to take place in this District.

21. On information and belief, NVIDIA employs engineers in this District to design and develop products, devices, systems, and/or components of systems, including GPU products, that that are accused of infringing one or more claims of the Asserted Patents. *See*, *e.g.*, https://nvidia.wd5.myworkdayjobs.com/NVIDIAExternalCareerSite/1/refreshFacet/318c8bb6f553100021d223d9780d30be (showing NVIDIA's ongoing efforts to hire engineers in Austin, Texas) (last accessed February 24, 2022). On information and belief, NVIDIA conducts software and hardware development, marketing, and promotion activities with respect to NVIDIA products that infringe one or more claims of the Asserted Patents.

22. Further, NVIDIA has regularly made new product announcements in the state of Texas and this District. For example, on May 6, 2016, NVIDIA selected a forum in this judicial district to announce and offer for sale certain NVIDIA graphics cards. Specifically, NVIDIA's co-founder and CEO Jensen Huang promoted NVIDIA products, including the NVIDIA GeForce GTX 1080 graphics card, at the Austin Convention Center located at 500 East Cesar Chavez Street, Austin, TX, 78701, in this judicial district. Mr. Huang demonstrated and touted the capabilities of the GeForce GTX 1080 product. NVIDIA also demonstrated for the first time the GeForce GTX 1070.

23. Additionally, NVIDIA—directly or through intermediaries (including distributors, retailers, and others), subsidiaries, alter egos, and/or agents—ships, distributes, offers for sale, and/or sells its products in the United States and this District. NVIDIA has purposefully and

voluntarily placed one or more of its infringing products into the stream of commerce with the awareness and/or intent that they will be purchased by consumers in this District. On information and belief, NVIDIA knowingly and purposefully ships infringing products into, and within, this District through an established distribution channel. These infringing products have been, and continue to be, purchased by consumers and businesses in this District.

24. Venue in this District is proper under 28 U.S.C. § 1391(c)(3) and 28 U.S.C. § 1400(b) with respect to TSMC Ltd. TSMC Ltd. is not a resident of the United States and may be sued in any district, including this District. In particular, TSMC Ltd. is a Taiwanese company, such that venue is proper because suits against foreign entities are proper in any judicial district where they are subject to personal jurisdiction.

25. Venue in this District is proper under 28 U.S.C. § 1400(b) with respect to TSMC NA because it has a regular and established place of business in this District and has committed acts of infringement in this District. TSMC NA has a permanent office location in Austin, Texas, which is in Travis County and within this District. On information and belief, TSMC NA employs full-time personnel such as sales personnel and engineers in this District, including in Austin, Texas. TSMC NA has also committed acts of infringement in this District by commercializing, marketing, selling, distributing, testing, and/or servicing certain products accused of being manufactured by patented processes in this action.

## JOINDER

26. Joinder of Defendants is proper under 35 U.S.C. § 299. The allegations of patent infringement contained herein arise out of the same series of transactions or occurrences relating to the importing into the United States and/or making, using, selling, or offering for sale within

the United States, the same Accused Products, which are fabricated by TSMC for Defendant NVIDIA, which sells the Accused Products in the United States.

## <u>THE PATENTS-IN-SUIT</u>

### A. U.S. Patent No. 7,005,376

27. U.S. Patent No. 7,005,376 ("the '376 patent"), titled "Ultra-Uniform Silicides in Integrated Circuit Technology," issued on February 28, 2006. Ocean Semiconductor owns all rights and title to the '376 patent, as necessary to bring this action and to recover past, present, and future damages for NVIDIA's infringement of the '376 patent. A true and correct copy of the '376 patent is attached as Exhibit 1.

28. The '376 patent discloses methods, systems, and devices related to siliciding in semiconductor devices. Semiconductor devices are made by forming integrated circuits comprising millions of transistors on a silicon substrate. Semiconductor transistors include source/drain junctions and a gate separated by substrate material. Metal contacts are formed in the integrated circuit to reach the source/drain junctions and gate of the transistors. Transition materials called "silicides" are formed between the metal contacts and the source/drain junctions and gate in a process known as "siliciding." The '376 patent discloses methods that overcome problems with existing siliciding techniques, including by reducing high electrical resistance between the metal contacts and the silicide through the formation of ultra-uniform silicides between the metal contacts and the source/drain junctions and gate.

29. For example, the '376 patent discloses a method of forming an integrated circuit comprising: providing a semiconductor substrate; forming a gate dielectric on the semiconductor substrate; forming a gate over the gate dielectric, forming source/drain junctions in the semiconductor substrate, forming ultra-uniform silicides on the source/drain junctions, depositing

a dielectric layer above the semiconductor substrate; and forming contacts in the dielectric layer to the ultra-uniform silicides.

30. The ’376 patent claims patent-eligible subject matter and is valid and enforceable.

**B. U.S. Patent No. 7,307,322**

31. U.S. Patent No. 7,307,322 (“the ’322 patent”), titled “Ultra-Uniform Silicides in Integrated Circuit Technology,” issued on December 11, 2007. Ocean Semiconductor owns all rights and title to the ’322 patent, as necessary to bring this action and to recover past, present, and future damages for Defendant NVIDIA’s infringement of the ’322 patent. A true and correct copy of the ’322 patent is attached as Exhibit 2.

32. The ’322 patent discloses methods, systems, and devices related to siliciding in semiconductor devices. Semiconductor devices are made by forming integrated circuits comprising millions of transistors on a silicon substrate. Semiconductor transistors include source/drain junctions and a gate separated by substrate material. Metal contacts are formed in the integrated circuit to reach the source/drain junctions and gate of the transistors. Transition materials called “silicides” are formed between the metal contacts and the source/drain junctions and gate in a process known as “siliciding.” The ’322 patent discloses integrated circuits that overcome problems with existing siliciding techniques, including integrated circuits that have reduced electrical resistance between the metal contacts and the silicide and include ultra-uniform silicides between the metal contacts and the source/drain junctions and gate.

33. For example, the ’322 patent discloses an integrated circuit comprising: a semiconductor substrate having source/drain junctions; a gate dielectric on the semiconductor substrate; a gate over the gate dielectric; ultra-uniform silicides on the source/drain junctions; a

dielectric layer above the semiconductor substrate; and contacts in the dielectric layer to the ultra-uniform silicides.

34. The ’322 patent claims patent-eligible subject matter and is valid and enforceable.

**C. U.S. Patent No. 7,629,211**

35. U.S. Patent No. 7,629,211 (“the ’211 patent”), titled “Field Effect Transistor and Method of Forming a Field Effect Transistor,” issued on December 8, 2009. Ocean Semiconductor owns all rights and title to the ’211 patent, as necessary to bring this action and to recover past, present, and future damages for Defendant NVIDIA’s infringement of the ’211 patent. A true and correct copy of the ’211 patent is attached as Exhibit 3.

36. The ’211 patent discloses methods, systems, and devices related to the formation of integrated circuits, in particular, field effect transistors comprising a strain-creating element formed adjacent to a gate electrode. Field effect transistors are used as switching elements in integrated circuits and provide a means to control current flowing through a channel region between source and drain regions. Conductivity in the channel region is controlled by a gate voltage applied to a gate electrode. The conductivity of the channel region depends on the mobility of the charge carriers in the channel region, such that an increase in charge carrier mobility leads to an increase of the channel conductivity. One way to increase charge carrier mobility is to modify the lattice structure of the channel region by creating tensile or compressive strain using strain-creating elements adjacent the gate electrode. The ’211 patent discloses methods of forming field effect transistors that overcome problems with existing strain-creating techniques, including methods that avoid or reduce the effects of strain relaxation that may occur in strain creating elements and result in reduced charge mobility.

37. For example, the ’211 patent discloses a method of forming a field effect transistor, comprising: providing a semiconductor substrate, a gate electrode being formed above said semiconductor substrate; forming at least one cavity in said substrate adjacent said gate electrode; and forming a strain-creating element in said at least one cavity, said strain-creating element comprising: a compound material comprising a first chemical element and a second chemical element, wherein said first chemical element comprises one of germanium and carbon, said second chemical element comprises silicon, and said semiconductor substrate comprises said second chemical element; a first portion and a second portion, wherein said second portion is located above said first portion; a first concentration ratio between a concentration of said first chemical element in said first portion and a concentration of said second chemical element in said first portion; and a second concentration ratio between a concentration of said first chemical element in said second portion and a concentration of said second chemical element in said second portion, wherein said first concentration ratio is smaller than said second concentration ratio and wherein a ratio between a concentration of said first chemical element and a concentration of said second chemical element increases in a vertical direction with increasing distance from a bottom surface of said at least one cavity formed in said substrate.

38. The ’211 patent claims patent-eligible subject matter and is valid and enforceable.

**COUNT I: INFRINGEMENT OF U.S. PATENT NO. 7,005,376**

39. Ocean Semiconductor incorporates by reference the foregoing paragraphs of this Second Amended Complaint as if fully set forth herein.

40. At least as of the date of service of the original Complaint, Ocean Semiconductor placed NVIDIA on actual notice of the ’376 patent and actual notice that its actions constituted and continued to constitute infringement of the ’376 patent. NVIDIA has had actual knowledge of the ’376 patent and its own infringement of the ’376 patent since at least that time. At least as

of the date of service of this Second Amended Complaint, Ocean Semiconductor placed Defendants on actual notice of the ’376 patent and actual notice that its actions constitute infringement of the ’376 patent. Defendants have had actual knowledge of the ’376 patent and its own infringement of the ’376 patent since at least that time.

41. On information and belief, Defendants have directly infringed and continue to infringe at least claims 1, 4, and 6 of the ’376 patent literally or under the doctrine of equivalents, by importing into the United States, and/or using, and/or selling, and/or offering for sale in the United States, without authority or license, integrated circuits that that are designed, developed, fabricated, and/or manufactured by a process including all of the limitations of at least claims 1, 4, and 6 of the ’376 patent, and systems, products, and/or devices containing these integrated circuits including at least the NVIDIA Accused Products (“’376 Accused Products”) in violation of 35 U.S.C. § 271. The ’376 Accused Products are manufactured by a process including all of the limitations of at least claim 1 of the ’376 patent.

42. Discovery is expected to uncover the full extent of Defendants’ infringement of the ’376 patent beyond the ’376 Accused Products already identified herein.

43. Specifically, on information and belief, Defendants have directly infringed and continue to infringe at least claims 1, 4, and 6 of the ’376 patent literally or under the doctrine of equivalents, by making, using, offering to sell, or selling in the United States, and/or by importing into the United States, without authority or license, the ’376 Accused Products, in violation of 35 U.S.C. § 271(a). In addition, Defendants have directly infringed and continue to directly infringe at least claims 1, 4, and 6 of the ’376 patent literally or directly under the doctrine of equivalents, by importing into the United States and/or offering to sell, selling, or using within the United States, without authority or license, the ’376 Accused Products which are made by the

process patented in the ’376 patent, in violation of 35 U.S.C. § 271(g). On information and belief, Defendants import the ’376 Accused Products into the United States for sale and distribution to customers located in the United States. On information and belief, Defendants sell and/or offers for sale the ’376 Accused Products in the United States. For example, Defendants provide direct sales through their own sales channels and/or their distributors or contract manufacturers and sell the ’376 Accused Products to businesses including original equipment manufacturers and electronic manufacturing service providers. On information and belief, these direct sales include sales of the ’376 Accused Products in the United States. On information and belief, Defendants offer the ’376 Accused Products for sale in the United States. For example, Defendants engage in sales, marketing, and contracting activity in the United States and/or with United States offices of their customers.

44. The ’376 Accused Products are manufactured by a process including all of the limitations of at least claims 1, 4, and 6 of the ’376 patent (e.g., TSMC’s 12 nm FinFET process). For example, during the manufacture of the ’376 Accused Products, a semiconductor substrate is provided, a gate dielectric is formed on the semiconductor substrate, and a gate is formed over the gate dielectric. *See*, *e.g.*, Exhibit 4. Source/drain junctions are formed in the semiconductor substrate, and ultra-uniform silicides are formed on the source/drain junctions. *Id*. A dielectric layer is deposited above the semiconductor substrate, and contacts are formed in the dielectric layer to the ultra-uniform silicides. *Id*.

45. Attached hereto as Exhibit 4, and incorporated by reference herein, is a claim chart detailing how the NVIDIA GeForce RTX 2070 Super (TU104 GPU based on Turing architecture and made using a 12 nm production process at TSMC), which is manufactured by a NVIDIA Foundry Partner (TSMC) on behalf of NVIDIA, satisfies each element of at least claims 1, 4, and

6 of the '376 patent, literally or under the doctrine of equivalents. On information and belief, the other '376 Accused Products are also manufactured by a NVIDIA Foundry Partner (e.g., TSMC) on behalf of NVIDIA and satisfy each element of at least claims 1, 4, and 6 of the '376 patent, literally or under the doctrine of equivalents.

46. On information and belief, the '376 Accused Products are neither materially changed by subsequent processes nor become trivial and nonessential components of another product.

47. On information and belief, at least as of the date of service of this Second Amended Complaint, Defendants have induced and continue to induce others actively, knowingly, and intentionally, including their suppliers and contract manufacturers, to infringe one or more claims of the '376 patent, including, but not limited to, claims 1, 4, and 6, pursuant to 35 U.S.C. § 271(b), by actively encouraging others to import into the United States, and/or make, use, sell, and/or offer to sell in the United States, the '376 Accused Products or products containing the infringing semiconductor components of the '376 Accused Products, by actively inducing others to infringe the '376 patent by making, using, selling, offering for sale, marketing, advertising, and/or importing the Accused Products to their customers for use in downstream products that infringe, or were manufactured using processes that infringe, the '376 patent, and by instructing others to infringe the '376 patent.

48. For example, NVIDIA actively promotes the sale, use, and importation of the '376 Accused Products in marketing materials, technical specifications, data sheets, web pages on its website (e.g., www.nvidia.com), press releases, training tutorials, development and design tools, user manuals, and developer forums as well as at trade shows (e.g., the Consumer Technology Association's Consumer Electronics Show ("CES")) and NVIDIA's online Discussion Forums for

GeForce products and developers) and through its sales and distribution channels that encourage infringing uses, sales, offers to sell, and importation of the '376 Accused Products. As another example, NVIDIA's representatives travel to customer sites in the United States for sales and support activity that includes working with customers to facilitate these customers' infringing testing, marketing, importation, and sales activity. On information and belief, NVIDIA supplies customers with '376 Accused Products so that they may be used, sold, or offered for sale by those customers. For example, NVIDIA provides direct sales to original equipment manufacturers and electronic manufacturing service providers. On information and belief, these direct sales include sales to customers in the United States. NVIDIA also promotes, publicly on its website, uses of the '376 Accused Products by customers in the United States. NVIDIA additionally provides a wide range of technical support to customers and businesses, including product-specific solutions. NVIDIA also encourages customers and other third parties to communicate directly with NVIDIA representatives about these products for purposes of technical assistance and repair (e.g., https://www.nvidia.com/en-us/support/enterprise/ and https://www.nvidia.com/en-us/support/consumer/).

49. TSMC actively promotes the sale, use, and importation of the '376 Accused Products through its sales and distribution channels in the United States that encourage infringing uses, sales, offers to sell, and importation of the '376 Accused Products. For example, TSMC supplies NVIDIA with '376 Accused Products so that they may be used, sold, or offered for sale by NVIDIA to original equipment manufacturers and electronic manufacturing service providers. On information and belief, these sales include sales to customers in the United States.

50. On information and belief, Defendants sell or offer for sale the '376 Accused Products to third parties that incorporate the '376 Accused Products into third party products ("the '376 Third Party Products").

51. On information and belief, Defendants assist third parties, directly and/or through intermediaries, in the development of the '376 Third Party Products and provides technical support and supports the sales of the '376 Third Party Products.

52. On information and belief, since at least as of the date of service of the original Complaint, NVIDIA has induced and continue to induce third parties with specific intent or willful blindness to import, make, use, sell, and/or offer to sell '376 Third Party Products that include at least one '376 Accused Product, whose make, use, sale, offer for sale, or importation constitutes direct infringement of at least one claim of the '376 patent. On information and belief, since at least as of the date of service of this Second Amended Complaint, Defendants have induced and continue to induce third parties with specific intent or willful blindness to import, make, use, sell, and/or offer to sell '376 Third Party Products that include at least one '376 Accused Product, whose make, use, sale, offer for sale, or importation constitutes direct infringement of at least one claim of the '376 patent.

53. On information and belief, the '376 Third Party Products are imported into the United States for use, sale, and/or offer for sale in this District and throughout the United States ("Imported '376 Third Party Products").

54. On information and belief, to the extent any entity other than Defendants, including but not limited to any of NVIDIA's other Foundry Partners or third-party importers, imports the '376 Accused Products and/or Imported '376 Third-Party Products into the United States for or on behalf of Defendants ("Third Party Importer"), Defendants are liable for inducement of

infringement by the Third Party Importer. Defendants have encouraged the Third Party Importer to infringe the ’376 patent and intended that it do so. This encouragement includes at least ordering or instructing the Third Party Importer to import the ’376 Accused Products and/or ’376 Third-Party Products into the United States, providing directions and other materials to the Third Party Importer to enable such importation, and/or conditioning the receipt of benefits (included but not limited to payment) to the Third Party Importer on such importation. On information and belief, this behavior has continued since Defendants first became aware of the ’376 patent and the infringement thereof.

55. On information and belief, to the extent any entity other than Defendants, including but not limited to any of NVIDIA’s other Foundry Partners, uses the patented method to fabricate or manufacture the ’376 Accused Products and/or Imported ’376 Third-Party Products in the United States for or on behalf of Defendants (“Third Party Manufacturer”), Defendants are liable for inducement of infringement by the Third Party Manufacturer. Defendants have encouraged the Third Party Manufacturer to infringe the ’376 patent and intended that it do so. This encouragement includes, without limitation, ordering the ’376 Accused Products from the Third Party Manufacturer since Defendants first became aware of the ’376 patent and its infringement by the Third Party Manufacturer.

56. Defendants have benefitted and continue to benefit from the importation into the United States of the ’376 Accused Products, ’376 Third Party Products, and Imported ’376 Third Party Products.

57. Ocean Semiconductor has suffered, and continues to suffer, damages as a result of Defendants’ infringement of the ’376 patent.

58. At least as of the date of service of the original Complaint, NVIDIA has infringed the ’376 patent knowingly, willfully, deliberately, and in disregard of Plaintiff’s patent rights, at least by performing acts of infringement with actual knowledge of its direct and indirect infringement or while remaining willfully blind to the fact of its direct and indirect infringement. As a result of at least this conduct, Plaintiff is entitled to enhanced damages under 35 U.S.C. § 284 and to attorneys’ fees and costs under 35 U.S.C. § 285. At least as of the date of service of this Second Amended Complaint, Defendants have infringed the ’376 patent knowingly, willfully, deliberately, and in disregard of Plaintiff’s patent rights, at least by performing acts of infringement with actual knowledge of its direct and indirect infringement or while remaining willfully blind to the fact of its direct and indirect infringement. As a result of at least this conduct, Plaintiff is entitled to enhanced damages under 35 U.S.C. § 284 and to attorneys’ fees and costs under 35 U.S.C. § 285.

59. Ocean Semiconductor reserves the right to modify its infringement theories as discovery progresses in this case. Ocean Semiconductor shall not be estopped or otherwise limited or restricted for purposes of its infringement contentions or its claim constructions by the claim charts that it provides with this Second Amended Complaint. Ocean Semiconductor intends for the claim chart (Exhibit 4) for the ’376 patent to satisfy the notice requirements of Rule 8(a)(2) of the Federal Rule of Civil Procedure. The claim chart is not Ocean Semiconductor’s preliminary or final infringement contentions or preliminary or final claim construction positions.

**COUNT II: INFRINGEMENT OF U.S. PATENT NO. 7,307,322**

60. Ocean Semiconductor incorporates by reference the foregoing paragraphs of this Second Amended Complaint as if fully set forth herein.

61. At least as of the date of service of the original Complaint, Ocean Semiconductor placed NVIDIA on actual notice of the ’322 patent and actual notice that its actions constituted and continued to constitute infringement of the ’322 patent. NVIDIA has had actual knowledge of the ’376 patent and its own infringement of the ’322 patent since at least that time. At least as of the date of service of this Second Amended Complaint, Ocean Semiconductor placed Defendants on actual notice of the ’322 patent and actual notice that its actions constitute infringement of the ’322 patent. Defendants have had actual knowledge of the ’322 patent and its own infringement of the ’322 patent since at least that time.

62. On information and belief, Defendants have directly infringed and continue to infringe at least claims 1, 2, and 4 of the ’322 patent literally or under the doctrine of equivalents, by importing into the United States, and/or using, and/or selling, and/or offering for sale in the United States, without authority or license, integrated circuits including all of the limitations of at least claims 1, 2, and 4 of the ’322 patent, and systems, products, and/or devices containing these integrated circuits including at least the NVIDIA Accused Products (“’322 Accused Products”) in violation of 35 U.S.C. § 271. The ’322 Accused Products include all of the limitations of at least claims 1, 2, and 4 of the ’376 patent.

63. Discovery is expected to uncover the full extent of Defendants’ infringement of the ’322 patent beyond the ’322 Accused Products already identified herein.

64. Specifically, on information and belief, Defendants have directly infringed and continue to infringe at least claims 1, 2, and 4 of the ’322 patent literally or under the doctrine of equivalents, by making, using, offering to sell, or selling in the United States, and/or by importing into the United States, without authority or license, the ’322 Accused Products, in violation of 35 U.S.C. § 271(a). On information and belief, Defendants import the ’322 Accused Products into

the United States for sale and distribution to customers located in the United States. On information and belief, Defendants sell and/or offers for sale the ’322 Accused Products in the United States. For example, Defendants provides direct sales through their own sales channels and/or their distributors or contract manufacturers and sells the ’322 Accused Products to businesses including original equipment manufacturers and electronic manufacturing service providers. On information and belief, these direct sales include sales of the ’322 Accused Products in the United States. On information and belief, Defendants offer the ’322 Accused Products for sale in the United States. For example, Defendants engage in sales, marketing, and contracting activity in the United States and/or with United States offices of its customers.

65. The ’322 Accused Products include all of the limitations of at least claims 1, 2, and 4 of the ’322 patent. For example, the ’322 Accused Products include an integrated circuit comprising a semiconductor substrate having source/drain junctions and a gate dielectric on the semiconductor substrate. *See*, *e.g.*, Exhibit 5. The ’322 Accused Products include a gate over the gate dielectric and ultra-uniform silicides on the source/drain junctions. *Id*. The ’322 Accused Products further include a dielectric layer above the semiconductor substrate and contacts in the dielectric layer to the ultra-uniform silicides. *Id*.

66. Attached hereto as Exhibit 5, and incorporated by reference herein, is a claim chart detailing how the NVIDIA GeForce RTX 2070 Super (TU104 GPU based on Turing architecture and made using a 12 nm production process at TSMC), which is manufactured by a NVIDIA Foundry Partner (TSMC) on behalf of NVIDIA, satisfies each element of at least claims 1, 2, and 4 of the ’322 patent, literally or under the doctrine of equivalents. On information and belief, the other ’322 Accused Products are also manufactured by a NVIDIA Foundry Partner (e.g., TSMC)

on behalf of NVIDIA and satisfy each element of at least claims 1, 2, and 4 of the ’322 patent, literally or under the doctrine of equivalents.

67. On information and belief, the ’322 Accused Products are neither materially changed by subsequent processes nor become trivial and nonessential components of another product.

68. On information and belief, at least as of the date of service of the original Complaint, NVIDIA has, and at least as of the date of service of this Second Amended Complaint Defendants have, induced and continue to induce others actively, knowingly, and intentionally, including its suppliers and contract manufacturers, to infringe one or more claims of the ’322 patent, including, but not limited to, claims 1, 2, and 4, pursuant to 35 U.S.C. § 271(b), by actively encouraging others to import into the United States, and/or make, use, sell, and/or offer to sell in the United States, the ’322 Accused Products or products containing the infringing semiconductor components of the ’322 Accused Products, by actively inducing others to infringe the ’322 patent by making, using, selling, offering for sale, marketing, advertising, and/or importing the Accused Products to their customers for use in downstream products that infringe, or were manufactured using processes that infringe, the ’322 patent, and by instructing others to infringe the ’322 patent.

69. For example, NVIDIA actively promotes the sale, use, and importation of the ’322 Accused Products in marketing materials, technical specifications, data sheets, web pages on its website (e.g., www.nvidia.com), press releases, training tutorials, development and design tools, user manuals, and developer forums as well as at trade shows (e.g., the Consumer Technology Association’s Consumer Electronics Show (“CES”)) and NVIDIA’s online Discussion Forums for GeForce products and developers) and through its sales and distribution channels that encourage infringing uses, sales, offers to sell, and importation of the ’322 Accused Products. As another

example, NVIDIA's representatives travel to customer sites in the United States for sales and support activity that includes working with customers to facilitate these customers' infringing testing, marketing, importation, and sales activity. On information and belief, NVIDIA supplies customers with '322 Accused Products so that they may be used, sold, or offered for sale by those customers. For example, NVIDIA provides direct sales to original equipment manufacturers and electronic manufacturing service providers. On information and belief, these direct sales include sales to customers in the United States. NVIDIA also promotes, publicly on its website, uses of the '322 Accused Products by customers in the United States. NVIDIA additionally provides a wide range of technical support to customers and businesses, including product-specific solutions. NVIDIA also encourages customers and other third parties to communicate directly with NVIDIA representatives about these products for purposes of technical assistance and repair (e.g., https://www.nvidia.com/en-us/support/enterprise/ and https://www.nvidia.com/en-us/support/consumer/).

70. TSMC actively promotes the sale, use, and importation of the '322 Accused Products through its sales and distribution channels in the United States that encourage infringing uses, sales, offers to sell, and importation of the '322 Accused Products. For example, TSMC supplies NVIDIA with '322 Accused Products so that they may be used, sold, or offered for sale by NVIDIA to original equipment manufacturers and electronic manufacturing service providers. On information and belief, these sales include sales to customers in the United States.

71. On information and belief, Defendants sell or offers for sale the '322 Accused Products to third parties that incorporate the '322 Accused Products into third party products ("the '322 Third Party Products").

72. On information and belief, Defendants assists third parties, directly and/or through intermediaries, in the development of the '322 Third Party Products and provides technical support and supports the sales of the '322 Third Party Products.

73. On information and belief, since at least as of the date of service of the original Complaint, NVIDIA has induced and continues to induce third parties with specific intent or willful blindness to import, make, use, sell, and/or offer to sell '322 Third Party Products that include at least one '322 Accused Product, whose make, use, sale, offer for sale, or importation constitutes direct infringement of at least one claim of the '322 patent. On information and belief, since at least as of the date of service of this Second Amended Complaint, Defendants have induced and continue to induce third parties with specific intent or willful blindness to import, make, use, sell, and/or offer to sell '322 Third Party Products that include at least one '322 Accused Product, whose make, use, sale, offer for sale, or importation constitutes direct infringement of at least one claim of the '322 patent.

74. On information and belief, the '322 Third Party Products are imported into the United States for use, sale, and/or offer for sale in this District and throughout the United States ("Imported '322 Third Party Products").

75. On information and belief, to the extent any entity other than Defendants, including but not limited to any of NVIDIA's other Foundry Partners or third-party importers, imports the '322 Accused Products and/or Imported '322 Third-Party Products into the United States for or on behalf of Defendants ("Third Party Importer"), Defendants are liable for inducement of infringement by the Third Party Importer. Defendants have encouraged the Third Party Importer to infringe the '322 patent and intended that it do so. This encouragement includes at least ordering or instructing the Third Party Importer to import the '322 Accused Products and/or '322 Third-

Party Products into the United States, providing directions and other materials to the Third Party Importer to enable such importation, and/or conditioning the receipt of benefits (included but not limited to payment) to the Third Party Importer on such importation. On information and belief, this behavior has continued since Defendants first became aware of the ’322 patent and the infringement thereof.

76. On information and belief, to the extent any entity other than Defendants, including but not limited to any of NVIDIA’s other Foundry Partners, uses the patented method to fabricate or manufacture the ’322 Accused Products and/or Imported ’322 Third-Party Products in the United States for or on behalf of Defendants (“Third Party Manufacturer”), Defendants are liable for inducement of infringement by the Third Party Manufacturer. Defendants haves encouraged the Third Party Manufacturer to infringe the ’322 patent and intended that it do so. This encouragement includes, without limitation, ordering the ’322 Accused Products from the Third Party Manufacturer since Defendants first became aware of the ’322 patent and its infringement by the Third Party Manufacturer.

77. Defendants have benefitted and continue to benefit from the importation into the United States of the ’322 Accused Products, ’322 Third Party Products, and Imported ’322 Third Party Products.

78. Ocean Semiconductor has suffered, and continues to suffer, damages as a result of Defendants’ infringement of the ’322 patent.

79. At least as of the date of service of the original Complaint, NVIDIA has infringed the ’322 patent knowingly, willfully, deliberately, and in disregard of Plaintiff’s patent rights, at least by performing acts of infringement with actual knowledge of its direct and indirect infringement or while remaining willfully blind to the fact of its direct and indirect infringement.

As a result of at least this conduct, Plaintiff is entitled to enhanced damages under 35 U.S.C. § 284 and to attorneys' fees and costs under 35 U.S.C. § 285. At least as of the date of service of this Second Amended Complaint, Defendants have infringed the '322 patent knowingly, willfully, deliberately, and in disregard of Plaintiff's patent rights, at least by performing acts of infringement with actual knowledge of its direct and indirect infringement or while remaining willfully blind to the fact of its direct and indirect infringement. As a result of at least this conduct, Plaintiff is entitled to enhanced damages under 35 U.S.C. § 284 and to attorneys' fees and costs under 35 U.S.C. § 285.

80. Ocean Semiconductor reserves the right to modify its infringement theories as discovery progresses in this case. Ocean Semiconductor shall not be estopped or otherwise limited or restricted for purposes of its infringement contentions or its claim constructions by the claim charts that it provides with this Second Amended Complaint. Ocean Semiconductor intends for the claim chart (Exhibit 5) for the '322 patent to satisfy the notice requirements of Rule 8(a)(2) of the Federal Rule of Civil Procedure. The claim chart is not Ocean Semiconductor's preliminary or final infringement contentions or preliminary or final claim construction positions.

**COUNT III: INFRINGEMENT OF U.S. PATENT NO. 7,629,211**

81. Plaintiff incorporates by reference the foregoing paragraphs of this Second Amended Complaint as if fully set forth herein.

82. At least as of the date of service of the original Complaint, Ocean Semiconductor placed NVIDIA on actual notice of the '211 patent and actual notice that its actions constituted and continued to constitute infringement of the '211 patent. NVIDIA has had actual knowledge of the '211 patent and its own infringement of the '211 patent since at least that time. At least as of the date of service of this Second Amended Complaint, Ocean Semiconductor placed

Defendants on actual notice of the ’211 patent and actual notice that its actions constitute infringement of the ’211 patent. Defendants have had actual knowledge of the ’211 patent and its own infringement of the ’211 patent since at least that time.

83. On information and belief, Defendants have directly infringed and continue to infringe at least claims 1 and 5 of the ’211 patent literally or under the doctrine of equivalents, by importing into the United States, and/or using, and/or selling, and/or offering for sale in the United States, without authority or license, integrated circuits that that are designed, developed, fabricated, and/or manufactured by a process including all of the limitations of at least claims 1 and 5 of the ’211 patent, and systems, products, and/or devices containing these integrated circuits including at least the NVIDIA Accused Products (“’211 Accused Products”) in violation of 35 U.S.C. § 271. The ’211 Accused Products are manufactured by a process including all of the limitations of at least claims 1 and 5 of the ’211 patent.

84. Discovery is expected to uncover the full extent of Defendants’ infringement of the ’211 patent beyond the ’211 Accused Products already identified herein.

85. Specifically, on information and belief, Defendants have directly infringed and continue to infringe at least claims 1 and 5 of the ’211 patent literally or under the doctrine of equivalents, by making, using, offering to sell, or selling in the United States, and/or by importing into the United States, without authority or license, the ’211 Accused Products, in violation of 35 U.S.C. § 271(a). In addition, Defendants have directly infringed and continue to directly infringe at least claims 1 and 5 of the ’211 patent literally or directly under the doctrine of equivalents, by importing into the United States and/or offering to sell, selling, or using within the United States, without authority or license, the ’211 Accused Products which are made by the process patented in the ’211 patent, without authority or license, in violation of 35 U.S.C. § 271(g).

On information and belief, Defendants import the '211 Accused Products into the United States for sale and distribution to customers located in the United States. On information and belief, Defendants sell and/or offers for sale the '211 Accused Products in the United States. For example, Defendants provide direct sales through their own sales channels and/or their distributors or contract manufacturers and sell the '211 Accused Products to businesses including original equipment manufacturers and electronic manufacturing service providers. On information and belief, these direct sales include sales of the '211 Accused Products in the United States. On information and belief, Defendants offer the '376 Accused Products for sale in the United States. For example, Defendants engage in sales, marketing, and contracting activity in the United States and/or with United States offices of its customers.

86. The '211 Accused Products are manufactured by a process including all of the limitations of at least claims 1 and 5 of the '211 patent. For example, during the manufacture of the '211 Accused Products, a field effect transistor is formed. *See*, *e.g.*, Exhibit 6. During manufacture, a semiconductor substrate is provided, and a gate electrode is formed above the semiconductor substrate. *Id*. At least one cavity in the substrate adjacent the gate electrode is formed, and a strain-creating element is formed in the at least one cavity. *Id*. The strain-creating element formed comprises a compound material comprising a first chemical element and a second chemical element. *Id*. The first chemical element comprises one of germanium and carbon, the second chemical element comprises silicon, and the semiconductor substrate comprises the second chemical element. *Id*. The strain-creating element further comprises a first portion and a second portion, wherein the second portion is located above the first portion. *Id*. The strain-creating element further comprises a first concentration ratio between a concentration of the first chemical element in the first portion and a concentration of the second chemical element in the first portion.

*Id*. The strain-creating element further comprises a second concentration ratio between a concentration of the first chemical element in the second portion and a concentration of the second chemical element in the second portion. *Id*. The first concentration ratio is smaller than said second concentration ratio, and a ratio between a concentration of the first chemical element and a concentration of the second chemical element increases in a vertical direction with increasing distance from a bottom surface of the at least one cavity formed in the substrate. *Id*.

87. Attached hereto as Exhibit 6, and incorporated by reference herein, is a claim chart detailing how the NVIDIA GeForce RTX 2070 Super (TU104 GPU based on Turing architecture and made using a 12 nm production process at TSMC), which is manufactured by a NVIDIA Foundry Partner (TSMC) on behalf of NVIDIA, satisfies each element of at least claims 1 and 5 of the ’211 patent, literally or under the doctrine of equivalents. On information and belief, the other ’211 Accused Products are also manufactured by a NVIDIA Foundry Partner (e.g., TSMC) on behalf of NVIDIA and satisfy each element of at least claims 1 and 5 of the ’211 patent, literally or under the doctrine of equivalents.

88. On information and belief, the ’211 Accused Products are neither materially changed by subsequent processes nor become trivial and nonessential components of another product.

89. On information and belief, at least as of the date of service of the original Complaint, NVIDIA has, and at least as of the date of service of this Second Amended Complaint Defendants have, induced and continues to induce others actively, knowingly, and intentionally, including its suppliers and contract manufacturers, to infringe one or more claims of the ’211 patent, including, but not limited to, claims 1 and 5, pursuant to 35 U.S.C. § 271(b), by actively encouraging others to import into the United States, and/or make, use, sell, and/or offer to sell in

the United States, the ’211 Accused Products or products containing the infringing semiconductor components of the ’211 Accused Products, by actively inducing others to infringe the ’211 patent by making, using, selling, offering for sale, marketing, advertising, and/or importing the Accused Products to their customers for use in downstream products that infringe, or were manufactured using processes that infringe, the ’211 patent, and by instructing others to infringe the ’211 patent.

90. For example, NVIDIA actively promotes the sale, use, and importation of the ’211 Accused Products in marketing materials, technical specifications, data sheets, web pages on its website (e.g., www.nvidia.com), press releases, training tutorials, development and design tools, user manuals, and developer forums as well as at trade shows (e.g., the Consumer Technology Association’s Consumer Electronics Show (“CES”)) and NVIDIA’s online Discussion Forums for GeForce products and developers) and through its sales and distribution channels that encourage infringing uses, sales, offers to sell, and importation of the ’211 Accused Products. As another example, NVIDIA’s representatives travel to customer sites in the United States for sales and support activity that includes working with customers to facilitate these customers’ infringing testing, marketing, importation, and sales activity. On information and belief, NVIDIA supplies customers with ’211 Accused Products so that they may be used, sold, or offered for sale by those customers. For example, NVIDIA provides direct sales to original equipment manufacturers and electronic manufacturing service providers. On information and belief, these direct sales include sales to customers in the United States. NVIDIA also promotes, publicly on its website, uses of the ’211 Accused Products by customers in the United States. NVIDIA additionally provides a wide range of technical support to customers and businesses, including product-specific solutions. NVIDIA also encourages customers and other third parties to communicate directly with NVIDIA representatives about these products for purposes of technical assistance and repair (e.g.,

https://www.nvidia.com/en-us/support/enterprise/ and https://www.nvidia.com/en-us/support/consumer/).

91. TSMC actively promotes the sale, use, and importation of the ’211 Accused Products through its sales and distribution channels in the United States that encourage infringing uses, sales, offers to sell, and importation of the ’211 Accused Products. For example, TSMC supplies NVIDIA with ’211 Accused Products so that they may be used, sold, or offered for sale by NVIDIA to original equipment manufacturers and electronic manufacturing service providers. On information and belief, these sales include sales to customers in the United States.

92. On information and belief, Defendants sell or offers for sale the ’211 Accused Products to third parties that incorporate the ’211 Accused Products into third party products (“the ’211 Third Party Products”).

93. On information and belief, Defendants assist third parties, directly and/or through intermediaries, in the development of the ’211 Third Party Products and provides technical support and supports the sales of the ’211 Third Party Products.

94. On information and belief, since at least as of the date of service of the original Complaint, NVIDIA has induced and continues to induce third parties with specific intent or willful blindness to import, make, use, sell, and/or offer to sell ’211 Third Party Products that include at least one ’211 Accused Product, whose make, use, sale, offer for sale, or importation constitutes direct infringement of at least one claim of the ’211 patent. On information and belief, since at least as of the date of service of this Second Amended Complaint, Defendants have induced and continue to induce third parties with specific intent or willful blindness to import, make, use, sell, and/or offer to sell ’211 Third Party Products that include at least one ’211 Accused

Product, whose make, use, sale, offer for sale, or importation constitutes direct infringement of at least one claim of the ’211 patent.

95. On information and belief, the ’211 Third Party Products are imported into the United States for use, sale, and/or offer for sale in this District and throughout the United States (“Imported ’211 Third Party Products”).

96. On information and belief, to the extent any entity other than Defendants, including but not limited to any of NVIDIA’s other Foundry Partners or third-party importers, imports the ’211 Accused Products and/or Imported ’211 Third-Party Products into the United States for or on behalf of Defendants (“Third Party Importer”), Defendants are liable for inducement of infringement by the Third Party Importer. Defendants have encouraged the Third Party Importer to infringe the ’211 patent and intended that it do so. This encouragement includes at least ordering or instructing the Third Party Importer to import the ’211 Accused Products and/or ’211 Third-Party Products into the United States, providing directions and other materials to the Third Party Importer to enable such importation, and/or conditioning the receipt of benefits (included but not limited to payment) to the Third Party Importer on such importation. On information and belief, this behavior has continued since Defendants first became aware of the ’211 patent and the infringement thereof.

97. On information and belief, to the extent any entity other than Defendants, including but not limited to any of NVIDIA’s other Foundry Partners, uses the patented method to fabricate or manufacture the ’211 Accused Products and/or Imported ’211 Third-Party Products in the United States for or on behalf of Defendants (“Third Party Manufacturer”), Defendants are liable for inducement of infringement by the Third Party Manufacturer. Defendants have encouraged the Third Party Manufacturer to infringe the ’211 patent and intended that it do so. This

encouragement includes, without limitation, ordering the ’211 Accused Products from the Third Party Manufacturer since Defendants first became aware of the ’211 patent and its infringement by the Third Party Manufacturer.

98. Defendants have benefitted and continue to benefit from the importation into the United States of the ’211 Accused Products, ’376 Third Party Products, and Imported ’211 Third Party Products.

99. Ocean Semiconductor has suffered, and continues to suffer, damages as a result of NVIDIA’s infringement of the ’211 patent.

100. At least as of the date of service of this Second Amended Complaint, NVIDIA has infringed the ’376 patent knowingly, willfully, deliberately, and in disregard of Plaintiff’s patent rights, at least by performing acts of infringement with actual knowledge of its direct and indirect infringement or while remaining willfully blind to the fact of its direct and indirect infringement. As a result of at least this conduct, Plaintiff is entitled to enhanced damages under 35 U.S.C. § 284 and to attorneys’ fees and costs under 35 U.S.C. § 285. At least as of the date of service of this Second Amended Complaint, Defendants have infringed the ’322 patent knowingly, willfully, deliberately, and in disregard of Plaintiff’s patent rights, at least by performing acts of infringement with actual knowledge of its direct and indirect infringement or while remaining willfully blind to the fact of its direct and indirect infringement. As a result of at least this conduct, Plaintiff is entitled to enhanced damages under 35 U.S.C. § 284 and to attorneys’ fees and costs under 35 U.S.C. § 285.

101. Ocean Semiconductor reserves the right to modify its infringement theories as discovery progresses in this case. Ocean Semiconductor shall not be estopped or otherwise limited or restricted for purposes of its infringement contentions or its claim constructions by the claim

charts that it provides with this Second Amended Complaint. Ocean Semiconductor intends for the claim chart (Exhibit 6) for the '211 patent to satisfy the notice requirements of Rule 8(a)(2) of the Federal Rule of Civil Procedure. The claim chart is not Ocean Semiconductor's preliminary or final infringement contentions or preliminary or final claim construction positions.

## PRAYER FOR RELIEF

WHEREFORE, Ocean Semiconductor prays for judgment against NVIDIA and TSMC as follows:

A. A judgment that Defendants have infringed, and continue to infringe, one or more claims of each of the Asserted Patents;

B. A judgment that Defendants have induced infringement, and continue to induce infringement, of one or more claims of each of the Asserted Patents;

C. A judgment that Defendants have contributed to, and continue to contribute to, the infringement of one or more claims of each of the Asserted Patents;

D. A judgment awarding Ocean Semiconductor damages to be paid by Defendants in an amount to be proven at trial adequate to compensate Ocean Semiconductor for Defendants' past infringement and any continuing or future infringement through the date such judgment is entered, but in no event less than a reasonable royalty for Defendants' infringement;

E. A judgment awarding Ocean Semiconductor treble damages pursuant to 35 U.S.C. § 284 as a result of Defendants' willfulness;

F. A judgment and order finding that this case is exceptional and awarding Ocean Semiconductor its reasonable attorneys' fees to be paid by Defendants pursuant to 35 U.S.C. § 285;

G. A judgment awarding expenses, costs, and disbursements in this action against Defendants, including pre-judgment and post-judgment interest;

H. A judgment granting a preliminary and permanent injunction that restrains and enjoins Defendants, their officers, directors, employees, agents, servants, parents, subsidiaries, successors, assigns, and all those in privity, concert or participation with them from directly or indirectly infringing the Asserted Patents; and

I. A judgment awarding Ocean Semiconductor such other relief as the Court may deem just and equitable.

**DEMAND FOR JURY TRIAL**

Pursuant to Federal Rule of Civil Procedure 38(b), Plaintiff hereby demands a trial by jury on all issues so triable.

Dated: July 28, 2022

Respectfully submitted,

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*Attorneys for Plaintiff Ocean Semiconductor LLC*

**CERTIFICATE OF SERVICE**

The undersigned certifies that a copy of the foregoing instrument has been served to all counsel of record per Local Rule CV-5(a)(3) on July 28, 2022.

*/s/ Taylor N. Mauze*
Taylor N. Mauze

# Exhibit 1

US007005376B2

(12) **United States Patent**
**Chiu et al.**

(10) **Patent No.: US 7,005,376 B2**
(45) **Date of Patent: Feb. 28, 2006**

(54) **ULTRA-UNIFORM SILICIDES IN INTEGRATED CIRCUIT TECHNOLOGY**


(75) Inventors: **Robert J. Chiu**, Santa Clara, CA (US); **Jeffrey P. Patton**, Santa Clara, CA (US); **Paul R. Besser**, Sunnyvale, CA (US); **Minh Van Ngo**, Fremont, CA (US)

(73) Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, CA (US)



( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 56 days.

(21) Appl. No.: **10/615,086**

(22) Filed: **Jul. 7, 2003**

(65) **Prior Publication Data**

US 2005/0006705 A1 Jan. 13, 2005

(51) **Int. Cl.**
***H01L 21/00*** (2006.01)

(52) **U.S. Cl.** ...................... **438/664**; 438/592; 438/586

(58) **Field of Classification Search** ................ 438/664, 438/592, 586

See application file for complete search history.


(56) **References Cited**


U.S. PATENT DOCUMENTS

4,443,930 A * 4/1984 Hwang et al. .............. 438/299
5,736,461 A 4/1998 Berti et al.
6,136,699 A 10/2000 Inoue
6,242,779 B1 6/2001 Maekawa
6,251,777 B1 * 6/2001 Jeng et al. .................. 438/682
6,365,507 B1 * 4/2002 Hu ............................ 438/627
6,495,460 B1 12/2002 Bertrand et al.
6,579,783 B1 * 6/2003 Saigal et al. ................ 438/581
2003/0104694 A1 6/2003 Maa et al.

FOREIGN PATENT DOCUMENTS

EP 0800204 A 10/1997
EP 0936664 A 8/1999

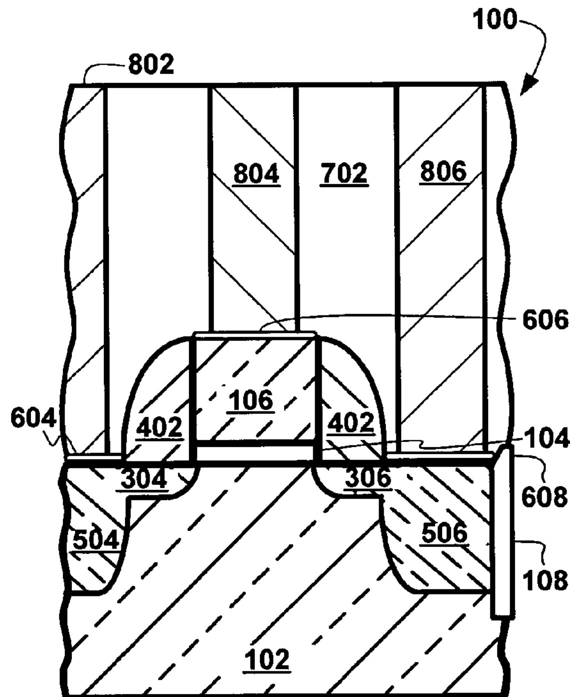
* cited by examiner


*Primary Examiner*—Laura M. Schillinger
(74) *Attorney, Agent, or Firm*—Mikio Ishimaru

(57) **ABSTRACT**


A method of forming and a structure of an integrated circuit are provided. A gate dielectric is formed on a semiconductor substrate, and a gate is formed over a gate dielectric on the semiconductor substrate. Source/drain junctions are formed in the semiconductor substrate. Ultra-uniform silicides are formed on the source/drain junctions, and a dielectric layer is deposited above the semiconductor substrate. Contacts are then formed in the dielectric layer to the ultra-uniform silicides.


**12 Claims, 3 Drawing Sheets**



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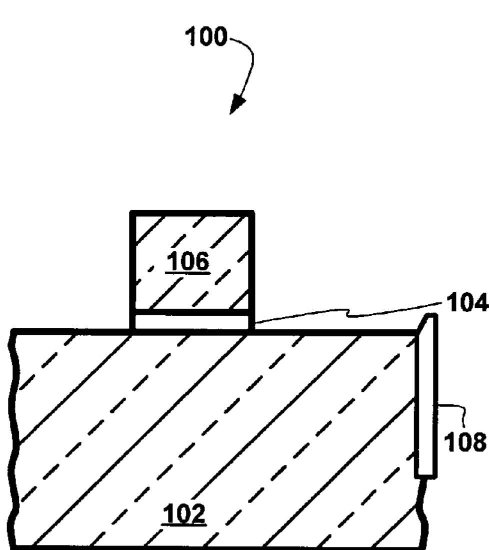

FIG. 1

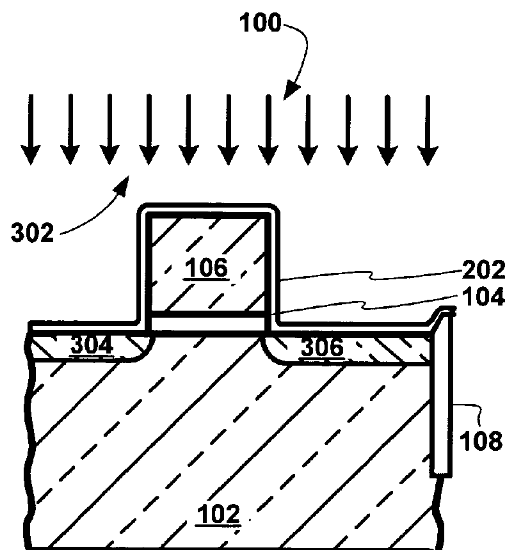

FIG.3

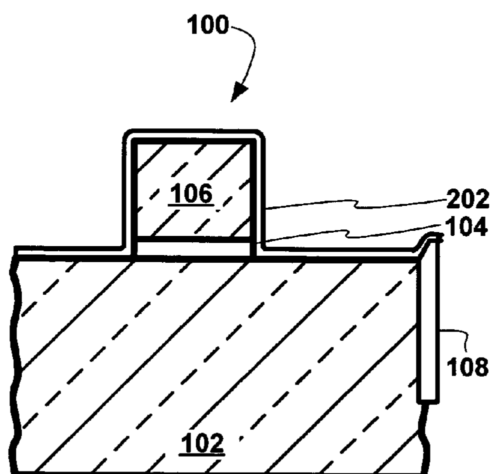

FIG. 2

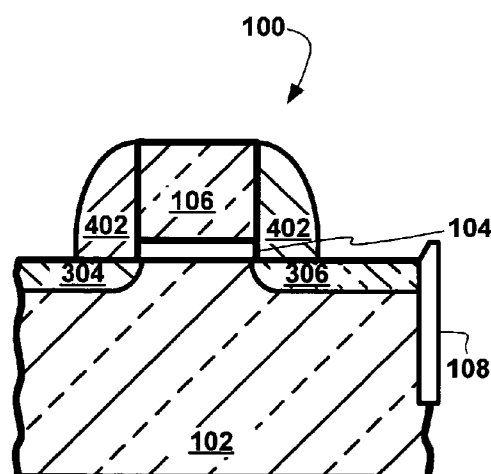

FIG. 4

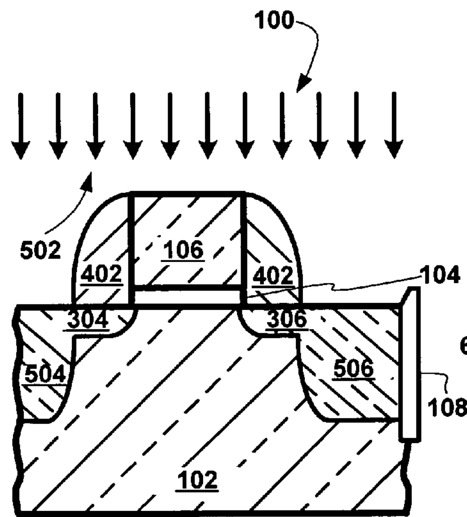


FIG. 5

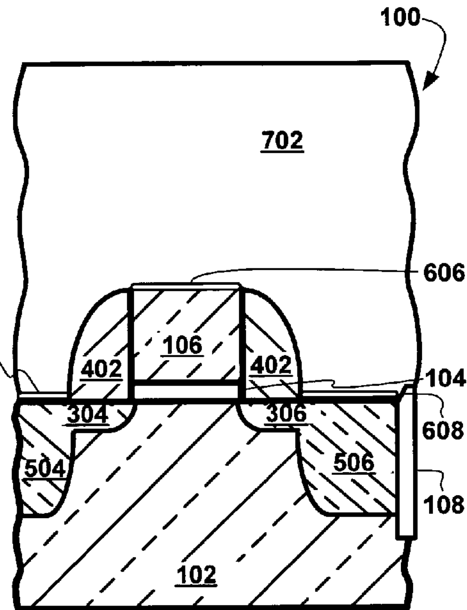


FIG. 7

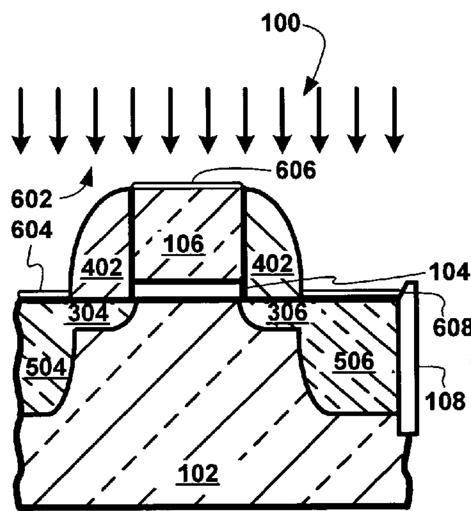


FIG. 6

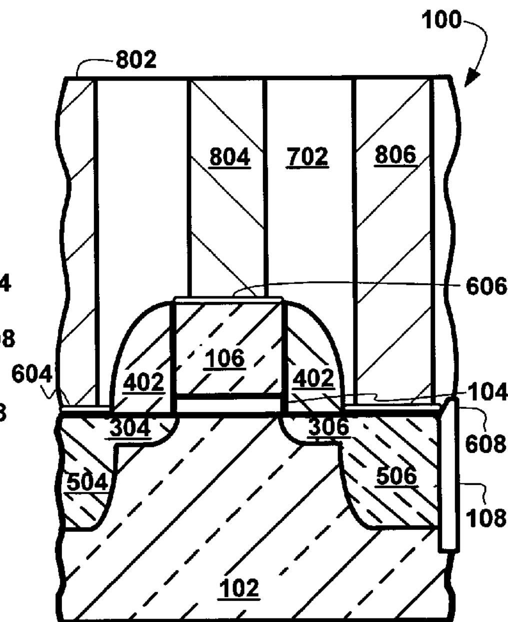


FIG. 8

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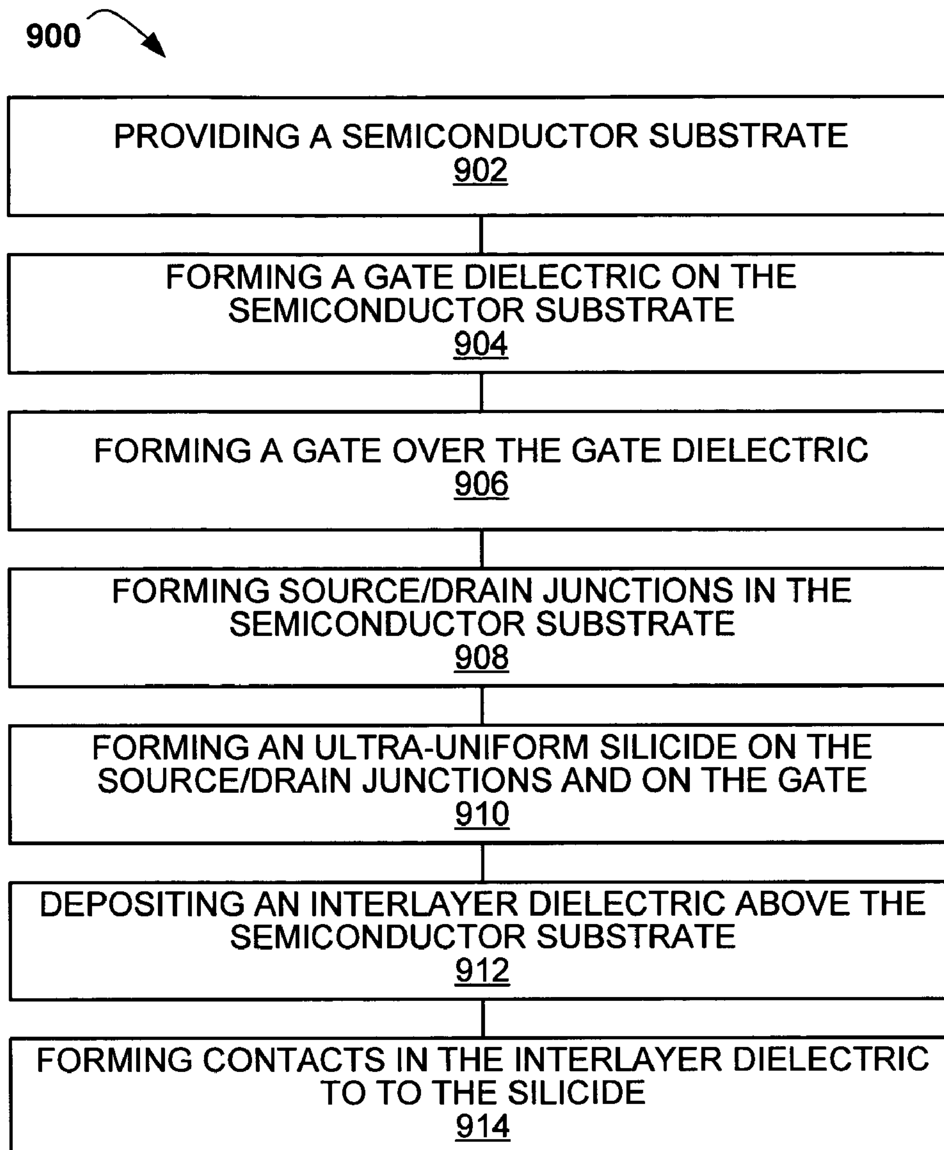


FIG. 9

# ULTRA-UNIFORM SILICIDES IN INTEGRATED CIRCUIT TECHNOLOGY

## BACKGROUND

1. Technical Field

The present invention relates generally to semiconductor technology, and more specifically to siliciding in semiconductor devices.

2. Background Art

At the present time, electronic products are used in almost every aspect of life, and the heart of these electronic products is the integrated circuit. Integrated circuits are used in everything from airplanes and televisions to wristwatches.

Integrated circuits are made in and on silicon wafers by extremely complex systems that require the coordination of hundreds or even thousands of precisely controlled processes to produce a finished semiconductor wafer. Each finished semiconductor wafer has hundreds to tens of thousands of integrated circuits, each worth hundreds or thousands of dollars.

Integrated circuits are made up of hundreds to millions of individual components. One common component is the semiconductor transistor. The most common and important semiconductor technology presently used is silicon-based, and the most preferred silicon-based semiconductor device is a Complementary Metal Oxide Semiconductor (CMOS) transistor.

The principal elements of a CMOS transistor generally consist of a silicon substrate having shallow trench oxide isolation regions cordoning off transistor areas. The transistor areas contain polysilicon gates on silicon oxide gates, or gate oxides, over the silicon substrate. The silicon substrate on both sides of the polysilicon gate is slightly doped to become conductive. The lightly doped regions of the silicon substrate are referred to as "shallow source/drain junctions", which are separated by a channel region beneath the polysilicon gate. A curved silicon oxide or silicon nitride spacer, referred to as a "sidewall spacer", on the sides of the polysilicon gate allows deposition of additional doping to form more heavily doped regions of the shallow source/drain junctions, which are called "deep source/drain junctions". The shallow and deep source/drain junctions are collectively referred to as "S/D junctions".

To complete the transistor, a silicon oxide dielectric layer is deposited to cover the polysilicon gate, the curved spacer, and the silicon substrate. To provide electrical connections for the transistor, openings are etched in the silicon oxide dielectric layer to the polysilicon gate and the source/drain junctions. The openings are filled with metal to form electrical contacts. To complete the integrated circuits, the contacts are connected to additional levels of wiring in additional levels of dielectric material to the outside of the dielectric material.

In operation, an input signal to the gate contact to the polysilicon gate controls the flow of electric current from one source/drain contact through one source/drain junction through the channel to the other source/drain junction and to the other source/drain contact.

Transistors are fabricated by thermally growing a gate oxide layer on the silicon substrate of a semiconductor wafer and forming a polysilicon layer over the gate oxide layer. The oxide layer and polysilicon layer are patterned and etched to form the gate oxides and polysilicon gates, respectively. The gate oxides and polysilicon gates in turn are used as masks to form the shallow source/drain regions by ion implantation of boron or phosphorus impurity atoms into the



surface of the silicon substrate. The ion implantation is followed by a high-temperature anneal above 700° C. to activate the implanted impurity atoms to form the shallow source/drain junctions.

A silicon nitride layer is deposited and etched to form sidewall spacers around the side surfaces of the gate oxides and polysilicon gates. The sidewall spacers, the gate oxides, and the polysilicon gates are used as masks for the conventional source/drain regions by ion implantation of boron or phosphorus impurity atoms into the surface of the silicon substrate into and through the shallow source/drain junctions. The ion implantation is again followed by a high-temperature anneal above 700° C. to activate the implanted impurity atoms to form the S/D junctions.

After formation of the transistors, a silicon oxide dielectric layer is deposited over the transistors and contact openings are etched down to the source/drain junctions and to the polysilicon gates. The contact openings are then filled with a conductive metal and interconnected by formation of conductive wires in other dielectric layers.

As transistors have decreased in size, it has been found that the electrical resistance between the metal contacts and the silicon substrate or the polysilicon has increased to the level where it negatively impacts the performance of the transistors. To lower the electrical resistance, a transition material is formed between the metal contacts and the silicon substrate or the polysilicon. The best transition materials have been found to be cobalt silicide ($CoSi_2$) and titanium silicide ($TiSi_2$).

The silicides are formed by first applying a thin layer of the cobalt or titanium on the silicon substrate above the source/drain junctions and the polysilicon gates. The semiconductor wafer is subjected to one or more annealing steps at temperatures above 800° C. and this causes the cobalt or titanium to selectively react with the silicon and the polysilicon to form the metal silicide. The process is generally referred to as "siliciding". Since the shallow trench oxide and the sidewall spacers will not react to form a silicide, the silicides are aligned over the source/drain junctions and the polysilicon gates so the process is also referred to as "self-aligned siliciding", or "saliciding".

However, existing siliciding and saliciding have not succeeded in solving all the problems related to connecting the metal contacts to silicon.

The problems include, but are not limited to, high resistance between metal contacts and the silicide.

Solutions to these problems have been long sought but prior developments have not taught or suggested any solutions and, thus, solutions to these problems have long eluded those skilled in the art.

## DISCLOSURE OF THE INVENTION

The present invention provides a method of forming and a structure of an integrated circuit. A gate dielectric is formed on a semiconductor substrate, and a gate is formed over a gate dielectric on the semiconductor substrate. Source/drain junctions are formed in the semiconductor substrate. An ultra-uniform silicide is formed on the source/drain junctions, and a dielectric layer is deposited above the semiconductor substrate. Contacts are then formed in the dielectric layer to the ultra-uniform silicide. This method significantly increases robustness and lowers the electrical resistance between the contacts and the silicon greatly improving performance of the integrated circuit.

Certain embodiments of the invention have other advantages in addition to or in place of those mentioned above.

The advantages will become apparent to those skilled in the art from a reading of the following detailed description when taken with reference to the accompanying drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a view of a transistor in an intermediate stage of fabrication in accordance with the present invention;

FIG. **2** is the structure of FIG. **1** with a liner layer deposited thereon;

FIG. **3** is the structure of FIG. **2** during ion implantation to form shallow source/drain junctions;

FIG. **4** is the structure of FIG. **3** after formation of a sidewall spacer;

FIG. **5** is the structure of FIG. **4** during ion implantation to form deep source/drain junctions;

FIG. **6** is the structure of FIG.**5** during the formation of silicide;

FIG. **7** is the structure of FIG. **6** after deposition of a dielectric layer over the silicide, the sidewall spacer, and shallow trench isolation;

FIG. **8** is the structure of FIG. **7** after formation of metal contacts; and

FIG. **9** is a simplified flow chart of the method of manufacturing the silicide in accordance with the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

In the following description, numerous specific details are given to provide a thorough understanding of the invention. However, it will be apparent to one skilled in the art that the invention may be practiced without these specific details. In order to avoid obscuring the present invention, some well-known configurations and process steps are not disclosed in detail. In addition, the drawings showing embodiments of the apparatus are semi-diagrammatic and not to scale and, particularly, some of the dimensions are for the clarity of presentation and may be exaggerated in the drawing FIGs. The same numbers will be used in all the drawing FIGS. to relate to the same elements.

The term "horizontal" as used herein is defined as a plane parallel to a substrate or wafer. The term "vertical" refers to a direction perpendicular to the horizontal as just defined. Terms, such as "on", "above", "below", "bottom", "top", "side" (as in "sidewall"), "higher", "lower", "over", and "under", are defined with respect to the horizontal plane.

Referring now to FIG. **1**, therein is shown a integrated circuit **100** in an intermediate stage of fabrication in accordance with the present invention.

To form the intermediate stage, a gate dielectric layer, such as silicon oxide, has been deposited on a semiconductor substrate **102** of a material such as silicon and a conductive gate layer, such as polysilicon, has been deposited over the gate dielectric layer. The layers are patterned and etched to form a gate dielectric **104** and a gate **106**. The semiconductor substrate **102** has been further patterned, etched, and filled with a silicon oxide material to form a shallow trench isolation (STI) **108**.

Referring now to FIG. **2**, therein is shown the structure of FIG. **1** having a liner layer **202** deposited thereon. The liner layer **202**, generally of silicon oxide, covers the semiconductor substrate **102**, the gate dielectric **104**, the gate **106**, and the STI **108**. The liner layer **202** can be of an etch stop material or an implant-protection material.

Referring now to FIG. **3**, therein is shown the structure of FIG. **2** during an ion implantation **302** to form shallow source/drain junctions **304** and **306**.

The gate **106** and the gate dielectric **104** act as masks for the formation of shallow source/drain junctions **304** and **306** by the ion implantation **302** of boron (B) or phosphorus (P) impurity atoms into the surface of the semiconductor substrate **102**. The ion implantation **302** is followed by a high-temperature anneal above 700° C. to activate the implanted impurity atoms to form the shallow source/drain junctions **304** and **306**.

Referring now to FIG. **4**, therein is shown the structure of FIG. **3** after formation of a sidewall spacer **402**.

The liner layer **202**, which protects from implant damage has been removed and a sidewall spacer layer, generally of silicon nitride, has been deposited and etched to form the curved shape of the sidewall spacer **402**.

Referring now to FIG. **5**, therein is shown the structure of FIG. **4** during an ion implantation **502** to form deep source/drain junctions **504** and **506**.

The sidewall spacer **402**, the gate **106**, and the STI **108**, act as masks for the formation of the deep source/drain junctions **504** and **506** by the ion implantation **502** of boron or phosphorus impurity atoms into the surface of the semiconductor substrate **102** and into and through the shallow source/drain junctions **304** and **306**, respectively. The ion implantation **502** is again followed by a high-temperature anneal above 700° C. to activate the implanted impurity atoms to form the source/drain junctions **504** and **506**.

Referring now to FIG. **6**, therein is shown a deposition process **602** used in the formation of ultra-uniform silicides **604**, **606**, and **608** in accordance with the present invention. The ultra-uniform silicides **604** and **608** are formed with the silicon surface of the semiconductor substrate **102** over the deep source/drain junctions **504** and **506**, respectively, and the ultra-uniform silicide **606** is formed with the polysilicon surface of the gate **106**.

There are three ways in which to form silicides. In one technique, the deposition process **602** deposits a pure metal on exposed silicon areas (both single crystalline and polycrystalline silicon). Thereafter, the metal is reacted with the silicon to form what is known as a first phase, metal-rich silicide. The non-reacted metal is then removed, and the pre-existing first phase product is then reacted again with the underlying silicon to form a second phase, silicon-rich silicide. In a second technique, the deposition process **602** involves co-evaporation of both metal and silicon onto the exposed silicon. Both metal and silicon are vaporized by, for example, an electron beam. The vapor is then drawn onto the wafer and across the silicon. In a third technique, the deposition process **602** involves co-sputtering both metal and silicon onto the silicon surface. Co-sputtering entails physically dislodging metal and silicon materials from a composite target or separate targets, and then directing the composite material onto the wafer.

Conventional salicidation processes have become problematic with modem semiconductor devices that have shallow source/drain junctions, e.g., junction depths on the order of 1000 Angstroms (Å). In particular, during such salicidation processes, some of the existing source/drain regions are consumed.

When cobalt is used as the refractory metal, it consumes about twice its thickness of silicon in the process of being converted to a metal silicide, e.g., a 100 Å layer of cobalt consumes about 103 Å of silicon. Such consumption acts to reduce the dopant present in the source/drain junctions and may adversely impact the electrical performance character-

istics of the source/drain junctions, and ultimately, degrades the performance of the integrated circuit.

When the refractory metal is titanium, titanium silicide forms between metal contacts because the sidewall spacer becomes smaller with smaller integrated circuits thereby allowing a capacitive-coupled or fully conductive path between the polysilicon gate and the source/drain junctions, and similarly, degrades the performance of the integrated circuit.

While the present invention may be used with various refractory metal silicides, it has been found that nickel silicide has many desirable characteristics. However, in working with nickel silicide, it has been found to be difficult to form robust nickel. It has been thought that thick silicides around 100 Å thick with rough surfaces would best protect the silicon substrate and provide good adhesion.

After much investigation, it has been discovered contrary to conventional wisdom that an ultra-uniform nickel silicide will form extremely robust nickel silicide. By definition, an ultra-uniform silicide means a layer of silicide where there are no variations in thickness greater than about 3% of the overall thickness.

One example of forming ultra-uniform nickel ultra-uniform silicides **604**, **606**, and **608**, has been discovered to be by depositing the nickel on the exposed silicon areas by a very low power vapor deposition process, where the very low power means a power level below 500 watts direct current and preferably between about 400 and 300 watts direct current.

In addition, it has been discovered that an extra slow rate of metal deposition must be used which is defined to be below 7.0 Å per second and preferably between about 6.8 and 6.0 Å per second.

Still further, it has been discovered that the nickel must be deposited under these power levels and deposition rates to an ultra-thin thickness of not more than 50 Å thickness in order to provide an ultra-uniform, ultra-thin silicide. The nickel is then converted to a nickel silicide by an annealing process, such as a high-temperature anneal around 700° C.

The above greatly improves robustness and lowers the electrical resistance between the contacts and the silicon or polysilicon greatly improving performance of the integrated circuit.

Referring now to FIG. **7**, therein is shown the structure of FIG. **6** after deposition of a dielectric layer **702** over the ultra-uniform silicides **604**, **606**, and **608**, the sidewall spacer **402**, and the STI **108**.

In various embodiments, the dielectric layer **702** are of medium dielectric constant dielectric materials such as silicon oxide ($SiO_x$), tetraethylorthosilicate (TEOS), borophosphosilicate (BPSG) glass, etc. with dielectric constants from 4.2 to 3.9 or low dielectric constant dielectric materials such as fluorinated tetraethylorthosilicate (FTEOS), hydrogen silsesquioxane (HSQ), bis-benzocyclobutene (BCB), tetramethylorthosilicate (TMOS), octamethyleyclotetrasiloxane (OMCTS), hexamethyldisiloxane (HMDS), trimethylsilil borxle (SOB), diaceloxyditerliarybutosiloxane (DADBS), trimethylsilil phosphate (SOP), etc. with dielectric constants below 3.9 to 2.5. Ultra-low dielectric constant dielectric materials, having dielectric constants below 2.5 and which are available, include commercially available Teflon-AF, Teflon microemulsion, polimide nanofoams, silica aerogels, silica xerogels, and mesoporous silica. Stop layers and capping layers (where used) are of materials such as silicon nitride ($Si_xN_x$) or silicon oxynitride (SiON).

Referring now to FIG. **8**, therein is shown the structure of FIG. **7** after formation of metal contacts **802**, **804**, and **806**.

The metal contacts **802**, **804**, and **806** are respectively electrically connected to the ultra-uniform silicides **604**, **606**, and **608**, and respectively to the deep source/drain junction **504**, the gate **106**, and the deep source/drain junction **506**.

In various embodiments, the metal contacts **802**, **804**, and **806** are of metals such as tantalum (Ta), titanium (Ti), tungsten (W), alloys thereof, and compounds thereof. In other embodiments, the metal contacts **802**, **804**, and **806** are of metals such as copper (Cu), gold (Au), silver (Ag), alloys thereof, and compounds thereof with one or more of the above elements with diffusion barriers around them.

Referring now to FIG. **9**, therein is shown a simplified flow chart of the method **900** of manufacturing the ultra-uniform silicides **604**, **606**, and **608** in accordance with the present invention. The method **900** includes: providing a semiconductor substrate in a step **902**; forming a gate dielectric on the semiconductor substrate in a step **904**; forming a gate over the gate dielectric in a step **906**; forming source/drain junctions in the semiconductor substrate in a step **908**; forming ultra-uniform silicides on the source/drain junctions and on the gate in a step **910**; depositing a dielectric layer above the semiconductor substrate in a step **912**; and forming contacts in the dielectric layer to the ultra-uniform silicide in a step **914**.

While the invention has been described in conjunction with a specific best mode, it is to be understood that many alternatives, modifications, and variations will be apparent to those skilled in the art in light of the aforegoing description. Accordingly, it is intended to embrace all such alternatives, modifications, and variations that fall within the spirit and scope of the included claims. All matters hither-to-fore set forth or shown in the accompanying drawings are to be interpreted in an illustrative and non-limiting sense.

The invention claimed is:

**1**. A method of forming an integrated circuit comprising:
- providing a semiconductor substrate;
- forming a gate dielectric on the semiconductor substrate;
- forming a gate over the gate dielectric;
- forming source/drain junctions in the semiconductor substrate;
- forming ultra-uniform silicides on the source/drain junctions;
- depositing a dielectric layer above the semiconductor substrate; and
- forming contacts in the dielectric layer to the ultra-uniform silicides.

**2**. The method as claimed in claim **1** wherein:
- forming the ultra-uniform silicides uses a very low power deposition technique using a power level below 500 watts direct current.

**3**. The method as claimed in claim **1** wherein:
- forming the ultra-uniform silicides uses an extra slow rate of deposition of a silicide metal below 7.0 Å per second.

**4**. The method as claimed in claim **1** wherein:
- forming the ultra-uniform silicides forms an ultra-thin thickness of a silicide metal of not more than 50 Å thick.

**5**. The method as claimed in claim **1** wherein:
- depositing the dielectric layer deposits a dielectric material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants.

**6**. The method as claimed in claim **1** wherein:

forming the contacts to the ultra-uniform silicides uses materials selected from a group consisting of tantalum, titanium, tungsten, copper, gold, silver, an alloy thereof, a compound thereof, and a combination thereof.

**7**. A method of forming an integrated circuit comprising:

providing a silicon substrate;

forming a gate oxide on the silicon substrate;

forming a polysilicon gate over the gate oxide;

forming source/drain junctions in the silicon substrate;

forming an ultra-uniform nickel silicide having no variations in thickness greater than 3% of the overall thickness on the source/drain junctions and on the gate;

depositing a dielectric layer above the silicon substrate; and

forming contacts in the dielectric layer to the ultra-uniform nickel silicide.

**8**. The method as claimed in claim **7** wherein:

forming the ultra-uniform nickel silicide uses a vapor deposition using a power level below 400 watts direct current.

**9**. The method as claimed in claim **7** wherein:

forming the ultra-uniform nickel silicide uses an extra slow rate of deposition of nickel below 6.8 Å per second; and

additionally comprising:

an annealing of the nickel to the ultra-uniform nickel silicide.

**10**. The method as claimed in claim **7** wherein:

forming the ultra-uniform nickel silicide uses an ultra-thin thickness of nickel of not more than 50 Å thickness.

**11**. The method as claimed in claim **7** wherein:

depositing the dielectric layer deposits a dielectric material having a dielectric constant below 4.2.

**12**. The method as claimed in claim **7** wherein:

forming the contacts to the ultra-uniform silicides uses materials selected from a group consisting of tantalum, titanium, tungsten copper, gold, silver, an alloy thereof, a compound thereof, and a combination thereof.

* * * * *

# Exhibit 2

US007307322B2

(12) **United States Patent**
**Chiu et al.**

(10) **Patent No.: US 7,307,322 B2**
(45) **Date of Patent: Dec. 11, 2007**

(54) **ULTRA-UNIFORM SILICIDE SYSTEM IN INTEGRATED CIRCUIT TECHNOLOGY**

(75) Inventors: **Robert J. Chiu**, Santa Clara, CA (US); **Jeffrey P. Patton**, Santa Clara, CA (US); **Paul R. Besser**, Sunnyvale, CA (US); **Minh Van Ngo**, Fremont, CA (US)

(73) Assignee: **Adavnced Micro Devices, Inc.**, Sunnyvale, CA (US)

( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 33 days.

(21) Appl. No.: **11/252,493**

(22) Filed: **Oct. 17, 2005**

(65) **Prior Publication Data**

US 2006/0267107 A1 Nov. 30, 2006

**Related U.S. Application Data**

(62) Division of application No. 10/615,086, filed on Jul. 7, 2003, now Pat. No. 7,005,376.

(51) **Int. Cl.**
***H01L 29/76*** (2006.01)

(52) **U.S. Cl.** ...................... **257/384**; 257/383; 438/664; 438/586; 438/592

(58) **Field of Classification Search** ................ 257/382, 257/384, 388, 412, 377, 413, 454, 456, 455, 257/486, 576, 383, E21.439, E21.619, E21.634
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,443,930 A 4/1984 Hwang et al.
5,736,461 A 4/1998 Berti et al.
6,136,699 A 10/2000 Inoue
6,242,779 B1 6/2001 Maekawa
6,251,777 B1 6/2001 Jeng et al.
6,365,507 B1 4/2002 Hu
6,495,460 B1 12/2002 Bertrand et al.
6,498,067 B1 * 12/2002 Perng et al. ................ 438/305
6,579,783 B2 6/2003 Saigal et al.
6,720,258 B2 4/2004 Maa et al.
2003/0008450 A1 * 1/2003 Tsai et al. ................... 438/200

FOREIGN PATENT DOCUMENTS

EP 0800204 A 10/1997
EP 0936664 A 8/1999

* cited by examiner

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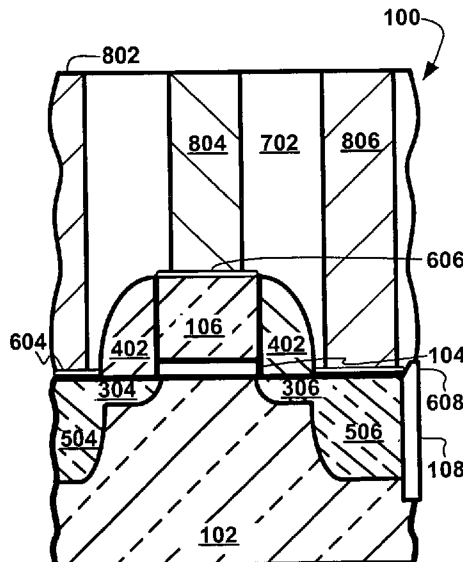
(74) *Attorney, Agent, or Firm*—Mikio Ishimaru

(57) **ABSTRACT**

A structure of an integrated circuit is provided. A gate dielectric is formed on a semiconductor substrate, and a gate is formed over a gate dielectric on the semiconductor substrate. Source/drain junctions are formed in the semiconductor substrate. Ultra-uniform suicides are formed on the source/drain junctions, and a dielectric layer is deposited above the semiconductor substrate. Contacts are then formed in the dielectric layer to the ultra-uniform silicides.

**8 Claims, 3 Drawing Sheets**



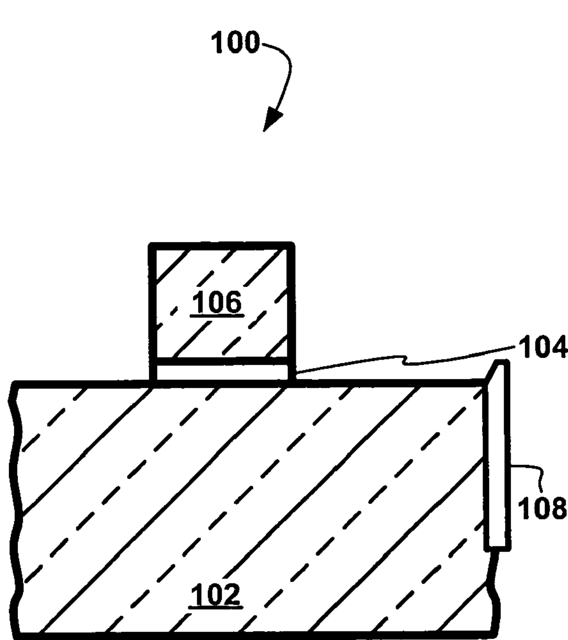



FIG. 1

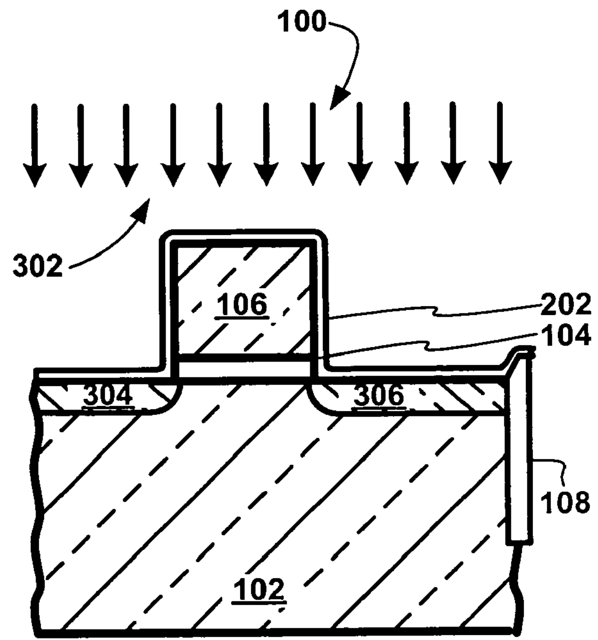



FIG.3

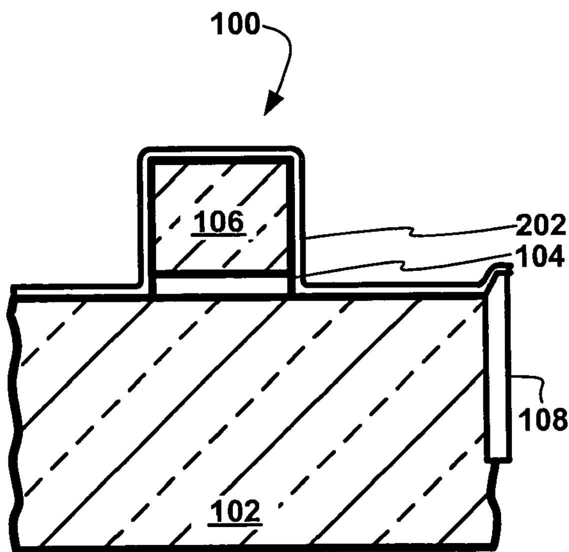



FIG. 2

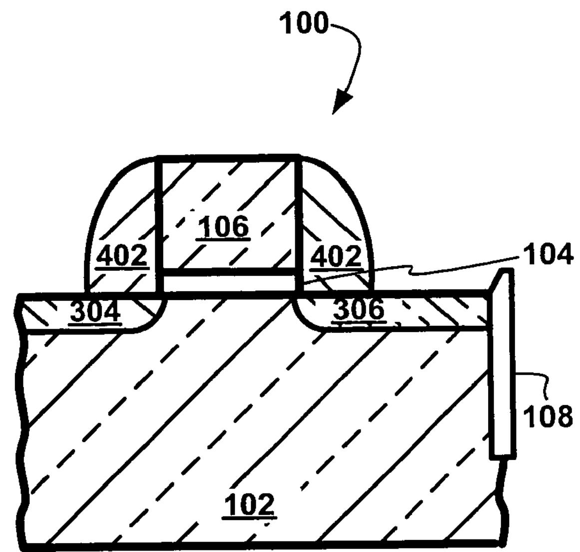



FIG. 4

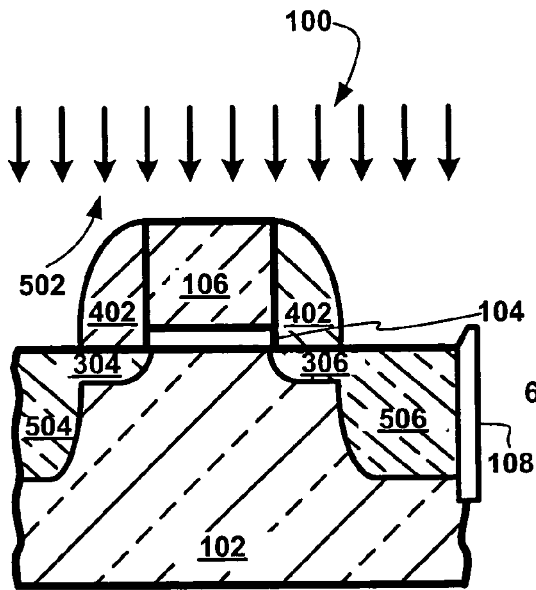



FIG. 5

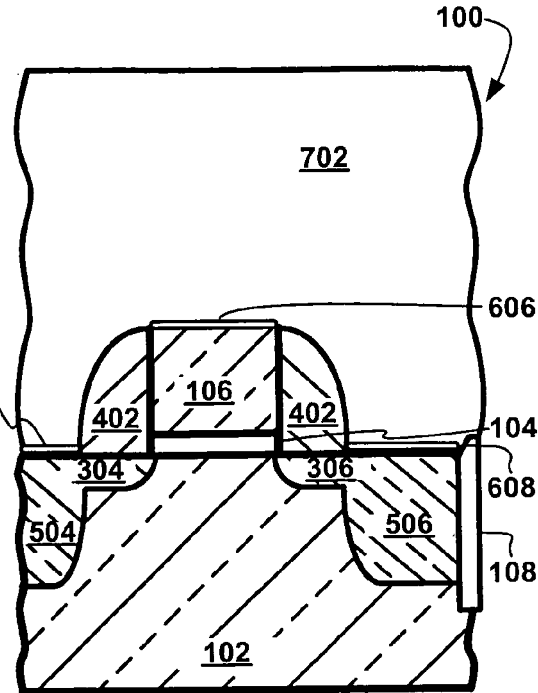



FIG. 7

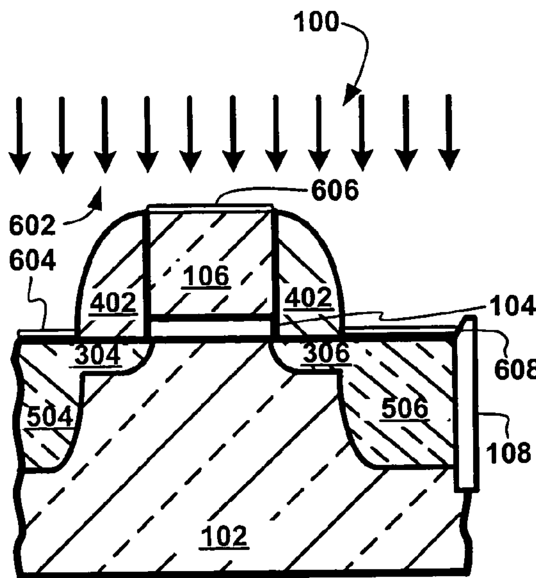



FIG. 6

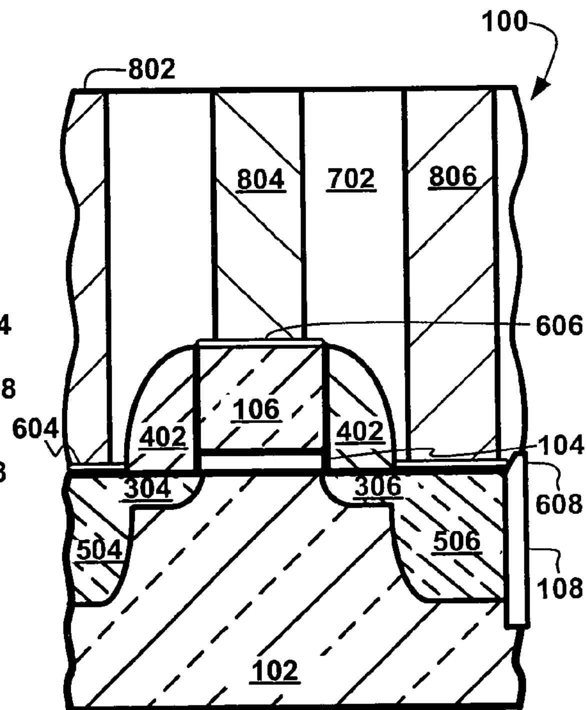



FIG. 8

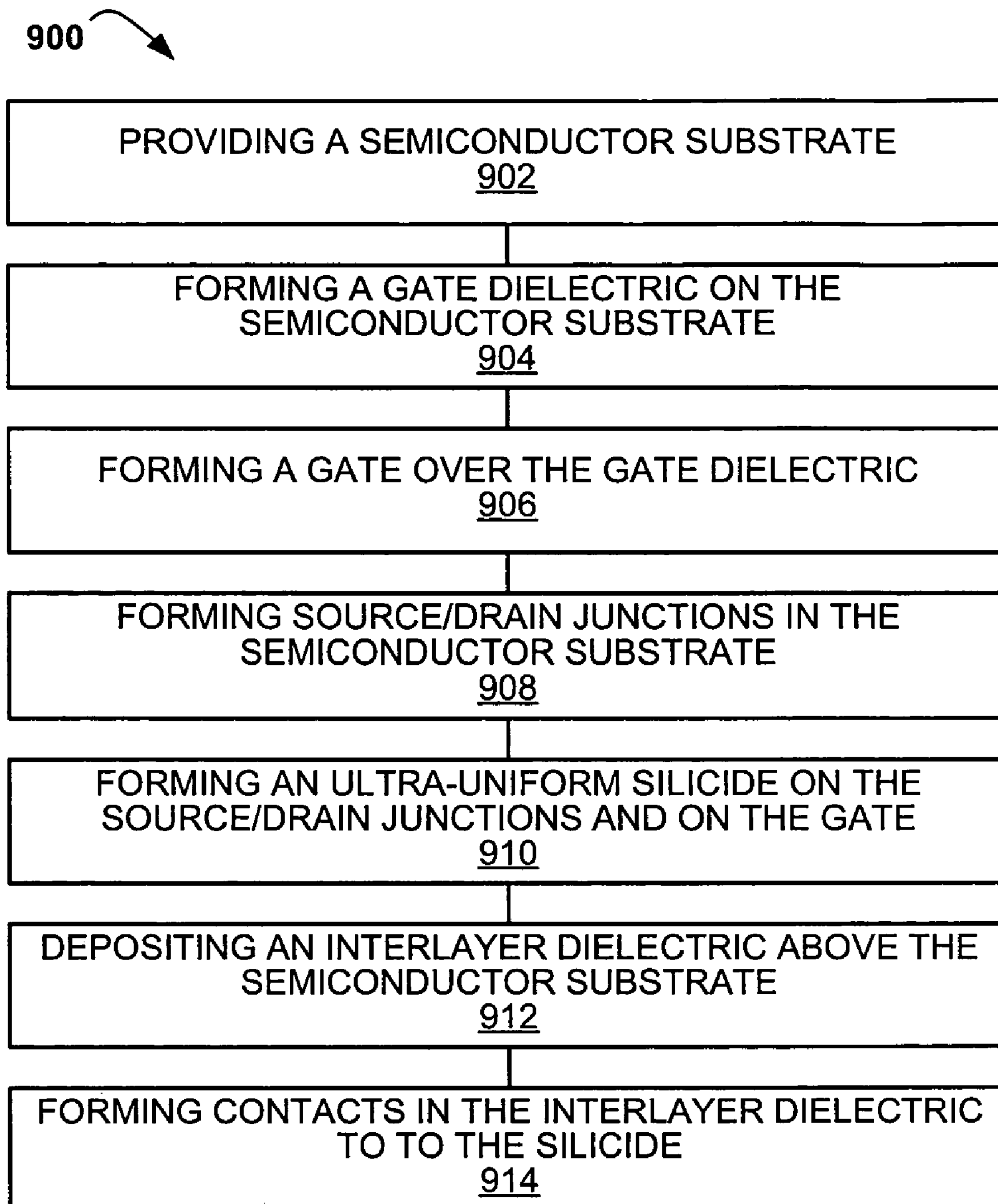



FIG. 9

## ULTRA-UNIFORM SILICIDE SYSTEM IN INTEGRATED CIRCUIT TECHNOLOGY

### CROSS REFERENCE TO RELATED APPLICATIONS

This is a divisional of application Ser. No. 10/615,086, filed on Jul. 7, 2003 now U.S. Pat. No. 7,005,376, which is incorporated herein by reference thereto.

### BACKGROUND

1. Technical Field

The present invention relates generally to semiconductor technology, and more specifically to siliciding in semiconductor devices.

2. Background Art

At the present time, electronic products are used in almost every aspect of life, and the heart of these electronic products is the integrated circuit. Integrated circuits are used in everything from airplanes and televisions to wristwatches.

Integrated circuits are made in and on silicon wafers by extremely complex systems that require the coordination of hundreds or even thousands of precisely controlled processes to produce a finished semiconductor wafer. Each finished semiconductor wafer has hundreds to tens of thousands of integrated circuits, each worth hundreds or thousands of dollars.

Integrated circuits are made up of hundreds to millions of individual components. One common component is the semiconductor transistor. The most common and important semiconductor technology presently used is silicon-based, and the most preferred silicon-based semiconductor device is a Complementary Metal Oxide Semiconductor (CMOS) transistor.

The principal elements of a CMOS transistor generally consist of a silicon substrate having shallow trench oxide isolation regions cordoning off transistor areas. The transistor areas contain polysilicon gates on silicon oxide gates, or gate oxides, over the silicon substrate. The silicon substrate on both sides of the polysilicon gate is slightly doped to become conductive. The lightly doped regions of the silicon substrate are referred to as "shallow source/drain junctions", which are separated by a channel region beneath the polysilicon gate. A curved silicon oxide or silicon nitride spacer, referred to as a "sidewall spacer", on the sides of the polysilicon gate allows deposition of additional doping to form more heavily doped regions of the shallow source/drain junctions, which are called "deep source/drain junctions". The shallow and deep source/drain junctions are collectively referred to as "S/D junctions".

To complete the transistor, a silicon oxide dielectric layer is deposited to cover the polysilicon gate, the curved spacer, and the silicon substrate. To provide electrical connections for the transistor, openings are etched in the silicon oxide dielectric layer to the polysilicon gate and the source/drain junctions. The openings are filled with metal to form electrical contacts. To complete the integrated circuits, the contacts are connected to additional levels of wiring in additional levels of dielectric material to the outside of the dielectric material.

In operation, an input signal to the gate contact to the polysilicon gate controls the flow of electric current from one source/drain contact through one source/drain junction through the channel to the other source/drain junction and to the other source/drain contact.



Transistors are fabricated by thermally growing a gate oxide layer on the silicon substrate of a semiconductor wafer and forming a polysilicon layer over the gate oxide layer. The oxide layer and polysilicon layer are patterned and etched to form the gate oxides and polysilicon gates, respectively. The gate oxides and polysilicon gates in turn are used as masks to form the shallow source/drain regions by ion implantation of boron or phosphorus impurity atoms into the surface of the silicon substrate. The ion implantation is followed by a high-temperature anneal above 700° C. to activate the implanted impurity atoms to form the shallow source/drain junctions.

A silicon nitride layer is deposited and etched to form sidewall spacers around the side surfaces of the gate oxides and polysilicon gates. The sidewall spacers, the gate oxides, and the polysilicon gates are used as masks for the conventional source/drain regions by ion implantation of boron or phosphorus impurity atoms into the surface of the silicon substrate into and through the shallow source/drain junctions. The ion implantation is again followed by a high-temperature anneal above 700° C. to activate the implanted impurity atoms to form the S/D junctions.

After formation of the transistors, a silicon oxide dielectric layer is deposited over the transistors and contact openings are etched down to the source/drain junctions and to the polysilicon gates. The contact openings are then filled with a conductive metal and interconnected by formation of conductive wires in other dielectric layers.

As transistors have decreased in size, it has been found that the electrical resistance between the metal contacts and the silicon substrate or the polysilicon has increased to the level where it negatively impacts the performance of the transistors. To lower the electrical resistance, a transition material is formed between the metal contacts and the silicon substrate or the polysilicon. The best transition materials have been found to be cobalt silicide ($CoSi_2$) and titanium silicide ($TiSi_2$).

The silicides are formed by first applying a thin layer of the cobalt or titanium on the silicon substrate above the source/drain junctions and the polysilicon gates. The semiconductor wafer is subjected to one or more annealing steps at temperatures above 800° C. and this causes the cobalt or titanium to selectively react with the silicon and the polysilicon to form the metal silicide. The process is generally referred to as "siliciding". Since the shallow trench oxide and the sidewall spacers will not react to form a silicide, the silicides are aligned over the source/drain junctions and the polysilicon gates so the process is also referred to as "self-aligned siliciding", or "saliciding".

However, existing siliciding and saliciding have not succeeded in solving all the problems related to connecting the metal contacts to silicon.

The problems include, but are not limited to, high resistance between metal contacts and the silicide.

Solutions to these problems have been long sought but prior developments have not taught or suggested any solutions and, thus, solutions to these problems have long eluded those skilled in the art.

### DISCLOSURE OF THE INVENTION

The present invention provides a structure of an integrated circuit. A gate dielectric is formed on a semiconductor substrate, and a gate is formed over a gate dielectric on the semiconductor substrate. Source/drain junctions are formed in the semiconductor substrate. An ultra-uniform silicide is formed on the source/drain junctions, and a dielectric layer

is deposited above the semiconductor substrate. Contacts are then formed in the dielectric layer to the ultra-uniform silicide. This method significantly increases robustness and lowers the electrical resistance between the contacts and the silicon greatly improving performance of the integrated circuit.

Certain embodiments of the invention have other advantages in addition to or in place of those mentioned above. The advantages will become apparent to those skilled in the art from a reading of the following detailed description when taken with reference to the accompanying drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a view of a transistor in an intermediate stage of fabrication in accordance with the present invention;

FIG. **2** is the structure of FIG. **1** with a liner layer deposited thereon;

FIG. **3** is the structure of FIG. **2** during ion implantation to form shallow source/drain junctions;

FIG. **4** is the structure of FIG. **3** after formation of a sidewall spacer;

FIG. **5** is the structure of FIG. **4** during ion implantation to form deep source/drain junctions;

FIG. **6** is the structure of FIG. **5** during the formation of silicide;

FIG. **7** is the structure of FIG. **6** after deposition of a dielectric layer over the silicide, the sidewall spacer, and shallow trench isolation;

FIG. **8** is the structure of FIG. **7** after formation of metal contacts; and

FIG. **9** is a simplified flow chart of the method of manufacturing the silicide in accordance with the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

In the following description, numerous specific details are given to provide a thorough understanding of the invention. However, it will be apparent to one skilled in the art that the invention may be practiced without these specific details. In order to avoid obscuring the present invention, some well-known configurations and process steps are not disclosed in detail. In addition, the drawings showing embodiments of the apparatus are semi-diagrammatic and not to scale and, particularly, some of the dimensions are for the clarity of presentation and may be exaggerated in the drawing FIGS. The same numbers will be used in all the drawing FIGS. to relate to the same elements.

The term "horizontal" as used herein is defined as a plane parallel to a substrate or wafer. The term "vertical" refers to a direction perpendicular to the horizontal as just defined. Terms, such as "on", "above", "below", "bottom", "top", "side" (as in "sidewall"), "higher", "lower", "over", and "under", are defined with respect to the horizontal plane.

Referring now to FIG. **1**, therein is shown a integrated circuit **100** in an intermediate stage of fabrication in accordance with the present invention.

To form the intermediate stage, a gate dielectric layer, such as silicon oxide, has been deposited on a semiconductor substrate **102** of a material such as silicon and a conductive gate layer, such as polysilicon, has been deposited over the gate dielectric layer. The layers are patterned and etched to form a gate dielectric **104** and a gate **106**. The semiconductor substrate **102** has been further patterned, etched, and filled with a silicon oxide material to form a shallow trench isolation (STI) **108**.

Referring now to FIG. **2**, therein is shown the structure of FIG. **1** having a liner layer **202** deposited thereon. The liner layer **202**, generally of silicon oxide, covers the semiconductor substrate **102**, the gate dielectric **104**, the gate **106**, and the STI **108**. The liner layer **202** can be of an etch stop material or an implant-protection material.

Referring now to FIG. **3**, therein is shown the structure of FIG. **2** during an ion implantation **302** to form shallow source/drain junctions **304** and **306**.

The gate **106** and the gate dielectric **104** act as masks for the formation of shallow source/drain junctions **304** and **306** by the ion implantation **302** of boron (B) or phosphorus (P) impurity atoms into the surface of the semiconductor substrate **102**. The ion implantation **302** is followed by a high-temperature anneal above 700° C. to activate the implanted impurity atoms to form the shallow source/drain junctions **304** and **306**.

Referring now to FIG. **4**, therein is shown the structure of FIG. **3** after formation of a sidewall spacer **402**.

The liner layer **202**, which protects from implant damage has been removed and a sidewall spacer layer, generally of silicon nitride, has been deposited and etched to form the curved shape of the sidewall spacer **402**.

Referring now to FIG. **5**, therein is shown the structure of FIG. **4** during an ion implantation **502** to form deep source/drain junctions **504** and **506**.

The sidewall spacer **402**, the gate **106**, and the STI **108**, act as masks for the formation of the deep source/drain junctions **504** and **506** by the ion implantation **502** of boron or phosphorus impurity atoms into the surface of the semiconductor substrate **102** and into and through the shallow source/drain junctions **304** and **306**, respectively. The ion implantation **502** is again followed by a high-temperature anneal above 700° C. to activate the implanted impurity atoms to form the source/drain junctions **504** and **506**.

Referring now to FIG. **6**, therein is shown a deposition process **602** used in the formation of ultra-uniform suicides **604**, **606**, and **608** in accordance with the present invention. The ultra-uniform silicides **604** and **608** are formed with the silicon surface of the semiconductor substrate **102** over the deep source/drain junctions **504** and **506**, respectively, and the ultra-uniform silicide **606** is formed with the polysilicon surface of the gate **106**.

There are three ways in which to form silicides. In one technique, the deposition process **602** deposits a pure metal on exposed silicon areas (both single crystalline and polycrystalline silicon). Thereafter, the metal is reacted with the silicon to form what is known as a first phase, metal-rich silicide. The non-reacted metal is then removed, and the pre-existing first phase product is then reacted again with the underlying silicon to form a second phase, silicon-rich silicide. In a second technique, the deposition process **602** involves co-evaporation of both metal and silicon onto the exposed silicon. Both metal and silicon are vaporized by, for example, an electron beam. The vapor is then drawn onto the wafer and across the silicon. In a third technique, the deposition process **602** involves co-sputtering both metal and silicon onto the silicon surface. Co-sputtering entails physically dislodging metal and silicon materials from a composite target or separate targets, and then directing the composite material onto the wafer.

Conventional salicidation processes have become problematic with modem semiconductor devices that have shallow source/drain junctions, e.g., junction depths on the order

of 1000 Angstroms (Å). In particular, during such salicidation processes, some of the existing source/drain regions are consumed.

When cobalt is used as the refractory metal, it consumes about twice its thickness of silicon in the process of being converted to a metal silicide, e.g., a 100 Å layer of cobalt consumes about 103 Å of silicon. Such consumption acts to reduce the dopant present in the source/drain junctions and may adversely impact the electrical performance characteristics of the source/drain junctions, and ultimately, degrades the performance of the integrated circuit.

When the refractory metal is titanium, titanium silicide forms between metal contacts because the sidewall spacer becomes smaller with smaller integrated circuits thereby allowing a capacitive-coupled or fully conductive path between the polysilicon gate and the source/drain junctions, and similarly, degrades the performance of the integrated circuit.

While the present invention may be used with various refractory metal silicides, it has been found that nickel silicide has many desirable characteristics. However, in working with nickel silicide, it has been found to be difficult to form robust nickel. It has been thought that thick suicides around 100 Å thick with rough surfaces would best protect the silicon substrate and provide good adhesion.

After much investigation, it has been discovered contrary to conventional wisdom that an ultra-uniform nickel silicide will form extremely robust nickel silicide. By definition, an ultra-uniform silicide means a layer of silicide where there are no variations in thickness greater than about 3% of the overall thickness.

One example of forming ultra-uniform nickel ultra-uniform silicides **604**, **606**, and **608**, has been discovered to be by depositing the nickel on the exposed silicon areas by a very low power vapor deposition process, where the very low power means a power level below 500 watts direct current and preferably between about 400 and 300 watts direct current.

In addition, it has been discovered that an extra slow rate of metal deposition must be used which is defined to be below 7.0 Å per second and preferably between about 6.8 and 6.0 Å per second.

Still further, it has been discovered that the nickel must be deposited under these power levels and deposition rates to an ultra-thin thickness of not more than 50 Å thickness in order to provide an ultra-uniform, ultra-thin silicide. The nickel is then converted to a nickel silicide by an annealing process, such as a high-temperature anneal around 700° C.

The above greatly improves robustness and lowers the electrical resistance between the contacts and the silicon or polysilicon greatly improving performance of the integrated circuit.

Referring now to FIG. **7**, therein is shown the structure of FIG. **6** after deposition of a dielectric layer **702** over the ultra-uniform silicides **604**, **606**, and **608**, the sidewall spacer **402**, and the STI **108**.

In various embodiments, the dielectric layer **702** are of medium dielectric constant dielectric materials such as silicon oxide ($SiO_x$), tetraethylorthosilicate (TEOS), borophosphosilicate (BPSG) glass, etc. with dielectric constants from 4.2 to 3.9 or low dielectric constant dielectric materials such as fluorinated tetraethylorthosilicate (FTEOS), hydrogen silsesquioxane (HSQ), bis-benzocyclobutene (BCB), tetramethylorthosilicate (TMOS), octamethyleyclotetrasiloxane (OMCTS), hexamethyldisiloxane (HMDS), trimethylsilil borxle (SOB), diaceloxyditerliarybutosiloxane (DADBS), trimethylsilil phosphate (SOP), etc. with dielectric constants below 3.9 to 2.5. Ultra-low dielectric constant dielectric materials, having dielectric constants below 2.5 and which are available, include commercially available Teflon-AF, Teflon microemulsion, polimide nanofoams, silica aerogels, silica xerogels, and mesoporous silica. Stop layers and capping layers (where used) are of materials such as silicon nitride ($Si_xN_x$) or silicon oxynitride (SiON).

Referring now to FIG. **8**, therein is shown the structure of FIG. **7** after formation of metal contacts **802**, **804**, and **806**. The metal contacts **802**, **804**, and **806** are respectively electrically connected to the ultra-uniform suicides **604**, **606**, and **608**, and respectively to the deep source/drain junction **504**, the gate **106**, and the deep source/drain junction **506**.

In various embodiments, the metal contacts **802**, **804**, and **806** are of metals such as tantalum (Ta), titanium (Ti), tungsten (W), alloys thereof, and compounds thereof. In other embodiments, the metal contacts **802**, **804**, and **806** are of metals such as copper (Cu), gold (Au), silver (Ag), alloys thereof, and compounds thereof with one or more of the above elements with diffusion barriers around them.

Referring now to FIG. **9**, therein is shown a simplified flow chart of the method **900** of manufacturing the ultra-uniform silicides **604**, **606**, and **608** in accordance with the present invention. The method **900** includes: providing a semiconductor substrate in a step **902**; forming a gate dielectric on the semiconductor substrate in a step **904**; forming a gate over the gate dielectric in a step **906**; forming source/drain junctions in the semiconductor substrate in a step **908**; forming ultra-uniform silicides on the source/drain junctions and on the gate in a step **910**; depositing a dielectric layer above the semiconductor substrate in a step **912**; and forming contacts in the dielectric layer to the ultra-uniform silicide in a step **914**.

While the invention has been described in conjunction with a specific best mode, it is to be understood that many alternatives, modifications, and variations will be apparent to those skilled in the art in light of the aforegoing description. Accordingly, it is intended to embrace all such alternatives, modifications, and variations that fall within the spirit and scope of the included claims. All matters hither-to-fore set forth or shown in the accompanying drawings are to be interpreted in an illustrative and non-limiting sense.

The invention claimed is:

**1**. An integrated circuit comprising:
a semiconductor substrate having source/drain junctions;
a gate dielectric on the semiconductor substrate;
a gate over the gate dielectric;
ultra-uniform silicides on the source/drain junctions;
a dielectric layer above the semiconductor substrate; and
contacts in the dielectric layer to the ultra-uniform silicides.

**2**. The integrated circuit as claimed in claim **1** wherein:
the ultra-uniform silicides is an ultra-thin thickness of a silicide metal of not more than 50 Å thick.

**3**. The integrated circuit as claimed in claim **1** wherein:
the dielectric layer deposits a dielectric material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants.

**4**. The integrated circuit as claimed in claim **1** wherein:
the contacts to the ultra-uniform silicides are of materials selected from a group consisting of tantalum, titanium, tungsten, copper, gold, silver, an alloy thereof, a compound thereof, and a combination thereof.

**5**. An integrated circuit comprising:
a silicon substrate having source/drain junctions;
a gate oxide on the silicon substrate;
a polysilicon gate over the gate oxide;

an ultra-uniform nickel silicide on the source/drain junctions and the polysilicon gate, the ultra-uniform nickel silicide having no variations in thickness greater than 3% of the overall thickness;

a dielectric layer above the silicon substrate; and

contacts in the dielectric layer to the ultra-uniform nickel silicide.

**6**. The integrated circuit as claimed in claim **5** wherein:

the ultra-uniform nickel silicide is an ultra-thin thickness of a silicide metal of not more than 50 Å thickness.

**7**. The integrated circuit as claimed in claim **5** wherein:

the dielectric layer is a dielectric material having a dielectric constant below 4.2.

**8**. The integrated circuit as claimed in claim **5** wherein:

the contacts to the ultra-uniform silicides are of materials selected from a group consisting of tantalum, titanium, tungsten copper, gold, silver, an alloy thereof, a compound thereof, and a combination thereof.

* * * * *

# Exhibit 3

US007629211B2

(12) **United States Patent**
**Beyer et al.**

(10) **Patent No.: US 7,629,211 B2**
(45) **Date of Patent: Dec. 8, 2009**

(54) **FIELD EFFECT TRANSISTOR AND METHOD OF FORMING A FIELD EFFECT TRANSISTOR**

(75) Inventors: **Sven Beyer**, Dresden (DE); **Thorsten Kammler**, Ottendorf-Okrilla (DE); **Rolf Stephan**, Dresden (DE); **Manfred Horstmann**, Duehrrroersdorf-Dittersbach (DE)

(73) Assignee: **Advanced Micro Devices, Inc.**, Austin, TX (US)

( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 101 days.

(21) Appl. No.: **11/684,211**

(22) Filed: **Mar. 9, 2007**

(65) **Prior Publication Data**

US 2008/0026531 A1 Jan. 31, 2008

(30) **Foreign Application Priority Data**

Jul. 31, 2006 (DE) ....................... 10 2006 035 665

(51) **Int. Cl.**
***H01L 21/331*** (2006.01)
***H01L 21/8234*** (2006.01)

(52) **U.S. Cl.** ....................... **438/199**; 438/206; 438/214; 438/350; 438/357; 438/360; 257/E21.419; 257/E21.428

(58) **Field of Classification Search** .......... 257/E21.419, 257/E21.428

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

| | | | | |
|---|---|---|---|---|
| 7,545,006 | B2 * | 6/2009 | Chen et al. | 257/382 |
| 2005/0093075 | A1 * | 5/2005 | Bentum et al. | 257/368 |
| 2005/0184345 | A1 | 8/2005 | Lin et al. | 257/375 |
| 2006/0292776 | A1 * | 12/2006 | Jin et al. | 438/197 |

FOREIGN PATENT DOCUMENTS

| | | | |
|---|---|---|---|
| WO | WO 2006/011939 | A2 | 2/2006 |
| WO | WO 2006/066194 | A2 | 6/2006 |

* cited by examiner

*Primary Examiner*—Charles D Garber
*Assistant Examiner*—Mohsen Ahmadi
(74) *Attorney, Agent, or Firm*—Williams, Morgan & Amerson, P.C.

(57) **ABSTRACT**

A method of forming a field effect transistor comprises providing a semiconductor substrate, a gate electrode being formed over the semiconductor substrate. At least one cavity is formed adjacent the gate electrode. A strain-creating element is formed in the at least one cavity. The strain-creating element comprises a compound material comprising a first chemical element and a second chemical element. A first concentration ratio between a concentration of the first chemical element in a first portion of the strain-creating element and a concentration of the second chemical element in the first portion of the strain-creating element is different from a second concentration ratio between a concentration of the first chemical element in a second portion of the strain-creating element and a concentration of the second chemical element in the second strain-creating element.

**7 Claims, 6 Drawing Sheets**

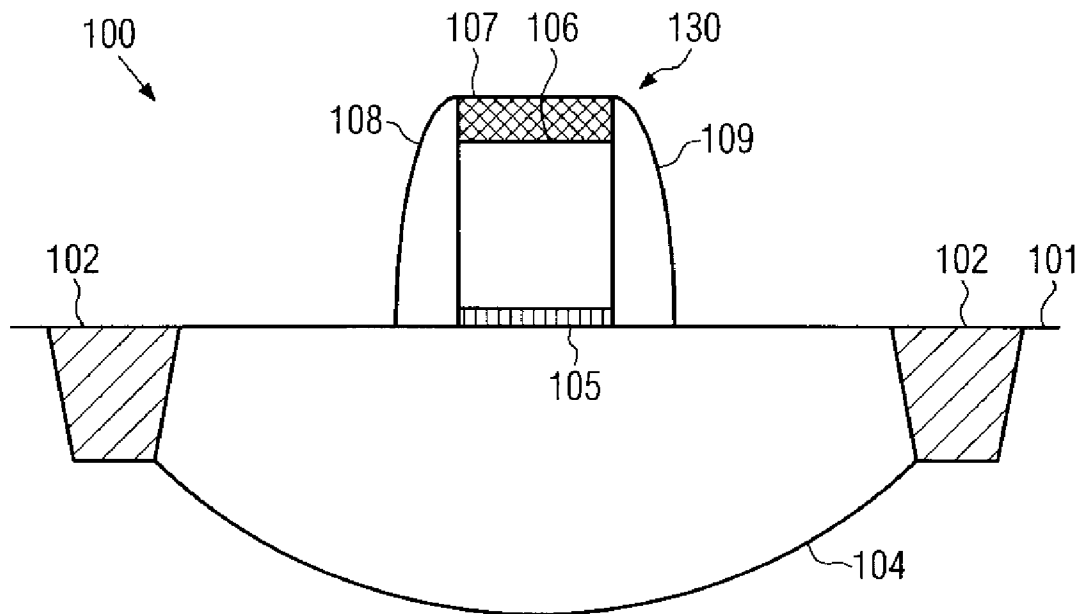



FIG. 1a
(prior art)

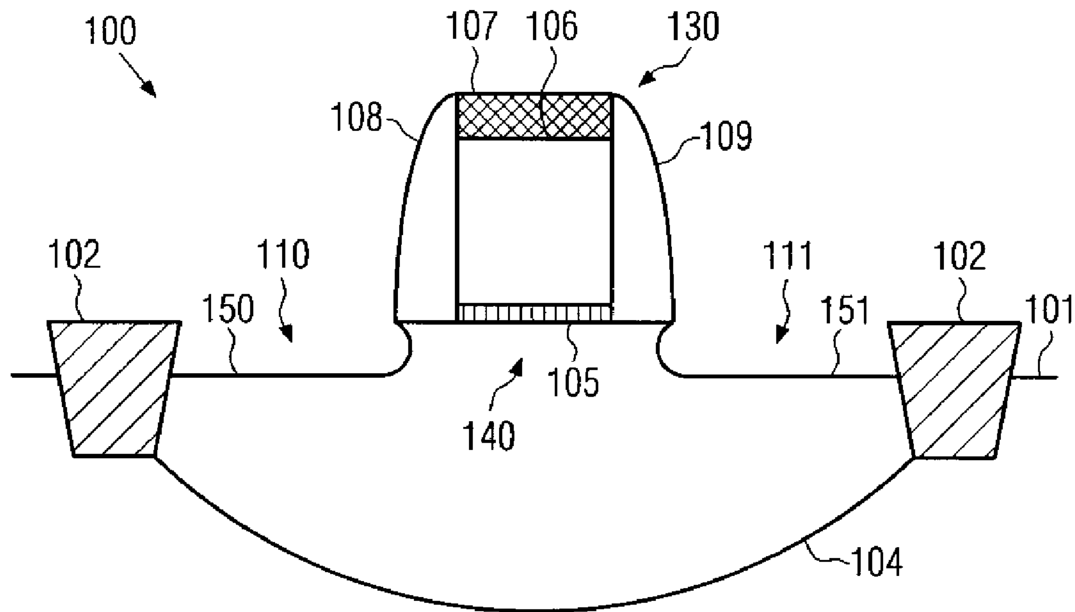



FIG. 1b
(prior art)

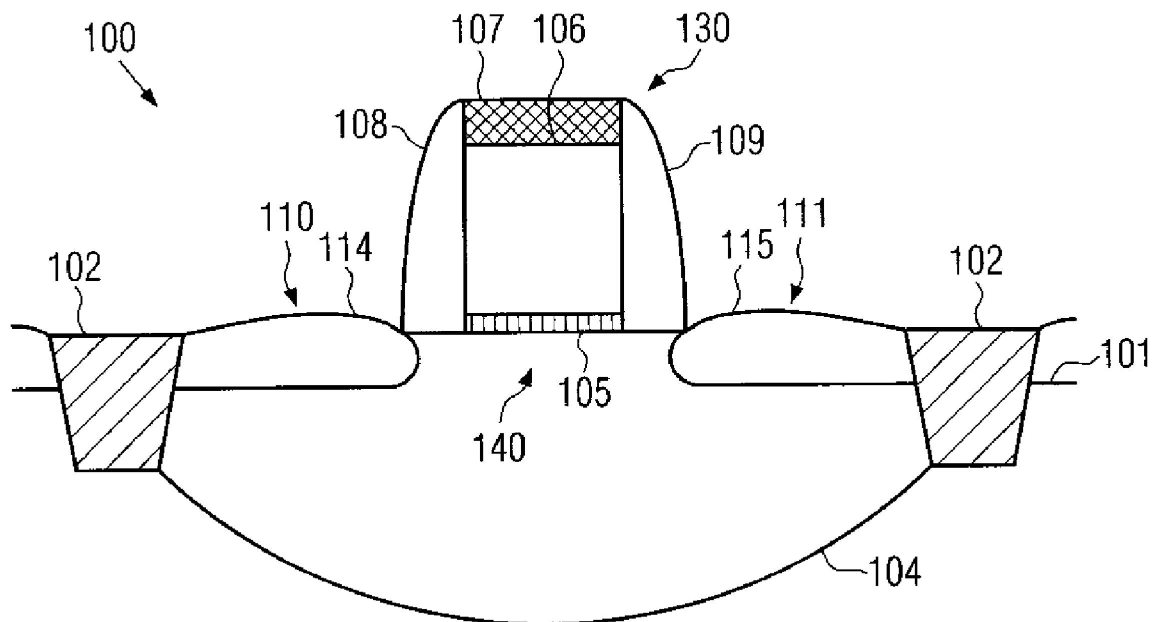



FIG. 1c
(prior art)

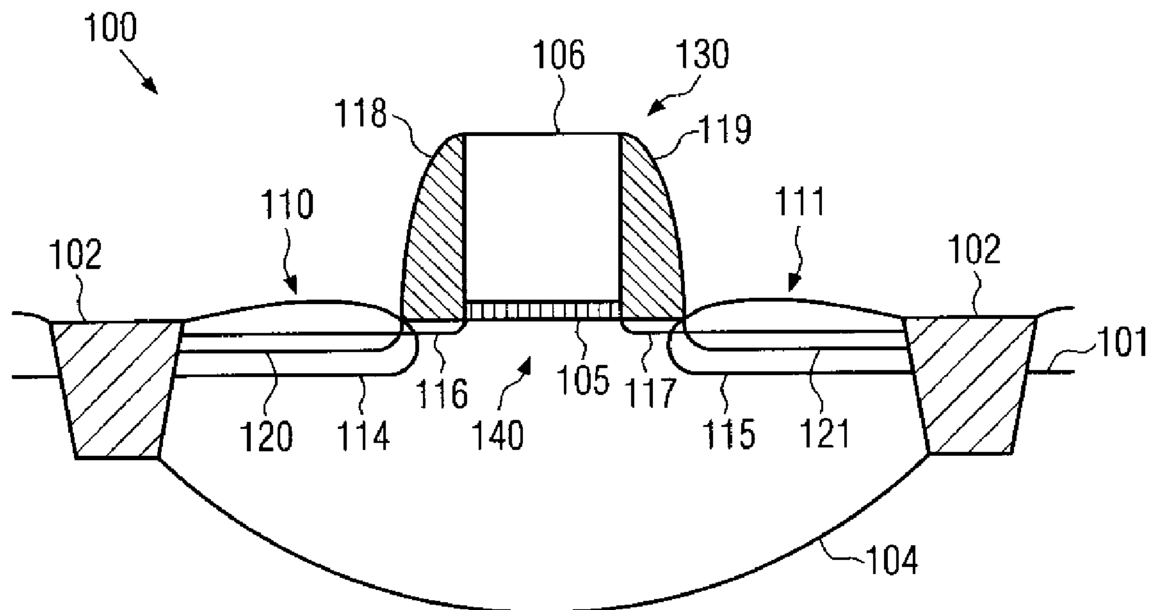



FIG. 1d
(prior art)

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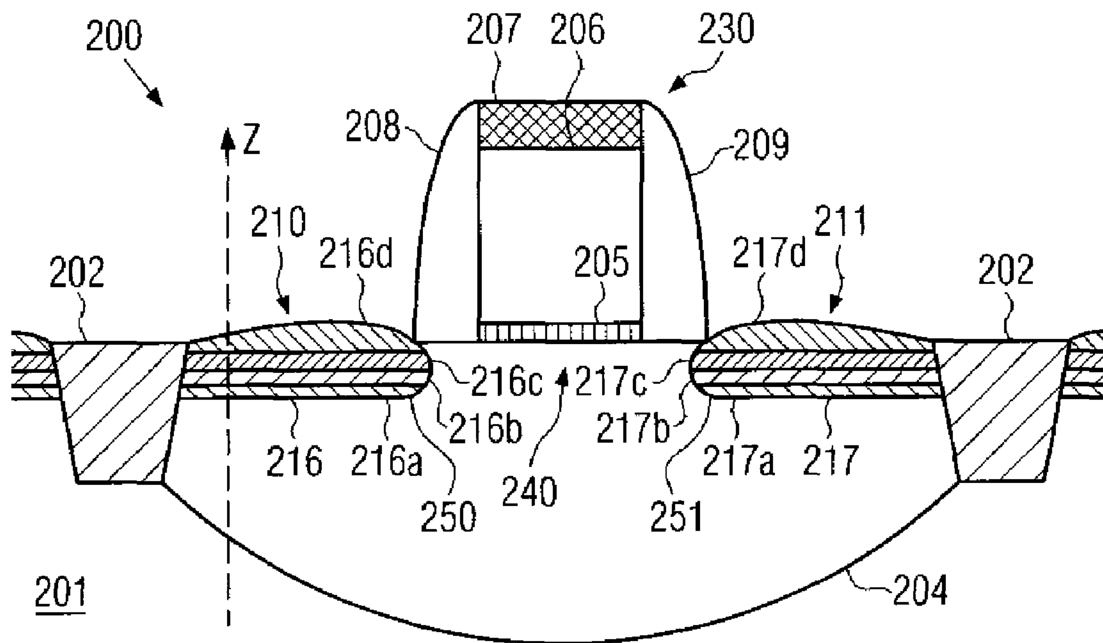



FIG. 2a

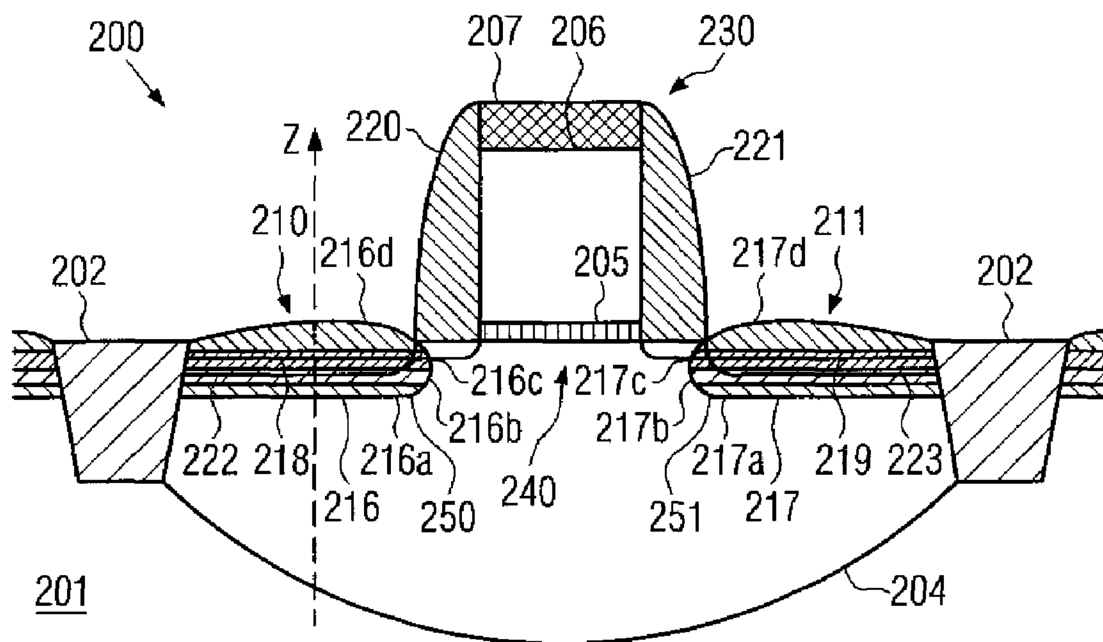



FIG. 2b

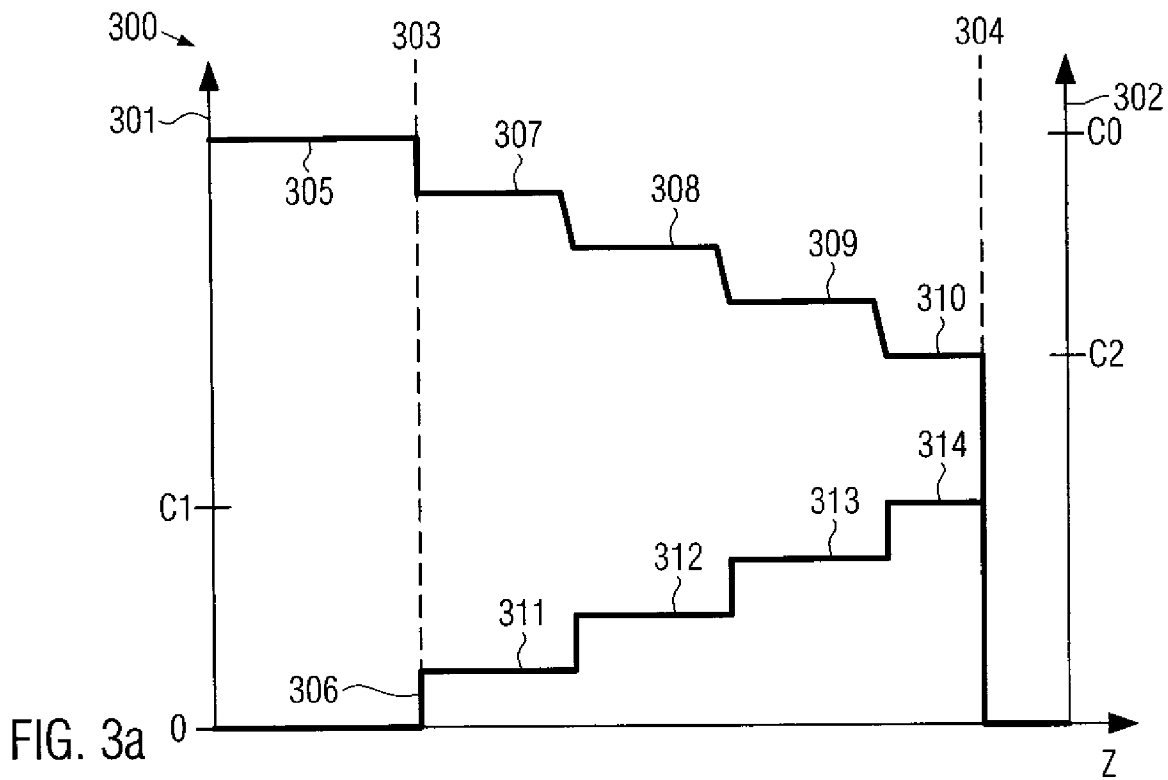


FIG. 3a

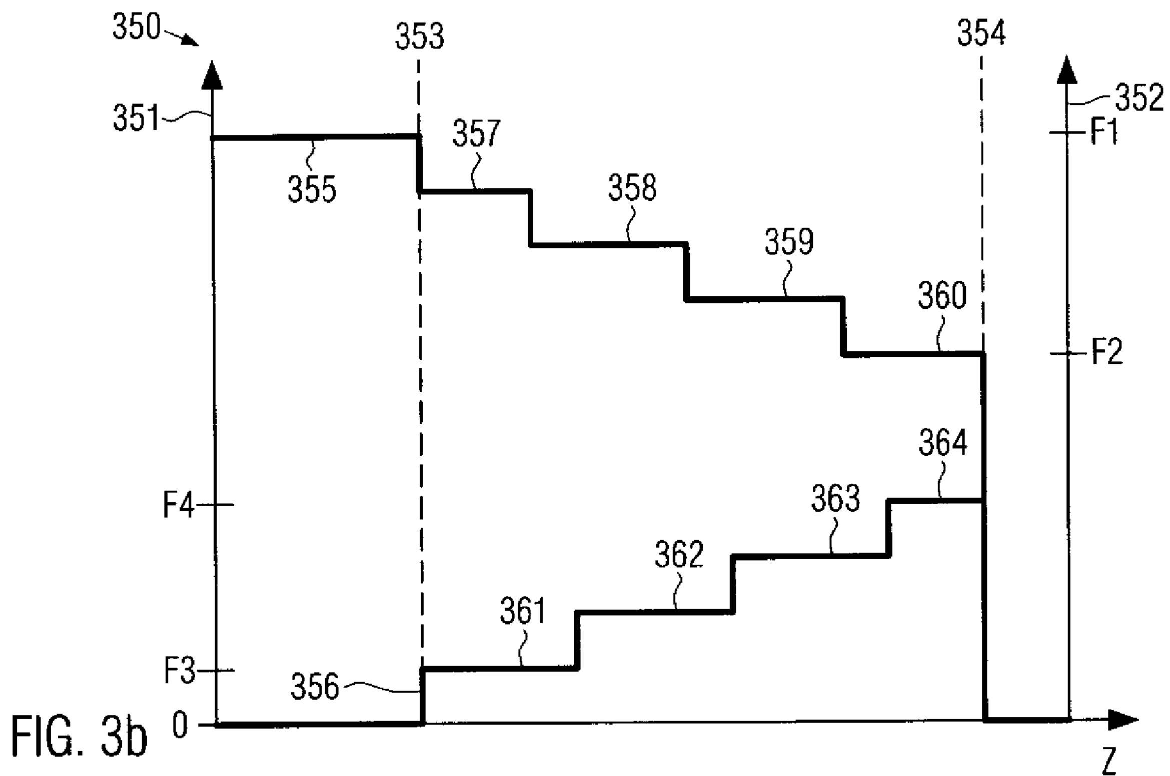


FIG. 3b

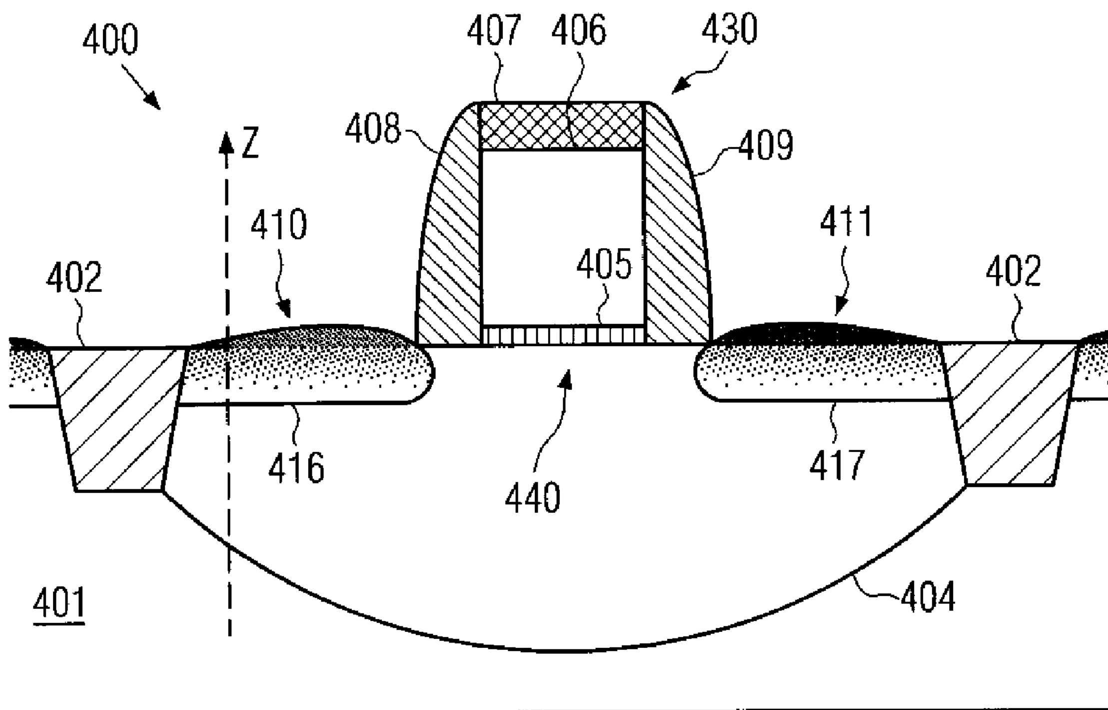



FIG. 4

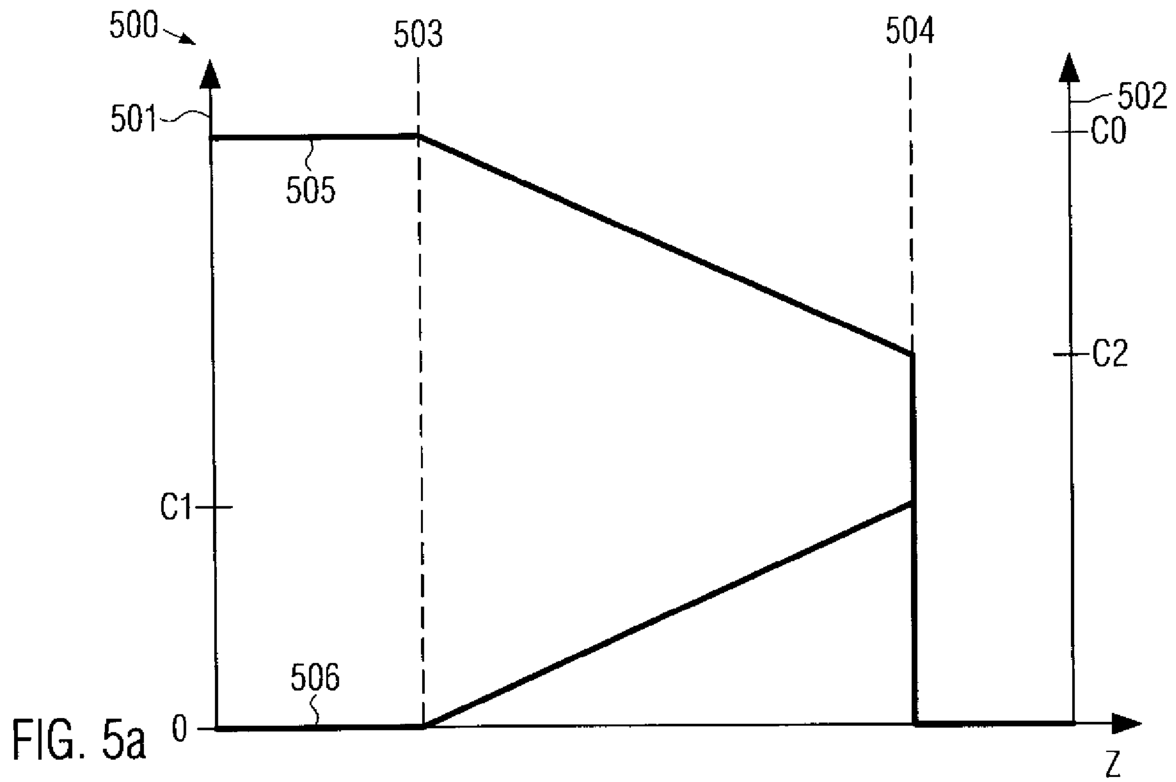


FIG. 5a

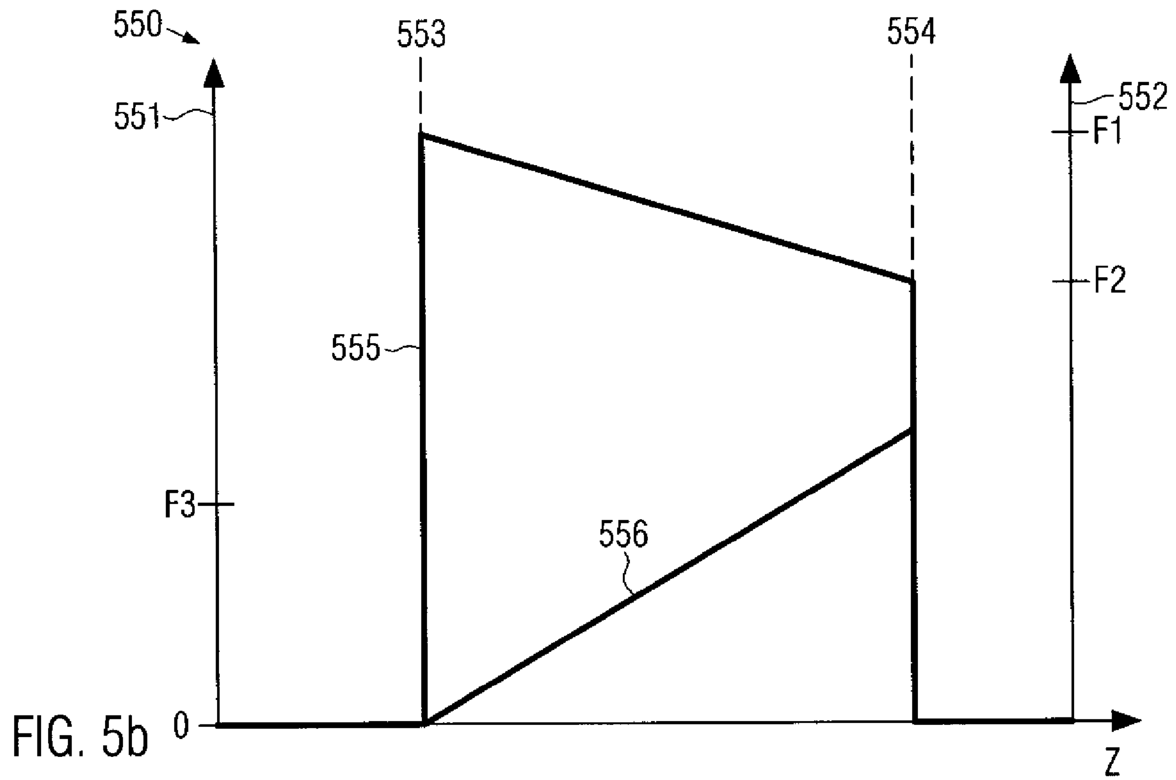


FIG. 5b

# FIELD EFFECT TRANSISTOR AND METHOD OF FORMING A FIELD EFFECT TRANSISTOR

## BACKGROUND OF THE INVENTION

1. Field of the Invention

The subject matter disclosed herein generally relates to the formation of integrated circuits, and, more particularly, to the formation of field effect transistors comprising at least one strain-creating element formed adjacent a gate electrode thereof.

2. Description of the Related Art

Integrated circuits comprise a large number of individual circuit elements, such as transistors, capacitors and resistors. These elements are connected internally to form complex circuits such as memory devices, logic devices and microprocessors. The performance of integrated circuits can be improved by increasing the number of functional elements in the circuit in order to increase their functionality and/or by increasing the speed of operation of the circuit elements. A reduction of feature sizes allows the formation of a greater number of circuit elements on the same area, hence allowing an extension of the functionality of the circuit, and also reduces signal propagation delays, thus making an increase of the speed of operation of circuit elements possible.

Field effect transistors are used as switching elements in integrated circuits. They provide a means to control a current flowing through a channel region located between a source region and a drain region. The source region and the drain region are highly doped. In N-type transistors, the source and drain regions are doped with an N-type dopant. Conversely, in P-type transistors, the source and drain regions are doped with a P-type dopant. The doping of the channel region is inverse to the doping of the source region and the drain region. The conductivity of the channel region is controlled by a gate voltage applied to a gate electrode formed above the channel region and separated therefrom by a thin insulating layer. Depending on the gate voltage, the channel region may be switched between a conductive "on" state and a substantially non-conductive "off" state.

When reducing the size of field effect transistors, it is important to maintain a high conductivity of the channel region in the "on" state. The conductivity of the channel region in the "on" state depends on the dopant concentration in the channel region, the mobility of the charge carriers, the extension of the channel region in the width direction of the transistor and the distance between the source region and the drain region, which is commonly denoted as "channel length." While a reduction of the width of the channel region leads to a decrease of the channel conductivity, a reduction of the channel length enhances the channel conductivity. An increase of the charge carrier mobility leads to an increase of the channel conductivity.

As feature sizes are reduced, the extension of the channel region in the width direction is also reduced. A reduction of the channel length entails a plurality of issues associated therewith. First, advanced techniques of photolithography and etching have to be provided in order to reliably and reproducibly create transistors having short channel lengths. Moreover, highly sophisticated dopant profiles, in the vertical direction as well as in the lateral direction, are required in the source region and in the drain region in order to provide a low sheet resistivity and a low contact resistivity in combination with a desired channel controllability.

In view of the problems associated with a further reduction of the channel length, it has been proposed to also enhance the



performance of field effect transistors by increasing the charge carrier mobility in the channel region. In principle, at least two approaches may be used to increase the charge carrier mobility.

First, the dopant concentration in the channel region may be reduced. Thus, the probability of scattering events of charge carriers in the channel region is reduced, which leads to an increase of the conductivity of the channel region. Reducing the dopant concentration in the channel region, however, significantly affects the threshold voltage of the transistor device. This makes the reduction of dopant concentration a less attractive approach.

Second, the lattice structure in the channel region may be modified by creating tensile or compressive strain. This leads to a modified mobility of electrons and holes, respectively. Depending on the magnitude of the strain, a compressive strain may significantly increase the mobility of holes in a silicon layer, and may also increase the electron mobility. The mobility of electrons may also be increased by providing a silicon layer having a tensile strain.

A method of forming a field effect transistor wherein the channel region is formed in strained silicon will be described in the following with reference to FIGS. **1***a*-**1***d*. FIG. **1***a* shows a schematic cross-sectional view of a semiconductor structure **100** in a first stage of a manufacturing process according to the state of the art. The semiconductor structure **100** comprises a substrate **101**. An active region **104** is provided in the substrate **101**. A trench isolation structure **102** separates the active region **104** from other elements of the semiconductor structure **100** which are not shown in FIG. **1***a*. A gate electrode **106**, which is separated from the substrate **101** by a gate insulation layer **105**, is formed over the substrate **101**. The gate electrode **106** is covered by a cap layer **107** and flanked by first sidewall spacers **108**, **109**. The active region **104**, the trench isolation structure **102**, the gate electrode **106**, the gate insulation layer **105**, as well as the first sidewall spacers **108**, **109** and the cap layer **107**, together form portions of a field effect transistor element **130**.

In the formation of the semiconductor structure **100**, the substrate **101** is provided and the trench isolation structure **102** is formed by means of methods of photolithography, deposition and/or oxidation techniques known to persons skilled in the art. Then, ions of a dopant material are implanted into the substrate **101** in order to form the active region **104**. The type of dopants corresponds to the doping of the channel region of the field effect transistor to be formed. Hence, in the formation of an N-type transistor, ions of a P-type dopant are implanted, whereas ions of an N-type dopant are implanted in the formation of a P-type transistor.

After the formation of the active region **104**, an oxidation process is performed to form the gate insulation layer **105**. Thereafter, the gate electrode **106** and the cap layer **107** are formed by deposition and photolithography processes known to persons skilled in the art. Subsequently, the first sidewall spacers **108**, **109** are formed by depositing a layer of a spacer material and performing an anisotropic etch process, wherein portions of the layer of spacer material over substantially horizontal portions of the semiconductor structure **100** are removed, whereas portions of the layer of spacer material provided on the sidewalls of the gate electrode **106** remain on the substrate **101** and form the first sidewall spacers **108**, **109**.

A schematic cross-sectional view of the semiconductor structure **100** in a later stage of the manufacturing process according to the state of the art is shown in FIG. **1***b*. An etch process is performed. The etch process can be an isotropic etch process adapted to selectively remove the material of the substrate **101**, leaving the material of the cap layer **107** and the

first sidewall spacers **108**, **109** substantially intact, for example, a known dry etch process. The cap layer **107** and the first sidewall spacers **108**, **109** protect the gate electrode **106**, the gate insulation layer **105** and a channel region **140** below the gate electrode **106** from being affected by an etchant used in the etch process.

Portions of the substrate **101** adjacent the gate electrode **106**, however, are etched away. Thus, a source side cavity **110** and a drain side cavity **111** are formed adjacent the gate electrode **106**. Due to the isotropy of the etch process, portions of the substrate **101** below the first sidewall spacers **108**, **109** and, optionally, the gate electrode **106** are removed. Therefore, the cavities **110**, **111** may extend below the sidewall spacers **108**, **109** and/or the gate electrode **106**, the bottom surface **150**, **151** of the cavities **110**, **111** having a somewhat rounded shape.

After the etch process, the cavities **110**, **111** may have a rough surface. If a strain-creating material were deposited over the substrate **101** in order to fill the cavities **110**, **111** as described below, unevenness on the bottom surface **150**, **151** of the cavities **110**, **111** would act as nucleation sites, leading to an undesirable polycrystalline growth of the strain-creating material. Therefore, a process is performed to reduce the roughness of the bottom surface of the cavities.

The roughness reducing process can be a high temperature prebake process wherein the semiconductor structure **100** is exposed to a temperature in a range from about 800-1000° C. for about 30 seconds to about 10 minutes. During the prebake process, the semiconductor structure **100** can be provided in an ambient comprising hydrogen gas which substantially does not react chemically with the materials of the semiconductor structure **100**. The high temperature prebake process leads to a diffusion of atoms on the surface of the cavities **110**, **111**. Due to the diffusion, a material transport may occur which leads to a reduction in the roughness of the surface of the cavities **110**, **111**.

FIG. **1***c* shows a schematic cross-sectional view of the semiconductor structure **100** in yet another stage of the manufacturing process. Strain-creating elements **114**, **115** are formed adjacent the gate electrode **106**. To this end, the cavities **110**, **111** are filled with a layer of a strain-creating material. In methods of forming a field effect transistor according to the state of the art, the strain-creating material may comprise silicon germanide. As persons skilled in the art know, silicon germanide is an alloy of silicon (Si) and germanium (Ge). Other materials may be employed as well.

Silicon germanide is a semiconductor material having a greater lattice constant than silicon. When silicon germanide is deposited in the cavities **110**, **111**, however, the silicon and germanium atoms in the strain-creating elements **114**, **115** tend to adapt to the lattice constant of the silicon in the substrate **101**. Therefore, the lattice constant of the silicon germanide in the strain-creating elements **114**, **115** is smaller than the lattice constant of a bulk silicon germanide crystal. Thus, the material of the strain-creating elements **114**, **115** is compressively strained.

The strain-creating elements **114**, **115** can be formed by means of selective epitaxial growth. As persons skilled in the art know, selective epitaxial growth is a variant of plasma enhanced chemical vapor deposition wherein parameters of the deposition process are adapted such that material is deposited only on the surface of the substrate **101** in the cavities **110**, **111**, whereas substantially no material deposition occurs on the surface of the first sidewall spacers **108**, **109** and the cap layer **107**.

Since the strain-creating elements **114**, **115** are compressively strained, they exhibit a force to portions of the substrate **101** in the vicinity of the gate electrode **106**, in particular to portions of the substrate **101** in the channel region **140**. Therefore, a compressive strain is created in the channel region **140**.

FIG. **1***d* shows a schematic cross-sectional view of the semiconductor structure **100** in yet another stage of the manufacturing process according to the state of the art. After the formation of the strain-creating elements **114**, **115**, the first sidewall spacers **108**, **109** are removed. Additionally, the cap layer **107** may be removed. Thereafter, an extended source region **116** and an extended drain region **117** are formed in portions of the substrate **101** and the strain-creating elements **114**, **115** by means of an ion implantation process known to persons skilled in the art. In the ion implantation process, ions of a dopant material are introduced into the substrate **101** and the strain-creating elements **114**, **115**. In case of the formation of an N-type field effect transistor, ions of an N-type dopant are introduced, wherein ions of a P-type dopant are provided in the formation of a P-type transistor.

Subsequently, second sidewall spacers **118**, **119** are formed adjacent the gate electrode **106**. Thereafter, a further ion implantation process is performed to form a source region **120** and a drain region **121** by introducing dopant material ions.

Finally, an annealing process may be performed to activate the dopant materials introduced in the formation of the extended source region **116**, the extended drain region **117**, the source region **120** and the drain region **121**.

One problem associated with the above method of forming a field effect transistor according to the state of the art is that a relaxation of strain may occur in the strain-creating elements **114**, **115**. Therefore, the strain in the strain-creating elements **114**, **115** and consequently the strain in the channel region **140** can be reduced. This may lead to a reduced enhancement of the mobility of holes and/or electrons in the channel region.

The present disclosure is directed to various methods that may avoid, or at least reduce, the effects of one or more of the problems identified above.

## SUMMARY OF THE INVENTION

The following presents a simplified summary of the invention in order to provide a basic understanding of some aspects of the invention. This summary is not an exhaustive overview of the invention. It is not intended to identify key or critical elements of the invention or to delineate the scope of the invention. Its sole purpose is to present some concepts in a simplified form as a prelude to the more detailed description that is discussed later.

According to an illustrative embodiment disclosed herein, a method of forming a field effect transistor comprises providing a semiconductor substrate, a gate electrode being formed above the semiconductor substrate. At least one cavity is formed in the substrate adjacent the gate electrode. A strain-creating element is formed in the at least one cavity. The strain-creating element comprises a compound material comprising a first chemical element and a second chemical element. A first concentration ratio between a concentration of the first chemical element in a first portion of the strain-creating element and a concentration of the second chemical element in the first portion of the strain-creating element is different from a second concentration ratio between a concentration of the first chemical element in a second portion of the strain-creating element and a concentration of the second chemical element in the second portion of the strain-creating element.

According to another illustrative embodiment disclosed herein, a method of forming a field effect transistor comprises providing a semiconductor substrate, a gate electrode being formed above the substrate. At least one cavity is formed in the substrate adjacent the gate electrode. A selective epitaxial growth process adapted to form a strain-creating element in the at least one cavity is performed. The strain-creating element comprises a compound material comprising a first chemical element and a second chemical element. The selective epitaxial growth process comprises supplying a first reactant comprising the first chemical element and a second reactant comprising the second chemical element. A ratio between a flow rate of the first reactant and a flow rate of the second reactant is changed at least once during the selective epitaxial growth process.

According to yet another illustrative embodiment disclosed herein, a field effect transistor comprises a substrate. A gate electrode is formed above the substrate. The substrate comprises at least one cavity located in the substrate adjacent the gate electrode. A strain-creating element is located in the at least one cavity. The strain-creating element comprises a compound material comprising a first chemical element and a second chemical element. A ratio between a concentration of the first chemical element and a concentration of the second chemical element increases in a vertical direction with increasing distance from a bottom surface of the cavity in the substrate.

## BRIEF DESCRIPTION OF THE DRAWINGS

The disclosure may be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements, and in which:

FIGS. **1***a*-**1***d* show schematic cross-sectional views of a semiconductor structure in stages of a manufacturing process according to the state of the art;

FIGS. **2***a*-**2***b* show schematic cross-sectional views of a semiconductor structure in stages of a manufacturing process according to an embodiment disclosed herein;

FIGS. **3***a*-**3***b* show schematic diagrams illustrating concentrations of chemical elements in a semiconductor structure formed by the manufacturing process illustrated in FIGS. **2***a*-**2***b* and reactant flows in the manufacturing process;

FIG. **4** shows a schematic cross-sectional view of a semiconductor structure in a stage of a manufacturing process according to another embodiment disclosed herein; and

FIGS. **5***a*-**5***b* show schematic diagrams illustrating concentrations of chemical elements in a semiconductor structure formed by the manufacturing process illustrated in FIG. **4** and reactant flows in the manufacturing process.

While the subject matter disclosed herein is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

## DETAILED DESCRIPTION OF THE INVENTION

Various illustrative embodiments of the invention are described below. In the interest of clarity, not all features of an actual implementation are described in this specification. It will of course be appreciated that in the development of any such actual embodiment, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking for those of ordinary skill in the art having the benefit of this disclosure.

The present subject matter will now be described with reference to the attached figures. Various structures, systems and devices are schematically depicted in the drawings for purposes of explanation only and so as to not obscure the present disclosure with details that are well known to those skilled in the art. Nevertheless, the attached drawings are included to describe and explain illustrative examples of the present disclosure. The words and phrases used herein should be understood and interpreted to have a meaning consistent with the understanding of those words and phrases by those skilled in the relevant art. No special definition of a term or phrase, i.e., a definition that is different from the ordinary and customary meaning as understood by those skilled in the art, is intended to be implied by consistent usage of the term or phrase herein. To the extent that a term or phrase is intended to have a special meaning, i.e., a meaning other than that understood by skilled artisans, such a special definition will be expressly set forth in the specification in a definitional manner that directly and unequivocally provides the special definition for the term or phrase.

The subject matter disclosed herein is generally based on the realization that the undesirable relaxation of strain observed in the strain-creating elements **114**, **115** formed in the method of manufacturing a field effect transistor according to the state of the art described above with reference to FIGS. **1***a*-**1***d* may be caused by a formation of crystal defects in the strain-creating elements **114**, **115**. Such crystal defects may be particularly formed at the interface between the semiconductor substrate **101** and the strain-creating elements **114**, **115** where large gradients of the strain may occur. The presence of crystal defects allows the crystal lattice of the strain-creating material in the strain-creating elements **114**, **115** to relax such that it more closely resembles the crystal lattice of an unstrained bulk crystal of the strain-creating material. Therefore, the strain in the strain-creating elements **114**, **115** and, thus, the strain in the channel region **140** of the transistor element **130** may be reduced.

In the present disclosure, strain-creating elements adjacent the gate electrode of a field effect transistor may be formed with a chemical composition which varies between different portions of the strain-creating elements. In particular, a composition of portions of the strain-creating elements in the vicinity of an interface between the strain-creating elements and an underlying semiconductor substrate may more closely resemble the composition of the semiconductor substrate than a composition of portions of the strain-creating elements provided at a greater distance from the semiconductor substrate. Thus, the strain in the strain-creating elements may gradually increase from a relatively low strain in the vicinity of the substrate to a moderately high strain in portions of the strain-creating elements that are a greater distance from the substrate. Hence, the presence of high gradients of the strain can be avoided. This may allow a reduction of the likelihood of the occurrence of crystal defects. Thus, a relaxation of strain caused by crystal defects may be advantageously reduced.

FIG. **2***a* shows a schematic cross-sectional view of a semiconductor structure **200** in a first stage of a method of forming

a field effect transistor. The semiconductor structure **200** comprises a substrate **201**. In the substrate **201**, a trench isolation structure **202** is formed. A gate insulation layer **205** electrically insulates a gate electrode **206** from an active region **204** formed in the substrate **201**. The gate electrode **206** is covered by a cap layer **207** and flanked by first sidewall spacers **208**, **209**. The trench isolation structure **202**, the active region **204**, the gate insulation layer **205**, the gate electrode **206**, the cap layer **207** and the first sidewall spacers **208**, **209** form a field effect transistor element **230** and may be formed by means of methods of photolithography, etching, deposition and oxidation well known to persons skilled in the art.

The substrate **201** and the gate electrode **206** may be comprised of silicon. For example, the substrate **201** may comprise crystalline silicon and the gate electrode **206** may comprise polysilicon. In some embodiments, the trench isolation structure **202**, the cap layer **207** and the first sidewall spacers **208**, **209** may be comprised of silicon nitride. In other embodiments, these features may comprise silicon dioxide. In still further embodiments, the trench isolation structure **202**, the cap layer **207** and the first sidewall spaces **208**, **209** can be formed from different materials. For example, the trench isolation structure can comprise silicon dioxide and the first sidewall spacers **208**, **209**, as well as the cap layer **207**, can comprise silicon nitride.

A source side cavity **210** and a drain side cavity **211** are formed in the substrate **201** adjacent the gate electrode **206**. Similar to the formation of the cavities **110**, **111** in the method of manufacturing a field effect transistor according to the state of the art described above with reference to FIGS. **1***a*-**1***d*, the cavities **210**, **211** may be formed by means of an etch process which may be isotropic, for example a dry etch process.

In dry etching, which is also known as plasma etching, reactive ion etching or ion enhanced etching, a radio frequency glow discharge produces a chemically reactive species such as atoms, radicals, and ions from a relatively inert molecular gas. The etching gas is selected such that a generated species reacts chemically with the material to be etched, creating a volatile reaction product. The energy of ions impinging on the substrate may be controlled by varying the frequency applied in creating the glow discharge and/or applying a DC bias to the substrate. In general, the greater the energy of the ions, the greater the anisotropy of the etch process.

In the etch process, the semiconductor structure **200** is exposed to an etchant adapted to selectively remove the material of the substrate **201**, leaving the gate electrode **206** covered by the first sidewall spacers **208**, **209** and the cap layer **207** substantially intact. In embodiments disclosed herein wherein the substrate **201** comprises silicon and the cap layer **207** and the first sidewall spacers **208**, **209** comprise silicon nitride and/or silicon dioxide, a selective removal of the material of the substrate **201** may be achieved by using a dry etch process performed by means of an etch gas comprising carbon tetrafluoride ($CF_4$) and/or oxygen ($O_2$). The isotropy of the etch process may be obtained by applying a low DC bias or no DC bias at all.

The present invention is not restricted to embodiments wherein a dry etch process is performed. In other embodiments, the cavities **210**, **211** can be formed by means of a wet etch process.

Due to the isotropic nature of the etch process, portions of the cavities **210**, **211** may extend below the first sidewall spacers **208**, **209** or even below the gate electrode **206**. After the etch process, the surface of the substrate **201** in the cavities **210**, **211** may be rough. Similar to the method of forming a field effect transistor according to the state of the art described above with reference to FIGS. **1***a*-**1***d*, the roughness of the surface of the substrate **201** in the cavities **210**, **211** can be reduced, for example by performing a prebake process wherein the semiconductor structure **200** is exposed to an elevated temperature in a range from about 800-1000° C. for about 30 seconds to about 10 minutes in a hydrogen ambient. In other embodiments, the reduction of the roughness of the surface of the substrate **201** in the cavities **210**, **211** can be performed by means of other methods or may even be omitted.

Strain-creating elements **216**, **217** are formed adjacent the gate electrode **206**. The strain-creating elements **216**, **217** comprise a compound material comprising a first chemical element and a second chemical element. In embodiments disclosed herein wherein the substrate **201** comprises silicon, the second chemical element may be silicon. In some embodiments, the first chemical element may comprise germanium. In other embodiments, the first chemical element may comprise carbon. In further embodiments, other materials may be employed as well.

Silicon germanide has a greater lattice constant than that of the silicon in the substrate **201**. Therefore, in embodiments wherein the strain-creating elements comprise silicon germanide, the strain-creating elements **216**, **217** can be compressively strained, since the silicon germanide adapts to the silicon in the substrate **201**. The value of the strain in the strain-creating elements **216**, **217** depends on the ratio between the concentration of germanium and the concentration of silicon. Portions of the strain-creating elements **216**, **217** having a moderately high ratio between the concentration of germanium and the concentration of silicon can be subject to a greater compressive strain than portions of the strain-creating elements **216**, **217** having a relatively low ratio between the concentration of germanium and the concentration of silicon.

Silicon carbide has a lattice constant which is smaller than the lattice constant of silicon. The silicon carbide in the strain-creating elements **216**, **217**, however, may adapt to the crystal lattice of the silicon in the substrate **201** such that the strain-creating elements **216**, **217** are subject to tensile strain. The tensile strain may influence the strain state of portions of the substrate **201** in the vicinity of the strain-creating elements. Thus, a tensile strain may be created in a channel region **240** below the gate electrode **206**.

The strength of the strain in the strain-creating elements **216**, **217** when comprising silicon carbide may be influenced by a ratio between the concentration of carbon and the concentration of silicon. Portions of the strain-creating elements **216**, **217** having a moderately high ratio between the concentration of carbon and the concentration of silicon may be subject to a greater tensile strain than portions of the strain-creating elements **216**, **217** having a moderately low ratio between the concentration of carbon and the concentration of silicon.

In general, the strain state of a portion of one of the strain-creating elements **216**, **217** can be influenced by a ratio between the concentration of the first chemical element and the concentration of the second chemical element in the portion of the strain-creating elements **216**, **217**.

The strain in the strain-creating elements **216**, **217** may act on portions of the substrate **201** in the vicinity of the strain-creating elements **216**, **217**, in particular on portions of the substrate **201** below the gate electrode **206** wherein a channel region **240** of the field effect transistor element **230** is formed. Thus, the mobility of holes and/or electrons in the channel region **240** can be increased.

Each of the strain-creating elements **216**, **217** comprises a first portion and a second portion, wherein a first concentration ratio between a concentration of the first chemical element in the first portion and a concentration of the second chemical element in the first portion is different from a second concentration ratio between a concentration of the first chemical element in the second portion and a concentration of the second chemical element in the second portion. In some embodiments, the first concentration ratio can be smaller than the second concentration ratio.

Each of the first portion and the second portion of the strain-creating element **216** can be provided in the form of one of a plurality of sub-layers **216***a*, **216***b*, **216***c*, **216***d* of the strain-creating element **216**, wherein the second portion is located above the first portion. For example, the first portion of the strain-creating element **216** can be provided in the form of the sub-layer **216***a* being located at the interface **250** between the semiconductor substrate **201** and the strain-creating element and the second portion can be provided in the form of one of the sub-layers **216***b*, **216***c*, **216***d*, for example in the form of the sub-layer **216***d* located at the surface of the strain-creating element **217**. In other embodiments, the first portion and the second portion can be provided in other arrangements of the sub-layers **216***a*, **216***b*, **216***c*, **216***d*, as long as the sub-layer corresponding to the second portion is located above the sub-layer corresponding to the first portion.

Similarly, the first portion and the second portion of the strain-creating element **217** can each be provided in the form of one of a plurality of sub-layers **217***a*, **217***b*, **217***c*, **217***d* of the second strain-creating element **217**, wherein the sub-layer corresponding to the second portion is located above the sub-layer corresponding to the first portion. Reference numeral **251** denotes an interface between the semiconductor substrate **201** and the strain-creating element **217**.

FIG. **3***a* shows a schematic diagram **300** of the concentrations of the first chemical element and the second chemical element along a line Z vertically running through the semiconductor substrate **201** and the first strain-creating element **216**, wherein the vertical direction is a direction substantially perpendicular to a surface of the substrate **201** and/or the interface between the substrate **201** and the strain-creating element **216**. A first coordinate axis **301** denotes values of the concentration of the first chemical element along the line Z and a second coordinate axis **302** denotes values of the concentration of the second chemical element along the line Z. The concentration of the first chemical element is represented by a curve **306** and the concentration of the second chemical element is represented by a curve **305**. A first vertical line **303** denotes the location of the interface between the substrate **201** and the first strain-creating element **216** and a second vertical line **304** denotes the location of the surface of the first strain-creating element **216**.

In the substrate **201**, the concentration of the second chemical element assumes a relatively high value C**0** whereas the concentration of the first chemical element can be approximately zero. The first sub-layer **216***a* comprises the first chemical element in a concentration greater than zero. Correspondingly, the concentration of the second chemical element in the first sub-layer **216***a* is smaller than the concentration of the second chemical element in the substrate **201**. The other sub-layers **216***b*, **216***c*, **216***d* may comprise the first chemical element and the second chemical element in concentrations which differ from those in the first sub-layer **216***a*. In particular, the concentration of the first chemical element in the second sub-layer **216***b* may be higher than the concentration of the first chemical element in the first sub-layer **216***a*. The third sub-layer **216***c* and the fourth sub-layer **216***d* may comprise the first chemical element in even higher concentrations. Correspondingly, the concentration of the second chemical element in the sub-layers **216***b*, **216***c*, **216***d* may become smaller.



The concentration of the first chemical element and the second chemical element in the individual sub-layers **216***a*, **216***b*, **216***c*, **216***d* may be approximately constant throughout the respective sub-layers. Therefore, the curve **305** corresponding to the concentration of the second chemical element may decrease in a series of steps **307**, **308**, **309**, **310** which correspond to the sub-layers **216***a*, **216***b*, **216***c*, **216***d* to a concentration C**2** of the second chemical element at the surface of the strain-creating element **216**. Correspondingly, the curve **306** which corresponds to the concentration of the first chemical element may increase in a series of steps **311**, **312**, **313**, **314** to a concentration C**1** of the first chemical element at the surface of the first strain-creating element **216**.

The ratio between the concentration of the first chemical element and the concentration of the second chemical element in the second portion of the strain-creating element can be greater than about 1%. In some embodiments, the ratio can be even greater than about 10%. In particular, a ratio C**1**/C**2** between the concentrations C**1** and C**2** can be greater than 1% or greater than 10%, respectively.

The composition of the sub-layers **217***a*, **217***b*, **217***c*, **217***d* of the second strain-creating element **217** may be substantially identical to that of the sub-layers **216***a*, **216***b*, **216***c*, **216***d* of the first strain-creating element **216**.

Since, as detailed above, the strain state of the first and second portions of the strain-creating elements **216**, **217** may depend on the ratio between the concentration of the first chemical element and the concentration of the second chemical element in the respective portion, high gradients of the strain, which can lead to an undesirable formation of dislocations, may be advantageously avoided by adapting the concentrations of the first chemical element and the second chemical element in the first and second portions of the strain-creating elements **216**, **217**.

The first strain-creating element **216** and the second strain-creating element **217** may be formed by means of a selective epitaxial growth process. Selective epitaxial growth is a variant of plasma enhanced chemical vapor deposition well known to persons skilled in the art, wherein process parameters such as temperature, pressure and composition of the reactant gas are adapted such that a layer of material is deposited only on the exposed portions of the substrate **201**, in particular in the cavities **210**, **211**, whereas there is substantially no deposition on the trench isolation structure **202**, the cap layer **207** and the first sidewall spacers **208**, **209**.

The concentration of the first chemical element and the second chemical element in the strain-creating elements **216**, **217** can be controlled by varying flow rates of a first reactant comprising the first chemical element and a second reactant comprising the second chemical element. In general, a greater ratio between the flow rate of the first reactant and the flow rate of the second reactant entails a greater concentration of the first chemical element in the deposited material.

In embodiments wherein the substrate **201** comprises silicon and the cap layer **207** and the first sidewall spacers **208**, **209** comprise silicon dioxide and/or silicon nitride, the first reactant may comprise germane ($GeH_4$) and the second reactant may comprise dichlorosilane ($SiH_2Cl_2$). These reactants can be supplied in gaseous form to form strain-creating elements **216**, **217** comprising silicon germanide. Additionally, hydrogen may be provided as a carrier gas and hydrochloric acid (HCl) may be supplied in order to increase the selectivity of the epitaxial growth of silicon germanide.

In other embodiments wherein the strain-creating elements **216**, **217** comprise silicon carbide, the first reactant may comprise ethene ($C_2H_4$) and the second reactant may comprise silane ($SiH_4$). Additionally, hydrochloric acid (HCl) may be provided in order to increase the selectivity of the growth process.

A ratio between the flow rate of the first reactant and the flow rate of the second reactant can be changed during the selective epitaxial growth process.

FIG. **3***b* shows a schematic diagram **300** of dependence of the flow rates of the first reactant and the second reactant on time t. A first coordinate axis **351** represents values of the flow of the first reactant which is indicated by a first curve **356**. A second coordinate axis **352** represents values of the flow of the second reactant which is indicated by a second curve **355**. A first vertical line **353** indicates the point in time where the selective epitaxial growth process is started and a second vertical line **354** indicates the point in time at which the selective epitaxial growth process is stopped after the completion of the formation of the strain-creating elements **216**, **217**.

At the beginning of the selective epitaxial growth process, a moderately large flow of the second reactant and a relatively small flow of the first reactant are supplied to form the first sub-layers **216***a*, **217***a* of the strain-creating elements **216**, **217**. After the formation of the first sub-layers **216***a*, **217***a*, at least one of the flow rate of the first reactant and the flow rate of the second reactant can be varied in order to change the ratio between the flow rate of the first reactant and the flow rate of the second reactant. Thereafter, the second sub-layers **216***b*, **217***b* of the strain-creating elements **216**, **217** can be formed. Subsequently, the ratio between the flow rate of the first reactant and the flow rate of the second reactant can be changed to form the third sub-layers **216***c*, **217***c*. After the formation of the third sub-layers **216***c*, **217***c*, the ratio between the flow rates can be changed once again to form the fourth sub-layers **216***d*, **217***d*.

The change of the flow rate of the first reactant is indicated in FIG. **3***b* by steps **361**, **362**, **363**, **364** of the curve **356**. Each of these steps corresponds to the formation of a respective pair of the sub-layers **216***a*, **217***a*, **216***b*, **217***b*, **216***c*, **217***c*, **216***d*, **217***d* of the strain-creating elements **216**, **217**. Similarly, the curve **355** comprises steps **357**, **358**, **359**, **360** corresponding to the change of the flow rate of the second reactant. In the course of the selective epitaxial growth process, the flow rate of the first reactant can be increased from a first flow rate F**3** to a second flow rate F**4**, while the flow rate of the second reactant is reduced from a first flow rate F**1** to a second flow rate F**2**.

FIG. **2***b* shows a schematic cross-sectional view of the semiconductor structure **200** in yet another stage of the manufacturing process. After the formation of the strain-creating elements **216**, **217**, the first sidewall spacers **208**, **209** and, optionally, the cap layer **207** can be removed. This can be done by means of a known etch process adapted to selectively remove the material of the first sidewall spacers **208**, **209** and/or the cap layer **207**, leaving the materials of the gate electrode **206**, the strain-creating elements **216**, **217** and the trench isolation structure **202** substantially intact.

Then, a first ion implantation process wherein ions of a dopant material are introduced into portions of the substrate **201** and/or the strain-creating elements **216**, **217** is performed to form an extended source region **218** and an extended drain region **219**.

Subsequently, second sidewall spacers **220**, **221** can be formed adjacent the gate electrode **206** by means of known methods comprising deposition of a layer of spacer material and an anisotropic etch process, and a source region **222** and a drain region **223** may be formed adjacent the second sidewall spacers **220**, **221** by means of a second ion implantation process. Finally, an annealing process can be performed in order to activate the dopants introduced into the extended source region **218**, the extended drain region **219**, the source region **222** and the drain region **223**.

The present invention is not restricted to embodiments wherein the first sidewall spacers **208**, **209** are removed after the formation of the strain-creating elements **216**, **217**. In other embodiments, an extended source region similar to the extended source region **218** and an extended drain region similar to the extended drain region **219** can be formed after the formation of the gate electrode **206** and before the formation of the first sidewall spacers **208**, **209**. During the processes performed in the formation of the cavities **210**, **211** and the strain-creating elements **216**, **217**, the first sidewall spacers **208**, **209** protect portions of the extended source region and the extended drain region below the first sidewall spacers **208**, **209**. Hence, these portions remain in the semiconductor structure **200**.

In such embodiments, the material deposited in the formation of the strain-creating elements **216**, **217** can be doped while the strain-creating elements are formed. To this end, a chemical compound comprising the dopant material can be added to the gas supplied in the selective epitaxial growth process. In the selective epitaxial growth process, the dopant material is incorporated into the material of the strain-creating elements **216**, **217** and doped strain-creating elements **216**, **217** are formed. The doped strain-creating elements, together with the portions of the extended source region and the extended drain region under the first sidewall spacers **220**, **221**, form a source and a drain.

In other embodiments wherein an extended source region and an extended drain region are formed prior to the formation of the strain-creating elements **216**, **217**, source and drain regions similar to the source region **222** and the drain region **223** can be formed by performing an ion implantation in order to introduce ions of a dopant material into the strain-creating elements **216**, **217**. The first sidewall spacers **208**, **209** may remain on the surface of the substrate **201** during this ion implantation. Thus, the source region and the drain region are spaced apart from the gate electrode **206**.

In a field effect transistor as disclosed herein, the first portions and the second portions of the strain-creating elements **216**, **217** need not be provided in the form of sub-layers of the strain-creating elements **216**, **217** wherein the concentrations of the first chemical element and the second chemical element are substantially constant in the interior of each of the sub-layers **216***a*-**216***d*, **217***a*-**217***d* as shown in FIG. **3***a*. In other embodiments, a smooth transition wherein the concentrations of the first chemical element and the second chemical element vary continuously may be provided between at least two of the sub-layers **216***a*-**216***d*, **217***a*-**217***d*. In particular, a continuous transition may be provided at each interface between adjacent ones of the sub-layers **216***a*-**216***d*, **217***a*-**217***d*. Advantageously, such embodiments may allow a further reduction of strain gradients in the strain-creating elements **216**, **217** and/or in the vicinity thereof.

In still further embodiments, a ratio between the concentration of the first chemical element and the concentration of the second chemical element in a strain-creating element may increase continuously in the vertical direction with increasing distance from a substrate.

In such embodiments, which will be described in the following with reference to FIGS. **4**, **5***a* and **5***b*, a first portion of a strain-creating element and a second portion of a strain-

creating element can be provided in the form of arbitrary sections of the strain-creating element whose centers of gravity are provided at a different distance from the substrate. Concentrations of the first chemical element and the second chemical element in the first and the second portion of the strain-creating element may be determined in the form of averaged values of local concentrations of the first and the second chemical element, wherein the averaging is performed as a spatial average over the respective portion of the strain-creating element.

FIG. **4** shows a schematic cross-sectional view of a semiconductor structure **400** in a stage of a manufacturing process according to the present disclosure. The semiconductor structure **400** comprises a substrate **401** and a field effect transistor element **430** formed in and on the substrate **401**. The field effect transistor element **430** comprises an active region **404** and a trench isolation structure **402** which insulates the active region **404** electrically from other circuit elements (not shown) in the semiconductor structure **400**. A gate electrode **406** which is separated from the active region **404** by a gate insulation layer **405** is formed over the active region **404**. The gate electrode **406** is flanked by first sidewall spacers **408**, **409** and may be covered by a cap layer **407**. Adjacent the gate electrode **406**, a source side cavity **410** and a drain side cavity **411** are formed.

The formation of these features may be performed by means of methods similar to those employed in the formation of the semiconductor structure **200** described above with reference to FIGS. **2***a*, **2***b*, **3***a* and **3***b*.

A first strain-creating element **416** is formed in the source side cavity **410** and a second strain-creating element **417** is formed in the drain side cavity **411**. Similar to the embodiments described above with reference to FIGS. **2***a*, **2***b*, **3***a* and **3***b*, the strain-creating elements **416**, **417** comprise a compound material comprising a first chemical element and a second chemical element.

A ratio between the concentration of the first chemical element and the concentration of the second chemical element increases in a vertical direction perpendicular to a surface of the substrate **401** and/or a surface of the strain-creating elements **416**, **417**, as indicated schematically by the shading of the strain-creating elements **416**, **417**. In FIG. **4**, the vertical direction is indicated by a dashed line Z. Thus, in portions of the strain-creating elements **416**, **417** in the vicinity of interfaces between the substrate **401** and the strain-creating elements **416**, **417**, the ratio between the concentration of the first chemical element and the concentration of the second chemical element assumes lower values than in portions of the strain-creating elements **416**, **417** in the vicinity of the surfaces of the strain-creating elements **416**, **417**.

The ratio between the concentration of the first chemical element and the concentration of the second chemical element may increase substantially continuously in the vertical direction Z with increasing distance from the substrate **401**. FIG. **5***a* shows a schematic drawing **500** of the concentrations of the first and the second chemical element in the semiconductor structure **400** along the vertical line Z (FIG. **4**). A first vertical coordinate axis **501** represent values of the concentration of the first chemical element and a second vertical coordinate axis **502** represents values of the concentration of the second chemical element. A first dashed vertical line **503** indicates a location of an interface between the substrate **401** and the first strain-creating element **416**. A second dashed vertical line **504** indicates a location of the surface of the first strain-creating element **416**. A first curve **506** shows the concentration of the first chemical element and a second curve **505** shows a concentration of the second chemical element.

Inside the substrate **401**, which may, apart from dopants introduced in the formation of the active region **404**, substantially comprise the second chemical element (which may, for example, be silicon), the concentration of the second chemical element may assume a relatively large value C**0**. The concentration of the first chemical element (which may, for example, comprise germanium or carbon) in the substrate **401** can be approximately zero. In the strain-creating element **416**, the concentration of the first chemical element may increase linearly to a value C**1** at the surface of the strain-creating element **416**. Correspondingly, the concentration of the second chemical element may drop to a concentration C**2** at the surface of the first strain-creating element **416**.

The increase of the concentration of the first chemical element with increasing distance from the substrate **401** need not be linear. In other embodiments, the concentration of the first chemical element may increase in a non-linear fashion. For example, there may be a relatively large increase of the concentration of the first chemical element in the vicinity of the interface between the substrate **401** and the first strain-creating element **416**, followed by a slower increase of the concentration of the first chemical element in the vicinity of the surface of the first strain-creating element **416**.

The ratio between the concentration of the first chemical element and the concentration of the second chemical element may be greater than about 1% in at least one portion of the strain-creating elements **416**, **417**, for example in the vicinity of the surface of the strain-creating elements **416** **417**. In some embodiments, the strain-creating elements **416**, **417** may even comprise portions wherein the ratio between the concentration of the first chemical element and the concentration of the second chemical element is greater than about 10%.

The concentrations of the first chemical element and the concentration of the second chemical element in the second strain-creating element **417** may be substantially identical to those in the first strain-creating element **416**.

Similar to the embodiments described above with reference to FIGS. **2***a*, **2***b*, **3***a* and **3***b*, the strain-creating elements **416**, **417** can be formed by means of a selective epitaxial growth process wherein a first reactant comprising the first chemical element and a second reactant comprising a second chemical element are supplied, optionally, in addition to further chemical compounds provided in order to increase the selectivity of the growth process and/or carrier gases. A ratio between a flow rate of the first reactant and a flow rate of the second reactant can be varied in order to deposit the material of the strain-creating elements **416**, **417** with a varying ratio between the concentration of the first chemical element and the concentration of the second chemical element.

FIG. **5***b* shows a schematic diagram **550** of the dependence of the flow rates of the first and the second chemical element on time t. A first coordinate axis **551** represents values of the flow rate of the first chemical element. A second coordinate axis **552** represents values of the flow rate of the second chemical element. A first vertical dashed line **553** indicates the point in time where the selective epitaxial growth process is started and a second vertical dashed line **554** indicates the point in time where the selective epitaxial growth process is stopped after the completion of the strain-creating elements **416**, **417**. A first curve **556** shows the flow rate of the first chemical element. The flow rate of the second chemical element is shown by a second curve **555**.

Before the start of the selective epitaxial growth process, the flow rates of both chemical elements may be approximately zero. At the start of the selective epitaxial growth process, a relatively large flow rate F**1** of the second reactant

may be provided while the flow rate of the first chemical element may be substantially zero. Thus, at the beginning of the selective epitaxial growth process, the second chemical element may be deposited in substantially pure form.

In embodiments wherein the semiconductor substrate **401** comprises the second chemical element, a deposition of the second chemical element in substantially pure form at the beginning of the selective epitaxial growth process may help reduce the roughness of the surface of the substrate **401** in the cavities **410**, **411**. In particular, reduction in the roughness may occur if the deposition process has a relatively low degree of anisotropy or is substantially isotropic. The roughness reduction effect of the deposition of the second chemical element in substantially pure form may be particularly advantageously used in embodiments wherein no roughness reduction process is performed after the formation of the cavities **410**, **411**.

During the selective epitaxial growth process, the flow rate of the first reactant may be substantially continuously increased until a relatively large flow rate F**3** is obtained at the end of the selective epitaxial growth process. The flow rate of the second reactant may be reduced concurrently with the increase of the flow rate of the first reactant until a flow rate F**2** smaller than the flow rate F**1** is obtained at the end of the selective epitaxial growth process. Thus, the ratio between the flow rate of the first reactant and the flow rate of the second reactant increases continuously during the selective epitaxial growth process.

Therefore, in the course of the selective epitaxial growth process, material may be deposited, wherein the ratio between the concentration of the first chemical element and the concentration of the second chemical element increases in material deposited at later points of time. Thus, in the strain-creating element **416**, **417**, the ratio between the concentration of the first chemical element and the concentration of the second chemical element may increase with increasing distance from the semiconductor substrate **401**.

After the formation of the strain-creating elements **416**, **417**, the first sidewall spacers **408**, **409** and, optionally, the cap layer **407** may be removed, and extended source and drain regions can be formed in the substrate **401** and the strain-creating elements **416**, **417** adjacent the gate electrode **406**. Then, second sidewall spacers (not shown) may be formed at the flanks of the gate electrode **406** and source and drain regions can be formed in the strain-creating elements **416**, **417**. The formation of the second sidewall spacers, the extended source and drain regions and the source and drain regions may be performed similar to the formation of the extended source and drain regions **218**, **219**, the second sidewall spacers **220**, **221** and the source and drain regions **222**, **223** in the embodiments described above with reference to FIGS. **2***a*, **2***b*, **3***a* and **3***b*.

Similar to the embodiments described above with reference to FIGS. **2***a*, **2***b*, **3***a* and **3***b*, other methods may be employed to form extended source and drain regions and source and drain regions adjacent the gate electrode **206**.

The particular embodiments disclosed above are illustrative only, as the invention may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. For example, the process steps set forth above may be performed in a different order. Furthermore, no limitations are intended to the details of construction or design herein shown, other than as described in the claims below. It is therefore evident that the particular embodiments disclosed above may be altered or modified and all such variations are considered within the scope and spirit of the invention. Accordingly, the protection sought herein is as set forth in the claims below.

What is claimed:

**1**. A method of forming a field effect transistor, comprising:

providing a semiconductor substrate, a gate electrode being formed above said semiconductor substrate;

forming at least one cavity in said substrate adjacent said gate electrode; and

forming a strain-creating element in said at least one cavity, said strain-creating element comprising:

a compound material comprising a first chemical element and a second chemical element, wherein said first chemical element comprises one of germanium and carbon, said second chemical element comprises silicon, and said semiconductor substrate comprises said second chemical element;

a first portion and a second portion, wherein said second portion is located above said first portion;

a first concentration ratio between a concentration of said first chemical element in said first portion and a concentration of said second chemical element in said first portion; and

a second concentration ratio between a concentration of said first chemical element in said second portion and a concentration of said second chemical element in said second portion, wherein said first concentration ratio is smaller than said second concentration ratio and wherein a ratio between a concentration of said first chemical element and a concentration of said second chemical element increases in a vertical direction with increasing distance from a bottom surface of said at least one cavity formed in said substrate.

**2**. The method of claim **1**, wherein said first portion of said strain-creating element and said second portion of said strain-creating element comprise sub-layers of said strain-creating element.

**3**. The method of claim **2**, wherein said second concentration ratio is greater than about 1%.

**4**. The method of claim **3**, wherein said second concentration ratio is greater than about 10%.

**5**. The method of claim **1**, wherein said formation of said strain-creating element comprises performing a selective epitaxial growth process.

**6**. The method of claim **5**, further comprising changing a ratio between a flow rate of a first reactant comprising said first chemical element and a flow rate of a second reactant comprising said second chemical element during said selective epitaxial growth process, wherein said ratio between said flow rates is increased substantially continuously during said selective epitaxial growth process.

**7**. A method of forming a field effect transistor, comprising:

providing a semiconductor substrate, a gate electrode being formed above said substrate;

forming at least one cavity in said substrate adjacent said gate electrode; and

performing a selective epitaxial growth process adapted to form a strain-creating element in said cavity, said strain-creating element comprising a compound material comprising a first chemical element and a second chemical element, said first chemical element comprising one of germanium and carbon, said second chemical element comprising silicon, and said semiconductor substrate comprising said second chemical element, wherein said selective epitaxial growth process comprises:

supplying a first reactant comprising said first chemical element and a second reactant comprising said second chemical element; and

increasing a ratio between a flow rate of said first reactant and a flow rate of said second reactant at least once during said selective epitaxial growth process, wherein said ratio between said flow rates is increased substantially continuously during said selective epitaxial growth process.

* * * * *

# Exhibit 4

**Exhibit 4** Case No. 6:22-cv-00200

## Claim Chart for U.S. Patent No. 7,005,376

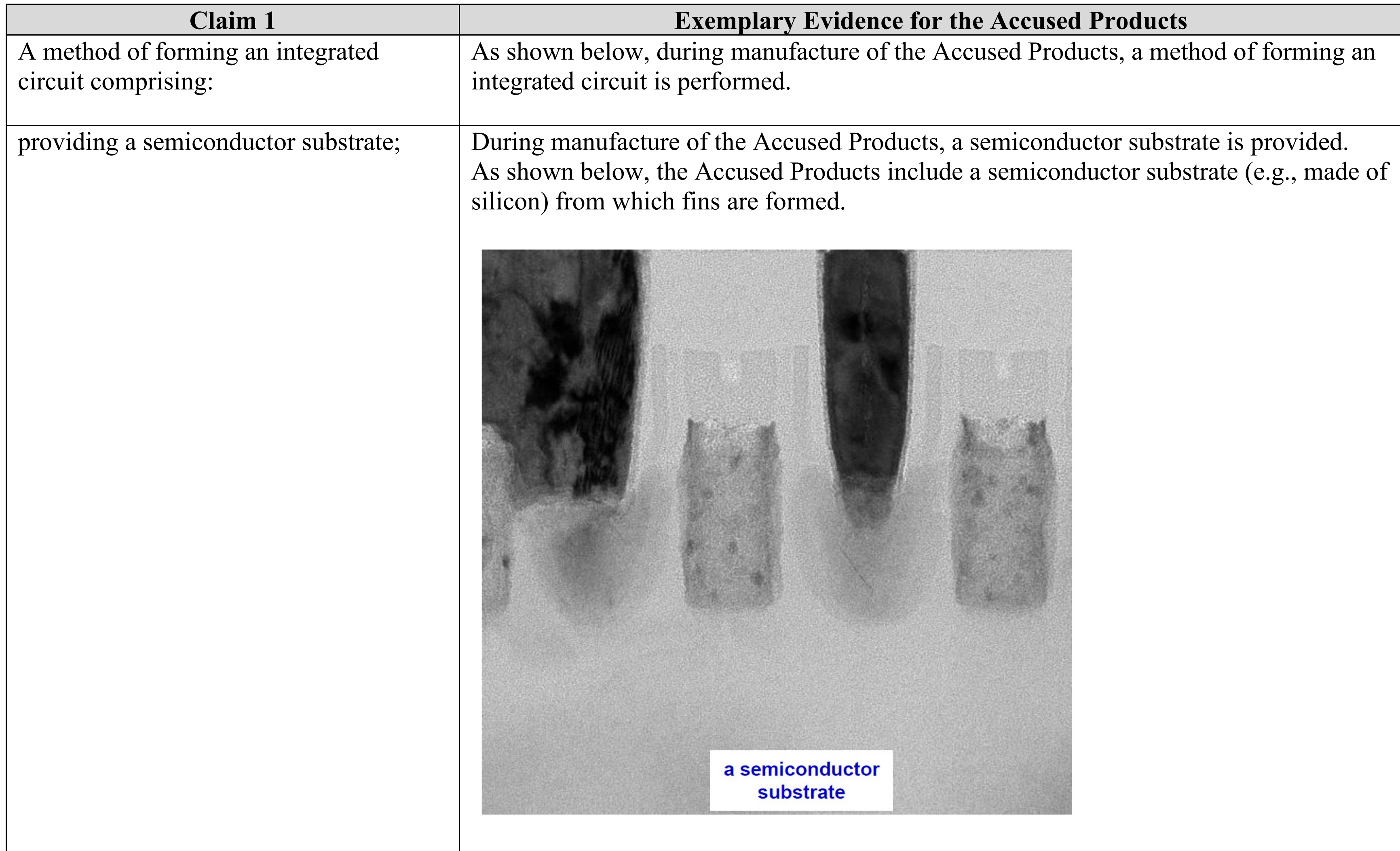
| Claim 1 | Exemplary Evidence for the Accused Products |
|---|---|
| A method of forming an integrated circuit comprising: | As shown below, during manufacture of the Accused Products, a method of forming an integrated circuit is performed. |
| providing a semiconductor substrate; | During manufacture of the Accused Products, a semiconductor substrate is provided.<br>As shown below, the Accused Products include a semiconductor substrate (e.g., made of silicon) from which fins are formed.<br> |

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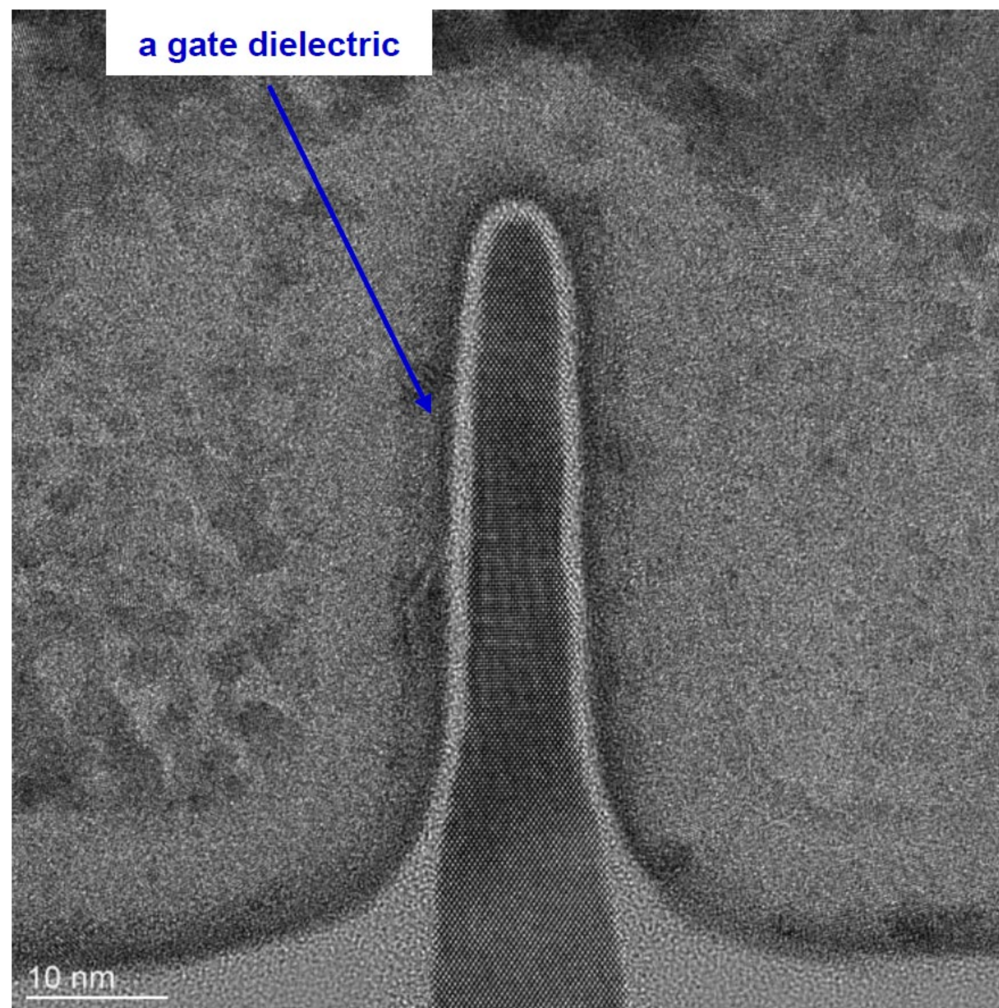
**Exhibit 4** Case No. 6:22-cv-00200

| | |
|---|---|
| forming a gate dielectric on the semiconductor substrate; | During manufacture of the Accused Products, a gate dielectric is formed on the semiconductor substrate. A shown below, the gate dielectric has an oxide interfacial layer followed by a high k dielectric (hafnium oxide) and is formed on the semiconductor substrate over the fin.   |

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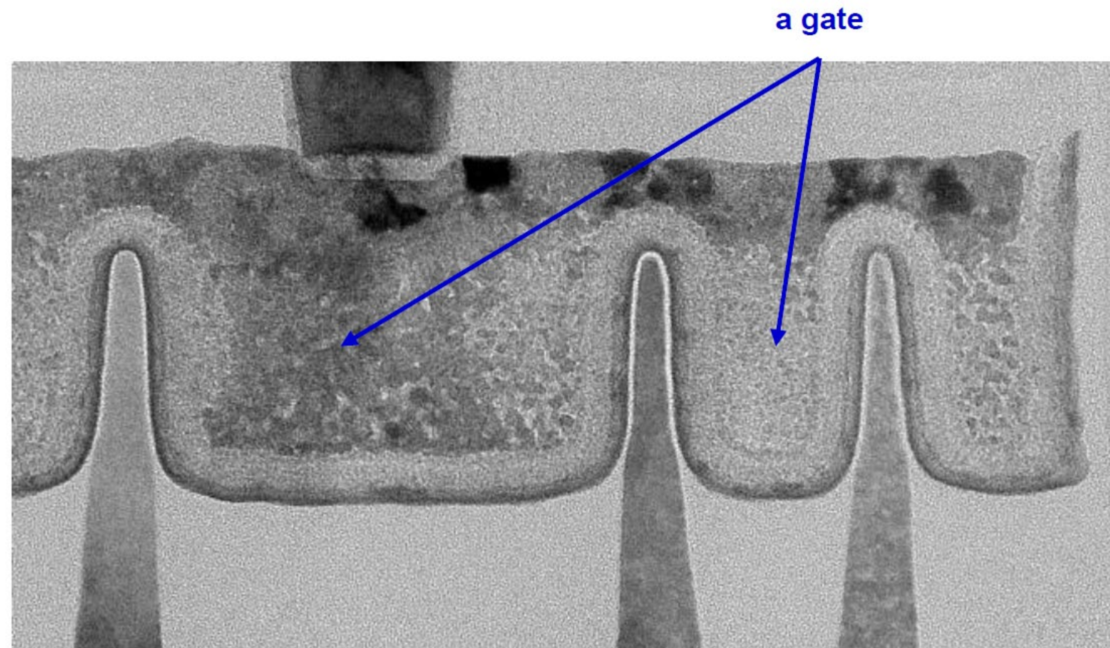
| | |
|---|---|
| forming a gate over the gate dielectric; | During manufacture of the Accused Products, a gate is formed over the gate dielectric. As shown below, the gate is a metal gate, which is formed over the gate dielectric and over the fin.   |
| forming source/drain junctions in the semiconductor substrate; | During manufacture of the Accused Products, source/drain junctions are formed in the semiconductor substrate. As shown below, the source and drain are formed in the upper portions of the fin on opposite sides of the gate. |

| | |
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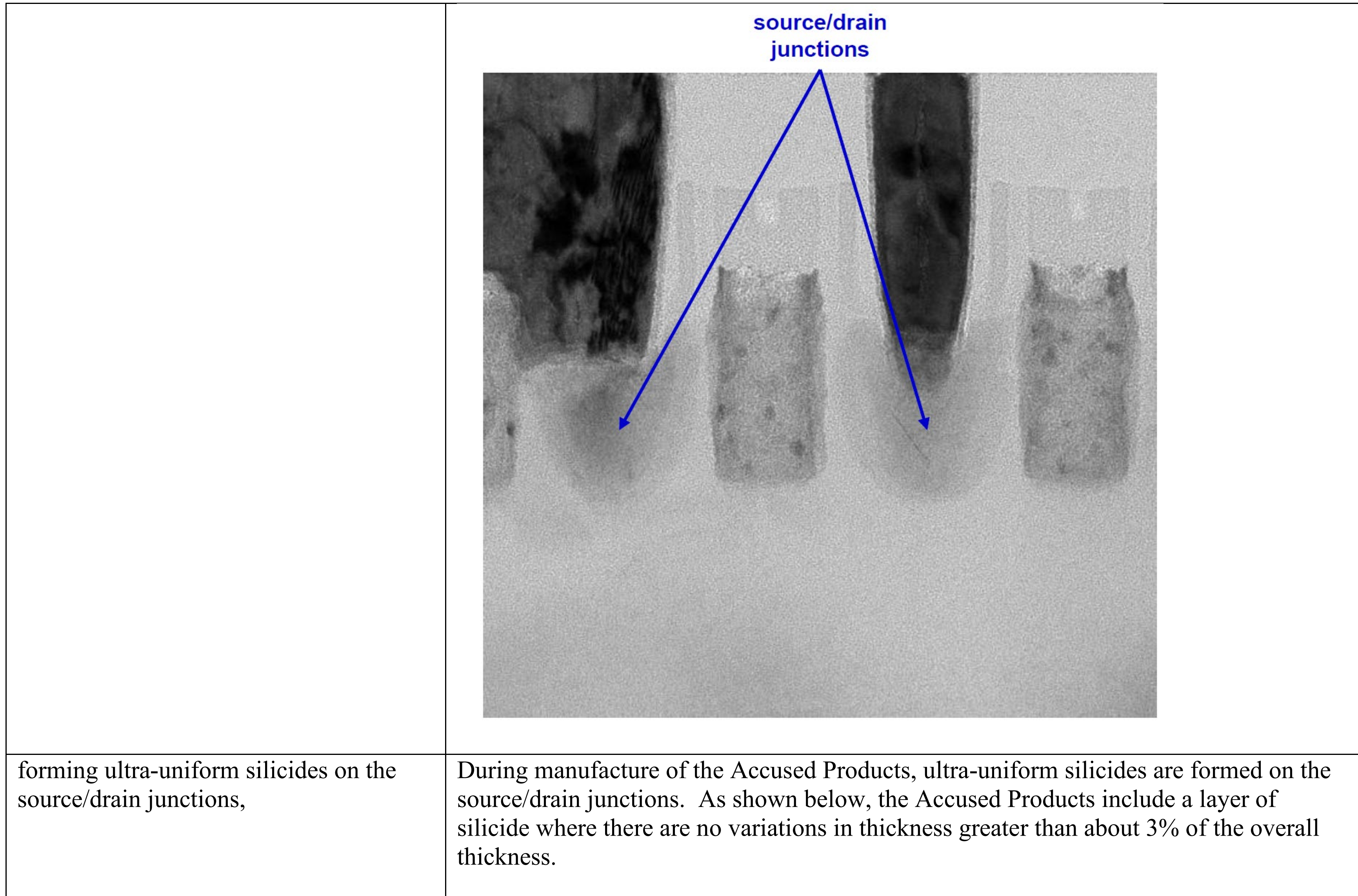
| |   |
| forming ultra-uniform silicides on the source/drain junctions, | During manufacture of the Accused Products, ultra-uniform silicides are formed on the source/drain junctions. As shown below, the Accused Products include a layer of silicide where there are no variations in thickness greater than about 3% of the overall thickness. |

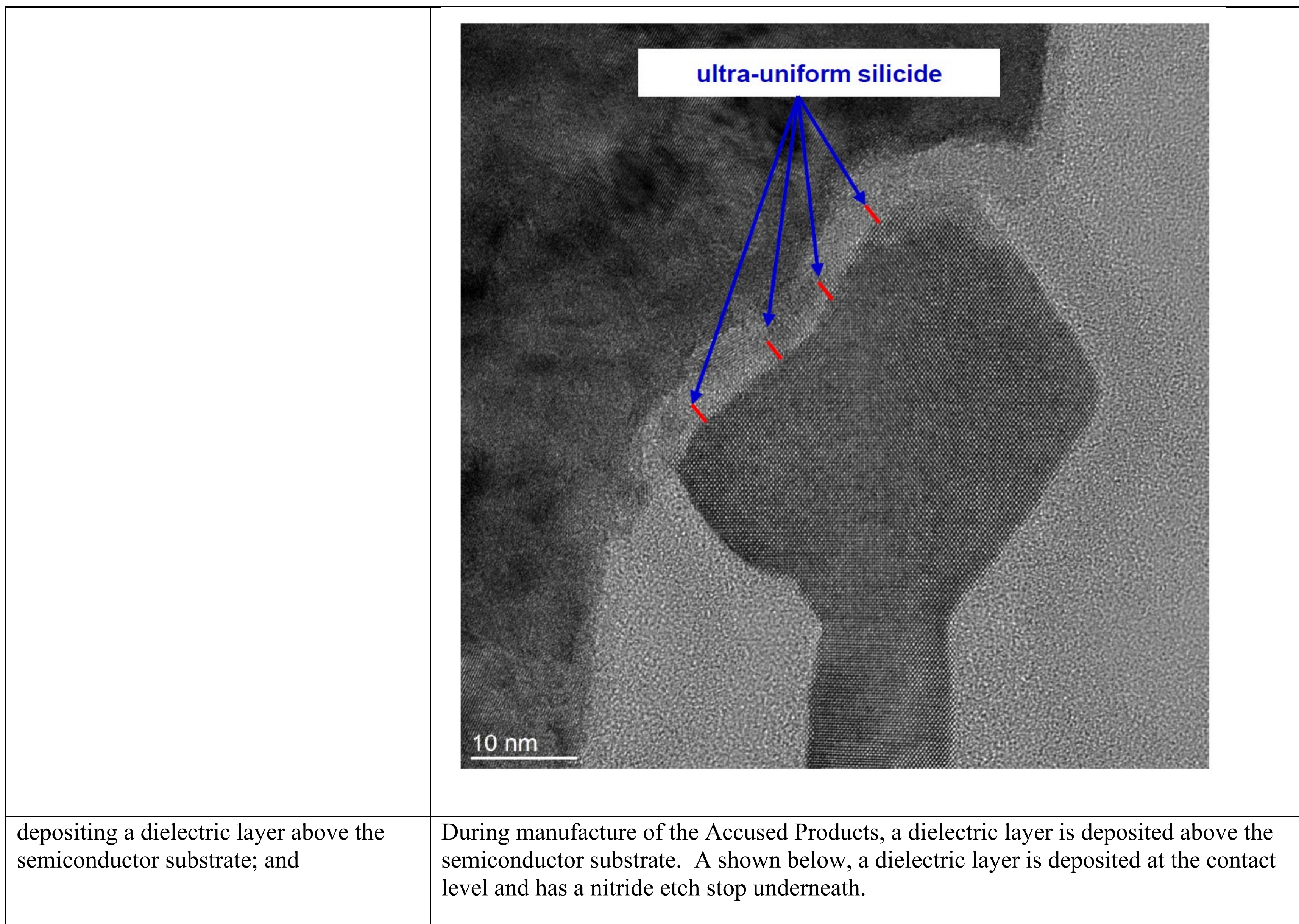
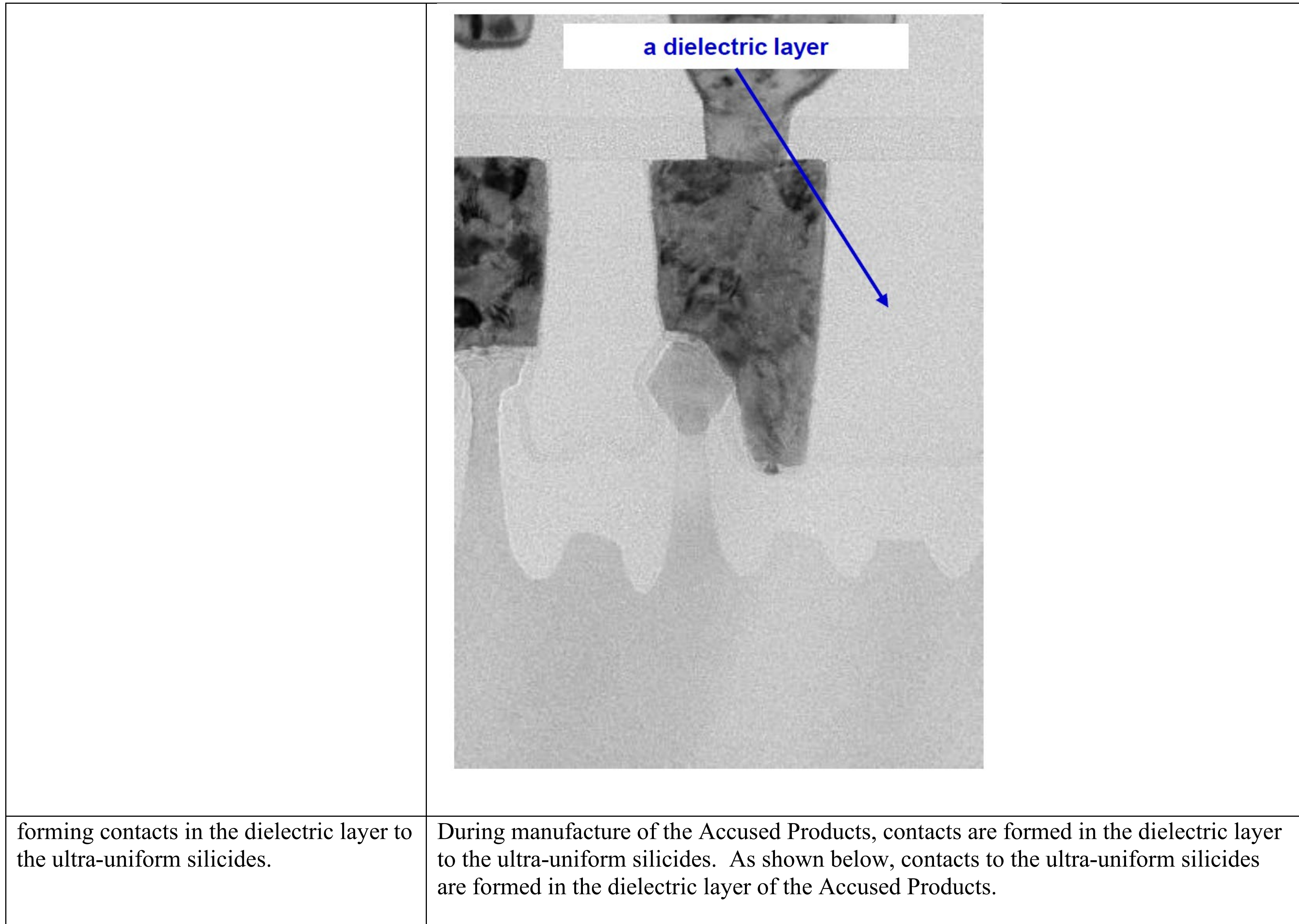
| | |
|---|---|
| |   |
| depositing a dielectric layer above the semiconductor substrate; and | During manufacture of the Accused Products, a dielectric layer is deposited above the semiconductor substrate. A shown below, a dielectric layer is deposited at the contact level and has a nitride etch stop underneath. |

**Exhibit 4** Case No. 6:22-cv-00200

<table>
<tr><td></td><td>
</td></tr>
<tr><td>forming contacts in the dielectric layer to the ultra-uniform silicides.</td><td>During manufacture of the Accused Products, contacts are formed in the dielectric layer to the ultra-uniform silicides. As shown below, contacts to the ultra-uniform silicides are formed in the dielectric layer of the Accused Products.</td></tr>
</table>

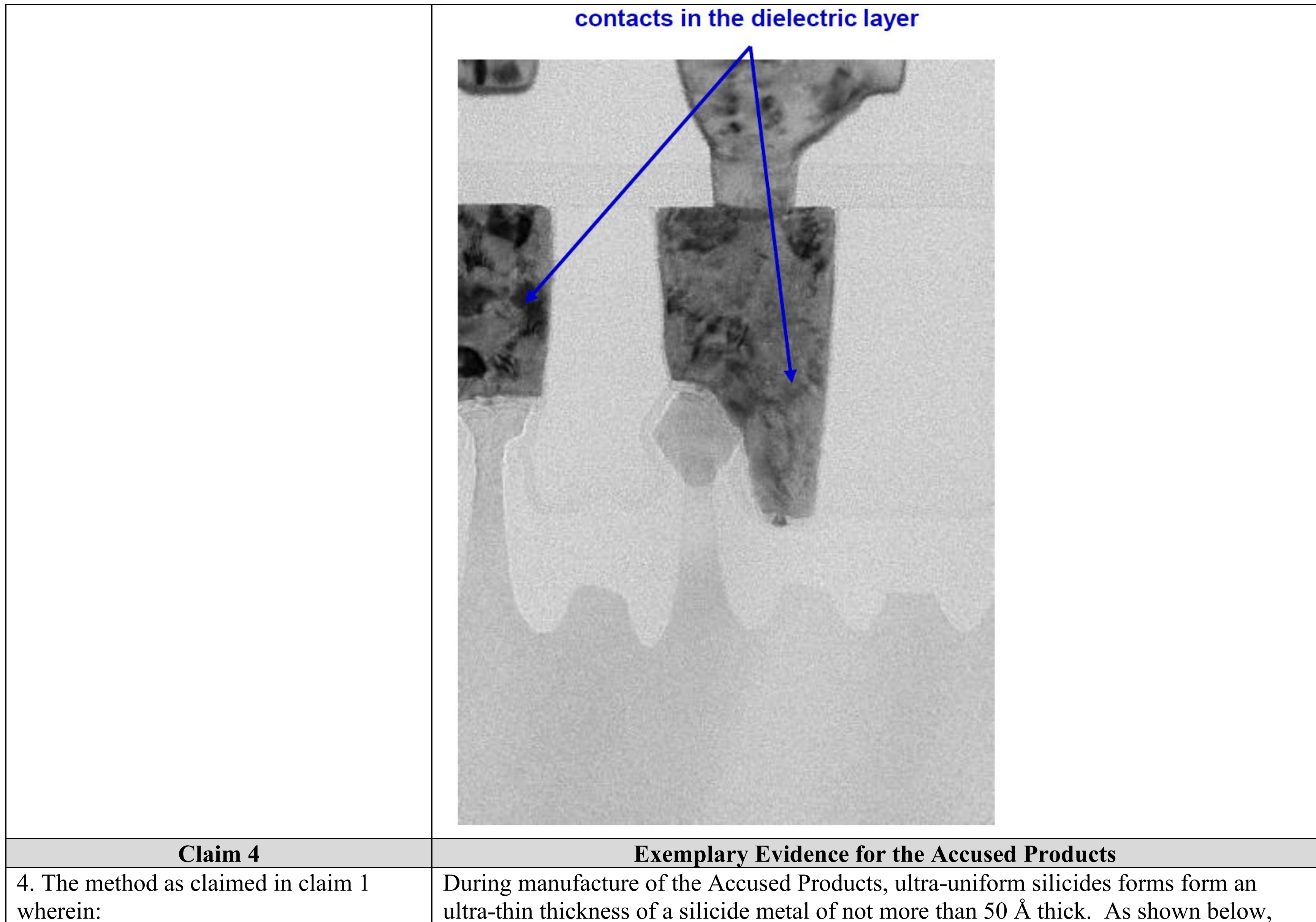
| |  |
|---|---|
| **Claim 4** | **Exemplary Evidence for the Accused Products** |
| 4. The method as claimed in claim 1 wherein: | During manufacture of the Accused Products, ultra-uniform silicides forms form an ultra-thin thickness of a silicide metal of not more than 50 Å thick. As shown below, |

**Exhibit 4** Case No. 6:22-cv-00200

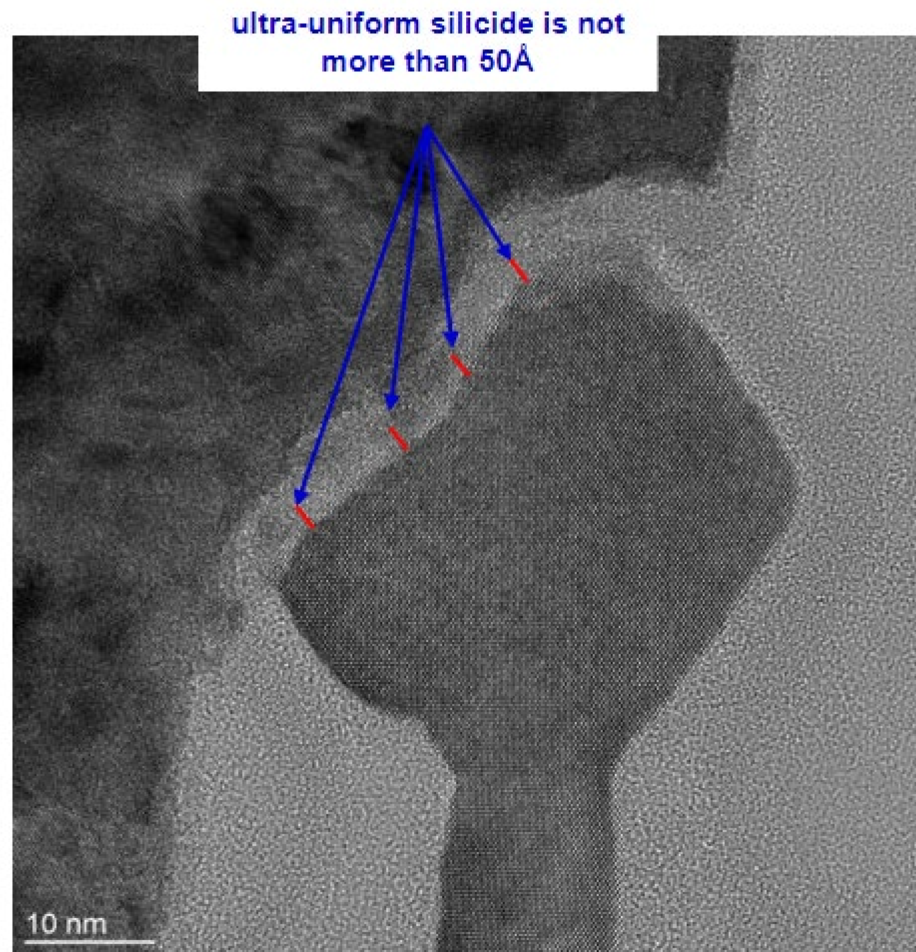
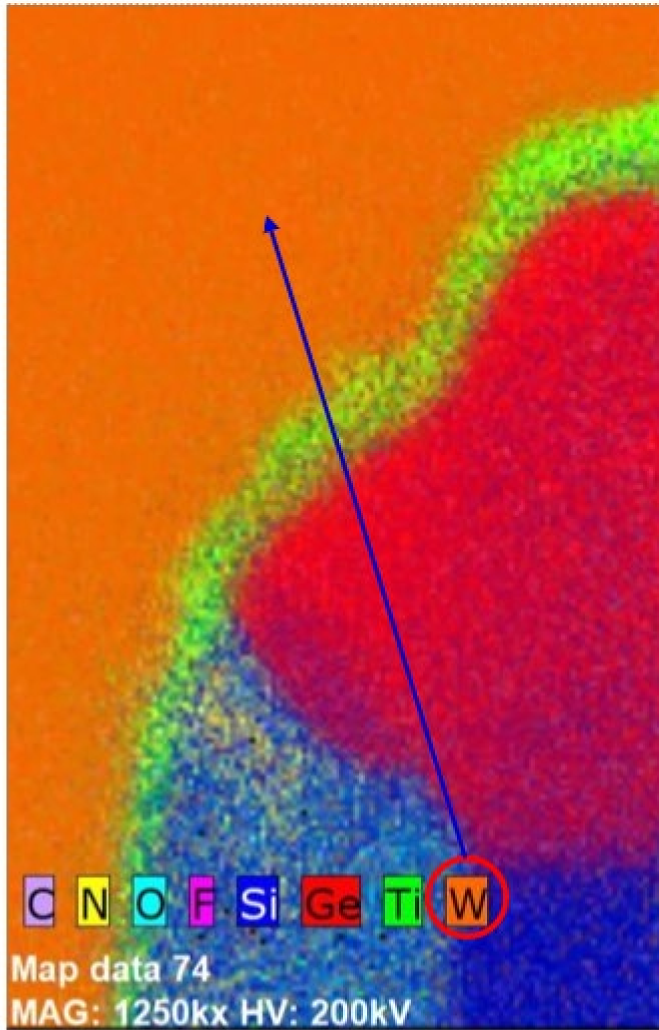
| | |
|---|---|
| forming the ultra-uniform silicides forms an ultra-thin thickness of a silicide metal of not more than 50 Å thick. | the ultra-uniform silicide forms an ultra-thin thickness of silicide metal, measuring 1.4 nm thick.   |
| **Claim 6** | **Exemplary Evidence for the Accused Products** |
| 6. The method as claimed in claim 1 wherein: | During manufacture of the Accused Products, the contacts to the ultra-uniform silicides are formed using materials selected from a group consisting of tantalum, titanium, tungsten, copper, gold, silver, an alloy thereof, a compound thereof, and a combination |

**Exhibit 4** Case No. 6:22-cv-00200

| | |
|---|---|
| forming the contacts to the ultra-uniform silicides uses materials selected from a group consisting of tantalum, titanium, tungsten, copper, gold, silver, an alloy thereof, a compound thereof, and a combination thereof. | thereof. As shown below, the contacts to the ultra-uniform silicides are made of tungsten.   |

# Exhibit 5

**Exhibit 5** Case No. 6:22-cv-00200

**Claim Chart for U.S. Patent No. 7,307,322**

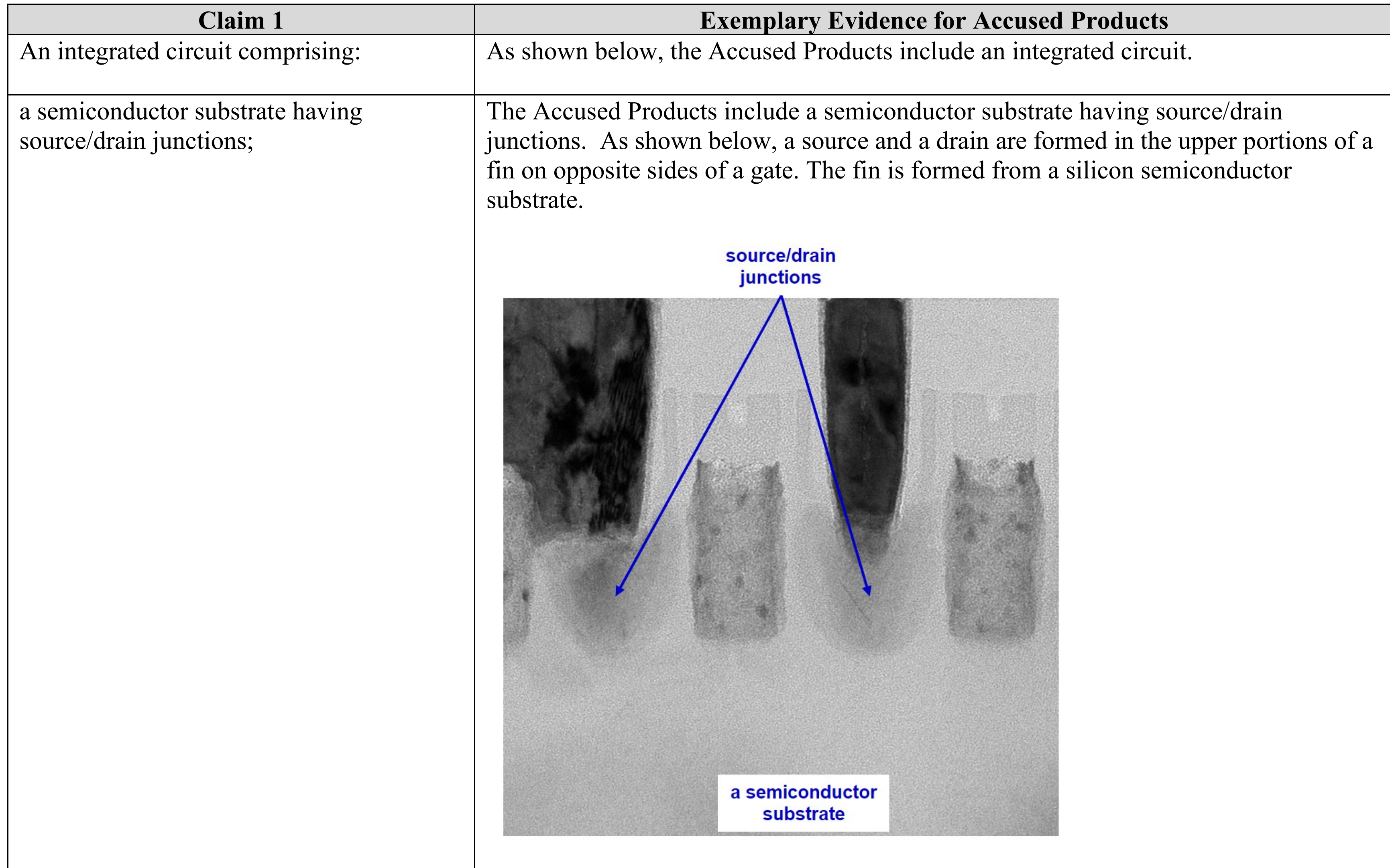
| Claim 1 | Exemplary Evidence for Accused Products |
|---|---|
| An integrated circuit comprising: | As shown below, the Accused Products include an integrated circuit. |
| a semiconductor substrate having source/drain junctions; | The Accused Products include a semiconductor substrate having source/drain junctions. As shown below, a source and a drain are formed in the upper portions of a fin on opposite sides of a gate. The fin is formed from a silicon semiconductor substrate.   |

**Exhibit 5** Case No. 6:22-cv-00200

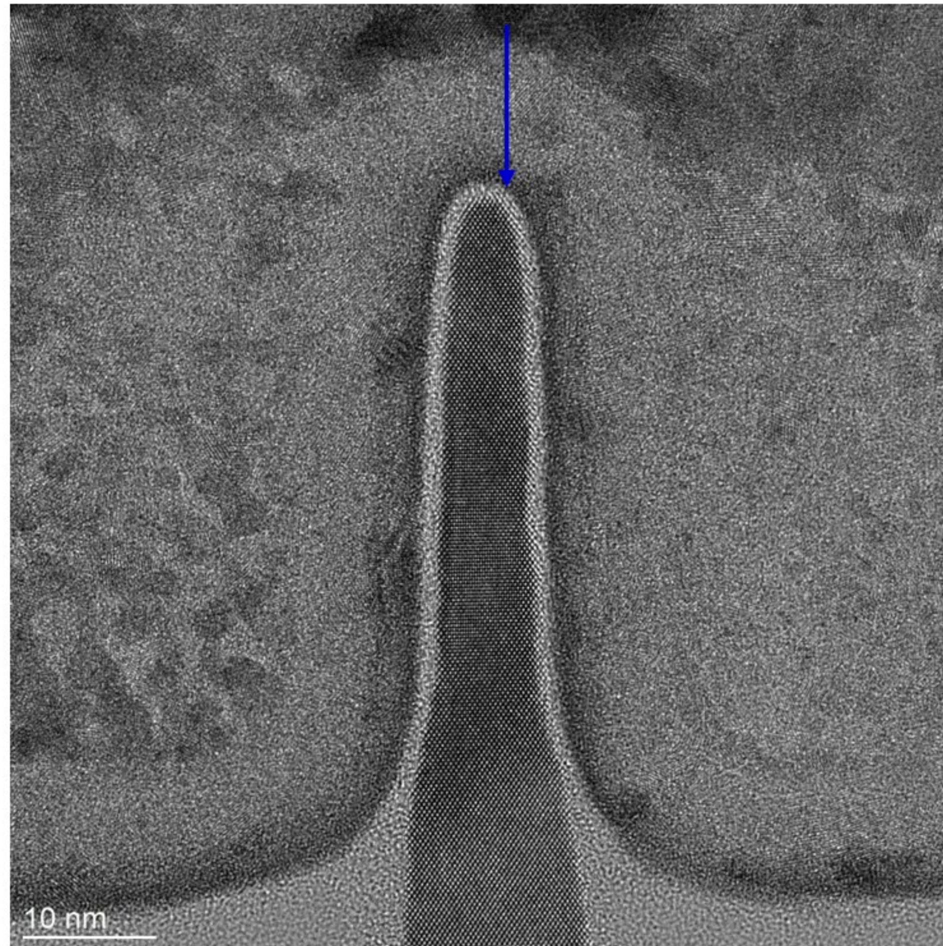
| | |
|---|---|
| a gate dielectric on the semiconductor substrate; | The Accused Products include a gate dielectric on the semiconductor substrate. As shown below, the gate dielectric has an oxide interfacial layer followed by a high k dielectric (hafnium oxide) and is over the fin.<br><br> |

**Exhibit 5** Case No. 6:22-cv-00200

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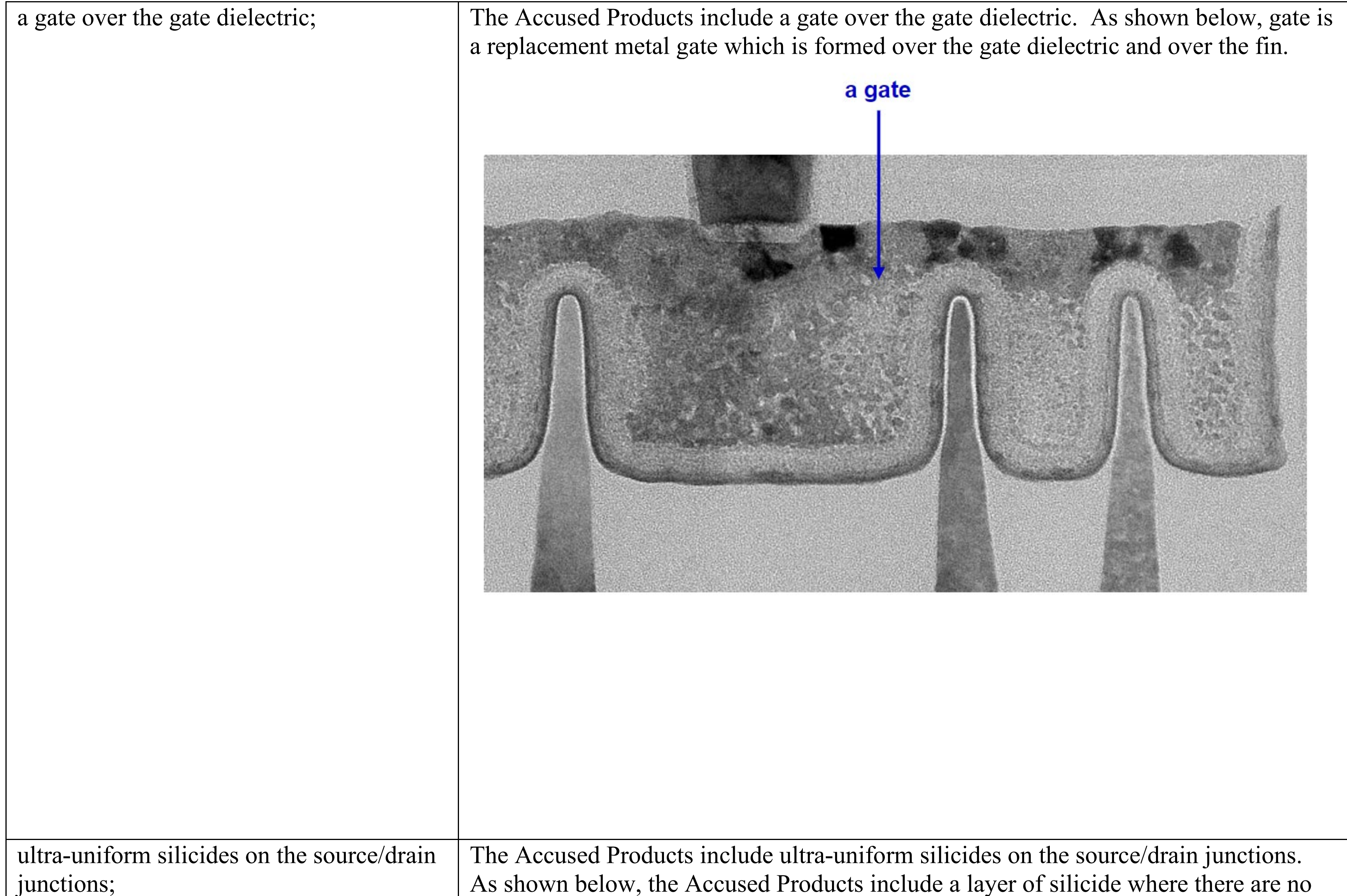
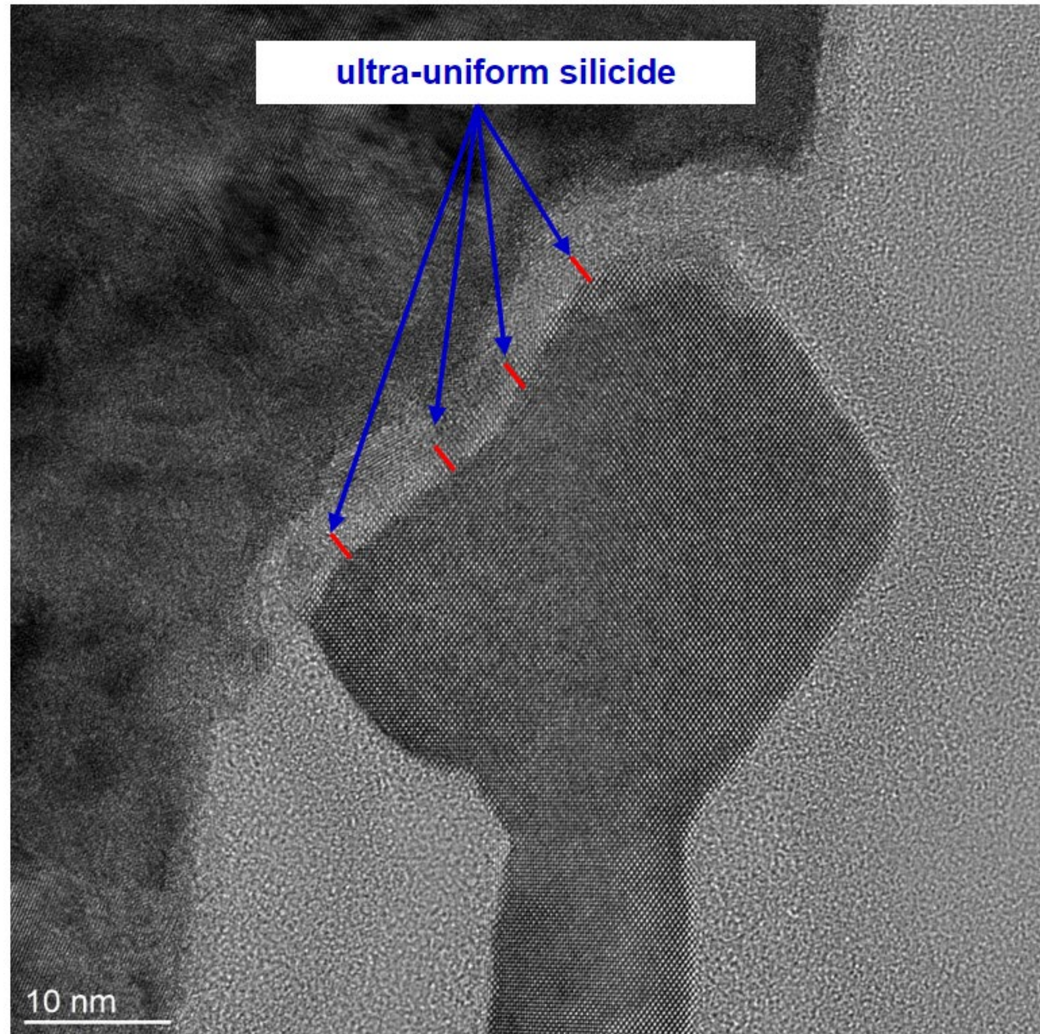
| a gate over the gate dielectric; | The Accused Products include a gate over the gate dielectric. As shown below, gate is a replacement metal gate which is formed over the gate dielectric and over the fin.   |
| ultra-uniform silicides on the source/drain junctions; | The Accused Products include ultra-uniform silicides on the source/drain junctions. As shown below, the Accused Products include a layer of silicide where there are no |

| | variations in thickness greater than about 3% of the overall thickness.   |
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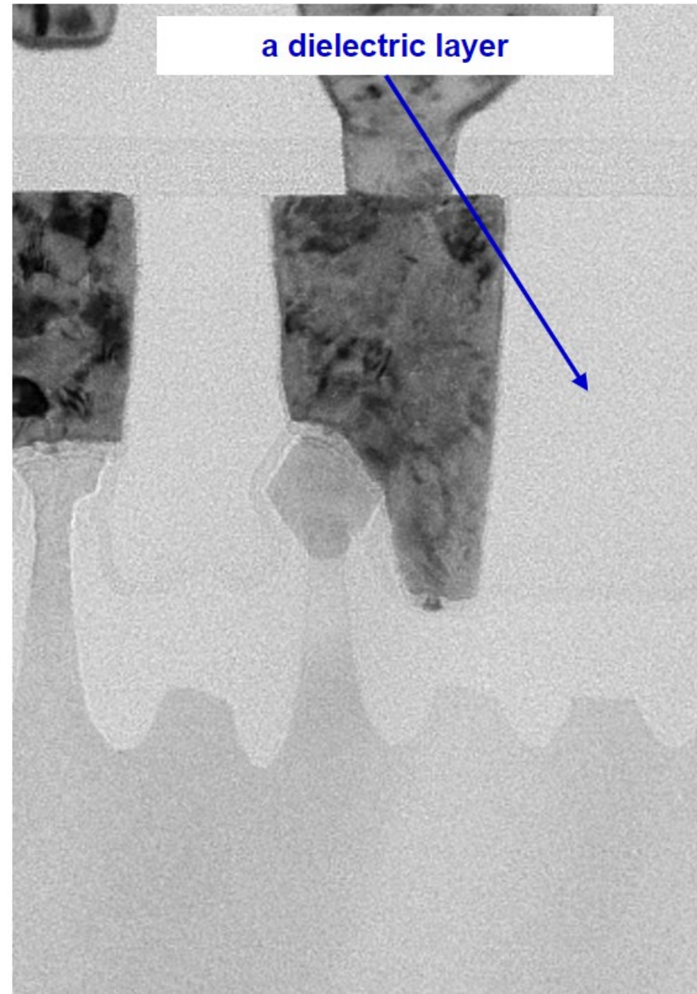
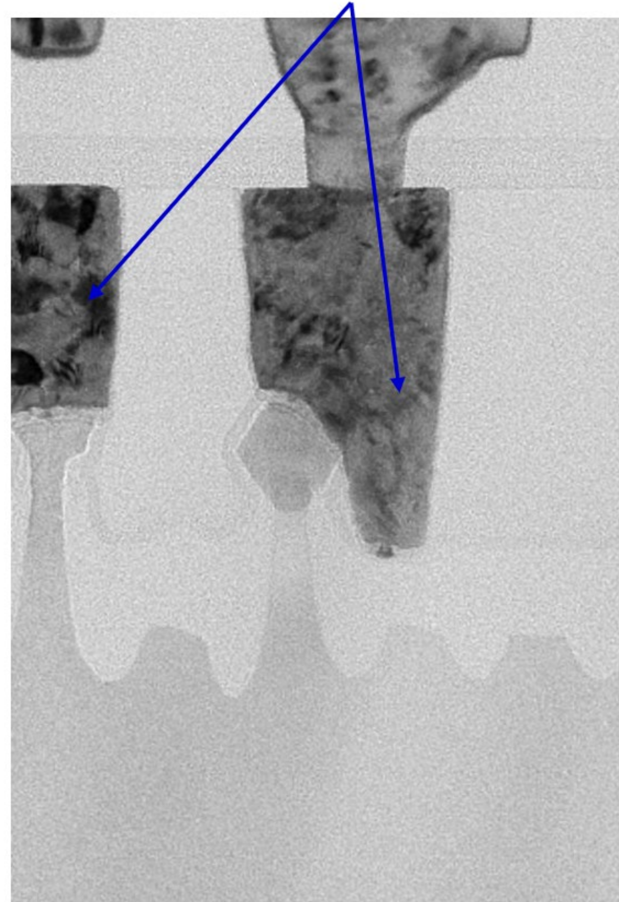
| a dielectric layer above the semiconductor substrate; and | The Accused Products include a dielectric layer above the semiconductor substrate. As shown below, there is a dielectric layer at the contact level that has a nitride etch stop underneath.<br><br> |

| contacts in the dielectric layer to the ultra-uniform silicides. | The Accused Products include contacts in the dielectric layer to the ultra-uniform silicides. As shown below, contacts to the ultra-uniform silicides are formed in the dielectric layer of the Accused Products.<br><br><br> |
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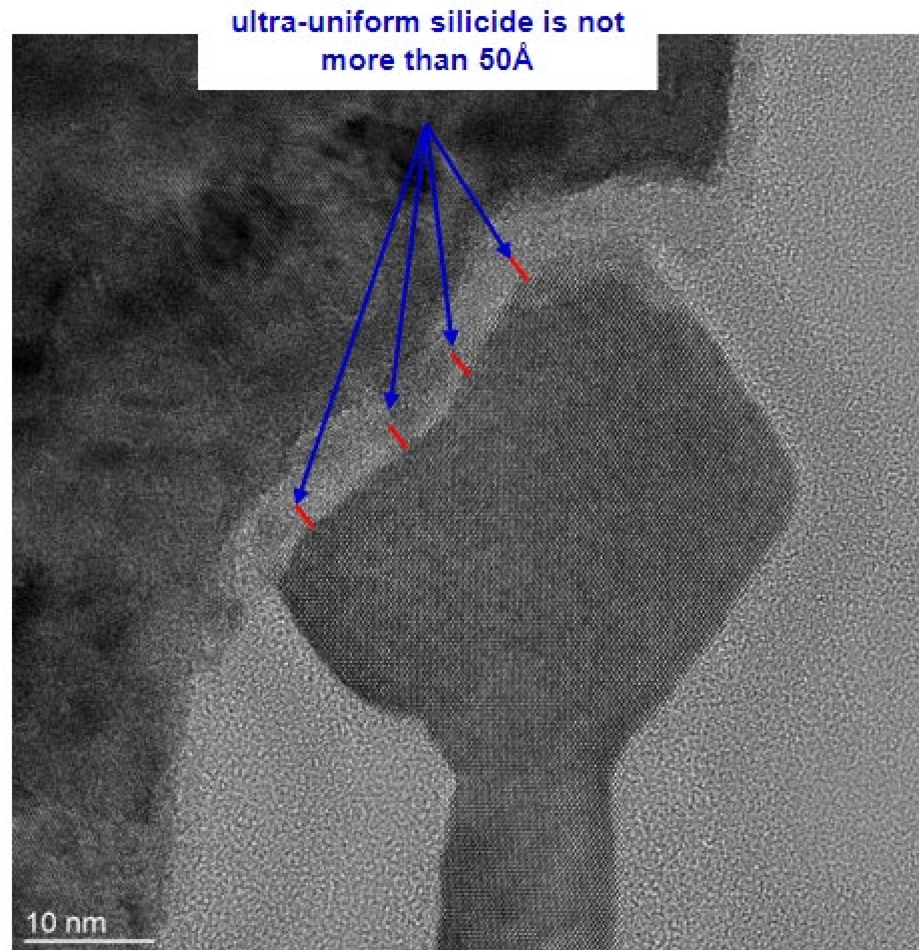
| **Claim 2** | **Exemplary Evidence for Accused Products** |

**Exhibit 5** Case No. 6:22-cv-00200

| 2. The integrated circuit as claimed in claim 1 wherein:<br>the ultra-uniform silicides is an ultra-thin thickness of a silicide metal of not more than 50 Å thick. | The Accused Products include ultra-uniform silicides that are an ultra-thin thickness of a silicide metal of not more than 50 Å thick. As shown below, the ultra-uniform silicide forms an ultra-thin thickness of silicide metal, measuring 1.4 nm thick.<br><br> |
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| Claim 4 | Exemplary Evidence for Accused Products |
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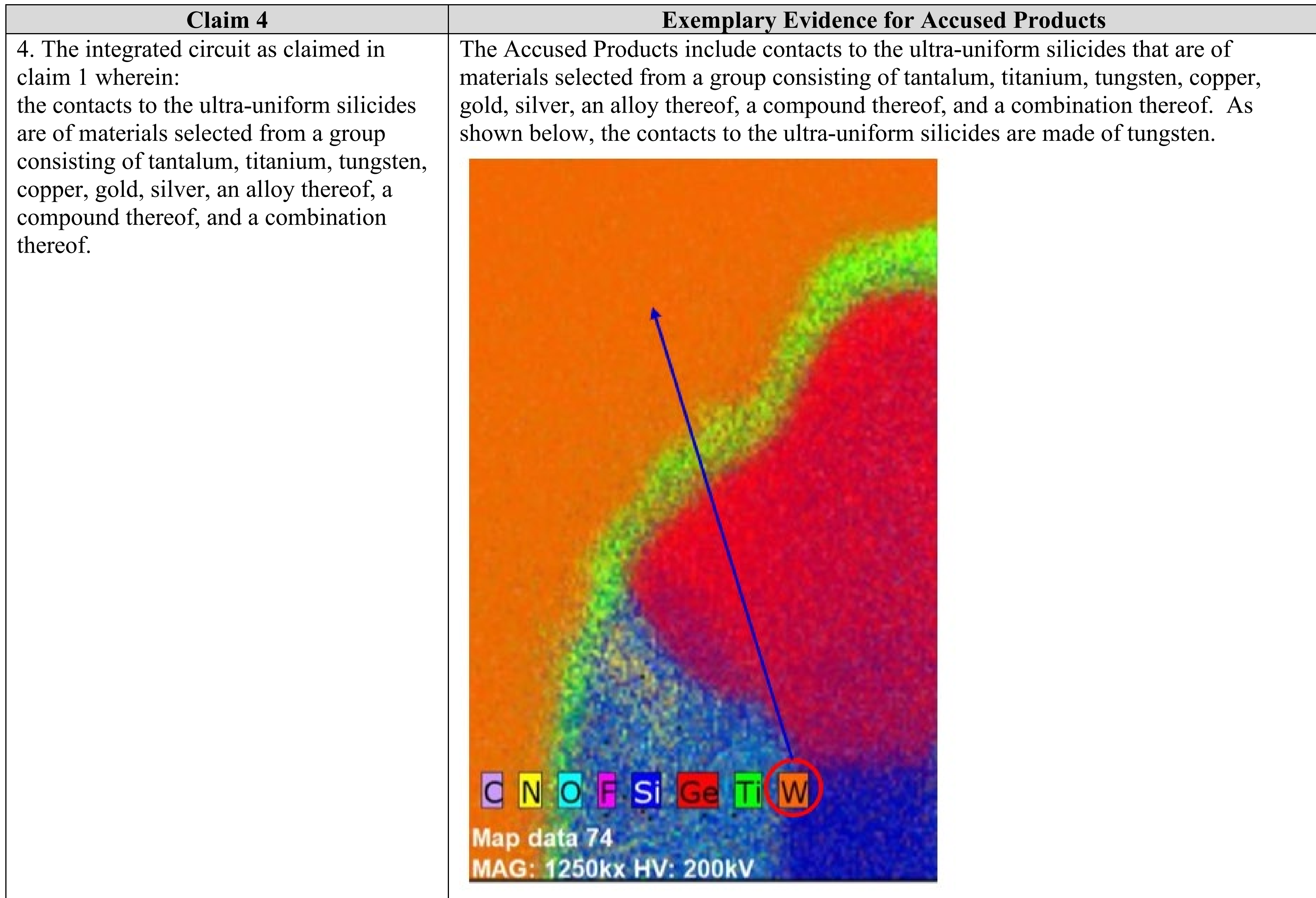
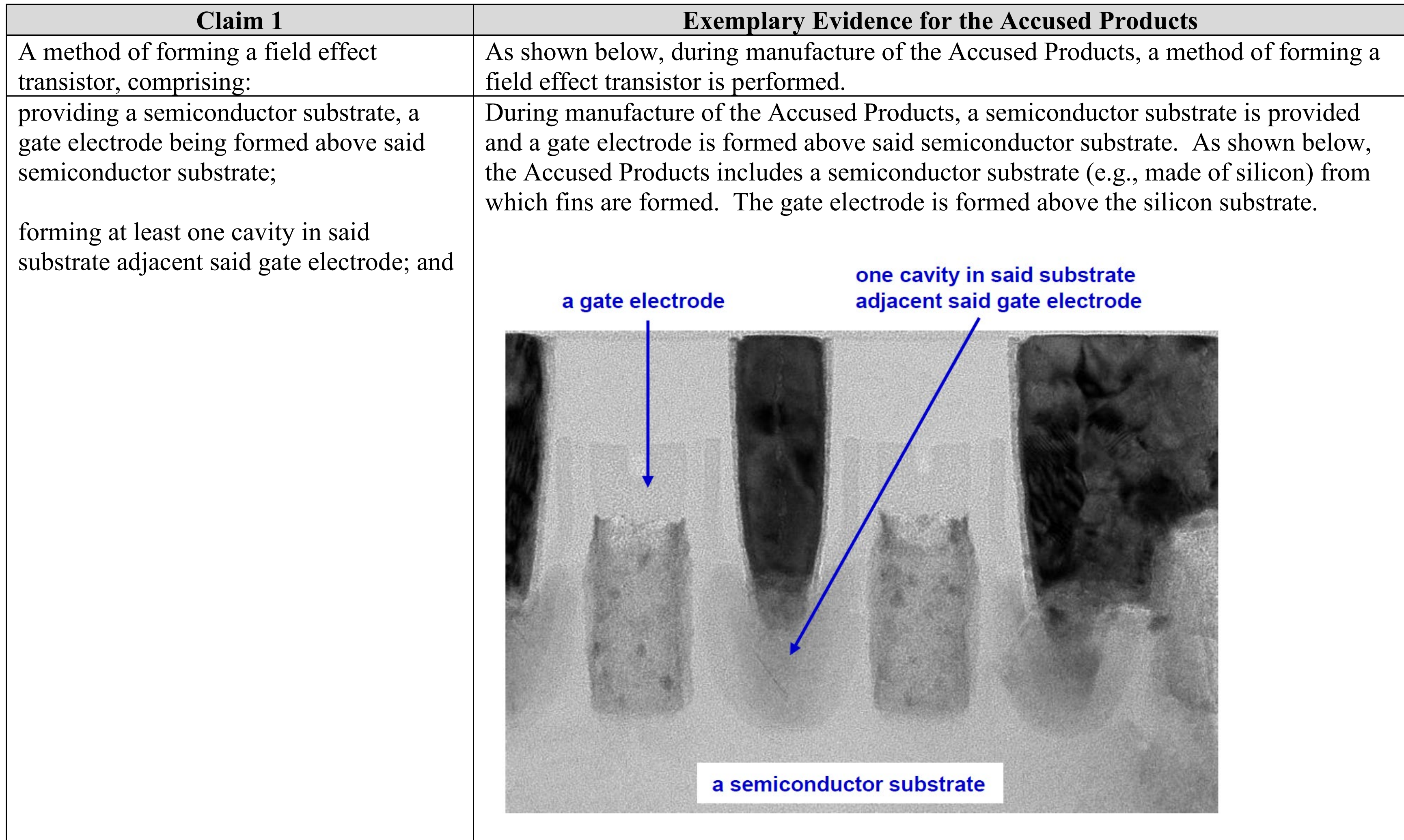
| 4. The integrated circuit as claimed in claim 1 wherein:<br>the contacts to the ultra-uniform silicides are of materials selected from a group consisting of tantalum, titanium, tungsten, copper, gold, silver, an alloy thereof, a compound thereof, and a combination thereof. | The Accused Products include contacts to the ultra-uniform silicides that are of materials selected from a group consisting of tantalum, titanium, tungsten, copper, gold, silver, an alloy thereof, a compound thereof, and a combination thereof. As shown below, the contacts to the ultra-uniform silicides are made of tungsten.<br> |

# Exhibit 6

**Exhibit 6** Case No. 6:22-cv-00200

**Claim Chart for U.S. Patent No. 7,629,211**

| Claim 1 | Exemplary Evidence for the Accused Products |
|---|---|
| A method of forming a field effect transistor, comprising: | As shown below, during manufacture of the Accused Products, a method of forming a field effect transistor is performed. |
| providing a semiconductor substrate, a gate electrode being formed above said semiconductor substrate;<br><br>forming at least one cavity in said substrate adjacent said gate electrode; and | During manufacture of the Accused Products, a semiconductor substrate is provided and a gate electrode is formed above said semiconductor substrate. As shown below, the Accused Products includes a semiconductor substrate (e.g., made of silicon) from which fins are formed. The gate electrode is formed above the silicon substrate.<br><br> |

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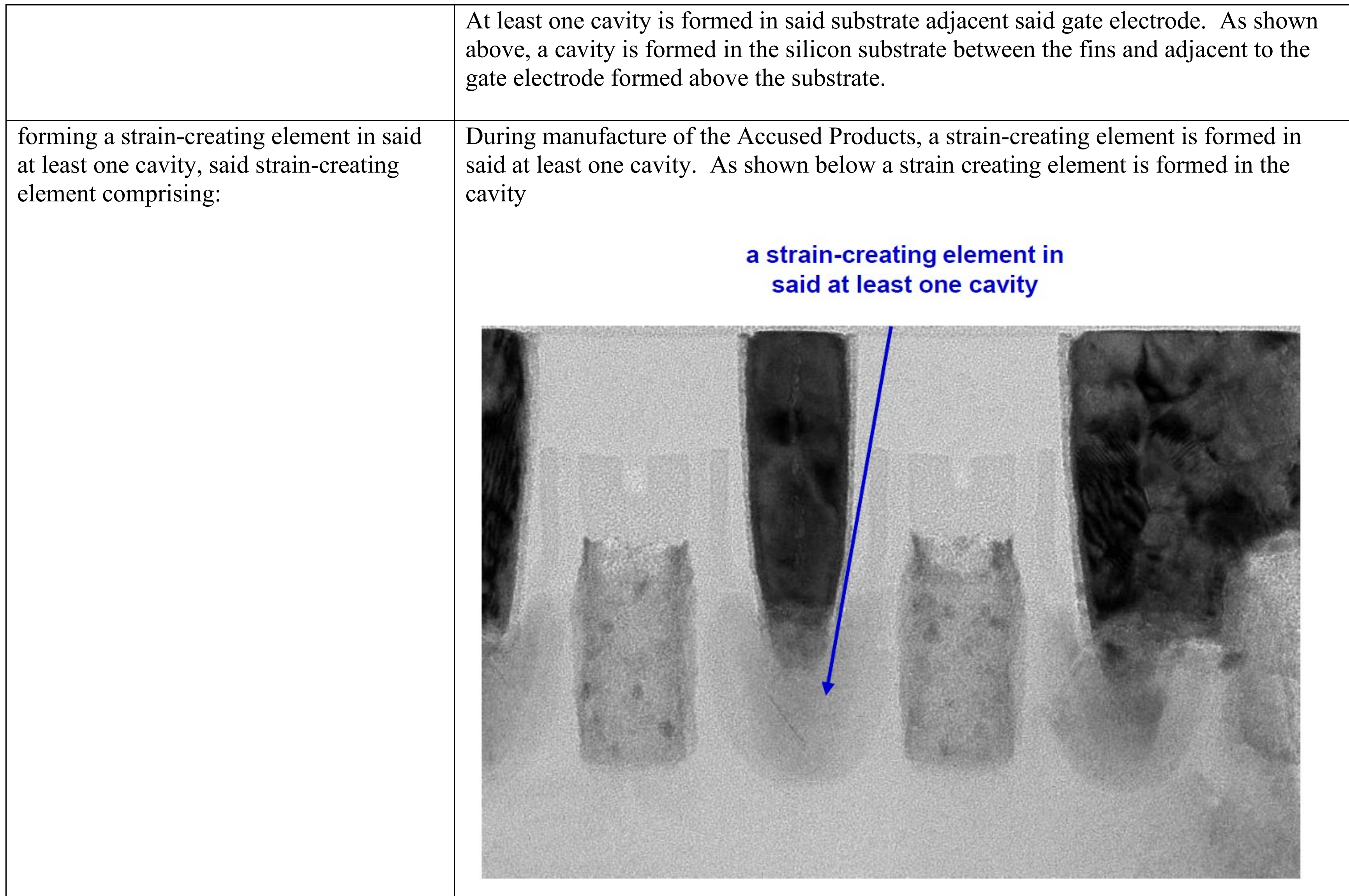
| | At least one cavity is formed in said substrate adjacent said gate electrode. As shown above, a cavity is formed in the silicon substrate between the fins and adjacent to the gate electrode formed above the substrate. |
| forming a strain-creating element in said at least one cavity, said strain-creating element comprising: | During manufacture of the Accused Products, a strain-creating element is formed in said at least one cavity. As shown below a strain creating element is formed in the cavity  |

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| | Silicon-Germanium (SiGe) is a strain-creating element and is formed in the cavity in the silicon substrate between the fins and adjacent to the gate electrode formed above the substrate. |
| a compound material comprising a first chemical element and a second chemical element, wherein said first chemical element comprises one of germanium and carbon, said second chemical element comprises silicon, and said semiconductor substrate comprises said second chemical element; | During manufacture of the Accused Products, said strain-creating element comprises a compound material comprising a first chemical element and a second chemical element, wherein said first chemical element comprises one of germanium and carbon, said second chemical element comprises silicon, and said semiconductor substrate comprises said second chemical element.<br><br>As shown below in an image of the cavity of the Accused Products using a color gradient, the strain-creating element formed in the cavity comprises SiGe (a compound material) that comprises germanium (a first chemical element that comprises one of germanium and carbon) and silicon (a second chemical element that comprises silicon). Germanium is shown in red and silicon is shown in blue. The semiconductor substrate (e.g., shown in blue near the bottom of the image) also comprises silicon (the second chemical element). |

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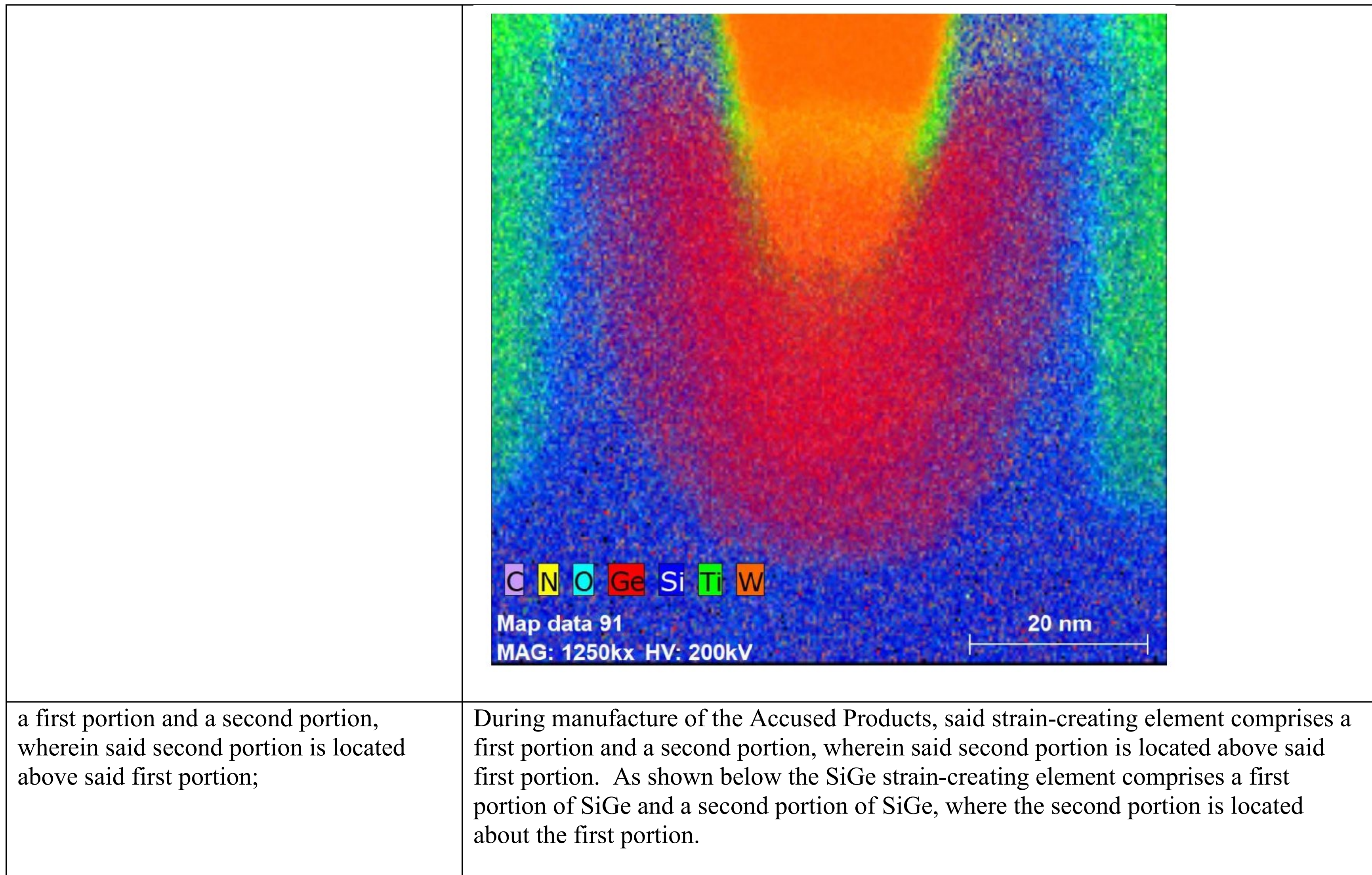
| |   |
| a first portion and a second portion, wherein said second portion is located above said first portion; | During manufacture of the Accused Products, said strain-creating element comprises a first portion and a second portion, wherein said second portion is located above said first portion. As shown below the SiGe strain-creating element comprises a first portion of SiGe and a second portion of SiGe, where the second portion is located about the first portion. |

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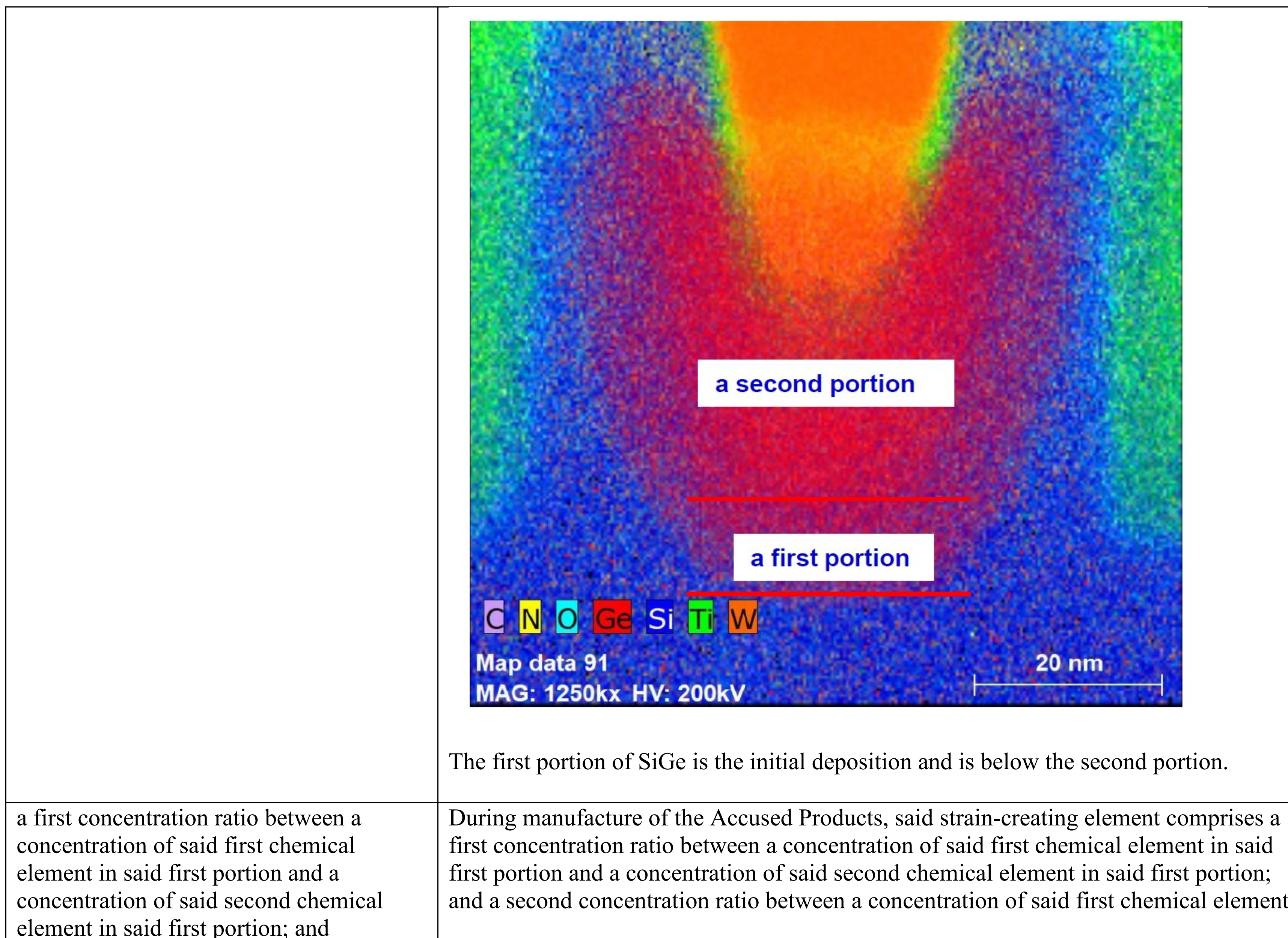
| |   The first portion of SiGe is the initial deposition and is below the second portion. |
| a first concentration ratio between a concentration of said first chemical element in said first portion and a concentration of said second chemical element in said first portion; and | During manufacture of the Accused Products, said strain-creating element comprises a first concentration ratio between a concentration of said first chemical element in said first portion and a concentration of said second chemical element in said first portion; and a second concentration ratio between a concentration of said first chemical element |

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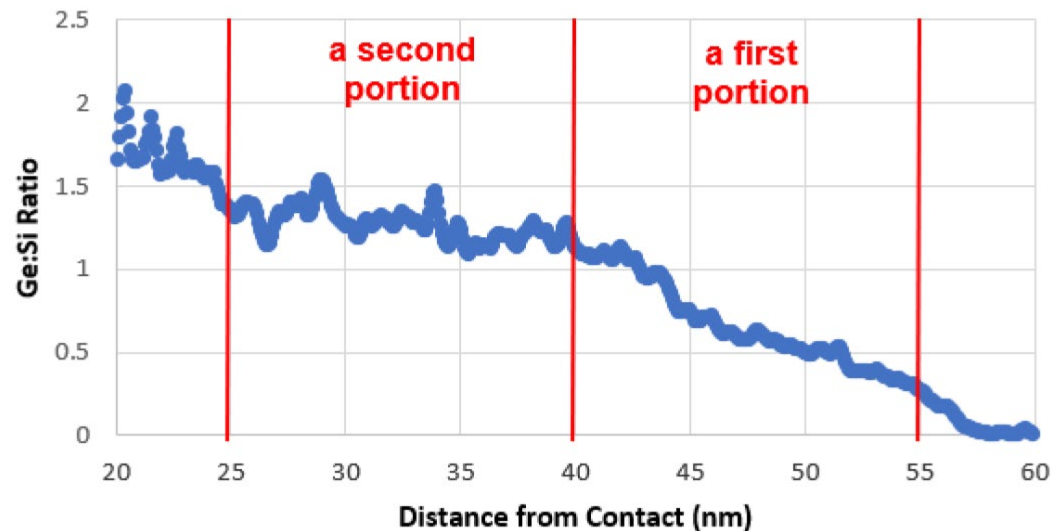
| a second concentration ratio between a concentration of said first chemical element in said second portion and a concentration of said second chemical element in said second portion, | in said second portion and a concentration of said second chemical element in said second portion.<br><br>As shown below, the SiGe strain-creating element comprises a first concentration ratio between a concentration of germanium (said first chemical element) in the initial deposition (in said first portion) and a concentration of silicon (said second chemical element) in the initial deposition (said first portion); and a second concentration ratio between a concentration of germanium (said first chemical element) in the upper portion from subsequent deposition (in said second portion) and a concentration of silicon (said second chemical element) in the upper portion from subsequent deposition (in said second portion).<br><br><br><br><br>As shown above, the first chemical element is Ge and the second chemical element is Si. The distance referenced in the chart above is measured from the bottom of the contact to the fin/substrate. |

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| | |
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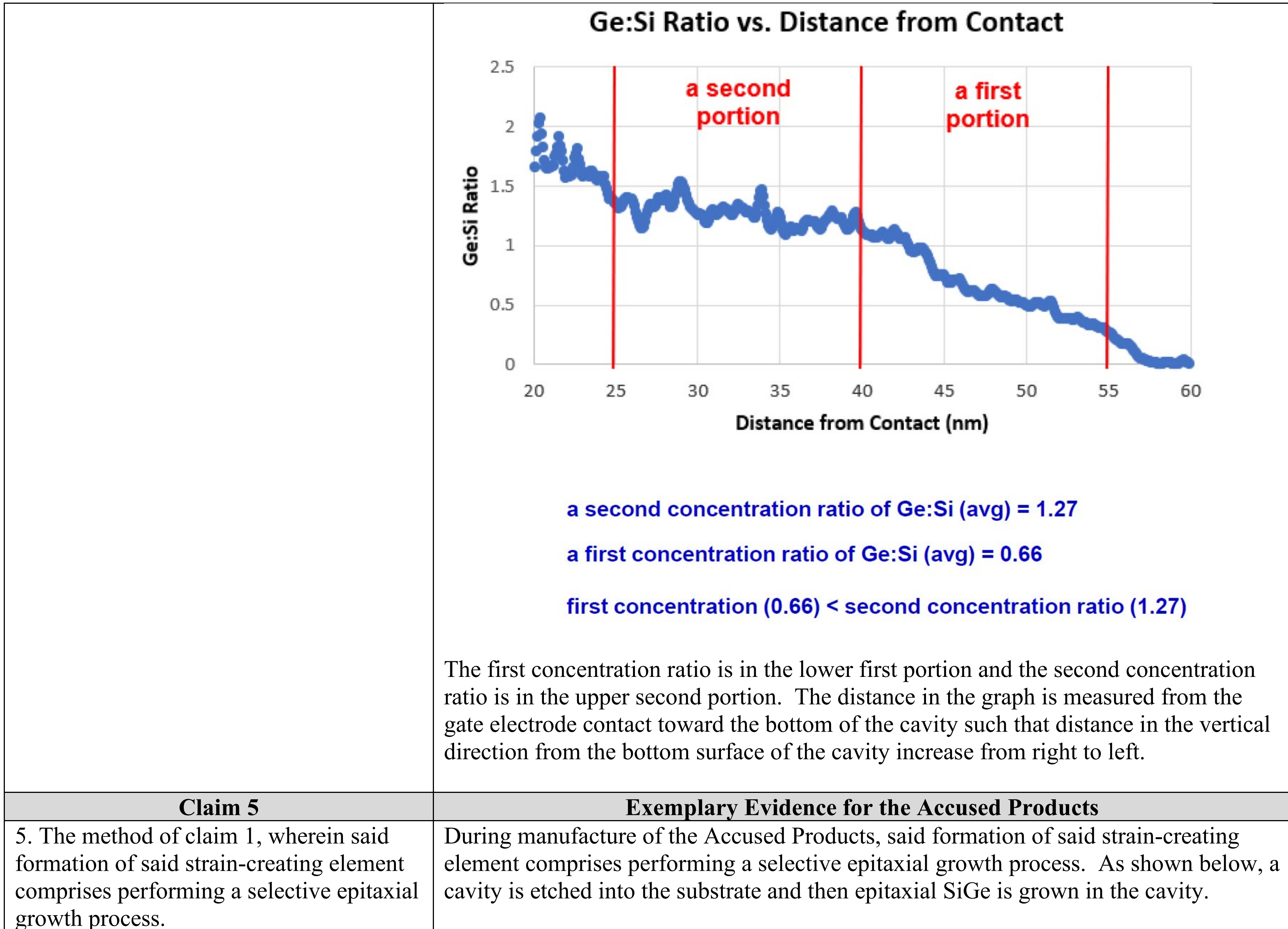
| | The first concentration ratio is in the lower first portion and the second concentration ratio is in the upper second portion. For example, the first concentration ratio of Ge:Si is approximately 1.7 (average), and the second concentration ratio of Ge:Si is 0.66 (average). The first concentration (0.66) is less than the second concentration (1.27). |
| wherein said first concentration ratio is smaller than said second concentration ratio and wherein a ratio between a concentration of said first chemical element and a concentration of said second chemical element increases in a vertical direction with increasing distance from a bottom surface of said at least one cavity formed in said substrate. | During manufacture of the Accused Products, said first concentration ratio is smaller than said second concentration ratio and wherein a ratio between a concentration of said first chemical element and a concentration of said second chemical element increases in a vertical direction with increasing distance from a bottom surface of said at least one cavity formed in said substrate.<br><br>As shown in the chart below, the first concentration ratio (e.g., 0.66 in the first, lower portion) is smaller than the second concentration ratio (e.g., 1.27 in the second, upper portion). The chart below also shows that the ratio between a concentration of germanium (said first chemical element) and a concentration of silicon (said second chemical element) increases in a vertical direction with increasing distance from a bottom surface of the cavity in the silicon substrate (i.e., said at least one cavity formed in said substrate). |




The first concentration ratio is in the lower first portion and the second concentration ratio is in the upper second portion. The distance in the graph is measured from the gate electrode contact toward the bottom of the cavity such that distance in the vertical direction from the bottom surface of the cavity increase from right to left.

| Claim 5 | Exemplary Evidence for the Accused Products |
|---|---|
| 5. The method of claim 1, wherein said formation of said strain-creating element comprises performing a selective epitaxial growth process. | During manufacture of the Accused Products, said formation of said strain-creating element comprises performing a selective epitaxial growth process. As shown below, a cavity is etched into the substrate and then epitaxial SiGe is grown in the cavity. |

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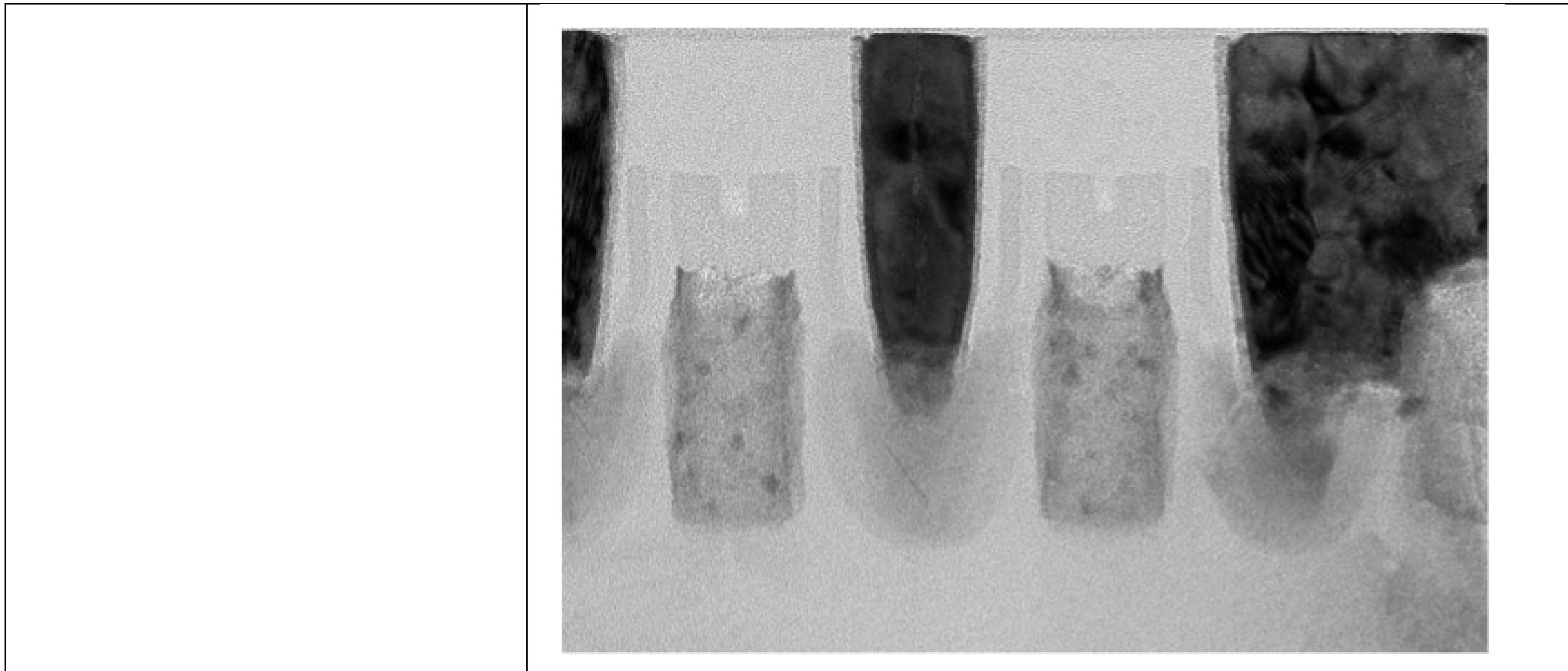
| |  |