IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

POLARIS INNOVATIONS LIMITED, an Ireland limited company Plaintiff, v. BROADCOM, INC., Defendant.	§ § § § § § § § § § §	CIVIL ACTION NO. 2:22-cv-347 **JURY TRIAL DEMANDED**

PLAINTIFF'S COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Polaris Innovations Limited ("Polaris") files this Complaint against Defendant Broadcom, Inc. ("Broadcom") for infringement of U.S. Patent No. 6,157,589 (the "'589 Patent"), U.S. Patent No. 6,794,894 (the "'894 Patent"), U.S. Patent No. 6,809,914 (the "'914 Patent"), U.S. Patent No. 8,161,344 (the "'344 Patent"), and U.S. Patent No. 8,207,976 (the "'976 Patent")r, collectively the "Asserted Patents."

THE PARTIES

1. Plaintiff Polaris Innovations Limited is a corporation organized and existing under the laws of Ireland, with its principal place of business at 77 Lower Camden Street, Dublin D02 XE80, Ireland.

2. On information and belief, Broadcom, Inc. is a corporation organized under the laws of Delaware with a regular and established place of business at 5465 Legacy Drive, Plano, TX 75024. Broadcom is a is a global infrastructure technology company providing semiconductor and infrastructure software solutions. Broadcom conducts business in Texas and in the Eastern District of Texas, directly or through intermediaries (including subsidiaries, distributors, affiliates,

retailers, suppliers, integrators, customers, and others). Broadcom has appointed Corporation Service Company d/b/a CSC-Lawyers Incorporating Service Company, located at 211 E. 7th St., Suite 620, Austin, TX 78701, as its agent for service of process.

3. Broadcom is engaged in making, using, selling, offering for sale, and/or importing products, such as semiconductors, integrated circuits, processors, controllers, and systems-on-a-chip SoCs, to and throughout the United States, including this District. Broadcom also induces its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, and customers in the making, using, selling, offering for sale, and/or importing such products to and throughout the United States, including this District.

JURISDICTION AND VENUE

4. This is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. §§ 1, *et seq*. This Court has jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and 1338(a) and 1367.

5. This Court has specific and personal jurisdiction over Broadcom consistent with the requirements of the Due Process Clause of the United States Constitution and the Texas Long Arm Statute because, *inter alia*, (i) Broadcom has done and continues to do business in Texas, and (ii) Broadcom has committed and continues to commit, directly or through intermediaries (including subsidiaries, distributors, affiliates, retailers, suppliers, integrators, customers, and others), acts of patent infringement in this State. Such acts of infringement include making, using, offering to sell, and/or selling Accused Products (as more particularly identified and described throughout this Complaint, below) in this State and this District and/or importing Accused Products into this State and/or inducing others to commit acts of patent infringement in this State. Indeed, Broadcom has purposefully and voluntarily placed, and is continuing to place, one or more

Accused Products into the stream of commerce through established distribution channels (including the Internet) with the expectation and intent that such products will be sold to and purchased by consumers in the United States, this State, and this District; and with the knowledge and expectation that such products (whether in standalone form or as integrated in downstream products) will be imported into the United States, this State, and this District.

6. Broadcom has derived substantial revenues from its infringing acts occurring within this State and this District. It has substantial business in this State and this District, including: (i) at least part of its infringing activities alleged herein; and (ii) regularly doing or soliciting business, engaging in other persistent conduct, and/or deriving substantial revenue from infringing goods offered for sale, sold, and imported, and services provided to Texas residents vicariously through and/or in concert with its alter egos, intermediaries, agents, distributors, importers, customers, subsidiaries, and/or consumers.

7. This Court has personal jurisdiction over Broadcom, Broadcom regularly conducts business and has committed acts of patent infringement and/or has induced acts of patent infringement by others in this District and/or has contributed to patent infringement by others in this District, the State of Texas, and elsewhere in the United States. Further, this Court has personal jurisdiction over Broadcom through intermediaries (including subsidiaries, distributors, affiliates, retailers, suppliers, integrators, customers, and others). Through direction and control of such intermediaries, Broadcom has committed acts of direct and/or indirect patent infringement within this State and elsewhere within the United States giving rise to this action and/or has established minimum contacts with this forum such that the exercise of personal jurisdiction over Broadcom would not offend traditional notions of fair play and substantial justice.

8. In addition, Broadcom has knowingly induced, and continues to knowingly induce, infringement within this District by advertising, marketing, offering for sale and/or selling Accused Products (such as semiconductors, integrated circuits, controllers, processors, and SoCs) that incorporate the fundamental technologies covered by the Asserted Patents. Such advertising, marketing, offering for sale and/or selling of Accused Products is directed to consumers, customers, manufacturers, integrators, suppliers, distributors, resellers, partners, and/or end users, and this includes providing instructions, user manuals, advertising, and/or marketing materials facilitating, directing and/or encouraging use of infringing functionality with Broadcom's knowledge thereof.

9. Broadcom has, thus, in the multitude of ways described above, availed itself of the benefits and privileges of conducting business in this State and willingly subjected itself to the exercise of this Court's personal jurisdiction over it. Indeed, Broadcom has sufficient minimum contacts with this forum through its transaction of substantial business in this State and this District and its commission of acts of patent infringement as alleged in this Complaint that are purposefully directed towards this State and District.

10. Venue is proper in this district for Broadcom Inc. pursuant to 28 U.S.C. § 1400(b). Broadcom Inc. has committed and continues to commit acts of patent infringement in this District, including making, using, offering to sell, and/or selling accused products in this District, and/or importing accused products into this District, including by Internet sales and sales via retail and wholesale stores, inducing others to commit acts of patent infringement in Texas, and/or committing at least a portion of any other infringements alleged herein in this District. Broadcom Inc. has a regular and established places of business in this district, including at least at 5465 Legacy Drive, Plano, Texas 75024.

THE ASSERTED PATENTS

11. Polaris is the sole and exclusive owner of all right, title, and interest in the '589 Patent, '894 Patent, '914 Patent, '344 Patent, and '976 Patent and holds the exclusive right to take all actions necessary to enforce its rights in, and to, the Asserted Patents, including the filing of this patent infringement lawsuit. Polaris also has the right to recover all damages for past, present, and future infringements of the Asserted Patents and to seek injunctive relief as appropriate under the law.

12. The '589 Patent is titled "Dynamic Semiconductor Memory Device And Method For Initializing A Dynamic Semiconductor Memory Device." The '589 Patent lawfully issued on December 5, 2000, and stems from U.S. Patent Application No. 09/343,431, which was filed on June 30, 1999.

13. The '894 Patent is titled "Method And System For Bidirectional Signal Transmission." The '894 Patent lawfully issued on September 21, 2004, and stems from U.S. Patent Application No. 10/178,252, which was filed on June 24, 2002.

14. The '914 Patent is titled "Use of DQ Pins On A RAM Memory Chip For A Temperature Sensing Protocol." The '914 Patent lawfully issued on October 26, 2004, and stems from U.S. Patent Application No. 10/144,579, which was filed on May 13, 2002.

15. The '344 Patent is titled "Circuits and Methods for Error Coding Data Blocks." The '344 Patent lawfully issued on April 17, 2012, and stems from U.S. Patent Application No. 12/046,099, which was filed on March 11, 2008.

16. The '976 Patent is titled "Circuit." The '976 Patent lawfully issued on June 26, 2012, and stems from U.S. Patent Application No. 11/726,401, which was filed on March 21, 2007.

17. Polaris and its predecessors complied with the requirements of 35 U.S.C. § 287, to the extent necessary, such that Polaris may recover pre-suit damages.

18. The claims of the Asserted Patents are directed to patent eligible subject matter under 35 U.S.C. § 101. They are not directed to an abstract idea, and the technologies covered by the claims comprise devices, systems and/or consist of ordered combinations of features and functions that, at the time of invention, were not, alone or in combination, well-understood, routine, or conventional.

DEFENDANT'S PRE-SUIT KNOWLEDGE OF ITS INFRINGEMENT

19. Prior to the filing of the Complaint, Polaris repeatedly attempted to engage Broadcom and/or its agents in licensing discussions related to the Asserted Patents:

20. On October 23, 2017, Polaris sent its first letter to Broadcom headquarters addressed to Mr. Mark Brazeal (Broadcom's Chief Legal Officer) to initiate patent licensing discussions. The letter identified certain Asserted Patents and exemplary claims as being infringed by exemplary Broadcom products.

21. On November 9, 2017, Broadcom's Senior IP Counsel acknowledged Polaris's letter and stated that "We are evaluating the issues raised in your letter and will be in touch." Broadcom's Senior IP Counsel later indicated that Broadcom was unable to meet with Polaris and did not respond to subsequent follow-up emails from Polaris.

22. Prior to filing this suit, Polaris sent Broadcom another letter via FedEx and email identifying some of its patents, including those asserted here, and attaching claim charts providing examples of Broadcom's infringement.

23. The Accused Products include, but are not limited to, the Exemplary Products identified in Polaris's letter to Broadcom. Broadcom's past and continuing sales of the Accused Products (i) willfully infringe the Asserted Patents, and (ii) impermissibly usurp the significant benefits of Polaris's patented technologies without fairly compensating Polaris.

COUNT I

(INFRINGEMENT OF U.S. PATENT NO. 6,157,589)

24. Plaintiff incorporates the preceding paragraphs herein by reference.

25. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

26. Polaris is the owner of all substantial rights, title, and interest in and to the '589 Patent including the right to exclude others and to enforce, sue, and recover damages for past infringements.

27. The '589 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on December 5, 2000, after full and fair examination.

28. Broadcom directly and/or indirectly infringed (by inducing infringement) one or more claims of the '589 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, Broadcom products, their components and processes, and/or products containing the same that incorporate the fundamental technologies covered by the '589 Patent, including, but not limited to, the Broadcom BCM63137, BCM58622, BCM4709, and BCM47189 Processors; and the SAS3324, SAS3316, SAS3108, SAS2208, SAS3516, and SAS3508 RAID-on-Chip (ROC), incorporated in the following Broadcom RAID Controller Cards SAS 9361 24i, SAS 9380 8i8e, SAS 9361 16i, SAS 9380 8e, SAS 9380 4i4e, SAS 9361 8i, SAS 9361 4i, SAS 9286 8e, SAS 9286CV 8e, SAS 9271 8i, SAS 9270 8i, SAS 9480 8i8e, SAS 9460 16i, and SAS 9460 8i (collectively, the "'589 Accused Products").

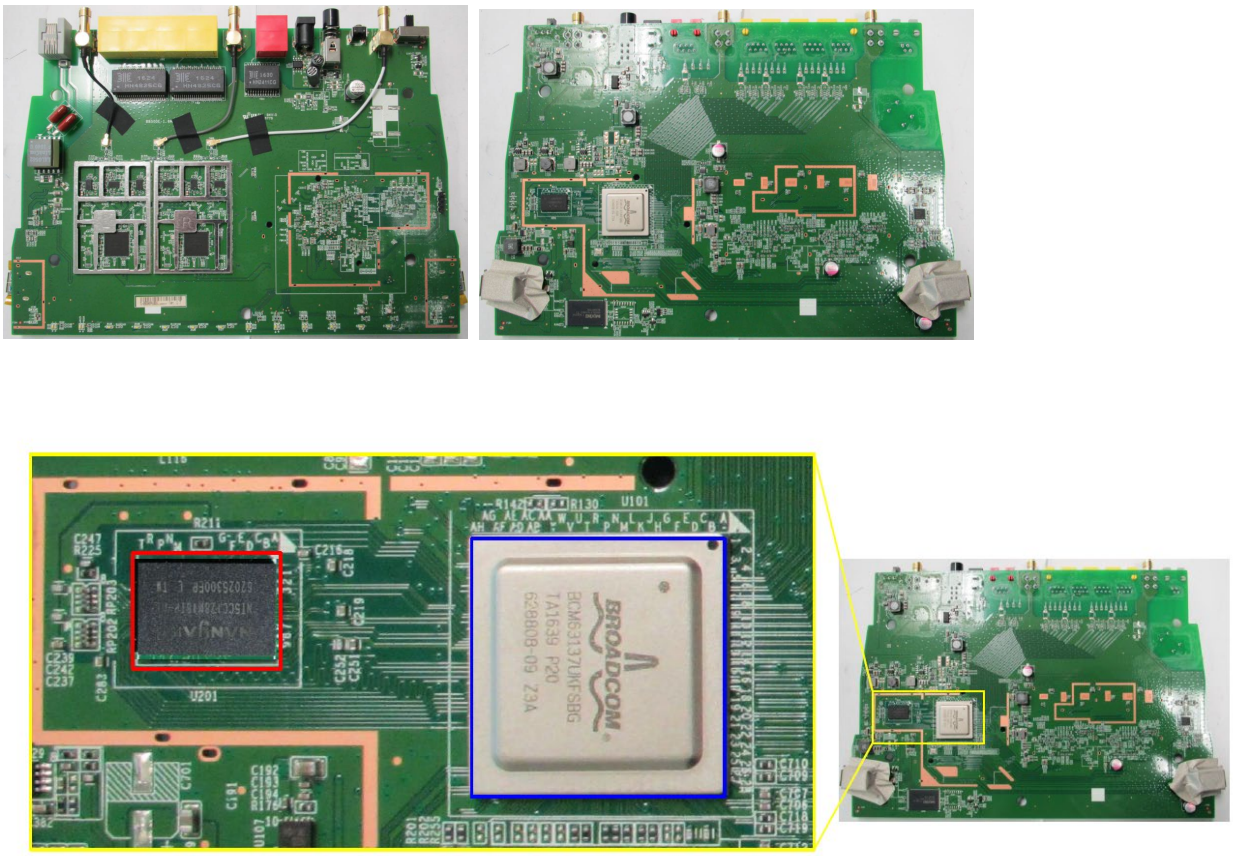
Direct Infringement (35 U.S.C. § 271(a))

29. Broadcom directly infringed one or more claims of the'589 Patent in this District and elsewhere in Texas and the United States.

30. Broadcom directly infringed, either by itself or via its agent(s), at least Claim 11 of the '589 Patent[1] as set forth under 35 U.S.C. § 271(a) by making, using, offering for sale, selling, and/or importing the '589 Accused Products. Furthermore, Broadcom made and sold the '589 Accused Products outside of the United States and either delivered those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivered the '589 Accused Products outside of the United States, it did so intending and/or knowing that those products were destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the '589 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013).

31. By way of illustration only, the '589 Accused Products perform each and every element of claim 11 of the '589 Patent. The '589 Accused Products perform "[a]n improved method for initializing a dynamic semiconductor memory device of a random access type via an initialization circuit controlling a switching on operation of the dynamic semiconductor memory device and of its circuit components." For example, the '589 Accused Products initialize a dynamic semiconductor memory device of a random access type via an initialization circuit, such as the BCM63137 Processor used in the Netgear D7000 WiFi VDSL/ADSL Modem Router shown in part below:

[1] Throughout this Complaint, wherever Polaris identifies specific claims of the Asserted Patents infringed by Broadcom, Polaris expressly reserves the right to identify additional claims and products in its infringement contentions in accordance with applicable local rules and the Court's case management orders. Specifically identified claims throughout this Complaint are provided for notice pleading only.



NetgearD7000 WiFiVDSL/ADSL Modem Router Mainboard Photograph

32. For example, the Simplified State Diagram for SDRAM, such as that included with the Broadcom BCM63137 on the Netgear D7000 is as follows:

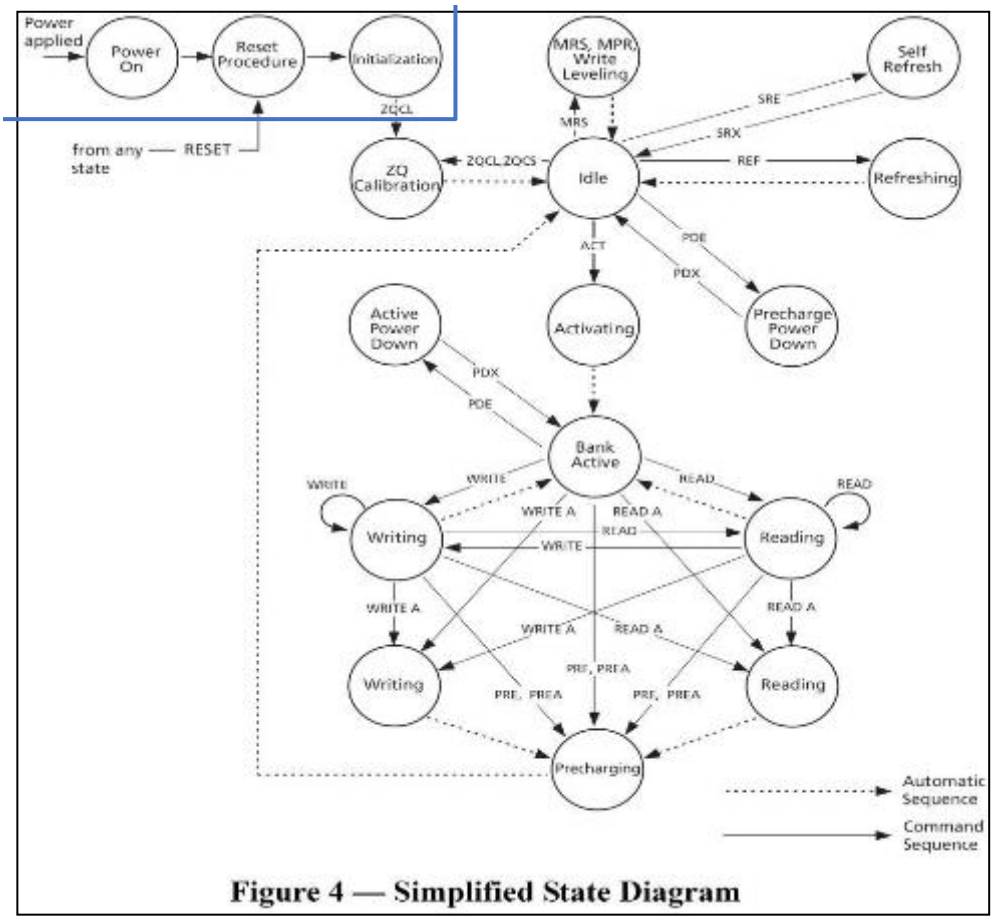


Figure 4 — Simplified State Diagram

Source: JEDEC DDR3 SDRAM Standard JESD79-3F, July 2012

33. The '589 Accused Products supply, "via the initialization circuit, a supply voltage stable signal once a supply voltage has been stabilized after the switching on operation of the dynamic semiconductor memory device." For example, the Broadcom BCM63137 in the Netgear D7000 supplies a supply voltage stable signal to the SDRAM:

Table 1 — Input/output functional description

Symbol	Type	Function
CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#.
CKE, (CKE0), (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK#, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS#, (CS0#), (CS1#), (CS2#), (CS3#)	Input	Chip Select: All commands are masked when CS# is registered HIGH. CS# provides for external Rank selection on systems with multiple Ranks. CS# is considered part of the command code.
ODT, (ODT0), (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, DQS# and DM/TDQS, NU/TDQS# (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x4/x8 configurations. For x16 configuration, ODT is applied to each DQ, DQSU, DQSU#, DQSL, DQSL#, DMU, and DML signal. The ODT pin will be ignored if MR1 and MR2 are programmed to disable RTT.
RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.
DM, (DMU), (DML)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/TDQS# is enabled by Mode Register A11 setting in MR1.
BA0 - BA2	Input	Bank Address Inputs: BA0 - BA2 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A15	Input	Address Inputs: Provide the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/BC# have additional functions; see below). The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC#	Input	Burst Chop: A12 / BC# is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET#	Input	Active Low Asynchronous Reset: Reset is active when RESET# is LOW, and inactive when RESET# is HIGH. RESET# must be HIGH during normal operation. RESET# is a CMOS rail-to-rail signal with DC high and low at 80% and 20% of V_{DD}, i.e., 1.20V for DC high and 0.30V for DC low.
DQ	Input / Output	Data Input/ Output: Bi-directional data bus.

Source: JEDEC DDR3 SDRAM Standard JESD79-3F, July 2012

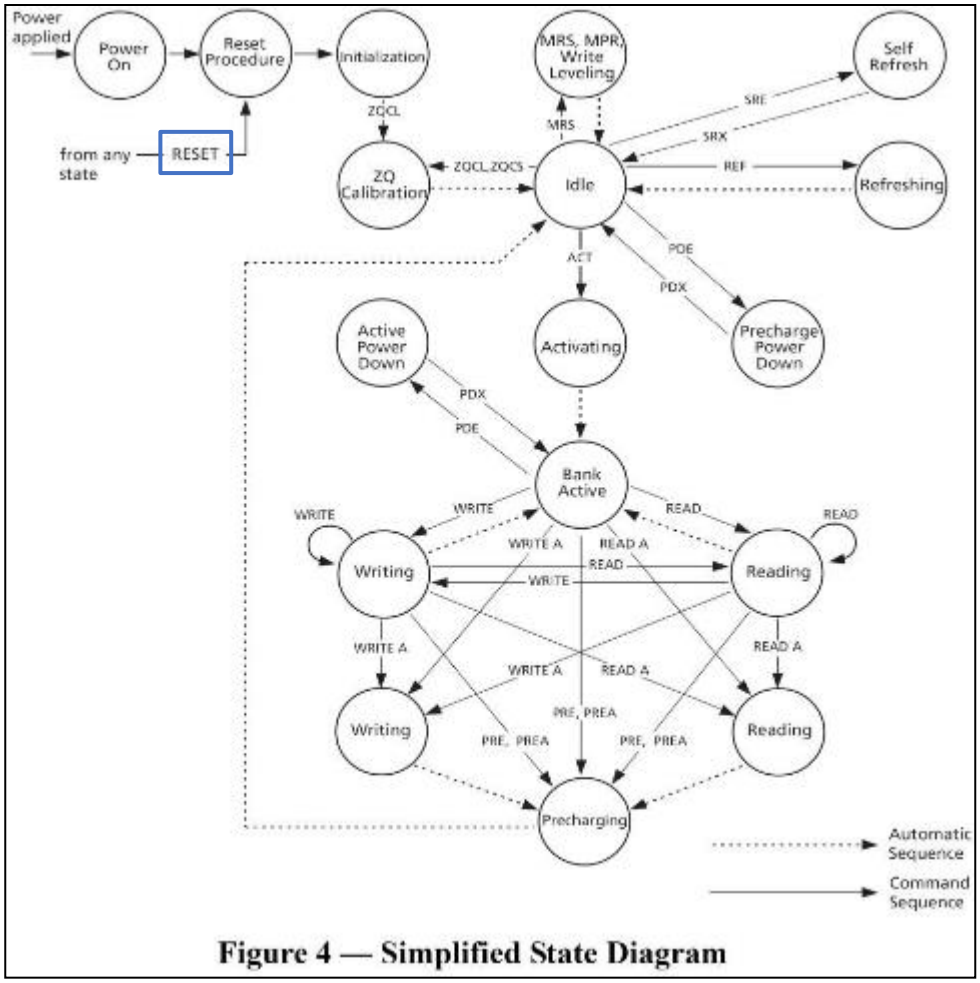


Figure 4 — Simplified State Diagram

Source: JEDEC DDR3 SDRAM Standard JESD79-3F, July 2012

34. The supply voltage stable signal is supplied once a supply voltage has been stabilized:

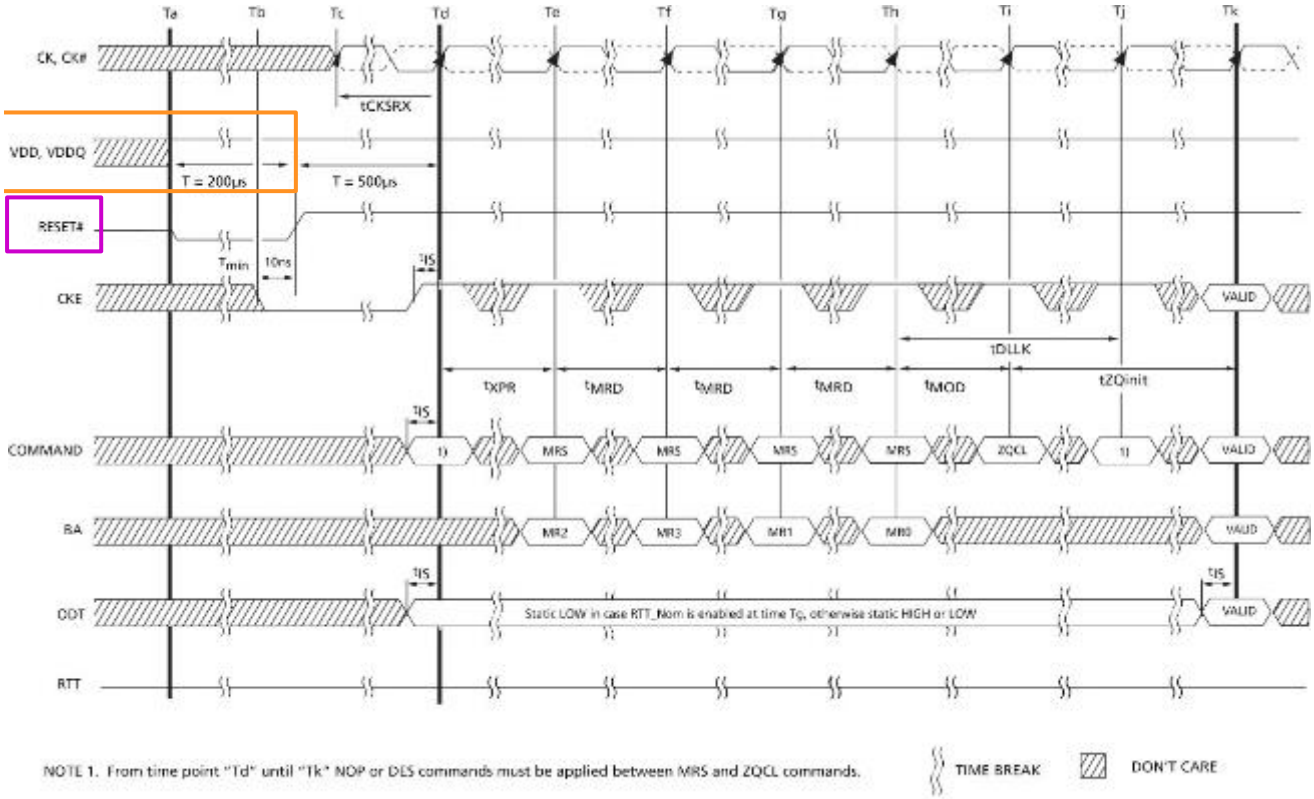


Figure 5 — Reset and Initialization Sequence at Power-on Ramping

Source: JEDEC DDR3 SDRAM Standard JESD79-3F, July 2012

35. The '589 Accused Products supply, "via an enable circuit of the initialization circuit, an enable signal, the initialization circuit receiving the supply voltage stable signal and further command signals externally applied to the dynamic semiconductor memory device, after an identification of a predetermined proper initialization sequence of the further command signals the enable signal being generated and effecting an unlatching of a control circuit provided for a proper operation of the dynamic semiconductor memory device." For example, the Broadcom BCM63137 in the Netgear D7000 shown below provides such an enable circuit that provides an enable signal, such as the CKE Clock Enable, as outlined in the JEDEC DDR3 SDRAM Standard:

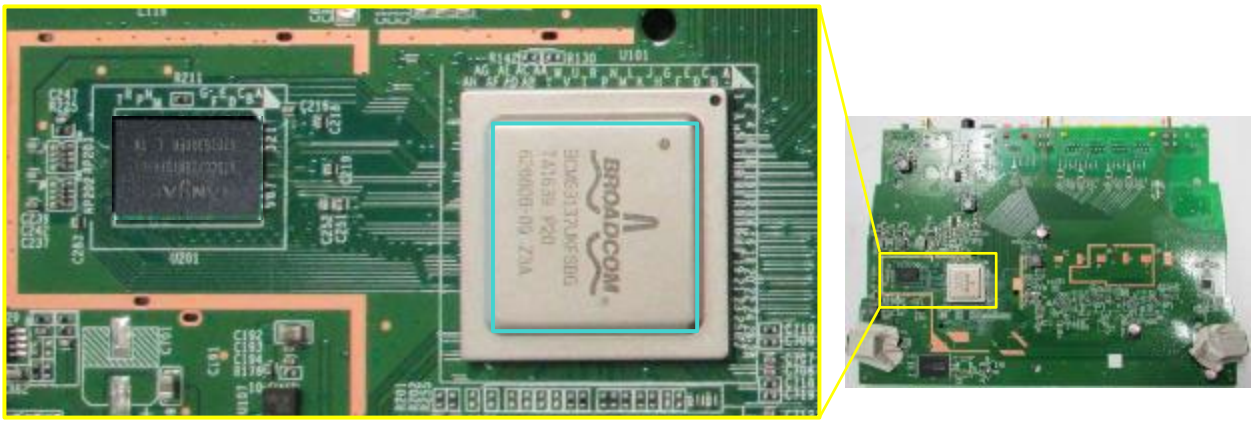


Table 1 — Input/output functional description

Symbol	Type	Function
CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#.
CKE, (CKE0), (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK#, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS#, (CS0#), (CS1#), (CS2#), (CS3#)	Input	Chip Select: All commands are masked when CS# is registered HIGH. CS# provides for external Rank selection on systems with multiple Ranks. CS# is considered part of the command code.
ODT, (ODT0), (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, DQS# and DM/TDQS, NU/TDQS# (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x4/x8 configurations. For x16 configuration, ODT is applied to each DQ, DQSU, DQSU#, DQSL, DQSL#, DMU, and DML signal. The ODT pin will be ignored if MR1 and MR2 are programmed to disable RTT.
RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.

Source: JEDEC DDR3 SDRAM Standard JESD79-3F, July 2012

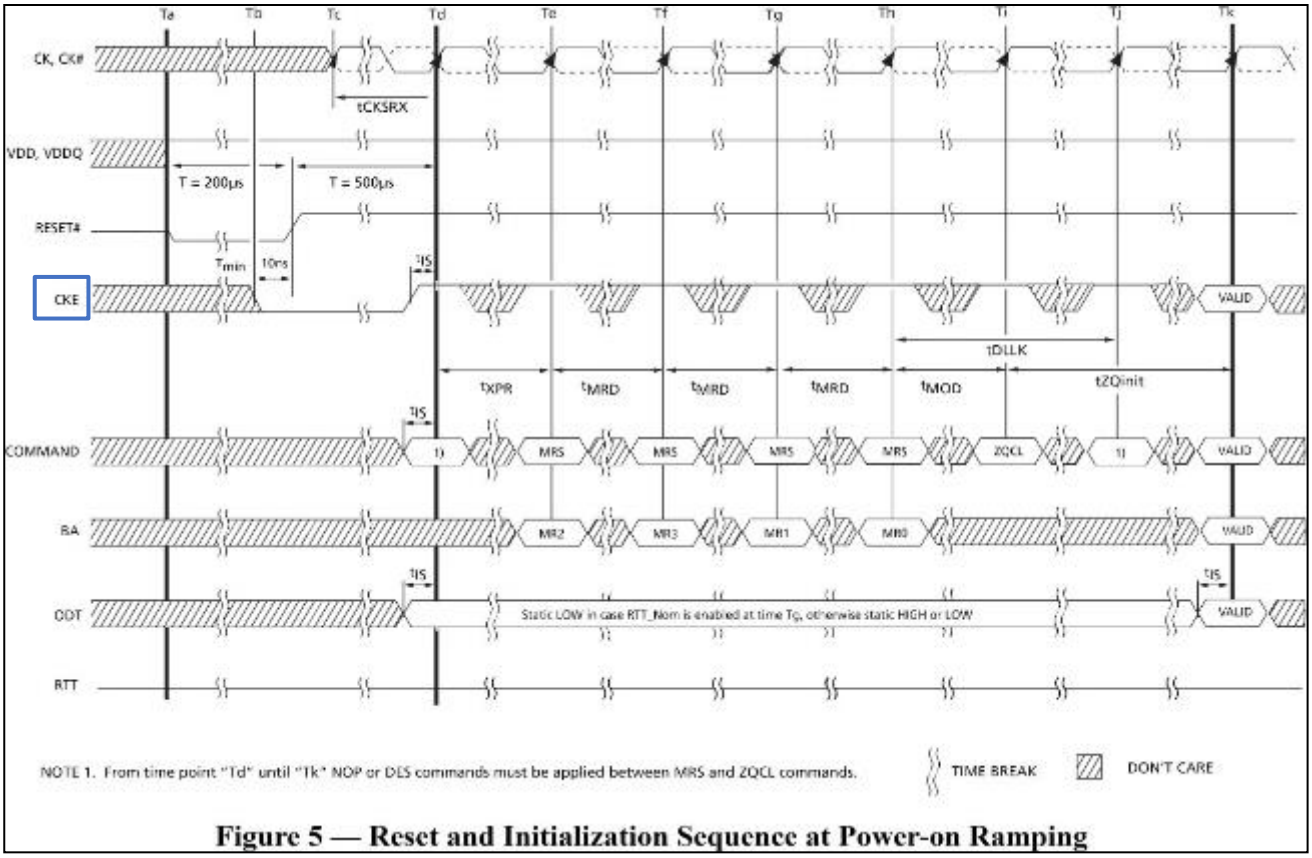


Figure 5 — Reset and Initialization Sequence at Power-on Ramping

Source: JEDEC DDR3 SDRAM Standard JESD79-3F, July 2012

36. The initialization circuit receives further command signals as indicated below:

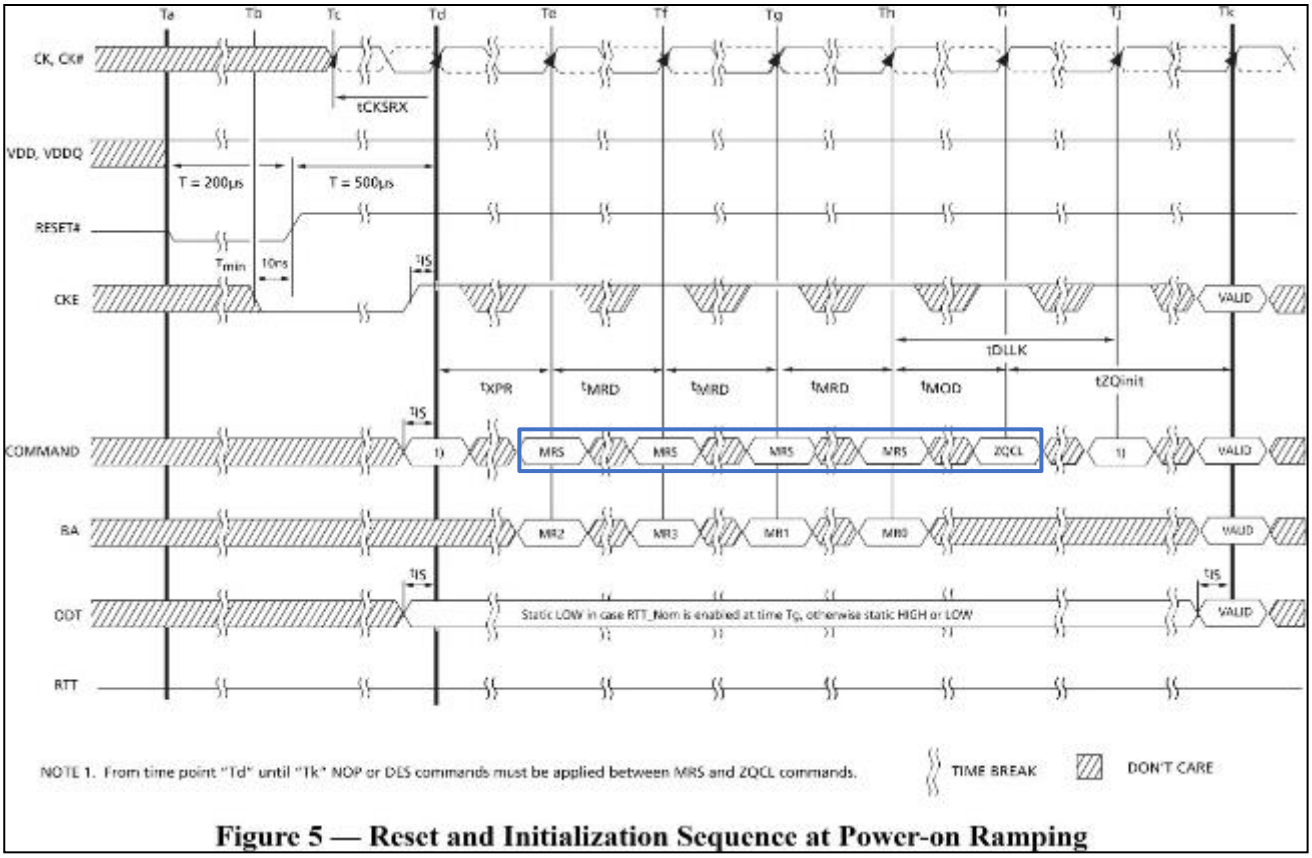


Figure 5 — Reset and Initialization Sequence at Power-on Ramping

Source: JEDEC DDR3 SDRAM Standard JESD79-3F, July 2012

37. After an identification of a predetermined proper initialization sequence of the further command signals the enable signal is generated and effects an unlatching of a control circuit provided for a proper operation of the dynamic semiconductor memory device:

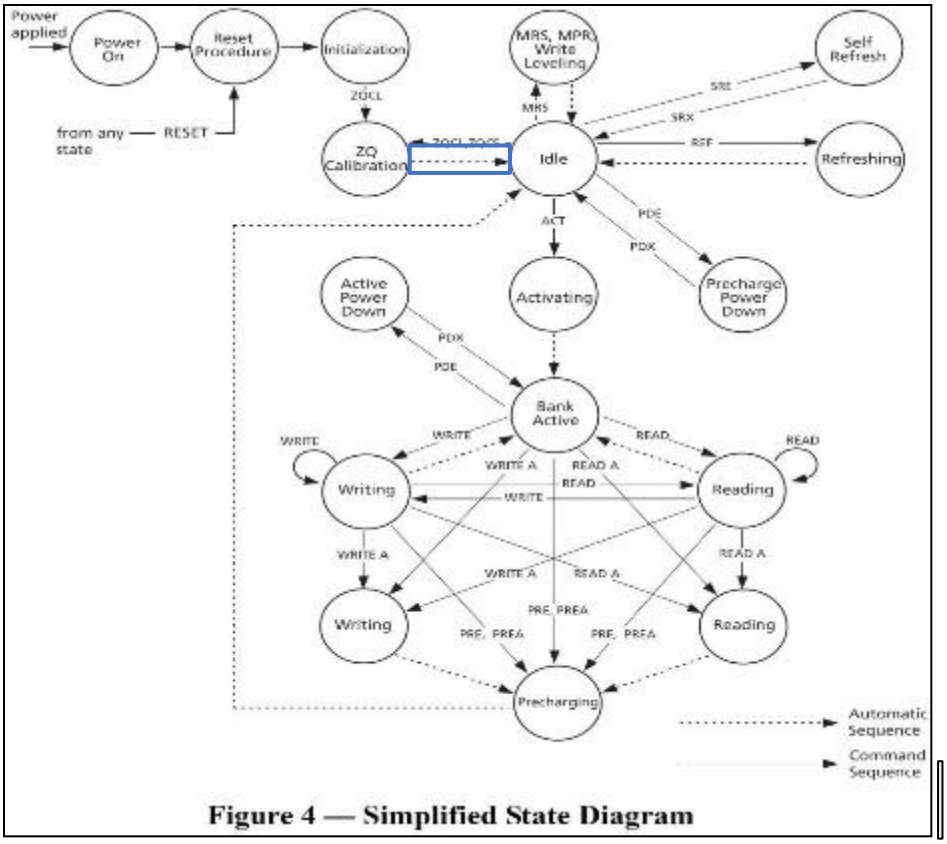


Figure 4 — Simplified State Diagram

Source: JEDEC DDR3 SDRAM Standard JESD79-3F, July 2012

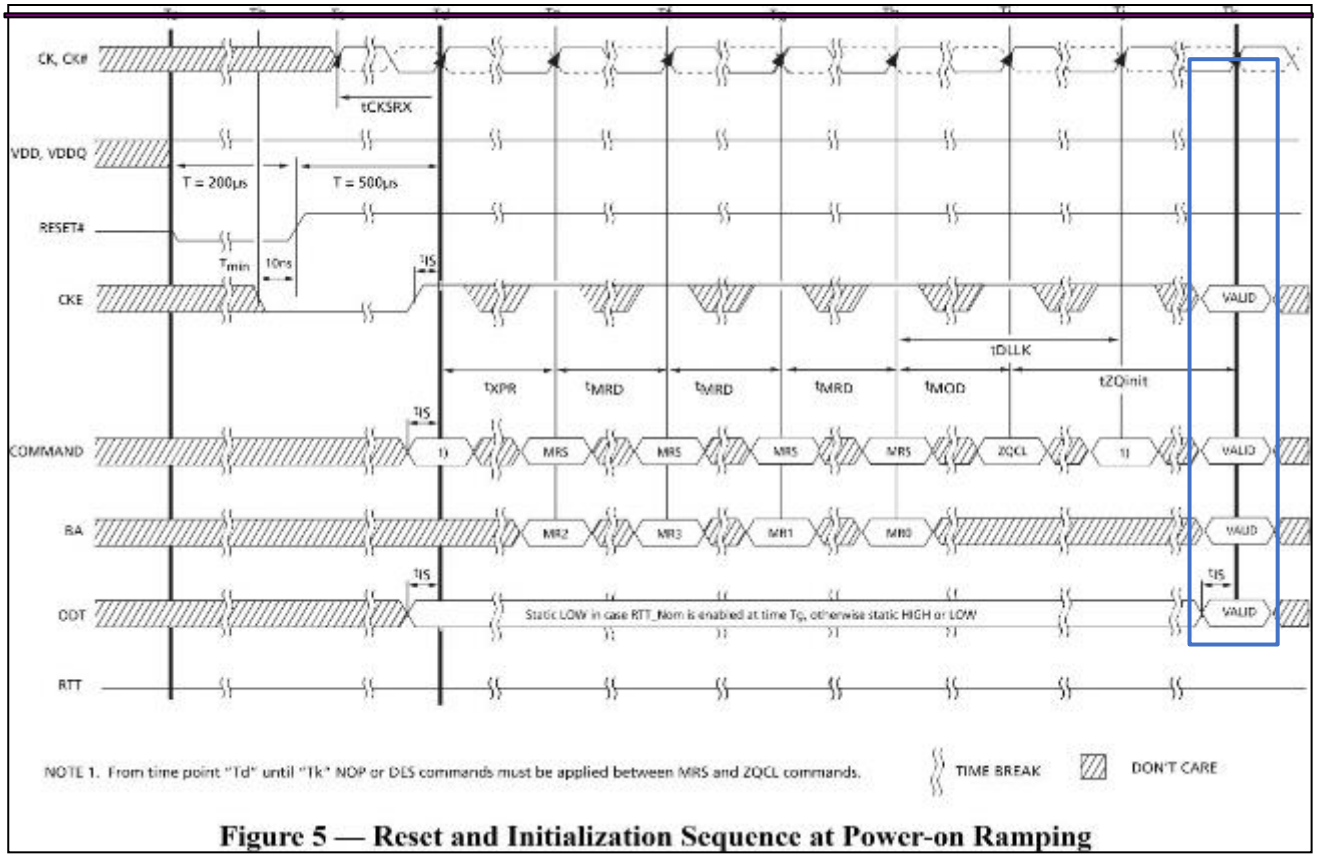


Figure 5 — Reset and Initialization Sequence at Power-on Ramping

Source: JEDEC DDR3 SDRAM Standard JESD79-3F, July 2012

Indirect Infringement (Inducement – 35 U.S.C. § 271(b))

38. In addition and/or in the alternative to its direct infringements, Broadcom has indirectly infringed one or more claims of the ’589 Patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the ’589 Accused Products.

39. At a minimum, Broadcom had knowledge of the ’589 Patent since Polaris’s October 23, 2017, letter identifying Broadcom products and the claims of the ’589 patent that they infringe. Broadcom additionally had knowledge of the ’589 Patent from Polaris’s letter and accompanying claim charts sent prior to the filing of this suit. Since receiving notice of its infringements, Broadcom actively induced the direct infringements of its subsidiaries, distributors, affiliates,

retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Such inducements have been committed with the knowledge, or with willful blindness to the fact, that the acts induced constitute infringement of the ’589 Patent. On information and belief, Broadcom intended to cause and took affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the ’589 Accused Products; creating and/or maintaining established distribution channels for the ’589 Accused Products into and within the United States; manufacturing the ’589 Accused Products in conformity with U.S. laws and regulations; distributing or making available datasheets supporting use of the ’589 Accused Products that promote their features, specifications, and applications; providing technical documentation and tools for the ’589 Accused Products, such as white papers, brochures, and/or manuals; promoting the incorporation of the ’589 Accused Products into end-user products, testing and certifying features related to initializing a dynamic semiconductor memory device of a random access in the ’589 Accused Products; and/or by providing technical support and/or related services for these products to purchasers in the United States.

Damages

40. On information and belief, despite having knowledge of the ’589 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the ’589 Patent, Broadcom has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. Broadcom’s infringing activities relative to the ’589 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, characteristic of a pirate, and an egregious case of misconduct beyond typical

infringement such that Polaris is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

41. Polaris has been damaged as a result of Broadcom's infringing conduct described in this Count. Broadcom is, thus, liable to Polaris in an amount that adequately compensates Polaris for Broadcom's infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

COUNT II

(INFRINGEMENT OF U.S. PATENT NO. 6,794,894)

42. Plaintiff incorporates the preceding paragraphs herein by reference.

43. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

44. Polaris is the owner of all substantial rights, title, and interest in and to the '894 Patent including the right to exclude others and to enforce, sue, and recover damages for past infringements.

45. The '894 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on September 21, 2004, after full and fair examination.

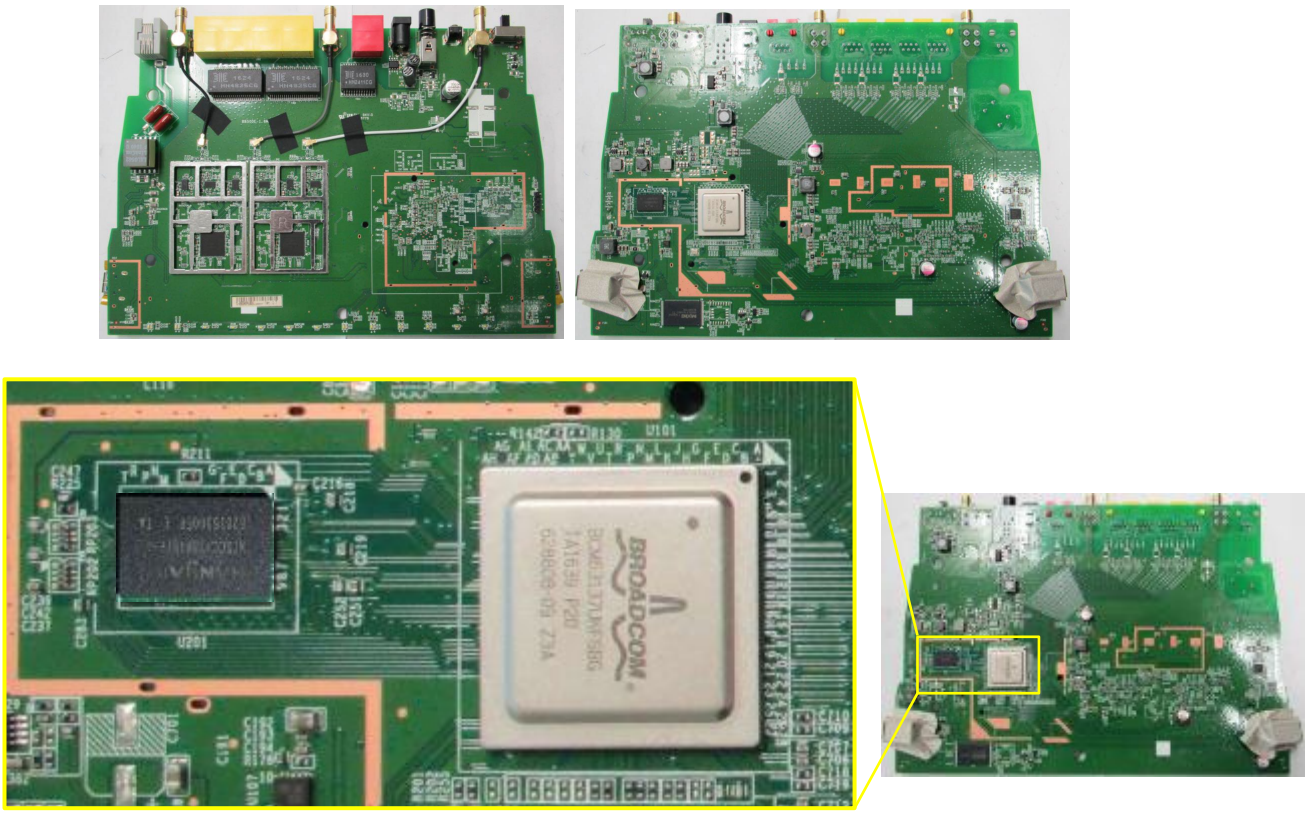
46. Broadcom directly and/or indirectly infringed (by inducing infringement) one or more claims of the '894 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, Broadcom products, their components and processes, and/or products containing the same that incorporate the fundamental technologies covered by the '894 Patent, including, but not limited to, the Broadcom BCM63137, BCM58622, BCM4709, and BCM47189 Processors (collectively, the "'894 Accused Products").

Direct Infringement (35 U.S.C. § 271(a))

47. Broadcom directly infringed one or more claims of the'894 Patent in this District and elsewhere in Texas and the United States.

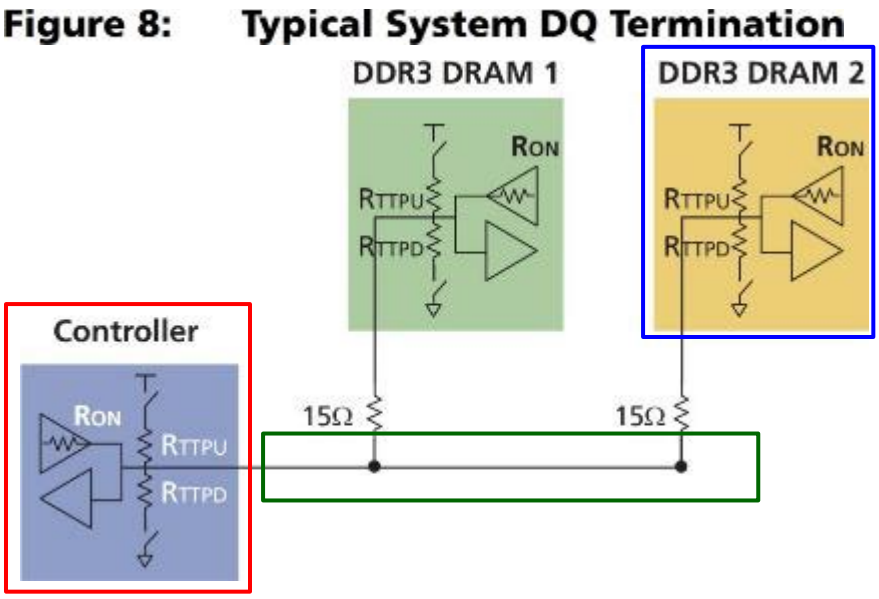
48. Broadcom directly infringed, either by itself or via its agent(s), at least Claim 1 of the '894 Patent as set forth under 35 U.S.C. § 271(a) by making, using, offering for sale, selling, and/or importing the '894 Accused Products, including by testing the '894 Accused Products in configurations as in the exemplary implementation discussed further below. Furthermore, Broadcom made and sold the '894 Accused Products outside of the United States and either delivered those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivered the '894 Accused Products outside of the United States, it did so intending and/or knowing that those products were destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the '894 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013).

49. By way of illustration only, the '894 Accused Products perform each and every element of claim 1 of the '894 Patent in conjunction with dynamic random access memory (DRAM). The '894 Accused Products "a method for bidirectional signal transmission" in conjunction with DRAM. For example, the '894 Accused Products, such as the BCM63137 Processor used in the Netgear D7000 WiFi VDSL/ADSL Modem Router shown in part below, provide bidirectional signal transmission with the associated synchronous DRAM (SDRAM):



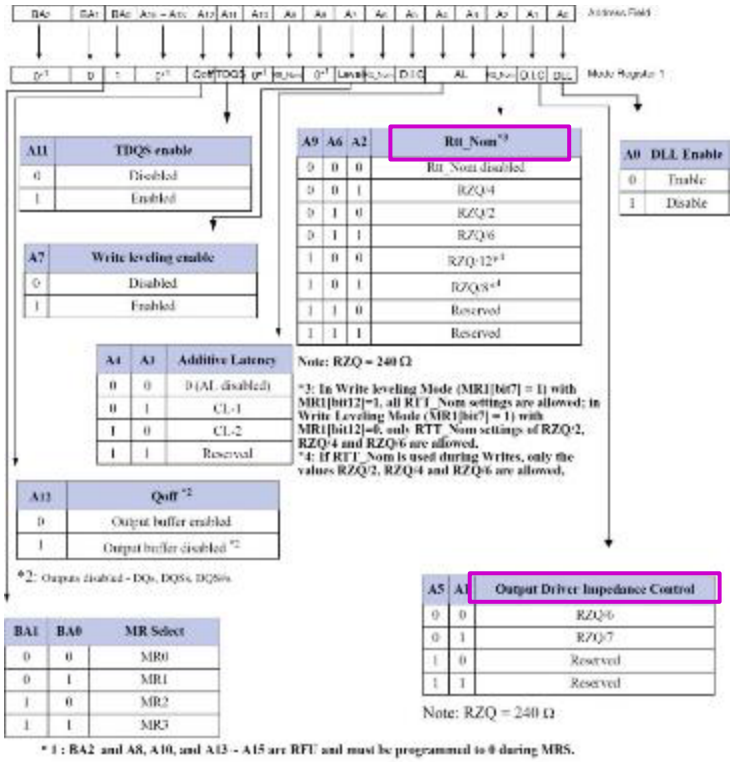
NetgearD7000 WiFiVDSL/ADSL Modem Router Mainboard Photograph

50. The '894 Accused Products and associated SDRAM provide a transmission/termination circuit configuration at a first location and a further transmission/termination circuit configuration at a second location, the transmission/termination circuit configurations being operatively connected via a common transmission line, each of the transmission/termination circuit configurations having a plurality of elements integrated in a single combined circuit configuration for switching together selectively between two functions, the functions being a transmission operating mode and a reception/termination operating mode. For example, as implemented in the Netgear D7000 WiFi VDSL/ADSL Modem Route, the BCM63137 Processor provides a transmission/termination circuit configuration at a first location and the SDRAM a further transmission/termination circuit configuration at a second location as illustrated in a typical system DQ termination block diagram:



Exemplary Circuit Block Diagram
Source: Micron Technical Note TN-41-01 "Calculating Memory System Power for DDR3", Rev. B, August 2007

51. Each of the transmission/termination circuit configurations has a plurality of elements integrated in a single combined circuit configuration for switching between two functions:



A11	TDQS enable
0	Disabled
1	Enabled

A7	Write leveling enable
0	Disabled
1	Enabled

A9	A6	A2	Rtt_Nom*3
0	0	0	Rtt_Nom disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/12*3
1	0	1	RZQ/8*4
1	1	0	Reserved
1	1	1	Reserved

A0	DLL Enable
0	Enable
1	Disable

A4	A3	Additive Latency
0	0	0 (AL disabled)
0	1	CL-1
1	0	CL-2
1	1	Reserved

Note: RZQ = 240 Ω

*3: In Write leveling Mode (MR1[bit7] = 1) with MR1[bit12]=1, all RTT_Nom settings are allowed; in Write Leveling Mode (MR1[bit7] = 1) with MR1[bit12]=0, only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.
*4: If RTT_Nom is used during Writes, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed.

A12	Qoff *2
0	Output buffer enabled
1	Output buffer disabled *2

*2: Outputs disabled - DQs, DQSs, DQSns.

A5	A1	Output Driver Impedance Control
0	0	RZQ/6
0	1	RZQ/7
1	0	Reserved
1	1	Reserved

Note: RZQ = 240 Ω

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

* 1 : BA2 and A8, A10, and A13 - A15 are RFU and must be programmed to 0 during MRS.

Figure 10 — MR1 Definition

Source: JEDEC DDR3 SDRAM Standard JESD79-3F, July 2012

52. The functions include a transmission operating mode and a reception/termination operating mode:

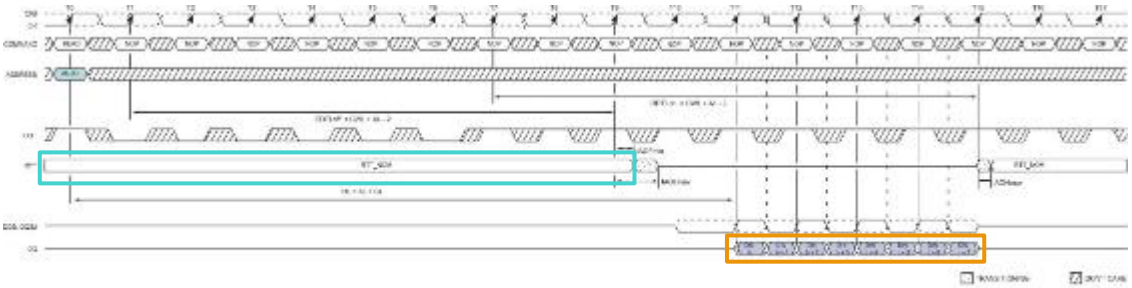


Figure 78 — ODT must be disabled externally during Reads by driving ODT low. (example: CL = 6; AL = CL - 1 = 5; RL = AL + CL = 11; CWL = 5; ODTLon = CWL + AL - 2 = 8; ODTLoff = CWL + AL - 2 = 8)

Source: JEDEC DDR3 SDRAM Standard JESD79-3F, July 2012

53. The '894 Accused Products supply a respective operating mode control signal to the transmission/termination circuit configurations in order to switch the impedance elements between the transmission operating mode and the reception/termination operating mode:

Table 1 — Input/output functional description

Symbol	Type	Function
CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#.
CKE, (CKE0), (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK#, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS#, (CS0#), (CS1#), (CS2#), (CS3#)	Input	Chip Select: All commands are masked when CS# is registered HIGH. CS# provides for external Rank selection on systems with multiple Ranks. CS# is considered part of the command code.
ODT, (ODT0), (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, DQS# and DM/TDQS, NU/TDQS# (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x4/x8 configurations. For x16 configuration, ODT is applied to each DQ, DQSU, DQSU#, DQSL, DQSL#, DMU, and DML signal. The ODT pin will be ignored if MR1 and MR2 are programmed to disable RTT.
RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.

Source: JEDEC DDR3 SDRAM Standard JESD79-3F, July 2012

54. The '894 Accused Products switch the elements of the transmission/termination circuit configurations depending on the respective operating mode control signal supplied thereto such that each of the transmission/termination circuit configurations is selectively switched to the transmission operating mode for transmitting an electrical signal via the common transmission line and to the reception/termination operating mode for forming a line termination such that an electrical signal received via the common transmission line is matched with the line termination, for example as indicated in the timing diagram for the SDRAM.

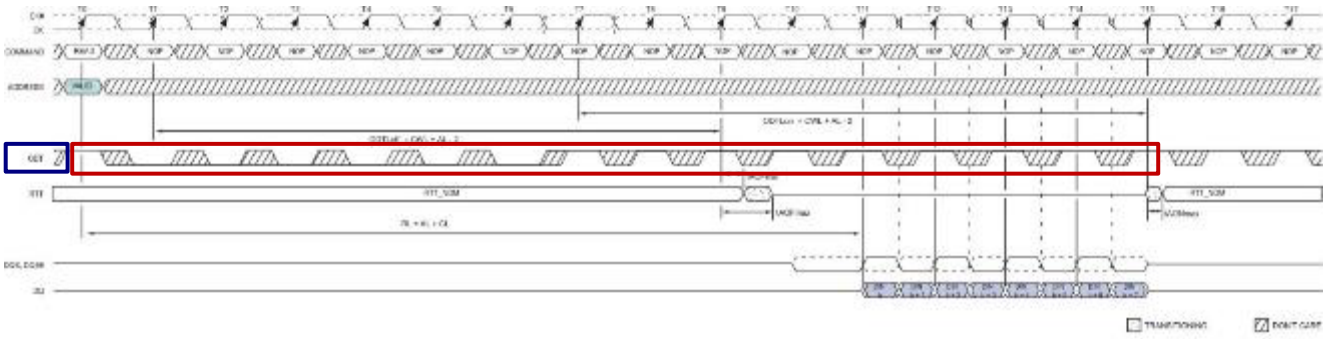


Figure 78 — ODT must be disabled externally during Reads by driving ODT low. (example: CL = 6; AL = CL - 1 = 5; RL = AL + CL = 11; CWL = 5; ODTLon = CWL + AL - 2 = 8; ODTLoff = CWL + AL - 2 = 8)

Source: JEDEC DDR3 SDRAM Standard JESD79-3F, July 2012

Indirect Infringement (Inducement – 35 U.S.C. § 271(b))

55. In addition and/or in the alternative to its direct infringements, Broadcom has indirectly infringed one or more claims of the '894 Patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the '894 Accused Products.

56. At a minimum, Broadcom had knowledge of the '894 Patent since Polaris's October 23, 2017, letter identifying Broadcom products and the claims of the '894 patent that they infringe. Broadcom additionally had knowledge of the '894 Patent from Polaris's letter and accompanying claim charts sent prior to the filing of this suit. Since receiving notice of its infringements, Broadcom actively induced the direct infringements of its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Such inducements have been committed with the knowledge, or with willful blindness to the fact, that the acts induced constitute infringement of the '894 Patent. On information and belief, Broadcom intended to cause and took affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the '894 Accused Products; creating and/or maintaining established distribution channels for the '894 Accused Products into and within the United States; manufacturing the '894 Accused Products in conformity with U.S. laws and regulations; distributing or making available datasheets supporting use of the '894 Accused Products that promote their features, specifications, and applications; providing technical documentation and tools for the '894 Accused Products, such as white papers, brochures, and/or manuals; promoting the incorporation of the '894 Accused Products into end-user products, testing and certifying features related to bidirectional signal

transmission in the '894 Accused Products; and/or by providing technical support and/or related services for these products to purchasers in the United States.

Damages

57. On information and belief, despite having knowledge of the '894 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the '894 Patent, Broadcom has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. Broadcom's infringing activities relative to the '894 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, characteristic of a pirate, and an egregious case of misconduct beyond typical infringement such that Polaris is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

58. Polaris has been damaged as a result of Broadcom's infringing conduct described in this Count. Broadcom is, thus, liable to Polaris in an amount that adequately compensates Polaris for Broadcom's infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

COUNT III

(INFRINGEMENT OF U.S. PATENT NO. 6,809,914)

59. Plaintiff incorporates the preceding paragraphs herein by reference.

60. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

61. Polaris is the owner of all substantial rights, title, and interest in and to the '914 Patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

62. The ’914 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on October 26, 2004, after full and fair examination.

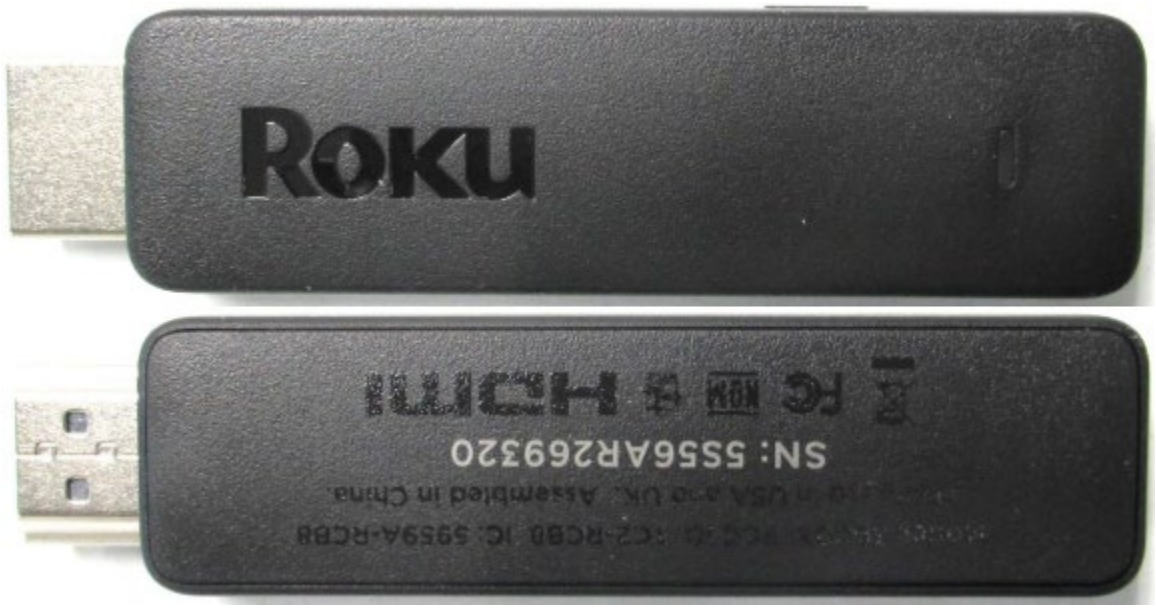
63. Broadcom has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the ’914 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, Broadcom products, their components and processes, and/or products containing the same that incorporate the fundamental technologies covered by the ’914 Patent, including, but not limited to, the Broadcom BCM2836 Processor (collectively, the “’914 Accused Products”).

Direct Infringement (35 U.S.C. § 271(a))

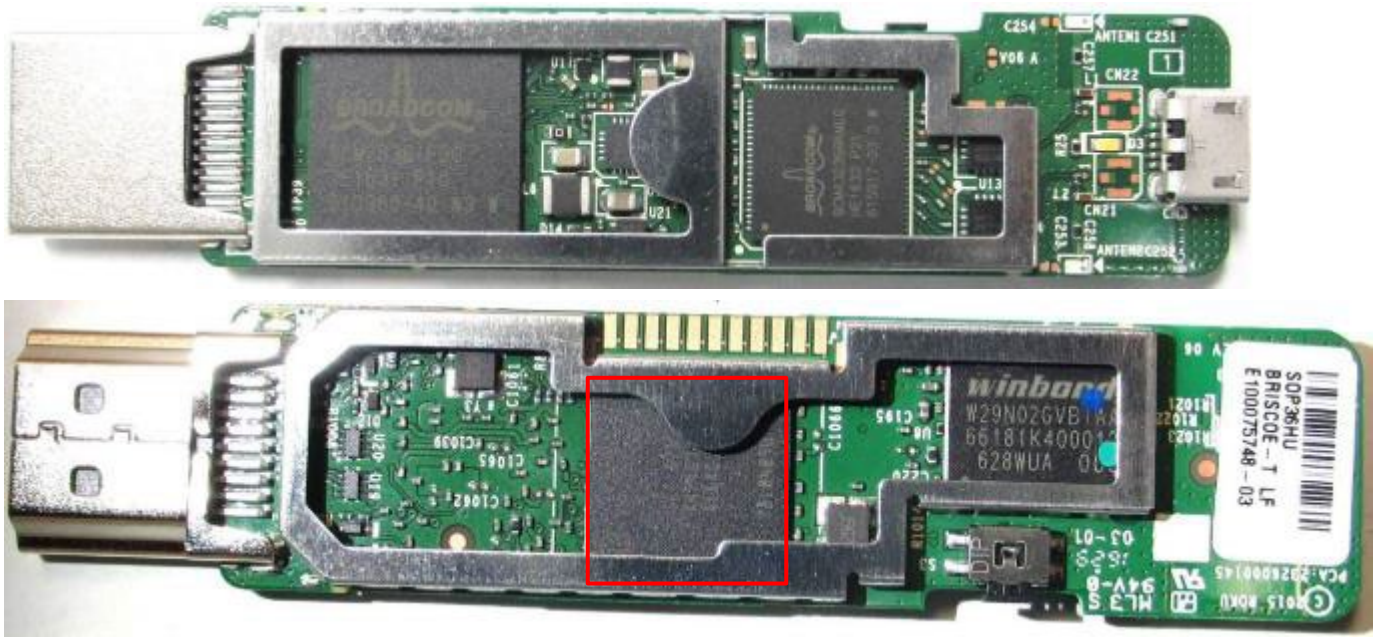
64. Broadcom has directly infringed and continues to directly infringe one or more claims of the’914 Patent in this District and elsewhere in Texas and the United States.

65. Broadcom has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 1 of the ’914 Patent as set forth under 35 U.S.C. § 271(a) by making, using, offering for sale, selling, and/or importing the ’914 Accused Products, including by testing the ’914 Accused Products in configurations as in the exemplary implementation discussed further below. Furthermore, Broadcom makes and sells the ’914 Accused Products outside of the United States and either delivers those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivers the ’914 Accused Products outside of the United States, it does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the ’914 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013).

66. By way of illustration only, the ’914 Accused Products perform each and every element of claim 1 of the ’914 Patent. The ’914 Accused Products perform “a method of protecting an integrated circuit, said integrated circuit comprising a data pin for receiving and sending input signals and output signals relating to the operation of said integrated circuit.” For example, the ’914 Accused Products protect an integrated circuit such as the Broadcom BCM2836 Processor that protects an integrated circuit in the Roku 3600R Streaming Stick shown below:



Roku 3600R



67. To the extent the preamble provides limitations, the integrated circuit protected by the Broadcom BCM2836 Processor in the Roku 3600R Streaming Stick comprises a data pin for receiving and sending input and output signals relating to the operation of the integrated circuit:

Table 2 — Pad Definition and Description

Name	Type	Description
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK_t. Single Data Rate (SDR) inputs, CS_n and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK_t and CK_c. The positive Clock edge is defined by the crosspoint of a rising CK_t and a falling CK_c. The negative Clock edge is defined by the crosspoint of a falling CK_t and a rising CK_c.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. See Command Truth Table on page 145 for command code descriptions. CKE is sampled at the positive Clock edge.
CS_n	Input	**Chip Select:** CS_n is considered part of the command code. See Command Truth Table on page 145 for command code descriptions. CS_n is sampled at the positive Clock edge.
CA0 - CA9	Input	**DDR Command/Address Inputs:** Uni-directional command/address bus inputs. CA is considered part of the command code. See Command Truth Table on page 145 for command code descriptions.
DQ0-DQ7 (x8) DQ0 - DQ15 (x16) DQ0 - DQ31 (x32)	I/O	**Data Inputs/Output:** Bi-directional data bus
DQS0_t, DQS0_c (x8) DQS0_t, DQS0_c, DQS1_t, DQS1_c (x16) DQS0_t - DQS3_t, DQS0_c - DQS3_c (x32)	I/O	**Data Strobe (Bi-directional, Differential):** The data strobe is bi-directional (used for read and write data) and differential (DQS_t and DQS_c). It is output with read data and input with write data. DQS_t is edge-aligned to read data and centered with write data. For x8, DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7. For x16, DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7; DQS1_t and DQS1_c to the data on DQ8 - DQ15. For x32 DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7, DQS1_t and DQS1_c to the data on DQ8 - DQ15, DQS2_t and DQS2_c to the data on DQ16 - DQ23, DQS3_t and DQS3_c to the data on DQ24 - DQ31.

Source: JEDEC LPDDR2 SDRAM Standard JESD209-2B, February 2010 –page 10

68. The integrated circuit protected by the Broadcom BCM2836 Processor in the Roku 3600R Streaming Stick senses a temperature of the integrated circuit and generates a temperature data signal based on the sensing:

5.12.1 Temperature Sensor

LPDDR2-SX and LPDDR2-N devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate (SDRAM), determine whether AC timing de-rating is required in the Extended Temperature Range (SDRAM and NVM), and/or monitor the operating temperature (SDRAM and NVM). Either the temperature sensor or the device TOPER (See "Operating Temperature Range" on page 158) may be used to determine whether operating temperature requirements are being met.

LPDDR2 devices shall monitor device temperature and update MR4 according to tTSI. Upon exiting self-refresh or power-down, the device temperature status bits shall be no older than tTSI.

When using the temperature sensor, the actual device case temperature may be higher than the TOPER specification (See "Operating Temperature Range" on page 158) that applies for the Standard or Extended Temperature Ranges. For example, TCASE may be above 85° C when MR4[2:0] equals 011B.

Source: JEDEC LPDDR2 SDRAM Standard JESD209-2B, February 2010 –page 126

3.5.1 Mode Register Assignment and Definition in LPDDR2 SDRAM and NVM (cont'd)

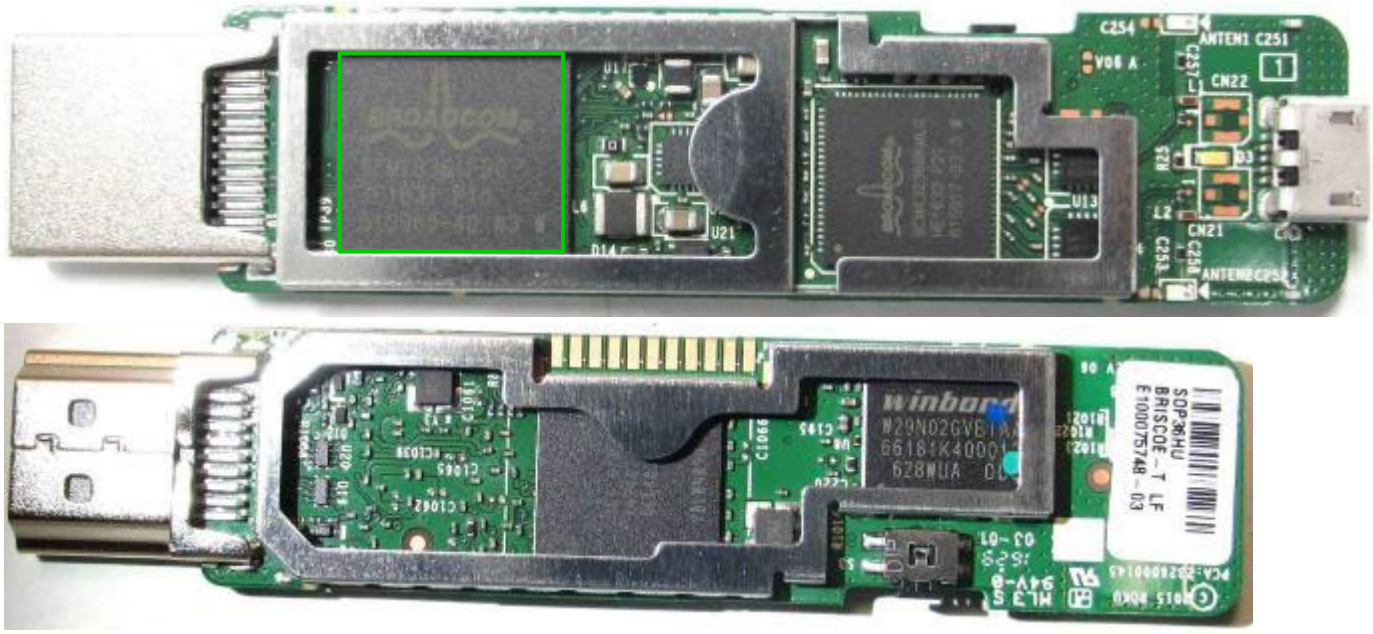
MR4_Device Temperature (MA<7:0> = 04_H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	(RFU)				SDRAM Refresh Rate		
TUF	(RFU)				NVM Temperature Alert		

SDRAM Refresh Rate	Read-only	OP<2:0>	**000_B:** SDRAM Low temperature operating limit exceeded **001_B:** 4x t_{REFI}, 4x t_{REFIpb}, 4x t_{REFW} **010_B:** 2x t_{REFI}, 2x t_{REFIpb}, 2x t_{REFW} **011_B:** 1x t_{REFI}, 1x t_{REFIpb}, 1x t_{REFW} (<=85°C) **100_B:** Reserved **101_B:** 0.25x t_{REFI}, 0.25x t_{REFIpb}, 0.25x t_{REFW}, do not de-rate SDRAM AC timing **110_B:** 0.25x t_{REFI}, 0.25x t_{REFIpb}, 0.25x t_{REFW}, de-rate SDRAM AC timing **111_B:** SDRAM High temperature operating limit exceeded
NVM Temperature Alert	Read-only	OP<2:0>	**000_B:** NVM Low temperature operating limit exceeded **001_B:** Reserved **010_B:** Reserved **011_B:** Temperature Alert not active, do not de-rate NVM AC timing (<=85°C) **100_B:** Temperature Alert not active, de-rate NVM AC timing **101_B:** Temperature Alert active, do not de-rate NVM AC timing **110_B:** Temperature Alert active, de-rate NVM AC timings **111_B:** NVM High temperature operating limit exceeded
Temperature Update Flag (TUF)	Read-only	OP<7>	**0_B:** OP<2:0> value has not changed since last read of MR4. **1_B:** OP<2:0> value has changed since last read of MR4.

Source: JEDEC LPDDR2 SDRAM Standard JESD209-2B, February 2010 –page 36

69. The ’914 Accused Products implement a temperature sensing protocol permitting supplying said temperature data signal to said data pin in addition to said input and output signals. For example, the Broadcom BCM2836 Processor in the Roku 3600R Streaming Stick implements such a protocol as outlined further below.



70. The Broadcom BCM28346 in the Roku 3600R Streaming Stick supplies the temperature data signal to the data pin of in addition to the input and output signals as specified by the integrated circuit:

5.12 Mode Register Read Command

The Mode Register Read command is used to read configuration and status data from mode registers for both NVM and SDRAM. The Mode Register Read (MRR) command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by {CA1f-CA0f, CA9r-CA4r}. The mode register contents are available on the first data beat of DQ0-DQ7, RL * t_{CK} + t_{DQSCK} + t_{DQSQ} after the rising edge of the clock where the Mode Register Read Command is issued. Subsequent data beats contain valid, but undefined content, except in the case of the DQ Calibration function DQC, where subsequent data beats contain valid content as described in "DQ Calibration" on page 127. All DQS shall be toggled for the duration of the Mode Register Read burst. The MRR command has a burst length of four. The Mode Register Read operation (consisting of the MRR command and the corresponding data traffic) shall not be interrupted. The MRR command period (t_{MRR}) is 2 clock cycles. Mode Register Reads to reserved and write-only registers shall return valid, but undefined content on all data beats and DQS shall be toggled.

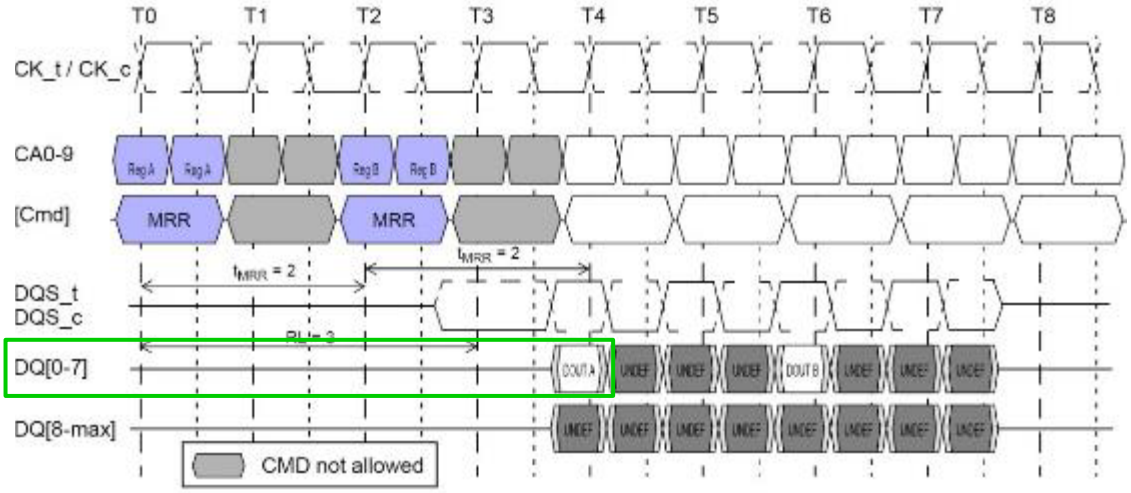
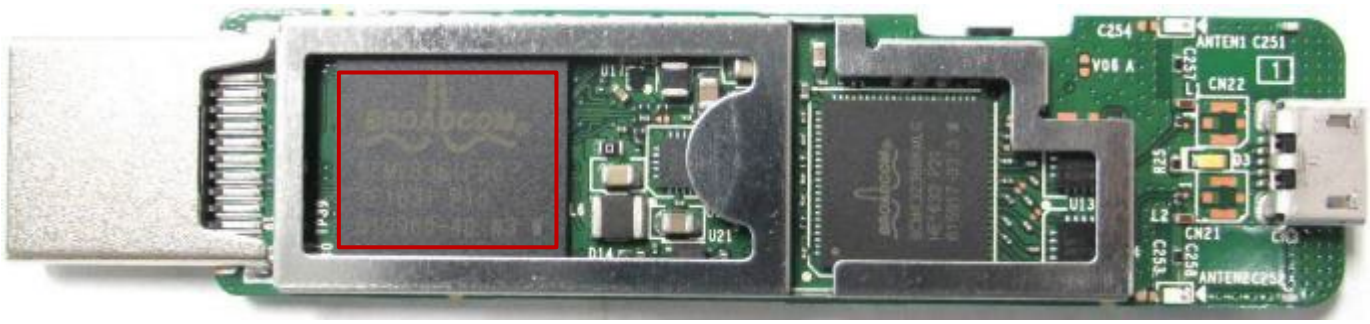
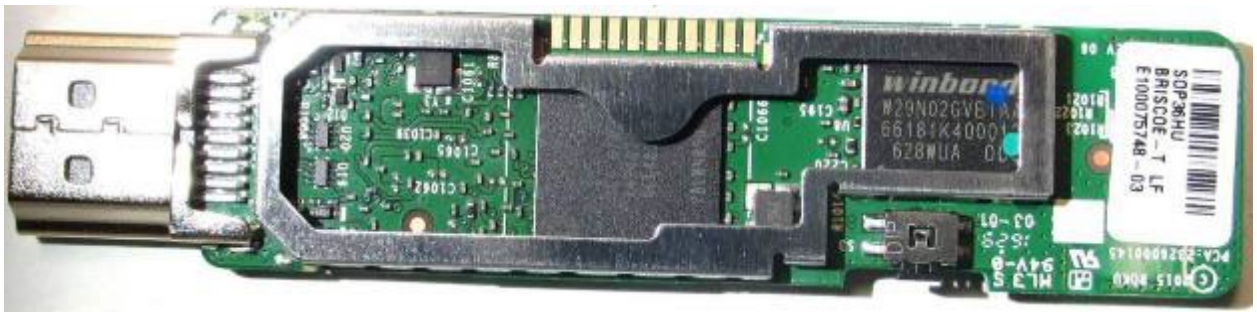


Figure 78 — Mode Register Read timing example: RL = 3, t_{MRR} = 2

Source: JEDEC LPDDR2 SDRAM Standard JESD209-2B, February 2010 –page 124

71. The '914 Accused Products, generate a command, such as for example the Broadcom BCM28346 in the Roku 3600R Streaming Stick, as part of the temperature sensing protocol:





5.12 Mode Register Read Command

The Mode Register Read command is used to read configuration and status data from mode registers for both NVM and SDRAM. The Mode Register Read (MRR) command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by {CA1f-CA0f, CA9r-CA4r}. The mode register contents are available on the first data beat of DQ0-DQ7, RL * t_{CK} + t_{DQSCK} + t_{DQSQ} after the rising edge of the clock where the Mode Register Read Command is issued. Subsequent data beats contain valid, but undefined content, except in the case of the DQ Calibration function DQC, where subsequent data beats contain valid content as described in "DQ Calibration" on page 127. All DQS shall be toggled for the duration of the Mode Register Read burst. The MRR command has a burst length of four. The Mode Register Read operation (consisting of the MRR command and the corresponding data traffic) shall not be interrupted. The MRR command period (t_{MRR}) is 2 clock cycles. Mode Register Reads to reserved and write-only registers shall return valid, but undefined content on all data beats and DQS shall be toggled.

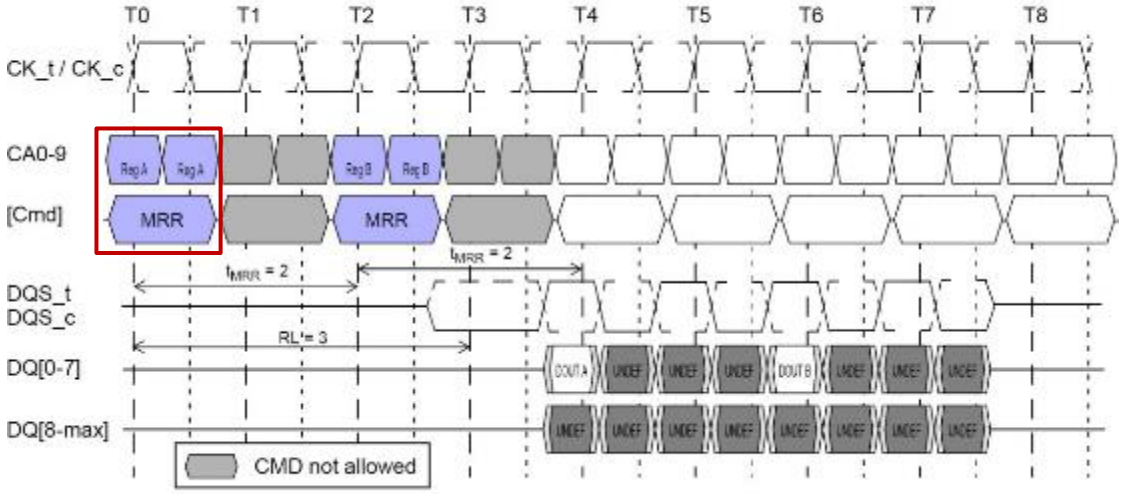


Figure 78 — Mode Register Read timing example: RL = 3, t_{MRR} = 2

Source: JEDEC LPDDR2 SDRAM Standard JESD209-2B, February 2010 –page 124

72. The '914 Accused Products place said temperature data signal on a data bus of said integrated circuit that is connected to said data pin after a time Δt as measured from a moment of discontinuation of said command, for example such as the Broadcom BCM28346 placing the

temperature data signal as indicated on the data bus of the integrated circuit in the Roku 3600R Streaming Stick, as part of the temperature sensing protocol:

5.12 Mode Register Read Command

The Mode Register Read command is used to read configuration and status data from mode registers for both NVM and SDRAM. The Mode Register Read (MRR) command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by {CA1f-CA0f, CA9r-CA4r}. The mode register contents are available on the first data beat of DQ0-DQ7, RL * t_{CK} + t_{DQSCK} + t_{DQSQ} after the rising edge of the clock where the Mode Register Read Command is issued. Subsequent data beats contain valid, but undefined content, except in the case of the DQ Calibration function DQC, where subsequent data beats contain valid content as described in "DQ Calibration" on page 127. All DQS shall be toggled for the duration of the Mode Register Read burst. The MRR command has a burst length of four. The Mode Register Read operation (consisting of the MRR command and the corresponding data traffic) shall not be interrupted. The MRR command period (t_{MRR}) is 2 clock cycles. Mode Register Reads to reserved and write-only registers shall return valid, but undefined content on all data beats and DQS shall be toggled.

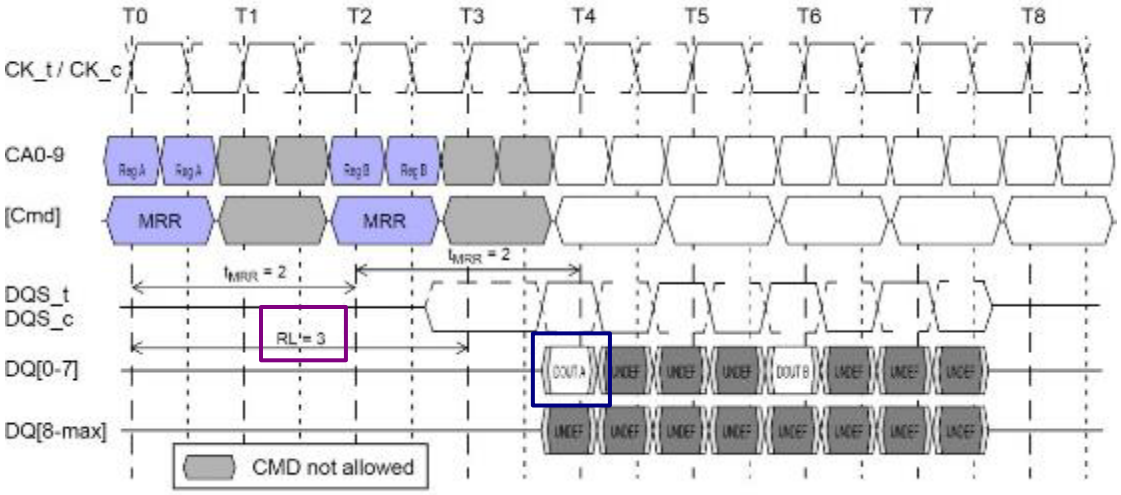


Figure 78 — Mode Register Read timing example: RL = 3, t_{MRR} = 2

Source: JEDEC LPDDR2 SDRAM Standard JESD209-2B, February 2010 –page 124

73. The '914 Accused Products supply said temperature data signal to said data pin based on said temperature sensing protocol, for example such as the Broadcom BCM28346 supplying the temperature data signal as indicated on the data bus of the integrated circuit in the Roku 3600R Streaming Stick:

5.12 Mode Register Read Command

The Mode Register Read command is used to read configuration and status data from mode registers for both NVM and SDRAM. The Mode Register Read (MRR) command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by {CA1f-CA0f, CA9r-CA4r}. The mode register contents are available on the first data beat of DQ0-DQ7, RL * t_{CK} + t_{DQSCK} + t_{DQSQ} after the rising edge of the clock where the Mode Register Read Command is issued. Subsequent data beats contain valid, but undefined content, except in the case of the DQ Calibration function DQC, where subsequent data beats contain valid content as described in "DQ Calibration" on page 127. All DQS shall be toggled for the duration of the Mode Register Read burst. The MRR command has a burst length of four. The Mode Register Read operation (consisting of the MRR command and the corresponding data traffic) shall not be interrupted. The MRR command period (t_{MRR}) is 2 clock cycles. Mode Register Reads to reserved and write-only registers shall return valid, but undefined content on all data beats and DQS shall be toggled.

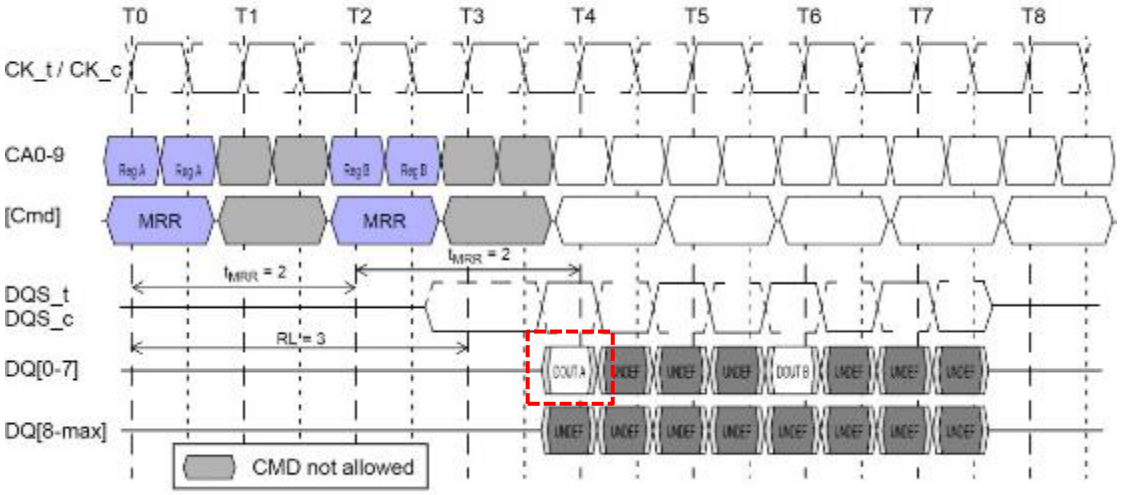


Figure 78 — Mode Register Read timing example: RL = 3, t_{MRR} = 2

Source: JEDEC LPDDR2 SDRAM Standard JESD209-2B, February 2010 –page 124

Indirect Infringement (Inducement – 35 U.S.C. § 271(b))

74. In addition and/or in the alternative to its direct infringements, Broadcom has indirectly infringed and continues to indirectly infringe one or more claims of the '914 Patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the '914 Accused Products.

75. At a minimum, Broadcom has knowledge of the '914 Patent since being served with this Complaint. Broadcom also has knowledge of the '914 Patent since Polaris's October 23,

2017, letter identifying Broadcom products and the claims of the '914 patent that they infringe. Broadcom additionally has knowledge of the '914 Patent from Polaris's letter and accompanying claim charts sent prior to the filing of this suit. Since receiving notice of its infringements, Broadcom has actively induced the direct infringements of its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Such inducements have been committed with the knowledge, or with willful blindness to the fact, that the acts induced constitute infringement of the '914 Patent. On information and belief, Broadcom has intended to cause, continues to intend to cause, and has taken, and continues to take affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the '914 Accused Products; creating and/or maintaining established distribution channels for the '914 Accused Products into and within the United States; manufacturing the '914 Accused Products in conformity with U.S. laws and regulations; distributing or making available datasheets supporting use of the '914 Accused Products that promote their features, specifications, and applications; providing technical documentation and tools for the '914 Accused Products, such as white papers, brochures, and/or manuals; promoting the incorporation of the '914 Accused Products into end-user products, testing and certifying features related to protecting an integrated circuit in the '914 Accused Products; and/or by providing technical support and/or related services for these products to purchasers in the United States.

Damages

76. On information and belief, despite having knowledge of the '914 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the '914 Patent, Broadcom has nevertheless continued its infringing conduct and disregarded an objectively high

likelihood of infringement. Broadcom's infringing activities relative to the '914 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, characteristic of a pirate, and an egregious case of misconduct beyond typical infringement such that Polaris is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

77. Polaris has been damaged as a result of Broadcom's infringing conduct described in this Count. Broadcom is, thus, liable to Polaris in an amount that adequately compensates Polaris for Broadcom's infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

COUNT IV

(INFRINGEMENT OF U.S. PATENT NO. 8,161,344)

78. Plaintiff incorporates the preceding paragraphs herein by reference.

79. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

80. Polaris is the owner of all substantial rights, title, and interest in and to the '344 Patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

81. The '344 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on April 17, 2012, after full and fair examination.

82. Broadcom has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the '344 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, Broadcom products, their components and processes, and/or products containing the same that incorporate the fundamental

technologies covered by the '344 Patent, including, but not limited to, Broadcom's GDDR6-based Products including the Broadcom BCM88480, BCM88280, BCM88800, BCM88790, BCM88690, BCM88480, and BCM88280 Processors (collectively, the "'344 Accused Products").

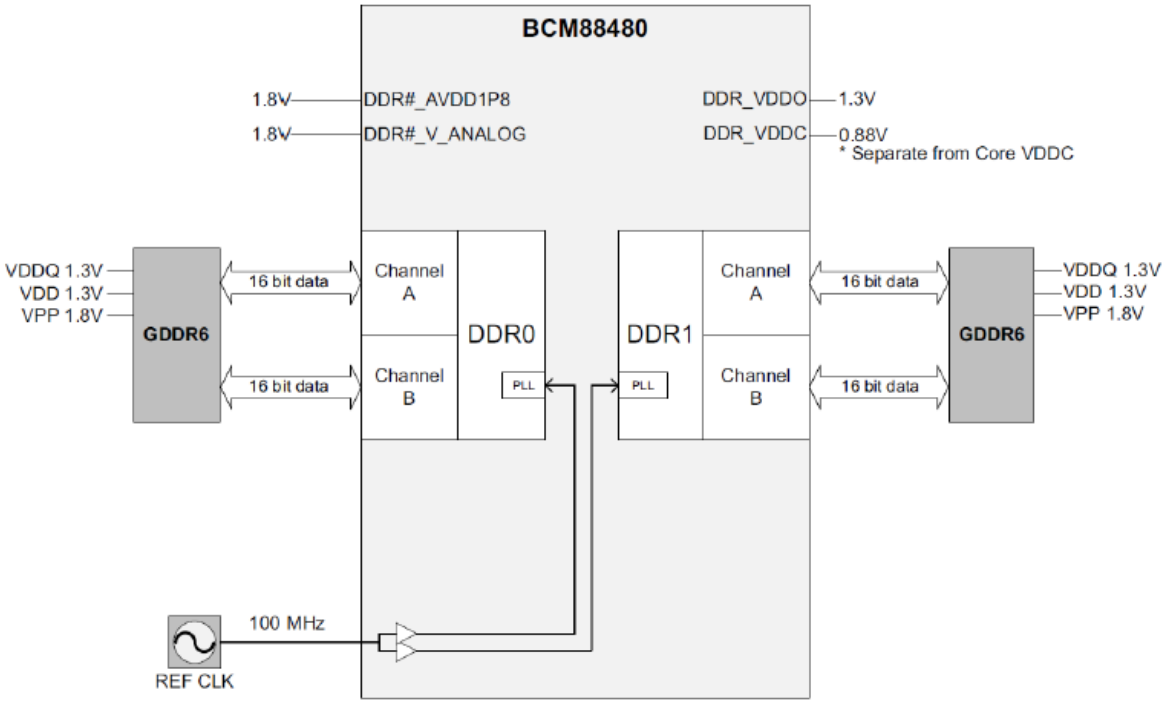
Direct Infringement (35 U.S.C. § 271(a))

83. Broadcom has directly infringed and continues to directly infringe one or more claims of the'344 Patent in this District and elsewhere in Texas and the United States.

84. Broadcom has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 2 of the '344 Patent as set forth under 35 U.S.C. § 271(a) by making, using, offering for sale, selling, and/or importing the '344 Accused Products, including by testing the '344 Accused Products in configurations as in the exemplary implementation discussed further below. Furthermore, Broadcom makes and sells the '344 Accused Products outside of the United States and either delivers those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivers the '344 Accused Products outside of the United States, it does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the '344 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013).

85. By way of illustration only, the '344 Accused Products comprise a circuit that satisfies each and every element of claim 2 of the '344 Patent. The '344 Accused Products comprise "[a] circuit for creating an error coding data block for a first data block." For example, the '344 Accused Products comprise a circuit for creating an error coding data block for a first data block, such as the BCM88480 Processor illustrated in the diagram below:

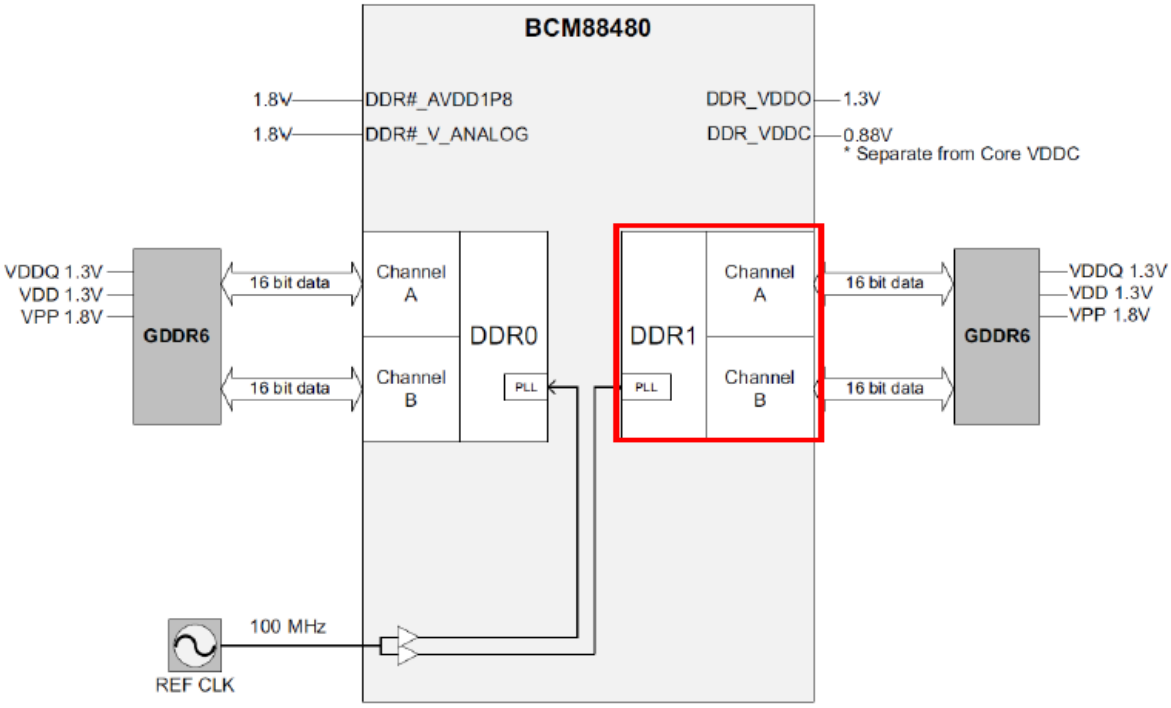
Figure 32: BCM88480 GDDR6 DRAM High-Level Blocks



Source: DNX16 Hardware Design Guidelines for StrataDNX™16-nm Devices, Broadcom, Page 64

86. The '344 Accused Products comprise a first error coding path adapted to selectively create a first error coding data block in accordance with a first error coding, for example as indicated below in the diagram of the BCM88480 and described in its Design Guide:

Figure 32: BCM88480 GDDR6 DRAM High-Level Blocks



Source: DNX16 Hardware Design Guidelines for StrataDNX™16-nm Devices, Broadcom, Page 64

6.7.1.2 DRAM-Packet-CRC

For every packet written to the DRAM, CRC16 is computed on the packet and on the FTMH. The CRC is checked for each packet when it is read from DRAM. If a CRC error occurs, the packet is still sent. There are two counters for CRC errors:

- Flipped CRC—Indicates that the error did not originate within the DRAM system; it originated in the SRAM.
- Other error—Indicates an error in the DRAM system.

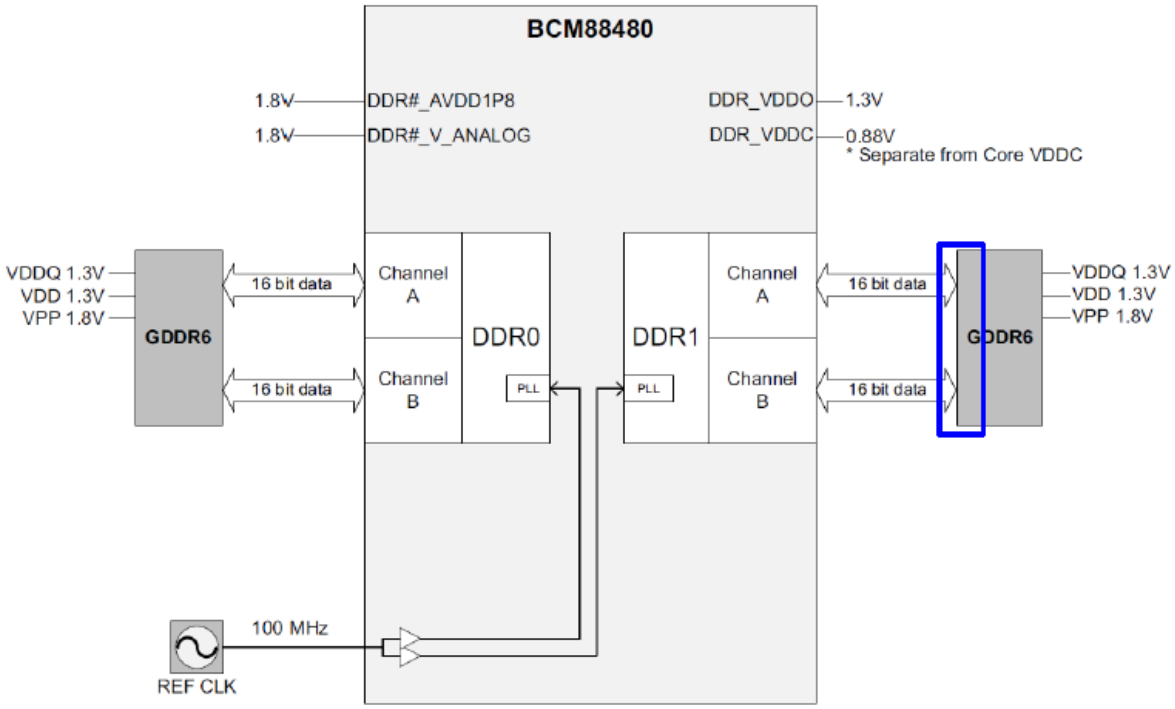
The CNI bit in the FTMH may be set after a DRAM dequeue; then the CRC is updated before the packet is sent to the fabric.

At the egress device, the packet CRC is rechecked. If the CRC within the packet is the flipped CRC, this indicates that the error originated within the ingress device; otherwise, it indicates that the error occurred within the fabric.

Source: Broadcom, BCM88480 Traffic Management Architecture Design Guide, 88480-DG105-PUB, February 19, 2021, page 30

87. The ’344 Accused Products further comprise a second error coding path adapted to selectively create a second error coding data block in accordance with a second error coding, for example as indicated below in the diagram of the BCM88480 and described in the SGRAM Standard:

Figure 32: BCM88480 GDDR6 DRAM High-Level Blocks



Source: DNX16 Hardware Design Guidelines for StrataDNX™16-nm Devices, Broadcom, Page 64

7.14 ERROR DETECTION CODE (EDC)

The GDDR6 SGRAM provides error detection on the data bus to improve system reliability. The device generates a checksum per byte lane for both READ and WRITE data and returns the checksum to the controller. GDDR6 supports 2 modes for the EDC with either a 16 bit checksum that runs at same rate as the data (Full data rate EDC) or an 8 bit checksum that runs at half the rate of the data (Half data rate EDC). Mode Register 2 OP8 selects between the 2 modes and is undefined at boot. The EDC rate register must be set during the initialization sequence after power up or after a reset.

The 16 bit checksum of the Full data rate EDC is calculated in two halves based on the 2 halves of the 16 bit burst. The first 8 bits of the checksum, CRC-L, are calculated on burst positions 0 thru 7 and the second half of the checksum, CRC-U, are calculated on burst positions 8 thru 15. The 8 bit checksum of the Half data rate EDC is calculated on the full 16bit burst using an XOR of the CRC-L and CRC-U as illustrated in Figure 90.

Based on the checksum, the controller can decide if the data (or the returned CRC) was transmitted in error and retry the READ or WRITE command. The device itself does not perform any error correction. The features of the EDC are:

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 108

88. In the '344 Accused Products, the first error coding path and the second error coding path are selected as a function of a control indicator for example as reflected in the BCM88480 Processor Design Guide and the SGRAM Standard:

6.7.1.2 DRAM-Packet-CRC

For every packet written to the DRAM, CRC16 is computed on the packet and on the FTMH. The CRC is checked for each packet when it is read from DRAM. If a CRC error occurs, the packet is still sent. There are two counters for CRC errors:

- Flipped CRC—Indicates that the error did not originate within the DRAM system; it originated in the SRAM.
- Other error—Indicates an error in the DRAM system.

Source: Broadcom, BCM88480 Traffic Management Architecture Design Guide, 88480-DG105-PUB, February 19, 2021 page 30

7.14 ERROR DETECTION CODE (EDC)

The GDDR6 SGRAM provides error detection on the data bus to improve system reliability. The device generates a checksum per byte lane for both READ and WRITE data and returns the checksum to the controller. GDDR6 supports 2 modes for the EDC with either a 16 bit checksum that runs at same rate as the data (Full data rate EDC) or an 8 bit checksum that runs at half the rate of the data (Half data rate EDC). Mode Register 2 OP8 selects between the 2 modes and is undefined at boot. The EDC rate register must be set during the initialization sequence after power up or after a reset.

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 108

89. In the '344 Accused Products, at least the first error coding path comprises a data arrangement alteration device, for example as reflected in the BCM88480 Processor Data Sheet and the SGRAM Standard:

Table 7: Pin List by Function (Continued)

Signal/Bus Name	Qty.	Type	Tech	Description
DDR0_A_DBI[1:0]_N	2	B	POD 1.3V	Data bus inversion. DBI0_N is associated with DQ[7:0]. DBI1_N is associated with DQ[15:8].
DDR0_A_EDC[1:0]	2	I	POD 1.3V	Error Detection Code from GDDR6 to controller. EDC0 is associate with DQ[7:0]. EDC1 is associate with DQ[15:8].
DDR0_A_DQ[15:00]	16	B	POD 1.3V	Data input/output.
DDR0_A_WCK[1:0]_T/C	2x2	O	POD 1.3V	Write clock differential clocks used for *write* data capture and *read* data output. WCK0_T and WCK0_C are associated with DQ[7:0], DBI0_N, and EDC0. WCK1_T and WCK1_C are associated with DQ[15:8], DBI1_N, and EDC1. For WCK per word, WCK0 is used for channel A, and WCK1 is used for channel B.

Source: Broadcom, BCM88480 Data Sheet 800-Gb/s Integrated Packet Processor and Traffic Manager Single-Chip Device, August 3, 2021, Page 50

7.14 ERROR DETECTION CODE (EDC) (cont'd)

The CRC calculation is embedded into the WRITE and READ data stream as shown in Figure 23:

- for WRITEs, the CRC checksum is calculated on the DQ and DBI_n input data before decoding with DBI
- for READs, the CRC checksum is calculated on the DQ and DBI_n output data after encoding with DBI

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 110

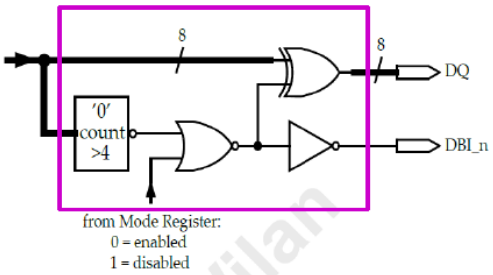


Figure 87 — Example of Data Bus Inversion Logic

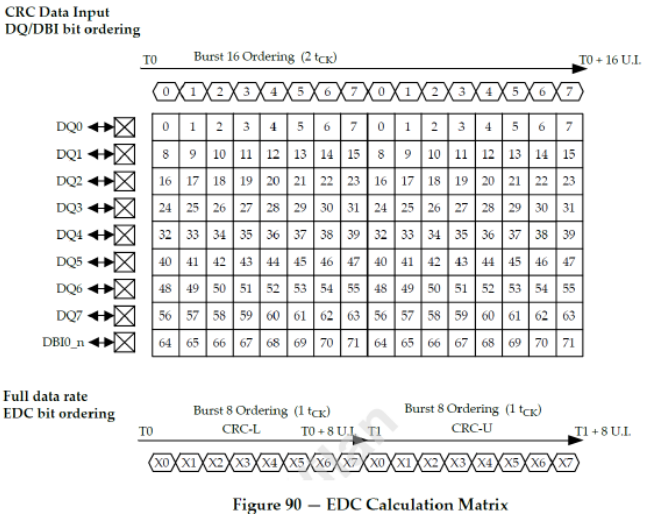


Figure 90 — EDC Calculation Matrix

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 106, 109

90. The '344 Accused Products further comprise a circuit wherein the first error coding path and the second error coding path are adapted to perform the same data arrangement alteration algorithm for the first and second error codings, for example as shown in the diagram below from the SGRAM Standard:

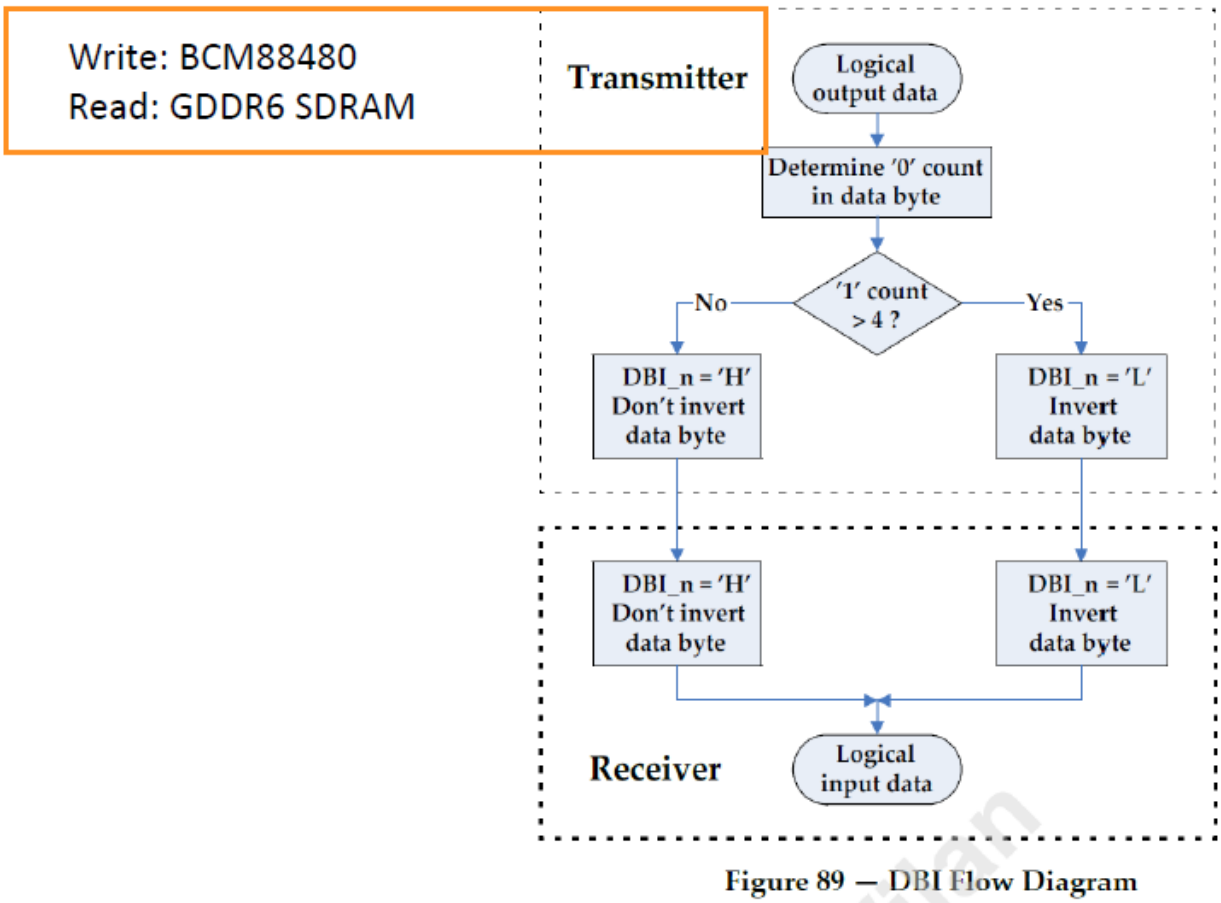


Figure 89 — DBI Flow Diagram

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 107

Indirect Infringement (Inducement – 35 U.S.C. § 271(b))

91. In addition and/or in the alternative to its direct infringements, Broadcom has indirectly infringed and continues to indirectly infringe one or more claims of the '344 Patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the '344 Accused Products.

92. At a minimum, Broadcom has knowledge of the '344 Patent since being served with this Complaint. Broadcom also has knowledge of the '344 Patent from Polaris's letter and accompanying claim charts sent prior to the filing of this suit. Since receiving notice of its

infringements, Broadcom has actively induced the direct infringements of its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Such inducements have been committed with the knowledge, or with willful blindness to the fact, that the acts induced constitute infringement of the '344 Patent. On information and belief, Broadcom has intended to cause, continues to intend to cause, and has taken, and continues to take affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the '344 Accused Products; creating and/or maintaining established distribution channels for the '344 Accused Products into and within the United States; manufacturing the '344 Accused Products in conformity with U.S. laws and regulations; distributing or making available datasheets supporting use of the '344 Accused Products that promote their features, specifications, and applications; providing technical documentation and tools for the '344 Accused Products, such as white papers, brochures, and/or manuals; promoting the incorporation of the '344 Accused Products into end-user products, testing and certifying features related to error coding in the '344 Accused Products; and/or by providing technical support and/or related services for these products to purchasers in the United States.

Damages

93. On information and belief, despite having knowledge of the '344 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the '344 Patent, Broadcom has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. Broadcom's infringing activities relative to the '344 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, characteristic of a pirate, and an egregious case of misconduct beyond typical

infringement such that Polaris is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

94. Polaris has been damaged as a result of Broadcom's infringing conduct described in this Count. Broadcom is, thus, liable to Polaris in an amount that adequately compensates Polaris for Broadcom's infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

COUNT V

(INFRINGEMENT OF U.S. PATENT NO. 8,207,976)

95. Plaintiff incorporates the preceding paragraphs herein by reference.

96. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

97. Polaris is the owner of all substantial rights, title, and interest in and to the '976 Patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

98. The '976 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on June 26, 2012, after full and fair examination.

99. Broadcom has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the '976 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, Broadcom products, their components and processes, and/or products containing the same that incorporate the fundamental technologies covered by the '976 Patent, including, but not limited to, Broadcom's GDDR6-based Products including the Broadcom BCM88480, BCM88280, BCM88800, BCM88790, BCM88690, BCM88480, and BCM88280 Processors (collectively, the "'976 Accused Products").

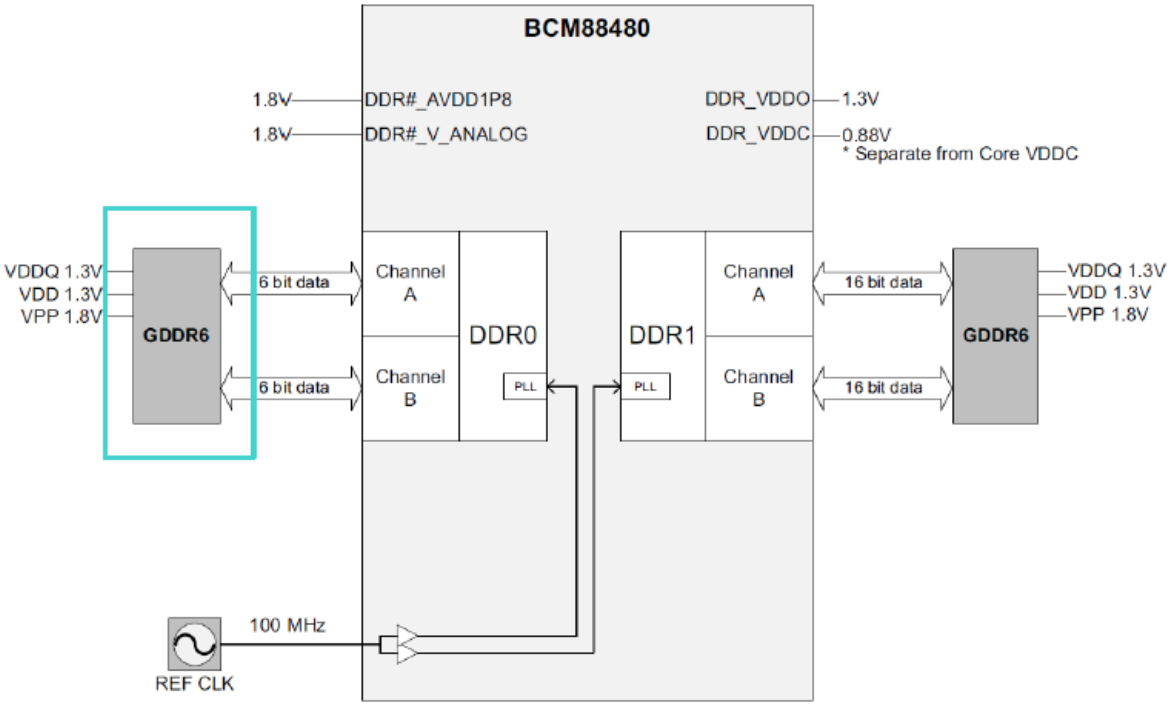
Direct Infringement (35 U.S.C. § 271(a))

100. Broadcom has directly infringed and continues to directly infringe one or more claims of the'976 Patent in this District and elsewhere in Texas and the United States.

101. Broadcom has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 35 of the '976 Patent as set forth under 35 U.S.C. § 271(a) by making, using, offering for sale, selling, and/or importing the '976 Accused Products. Furthermore, Broadcom makes and sells the '976 Accused Products outside of the United States and either delivers those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivers the '976 Accused Products outside of the United States, it does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the '976 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013).

102. By way of illustration only, the '976 Accused Products comprise each and every element of claim 35 of the '976 Patent. The '976 Accused Products comprise "[a] memory system comprising a memory circuit." For example, the '976 Accused Products comprise a memory system and memory circuit, such as the BCM88480 Processor:

Figure 32: BCM88480 GDDR6 DRAM High-Level Blocks



Source: DNX16 Hardware Design Guidelines for StrataDNX™16-nm Devices, Broadcom, Page 64

103. The memory circuit further comprises an output buffer comprising an input and an output, for example as indicated below in the figure from the SGRAM Standard:

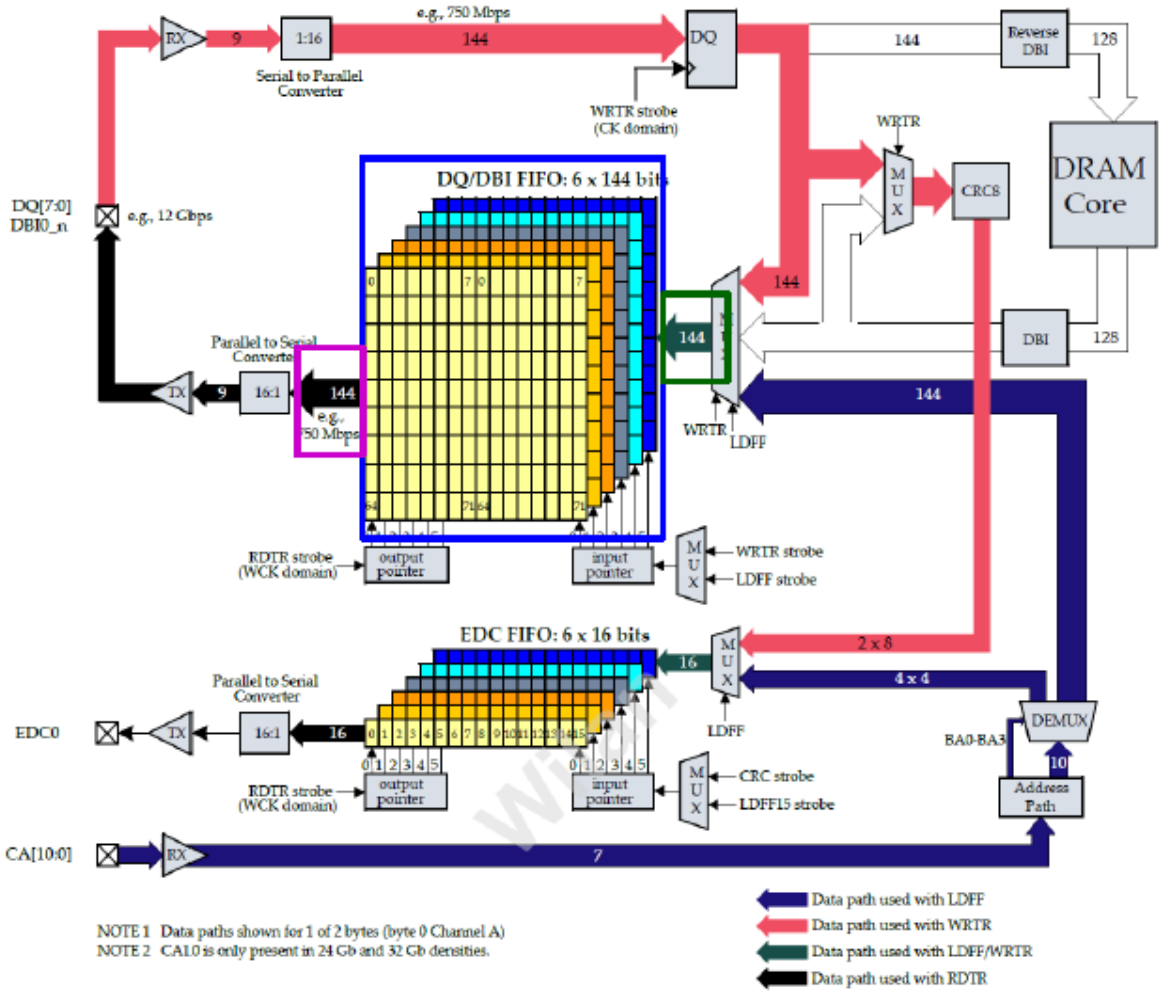


Figure 23 — Data Paths used for Read and Write Training

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 35

104. The memory circuit further comprises a data interface for transmitting and receiving data, for example as indicated in the figure below from the SGRAM Standard:

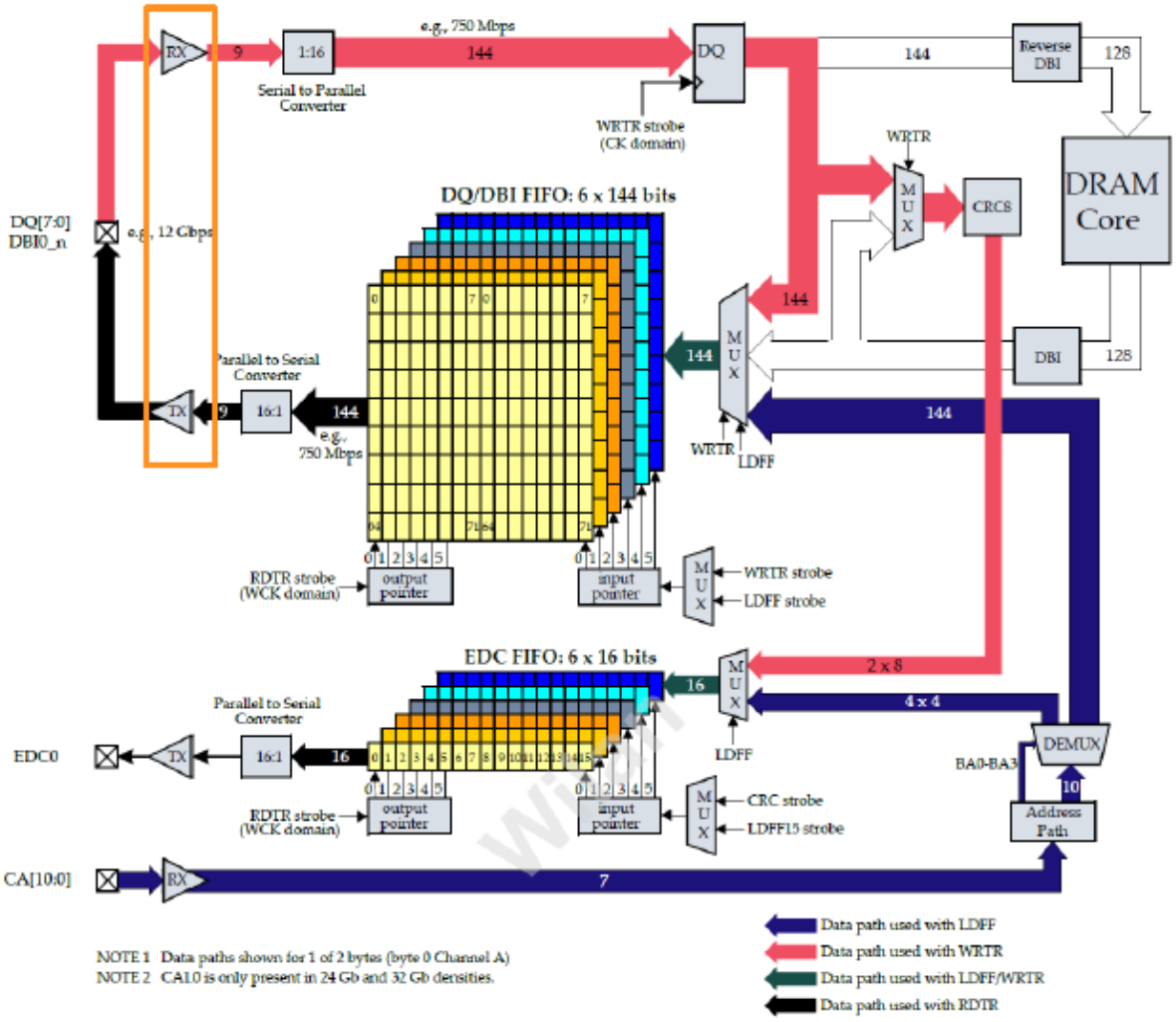


Figure 23 — Data Paths used for Read and Write Training

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 35

105. The data interface is coupled to the output of the output buffer, for example as indicated in the figure below from the SGRAM Standard:

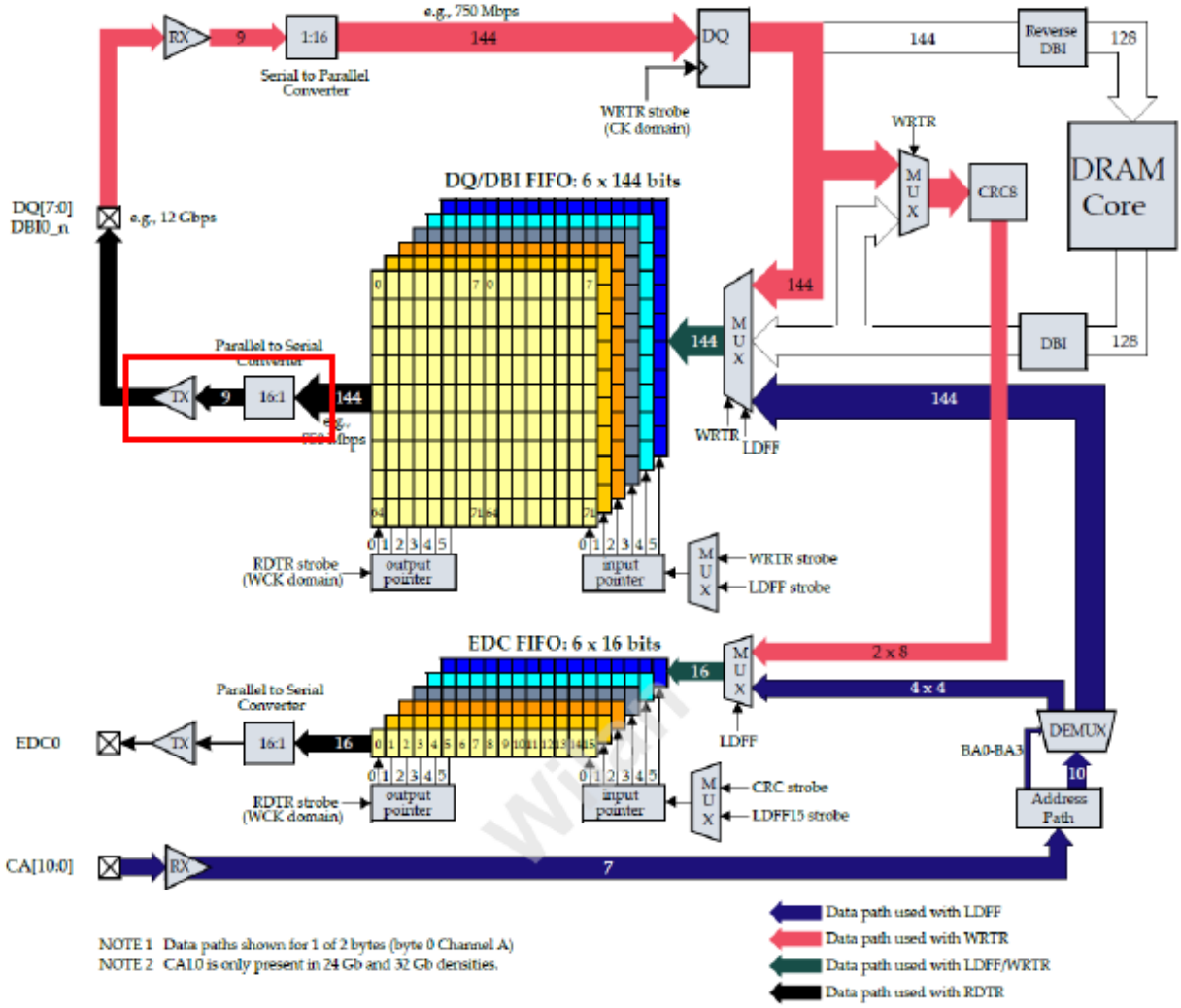


Figure 23 — Data Paths used for Read and Write Training

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 35

106. The memory circuit further comprises a command/address interface coupled to the input of the output buffer, for example as shown below in the diagrams from the SGRAM Standard:

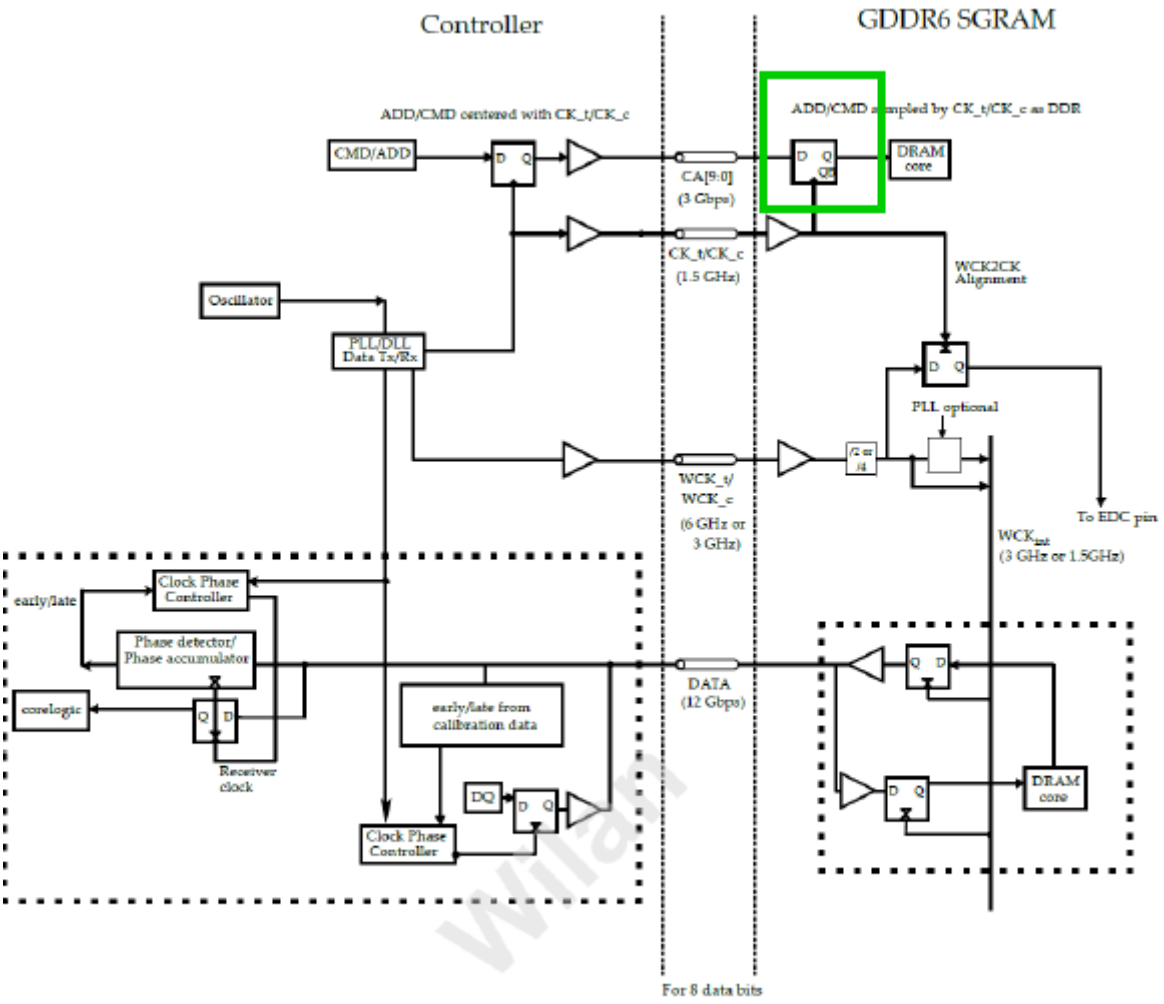


Figure 2 — Block Diagram of an example clock system

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 7

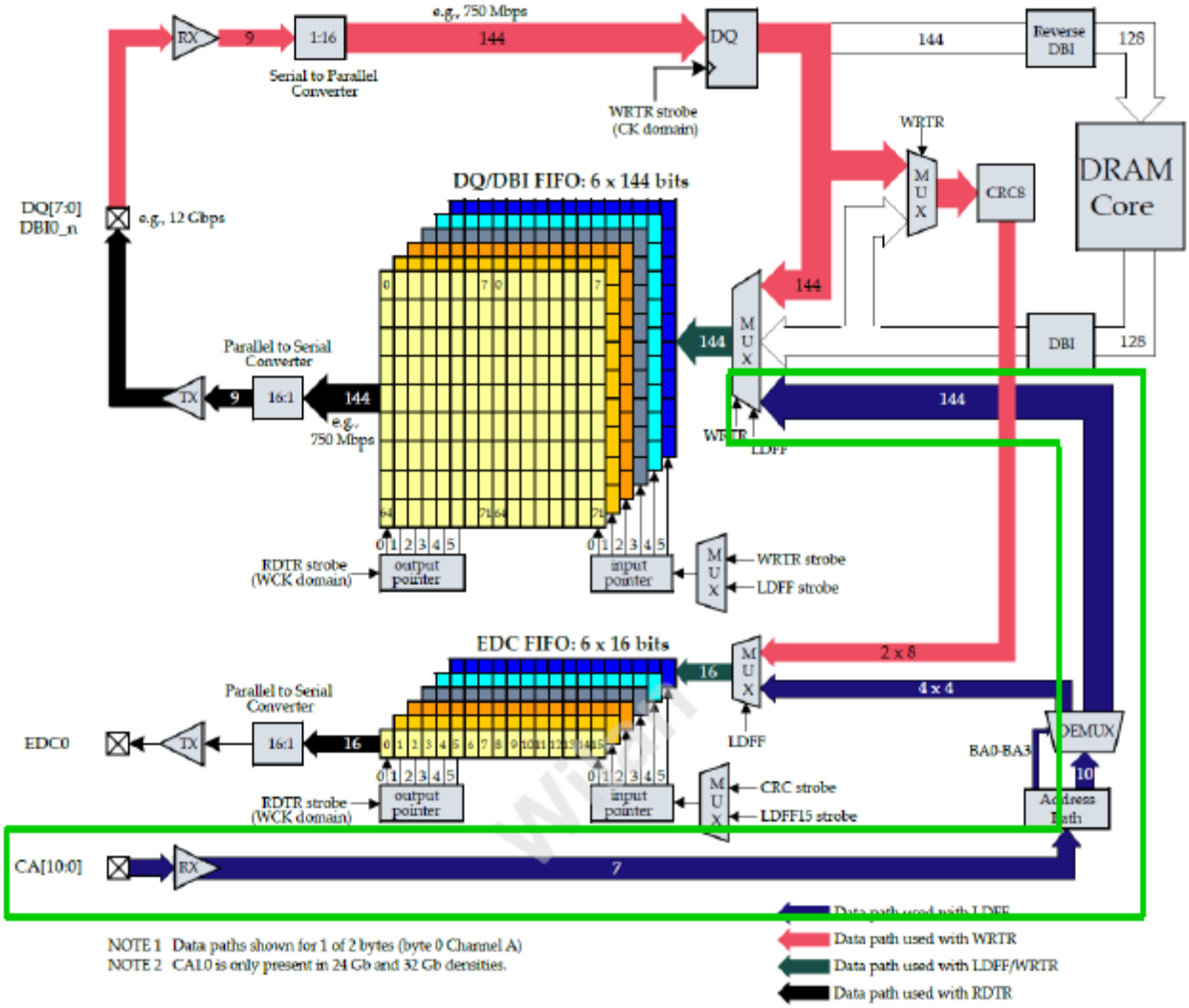


Figure 23 — Data Paths used for Read and Write Training

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 35

107. The memory circuit further comprises a memory core coupled to the input of the output buffer, for example as shown below in the diagrams from the SGRAM Standard:

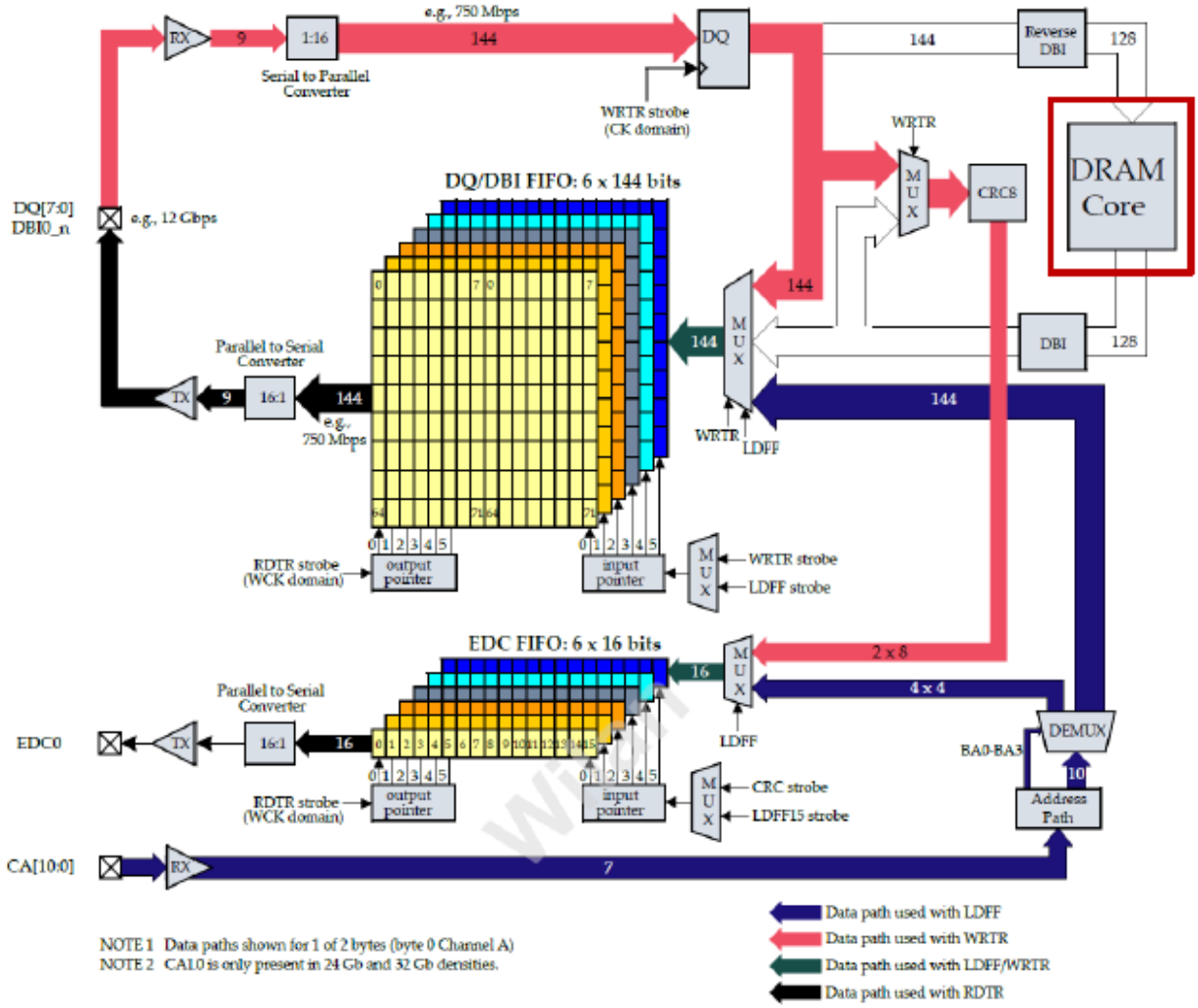


Figure 23 — Data Paths used for Read and Write Training

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 35

108. The memory circuit further comprises a second output buffer comprising an input and an output, for example as shown below in the diagrams from the SGRAM Standard:

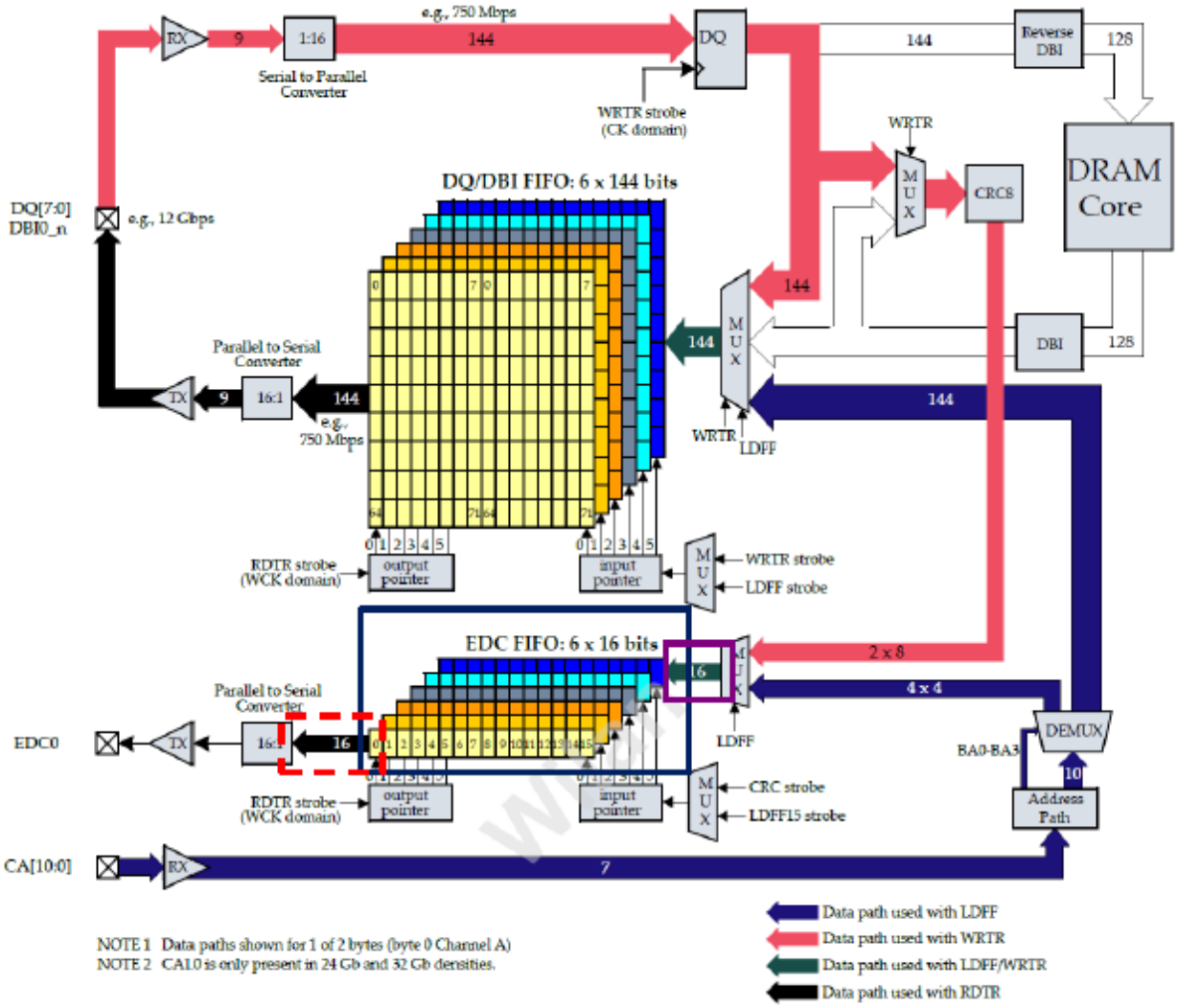


Figure 23 — Data Paths used for Read and Write Training

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 35

109. The output of the second output buffer is coupled to the data interface or to a further output pin, for example as shown below in the diagrams from the SGRAM Standard:

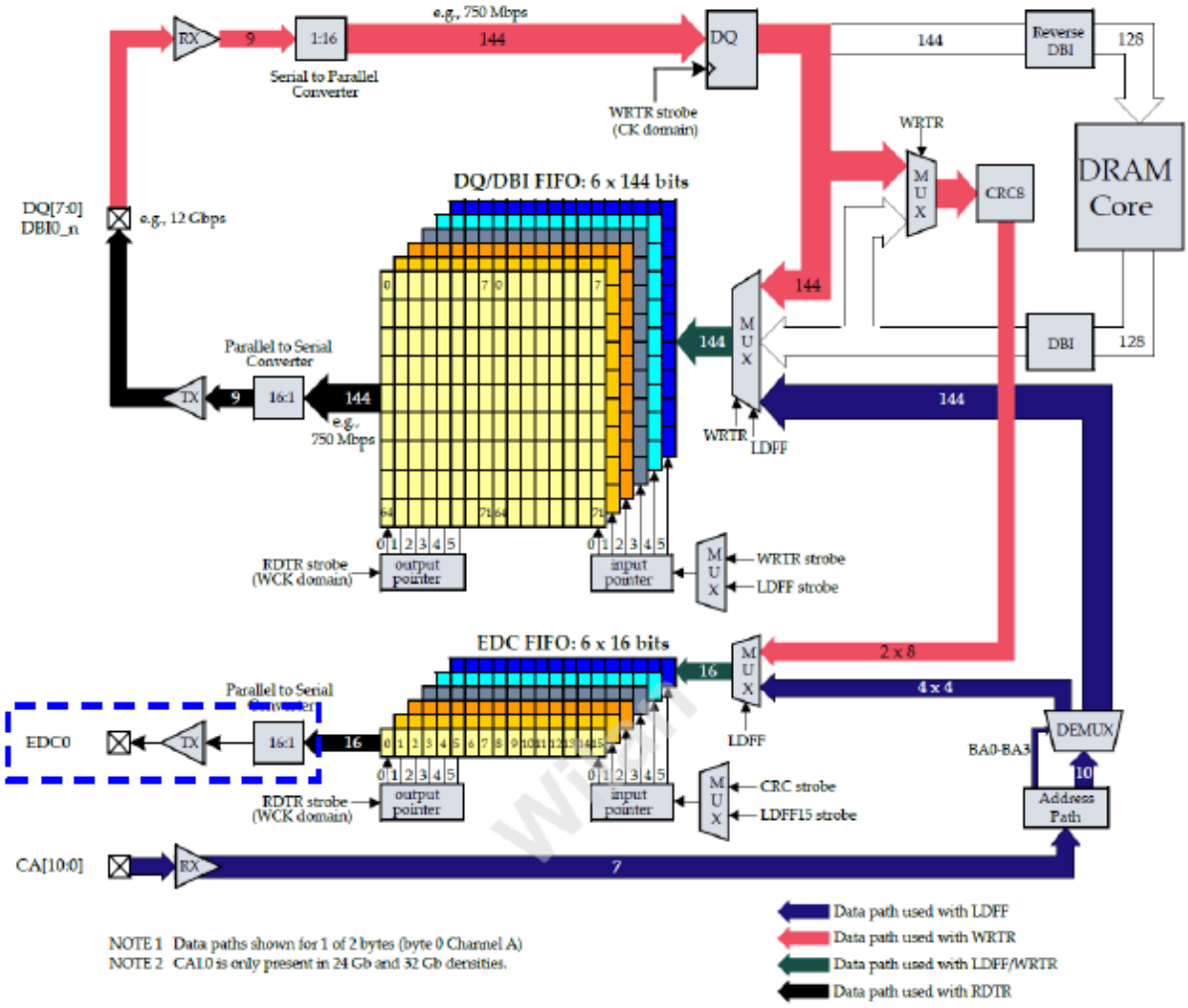


Figure 23 — Data Paths used for Read and Write Training

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 35

110. The memory circuit further comprises an EDC circuit having an output coupled to the input of the second output buffer, for example as shown below in the diagram and description from the SGRAM Standard:

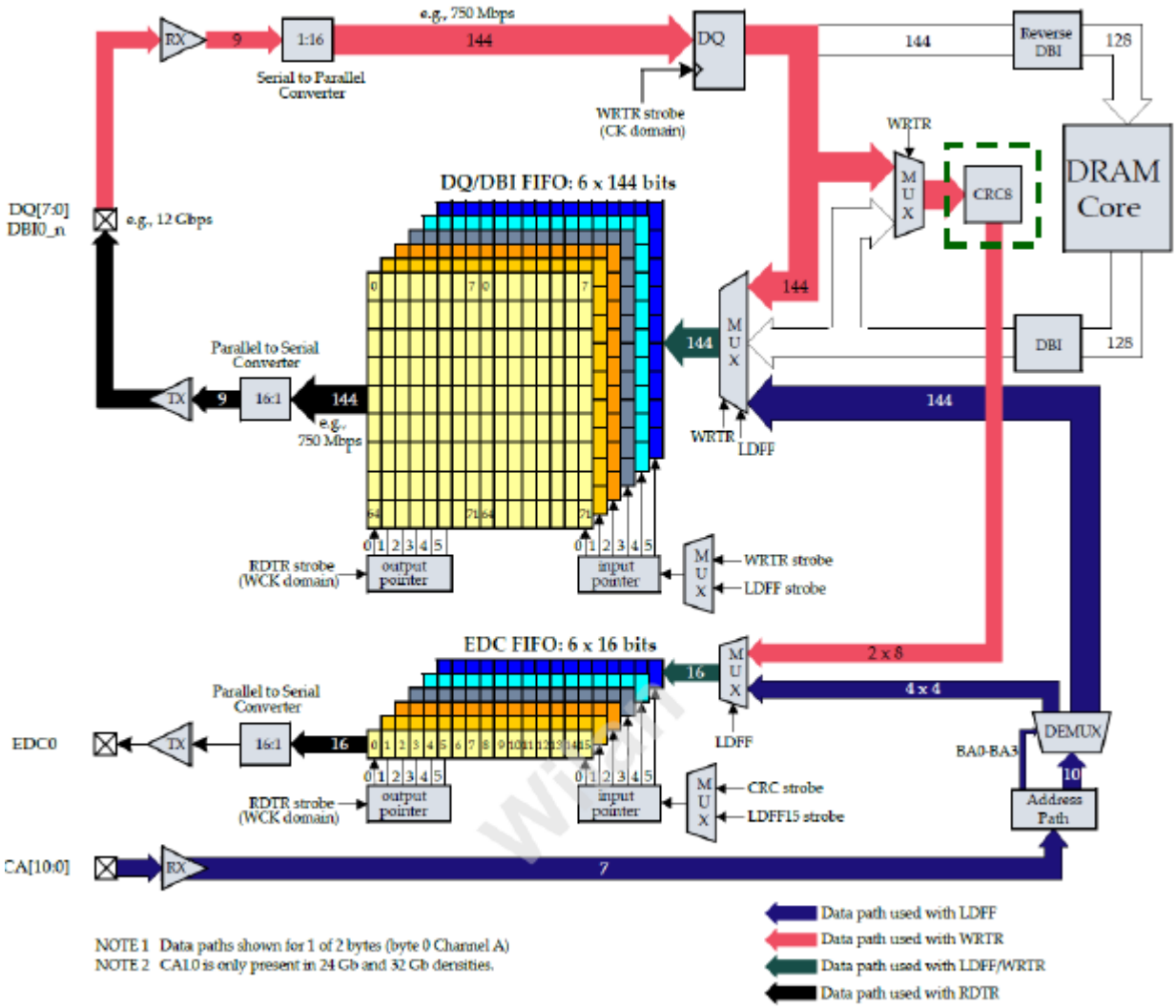


Figure 23 — Data Paths used for Read and Write Training

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 35

7.14 ERROR DETECTION CODE (EDC)

The GDDR6 SGRAM provides error detection on the data bus to improve system reliability. The device generates a checksum per byte lane for both READ and WRITE data and returns the checksum to the controller. GDDR6 supports 2 modes for the EDC with either a 16 bit checksum that runs at same rate as the data (Full data rate EDC) or an 8 bit checksum that runs at half the rate of the data (Half data rate EDC). Mode Register 2 OP8 selects between the 2 modes and is undefined at boot. The EDC rate register must be set during the initialization sequence after power up or after a reset.

The 16 bit checksum of the Full data rate EDC is calculated in two halves based on the 2 halves of the 16 bit burst. The first 8 bits of the checksum, CRC-L, are calculated on burst positions 0 thru 7 and the second half of the checksum, CRC-U, are calculated on burst positions 8 thru 15. The 8 bit checksum of the Half data rate EDC is calculated on the full 16bit burst using an XOR of the CRC-L and CRC-U as illustrated in Figure 90.

Based on the checksum, the controller can decide if the data (or the returned CRC) was transmitted in error and retry the READ or WRITE command. The device itself does not perform any error correction. The features of the EDC are:

- 8 bit checksum on 72 bits (9 bit lanes x 8 bit burst) x 2 for 16bit checksum (Full data rate EDC) or 8 bit checksum on 144 bits (9 bit lanes x 16 bit burst) for 8 bit checksum (Half data rate EDC)
- dedicated EDC transfer pin per 9 bit lanes (2x per channel)
- asymmetrical latencies on EDC transfer for READs and WRITEs

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 108

111. The '976 Accused Products further comprise a memory system and controller circuit adapted to cause data stored within the output buffer to be output to the data interface upon reception of a first signal, for example as indicated below:

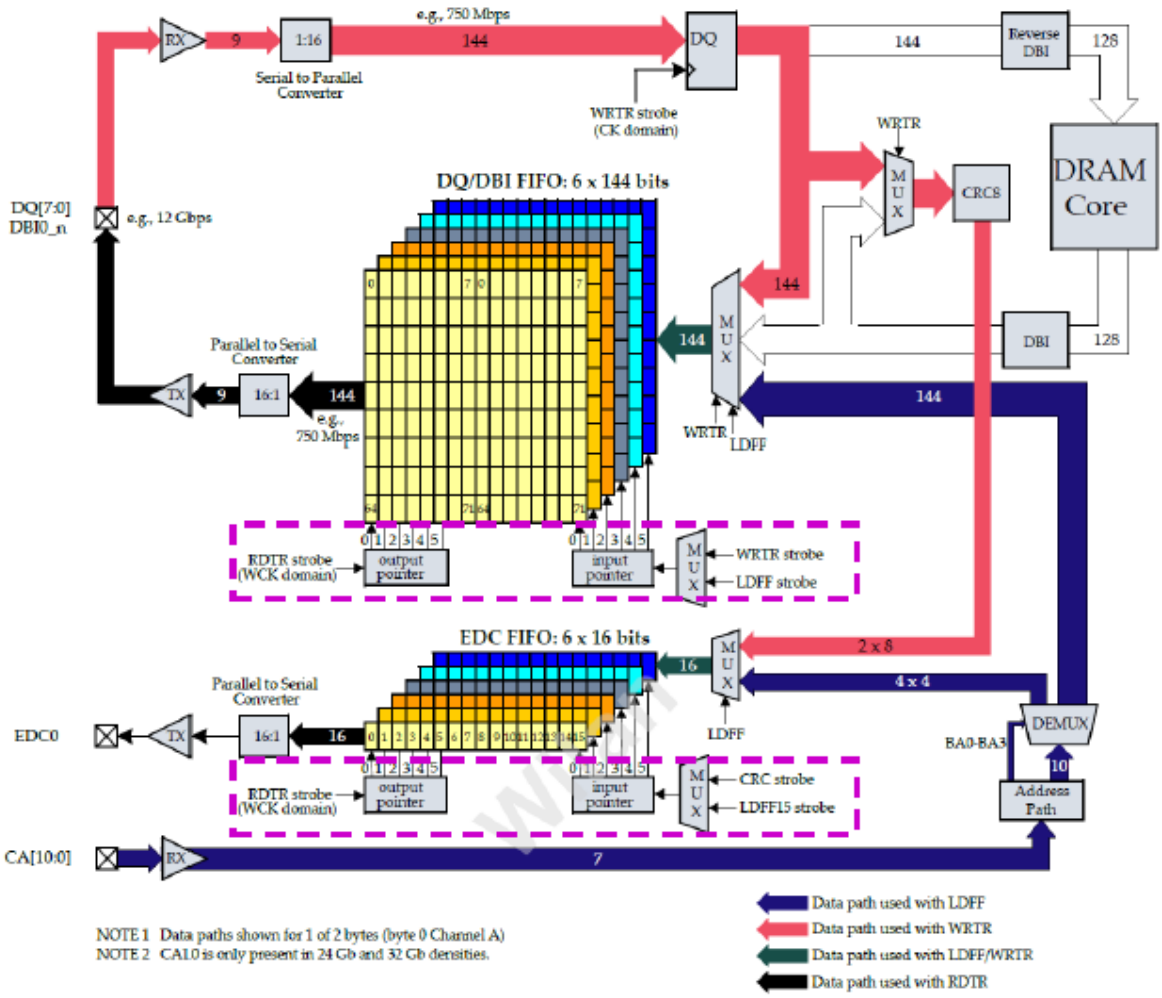


Figure 23 — Data Paths used for Read and Write Training

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 35

5.4 READ TRAINING

Read training allows the memory controller to find the data-eye optimal position (symbol training) and burst frame location (frame training) for each high-speed output of the device. Each pin (DQ[15:0], DBI[1:0]_n, EDC[1:0]) can be individually trained during this sequence.

For Read Training the following conditions must be true:

- at least one bank is active, or a REFab must be in progress and OP2 in Mode Register 5 (MR5) is set to 0 to allow training during a REFab (to disable this special refresh enabling of the WCK clock tree an ACT command must be issued, or the device must be set into power-down or self refresh mode)
- WCK2CK training must be complete
- the PLL/DLL must be locked, if enabled
- RDBI and WDBI must be enabled prior to and during Read Training if the training shall include DBI_n. RDCRC and WRCRC must be enabled prior to and during Read Training if the training shall include the EDC signals.

The following commands are associated with Read Training:

- LDFF to preload the Read FIFO;
- RDTR to read a burst of data directly out of the Read FIFO.

Neither LDFF nor RDTR access the memory core. No MRS is required to enter Read Training.

Figure 23 shows an example of the internal data paths used with LDFF and RDTR. Table 22 lists AC timing parameters associated with Read Training.

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 34

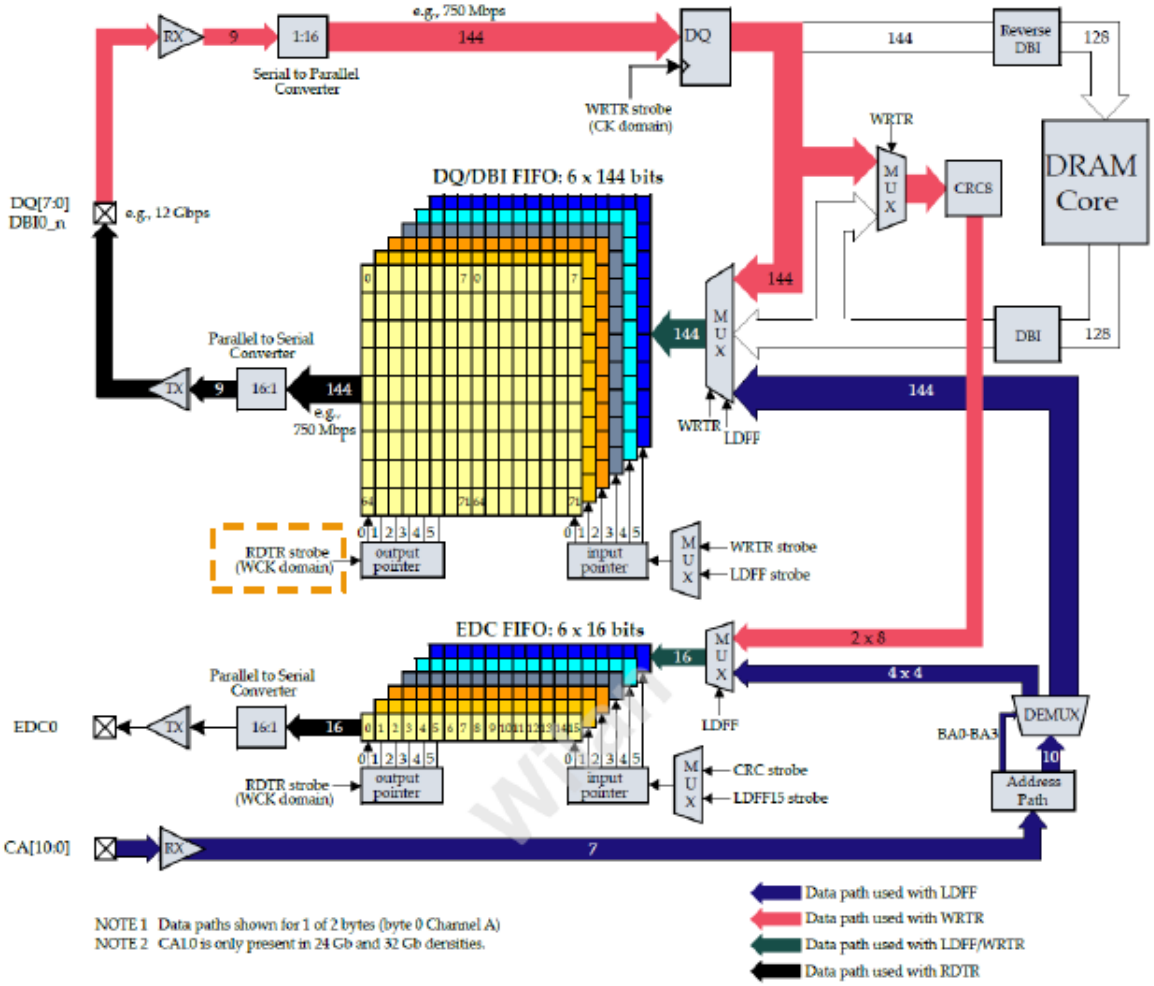


Figure 23 — Data Paths used for Read and Write Training

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 35

112. The controller circuit is further adapted to cause data stored within the memory core to be output to the input of the output buffer upon reception of a second signal, for example as indicated below from the SGRAM Standard:

7.10 READ

A READ burst is initiated with a READ command as shown in Figure 74. The bank and column addresses are provided with the READ command and auto precharge is either enabled or disabled for that access with the AP bit (CA4 input falling edge of CK). If auto precharge is enabled, the row being accessed is precharged at a time t_{RTP} after the READ command and after t_{RAS}(min) has been met or after the number of clock cycles programmed in the RAS field of MR5, depending on the implementation choice per DRAM vendor. The length of the burst initiated with a READ command is sixteen and the column address is unique for this burst of sixteen. There is no interruption nor truncation of READ bursts. The array read access is suppressed, no read data and the EDC hold pattern instead of a CRC burst are transmitted when the CE bit is LOW. In two channel mode CE shall be driven HIGH.

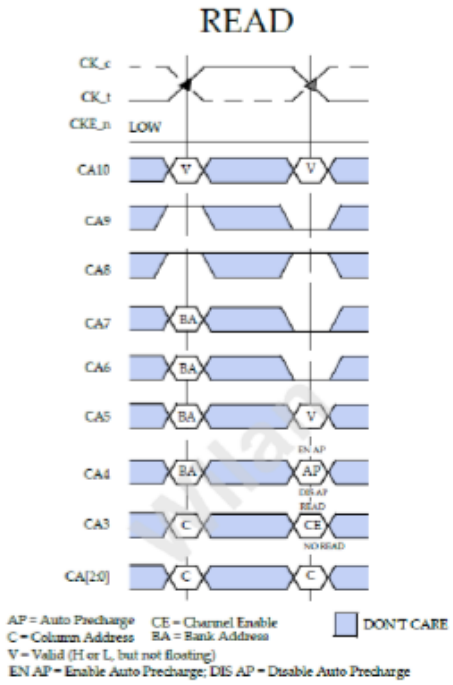


Figure 74 — READ Command

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 96

113. The controller circuit is further adapted to cause provision of data received at the command/address interface via an address portion thereof to the input of the output buffer upon reception of a third signal so that the data is stored within the output buffer, for example as indicated below from the SGRAM Standard:

5.4 READ TRAINING

Read training allows the memory controller to find the data-eye optimal position (symbol training) and burst frame location (frame training) for each high-speed output of the device. Each pin (DQ[15:0], DBI[1:0]_n, EDC[1:0]) can be individually trained during this sequence.

For Read Training the following conditions must be true:

- at least one bank is active, or a REFab must be in progress and OP2 in Mode Register 5 (MR5) is set to 0 to allow training during a REFab (to disable this special refresh enabling of the WCK clock tree an ACT command must be issued, or the device must be set into power-down or self refresh mode)
- WCK2CK training must be complete
- the PLL/DLL must be locked, if enabled
- RDBI and WDBI must be enabled prior to and during Read Training if the training shall include DBI_n. RDCRC and WRCRC must be enabled prior to and during Read Training if the training shall include the EDC signals.

The following commands are associated with Read Training:

- LDFF to preload the Read FIFO;
- RDTR to read a burst of data directly out of the Read FIFO.

Neither LDFF nor RDTR access the memory core. No MRS is required to enter Read Training.

Figure 23 shows an example of the internal data paths used with LDFF and RDTR. Table 22 lists AC timing parameters associated with Read Training.

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 34

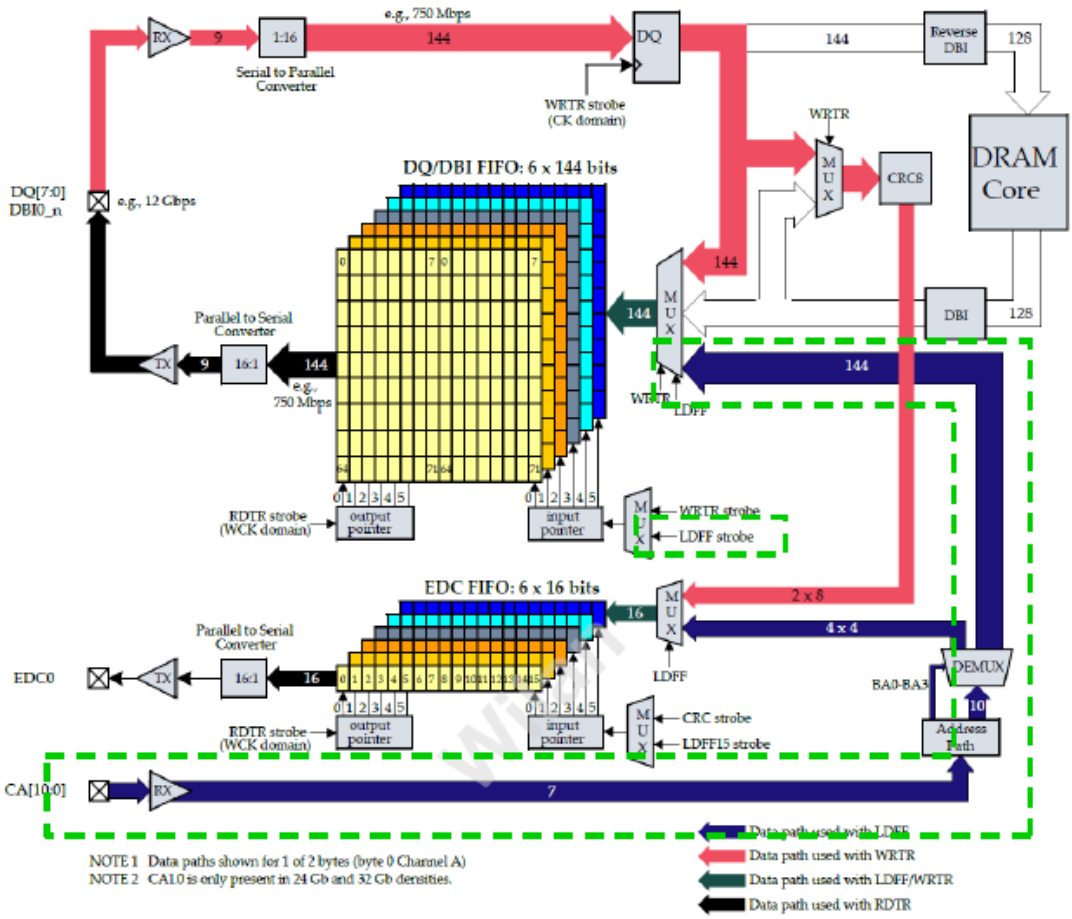


Figure 23 — Data Paths used for Read and Write Training

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 35

114. The controller circuit is further adapted to cause data which is stored within the second output buffer to be output to the data interface or the further output pin, for example as indicated below from the SGRAM Standard:

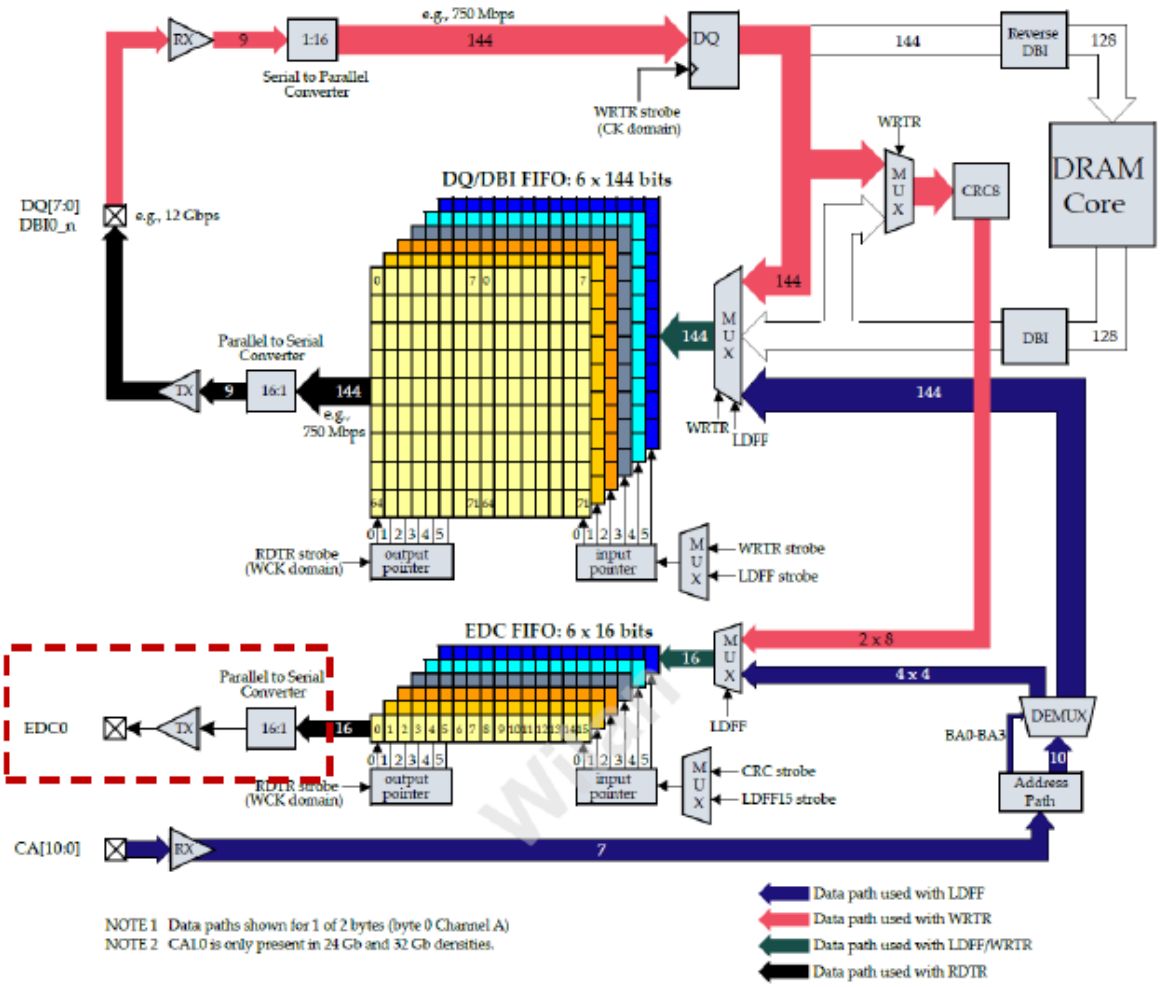


Figure 23 — Data Paths used for Read and Write Training

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 35

115. The controller circuit is further adapted to cause data which is provided by the EDC circuit to be stored within the second output buffer, for example as indicated below from the SGRAM Standard:

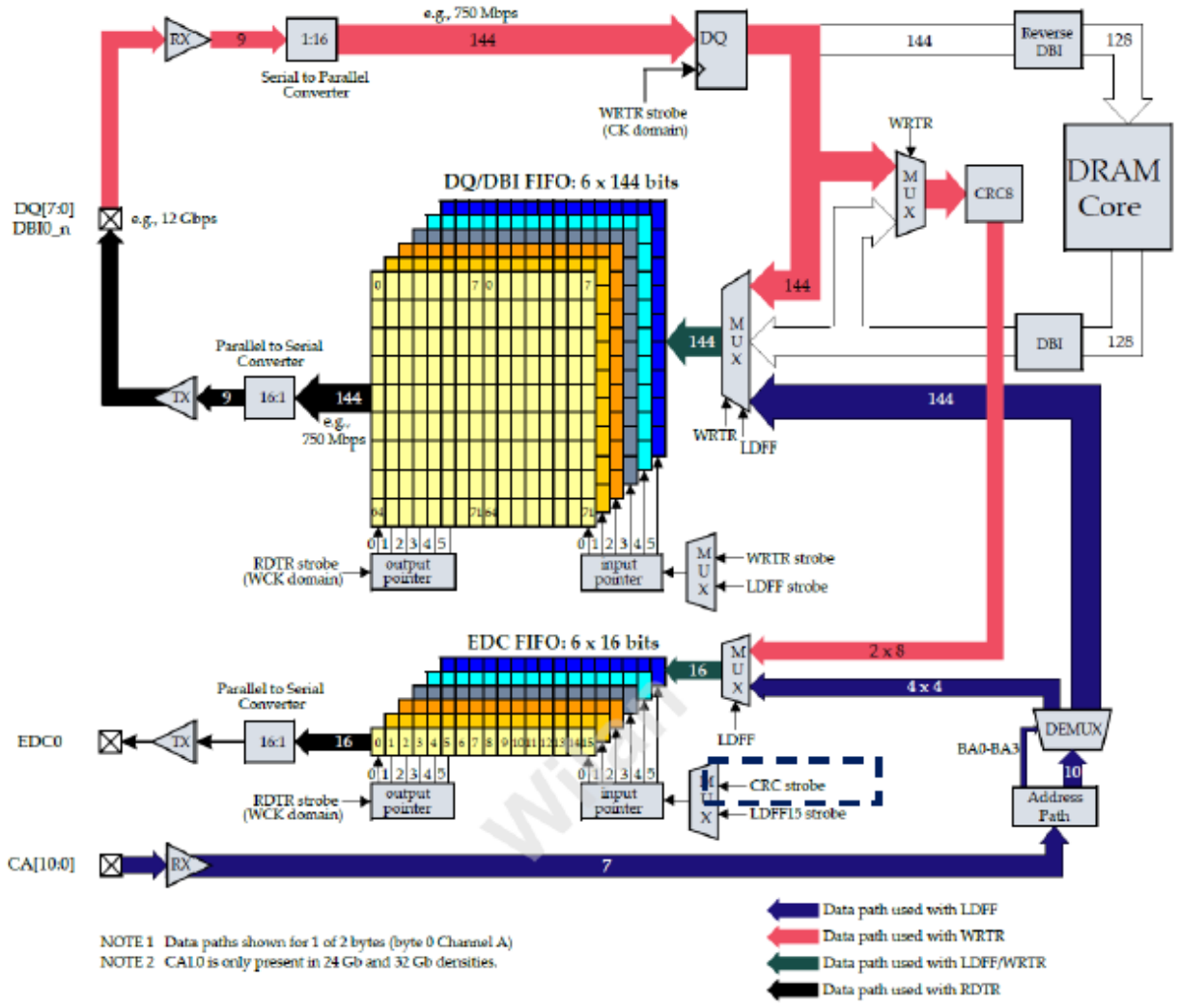


Figure 23 — Data Paths used for Read and Write Training

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 35

116. The controller circuit is further adapted to cause data which is received at the command/address interface to be stored within the second output bueffer, for example as indicated below from the SGRAM Standard:

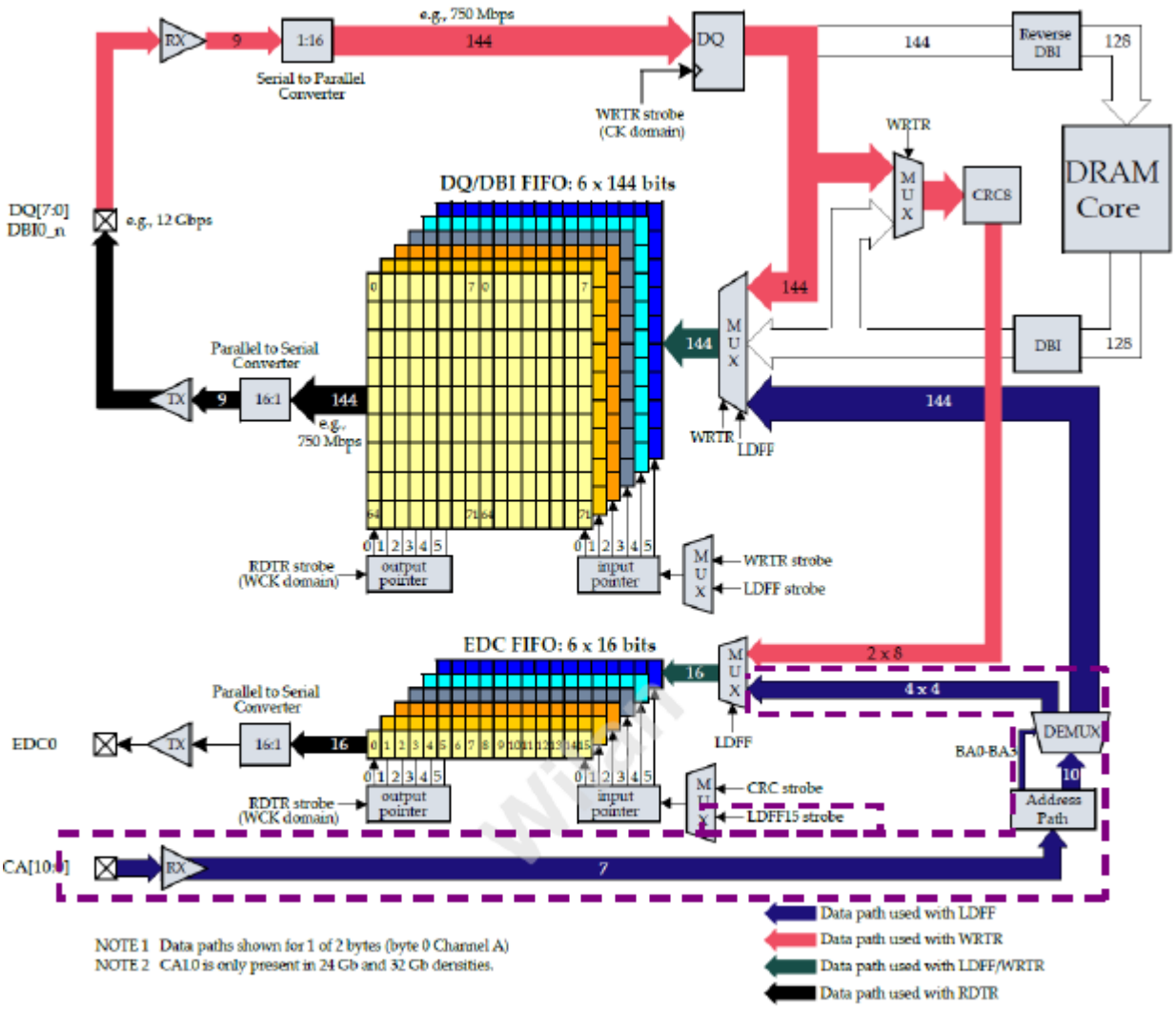
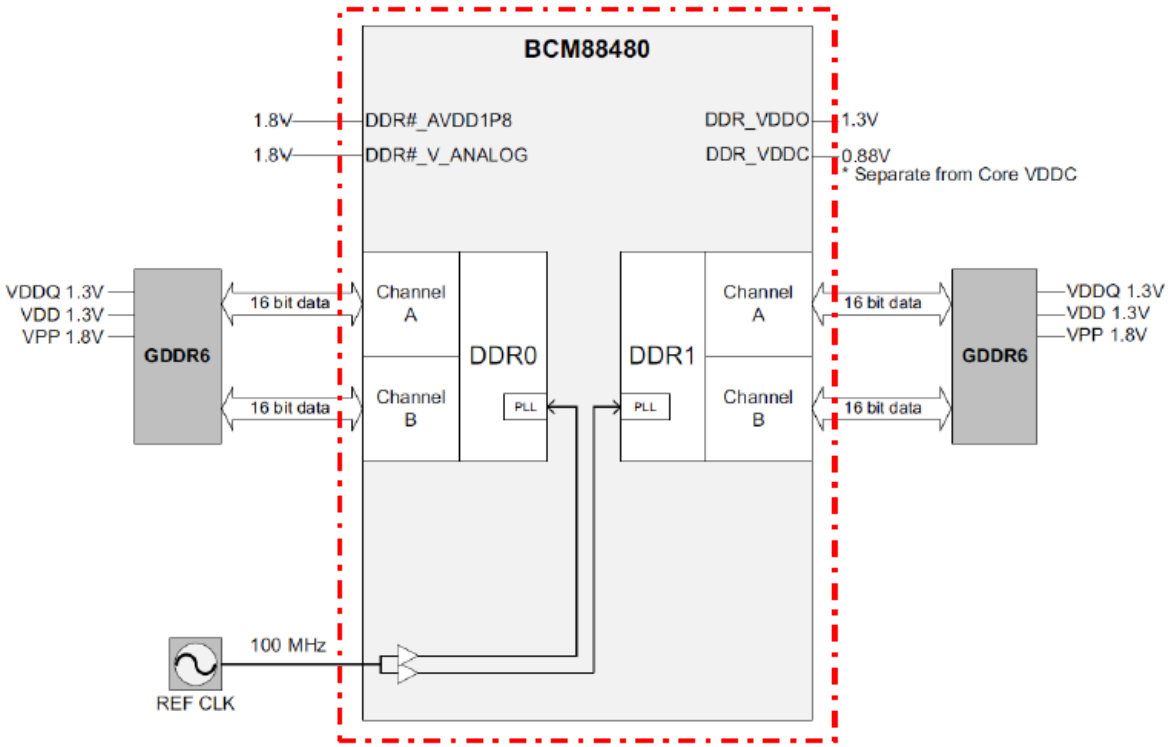


Figure 23 — Data Paths used for Read and Write Training

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 35

117. The '976 Accused Products further comprise a memory system and memory controller, for example such as the BCM88480:

Figure 32: BCM88480 GDDR6 DRAM High-Level Blocks



Source: DNX16 Hardware Design Guidelines for StrataDNX™ 16-nm Devices, Broadcom, Page 64

Source: DNX16 Hardware Design Guidelines for StrataDNX™16-nm Devices, Broadcom, Page 64

118. The memory controller further comprises a command/address interface, such as for example as indicated below from the SGRAM Standard:

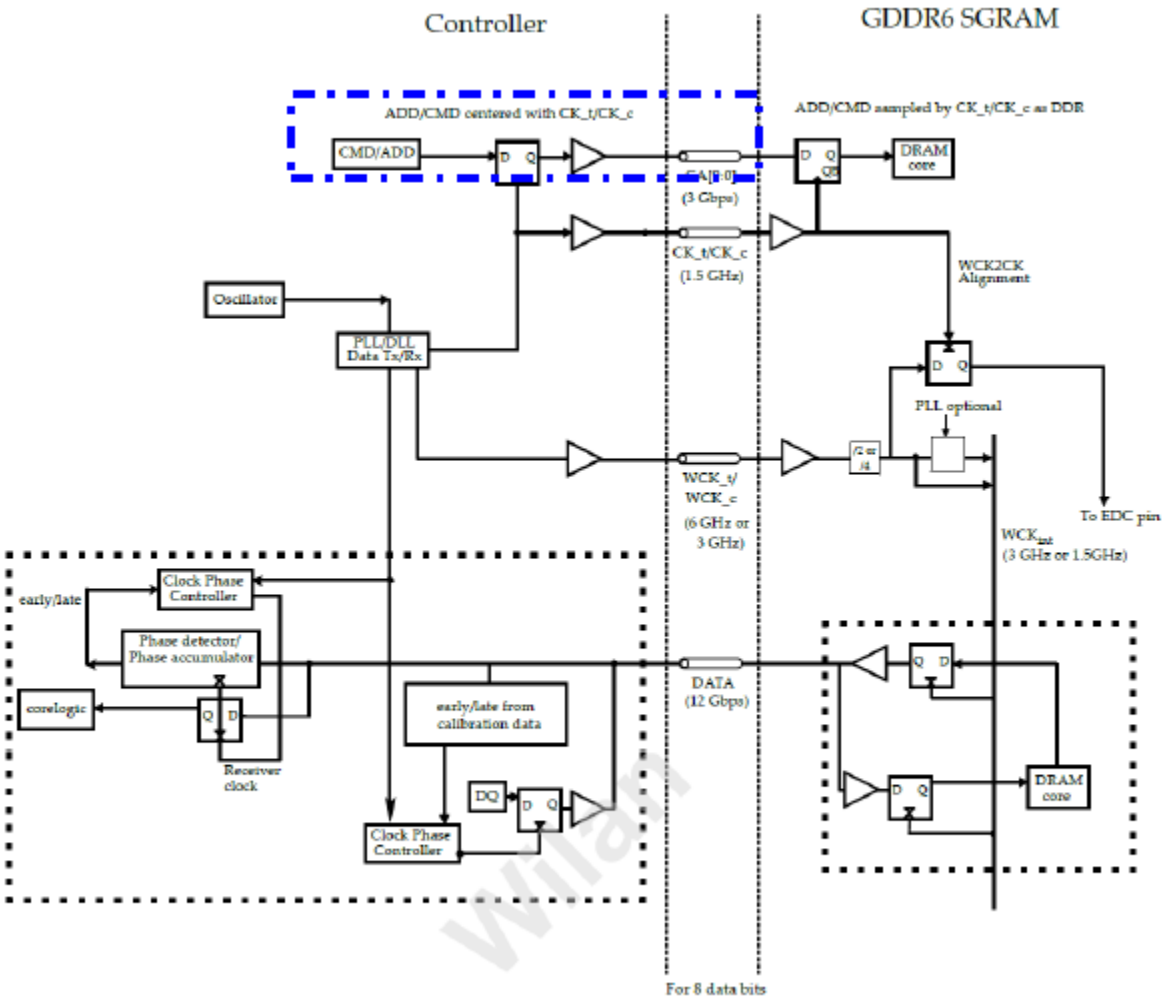


Figure 2 — Block Diagram of an example clock system

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 7

119. The memory controller further comprises a data interface, such as for example as indicated below from the SGRAM Standard:

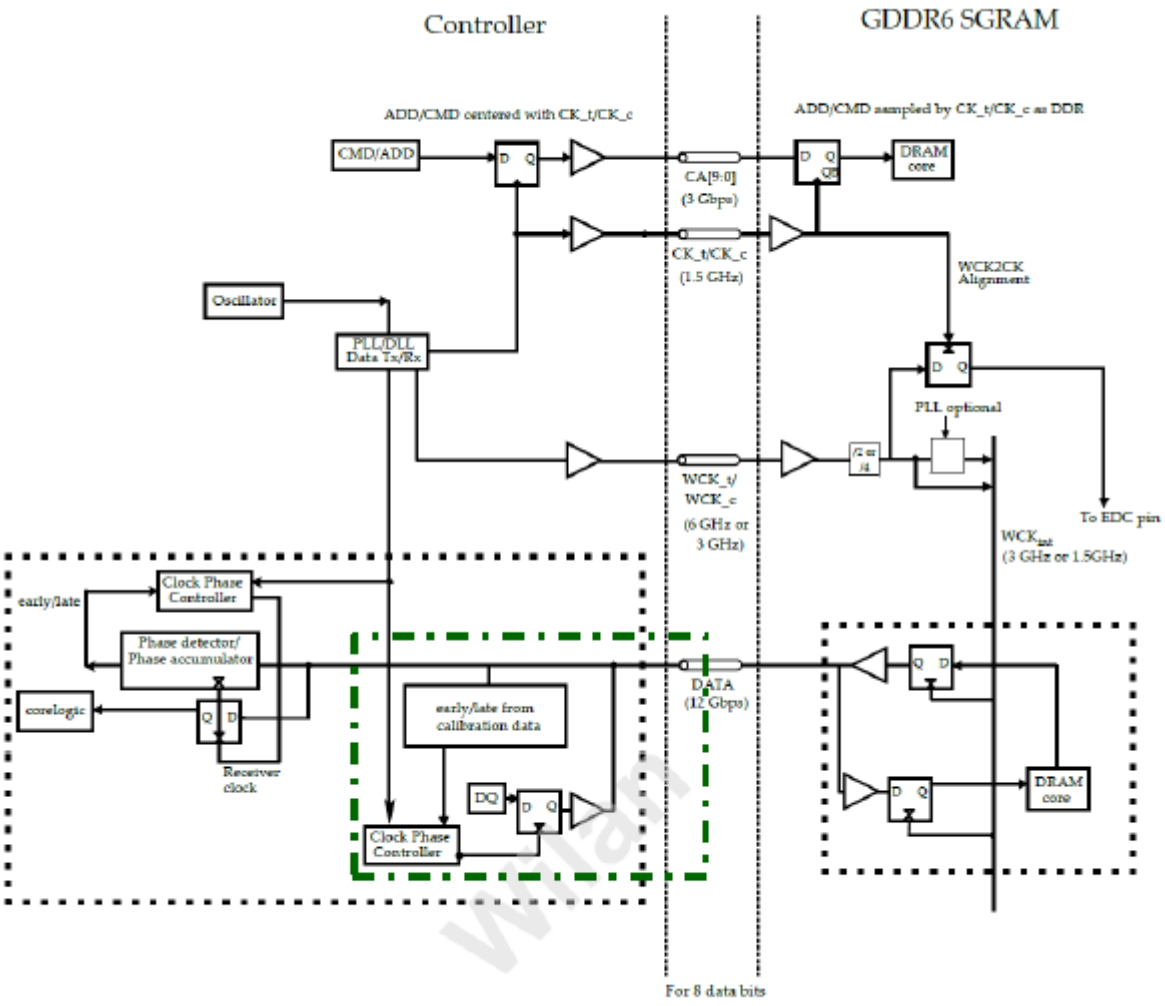


Figure 2 — Block Diagram of an example clock system

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 7

120. The memory controller further comprises a synchronization circuit coupled to the command/address interface and to the data interface, such as for example as indicated below from the SGRAM Standard:

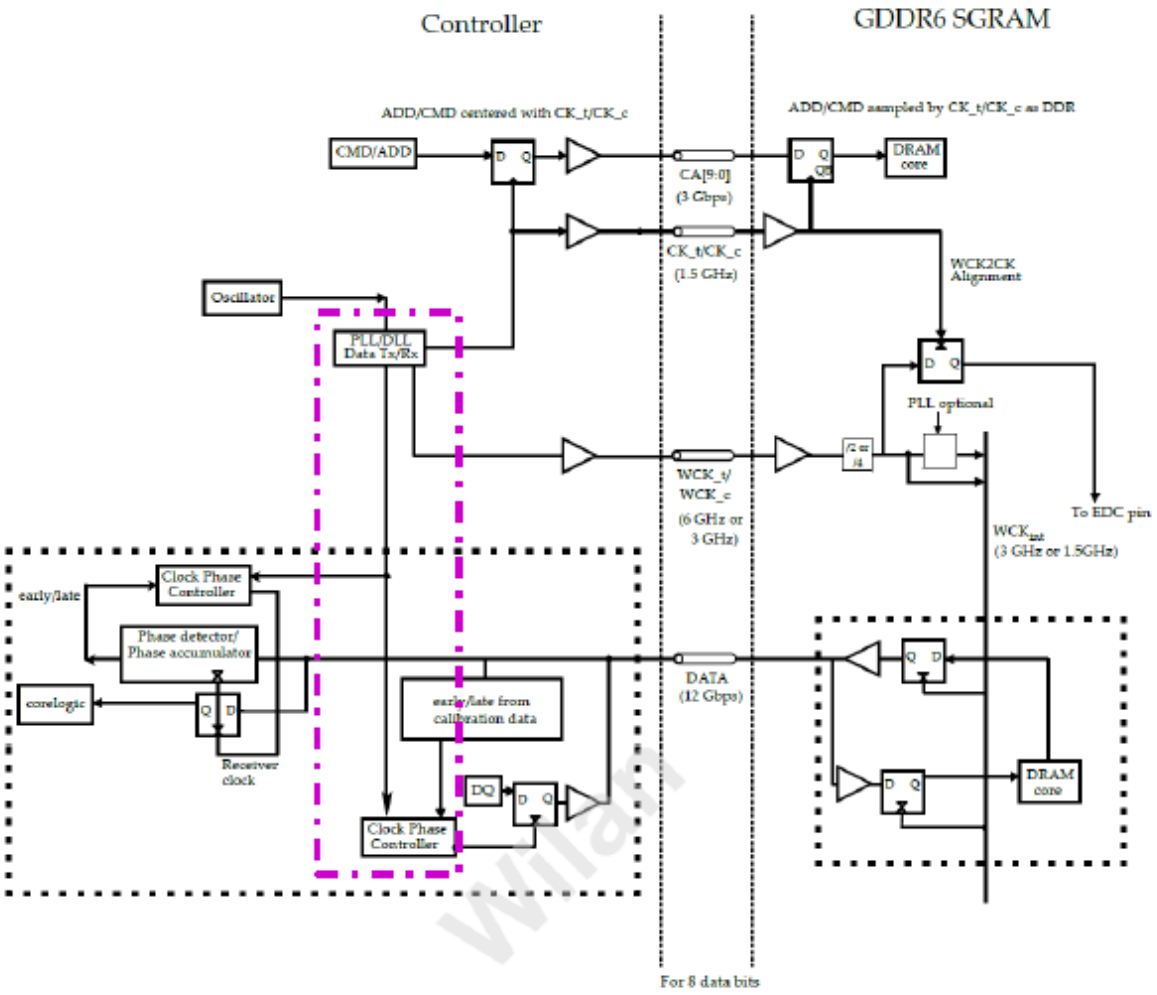


Figure 2 — Block Diagram of an example clock system

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 7

121. The a synchronization circuit is adapted to output a transmit data pattern as the synchronization data on the command/address interface via an address portion thereof, for example as indicated below from the SGRAM Standard:

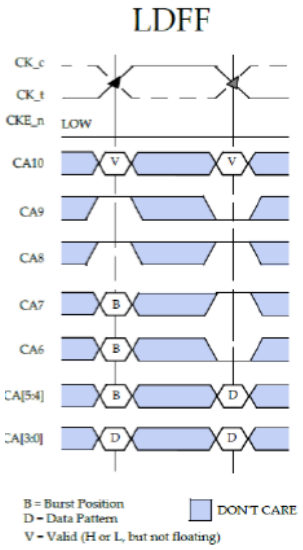


Figure 24 — LDFF Command

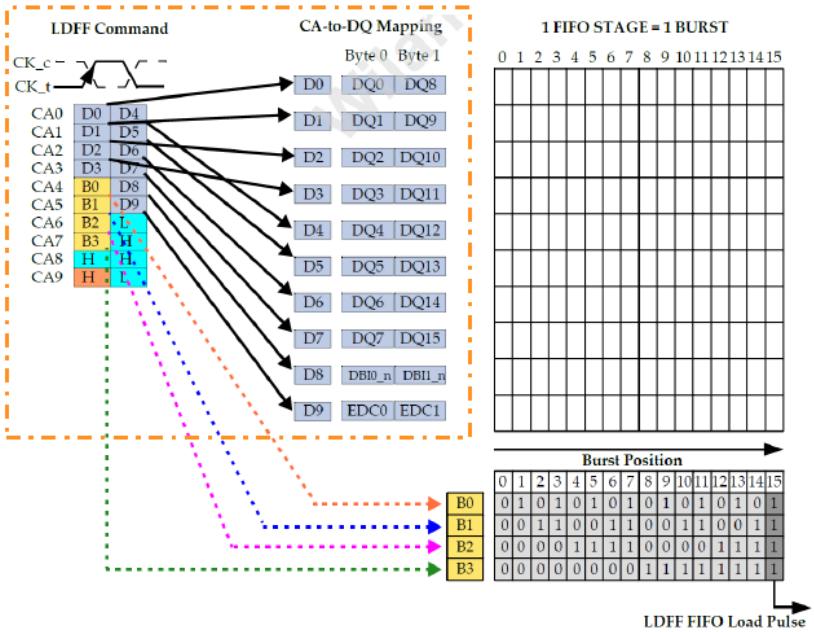


Figure 25 — LDFF Command Address to DQ/DBI_n/EDC Mapping

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 36

122. The synchronization circuit is adapted to receive a receive data pattern from the data interface, for example as indicated below from the SGRAM Standard:

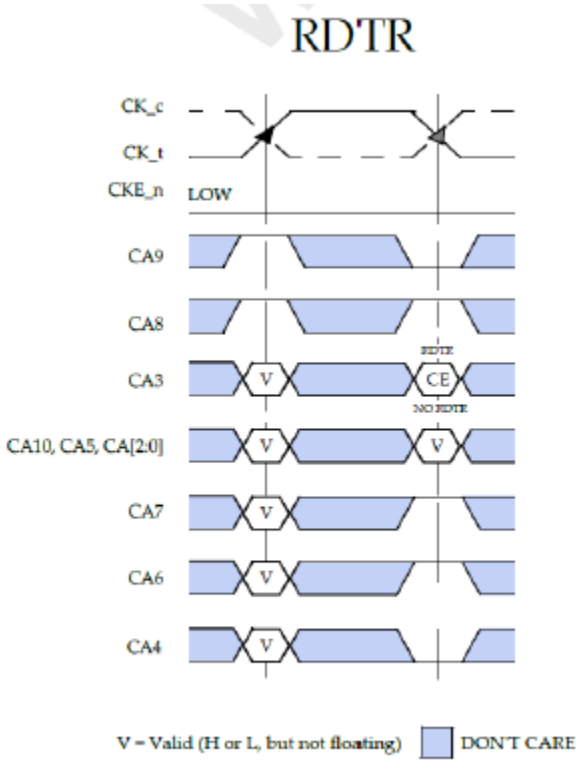


Figure 26 — RDTR Command

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 37

123. The synchronization circuit is further adapted to perform a training operation on the data interface on the basis of the transmit data pattern and the receive data pattern, for example as indicated below from the SGRAM Standard:

5.4 READ TRAINING

Read training allows the memory controller to find the data-eye optimal position (symbol training) and burst frame location (frame training) for each high-speed output of the device. Each pin (DQ[15:0], DBI[1:0]_n, EDC[1:0]) can be individually trained during this sequence.

For Read Training the following conditions must be true:

- at least one bank is active, or a REFab must be in progress and OP2 in Mode Register 5 (MR5) is set to 0 to allow training during a REFab (to disable this special refresh enabling of the WCK clock tree an ACT command must be issued, or the device must be set into power-down or self refresh mode)
- WCK2CK training must be complete
- the PLL/DLL must be locked, if enabled
- RDBI and WDBI must be enabled prior to and during Read Training if the training shall include DBI_n. RDCRC and WRCRC must be enabled prior to and during Read Training if the training shall include the EDC signals.

The following commands are associated with Read Training:

- LDFF to preload the Read FIFO;
- RDTR to read a burst of data directly out of the Read FIFO.

Neither LDFF nor RDTR access the memory core. No MRS is required to enter Read Training.

Figure 23 shows an example of the internal data paths used with LDFF and RDTR. Table 22 lists AC timing parameters associated with Read Training.

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 34

124. In the '976 Accused Products, the transmit data pattern is selected to perform one of a symbol training operation and a frame synchronization operation, for example as indicated below from the SGRAM Standard:

5.4 READ TRAINING

Read training allows the memory controller to find the data-eye optimal position (symbol training) and burst frame location (frame training) for each high-speed output of the device. Each pin (DQ[15:0], DBI[1:0]_n, EDC[1:0]) can be individually trained during this sequence.

For Read Training the following conditions must be true:

- at least one bank is active, or a REFab must be in progress and OP2 in Mode Register 5 (MR5) is set to 0 to allow training during a REFab (to disable this special refresh enabling of the WCK clock tree an ACT command must be issued, or the device must be set into power-down or self refresh mode)
- WCK2CK training must be complete
- the PLL/DLL must be locked, if enabled
- RDBI and WDBI must be enabled prior to and during Read Training if the training shall include DBI_n. RDCRC and WRCRC must be enabled prior to and during Read Training if the training shall include the EDC signals.

The following commands are associated with Read Training:

- LDFF to preload the Read FIFO;
- RDTR to read a burst of data directly out of the Read FIFO.

Neither LDFF nor RDTR access the memory core. No MRS is required to enter Read Training.

Figure 23 shows an example of the internal data paths used with LDFF and RDTR. Table 22 lists AC timing parameters associated with Read Training.

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 34

125. In the '976 Accused Products, the data interface of the memory circuit and the data interface of the memory controller are coupled to one another, for example as indicated below from the SGRAM Standard:

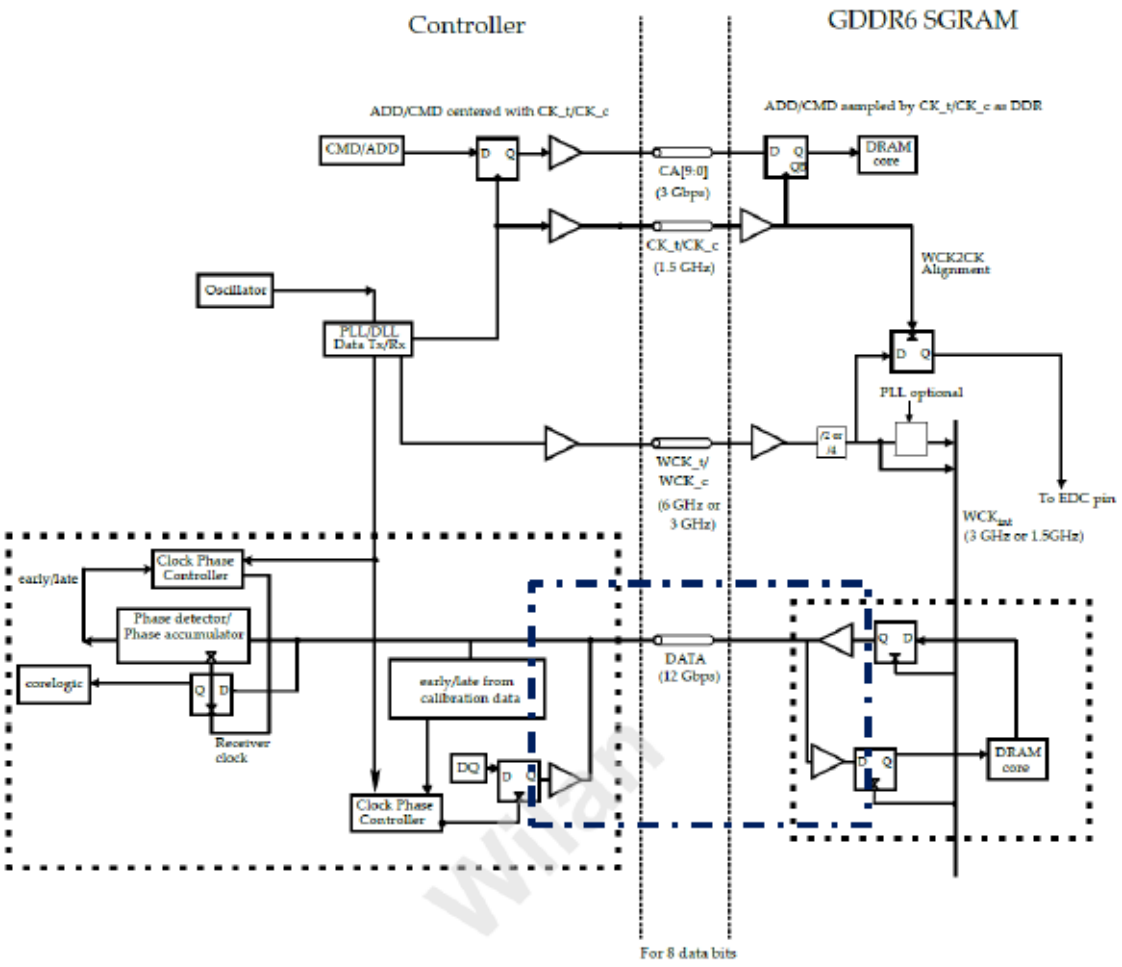


Figure 2 — Block Diagram of an example clock system

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 7

126. In the '976 Accused Products, the command/address interface of the memory circuit is coupled to the command/address interface of the memory controller, for example as indicated below from the SGRAM Standard:

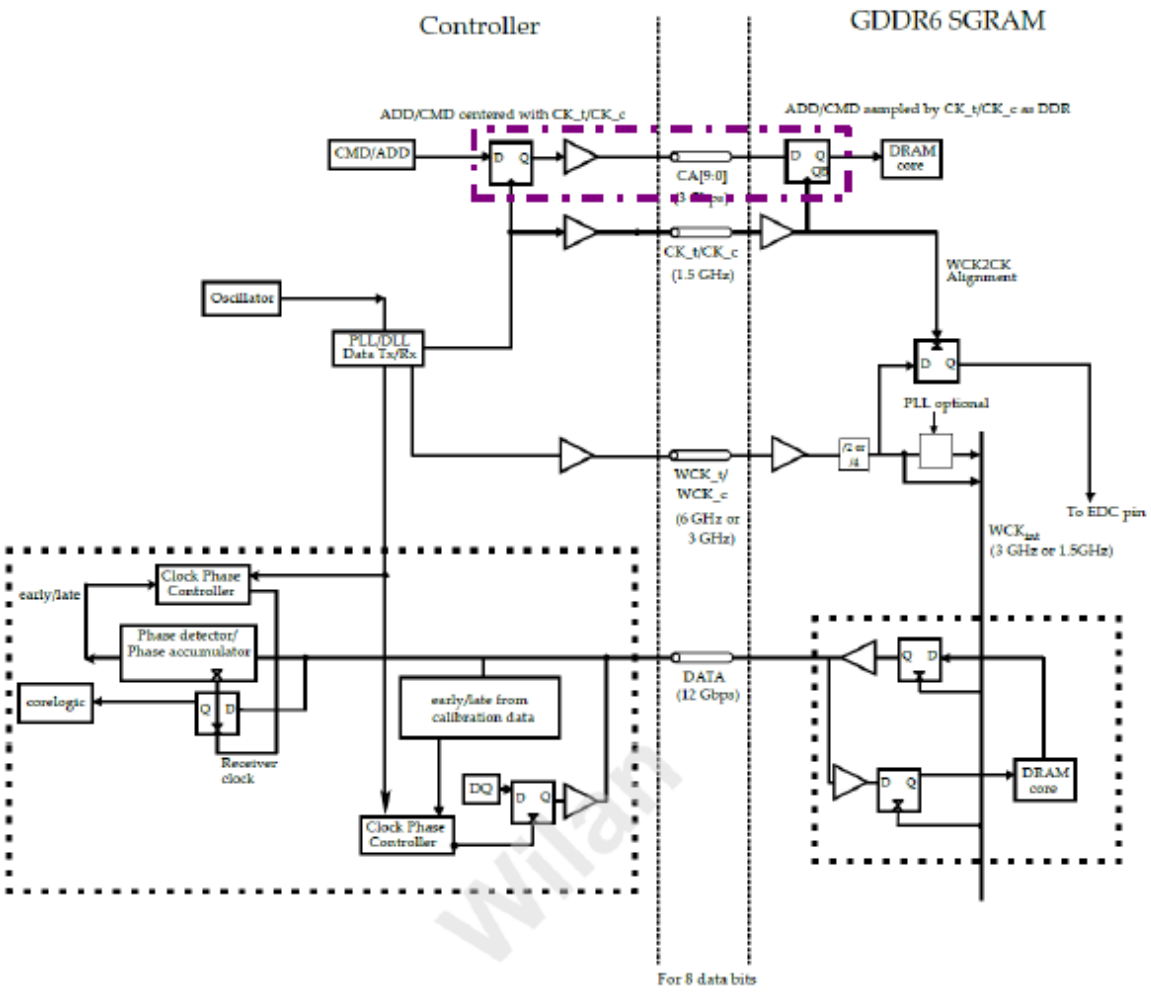


Figure 2 — Block Diagram of an example clock system

Source: JEDEC Standard Graphics Double Data Rate (GDDR6) SGRAM Standard JESD250B July 2017, Page 7

Indirect Infringement (Inducement – 35 U.S.C. § 271(b))

127. In addition and/or in the alternative to its direct infringements, Broadcom has indirectly infringed and continues to indirectly infringe one or more claims of the '976 Patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the '976 Accused Products.

128. At a minimum, Broadcom has knowledge of the '976 Patent since being served with this Complaint. Broadcom also has knowledge of the '976 Patent from Polaris's letter and accompanying claim charts sent prior to the filing of this suit. Since receiving notice of its infringements, Broadcom has actively induced the direct infringements of its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Such inducements have been committed with the knowledge, or with willful blindness to the fact, that the acts induced constitute infringement of the '976 Patent. On information and belief, Broadcom has intended to cause, continues to intend to cause, and has taken, and continues to take affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the '976 Accused Products; creating and/or maintaining established distribution channels for the '976 Accused Products into and within the United States; manufacturing the '976 Accused Products in conformity with U.S. laws and regulations; distributing or making available datasheets supporting use of the '976 Accused Products that promote their features, specifications, and applications; providing technical documentation and tools for the '976 Accused Products, such as white papers, brochures, and/or manuals; promoting the incorporation of the '976 Accused Products into end-user products, testing and certifying features related to memory systems in the '976 Accused Products; and/or by providing technical support and/or related services for these products to purchasers in the United States.

Damages

129. On information and belief, despite having knowledge of the '976 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the '976 Patent, Broadcom has nevertheless continued its infringing conduct and disregarded an objectively high

likelihood of infringement. Broadcom's infringing activities relative to the '976 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, characteristic of a pirate, and an egregious case of misconduct beyond typical infringement such that Polaris is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

130. Polaris has been damaged as a result of Broadcom's infringing conduct described in this Count. Broadcom is, thus, liable to Polaris in an amount that adequately compensates Polaris for Broadcom's infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

CONCLUSION

131. Polaris is entitled to recover from Broadcom the damages sustained by Polaris as a result of Broadcom's wrongful acts, and willful infringements, in an amount subject to proof at trial, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court.

132. Polaris has incurred and will incur attorneys' fees, costs, and expenses in the prosecution of this action. The circumstances of this dispute may give rise to an exceptional case within the meaning of 35 U.S.C. § 285, and Polaris is entitled to recover its reasonable and necessary attorneys' fees, costs, and expenses.

JURY DEMAND

133. Polaris hereby requests a trial by jury pursuant to Rule 38 of the Federal Rules of Civil Procedure.

PRAYER FOR RELIEF

134. Polaris respectfully requests that the Court find in its favor and against Broadcom, and that the Court grant Polaris the following relief:

(i) A judgment that one or more claims of the Asserted Patents have been infringed, either literally and/or under the doctrine of equivalents, by Defendant

(ii) A judgment that one or more claims of the Asserted Patents have been willfully infringed, either literally and/or under the doctrine of equivalents, by Defendant;

(iii) A judgment that Defendant account for and pay to Plaintiff all damages and costs incurred by Plaintiff because of Defendant's infringing activities and other conduct complained of herein, including an accounting for any sales or damages not presented at trial;

(iv) A judgment that Defendant account for and pay to Plaintiff a reasonable, ongoing, post judgment royalty because of Defendant's infringing activities, including continuing infringing activities, and other conduct complained of herein;

(v) A judgment that Plaintiff be granted pre-judgment and post judgment interest on the damages caused by Defendant's infringing activities and other conduct complained of herein;

(vi) A judgment that this case is exceptional under the provisions of 35 U.S.C. § 285 and award enhanced damages; and

(vii) Such other and further relief as the Court deems just and equitable.

Dated: September 7, 2022

Respectfully submitted,

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