IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF MASSACHUSETTS

Bell Semiconductor, LLC Plaintiff, v. NVidia Corporation, Defendant.	**Civil Action No. _____** **JURY TRIAL DEMANDED**

COMPLAINT

Plaintiff Bell Semiconductor, LLC ("Bell Semic" or "Plaintiff") brings this Complaint against Defendant NVidia Corporation ("NVidia") for infringement of U.S. Patent No. 7,396,760 ("the '760 patent") and U.S. Patent No. 6,436,807 ("the '807 patent"). Plaintiff, on personal knowledge of its own acts, and on information and belief as to all others based on investigation, alleges as follows:

SUMMARY OF THE ACTION

1. This is a patent infringement suit relating to NVidia's unauthorized and unlicensed use of the '760 and '807 patents. The circuit design methodologies claimed in the '760 and '807 patents are used by NVIDIA in the production of one or more of its semiconductor chips, including at least the NVIDIA GV100-400-A1 device ("NVidia Accused Product").

2. Semiconductor devices include different kinds of materials to function as intended. For example, these devices typically include both metal (i.e., conductor) and insulator materials, which are deposited or otherwise processed sequentially in layers to form the final device. These layers—and the interconnects and components formed within them—have gotten much smaller

over time, increasing the performance of these devices dramatically. As a result, it has become even more important to keep the layers planar as the device is being built because defects and warpage can cause fabrication issues and malfunctioning of the device. Manufacturers use a process called Chemical Mechanical Planarization/Polishing ("CMP") to smooth out the surface of the device to prepare the device for further processing, such as deposition of another layer. This allows subsequent layers to be built and connected more easily with fewer opportunities for short circuits or other errors that render the device defective. CMP functions best when there is a certain density and variance of the same material on the surface of the chip. This is because different materials will be "polished" away at different rates, leading to erosion or dishing on the surface. To reduce this problem "dummy" material, also known as "dummy fill," is typically inserted into low-density regions of the device to increase the overall uniformity of the structures on the surface of the layer and reduce the density variability across the surface of the device. However, dummy fill can increase capacitance if it is placed too close to signal wires, which slows the transmission speed of signals and degrades the overall performance of the device.

3. Prior to development of the methodology described in the '807 patent, the placement of dummy fill in the open areas of the interconnect layer was performed based upon a predetermined set density. However, use of predetermined set densities was not ideal because it often resulted in unnecessary placement of dummy fill and increased capacitance. For example, if the density of an active interconnect feature was high in relation to an adjacent open area, then it would not be necessary to place dummy fill in the corresponding open area at the predetermined density.

4. Recognizing these drawbacks, as well as the importance of having a flat or planarized surface on the devices, Donald Cwynar, Sudhanshu Misra, Dennis Ouma, Vivek

Saxena, and John Sharpe ("the '807 Inventors"), the inventors of the '807 patent, set out to develop a design process that would achieve uniform density throughout the interconnect layer.

5. The '807 Inventors ultimately conceived of a method for making the layout for an interconnect layout that allows for uniform density throughout the layer and facilitates planarization during manufacturing of the device. The claimed invention begins by determining an active interconnect feature density for each of a plurality of layout regions of the interconnect layout. Dummy fill is then added to each layout region in order to obtain a desired density of active interconnect features and dummy fill features in order to facilitate uniformity of planarization. In order to add dummy fill in this manner, one must define a minimum dummy fill feature lateral dimension based upon a dielectric layer deposition bias for a dielectric layer to be deposited over the interconnect layer.

6. The inventions disclosed in the '807 patent provide many advantages over the prior art. In particular, having a uniform density for each layout region facilitates uniformity of planarization during manufacturing of the semiconductor device. *See* Ex. D at 3:3-5, 5:9–12. Furthermore, adding dummy fill features to obtain a desired density of active interconnect features and dummy fill features also helps ensure that dummy fill features are not unnecessarily added. *Id.* at 2:63-67, 5:19-22. Avoiding unnecessary dummy fill features is desirable because it deceases the parasitic capacitance of the interconnect layer. *Id.* at 2:67-3:2, 5:22-24. The invention claimed in the '807 patent also provides for the selective positioning of dummy fill features, which minimizes parasitic capacitance. *Id.* at 5:28-33. These significant advantages are achieved through the use of the patented inventions and thus the '807 patent presents significant commercial value for companies like NVidia.

7. Traditionally, the process flow for IC design is highly linear, with each phase of the

design process depending on the previous steps. Accordingly, when revisions to portions of the physical design are made, as typically happens numerous times during the design process, all the subsequent steps typically need to be redone in their entirety for at least the layer, if not the entire device. This is because regardless of the size or extent of the revision to the physical design, the changes must be merged into a much larger integrated circuit design and then the remaining steps of the design process flow re-run.

8. Semiconductor devices include different kinds of materials to function as intended. For example, these devices typically include both metal (*i.e.*, conductor) and insulator materials, which are deposited or otherwise processed sequentially in layers to form the final device. These layers—and the interconnects and components formed within them—have gotten much smaller over time, increasing the performance of these devices dramatically. As a result, it has become even more important to keep the layers planar as the device is being built because defects and warpage can cause fabrication issues and malfunctioning of the device.

9. Manufacturers use a process called Chemical Mechanical Planarization/Polishing ("CMP") to smooth out the surface of the device to prepare the device for further processing, such as deposition of another layer. This allows subsequent layers to be built and connected more easily with fewer opportunities for short circuits or other errors that render the device defective. CMP functions best when there is a certain density and variance of the same material on the surface of the chip. This is because different materials will be "polished" away at different rates, leading to erosion or dishing on the surface.

10. To reduce this problem "dummy" material, also known as "dummy fill," is typically inserted into low-density regions of the device to increase the overall uniformity of the structures on the surface of the layer and reduce the density variability across the surface of the device.

However, dummy fill can increase capacitance if it is placed too close to signal wires, which slows the transmission speed of signals and degrades the overall performance of the device.

11. Just as unwanted capacitance can result from the interaction of elements within the layer of an integrated circuit, it can also result from interaction of elements across adjacent layers. While certain elements (such as signal lines and power lines) cannot be easily moved without affecting circuit performance, there is substantially more flexibility regarding placement, positioning, and spacing of non-signal carrying features such as dummy fill, even when certain quantities of dummy fill are needed within layers and portions of layers to meet processing requirements.

12. Prior to development of the methodology described in the '760 patent, the placement of dummy fill in the open areas of the interconnect layer was performed based primarily upon meeting density requirements. To the extent that timing and capacitance effects were considered in dummy fill dimensions, orientation, positioning, or otherwise in dummy fill placement, the conventional dummy fill tools at the time only considered intralayer effects—i.e., interactions between dummy fill features and other elements (such as signal nets) on that same layer. However, use of dummy fill that overlapped on successive layers could and often did create a substantial interlayer bulk capacitive effect that had a negative impact on circuit timing and performance, and which was not considered by the conventional dummy fill tools at the time even when they considered certain intralayer timing effects. *See* Ex. A at 1:43–2:6, 4:11–16.

13. Recognizing these drawbacks, as well as the importance of having a flat or planarized surface on the devices, the inventors of the '760 patent set out to develop a design process that would also consider the interlayer bulk capacitance created by overlapping dummy fill and consider those intralayer effects in arranging dummy fill in the chip layout so as to

minimize the unwanted bulk capacitance created by overlapping dummy fill features.

14. The inventors of the ’760 patent ultimately conceived of a method for addressing the interlayer capacitive effects of dummy fill by treating each successive set of layers as a pair and then rearranging the dummy fill in one or both layers so as to minimize their overlap. This was particularly advantageous in “intelligent dummy fill placement,” i.e., when timing impact is considered when placing dummy fill. *See* Ex. A at 2:10–19.

15. The inventions disclosed in the ’760 patent provide many advantages over the prior art. In particular, rearranging the dummy fill features such that they do not align vertically in successive layers can reduce unwanted bulk capacitance introduced by dummy fill and thus minimize the interlayer capacitance. *See* Ex. A at 2:45–48, 2:47–59, 3:30–33, 5:19–39. This removed unwanted bulk capacitance that would otherwise slow down signals in the circuit and adversely affect timing in the IC, thus improving its speed and performance. *See* Ex. A at 2:3–6. These significant advantages are achieved through the use of the patented inventions and thus the ’760 patent presents significant commercial value for companies like NVidia.

16. Bell Semic brings this action to put a stop to NVIdia’s unauthorized and unlicensed use of the inventions claimed in the ’760 and ’807 patents.

THE PARTIES

17. Plaintiff Bell Semic is a limited liability company organized under the laws of the State of Delaware with a place of business at One West Broad Street, Suite 901, Bethlehem, PA 18018.

18. Bell Semic stems from a long pedigree that began at Bell Labs. Bell Labs sprung out of the Bell System as a research and development laboratory, and eventually became known as one of America’s greatest technology incubators. Bell Labs employees invented the transistor

in 1947 in Murray Hill, New Jersey. It was widely considered one of the most important technological breakthroughs of the time, earning the inventors the Nobel Prize in Physics. Bell Labs made the first commercial transistors at a plant in Allentown, Pennsylvania. For decades, Bell Labs licensed its transistor patents to companies throughout the world, creating a technological boom that led to the use of transistors in the semiconductor devices prevalent in most electronic devices today.

19. Bell Semic, a successor to Bell Labs' pioneering efforts, owns over 1,900 worldwide patents and applications, approximately 1,500 of which are active United States patents. This patent portfolio of semiconductor–related inventions was developed over many years by some of the world's leading semiconductor companies, including Bell Labs, Lucent Technologies, Agere Systems, and LSI Logic and LSI Corporation ("LSI"). This portfolio reflects technology that underlies many important innovations in the development of semiconductors and integrated circuits for high–tech products, including smartphones, computers, wearables, digital signal processors, IoT devices, automobiles, broadband carrier access, switches, network processors, and wireless connectors.

20. The principals of Bell Semic all worked at Bell Labs' Allentown facility, and have continued the rich tradition of innovating, licensing, and helping the industry at large since those early days at Bell Labs. For example, Bell Semic's CTO was a LSI Fellow and Broadcom Fellow. He is known throughout the world as an innovator with more than 300 patents to his name, and he has a sterling reputation for helping semiconductor fabs improve their efficiency. Bell Semic's CEO took a brief hiatus from the semiconductor world to work with Nortel Networks in the telecom industry during its bankruptcy. His efforts saved the pensions of tens of thousands of Nortel retirees and employees. In addition, several Bell Semic executives previously served as

engineers at many of these companies and were personally involved in creating the ideas claimed throughout Bell Semic's extensive patent portfolio.

21. On information and belief, NVidia has its principal place of business and headquarters at 2788 San Tomas Expressway, Santa Clara, CA 95051.

22. On information and belief, NVidia develops, designs, and/or manufactures products in the United States, including in this District, according to the '760 and '807 patented processes/methodologies; and/or uses the '760 and '807 patented processes/methodologies in the United States, including in this District, to make products; and/or distributes, markets, sells, or offers to sell in the United States and/or imports products into the United States, including in this District, that were manufactured or otherwise produced using the patented process. Additionally, NVidia introduces those products into the stream of commerce knowing that they will be sold and/or used in this District and elsewhere in the United States.

JURISDICTION AND VENUE

23. This is an action for patent infringement arising under the Patent Laws of the United States, Title 35 of the United States Code. Accordingly, this Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

24. This Court has personal jurisdiction over NVIDIA under the laws of the State of Massachusetts, due at least to its substantial business in Massachussetts and in this District. NVIDIA has purposefully and voluntarily availed itself of the privileges of conducting business in the United States, in the State of Massachusetts, and in this District by continuously and systematically placing goods into the stream of commerce through an established distribution channel with the expectation that they will be purchased by consumers in this District. In the State of Massachusetts and in this District, NVIDIA, directly or through intermediaries: (i)

performs at least a portion of the infringements alleged herein; (ii) develops, designs, and/or manufactures products according to the '760 and '807 patented processes/methodologies; (iii) distributes, markets, sells, or offers to sell products formed according to the '760 and '807 patented processes/methodologies; and/or (iv) imports products formed according to the '760 and '807 patented processes/methodologies.

25. On information and belief, venue is proper in this Court pursuant to 28 U.S.C. §§ 1391 and 1400 because NVIDIA has committed, and continues to commit, acts of infringement in this District and has a regular and established place of business in this District. For example, NVidia maintains a regular and established place of business in both Westborough, Massachusetts and Westford, Massachusetts. *See* Our Locations, NVidia (available at https://www.nvidia.com/en-us/contact/?section=lo) (last visited November 4, 2022). Moreover, on information and belief, NVidia employs more than 40 engineers in Massachusetts. *See* Search Results for Current NVidia Employees, LinkedIn (available at https://www.linkedin.com/search/results/people/?currentCompany=%5B%223608%22%5D&geoUrn=%5B%22101098412%22%5D&keywords=nvidia%20engineer%20massachusetts&origin=FACETED_SEARCH&sid=5H%2C) (last visited November 4, 2022).

26. Currently, on information and belief, NVidia is advertising nearly 50 jobs in Massachusetts. *See Careers at NVidia,* NVidia (https://nvidia.wd5.myworkdayjobs.com/en-US/NVIDIAExternalCareerSite/jobs?locations=91336993fab910af6d6fe9a03534c248&locations=91336993fab910af6d7008ff1774c28e&locations=91336993fab910af6d702d89918cc2e3) (last visited November 4, 2022). These positions include those that relate to the '626 and '760 patented technologies, such as positions for a Senior SoC Architect, Director Custom SoC Chip Lead, and Senior Verification Engineer, SoC. *Id.*

27. Venue is also convenient in this District. This is at least true because of this District's close ties to this case—including the technology, relevant witnesses, and sources of proof noted above—and its ability to quickly and efficiently move this case to resolution.

28. On information and belief, Bell Semic's causes of action arise directly from NVidia's circuit design work and other activities in this District. Moreover, on information and belief, NVidia has derived substantial revenues from its infringing acts occurring within the State of NVidia and within this District.

U.S. PATENT NO. 7,396,760

29. Bell Semic is the owner by assignment of the '760 patent. The '760 patent is titled "Method and System for Reducing Inter-Layer Capacitance in Integrated Circuits."

30. A true and correct copy of the '760 patent is attached as Exhibit A.

31. The inventors of the '760 patent are Kunal Taravade, Neal Callan, and Paul Filseth.

32. The '760 patent issued on July 8, 2008 from an application filed on November 17, 2004.

33. The '760 patent generally relates to "a method for reducing inter-layer capacitance" in integrated circuits "through dummy fill methodology." Ex. A at 1:8–10.

34. The background section of the '760 patent identifies the shortcomings of the prior art. More specifically, the specification describes that the prior dummy fill methodologies were disadvantageous because they typically focused on achieving uniformity of feature density and failed to sufficiently address adverse effects of the dummy fill on electric field and unwanted bulk capacitance. *See* Ex. A at 1:62–66. In addition, these dummy fill methodologies only considered intralayer effects of dummy fill, to the extent that they considered timing impact at all. *See* Ex. A at 1:66–2:3. Thus, placement of dummy fill, even if advantageous on each

individual layer, could create problems when it overlapped with dummy fill features on successive layers, introducing an additional bulk capacitance component that could be substantial. *See id.* at 4:11–17, 4:25–28. These methodologies failed to consider interlayer effects such as those caused by the overlap of dummy fill features in successive layers, which could have a substantial negative impact on timing. *See id.* at 2:3–6.

35. In light of the drawbacks of the prior art, the inventors of the '760 patent recognized a need for "intelligent dummy fill placement to reduce interlayer capacitance caused by overlaps of dummy fill area on successive layers," which would also "treat[] each consecutive pair of layers together when the intelligent dummy filling placement is performed." Ex. A at 2:7–13. The inventions claimed in the '760 patent address this need.

36. The '760 patent contains two independent claims and 19 total claims. Claim 1 reads:

> 1. A method for placing dummy fill patterns in an integrated circuit fabrication process, comprising:
>
> obtaining layout information of the integrated circuit, the integrated circuit including a plurality of layers;
>
> obtaining a first dummy fill space for a first layer based on the layout information;
>
> obtaining a second dummy fill space for a second layer, the second layer being placed successively to the first layer;
>
> determining an overlap between the first dummy fill space and the second dummy fill space; and
>
> minimizing the overlap by re-arranging a plurality of first dummy fill features and a plurality of second dummy fill features,
>
> wherein the first dummy fill space includes non-signal carrying lines on the first layer and the second dummy fill space includes non-signal carrying lines on the second layer.

37. This claim, as a whole, provides significant benefits and improvements to the

function of the semiconductor device, *e.g.,* minimizing interlayer bulk capacitance and thus improving the timing characteristics and performance of the IC while meeting interconnect density requirements during processing. *See, e.g.*, Ex. A at 1:37–55, 5:19–39.

38. The claims of the ’760 patent also recite inventive concepts that improve the functioning of the fabrication process, particularly as to dummy filling. The claims of the ’760 patent disclose a new and novel solution to specific problems related to improving semiconductor fabrication. As explained in detail above and in the ’760 patent specification, the claimed inventions improve upon the prior art processes by considering successive layers rather than each layer on its own, and then determining the overlap between dummy fill features on successive layers before rearranging them to minimize their overlap and thus reduce interlayer bulk capacitance. This has advantages such as minimizing the parasitic capacitance of the interconnect layers, especially the bulk capacitance contributed by the interlayer effects of overlapping dummy fill features, while maintaining necessary interconnect density to meet fabrication requirements.

U.S. PATENT NO. 6,436,807

39. Bell Semic is the owner by assignment of the ’807 patent. The ’807 patent is titled “Method for Making an Interconnect Layer and a Semiconductor Device Including the Same.” The ’807 patent issued on August 20, 2002. A true and correct copy of the ’807 patent is attached as Exhibit D.

40. The inventors of the ’807 patent are Donald Cwynar, Sudhanshu Misra, Dennis Ouma, Vivek Saxena, and John Sharpe.

41. The application that resulted in the issuance of the ’807 patent was filed on January 18, 2000. The ’807 patent claims priority to January 18, 2000.

42. The ’807 patent generally relates to “a method for making a layout for an interconnect layer that has uniform density throughout to facilitate planarization during manufacturing of a semiconductor device.” Ex. D at 2:43-46. The background section of the ’807 patent identifies the shortcomings of the prior art. More specifically, the specification describes that the prior circuit design methodology was disadvantageous because it could lead to “protrusions[] in the upper surface of the dielectric material[] above respective active interconnect features[.]” *Id.* at 1:40-42. The specification states that “if pattern density variations of the active interconnect features[] are large, CMP is not adequate to sufficiently planarize the interconnect layer[.]” *Id.* at 1:67-2:2. Although “[c]onventional layout algorithms” were typically used to place dummy fill features in open areas of the interconnect layer, those algorithms placed dummy metal “based upon a predetermined set density.” *Id.* at 2:17-21. Relying on “predetermined set densit[ies]” could lead to the unnecessary placement of dummy fill features, which in turn could increase the parasitic capacitance of the interconnect layer. *Id.* at 2:31-33. The specification notes that “variations in the density of the interconnect layer [could] cause deviations when the interconnect layer [was] planarized.” *Id.* at 2:35-37.

43. In light of the drawbacks of the prior art, the ’807 Inventors recognized “a need for making a layout for an interconnect layer that determines placement of dummy fill features for achieving a uniform density throughout the interconnect layer.” Ex. D at 2:37–40. The inventions claimed in the ’807 patent address this need.

44. The ’807 patent contains two independent claims and 18 total claims. Claim 1 reads:

> 1. A method for making a layout for an interconnect layer of a semiconductor device to facilitate uniformity of planarization during manufacture of the semiconductor device, the method comprising the steps of:

> (a) determining an active interconnect feature density for each of a plurality of layout regions of the interconnect layout; and
>
> (b) adding dummy fill features to each layout region to obtain a desired density of active interconnect features and dummy fill features to facilitate uniformity of planarization during manufacturing of the semiconductor device, the adding comprising defining a minimum dummy fill feature lateral dimension based upon a dielectric layer deposition bias for a dielectric layer to be deposited over the interconnect layer.

45. This claim, as a whole, provides significant benefits and improvements to the function of the semiconductor device, *e.g.,* uniform planarization during manufacturing, avoidance of adding unnecessary dummy fill features, and minimizing parasitic capacitance. *See, e.g.*, Ex. D at 5:9–34.

46. The claims of the '807 patent also recite inventive concepts that improve the functioning of the fabrication process, particularly as to dummy filling. The claims of the '807 patent disclose a new and novel solution to specific problems related to improving semiconductor fabrication. As explained in detail above and in the '807 patent specification, the claimed inventions improve upon the prior art processes by determining an active interconnect feature density for each of a plurality of layout regions of the interconnect layout and adding dummy fill to each layout region to obtain a desired density of active interconnect features and dummy fill features to facilitate uniformity of planarization. This has advantages such as avoiding the unnecessary adding of dummy fill features and minimizing the parasitic capacitance of the interconnect layer.

COUNT I – INFRINGEMENT OF U.S. PATENT NO. 7,396,760

47. Bell Semic re-alleges and incorporates by reference the allegations of the foregoing paragraphs as if fully set forth herein.

48. The '760 patent is valid and enforceable under the United States Patent Laws.

49. Bell Semic owns, by assignment, all right, title, and interest in and to the '760 patent, including the right to collect for past damages.

50. A copy of the '760 patent is attached at Exhibit A.

51. On information and belief, NVidia has and continues to directly infringe pursuant to 35 U.S.C. § 271(a) one or more claims of the '760 patent by using the patented methodology to design one or more semiconductor devices, including by example the NVidia Accused Product, in the United States.

52. On information and belief, NVidia employs a variety of design tools, for example, Cadence, Synopsys, and/or Siemens tools, to rearrange dummy fill to minimize its overlap in successive layers (the "Accused Processes") as recited in the '760 patent claims. As one example, NVidia's Accused Processes allow arrangement and rearrangement of dummy fill in a timing aware fashion, including with the ability to stagger the dummy fill in successive layers so as to minimize the interlayer bulk capacitance after determining their overlap as required by claim 1 of the '760 patent. NVidia does so by employing a design tool, such as at least one of a Cadence, Synopsys, and/or Siemens tool, rearrange the dummy fill features in successive layers of its Accused Product.

53. NVidia's Accused Processes also form the dummy fill features in a grid within one or more of the successive layers, provide square-shaped dummy fill features in one or more of the successive layers, determine the dummy fill space based on a local pattern density in one or more of the successive layers, and minimize total bulk capacitance and/or certain of its components. NVidia does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, to implement dummy fill functionality in a timing-aware fashion and with consideration of interlayer capacitive effects in creation and design of its Accused

Product.

54. An exemplary infringement analysis showing infringement of one or more claims of the ’760 patent is set forth in Exhibit B. The declaration of Dhaval Brahmbhatt, an expert in the field of semiconductor device design, is attached at Exhibit C and further describes NVidia’s infringement of the ’760 patent.

55. NVidia’s Accused Processes infringe and continue to infringe one or more claims of the ’760 patent during the pendency of the ’760 patent.

56. On information and belief, NVidia has and continues to infringe directly pursuant to 35 U.S.C. § 271, *et. seq.*, either literally or under the doctrine of equivalents, by using the Accused Processes in violation of one or more claims of the ’760 patent. NVidia has and continues to infringe directly pursuant to 35 U.S.C. § 271, *et. seq.*, either literally or under the doctrine of equivalents, by making, selling, or offering to sell in the United States, or importing into the United States products manufactured or otherwise produced using the Accused Processes in violation of one or more claims of the ’760 patent.

57. NVidia’s infringement of the ’760 patent is exceptional and entitles Bell Semic to attorneys’ fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

58. Bell Semic has been damaged by NVidia’s infringement of the ’760 patent and will continue to be damaged unless NVidia is enjoined by this Court. Bell Semic has suffered and continues to suffer irreparable injury for which there is no adequate remedy at law. The balance of hardships favors Bell Semic, and public interest is not disserved by an injunction.

59. Bell Semic is entitled to recover from NVidia all damages that Bell Semic has sustained as a result of NVidia’s infringement of the ’760 patent, including without limitation and/or not less than a reasonable royalty.

COUNT II – INFRINGEMENT OF U.S. PATENT NO. 6,436,807

60. Bell Semic re-alleges and incorporates by reference the allegations of the foregoing paragraphs as if fully set forth herein.

61. The ’807 patent is valid and enforceable under the United States Patent Laws.

62. Bell Semic owns, by assignment, all right, title, and interest in and to the ’807 patent, including the right to collect for past damages.

63. A copy of the ’807 patent is attached at Exhibit D.

64. On information and belief, NVidia has and continues to directly infringe pursuant to 35 U.S.C. § 271(a) one or more claims of the ‘807 patent by using the patented methodology to design one or more semiconductor devices, including as one example the Accused Product, in the United States.

65. On information and belief, NVidia employs a variety of design tools, for example, Cadence, Synopsys, and/or Siemens tools, to make a layout for an interconnect layer of a semiconductor device (the “Accused Processes”) as recited in the ’807 patent claims. As one example, NVidia’s Accused Processes perform a method for making a layout for an interconnect layer of a semiconductor device, where the layout facilitates uniformity of planarization during manufacture of the semiconductor device as required by claim 1 of the ’807 patent. NVidia does so by employing a design tool, such as at least one of a Cadence, Synopsys, and/or Siemens tool, to make a layout for the interconnect layer of its Accused Product. The Accused Product’s layout facilitates uniformity of planarization during manufacture of the device.

66. NVidia’s Accused Processes also determine an active interconnect feature density for each of a plurality of layout regions of the interconnect layout. NVidia does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, to determine

an active interconnect feature density for each of a plurality of layout regions of the interconnect layout of its Accused Product.

67. NVidia's Accused Processes also add dummy fill features to each layout region to obtain a desired density of active interconnect features and dummy fill features to facilitate uniformity of planarization during manufacturing of the semiconductor device, the adding comprising defining a minimum dummy fill feature lateral dimension based upon a dielectric layer deposition bias for a dielectric layer to be deposited over the interconnect layer.

68. NVidia does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, to add dummy fill features to each layout region to obtain a desired density of active interconnect features and dummy fill features to facilitate uniformity of planarization during manufacturing of the semiconductor device. The adding of dummy fill through the use of these design tools comprises defining a minimum dummy fill feature lateral dimension based upon a dielectric layer deposition bias for a dielectric layer to be deposited over the interconnect layer. An exemplary infringement analysis showing infringement of one or more claims of the '807 patent is set forth in Exhibit E. The declaration of Lloyd Linder, an expert in the field of semiconductor device design, is attached at Exhibit F and further describes NVidia's infringement of the '807 patent.

69. NVidia's Accused Processes infringe and continue to infringe one or more claims of the '807 patent during the pendency of the '807 patent.

70. On information and belief, NVidia has and continues to infringe directly pursuant to 35 U.S.C. § 271, *et. seq.*, either literally or under the doctrine of equivalents, by using the Accused Processes in violation of one or more claims of the '807 patent. NVidia has and continues to infringe directly pursuant to 35 U.S.C. § 271, *et. seq.*, either literally or under the

doctrine of equivalents, by making, selling, or offering to sell in the United States, or importing into the United States products manufactured or otherwise produced using the Accused Processes in violation of one or more claims of the '807 patent.

71. NVidia's infringement of the '807 patent is exceptional and entitles Bell Semic to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

72. Bell Semic is entitled to recover from NVidia all damages that Bell Semic has sustained as a result of NVidia's infringement of the '807 patent, including without limitation and/or not less than a reasonable royalty.

PRAYER FOR RELIEF

WHEREFORE, Bell Semic respectfully requests that this Court enter judgment in its favor as follows and award Bell Semic the following relief:

(a) a judgment declaring that NVidia has infringed one or more claims of the '760 and '807 patents in this litigation pursuant to 35 U.S.C. § 271, *et seq.*;

(b) an award of damages adequate to compensate Bell Semic for infringement of the '760 and '807 patents by NVidia, in an amount to be proven at trial, including supplemental post-verdict damages until such time as NVidia ceases its infringing conduct;

(c) a permanent injunction, pursuant to 35 U.S.C. § 283, prohibiting NVidia and its officers, directors, employees, agents, consultants, contractors, suppliers, distributors, all affiliated entities, and all others acting in privity with NVidia from committing further acts of infringement with respect to the '760 patent;

(d) a judgment requiring NVidia to make an accounting of damages resulting from NVidia's infringement of the '760 and '807 patents;

(e) the costs of this action, as well as attorneys' fees as provided by 35 U.S.C. § 285;

(f) pre-judgment and post-judgment interest at the maximum amount permitted by law;

(g) all other relief, in law or equity, to which Bell Semic is entitled.

DEMAND FOR JURY TRIAL

Plaintiff hereby demands a jury trial for all issues so triable.

Dated: November 14, 2022

/s/ William F. McGonigle
Raymond P. Ausrotas (BBO #640315)
RAusrotas@arrowoodllp.com
William F. McGonigle (BBO #569490)
wmcgonigle@arrowoodllp.com
ARROWOOD LLP
10 Post Office Square,
7th Floor South
Boston, MA 02109
(617)849-6212

DEVLIN LAW FIRM LLC
1526 Gilpin Avenue
Wilmington, Delaware 19806
Telephone: (302) 449–9010
Facsimile: (302) 353–4251
Paul Richter (*pro hac vice* forthcoming)
prichter@devlinlawfirm.com

MCKOOL SMITH, P.C.
300 Crescent Court Suite 1500
Dallas, TX 75201
Telephone: (214) 978-4000
Telecopier: (214) 978-4044

David Sochia (*pro hac vice* forthcoming)
Texas State Bar No. 00797470
dsochia@McKoolSmith.com
Ashley N. Moore (*pro hac vice* forthcoming)
Texas State Bar No. 24074748
amoore@McKoolSmith.com
Richard A. Kamprath (*pro hac vice* forthcoming)
Texas State Bar No. 24078767
rkamprath@McKoolSmith.com
Alexandra Easley (*pro hac vice* forthcoming)
Texas State Bar No. 24099022
aeasley@McKoolSmith.com

Attorneys for Plaintiff Bell Semiconductor, LLC