UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
WACO DIVISION

ARIGNA TECHNOLOGY LIMITED, Plaintiff, vs. APPLE INC. Defendant.	Case No. 6:21-cv-943 JURY TRIAL DEMANDED

FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT

This is an action for patent infringement in which Arigna Technology Limited makes the following allegations against Defendant Apple Inc., which is a manufacturer and/or distributor that, without authority, imports, makes, offers for sale and/or sells in the United States mobile devices and computers that infringe the Patents asserted in this matter.

PARTIES

Arigna

1. Plaintiff Arigna Technology Limited ("Plaintiff" or "Arigna") is an Irish company conducting business at The Hyde Building, Carrickmines, Suite 23, Dublin 18, Ireland. Arigna owns a portfolio of patents that cover radio frequency amplifiers and circuits with applications in a wide variety of consumer electronics products, including smartphones and laptops, as well as power semiconductors for applications in the communications, automotive, industrial automation, and energy industries. Arigna is the owner of all rights, title, and interest in and to United States Patent No. 6,603,343 (the "'343 Patent") and United States Patent No. 8,947,164 (the "'164 Patent").

Apple

2. Defendant Apple Inc. ("Apple") is a corporation organized under the laws of the State of California with its headquarters at One Apple Park Way, Cupertino, California 95014. Apple

imports, makes, markets, distributes, offers for sale, and sells mobile devices, computers, and components under the Apple brand name in the United States.

3. Apple maintains regular and established offices in this District, including at 6900 W. Parmer Lane, Austin, Texas, and 12545 Riata Vista Circle, Austin, Texas.[1] Apple also owns and operates multiple retail stores in this District, including Apple stores in Austin and San Antonio.[2]

4. On information and belief, Apple has thousands of employees based in the Western District of Texas and does business in this District and across the State of Texas.[3] Apple's employees in Austin include Hardware Engineers,[4] Hardware Design Engineers,[5] and Hardware Design Verification Engineers.[6] Given the location of such Apple employees in Austin, on information and belief, documents and witnesses relevant to this action are located in this District.

5. Apple's website lists numerous job openings in its Austin offices, including for hardware engineering roles. For example, Apple has open positions in Austin for a "Silicon Validation Hardware Engineer – PCB CAD Layout" responsible for "circuit board design and layout,"[7] as well as a "Silicon Validation Hardware Engineer - Board Design" responsible for "circuit

---

[1] Apple, *Apple expands in Austin* (Nov. 20, 2019), available at https://www.apple.com/newsroom/2019/11/apple-expands-in-austin/.

[2] Apple, *Find a store* (accessed Aug 30, 2021), available at https://www.apple.com/retail/

[3] *Id.*

[4] *See, e.g.*, LinkedIn, *Hardware Engineer at Apple* (accessed Sept. 7, 2021), available at: https://www.linkedin.com/in/rakesh karmakar94713113b/?miniProfileUrn=urn%3Ali%3Afs_miniProfile%3AACoAACIDOwcBVUjwDcr652 z0ejpLVQQdzBLmsM4.

[5] *See, e.g.*, LinkedIn, *Hardware Design Engineer at Apple* (accessed Sept. 7, 2021), available at: https://www.linkedin.com/in/sandhya krishnakumar/?miniProfileUrn=urn%3Ali%3Afs_miniProfile%3AACoAACEyx0QBPPGR_8S1LGGCcq5BUtFLMvmHfx0.

[6] *See, e.g.*, LinkedIn, *Hardware Design Verification Engineer at Apple* (accessed Sept. 7, 2021), available at: https://www.linkedin.com/in/anand-saharan- 41833485/?miniProfileUrn

[7] Careers at Apple, *Silicon Validation Hardware Engineer - PCB CAD Layout* (accessed Sept. 7, 2021), available at: https://jobs.apple.com/en-us/details/200226046/silicon-validation-hardwareengineer-pcb-cad-layout.

design, defining routing constraints, layout review and simulation" and "[p]ower and signal integrity analysis."[8]

6. Apple has placed or contributed to placing infringing products like the iPhone 12 into the stream of commerce via established distribution channels knowing or understanding that such products would be sold and used in the United States, including in the Western District of Texas. Apple also has derived substantial revenue from infringing acts in the Western District of Texas, including from the sale and use of infringing products like the iPhone 12.

7. On information and belief, Apple designs, manufactures, distributes, imports, offers for sale, and/or sells in the State of Texas and the Western District of Texas mobile devices and computers that infringe the Patents asserted in this matter.

JURISDICTION AND VENUE

8. This is an action for patent infringement arising under the patent laws of the United States. This Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

9. This Court has personal jurisdiction over Apple because Apple conducts business in and has committed acts of patent infringement in this District, the State of Texas, and elsewhere in the United States and has established minimum contacts with this forum state such that the exercise of jurisdiction over Apple would not offend the traditional notions of fair play and substantial justice. Upon information and belief, Apple transacts substantial business with entities and individuals in the State of Texas and the Western District of Texas by, among other things, importing, offering to sell, distributing, and selling products that infringe the Asserted Patents, including the infringing mobile devices and computers that Apple purposefully directs into the State of Texas and this District as alleged herein, as well as by providing service and support to customers in this District. Apple places

[8] Careers at Apple, *Silicon Validation Hardware Engineer - Board Design* (accessed Sept. 7, 2021), available at: https://jobs.apple.com/en-us/details/200069399/silicon-validation-hardwareengineer-board-design.

the accused mobile devices and computers into the stream of commerce via authorized and established distribution channels with the knowledge and expectation that they will be sold in the United States, including in the State of Texas and this District, and does not otherwise permit the sale of the accused products in the State of Texas, or in this District, outside of these established, authorized, and ratified distribution channels.

10. Venue is proper in this District pursuant to 28 U.S.C. §§ 1391(b)-(c) and 1400(b), because Apple resides in this District and/or has committed acts of infringement in this District and has a regular and established place of business in this District.

11. Apple is subject to this Court's jurisdiction pursuant to due process and/or the Texas Long Arm Statute due at least to Apple's substantial business in the State of Texas and this District, including through its past infringing activities, because Apple regularly does and solicits business herein, and/or because Apple has engaged in persistent conduct and/or has derived substantial revenues from goods and services provided to customers in the State of Texas and this District.

THE ASSERTED PATENTS

This complaint asserts causes of action for infringement of United States Patent No. 6,603,343 and United States Patent No. 8,947,164 (together, the "Asserted Patents"). The Asserted Patents are valid and enforceable United States Patents, the entire right, title, and interest to which Arigna owns by assignment.

12. The Asserted Patents relate to power semiconductor devices using high-frequency RF signals for use in mobile devices, including smartphones, tablets, and computers.

13. On August 5, 2003, the U.S. Patent and Trademark Office duly and legally issued the '343 Patent, which is entitled "Phase Correction Circuit for Transistor Using High-Frequency Signal." Plaintiff holds all rights and title to the '343 Patent, including the sole and exclusive right to bring a claim for its infringement. A true and correct copy of the '343 Patent is attached as **Exhibit**

A.

14. The ’343 Patent generally claims a phase correction circuit for a transistor using a high-frequency signal. The claimed phase correction circuit stabilizes a phase of an output signal of a transistor even if the transistor’s gate potential is increased by a temperature increase or other factors.

15. To the extent applicable, Plaintiff has complied with 35 U.S.C. § 287(a) with respect to the ’343 Patent.

16. On February 3, 2015, the U.S. Patent and Trademark Office duly and legally issued the ’164 Patent, which is entitled “Integrated Technique for Enhanced Power Amplifier Forward Power Detection.” Plaintiff holds all rights and title to the ’164 Patent, including the sole and exclusive right to bring a claim for its infringement. A true and correct copy of the ’164 Patent is attached as **Exhibit B**.

17. The ’164 Patent generally claims a method for accurate power detection in power amplifiers at a low cost, and in which the power detector’s design does not affect the design of the power amplifier.

18. To the extent applicable, Plaintiff has complied with 35 U.S.C. § 287(a) with respect to the ’164 Patent.

19. Plaintiff owns all rights, title, and interest in and to the Asserted Patents and possesses all rights of recovery.

FACTUAL ALLEGATIONS

20. As referred to in this Complaint, and consistent with 35 U.S.C. § 100(c), the “United States” means “the United States of America, its territories and possessions.”

21. Apple does not have any right to practice the intellectual property protected by the Asserted Patents.

22. Apple makes, uses, offers to sell, sells, and/or imports into the United States products

made in accordance with the ’343 Patent, including but not limited to the Apple iPhone 12, Apple iPhone 12 Pro, Apple iPhone 12 Pro Max, and iPhone 12 mini, iPhone 13, iPhone 13 Pro, iPhone 13 Pro Max, iPhone 13 mini, iPhone 14, iPhone 14 Plus, iPhone 14 Pro, iPhone 14 Pro Max, iPad Pro 5th Gen (12.9”) (wifi + cell), iPad Pro 5th Gen (11”) (wifi + cell), iPad Pro 3rd Gen (11”) (A2301), iPad Pro 3rd Gen (11”) (A2379), in addition to other mobile devices and computers.

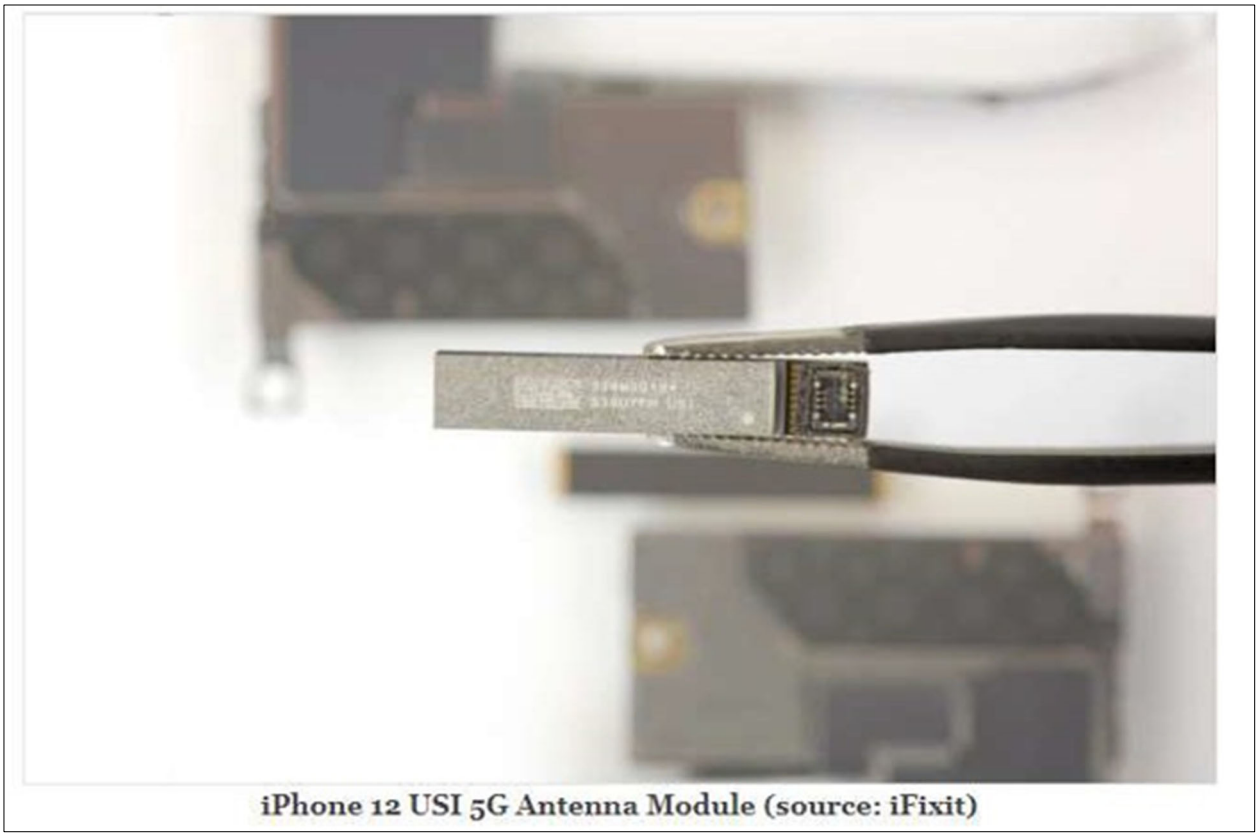
23. Apple makes, uses, offers to sell, sells, and/or imports into the United States products made in accordance with the ’164 Patent, including but not limited to the Apple iPhone 12, Apple iPhone 12 Pro, Apple iPhone 12 Pro Max, and iPhone 12 mini, iPhone 13, iPhone 13 Pro, iPhone 13 Pro Max, iPhone 13 mini, iPhone 14, iPhone 14 Plus, iPhone 14 Pro, iPhone 14 Pro Max, iPhone SE (3rd Gen), iPad Pro 5th Gen (12.9”) (wifi + cell), iPad Pro 5th Gen (11”) (wifi + cell), iPad Pro 3rd Gen (11”) (A2301), iPad Pro 3rd Gen (11”) (A2379), iPad mini 6th Gen (wifi + cell), in addition to other mobile devices and computers.

COUNT ONE
INFRINGEMENT OF U.S. PATENT NO. 6,603,343

24. Apple has infringed and continues to infringe at least claim 1 of the ’343 Patent in violation of 35 U.S.C. § 271, either literally or through the doctrine of equivalents, by making, using, selling, or offering for sale in the United States, and/or importing into the United States, without authorization, products that practice at least claim 1 of the ’343 Patent. Apple is liable for its infringement of the ’343 Patent pursuant to 35 U.S.C. § 271(a), (b), and (c).

25. More specifically, Apple designs, manufactures, assembles, imports, offers for sale, and/or sells mobile devices that incorporate the HG11-PG660-200 RF die semiconductor device, which infringes at least independent claim 1 of the ’343 Patent. For example, the HG11-PG660-200 RF die is found inside the Universal Scientific Industrial 339M00104 semiconductor device, which comes pre-installed in at least the Apple iPhone 12 Pro Max.

FIGURE 1

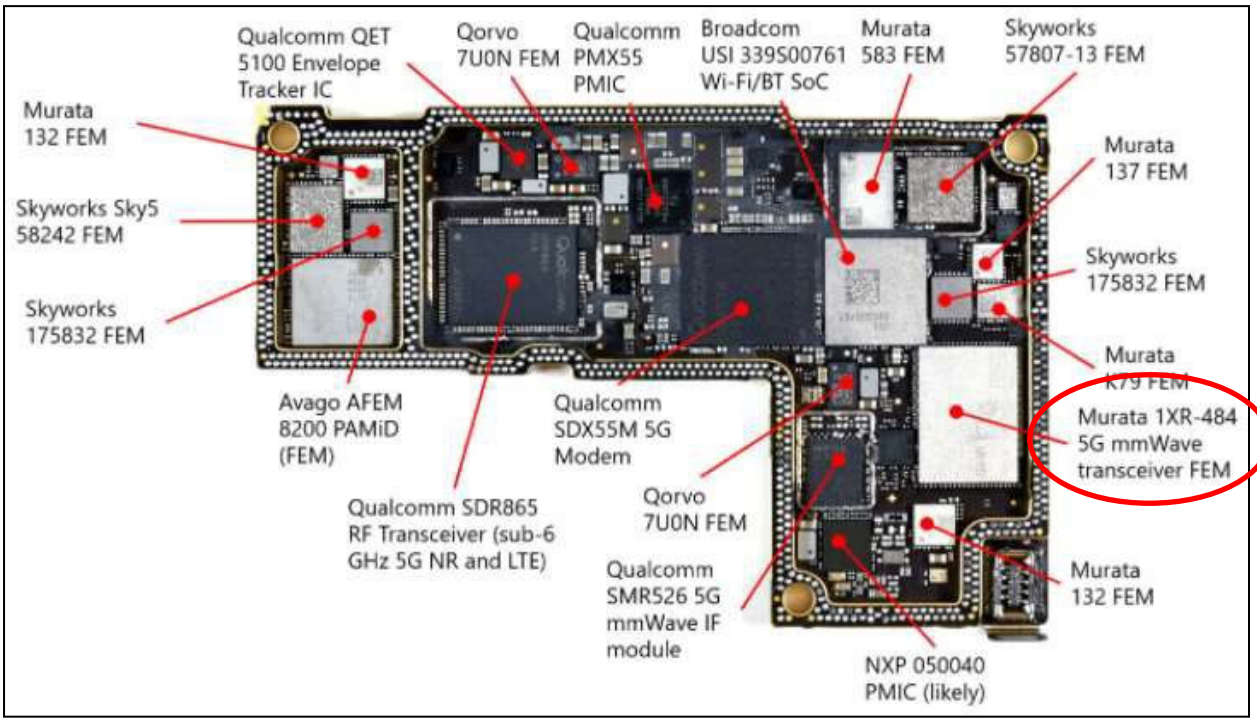


iPhone 12 USI 5G Antenna Module (source: iFixit)

Source: EE Times, *5G iPhone: What's Apple's Next Step in RF, Antenna?* (Oct. 29, 2020), available at: https://www.eetimes.com/5g-iphone-whats-apples-next-step-in-rf-antenna/#

26. Likewise, the HG11-PG660-200 RF die is found inside the Qualcomm SMR525 semiconductor device, which comes pre-installed in at least the Apple iPhone 12 Pro. As another example, and as shown in Figure 2, the HG11-PG660-200 RF die is found inside the Murata 1XR- 484 front-end module, which comes pre-installed in at least the Apple iPhone 12 and iPhone 12 Pro Max.

FIGURE 2



Source: UnitedLex, *Apple iPhone 12 Pro Max Teardown Report* (accessed Sept. 6, 2021), available at: https://unitedlex.com/insights/apple-iphone-12-pro-max-teardown-report.

27. Claim 1 is illustrative of the '343 Patent. It recites "[a] phase correction circuit for a transistor, comprising: a circuit element having an output terminal connected to a gate of a transistor to which a control signal line is connected, and an input terminal, wherein the circuit element has a reactance that changes with potential difference between the input terminal and the output terminal; and a voltage control circuit supplying a voltage to the input terminal of the circuit element so that the reactance of the circuit element decreases in response to an increase in potential of the gate, wherein a sum of the reactance of the circuit element and a gate-source reactance of the transistor remains substantially constant."

28. Devices with transceivers, antenna modules, front-end modules (FEMs), and/or other components which incorporate the HG11-PG660-200 RF die meet every element of this claim.[9] The

[9] This description of infringement is illustrative and not intended to be an exhaustive or limiting explanation of every manner in which Apple's products infringe the '343 Patent.

HG11-PG660-200 RF die contains a phase correction circuit for a transistor. For example, the transmitter portion of the HG11-PG660-200 RF die contains transistors with a phase correction circuit. For instance, a circuit element in the HG11-PG660-200 RF die (hereafter called "MOS-C") forms part of a phase correction circuitry for a transistor in the HG11-PG660-200 RF die (hereafter called "MOS7").

29. This phase correction circuit contains a circuit element having an output terminal connected to a gate of a transistor to which a control signal line is connected. For example, in the HG11-PG660-200 RF die, the circuit element MOS-C has an output terminal connected to a gate of the MOS7 transistor. It also has an input terminal.

30. A control signal line is also connected to the gate of the transistor. For example, a control signal line is connected to the gate of the MOS7 transistor through a passive bias network.

31. The circuit element has a reactance that changes with potential difference between the input terminal and the output terminal. For example, the identified MOS-C circuit element is an NMOS Field Effect Transistor whose source and drain are connected. MOS-C acts as a varactor whose capacitance (and thus reactance) changes according to the potential difference between the input terminal (drain and source node) and the output terminal (gate node).

32. This phase correction circuit in the HG11-PG660-200 RF die also contains a voltage control circuit supplying a voltage to the input terminal of the circuit element so that the reactance of the circuit element decreases in response to an increase in the potential of the gate. For example, another transistor in the HG11-PG660-200 RF die forms part of the voltage control circuit supplying a voltage to the input terminal of the circuit element MOS-C.

33. The reactance of the circuit element decreases in response to an increase in potential of the gate, wherein a sum of the reactance of the circuit element and a gate-source reactance of the transistor remains substantially constant. For example, when the magnitude of the gate-source

potential at MOS7 increases, it leads to a reduction in the capacitance of the circuit element (MOS-C). As the gate potential of the MOS7 gets more negative (i.e., the magnitude of gate-source potential increases), the gate-source capacitance of transistor MOS7 increases. This increase is offset, however, by the decrease in the capacitance of the circuit element (MOS-C) that occurs due to the increase in the magnitude of the gate potential of MOS7 such that the sum of capacitance (i.e. reactance) of the circuit element (MOS-C) and transistor (MOS7) remains substantially constant.

34. Apple makes, uses, imports, offers for sale, and/or sells mobile devices, such as smartphones, that incorporate the HG11-PG660-200 RF die in their antenna modules, including but not limited to the iPhone 12, iPhone 12 Mini, iPhone 12 Pro, and iPhone 12 Pro Max.

35. Apple has imported and sold, and continues to sell and offer for sale, these infringing mobile devices in the United States, including through the Apple website (Apple.com) and at Apple stores in Austin and San Antonio, among other places in the Western District of Texas.

36. Apple committed and is committing the foregoing infringing activities without license from Arigna. Apple's acts of infringement have damaged Arigna, as owner and assignee of the '343 Patent. Arigna is entitled to recover from Apple the damages it has sustained as a result of Apple's wrongful acts in an amount subject to proof at trial. Apple's infringement of Arigna's rights under the '343 Patent is ongoing and will continue to damage Arigna.

37. Apple has had actual knowledge of the '343 Patent and Arigna's allegations of Apple's infringement of the '343 Patent since no later than September 10, 2021. Apple's continued infringement despite its knowledge of the '343 Patent and Arigna's infringement allegations, is intentional and deliberate and willful.

38. Despite having knowledge of its infringement of the '343 Patent since no later than September 10, 2021, Apple has taken no remedial action to stop or mitigate that infringement, further demonstrating Apple's disregard for Arigna's patent rights.

39. Apple has not switched to any alleged non-infringing alternatives in its Accused Products. Nor has Apple made any design-around efforts to cease its infringement of the '343 Patent.

40. Further, despite requests from Arigna that Apple abate its infringement and take a license to the '343 Patent, Apple has unreasonably rejected such non-exclusive licensing offers and has decided instead to continue its willful infringement of the '343 Patent, further demonstrating Apple's intentional disregard of Arigna's patent rights.

41. Not only has Apple not ceased to make, use, import, offer for sale, and/or sell the Apple devices that Arigna accused of infringement on September 10, 2021, but—with full knowledge of its infringement and lack of any reasonable defense thereto—Apple has also doubled-down on its use of the infringing technology by making, using, importing, offering for sale, and/or selling additional infringing products that were not on the market when Apple first became aware of its infringement of the '343 Patent.[10] For example, Apple has released at least two new lines of Apple iPhones since September 10, 2021,[11] and in each case, Apple has intentionally and deliberately chosen to incorporate Arigna's patented technology into those iPhones—given the substantial benefits they provide to Apple and its consumers—despite knowing that Apple had no legal right to do so and without seeking a license from Arigna. Apple's so-called "efficient infringement" and willful sale of tens or even hundreds of millions of these latest infringing devices is deliberate and intentional and willful.

---

[10] *E.g.*, United Lex, *Apple iPhone 13 Pro Max Teardown Report* (accessed Nov. 16, 2022), available at https://unitedlex.com/insights/apple-iphone-13-pro-max-teardown-report/; iFixit, *iPhone 14 Pro Max Chip ID* (accessed November 16, 2022), available at https://www.ifixit.com/Guide/iPhone+14+Pro+Max+Chip+ID/153224.

[11] Rado Minkov, *iPhone 13 Release Date, Price and Features*, Phone Arena (updated Sept. 12, 2022), available at https://www.phonearena.com/apple-iphone-13-release-date-price-features#:~:text=The%20iPhone%2013%20was%20announced,shortly%20after%20%E2%80%93%20on%20September%2024; Peter Kostadinov, *Apple iPhone 14 Release Date, Price and Features*, Phone Arena (updated Nov. 4, 2022), available at https://www.phonearena.com/iphone-14-release-date-price-features.

42. Apple's made-for-litigation defenses are not reasonable or meritorious, and Apple's subjective knowledge that it lacks reasonable defenses, as to infringement and validity and otherwise, further supports a finding that Apple's infringement has been willful.

43. Apple's litigation misconduct further demonstrates that its infringement is willful. Apple has used unfair tactics and gamesmanship throughout the discovery process in an attempt to gain a litigation advantage, or otherwise "punish" Arigna for enforcing its patent rights. For example, Apple has engaged in sanctionable misconduct by willfully disregarding the Federal Rules and failing to appear for a corporate deposition, after filing a meritless transfer motion and venue declaration of questionable veracity.[12] Other examples abound, including that Apple failed to comply with this Court's requirements to produce its technical documents, including software where applicable, sufficient to show the operation of the accused product(s) by March 3, 2022—indeed, Apple has yet to comply with that obligation, more than eight months later. In an obvious attempt to frustrate Arigna's enforcement of its patent rights, and to increase the time and expense of Arigna doing so, Apple instead produced hundreds of thousands of publicly available and completely irrelevant documents concerning features that have nothing to do with the accused functionality.

44. Apple's conduct since no later than September 10, 2022, amounts to intentional, deliberate, and willful infringement of the '343 Patent.

COUNT TWO
INFRINGEMENT OF U.S. PATENT NO. 8,947,164

45. Plaintiff repeats and incorporates by reference each preceding paragraph as if fully set forth herein and further states:

46. Apple has infringed and continues to infringe at least claim 1 of the '164 Patent in violation of 35 U.S.C. § 271, either literally or through the doctrine of equivalents, by making, using,

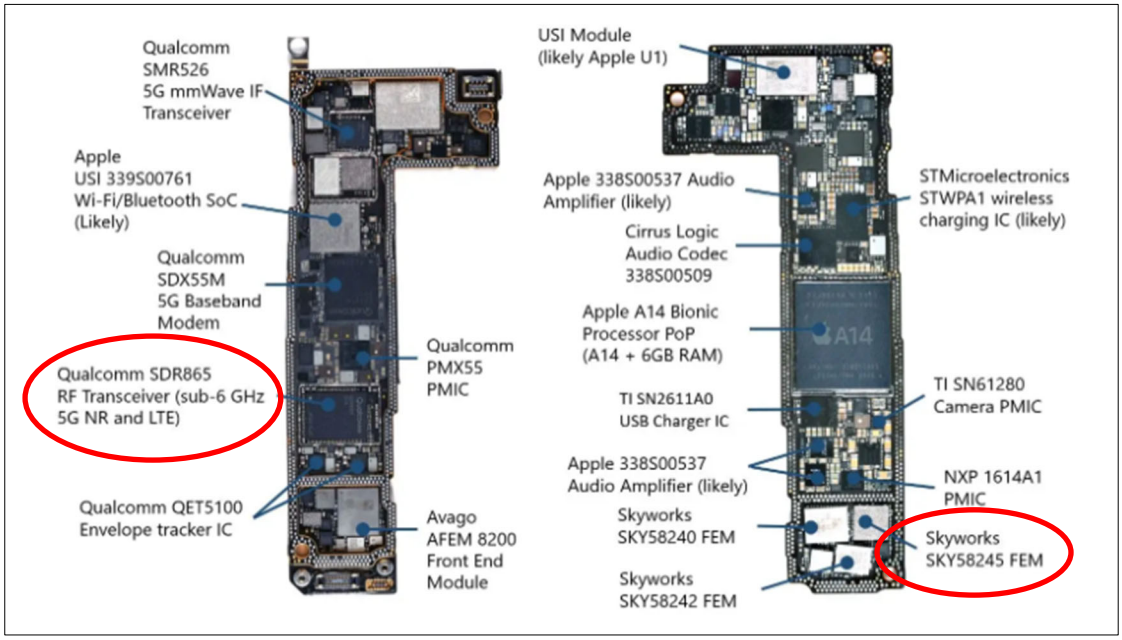
[12] *See* Order Granting Motion for Sanctions Against Apple (July 20, 2022) (Dkt. 107).

selling, or offering for sale in the United States, and/or importing into the United States, without authorization, products that practice at least claim 1 of the '164 Patent. Apple is liable for its infringement of the '164 Patent pursuant to 35 U.S.C. § 271(a), (b), and (c).

47. More specifically, Apple designs, manufactures, assembles, imports, offers for sale, and/or sells mobile devices that incorporate the Qualcomm SDR865 transceiver and Skyworks SKY58245-19 front-end module, and/or other components, which infringe at least independent claim 1 of the '164 Patent.

48. For example, the SDR865 transceiver and SKY58245-19 front-end module come preinstalled in certain Apple mobile devices, including the iPhone 12 Pro, as shown in Figure 3.

FIGURE 3



Source: United Lex, *Apple iPhone 12 Pro 5G mmWave Report* (accessed November 16, 2022), available at: https://unitedlex.com/insights/apple-iphone-12-pro-5g-mmwave-report.

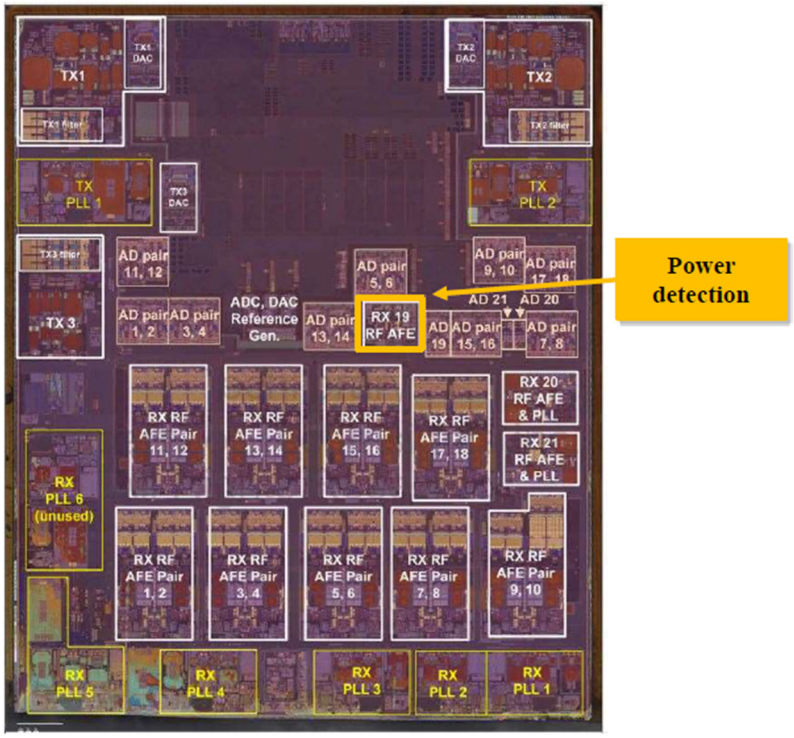
49. Claim 1 is illustrative of the '164 Patent. It recites "[a] power amplifier with power detection, comprising: a radio frequency (RF) power amplifier having a gain stage that includes a gain stage input, a gain stage output, and a feedback loop coupled between an input and an output of the power amplifier; a detection circuit having a first detection circuit input electrically coupled to the gain

stage input and having a detection circuit output; an amplitude control circuit and a phase control circuit electrically coupled together in series between the gain stage output and a second detection circuit input; wherein the amplitude control circuit and the phase control circuit produce a signal received by the second detection circuit input so that the detection circuit detects a signal at the output of the detection circuit that has a power proportional to a forward power output of the power amplifier."

50. The SDR865 transceiver and SKY58245-19 front-end module, as installed in various Apple products, meet every element of this claim.[13]

51. A power amplifier is present in the SKY58245-19 with power detection provided by the SDR865. For example, the RX19 RF AFE identified in Figure 4 is part of a feedback receiver in the SDR865 that carries out a power detection function.

FIGURE 4



[13] This description of infringement is illustrative and not intended to be an exhaustive or limiting explanation of every manner in which Apple's products infringe the '164 Patent.

Source: Tech Insights, *Analysis of Qualcomm's Snapdragon SDR865 Transceiver* (accessed Sept. 6, 2021) available at: https://www.techinsights.com/blog/analysis-qualcomms-snapdragonsdr865-transceiver-supporting-5g-sub-6-ghz-and-lte-services

52. The SKY58245-19 front-end module contains a radio frequency (RF) power amplifier having a gain stage that includes a gain stage input and a gain stage output. On information and belief, a feedback loop is coupled between an input and an output of the power amplifier.

53. The SDR865 contains a detection circuit, which has a first detection circuit input electrically coupled to the gain stage input and having a detection circuit output. For example, the gain stage input of the power amplifier in the SKY58245-19 is electrically coupled to a first detection circuit input in the SDR865. For instance, in the Apple iPhone 12 Pro Max, TXRFPAD(7) and TXRFPAD(8) on the first detection circuit in the SDR865 are electrically coupled to the gain stage input of the power amplifier in the SKY58245-19.

54. The SDR865 and SKY58245-19 also contain an amplitude control circuit and a phase control circuit electrically coupled together in series between the gain stage output and a second detection circuit input. The phase control circuit consists of an inductor and a capacitor in series with a low noise amplifier acting as an amplitude control circuit.

55. The amplitude control circuit and the phase control circuit produce a signal received by the second detection circuit input so that the detection circuit detects a signal at the output of the detection circuit that has a power proportional to a forward power output of the power amplifier. For example, the amplitude and phase control circuit produce a signal that is received into the mixer of the detection circuit (second input). The mixer also receives a LO signal (first input) and the result is used to estimate the forward power output of the power amplifier in the front-end module.

56. Apple makes, uses, imports, offers for sale, and/or sells mobile devices that incorporate the combination of SDR865 and SKY58245-19 components, including but not limited to the iPhone 12, iPhone 12 Mini, iPhone 12 Pro, and iPhone 12 Pro Max.

57. Apple has imported and sold, and continues to sell and offer for sale, these infringing mobile devices in the United States, including through the Apple website (Apple.com) and at Apple stores in Austin and San Antonio, among other places in the Western District of Texas.

58. Apple committed and is committing the foregoing infringing activities without license from Arigna. Apple's acts of infringement have damaged Arigna, as owner and assignee of the '164 Patent. Arigna is entitled to recover from Apple the damages it has sustained as a result of Apple's wrongful acts in an amount subject to proof at trial. Apple's infringement of Arigna's rights under the '164 Patent will continue to damage Arigna.

59. Apple has had actual knowledge of the '164 Patent and Arigna's allegations of Apple's infringement of the '164 Patent since no later than September 10, 2021. Apple's continued infringement despite its knowledge of the '164 Patent and Arigna's infringement allegations, is intentional and deliberate and willful.

60. Despite having knowledge of its infringement of the '164 Patent since no later than September 10, 2021, Apple has taken no remedial action to stop or mitigate that infringement, further demonstrating Apple's disregard for Arigna's patent rights.

61. Apple has not switched to any alleged non-infringing alternatives in its Accused Products. Nor has Apple made any design-around efforts to cease its infringement of the '164 Patent.

62. Further, despite requests from Arigna that Apple abate its infringement and take a license to the '164 Patent, Apple has unreasonably rejected such non-exclusive licensing offers and has decided instead to continue its willful infringement of the '164 Patent, further demonstrating Apple's intentional disregard of Arigna's patent rights.

63. Not only has Apple not ceased to make, use, import, offer for sale, and/or sell the Apple devices that Arigna accused of infringement on September 10, 2021, but—with full knowledge of its infringement and lack of any reasonable defense thereto—Apple has also doubled-down on its

use of the infringing technology by making, using, importing, offering for sale, and/or selling additional infringing products that were not on the market when Apple first became aware of its infringement of the '164 Patent.[14] For example, Apple has released at least two new lines of Apple iPhones since September 10, 2021,[15] and in each case, Apple has intentionally and deliberately chosen to incorporate Arigna's patented technology into those iPhones—given the substantial benefits they provide to Apple and its consumers—despite knowing that Apple had no legal right to do so and without seeking a license from Arigna. Apple's so-called "efficient infringement" and willful sale of tens or even hundreds of millions of these latest infringing devices is deliberate and intentional and willful.

64. Apple's made-for-litigation defenses are not reasonable or meritorious, and Apple's subjective knowledge that it lacks reasonable defenses, as to infringement and validity and otherwise, further supports a finding that Apple's infringement has been willful.

65. Apple's litigation misconduct further demonstrates that its infringement is willful. Apple has used unfair tactics and gamesmanship throughout the discovery process in an attempt to gain a litigation advantage, or otherwise "punish" Arigna for enforcing its patent rights. For example, Apple has engaged in sanctionable misconduct by willfully disregarding the Federal Rules and failing to appear for a corporate deposition, after filing a meritless transfer motion and venue declaration of

[14] *E.g.*, United Lex, *Apple iPhone 13 Pro Max Teardown Report* (accessed Nov. 16, 2022), available at https://unitedlex.com/insights/apple-iphone-13-pro-max-teardown-report/; iFixit, *iPhone 14 Pro Max Chip ID* (accessed November 16, 2022), available at https://www.ifixit.com/Guide/iPhone+14+Pro+Max+Chip+ID/153224.

[15] Rado Minkov, *iPhone 13 Release Date, Price and Features*, Phone Arena (updated Sept. 12, 2022), available at https://www.phonearena.com/apple-iphone-13-release-date-price-features#:~:text=The%20iPhone%2013%20was%20announced,shortly%20after%20%E2%80%93%20on%20September%2024; Peter Kostadinov, *Apple iPhone 14 Release Date, Price and Features*, Phone Arena (updated Nov. 4, 2022), available at https://www.phonearena.com/iphone-14-release-date-price-features.

questionable veracity.[16] Other examples abound, including that Apple failed to comply with this Court's requirements to produce its technical documents, including software where applicable, sufficient to show the operation of the accused product(s) by March 3, 2022—indeed, Apple has yet to comply with that obligation, more than eight months later. In an obvious attempt to frustrate Arigna's enforcement of its patent rights, and to increase the time and expense of Arigna doing so, Apple instead produced hundreds of thousands of publicly available and completely irrelevant documents concerning features that have nothing to do with the accused functionality.

66. The

67. Apple's conduct since no later than September 10, 2022, amounts to intentional, deliberate, and willful infringement of the '164 Patent.

DEMAND FOR JURY TRIAL

68. Plaintiff Arigna hereby demands a jury trial for all issues so triable.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff Arigna Technology Limited requests entry of judgment in its favor and against Defendant Apple as follows:

A. Declaring that Apple has infringed United States Patent No. 6,603,343;

B. Declaring that Apple has infringed United States Patent No. 8,947,164;

C. Declaring that Apple's infringement of United States Patent No. 6,603,343 has been willful and deliberate, at least from the filing of Arigna's Original Complaint on September 10, 2021;

D. Declaring that Apple's infringement of United States Patent No. 8,947,164 has been willful and deliberate, at least from the filing of Arigna's Original Complaint on September 10, 2021;

E. Awarding damages to Plaintiff in an amount no less than a reasonable royalty for Apple's infringement of United States Patent No. 6,603,343 and United States Patent No. 8,947,164,

[16] *See* Order Granting Motion for Sanctions Against Apple (July 20, 2022) (Dkt. 107).

together with treble damages for willful infringement, prejudgment and post-judgment interest, and costs as permitted under 35 U.S.C. § 284;

F. Awarding attorneys' fees pursuant to 35 U.S.C. § 285 or as otherwise permitted by law;

G. Ordering Apple to pay supplemental damages to Arigna, including any ongoing royalties and interest, with an accounting, as needed; and

H. Awarding such other costs and further relief as the Court may deem just and proper.

Dated: November 17, 2022

Respectfully submitted,

/s/ Matthew R. Berry

Charles L. Ainsworth (Texas 00783521)
charley@pbatyler.com
Robert Christopher Bunt (Texas 00787165)
rcbunt@pbatyler.com
PARKER, BUNT & AINSWORTH, P.C.
100 East Ferguson, Suite 418
Tyler, Texas 75702
Tel: (903) 531-3535

Matthew R. Berry (Washington 37364)
mberry@susmangodfrey.com
Andres Healy (Washington 45578)
ahealy@susmangodfrey.com
John E. Schiltz (Washington 48973)
jschiltz@susmangodfrey.com
Kemper Diehl (Washington 53212)
kdiehl@susmanodfrey.com
SUSMAN GODFREY L.L.P.
1201 Third Avenue, Suite 3800
Seattle, WA 98101-3000
Tel: (206) 516-3880
Fax: (206) 516-3883

Amy V. Hall (Texas 24123368)
ahall@susmangodfrey.com
Bryce Barcelo (Texas 24092081)
bbarcelo@susmangodfrey.com
SUSMAN GODFREY L.L.P.
1000 Louisiana St., Ste. 5100
Houston, TX 77002
Tel: (713) 651-9366

Fax: (713) 654-6666

Attorneys for Arigna Technology Limited

CERTIFICATE OF SERVICE

I certify that on November 17, 2022, a copy of the foregoing document was served on all counsel of record.

/s/ Matthew R. Berry
Matthew R. Berry

EXHIBIT A

US006603343B2

(12) **United States Patent**
Yamaguchi et al.

(10) **Patent No.: US 6,603,343 B2**
(45) **Date of Patent: Aug. 5, 2003**

(54) **PHASE CORRECTION CIRCUIT FOR TRANSISTOR USING HIGH-FREQUENCY SIGNAL**

(75) Inventors: **Mamiko Yamaguchi**, Tokyo (JP); **Yoshinobu Sasaki**, Tokyo (JP)

(73) Assignee: **Mitsubishi Denki Kabushiki Kaisha**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/171,983**

(22) Filed: **Jun. 17, 2002**

(65) **Prior Publication Data**

US 2003/0112054 A1 Jun. 19, 2003

(30) **Foreign Application Priority Data**

Dec. 18, 2001 (JP) 2001-384257

(51) **Int. Cl.**[7] **H03L 35/00**; H03K 17/78
(52) **U.S. Cl.** **327/513**
(58) **Field of Search** 327/512, 513, 327/580, 584, 314, 317, 320, 325, 326

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,584,233 A * 6/1971 Cath et al. 327/362
5,617,048 A * 4/1997 Ward et al. 327/143
6,278,313 B1 * 8/2001 Kakuta et al. 327/317

FOREIGN PATENT DOCUMENTS

JP	3-258008	11/1991
JP	11-74367	3/1999
JP	1-137713	5/1999

* cited by examiner

Primary Examiner—My-Trang Nu Ton
(74) *Attorney, Agent, or Firm*—Leydig, Voit & Mayer, Ltd.

(57) **ABSTRACT**

In order to stabilize a phase of an output signal of a transistor, a phase correction circuit includes: a) a circuit element connected in parallel to a gate of the transistor, an impedance including a reactance changing in response to a potential difference; and b) a voltage control circuit to decrease the reactance component in response to the increase in potential of the gate, wherein total reactance component of the circuit element and the transistor is maintained to a predetermined value. Because of the function of the phase correction circuit, another circuit using the output signal of the transistor can work correctly.

4 Claims, 6 Drawing Sheets

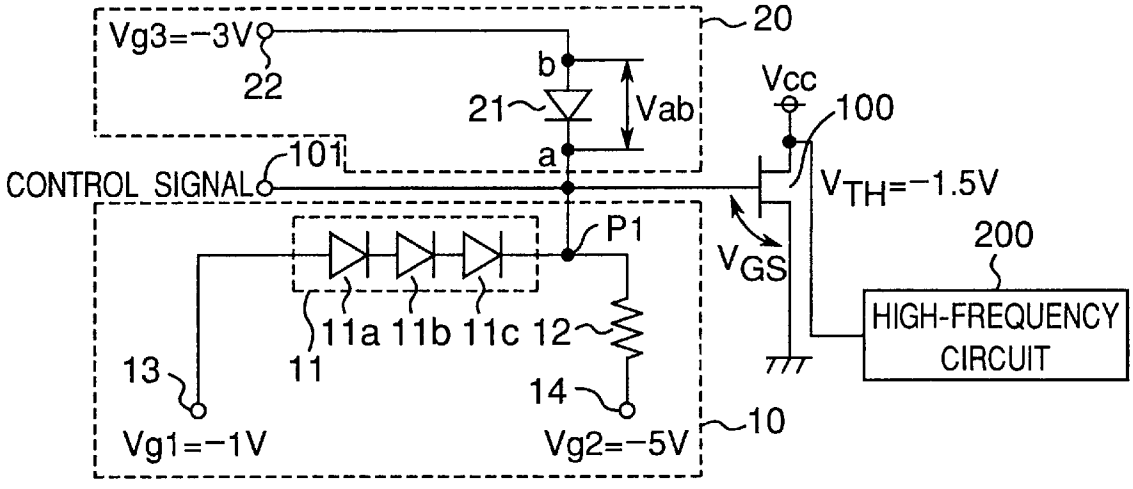


Fig.1

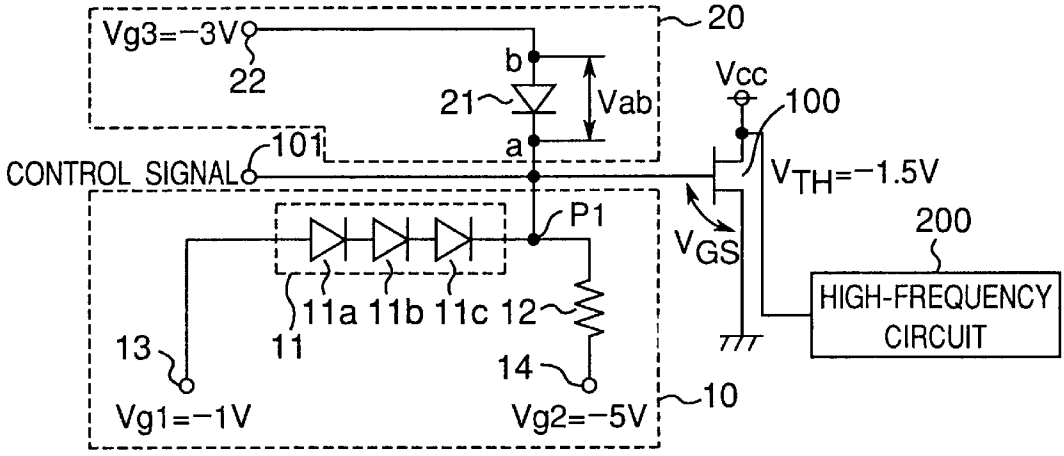


Fig.2

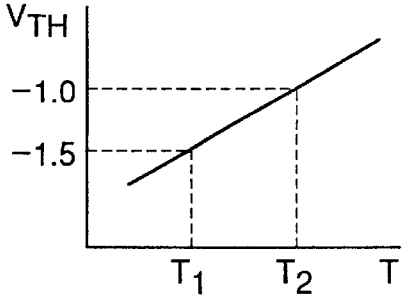


Fig.3

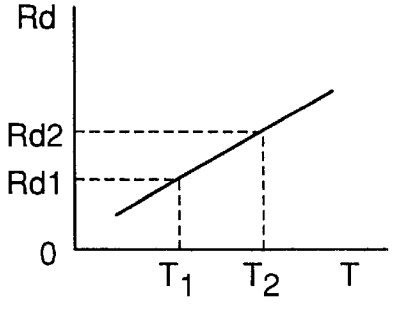


Fig.4

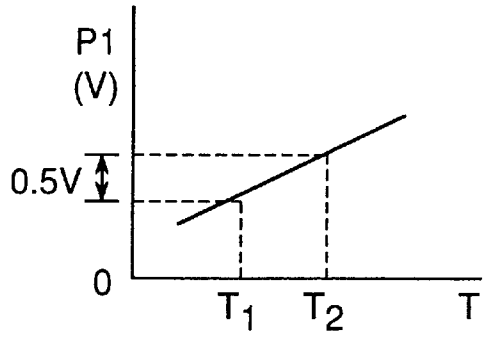


Fig.5

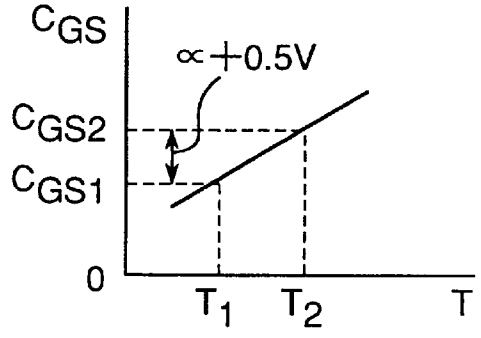


Fig.6

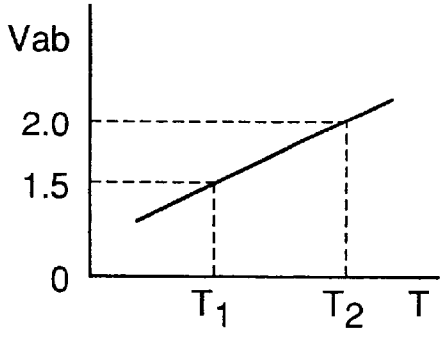


Fig.7

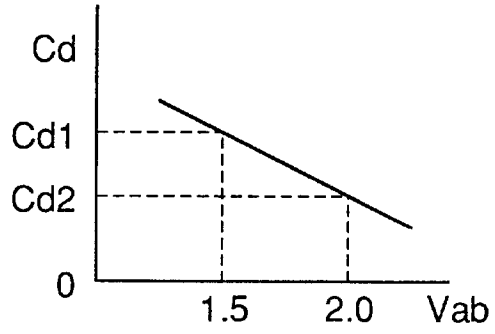


Fig.8

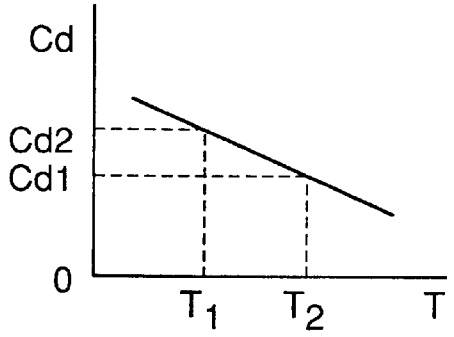


Fig.9

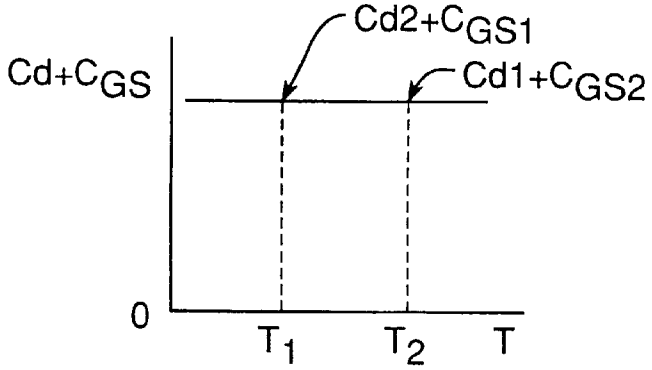


Fig.10

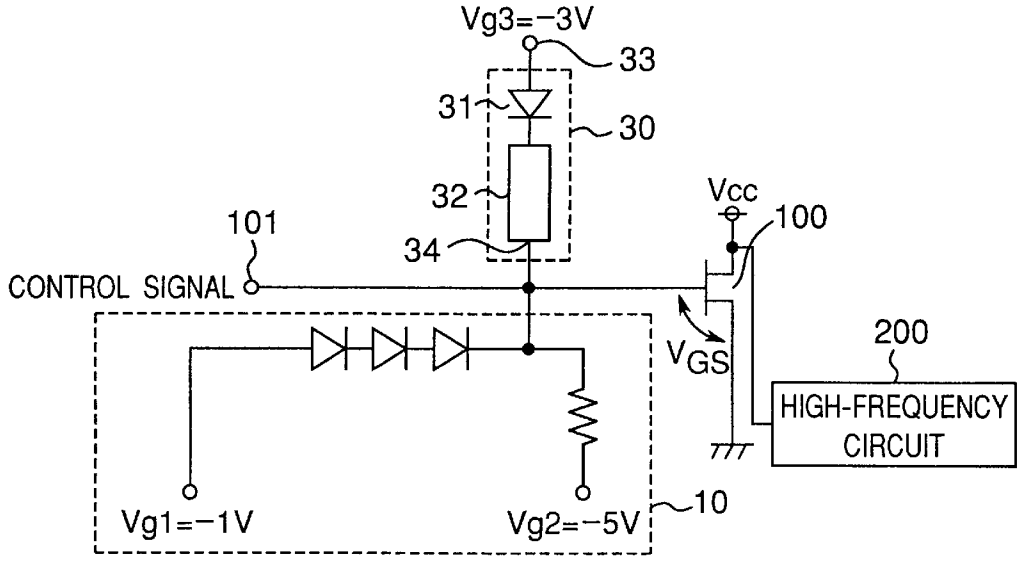

Vg3=−3V
33
31
30
32
34
101
CONTROL SIGNAL
Vcc
100
VGS
200
HIGH-FREQUENCY CIRCUIT
Vg1=−1V
Vg2=−5V
10

Fig.11

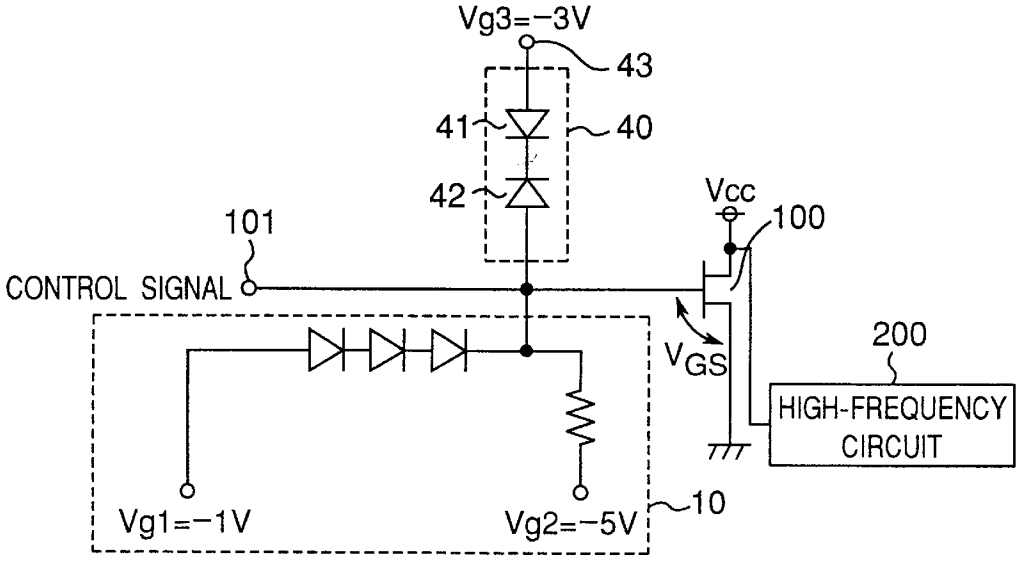

Vg3=−3V
43
41
40
42
101
CONTROL SIGNAL
Vcc
100
VGS
200
HIGH-FREQUENCY CIRCUIT
Vg1=−1V
Vg2=−5V
10

Fig.12A

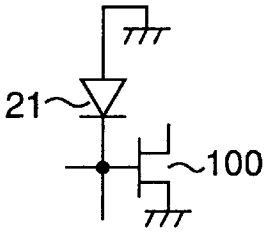


Fig.12B

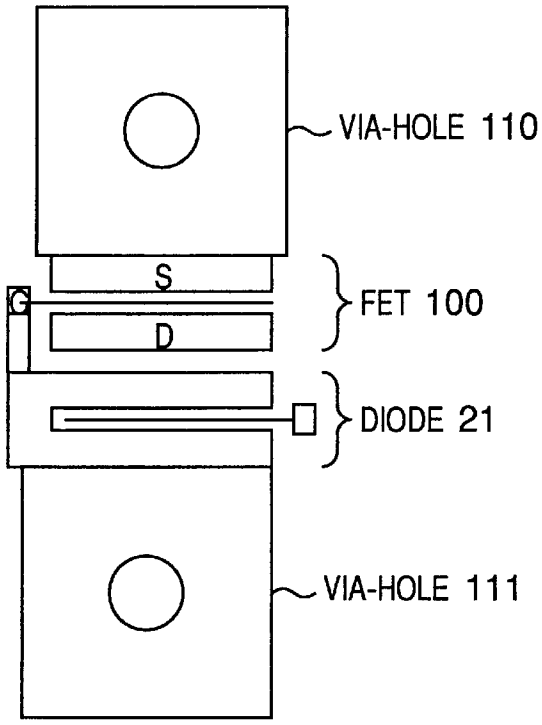


Fig.13A

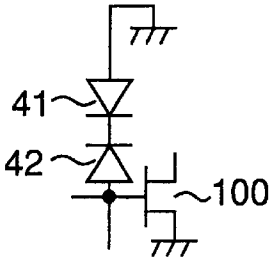


Fig.13B

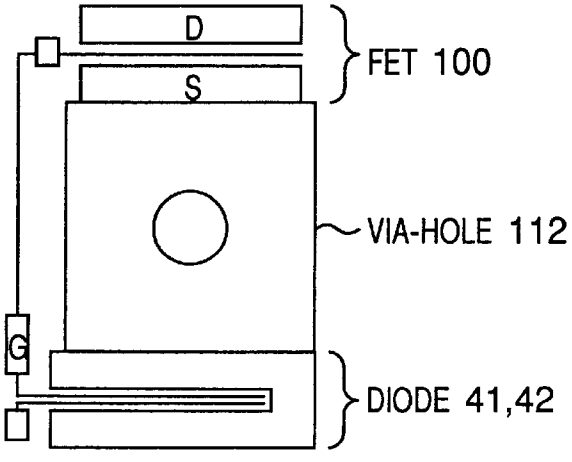
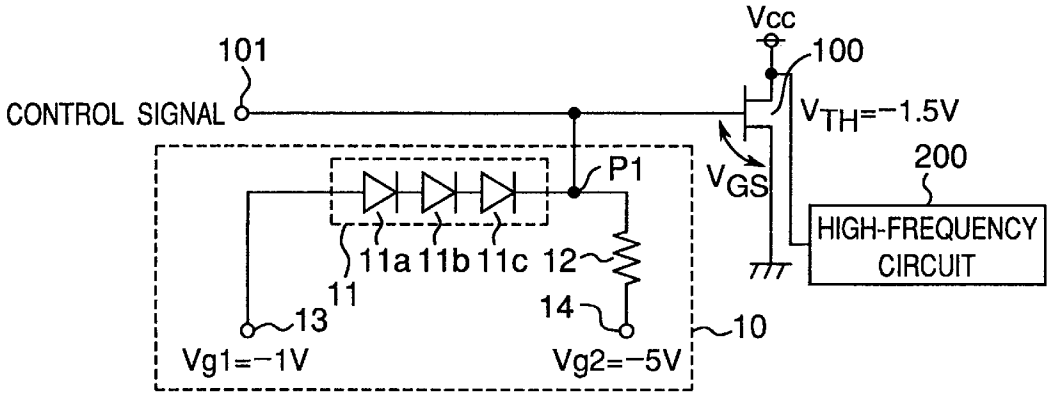


Fig.14 PRIOR ART



PHASE CORRECTION CIRCUIT FOR TRANSISTOR USING HIGH-FREQUENCY SIGNAL

FIELD OF THE INVENTION

The present invention relates to a phase correction circuit for a transistor using a high-frequency signal, which is used for a radio communication device, for example.

BACKGROUND OF THE INVENTION

It has been well known to those skilled in the art that a threshold voltage V_{TH} of a gate of a transistor is increased by an increase in the temperature of the transistor. If the threshold voltage V_{TH} has been increased, a high-level voltage of a control signal supplied to the gate needs to increase up to a value corresponding to the increased threshold voltage V_{TH}, so that the transistor can work correctly. Otherwise, other circuits provided on the downstream side of the transistor and using an output signal of the transistor cannot work correctly.

In order to solve the problem, a temperature compensation circuit has been proposed so far. The circuit supplies a compensation voltage which increases together with the increase in temperature of the transistor, so that the transistor can work correctly, even if the high-level voltage of the control signal is fixed irrelevant to its temperature change.

FIG. **14** shows a depletion type n-channel field effect transistor **100** of which a gate is connected to not only a control signal line but also a temperature compensation circuit **10**. A threshold voltage V_{TH} of the transistor **100** is −1.5V. A drain of the transistor **100** is supplied with a voltage Vcc. A source of the transistor **100** is connected to the ground. Also, the drain of the transistor **100** is connected to a high-frequency circuit **200**.

The temperature compensation circuit **10** functions as a potential dividing circuit. The circuit **10** has a load circuit **11** and a resistor **12** connected in series to the load circuit **11**. The joint P1 between the load circuit **11** and the resistor **12** is connected to the gate of the transistor **100**. More particularly, the load circuit **11** has three diodes **11***a*, **11***b* and **11***c*, connected in series and supplied with a forward bias. A terminal **13** beside the load circuit **11** is supplied with Vg**1**=−1v. A terminal **14** beside the resistor **12** is supplied with Vg**2**=−5v. A resistance Rd of the load circuit **11** is increased by a temperature increase. This is caused by a well-known temperature characteristic of the diode being supplied with forward bias, i.e., each resistance of the forward biased diode **11***a*, **11***b* and **11***c* is increased by the temperature increase.

A potential of the joint P1, or a compensation voltage being supplied to the gate of the transistor **100** is increased by an increase in resistance Rd of the load circuit **11** with the temperature increase. An incremental ratio of the compensation voltage for the temperature increase is determined identically to that of the threshold V_{TH} of the transistor **100** for the temperature increase. Therefore, the transistor **100** can work correctly, even if the high-level voltage control signal is not changed with the increase in temperature of the transistor **100**.

As described above, the temperature compensation circuit **10** can supply the compensation voltage increasing together with the increase in temperature of the transistor **100** to the gate of the transistor **100**. If the transistor **100** having the temperature compensation circuit **10** is used as a transistor for a high-frequency circuit, it causes a problem that a phase of output signal from the transistor **100** is shifted together with the increase in supply voltage, because a depletion capacitance increases together with the increase in supply voltage. If an amount of phase shift is increased, a following high-frequency circuit **200** can not work correctly.

As the phase correction circuit for a transistor using a high-frequency signal, several circuits have been proposed in various documents: a phase temperature compensation high frequency amplifier in JP A 03-258008, a semiconductor device and amplifier in JP A 11-74367, and a peaking circuit in JP A 01-137713, for example.

The phase temperature compensation high frequency amplifier in JP A 03-258008 has a circuit functioning as a phase correction circuit. The circuit has a varactor diode and a potential dividing circuit, adjusting a supply voltage of the varactor diode. The potential dividing circuit uses a positive thermistor having a resistance varying with its temperature. It is well known by those skilled in the art that the relationship of the capacitance of the varactor diode to the supply voltage is determined by a state of a p-n junction. That is, at the step junction, the depletion capacitance of the varactor diode changes in simple proportion to the square root of the supply voltage. In addition, at the graded junction, the depletion capacitance of the varactor diode changes in inverse proportion to the cube root of the supply voltage. On the contrary, the depletion capacitance of the transistor changes in simple proportion to the increase of its temperature. Therefore a compensated phase does not indicate any constant value in relation to its temperature change, or cannot have a linear relationship as described in JP A 03-258008. In addition, the semiconductor chip size becomes large because the amplifier needs to include not only the varactor diode but also a potential dividing circuit.

The semiconductor device and amplifier in JP A 11-74367 uses a diode that is inverse connected to another diode in an equivalent circuit of a transistor. The circuit supplies an inverse bias to the inverse connected diode. An electric potential of the inverse bias is set the same potential of the diode in the equivalent circuit. Therefore the capacitance changes of each of the diodes are canceled and therefore secondary unsymmetrical wave distortion can be removed. Nevertheless, this circuit cannot correct a phase shift caused by the increase in threshold voltage. In addition, JP A 11-74367 fails to disclose any circuit to correct a phase shift being caused by the temperature increase.

The peaking circuit in JP A 01-137713 can adjust a phase of an output signal from a transistor by means of a side-gate at a constant environment temperature. However, the circuit is not constructed to correct a phase shift caused by the increase in threshold voltage V_{TH} due to the temperature increase. Also, in this third document, there is no description of a circuit to correct a phase shift caused by the temperature increase. In addition, the compensation circuit described in the third document is an only circuit to cancellation an influence from the side-gate.

SUMMARY OF THE INVENTION

Therefore, a purpose of the present invention is to provide a phase correction circuit to stabilize a phase of an output signal of the transistor, even if its gate potential is increased by a temperature compensation function, the temperature increase and the other reasons.

To this end, the phase correction circuit for the transistor using high-frequency signal, comprising: a) a circuit element connected in parallel to a gate of the transistor together

with a control signal line, an impedance including a reactance component of the circuit element being changed by a potential difference between an input terminal and an output terminal of the circuit element; and b) a voltage control circuit for adjusting a supply voltage to the circuit element to decrease the reactance component in response to an increase in potential of the gate, wherein a total value of reactance components of the circuit element and the transistor is set to a predetermined value, so that another circuit using an output of the transistor can work correctly.

In another aspect of the present invention, the circuit element may be a diode of which a cathode is connected to the gate of the transistor. In this case, the voltage control circuit supplies predetermined reverse bias to the diode.

In another aspect of the present invention, the circuit element may be a diode of which a cathode is connected directly or indirectly to the gate of the transistor and a transmission line connected in series to the anode or cathode of the diode. In this case, the voltage control circuit supplies predetermined reverse bias to the diode.

In another aspect of the present invention, the circuit element may be two diodes of that the cathodes connected each other. One anode of the two diodes is connected to the gate of the transistor. In this case, the voltage control circuit supplies predetermined reverse bias to another anode of the two diodes.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a circuit diagram showing a phase correction circuit of a first embodiment;

FIG. **2** is a temperature characteristic diagram of the threshold V_{TH};

FIG. **3** is a temperature characteristic diagram of the resistance Rd;

FIG. **4** is a temperature characteristic diagram of the potential voltage of the point P1;

FIG. **5** is a temperature characteristic diagram of the depletion capacitance C_{GS} of the transistor;

FIG. **6** is a temperature characteristic diagram of the potential voltage of V_{ab};

FIG. **7** is a characteristic of the depletion capacitance Cd of the diode in relation to the potential voltage V_{ab};

FIG. **8** is a temperature characteristic diagram of the depletion capacitance Cd of the diode;

FIG. **9** is a temperature characteristic diagram of the capacitance C_{GS}+Cd;

FIG. **10** is a circuit diagram showing a phase correction circuit of a second embodiment;

FIG. **11** is a circuit diagram showing a phase correction circuit of a third embodiment;

FIG. **12**A is a partial circuit diagram showing the phase correction circuit of the first embodiment;

FIG. **12**B is a diagram showing a partial layout pattern of the phase correction circuit of the first embodiment;

FIG. **13**A is a partial circuit diagram showing the phase correction circuit of the third embodiment;

FIG. **13**B is a diagram showing a partial layout pattern of the phase correction circuit of the third embodiment; and

FIG. **14** is a circuit diagram showing a transistor with a well-known temperature compensation circuit.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

With reference to the drawings, several embodiments of the present invention will be described in detail hereinafter. It should be noted that like reference numerals designate like parts throughout the drawings.

FIRST EMBODIMENT

FIG. **1** shows a transistor **100** for high-frequency signal of which a gate is connected to not only a control signal line but also a well-known temperature compensation circuit **10** and a phase correction circuit **20**. The transistor **100** is a depletion type n-channel field effect transistor and its threshold V_{TH} is −1.5V at a temperature T1. A drain of the transistor **100** is supplied with a supply voltage Vcc. A source of the transistor **100** is connected to a ground. Also, a drain of the transistor **100** is connected to a high-frequency circuit **200**. As shown in FIG. **2**, the threshold V_{TH} of the transistor **100** increases from −1.5V to −1.0V when the transistor's temperature increases T1 to T2.

Before a detail explanation about the phase correction circuit **20** is described, a simple explanation about the temperature compensation circuit **10** will be made.

The temperature compensation circuit **10** functions as a potential dividing circuit. The circuit **10** has a load circuit **11** and a resistor **12** connected in series to the load circuit **11**. A joint P1 between the load circuit **11** and the resistor **12** is connected to the gate of the transistor **100**. More particularly, the load circuit **11** has three diodes **11***a*, **11***b* and **11***c* connected in series and supplied with forward bias. A terminal **13** beside the load circuit **11** is supplied with Vg**1**=−1V. A terminal **14** beside the resistor **12** is supplied with Vg**2**=−5V.

As shown in FIG. **3**, a resistance Rd of the load circuit **11** increases Rd**1** to Rd**2** together with an increase in temperature T1 to T2. Also, as shown in FIG. **4**, a potential voltage of the point P1, or a compensation voltage being supplied to the gate of the transistor **100**, increases by 0.5V in response to an increase in resistance Rd. The change ratio of the compensation voltage in the temperature increase is set to be substantially identical to that of the threshold V_{TH} in the temperature increase. Therefore, the transistor **100** always can work correctly, even if the high-level voltage of the control signal does not changes by the temperature increase.

However, the temperature increase causes not only an increase in threshold V_{TH} but also an increase in depletion capacitance. For example, when the compensation voltage (the potential voltage of the point P1) is increased by 0.5V, a depletion capacitance C_{GS1} between the gate and the source of the transistor **100** is increased from C_{GS1} to C_{GS2} as shown in FIG. **5**.

The phase correction circuit **20** includes the reactance component Cd of its impedance to decrease inversely with the increase in depletion capacitance C_{GS} caused by the temperature increase. Therefore, the total capacitance of C_{GS} and Cd approaches to a substantially constant value, as shown in FIG. **9**.

The phase correction circuit **20** is connected to the gate of the transistor **100** together with the control signal line. The phase correction circuit **20** has a diode **21** as a circuit element of which a reactance component of its impedance is varied by a potential difference of between an input terminal and an output terminal of the diode **21**.

A cathode of the diode **21** is connected with the gate of the transistor **100**. An anode of the diode **21** is connected with the voltage-supplying terminal **22**. The voltage terminal **22** is supplied with Vg**3**=−3V. Therefore, a potential of the gate is always higher than a potential of the terminal **22**.

The phase correction circuit **20** having diode **21** and the terminal **22**, functioning as a voltage control circuit, adjusts potential difference between the input terminal and the output terminal of the diode **21** in order to decrease a

reactance component of the diode **21** in accordance with an increase in potential of the gate of the transistor **100**.

The depletion capacitance Cd of the diode **21** decreases inversely with the increase in potential of the gate of the transistor **100** in order that the total capacitance of C_{GS} and Cd reaches a substantially constant value, so that the following high-frequency circuit **200** using an output signal of the transistor **100** can function correctly.

FIG. **6** shows a temperature characteristic diagram of a potential difference Vab between a terminal-a and a terminal-b of the diode **21**. The potential difference Vab increases from 1.5V to 2.0V in response to the increase in temperature from T1 to T2 (T2>T1). This change is caused by an increase in voltage supplied to the gate of the transistor **100**. This voltage increment is caused by a function of a temperature compensation circuit **10** with the temperature increase.

FIG. **7** shows a character of the depletion capacitance Cd to the potential difference Vab. The depletion capacitance Cd decreases from Cd**2** to Cd**1** (Cd**1**<Cd**2**) in response to the increase in potential difference Vab. This change is caused by a well-known character of an inverse connected and inverse biased pin diode.

FIG. **8** shows a temperature characteristic diagram of the depletion capacitance Cd. The depletion capacitance Cd decreases from Cd**2** to Cd**1** in response to the increase in temperature from T1 to T2 (T2>T1). This change is caused by the increase in temperature from T1 to T2 (T2>T1) due to the function of the temperature compensation circuit **10** with the temperature increase.

FIG. **9** shows a temperature characteristic diagram of the total capacitance of Cd and C_{GS}. The total capacitance of Cd and C_{GS} is maintained constant irrelevant to the temperature. This can be attained by the set of an appropriate diode **21** of which a temperature characteristic of depletion capacitance Cd has an inverse temperature characteristic of depletion capacitance C_{GS} of the transistor **100**.

The phrase of "The total capacitance of Cd and C_{GS} shows a constant value" means that a phase shift caused by the total capacitance of Cd and C_{GS} provides no adverse affect to the high-frequency circuit **200**. Also, this definition of "the total capacitance of Cd and C_{GS} shows a constant value" can be used in each phase correction circuits **20**,**30** in the following embodiments.

In an embodiment of semiconductor circuit having the transistor **100** of which the gate is connected with the temperature compensation circuit **10** and the phase correction circuit **20**, a size of the semiconductor circuit can be reduced, in compared with another semiconductor circuit using the transistor **100** connected with the circuit **10** and an adjusting means for adjusting the phase of the output signal of the transistor **100**, because the phase correction circuit **20** has a simple construction. Specifically, the circuit **20** has one diode **21** and two lines supplying an inverse bias that varies with a voltage of the gate of the transistor **100** to the diode **21**. However, in the case where the transistor **100** connected with the circuit **10** and the adjusting means are used for the semiconductor circuit, the adjusting means need two complex circuits. One circuit is a detecting circuit for detecting a reference signal and an amount of a phase shift, and another circuit is an adjusting circuit for adjusting a shifted signal according to the reference signal. Each phase correction circuit **30**,**40** in the following embodiments described below can also reduce the semiconductor circuit size by similar reasons.

SECOND EMBODIMENT

FIG. **10** shows a transistor **100** of which the gate is connected with the temperature compensation circuit **10** and a phase correction circuit **30**. The drain of the transistor **100** is supplied with Vcc. The source of the transistor **100** is connected to a ground. Also, the drain of the transistor **100** is connected to the high-frequency circuit **200**.

The phase correction circuit **30** uses a loaded line type phase device as a circuit element which is connected in parallel to the gate of the transistor **100** together with a control signal line, and of which an impedance including reactance component is changed by the potential difference between its input and output terminals. The loaded line type device has a diode **31** and a transmission line **32**. A cathode of the diode **31** is turned to the gate of the transistor **100**. The transmission line **32** is connected serially to the diode **31**.

Also, in the phase correction circuit **30**, a terminal **34** of the transmission line **32** is connected to the gate of the transistor **100**. A terminal **31** of an anode of the diode **31** is supplied with Vg**3**=−3V. Therefore, the circuit **30** can function as a voltage control circuit that can adjust the supply voltage to the diode **31** in order to decrease the reactance component according to the increase in potential of the gate of the transistor **100**.

The phase correction circuit **30** of second embodiment has not only a phase correctable function effected by a diode **21** of the phase correction circuit **20** of first embodiment but also an additional phase correctable function effected by a reactance component of the transmission line **32**. Therefore, the phase correction circuit **30** can adjust flexibly a phase of an output signal of the transistor **100** to a request of the high-frequency circuit **200**.

It should be noted that, a connecting order of the diode **31** and the transmission line **32** is replaceable.

THIRD EMBODIMENT

FIG. **11** shows the transistor **100** of which the gate is connected not only to the control signal line but also to the temperature compensation circuit **10** and a phase correction circuit **40** of third embodiment. The drain of the transistor **100** is supplied with power supply Vcc. The source of the transistor **100** is connected to a ground. Also, the drain of the transistor **100** is connected to the high-frequency circuit **200**.

The phase correction circuit **40** uses two diodes **41**,**42** of which cathodes are connected to each other to form a circuit element which is connected in parallel to the gate of the transistor **100** together with a control signal line, and of which the impedance including reactance component is changed by the potential difference between its input and output terminals. Because both cathodes of the diodes **41**,**42** are formed into a single unit in a semiconductor circuit, a size of layout pattern can be reduced.

Also, in the phase correction circuit **40**, an anode of the diode **42** is connected to the gate of the transistor **100**. A terminal **43** of the anode of the diode **41** is supplied with Vg**3**=−3V in order to set a potential of the gate of the transistor **100** higher than a potential of the terminal **43**. Therefore, the circuit **40** can work as a voltage control circuit which adjusts the supply voltage to the diode **41** in order to decrease the reactance component in accordance with the increase in potential of the gate of the transistor **100**.

FIG. **12**A shows a connecting phase of the diode **21** of the phase correction circuit **20** of first embodiment and the transistor **100**. FIG. **12**B shows a layout pattern of the connecting phase. As shown in FIG. **12**B, in the phase correction circuit **20**, two via-holes **110**,**111** are needed in the layout pattern.

FIG. **13**A shows a connecting phase of the diodes **41**,**42** of the phase correction circuit **40** of the third embodiment

and the transistor **100**. FIG. **13**B shows a layout pattern of the connecting phase. As shown in FIG. **13**B, since the cathodes of the diodes **41**,**42** are made with a single unit, only one via-hole **112** is needed in the layout pattern.

Comparing with two layout patterns in FIG. **12**B and FIG. **13**B, it can be understood that the phase correction circuit **40** could be reduced in size corresponding to one via-hole.

As described above, the phase correction circuits **20**,**30** and **40** according to the embodiments **1**,**2** and **3** can stabilize the phase shift of the output signal of the transistor **100** by maintaining the total capacitance of Cd and C_{GS} in the predetermined constant value, even if the supply voltage to the gate of the transistor **100** is increased by, for example, the function of the temperature compensation circuit **10**, so that the following circuit using the output signal of the transistor **100** can work correctly.

What is claimed is:

1. A phase correction circuit for a transistor, comprising:

a circuit element having an output terminal connected to a gate of a transistor to which a control signal line is connected, and an input terminal, wherein the circuit element has a reactance that changes with potential difference between the input terminal and the output terminal; and

a voltage control circuit supplying a voltage to the input terminal of the circuit element so that the reactance of the circuit element decreases in response to an increase in potential of the gate, wherein a sum of the reactance of the circuit element and a gate-source reactance of the transistor remains substantially constant.

2. The phase correction circuit according to claim **1**, wherein the circuit element is a diode having an anode as the input terminal and a cathode as the output terminal, the cathode of the diode is connected to the gate of the transistor, and the voltage control circuit supplies a reverse bias to the anode of the diode.

3. The phase correction circuit according to claim **1**, wherein the circuit element includes a diode having an anode as the inputs terminal and a cathode as the output terminal, the cathode being connected directly, or indirectly to the gate of the transistor, and including a transmission line serially connected to one of the anode and cathode of the diode, wherein the voltage control circuit supplies a reverse bias to the anode of the diode.

4. The phase correction circuit according to claim **1**, wherein the circuit element includes first and second diodes having respective anodes and cathodes, the cathodes are connected to each other, the anode of the first diode is the output terminal connected to the gate of the transistor and, the voltage control circuit supplies a reverse bias to the anode of the second diode as the input terminal.

* * * * *

EXHIBIT B

US008947164B2

(12) **United States Patent**
Eplett

(10) **Patent No.: US 8,947,164 B2**
(45) **Date of Patent: Feb. 3, 2015**

(54) **INTEGRATED TECHNIQUE FOR ENHANCED POWER AMPLIFIER FORWARD POWER DETECTION**

(71) Applicant: **Microsemi Corporation**, Aliso Viejo, CA (US)

(72) Inventor: **Brian Eplett**, Lilburn, GA (US)

(73) Assignee: **Microsemi Corporation**, Aliso Viejo, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 92 days.

(21) Appl. No.: **13/894,221**

(22) Filed: **May 14, 2013**

(65) **Prior Publication Data**

US 2013/0307624 A1 Nov. 21, 2013

Related U.S. Application Data

(60) Provisional application No. 61/648,721, filed on May 18, 2012.

(51) **Int. Cl.**

H03G 3/10	(2006.01)
H03G 3/00	(2006.01)
H03F 1/56	(2006.01)
H03F 3/19	(2006.01)

(52) **U.S. Cl.**

CPC ***H03G 3/004*** (2013.01); ***H03F 1/56*** (2013.01); ***H03F 3/19*** (2013.01)

USPC **330/278**; 330/129

(58) **Field of Classification Search**

USPC 330/278, 279, 129, 136

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,148,117	A	9/1992	Talwar	
5,977,831	A *	11/1999	Davis et al.	330/279
7,777,566	B1 *	8/2010	Drogi et al.	330/136
2006/0222104	A1	10/2006	Braithwaite	
2011/0148519	A1 *	6/2011	Drogi et al.	330/129

FOREIGN PATENT DOCUMENTS

EP 0803974 A1 10/1997

OTHER PUBLICATIONS

European Patent Office, ISA/EP, International Search Report/Written Opinion, PCT/US2013/041202, Rijswijk, The Netherlands, Nov. 29, 2013, 7 pages.

* cited by examiner

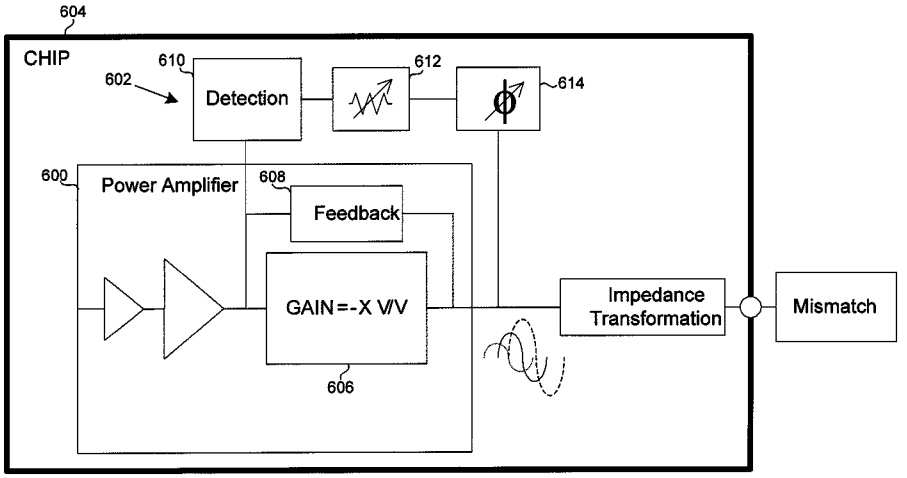
Primary Examiner — Henry Choe

(74) *Attorney, Agent, or Firm* — Marger Johnson & McCollom, PC

(57) **ABSTRACT**

A power amplifier has power detection capabilities that include a radio frequency (RF) power amplifier that has a gain stage that includes a gain stage input, a gain stage output, and a feedback loop coupled between an input and an output of the power amplifier. A detection circuit has a first detection circuit input electrically coupled to the gain stage input and has a detection circuit output. An amplitude control circuit and a phase control circuit are electrically coupled together in series between the gain stage output and a second detection circuit input. The amplitude control circuit and the phase control circuit produce a signal that is received by the second detection circuit input so that the detection circuit can detect a signal at the detection circuit output that is proportional to a the forward power output of the power amplifier and is insensitive to power amplifier output load mismatch.

17 Claims, 10 Drawing Sheets



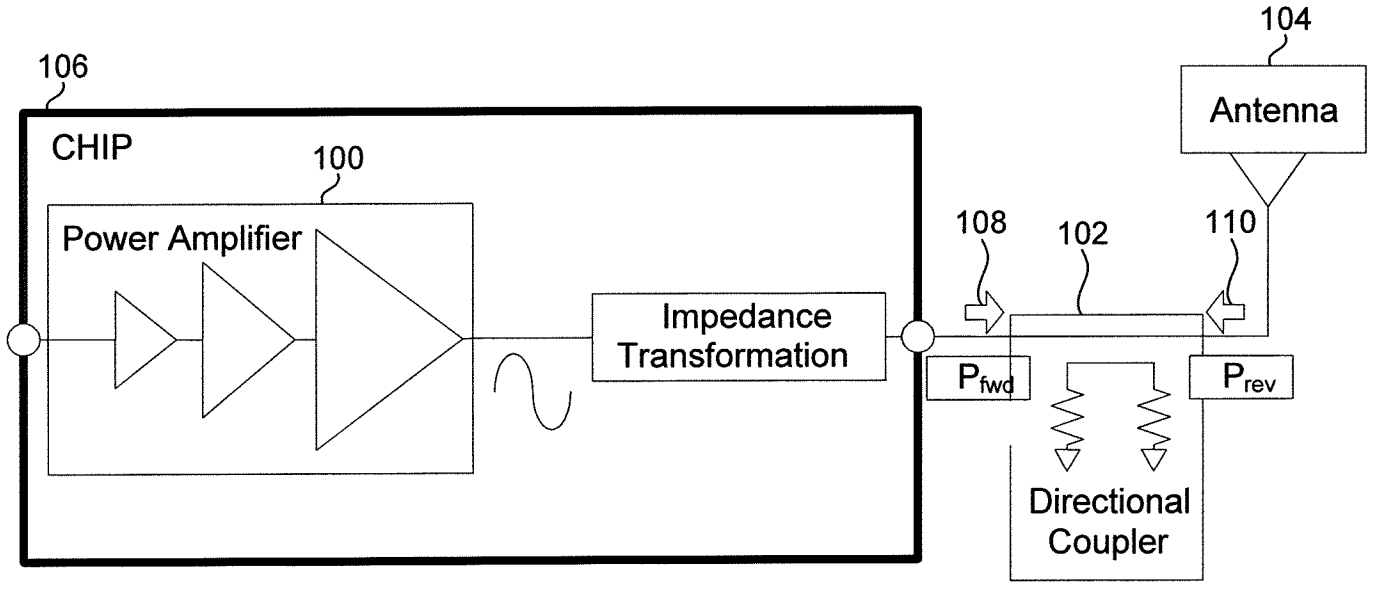


FIG. 1
PRIOR ART

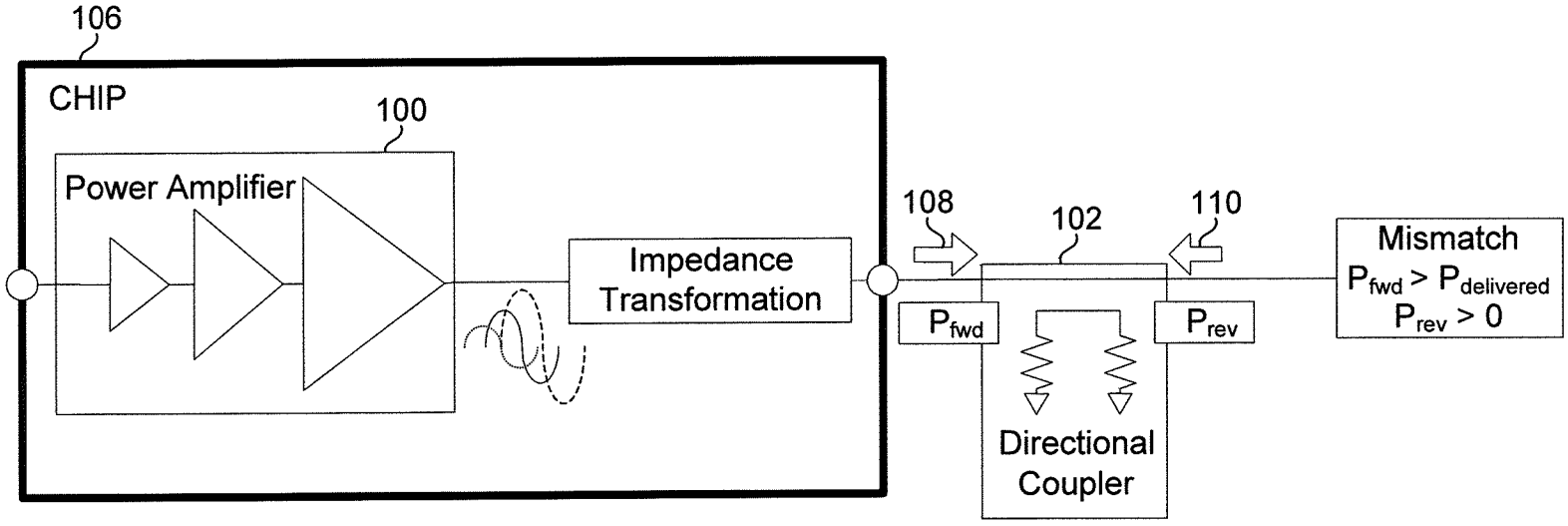


FIG. 2
PRIOR ART

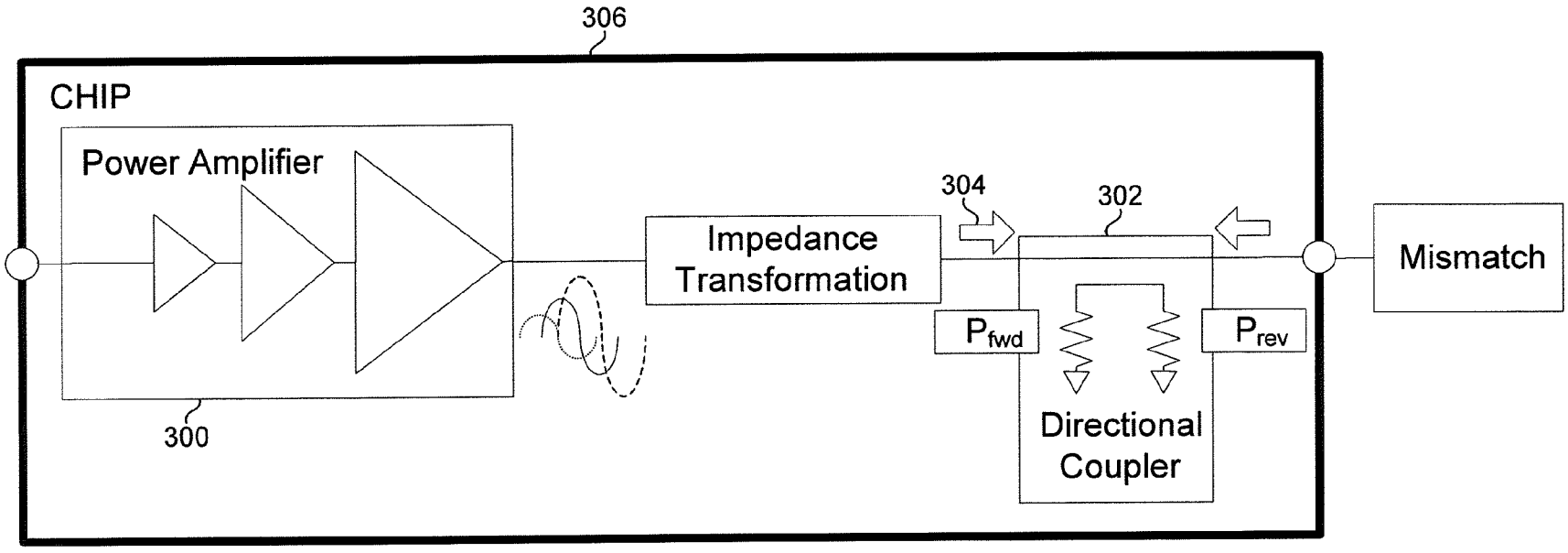


FIG. 3
PRIOR ART

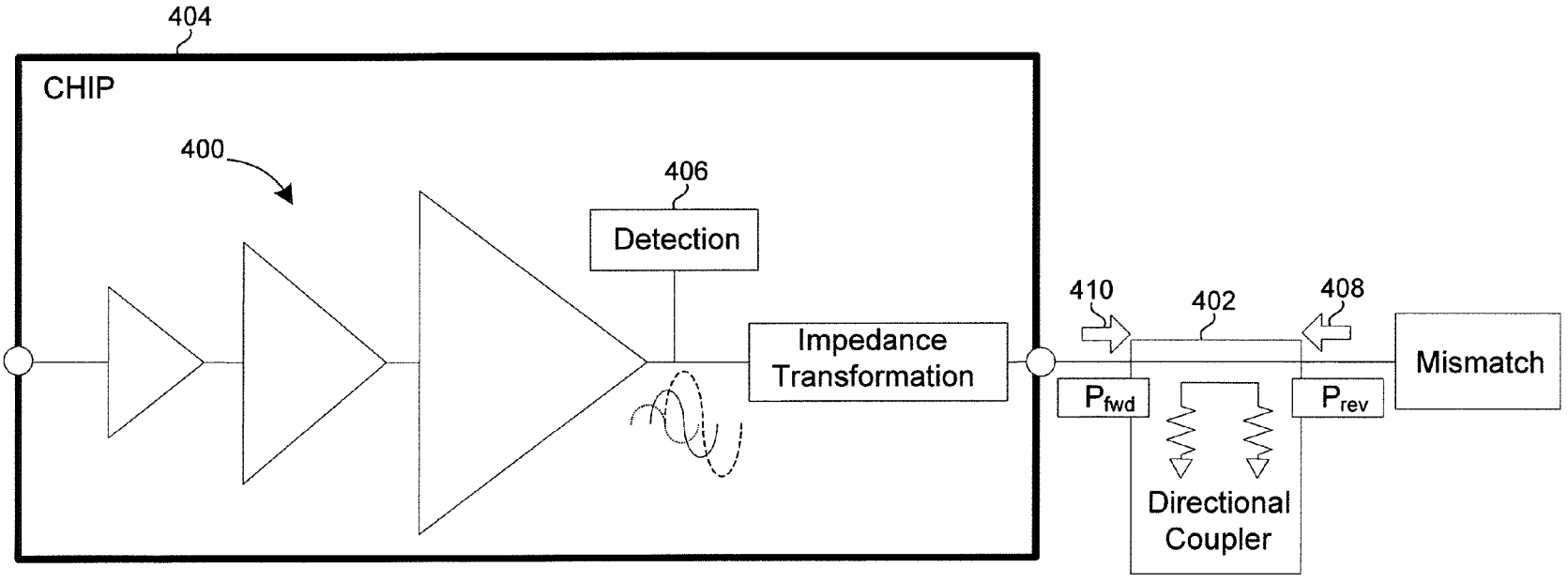


FIG. 4

PRIOR ART

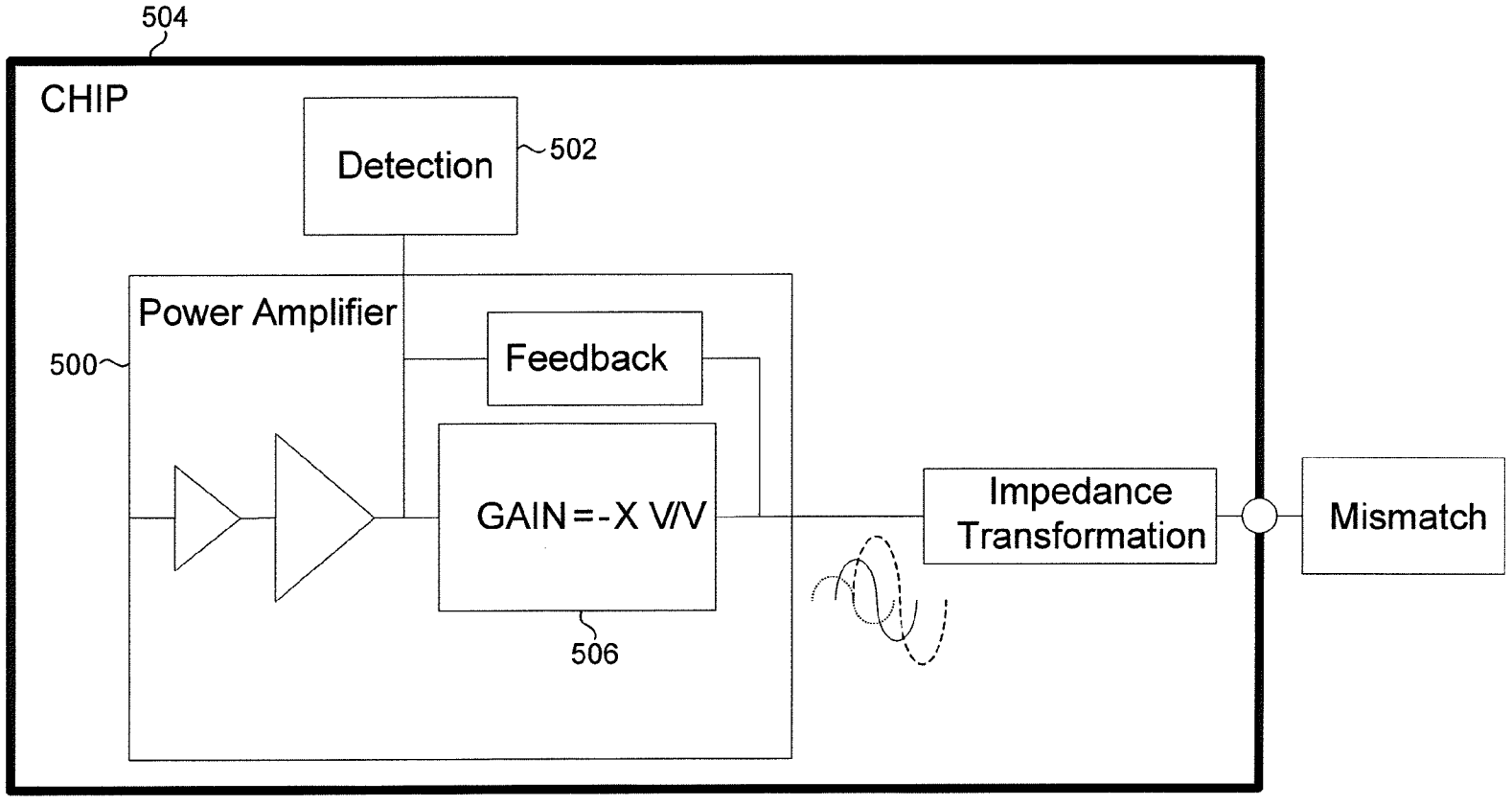


FIG. 5

PRIOR ART

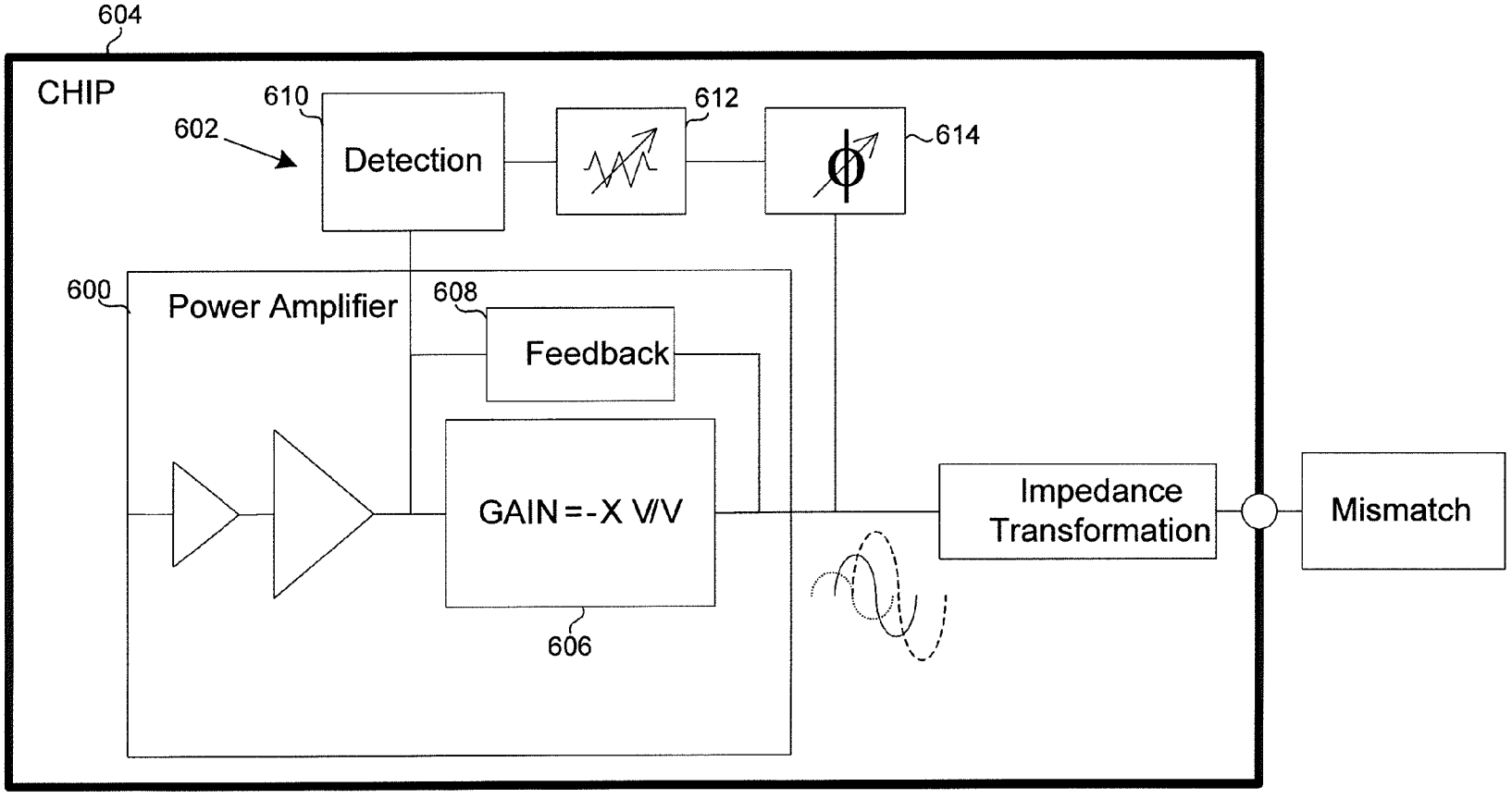

604
CHIP
610
602
Detection
612
614
600
Power Amplifier
608
Feedback
GAIN = -X V/V
606
Impedance Transformation
Mismatch

FIG. 6

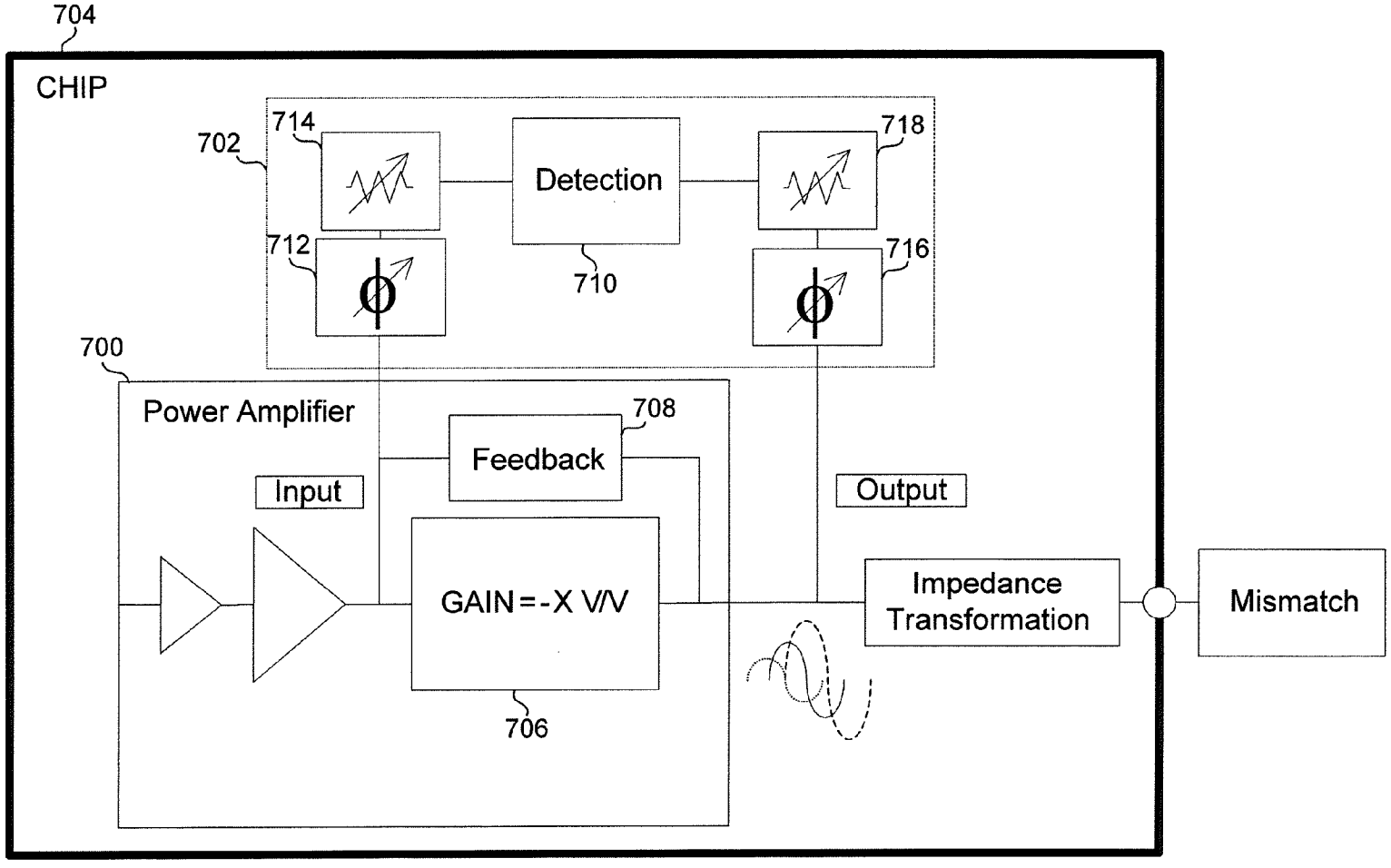

704
CHIP
702
714
712
Detection
710
718
716
700
Power Amplifier
708
Feedback
Input
Output
GAIN = -X V/V
706
Impedance Transformation
Mismatch

FIG. 7

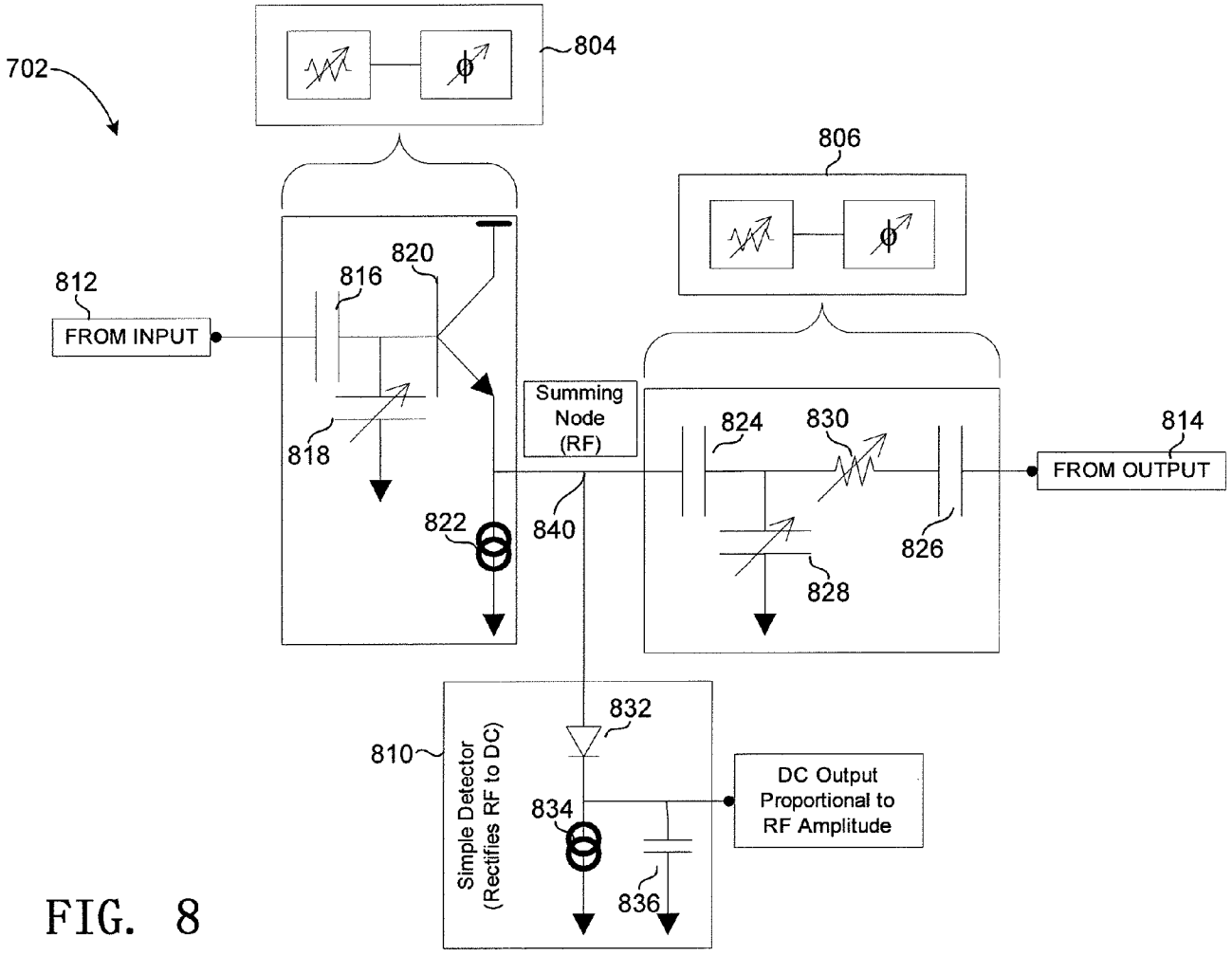

702
804
806
812
FROM INPUT
820
816
818
822
Summing Node (RF)
840
824
830
814
FROM OUTPUT
826
828
810
Simple Detector (Rectifies RF to DC)
832
834
836
DC Output Proportional to RF Amplitude

FIG. 8

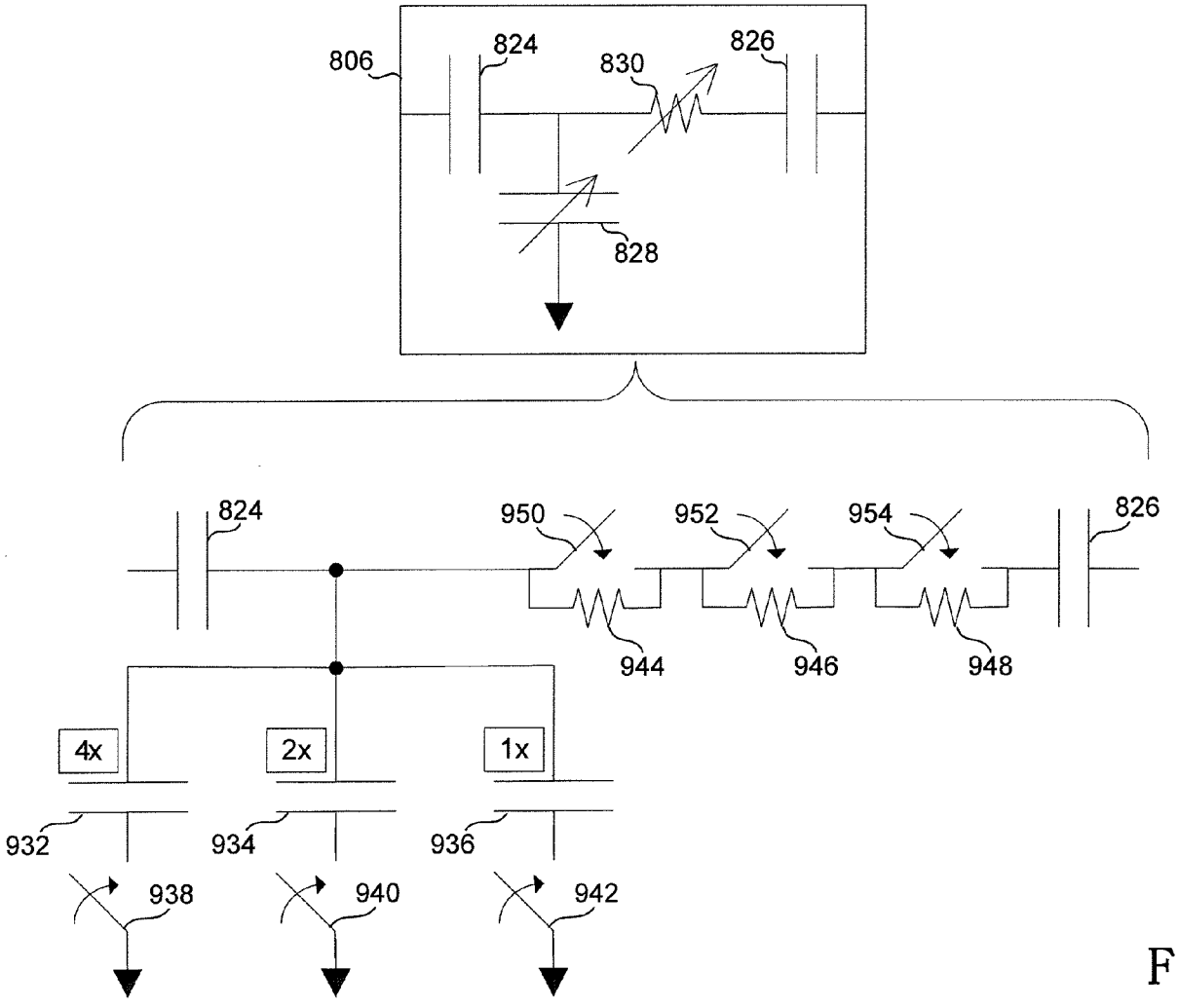

806
824
830
826
828
824
950
952
954
826
944
946
948
4x
2x
1x
932
934
936
938
940
942

FIG. 9

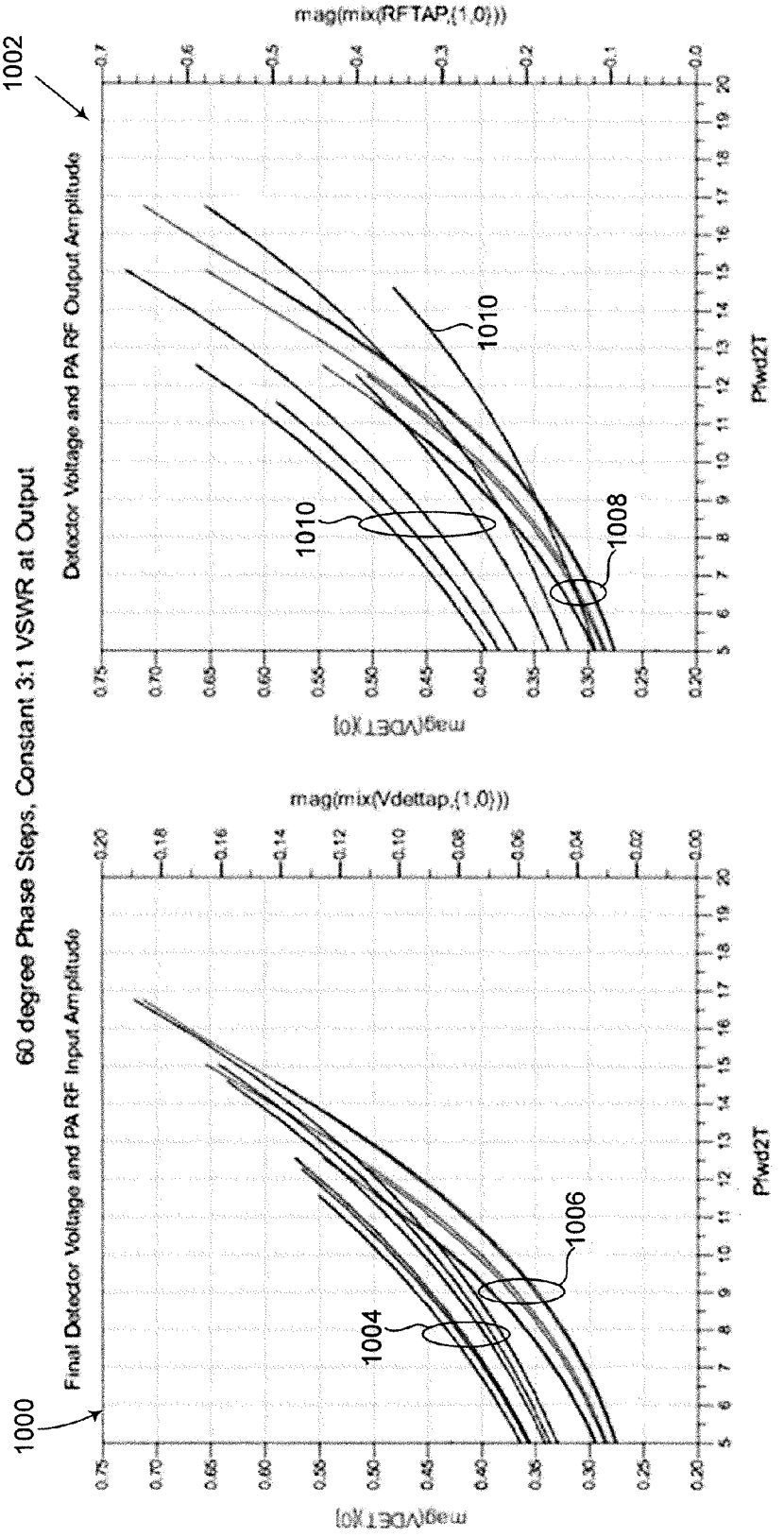

60 degree Phase Steps, Constant 3:1 VSWR at Output
1002
Detector Voltage and PA RF Output Amplitude
mag(mix(RFTAP,{1,0}))
mag(VDET,{0})
Pfwd2T
1010
1008
1000
Final Detector Voltage and PA RF Input Amplitude
mag(mix(Vdettap,{1,0}))
1006
1004

FIG. 10

INTEGRATED TECHNIQUE FOR ENHANCED POWER AMPLIFIER FORWARD POWER DETECTION

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of U.S. provisional patent application Ser. No. 61/648,721, filed May 18, 2012, incorporated by reference herein.

FIELD OF THE INVENTION

This disclosure relates to enhancing power amplifier performance and more specifically to improving the forward power detection under variable loading conditions caused by the environment.

BACKGROUND OF THE INVENTION

Many power amplifiers are used in environments in which the amount of power of the transmitted signal must be within a specified range. For example, federal agencies like the Federal Communications Commission (FCC) restrict the amount of power permissible in a signal transmitted in wireless LAN communications. Power detection in circuits that include power amplifiers in such controlled environments is critical to ensuring that the power of the transmitted signals are compliant with FCC regulations.

Accurate power detection in power amplifiers can be challenging, especially when the load condition on the output of the power amplifier changes over time, such as when the user of a cell phone moves from outside of a building to inside of a building. The performance of the power amplifier changes with the new loading condition, and this performance change must be reliably detected. Existing solutions for detecting power in power amplifiers can rely on printed circuit board (PCB) level directional couplers that are large and costly. Other existing solutions rely on power detection at the output of the power amplifier, which produces a significant amount of variation for detecting the forward power. Still other existing solutions rely on power detection at the input of the final gain stage of the power amplifier, but such an arrangement suffers from a dependent relationship between the power amplifier design and the detector and requires the power amplifier design to consider the design parameters of the detector, which limits the power amplifier capabilities.

Therefore, there is a need for improvements to power detection in power amplifiers that can be integrated in monolithic solutions, such as a standard CMOS/BiCMOS or GaAs process, that can be independent of power amplifier design parameters and provide a degree of freedom from the performance of the power amplifier without sacrificing the ability to accurately detect power in the output signal of the power amplifier.

SUMMARY OF THE INVENTION

An object of this invention is to provide methods and device structures suitable for improving the forward power detection of a power amplifier.

An exemplary power amplifier has power detection capabilities. Such devices and methods can include a radio frequency (RF) power amplifier that has a gain stage that includes a gain stage input, a gain stage output, and a feedback loop coupled between an input and an output of the power amplifier. A detection circuit has a first detection circuit input that is electrically coupled to the gain stage input and a detection circuit output. An amplitude control circuit and a phase control circuit are electrically coupled together in series between the gain stage output and a second detection circuit input. The amplitude control circuit and the phase control circuit produce a signal that is received by the second detection circuit input so that the detection circuit can detect a signal at the output of the detection circuit that has a power proportional to a forward power output of the power amplifier.

A method of detecting forward power in a detection circuit that is coupled to a power amplifier is also disclosed. A first amplitude control circuit is coupled in series to an input of a gain stage of a power amplifier to produce a corrected input signal. A second amplitude control circuit and a phase control circuit are coupled in series to an output of the gain stage of the power amplifier to produce a corrected output signal. The corrected input signal and the corrected output signal are summed to produce a summed node signal that is proportional to the forward power output of the power amplifier. The summed node signal is applied to the detection circuit to detect the forward power output of the power amplifier.

The foregoing and other objects, features and advantages of the invention will become more readily apparent from the following detailed description of embodiments of the invention which proceeds with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a prior art power detection circuit for use with a power amplifier under matched power conditions.

FIG. **2** is the prior art power detection circuit shown in FIG. **1** under mismatched power conditions.

FIG. **3** is a prior art integrated forward power detection circuit with an external directional coupler under mismatched conditions.

FIG. **4** is a prior art integrated forward power detection circuit with a detection circuit that detects voltage at the output of the power amplifier under mismatched conditions.

FIG. **5** is a prior art integrated forward power detection circuit with a detection circuit that detects voltage on the input of the final gain stage of the power amplifier under mismatched conditions.

FIG. **6** is an integrated forward power detector in accordance with aspects of the disclosure.

FIG. **7** is another embodiment of an integrated forward power detector in accordance with aspects of the disclosure.

FIG. **8** is an example summing detection circuit electrically coupled to a first amplitude and phase control circuit and a second amplitude and phase control circuit.

FIG. **9** is an example resistor and capacitor tuning circuit for an amplitude and phase control circuit combination.

FIG. **10** is a graphical representation of VWSR insensitive forward power detection improvement when the power detection of the power amplifier is performed by the disclosed power detectors.

DETAILED DESCRIPTION

In the drawings, which are not necessarily to scale, like or corresponding elements of the disclosed systems and methods are denoted by the same reference numerals.

To detect power in power amplifiers, such as those in the LX5586 and LX5588 Integrated Front End Modules manufactured by Microsemi Corporation®, the disclosed circuits and methods provide for an integrated power detection solu-

tion that provides design freedom from the power amplifier. The disclosed power amplifiers with integrated power detectors minimize power loss, have a flat frequency response, improved directivity, can be integrated alongside and independently from the power amplifier, and are physically small to conserve die area. All of these features of the disclosed power amplifiers with integrated power detectors improve the size and cost of power detection for power amplifiers. The circuits and methods of the disclosure sample the input and output of the final stage of a power amplifier to accurately detect power in the signal transmitted from the power amplifier.

FIGS. **1-5** show prior art solutions to detecting power in power amplifiers. FIGS. **1** and **2** show a prior art power amplifier **100** with a directional coupler **102** that detects the power of the signal being transmitted from the power amplifier **100** through the antenna **104** under matched and mismatched signal conditions, respectively. In the prior art power detector shown in FIGS. **1** and **2**, the directional coupler **102** and antenna **104** are located off of the integrated circuit die or chip **106**. Under the matched conditions shown in FIG. **1**, the voltage standing wave ratio (VSWR) is zero. Under the mismatched conditions shown in FIG. **2**, the VSWR is greater than zero. Calculating the VSWR is a ratio of the maximum and minimum radio frequency (RF) voltage amplitude on the transmission path. The variation in voltage amplitude is caused by non-zero reflected power (P_{rev}). This reverse power is caused by load mismatch on the output of the power amplifier, which reflects the forward power back toward the power amplifier.

A matched signal is a signal that has forward power, P_{fwd}, **108** that is equal to the power delivered to the load (i.e., the antenna that transmits the signal from the power amplifier). Under these conditions, the reflected power, P_{rev}, **110** is zero. Forward power, P_{fwd}, **108** is the power of the signal that is being transmitted from the power amplifier **100** through the antenna **104**. Reflected power, P_{rev}, **110** is the power that is being reflected due to load match from the antenna **104** back toward the amplifier. Reflected power, P_{rev}, **110** is generated when a signal is returned by the antenna **104**, which often occurs when signals are transmitted in areas in which signals are likely to reflect off of an object, such as a metal box, building, vehicle, or the like.

FIG. **2** shows the prior art power detection solution in which the forward power, P_{fwd}, **108** is no longer equal to the power delivered to the load. Some amount of the power is reflected, depending on the degree of mismatch. Under these conditions, P_{rev} longer zero. Such mismatched conditions cause voltage amplitude variation in the transmission path and makes the forward power, P_{fwd}, **108** no longer proportional to the voltage amplitude of the power signal output from the power amplifier. This variation prevents accurate power detection in a voltage detection-based solution. Variation in the phase and magnitude of the mismatch makes accurately detecting the forward power, P_{fwd}, **108** difficult since integrated detection schemes are most easily realized in the voltage domain.

In the presence of mismatch, the voltage signal at any given location in the system varies in phase as well as amplitude. The prior art detectors shown in FIGS. **1** and **2** rely on only sampling the output voltage, which makes this solution inherently inaccurate because the forward power, P_{fwd}, **108** is no longer proportional to the voltage amplitude of the power of the output signal from the power amplifier.

FIG. **3** shows a prior art power amplifier that implements an external on-chip directional coupler **302** that detects forward power, P_{fwd}, **304** output by the power amplifier **300** all on the same chip **306**. The amplitude and frequency response of the signal detected by the directional coupler **302** is a direct function of the size of the on-chip directional coupler **302**. As the size of the directional coupler **302** grows, the loss of the structure increases and the area cost of the on-chip solution increases. The behavior of the directional coupler **302** is dictated by the wavelength of the signal, the directional coupler **302** can experience a significant trade-off between frequency response and size, which translates into loss. Further, this prior art on-chip directional coupler **302**, is intimately tied to the behavior of the power amplifier **300**, which complicates the design of the power amplifier **300** and compromises power amplifier performance for detector or directional coupler performance.

FIG. **4** shows another prior art power amplifier **400** with a power detector **402** in which a directional coupler **402** is located off the chip **404** on which the power amplifier **400** is located. The power from the power amplifier **400** in the example shown in FIG. **4** is detected at the output of the power amplifier **400**. As described above, the reflected power, P_{rev}, **408** interacts with the forward power, P_{fwd}, **410** such that the voltage amplitude at a given point between the power amplifier **400** output and the mismatch causes the voltage amplitude to vary. Detection of the voltage on the power amplifier **400** output produces a significant amount of variation for a constant forward power, P_{fwd} **410**.

FIG. **5** shows yet another prior art power amplifier **500** with a power detector **502** located on the same chip **504**. The power detector **502** detects power, on-chip, at the input of a final gain stage **506** of the power amplifier **500** without need for a directional coupler, as shown in the prior art examples described above in reference to FIGS. **1-4**. The input of the final gain stage **506** of the power amplifier **500** is less sensitive to mismatched signals because transistors in the final stage of the power amplifier have a negative voltage gain and a finite reverse isolation so the impact of VSWR due to mismatched signals can be diminished. However, a detector design that detects power at the input of the final gain stage of the power amplifier, such as the detector **502** shown in FIG. **5**, suffers from a dependence upon the power amplifier design, a reduced ability to control the phase and amplitude mismatch that may be seen at the input of the final gain stage of the power amplifier, and a reduced ability to detect signals with relatively low power values.

Turning now to FIGS. **6** and **7**, two power amplifiers with power detectors are disclosed that detect power of a signal output from a power amplifier, in accordance with aspects of the disclosure. In FIG. **6**, the power amplifier **600** and the detector **602** are both located on the same chip **604**. The power amplifier **600** can be a radio frequency RF power amplifier with multiple gain stages, including a final gain stage **606**. The final gain stage **606** of the power amplifier **600** has an input and an output and a feedback loop **608** is coupled between the input and output of the power amplifier **600**. The detector **602** includes a detection circuit **610** that has a detection circuit input that is electrically coupled to the final gain stage **606** input of the power amplifier **600** and has a detection circuit output (**840** in the FIG. **8** example). An amplitude control circuit **612** and a phase control circuit **614** that are electrically coupled between the final gain stage **606** output and a second detection circuit **610** input. The amplitude control circuit **612** and phase control circuit **614** are electrically coupled in series and their order can be reversed in other examples. The amplitude control circuit **612** and the phase control circuit **614** produce a signal that is received by the second detection circuit **610** input so that the detection circuit

610 produces an output signal that is proportional to the forward power output of the power amplifier 600.

The detection circuit 610 of the power amplifier 600 shown in FIG. 6 can be independent of the power amplifier 600 design parameters, which produces VSWR insensitive forward power detection in the power amplifier 600 output signal. The signal detected by the detection circuit 610 input on the input of the final gain stage 606 of the power amplifier 600 and the output signal that has been corrected for both amplitude and phase signal mismatch by the amplitude control circuit 612 and the phase control circuit 614 are summed in the detection circuit 610 independently of the performance characteristics inherent in the power amplifier 600. The detection circuit 610 operates separately from the power amplifier 600 in this example.

FIG. 7 shows another embodiment of a power amplifier 700 with a power detector 702 that detects power of a signal output from the power amplifier 700, in accordance with aspects of the disclosure. Similar to FIG. 6, the power amplifier 700 and the detector 702 are both located on the same chip 704. In this example, a final gain stage 706 of the power amplifier 700 has an input and an output and a feedback loop 708 coupled between the input and output. The detector 702 includes a detection circuit 710 that has a detection circuit input that is electrically coupled to a first phase control circuit 712 and a first amplitude control circuit 714. The input to the first phase control circuit 712 and the first amplitude control circuit 714 is electrically coupled to the input of the final gain stage 706 of the power amplifier 700.

The detection circuit 710 also includes a detection circuit output that is electrically coupled to a second phase control circuit 716 and a second amplitude control circuit 718. The output of the second phase control circuit 716 and the second amplitude control circuit 718 is electrically coupled to the output of the final gain stage 706 of the power amplifier 700. The order of both the first and second phase control 712, 716 and amplitude control circuits 714, 718 can be reversed. In a similar manner described above with reference to FIG. 6, the signal produced by the first phase and amplitude control circuits 712, 714 and the signal produced by the second phase and amplitude control circuits 716, 718 are summed in the detection circuit 710 to produce a summed RF signal. The summed RF signal has a power proportional to a forward power output of the power amplifier 700.

The phase control circuit 712 may be omitted while having the amplitude control circuit 714 remain electrically coupled to the final gain stage 706 input. The final gain stage of the power amplifier has an input and an output and a feedback loop coupled between the input and output, as described above. The detector includes a detection circuit that has a detection circuit input that is electrically coupled to a first amplitude control circuit. The input to the first amplitude control circuit is electrically coupled to the input of the final gain stage of the power amplifier. This detection circuit also includes a detection circuit output that is electrically coupled to a phase control circuit and a second amplitude control circuit that are electrically coupled together in series. The output of the phase control circuit and the second amplitude control circuit is electrically coupled to the output of the final gain stage of the power amplifier. The order of the phase and second amplitude control circuits can be reversed. The detection circuit is electrically coupled between a first amplitude control circuit and a combined second amplitude control circuit and a phase control circuit in this example. The gain stage output or the signal output by the power amplifier exhibits a VSWR that is greater than zero in any of the example power amplifiers and detectors described above.

Referring now to FIG. 8, an example summing detection circuit is disclosed that illustrates the detector shown in FIG. 7. The summing detection circuit includes a first phase and amplitude control circuit 804, a second phase and amplitude control circuit 806, a summing node 808, and a detection circuit 810. The input to the first phase and amplitude control circuit 804 is electrically coupled to the input 812 of the final gain stage of the power amplifier. The output 814 of the second phase and amplitude control circuit is electrically coupled to the output of the final gain stage of the power amplifier. The first phase and amplitude control circuit 804 includes a capacitor 816, a variable or selectable blocking capacitor 818, a transistor 820, and a current source 822. The second phase and amplitude control circuit 806 includes two capacitors 824, 826, a variable or selectable blocking capacitor 828, and a programmable resistor 830. The output of the first phase and amplitude control circuit 804 is electrically coupled or summed together with the input to the second phase and amplitude control circuit 806 at the summing node 808 of the detection circuit 810. FIG. 8 shows an example of a summing node 808, although summing the output of the first phase and amplitude control circuit 804 and the second phase and amplitude control circuit 806 can be accomplished in various manners.

The detection circuit 702 shown in FIG. 8 includes a rectifier 834, such as a diode or any other circuit element that can transform an RF signal into a DC voltage, a current source 836, and a capacitor 838. The output 840 of the detection circuit 702 is proportional to the RF signal output of the power amplifier. The detection circuit creates a direct current (DC) voltage that is proportional to the amplitude of the RF signal at the summing node 808. The DC voltage produced by the detection circuit 702 is also proportional to the voltage associated with the power of the signal output from the power amplifier. Because the signal is now a low frequency signal, i.e., a DC signal, it can be accurately communicated to other elements of the RF transmission system.

FIG. 9 shows an example of the second phase and amplitude control circuit 806 shown in FIG. 8. The blocking capacitor 828 includes a series of three capacitors 932, 934, 936 and respective switches that provide different capacitor values depending on which switches 938, 940, 942 are open and closed. The three capacitors 932, 934, 936 are electrically coupled together in parallel. The programmable resistor 832 includes a series of three resistors 944, 946, 948 and respective switches 950, 952, 954, which can be gate-controlled FETs in some examples. When all of the resistor switches 950, 952, 954 are open, the total resistance equals the sum of the values of all three resistors 944, 946, 948. When all of the resistor switches 950, 952, 954 are closed, the total resistance is the line resistance and the three resistors 944, 946, 948 add no resistance to the circuit. The resistance across the programmable resistor can be varied by opening and closing one or more of the switches 950, 952, 954, as desired. Because of the programmable nature of the phase and amplitude control circuit 806 shown in FIG. 9, the detector can be programmed in response to variations in power of an output signal of the power amplifier. For example, any of the phase and amplitude control circuits discussed above in reference to FIGS. 6-8 can have programmable components that can be programmed in response to variations in power of the output signal of the power amplifier.

FIG. 10 shows graphical representations of the performance improvement of forward power detection using the disclosed power amplifiers with power detectors. For each graph, the forward power is sampled along the X-axis and a constant voltage is plotted along the Y-axis. Each line repre-

sents a different load condition with a 3:1 VSWR (the magnitude of the mismatch) with a variable phase (60 degree steps). The first graph **1000** shows the final detector response to forward power and represents the amplitude of the RF signal input to the final gain stage of the power amplifier. The second graph **1002** represents the amplitude of the RF output voltage signal. The output voltage signal has much higher amplitude and greater variation for the same forward power than the amplitude and variation of the RF signal input to the final gain stage of the power amplifier.

The first graph **1000** shows a constant RF amplitude of 125 mV has nearly 1.9 dB of forward power variation, which represents forward power detection of a power amplifier without the disclosed detectors at **1004** and with the disclosed detectors at **1006**. A detector solution that relies solely on detecting RF amplitude at the input of the final gain stage of the power amplifier, such as the detector shown in FIG. **5**, cannot improve on this variation. The variation of the final detector output voltage, $V_{DET[0]}$, is only 1.4 dB for the same RF amplitude when the disclosed detector is used with the power amplifier. Likewise, the second graph shows a constant RF output amplitude having an 8 dB forward power variation in which the output values of measured without disclosed detectors at **1008** and with the disclosed detectors at **1010**. A detector that relied solely on detecting the RF amplitude at the output of the power amplifier, such as the detectors show in FIG. **4**, suffers from excessive variation of detector voltage for constant forward power. Power detection of the power amplifier using the disclosed detectors provide significant performance advantages over other possible solutions.

Methods of detecting forward power in a detection circuit coupled to a power amplifier are also disclosed. Such methods can include coupling, in series, a first amplitude control circuit to an input of a gain stage of a power amplifier to produce a corrected input signal, coupling, in series, a second amplitude control circuit and a second phase control circuit to an output of the gain stage of the power amplifier to produce a corrected output signal, summing the corrected input signal and the corrected output signal to produce a summed node signal that is proportional to the forward power output of the power amplifier, and applying the summed node signal to the detection circuit to detect the forward power output. In this example, the summed node signal can be an RF signal having a power. The method can also include producing a DC output signal having a power that is proportional to the summed node signal power. This output signal can have a VSWR that is greater than zero. Detecting the summed node signal can be performed independently of the VSWR variations in an output signal of the power amplifier, as described above.

Having described and illustrated the principles of the invention in a preferred embodiment thereof, it should be apparent that the invention can be modified in arrangement and detail without departing from such principles. We claim all modifications and variations coming within the spirit and scope of the following claims.

The invention claimed is:

1. A power amplifier with power detection, comprising:

a radio frequency (RF) power amplifier having a gain stage that includes a gain stage input, a gain stage output, and a feedback loop coupled between an input and an output of the power amplifier;

a detection circuit having a first detection circuit input electrically coupled to the gain stage input and having a detection circuit output;

an amplitude control circuit and a phase control circuit electrically coupled together in series between the gain stage output and a second detection circuit input;

wherein the amplitude control circuit and the phase control circuit produce a signal received by the second detection circuit input so that the detection circuit detects a signal at the output of the detection circuit that has a power proportional to a forward power output of the power amplifier.

2. The power detection device of claim **1**, wherein the amplitude control circuit is a first amplitude control circuit and further comprising a second amplitude control circuit that is electrically coupled in series between the first detection circuit input and the gain stage input.

3. The power detection device of claim **2**, wherein the phase control circuit is a first phase control circuit and further comprising a second phase control circuit that is electrically coupled in series between the first amplitude control circuit and the first detection circuit input.

4. The power detection device of claim **3**, wherein the output of the first phase control circuit and the output of the second phase control circuit are summed to produce a summed RF signal.

5. The power detection circuit of claim **1**, wherein the gain stage output of the power amplifier exhibits a voltage standing wave ratio (VSWR) that is greater than one.

6. The power detection circuit of claim **1**, wherein the power amplifier, the amplitude control circuit, the phase control circuit, and the detection circuit are each physically located together on an integrated circuit die.

7. A method of detecting forward power in a detection circuit coupled to a power amplifier, comprising:

coupling in series a first amplitude control circuit to an input of a gain stage of a power amplifier to produce a corrected input signal;

coupling in series a second amplitude control circuit and a second phase control circuit to an output of the gain stage of the power amplifier to produce a corrected output signal;

summing the corrected input signal and the corrected output signal to produce a summed node signal that is proportional to the forward power output of the power amplifier; and

applying the summed node signal to the detection circuit to detect the forward power output.

8. The method of claim **7**, wherein the summed node signal is a radio frequency (RF) signal having a power and further comprising producing a direct current (DC) output signal having a power that is proportional to the summed node signal power.

9. The method of claim **7**, further comprising coupling a first phase control circuit in series with the first amplitude control circuit between the gain stage input and the first amplitude control circuit.

10. The method of claim **7**, wherein the output signal of the power amplifier has a voltage standing wave ratio that is greater than one.

11. The method of claim **7**, wherein coupling a first amplitude control circuit to the input of the gain stage of the power amplifier, coupling the second amplitude control circuit and the second phase control circuit to the output of the gain stage of the power amplifier, and summing the corrected input signal and the corrected output signal occurs in parallel with a feedback loop of the gain stage of the power amplifier.

12. The method of claim **11**, further comprising detecting the summed node signal independently of VSWR variations in an output signal of the power amplifier.

13. The method of claim **12**, wherein coupling a first amplitude control circuit to an input of a gain stage of a power amplifier, coupling a second amplitude control circuit and a

second phase control circuit to an output of the gain stage of the power amplifier, summing the corrected input signal and the corrected output signal to produce a summed node signal, and detecting the summed node signal all occur on the same integrated circuit die.

14. The method of claim **7**, further comprising programming at least one of the first amplitude control circuit, the second amplitude control circuit, and the second phase control circuit in response to variations in power of an output signal of the power amplifier.

15. The method of claim **14**, wherein the first amplitude control circuit, the second amplitude control circuit, and the second phase control circuit each include a blocking capacitor.

16. The method of claim **15**, wherein the programming at least one of the first amplitude control circuit, the second amplitude control circuit, and the second phase control circuit includes adjusting the capacitance of the blocking capacitor.

17. The method of claim **7**, wherein the detecting the summed node signal includes receiving the corrected input signal and the corrected output signal at an input of a detection circuit.

* * * * *