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Attorneys for Plaintiff
BELL SEMICONDUCTOR, LLC

IN THE UNITED STATES DISTRICT COURT

FOR THE EASTERN DISTRICT OF CALIFORNIA

BELL SEMICONDUCTOR, LLC Plaintiff, v. KIOXIA AMERICA, INC. and KIOXIA CORPORATION, Defendant.	**Case No. 2:22-cv-01880-KJM-JDP** **FIRST AMENDED COMPLAINT** **JURY TRIAL DEMANDED**

Plaintiff Bell Semiconductor, LLC ("Bell Semic" or "Plaintiff") brings this Complaint against Defendant Kioxia America, Inc. and Kioxia Corporation (collectively, "Kioxia") for infringement of U.S. Patent No. 7,231,626 ("the '626 patent") and U.S. Patent No. 6,436,807 ("the '807 patent"). Plaintiff, on personal knowledge of its own acts, and on information and belief as to all others based on investigation, alleges as follows:

SUMMARY OF THE ACTION

1. This is a patent infringement suit relating to Kioxia's unauthorized and unlicensed use of the '626 patent and '807 patent. The circuit design methodologies claimed in the '626 patent and'807 patent are used by Kioxia in the production of one or more of its devices, including its SSD chips, TC58NC0L1XGSD PCIe Gen 4.0 NVMe SSD Controller ("Kioxia Accused Product").

2. Traditionally, the process flow for IC design is highly linear, with each phase of the design process depending on the previous steps. Accordingly, when revisions to portions of the physical design are made, as typically happens numerous times during the design process, all the subsequent steps typically need to be redone in their entirety for at least the layer, if not the entire device. This is because regardless of the size or extent of the revision to the physical design, the changes must be merged into a much larger integrated circuit design and then the remaining steps of the design process flow re-run.

3. Before the inventions claimed in the '626 patent, the typical turnaround time for implementing a change to the physical design for cutting edge devices was approximately one week regardless of the size of the change. This is extremely inefficient in most instances where the change relates to only a small fraction of the overall design. *See* Ex. A at 3:16–18 & Fig. 1.

4. The '626 patent's inventors solved this problem by defining a window that encloses a change specified by the revision to physical design. The window defines an area that is less than the area of the entire circuit design. Only the nets within that window are routed pursuant to the revision, leaving the remaining nets in the design unaffected. Then, the results of that incremental routing are inserted into a copy of the original IC design to produce a revised IC design that effects the physical design change without needing to redo the entire process flow.

5. Semiconductor devices include different kinds of materials to function as intended. For example, these devices typically include both metal (*i.e.*, conductor) and insulator materials, which are deposited or otherwise processed sequentially in layers to form the final device. These layers—and the interconnects and components formed within them—have gotten much smaller over time, increasing the performance of these devices dramatically. As a result, it has become even more important to keep the layers planar as the device is being built because defects and warpage can cause fabrication issues and malfunctioning of the device. Manufacturers use a process called Chemical Mechanical Planarization/Polishing ("CMP") to smooth out the surface of the device to prepare the device for further processing, such as deposition of another layer. This allows subsequent layers to be built and connected more easily with fewer opportunities for short circuits or other errors that render the device defective. CMP functions best when there is a certain density and variance of the same material on the surface of the chip. This is because different materials will be "polished" away at different rates, leading to erosion or dishing on the surface. To reduce this problem "dummy" material, also known as "dummy fill," is typically inserted into low-density regions of the device to increase the overall uniformity of the structures on the surface of the layer and reduce the density variability across the surface of the device. However, dummy fill can increase capacitance if it is placed too close to signal wires, which slows the transmission speed of signals and degrades the overall performance of the device.

6. Prior to development of the methodology described in the '807 patent, the placement of dummy fill in the open areas of the interconnect layer was performed based upon a predetermined set density. However, use of predetermined set densities was not ideal because it often resulted in unnecessary placement of dummy fill and increased capacitance. For example, if the density of an active interconnect feature was high in relation to an adjacent open area, then it would not be necessary to place dummy fill in the corresponding open area at the predetermined density.

7. Recognizing these drawbacks, as well as the importance of having a flat or planarized surface on the devices, Donald Cwynar, Sudhanshu Misra, Dennis Ouma, Vivek Saxena, and John Sharpe ("the '807 Inventors"), the inventors of the '807 patent, set out to develop a design process that would achieve uniform density throughout the interconnect layer.

8. The ’807 Inventors ultimately conceived of a method for making the layout for an interconnect layout that allows for uniform density throughout the layer and facilitates planarization during manufacturing of the device. The claimed invention begins by determining an active interconnect feature density for each of a plurality of layout regions of the interconnect layout. Dummy fill is then added to each layout region in order to obtain a desired density of active interconnect features and dummy fill features in order to facilitate uniformity of planarization. In order to add dummy fill in this manner, one must define a minimum dummy fill feature lateral dimension based upon a dielectric layer deposition bias for a dielectric layer to be deposited over the interconnect layer.

9. The inventions disclosed in the ’807 patent provide many advantages over the prior art. In particular, having a uniform density for each layout region facilitates uniformity of planarization during manufacturing of the semiconductor device. *See* Ex. D at 3:3-5, 5:9–12. Furthermore, adding dummy fill features to obtain a desired density of active interconnect features and dummy fill features also helps ensure that dummy fill features are not unnecessarily added. *Id.* at 2:63-67, 5:19-22. Avoiding unnecessary dummy fill features is desirable because it deceases the parasitic capacitance of the interconnect layer. *Id.* at 2:67-3:2, 5:22-24. The invention claimed in the ’807 patent also provides for the selective positioning of dummy fill features, which minimizes parasitic capacitance. *Id.* at 5:28-33. These significant advantages are achieved through the use of the patented inventions and thus the ’807 patent presents significant commercial value for companies like Kioxia.

10. Bell Semic brings this action to put a stop to Kioxia’s unauthorized and unlicensed use of the inventions claimed in the ’626 and ’807 patents.

THE PARTIES

11. Plaintiff Bell Semic is a limited liability company organized under the laws of the State of Delaware with a place of business at One West Broad Street, Suite 901, Bethlehem, PA 18018.

12. Bell Semic stems from a long pedigree that began at Bell Labs. Bell Labs sprung out of the Bell System as a research and development laboratory, and eventually became known as one of America’s greatest technology incubators. Bell Labs employees invented the transistor in 1947 in Murray Hill, New Jersey. It was widely considered one of the most important technological breakthroughs of the time, earning the inventors the Nobel Prize in Physics. Bell Labs made the first

commercial transistors at a plant in Allentown, Pennsylvania. For decades, Bell Labs licensed its transistor patents to companies throughout the world, creating a technological boom that led to the use of transistors in the semiconductor devices prevalent in most electronic devices today.

13. Bell Semic, a successor to Bell Labs' pioneering efforts, owns over 1,900 worldwide patents and applications, approximately 1,500 of which are active United States patents. This patent portfolio of semiconductor–related inventions was developed over many years by some of the world's leading semiconductor companies, including Bell Labs, Lucent Technologies, Agere Systems, and LSI Logic and LSI Corporation ("LSI"). This portfolio reflects technology that underlies many important innovations in the development of semiconductors and integrated circuits for high–tech products, including smartphones, computers, wearables, digital signal processors, IoT devices, automobiles, broadband carrier access, switches, network processors, and wireless connectors.

14. The principals of Bell Semic all worked at Bell Labs' Allentown facility, and have continued the rich tradition of innovating, licensing, and helping the industry at large since those early days at Bell Labs. For example, Bell Semic's CTO was a LSI Fellow and Broadcom Fellow. He is known throughout the world as an innovator with more than 300 patents to his name, and he has a sterling reputation for helping semiconductor fabs improve their efficiency. Bell Semic's CEO took a brief hiatus from the semiconductor world to work with Nortel Networks in the telecom industry during its bankruptcy. His efforts saved the pensions of tens of thousands of Nortel retirees and employees. In addition, several Bell Semic executives previously served as engineers at many of these companies and were personally involved in creating the ideas claimed throughout Bell Semic's extensive patent portfolio.

15. On information and belief, Kioxia America, Inc. has its principal place of business and headquarters at 2610 Orchard Parkway, San Jose, California 95134. On information and belief, Kioxia Corporation has its principal place of business and headquarters at 3-1-21, Shibaura, Minato-ku, Tokyo 108-0023, Japan. On information and belief, Kioxia America is a subsidiary of or otherwise controlled by Kioxia Corporation.

16. On information and belief, Kioxia develops, designs, and/or manufactures products in the United States, including in this District, according to the '626 and '807 patented

processes/methodologies; and/or uses the '626 and '807 patented processes/methodologies in the United States, including in this District, to make products; and/or distributes, markets, sells, or offers to sell in the United States and/or imports products into the United States, including in this District, that were manufactured or otherwise produced using the patented process. Additionally, Kioxia introduces those products into the stream of commerce knowing that they will be sold and/or used in this District and elsewhere in the United States.

JURISDICTION AND VENUE

17. This is an action for patent infringement arising under the Patent Laws of the United States, Title 35 of the United States Code. Accordingly, this Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

18. This Court has personal jurisdiction over Kioxia under the laws of the State of California, due at least to its substantial business in California and in this District. Kioxia has purposefully and voluntarily availed itself of the privileges of conducting business in the United States, in the State of California, and in this District by continuously and systematically placing goods into the stream of commerce through an established distribution channel with the expectation that they will be purchased by consumers in this District. In the State of California and in this District, Kioxia, directly or through intermediaries: (i) performs at least a portion of the infringements alleged herein; (ii) develops, designs, and/or manufactures products according to the '626 and '807 patented processes/methodologies; (iii) distributes, markets, sells, or offers to sell products formed according to the '626 and '807 patented processes/methodologies; and/or (iv) imports products formed according to the '626 and '807 patented processes/methodologies.

19. On information and belief, venue is proper in this Court pursuant to 28 U.S.C. §§ 1391 and 1400 because Kioxia has committed, and continues to commit, acts of infringement in this District and has a regular and established place of business in this District. For example, Kioxia a regular and established place of business located in this District at 35 Iron Point Cir, Folsom, CA 95630.

20. Currently, Kioxia is advertising more than 2 jobs at the Folsom location. These positions include those that relate to the patented processes/methodologies, such as positions for a Principal Validation Engineer and ASIC Design Engineer. *See Job Search*, Kioxia

(https://americas.kioxia.com/en-us/careers.html) (last visited O, 2022). Moreover, on information and belief, Kioxia employs close to 25 engineers in the Folsom area. *See Search Results for Current Kioxia Employees*, LinkedIn (available at https://www.linkedin.com/search/results/people/?currentCompany=%5B%2228493031%22%5D&geoUrn=%5B%22107149401%22%5D&keywords=engineer&origin=FACETED_SEARCH&sid=MYK&title=engineer) (last visited Oct. 17, 2022).

21. Venue is also convenient in this District. This is at least true because of this District's close ties to this case—including the technology, relevant witnesses, and sources of proof noted above—and its ability to quickly and efficiently move this case to resolution.

22. On information and belief, Bell Semic's causes of action arise directly from Kioxia's circuit design work and other activities in this District. Moreover, on information and belief, Kioxia has derived substantial revenues from its infringing acts occurring within the State of Kioxia and within this District.

U.S. PATENT NO. 7,231,626

23. Bell Semiconductor owns by assignment the entire right, title, and interest in the '626 patent, entitled "Method Of Implementing An Engineering Change Order In An Integrated Circuit Design By Windows."

24. A true and correct copy of the '626 patent is attached as Exhibit A.

25. The '626 patent issued to inventors Jason K. Hoff, Viswanathan Lakshmanan, Michael Josephides, Daniel W. Prevedel, Richard D. Blinne, and Johathan P. Kuppinger.

26. The application that resulted in issuance of the'626 patent, United States Patent Application No. 11/015,123, was filed December 17, 2004. It issued on June 12, 2007 and expires on July 26, 2025.

27. The '626 patent generally relates to "methods of implementing an engineering change order (ECO) in an integrated circuit design." Ex. A at 1:1–13.

28. The background section of the '626 patent identifies the shortcomings of the prior art. More specifically, the specification describes that the prior circuit design methodology was disadvantageous because "[i]n previous methods for implementing an engineering change order

(ECO) request in an integrated circuit design, design tools are run for the entire integrated circuit design, even though the engineering change order typically is only a small fraction of the size of the integrated circuit design" Ex. A at 2:15–19.

29. The '626 patent elaborates that because "cell placement, routing, design rule check validation, and timing closure run times typically scale with the size of the entire integrated circuit design," Ex. A at 2:20–22, this produced a "typical turnaround time" of "about one week regardless of the size of the engineering change order. . . . because although the engineering change order may only have a size of a few cells, it must be merged with an integrated circuit design that typically has a much greater size." *Id.* at 2:37–44. Certain of these steps "may be especially time consuming and resource intensive." *Id.* at 3:16–17.

30. The inventions disclosed in the '626 patent provide many advantages over the prior art. In particular, they provide a simple and efficient method for ensuring that revisions to the physical design of the IC do not unduly delay the completion of the design process. As the '626 patent explains, "significant savings in the resources required to perform routing, design rule check verification, net delay calculation, and parasitic extraction may be realized by creating windows in the integrated circuit design that include only the incremental changes to the overall integrated circuit design." Ex. A at 3:19–23.

31. As mentioned above, this is very beneficial because it substantially reduces the run time of the routing tools and related follow-on steps of the layout portion of the design process flow (such as calculation of net delay, design rule check, and parasitic extraction). Thus, it shortens the overall design timeline, and avoids cost overruns and delays, making it less costly to make changes later in the design process or more often. *See id.*

32. Given the aforementioned increased complexity of circuit designs and the corresponding delays from design changes, these efficiency gains have become more and more important in completing the design process without affecting time-to-market. These significant advantages are achieved through the use of the patented inventions and thus the '626 patent presents significant commercial value for chip designers.

33. In light of the drawbacks of the prior art, the '626 patent's inventors recognized the

need for a circuit design methodology in which the time required to implement an ECO "depend[s] on the number of net changes in the [ECO] rather than on the total number of nets in the entire integrated circuit design." Ex. A at 2:51–53. The inventions claimed in the'626 patent address this need.

34. The '626 patent contains two independent claims and 8 total claims, covering a method and computer readable medium for implementing a change order in an integrated circuit design. Claim 1 reads:

> 1. A method comprising steps of:
>
> (a) receiving as input an integrated circuit design;
>
> (b) receiving as input an engineering change order to the integrated circuit design;
>
> (c) creating at least one window in the integrated circuit design that encloses a change to the integrated circuit design introduced by the engineering change order wherein the window is bounded by coordinates that define an area that is less than an entire area of the integrated circuit design;
>
> (d) performing an incremental routing of the integrated circuit design only for each net in the integrated circuit design that is enclosed by the window;
>
> (e) replacing an area in a copy of the integrated circuit design that is bounded by the coordinates of the window with results of the incremental routing to generate a revised integrated circuit design; and
>
> (f) generating as output the revised integrated circuit design.

35. This claim, as a whole, provides significant benefits and improvements to the function of the semiconductor device design process, *e.g.,* providing a novel and substantially more efficient process flow in which only the affected nets would be considered in the incremental routing. This results in substantial reduction in the expected time of the design portion of producing semiconductor devices.

36. The claims of the '626 patent also recite inventive concepts that improve the functioning of the fabrication process, particularly as to post-ECO routing. The claims of the '626 patent disclose a new and novel solution to specific problems related to improving semiconductor

fabrication. As explained in detail above and in the '626 patent specification, the claimed inventions improve upon the prior art processes by ignoring nets that are unaffected by an ECO in performing routing following the ECO. This has the advantage of substantially reducing the impact on design schedule of ECOs and other layout changes, thus increasing the efficiency of the design process and making it easier to improve the design and fix design errors without unduly delaying time-to-market. By making it easier to fix errors as they are found, and causing substantially less incremental delay upon finding and fixing errors, the claimed inventive processes also increase the performance and reliability of the finished product. Because of the claimed inventive processes, individual less impactful design issues that still impact design performance (albeit not on a critical scale) can be caught and fixed without costing the same delay as more substantial errors.

U.S. PATENT NO. 6,436,807

37. Bell Semic is the owner by assignment of the '807 patent. The '807 patent is titled "Method for Making an Interconnect Layer and a Semiconductor Device Including the Same." The '807 patent issued on August 20, 2002. A true and correct copy of the '807 patent is attached as Exhibit D.

38. The inventors of the '807 patent are Donald Cwynar, Sudhanshu Misra, Dennis Ouma, Vivek Saxena, and John Sharpe.

39. The application that resulted in the issuance of the '807 patent was filed on January 18, 2000. The '807 patent claims priority to January 18, 2000.

40. The '807 patent generally relates to "a method for making a layout for an interconnect layer that has uniform density throughout to facilitate planarization during manufacturing of a semiconductor device." Ex. D at 2:43-46. The background section of the '807 patent identifies the shortcomings of the prior art. More specifically, the specification describes that the prior circuit design methodology was disadvantageous because it could lead to "protrusions[] in the upper surface of the dielectric material[] above respective active interconnect features[.]" *Id.* at 1:40-42. The specification states that "if pattern density variations of the active interconnect features[] are large, CMP is not adequate to sufficiently planarize the interconnect layer[.]" *Id.* at 1:67-2:2. Although "[c]onventional layout algorithms" were typically used to place dummy fill features in open areas of the interconnect

layer, those algorithms placed dummy metal "based upon a predetermined set density." *Id.* at 2:17-21. Relying on "predetermined set densit[ies]" could lead to the unnecessary placement of dummy fill features, which in turn could increase the parasitic capacitance of the interconnect layer. *Id.* at 2:31-33. The specification notes that "variations in the density of the interconnect layer [could] cause deviations when the interconnect layer [was] planarized." *Id.* at 2:35-37.

41. In light of the drawbacks of the prior art, the '807 Inventors recognized "a need for making a layout for an interconnect layer that determines placement of dummy fill features for achieving a uniform density throughout the interconnect layer." Ex. D at 2:37–40. The inventions claimed in the '807 patent address this need.

42. The '807 patent contains two independent claims and 18 total claims. Claim 1 reads:

> 1. A method for making a layout for an interconnect layer of a semiconductor device to facilitate uniformity of planarization during manufacture of the semiconductor device, the method comprising the steps of:
>
> (a) determining an active interconnect feature density for each of a plurality of layout regions of the interconnect layout; and
>
> (b) adding dummy fill features to each layout region to obtain a desired density of active interconnect features and dummy fill features to facilitate uniformity of planarization during manufacturing of the semiconductor device, the adding comprising defining a minimum dummy fill feature lateral dimension based upon a dielectric layer deposition bias for a dielectric layer to be deposited over the interconnect layer.

43. This claim, as a whole, provides significant benefits and improvements to the function of the semiconductor device, *e.g.,* uniform planarization during manufacturing, avoidance of adding unnecessary dummy fill features, and minimizing parasitic capacitance. *See, e.g.*, Ex. D at 5:9–34.

44. The claims of the '807 patent also recite inventive concepts that improve the functioning of the fabrication process, particularly as to dummy filling. The claims of the '807 patent disclose a new and novel solution to specific problems related to improving semiconductor fabrication. As explained in detail above and in the '807 patent specification, the claimed inventions improve upon

the prior art processes by determining an active interconnect feature density for each of a plurality of layout regions of the interconnect layout and adding dummy fill to each layout region to obtain a desired density of active interconnect features and dummy fill features to facilitate uniformity of planarization. This has advantages such as avoiding the unnecessary adding of dummy fill features and minimizing the parasitic capacitance of the interconnect layer.

COUNT I – INFRINGEMENT OF U.S. PATENT NO. 7,231,626

45. Bell Semic re-alleges and incorporates by reference the allegations of the foregoing paragraphs as if fully set forth herein.

46. The ’626 patent is valid and enforceable under the United States Patent Laws.

47. Bell Semic owns, by assignment, all right, title, and interest in and to the ’626 patent, including the right to collect for past damages.

48. A copy of the ’626 patent is attached at Exhibit A.

49. On information and belief, Kioxia has and continues to directly infringe pursuant to 35 U.S.C. § 271(a) one or more claims of the ’626 patent by using the patented methodology to design one or more semiconductor devices, including as one example the Kioxia Accused Product, in the United States.

50. On information and belief, Kioxia employs a variety of design tools, for example, Cadence, Synopsys, and/or Siemens tools, to perform incremental routing in implementing an ECO (the “Accused Processes”) as recited in the ’626 patent claims. As one example, Kioxia’s Accused Processes perform a method for only routing the nets affected by the ECO and merging that changed area into the overall circuit layout as required by claim 1 of the ’626 patent. Kioxia does so by employing a design tool, such as at least one of a Cadence, Synopsys, and/or Siemens tool, to perform incremental routing as part of implementing an ECO for the Kioxia Accused Product to generate a revised integrated circuit design.

51. Kioxia’s Accused Processes also calculate and perform a parasitic extraction only for each net in the IC design enclosed by the window defining the ECO. (This parasitic extraction is also how the Accused Processes further calculate a net delay only for each net in the IC design enclosed by the window defining the ECO.) Kioxia does so by employing a design tool, such as at least one of

the Cadence, Synopsys, and/or Siemens tools, to perform the incremental routing during implementation of the ECO for the Kioxia Accused Product's circuit designs.

52. Kioxia's Accused Processes also perform a design rule check only for each net in the IC design enclosed by the ECO window. Kioxia does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, perform the incremental ECO and automatically perform a DRC for those nets to ensure that the ECO did not violate any design rules when it fixed other issues.

53. An exemplary infringement analysis showing infringement of one or more claims of the '626 patent is set forth in Exhibit B. The declaration of Lloyd Linder, an expert in the field of semiconductor device design, is attached at Exhibit C and further describes Kioxia's infringement of the '626 patent.

54. Kioxia's Accused Processes infringe and continue to infringe one or more claims of the '626 patent during the pendency of the '626 patent.

55. On information and belief, Kioxia has and continues to infringe pursuant to 35 U.S.C. § 271, *et. seq.*, directly, either literally or under the doctrine of equivalents, by using the Accused Processes in violation of one or more claims of the '626 patent. Kioxia has and continues to infringe pursuant to 35 U.S.C. § 271, *et. seq.*, directly, either literally or under the doctrine of equivalents, by making, selling, or offering to sell in the United States, or importing into the United States products manufactured or otherwise produced using the Accused Processes in violation of one or more claims of the '626 patent.

56. Kioxia's infringement of the '626 patent is exceptional and entitles Bell Semic to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

57. Bell Semic has been damaged by Kioxia's infringement of the '626 patent and will continue to be damaged unless Kioxia is enjoined by this Court. Bell Semic has suffered and continues to suffer irreparable injury for which there is no adequate remedy at law. The balance of hardships favors Bell Semic, and public interest is not disserved by an injunction.

58. Bell Semic is entitled to recover from Kioxia all damages that Bell Semic has sustained as a result of Kioxia's infringement of the '626 patent, including without limitation and/or not less

than a reasonable royalty.

COUNT II – INFRINGEMENT OF U.S. PATENT NO. 6,436,807

59. Bell Semic re-alleges and incorporates by reference the allegations of the foregoing paragraphs as if fully set forth herein.

60. The ’807 patent is valid and enforceable under the United States Patent Laws.

61. Bell Semic owns, by assignment, all right, title, and interest in and to the ’807 patent, including the right to collect for past damages.

62. A copy of the ’807 patent is attached at Exhibit D.

63. On information and belief, Kioxia has and continues to directly infringe pursuant to 35 U.S.C. § 271(a) one or more claims of the ’807 patent by using the patented methodology to design one or more semiconductor devices, including as one example the Accused Product, in the United States.

64. On information and belief, Kioxia employs a variety of design tools, for example, Cadence, Synopsys, and/or Siemens tools, to make a layout for an interconnect layer of a semiconductor device (the “Accused Processes”) as recited in the ’807 patent claims. As one example, Kioxia’s Accused Processes perform a method for making a layout for an interconnect layer of a semiconductor device, where the layout facilitates uniformity of planarization during manufacture of the semiconductor device as required by claim 1 of the ’807 patent. Kioxia does so by employing a design tool, such as at least one of a Cadence, Synopsys, and/or Siemens tool, to make a layout for the interconnect layer of its Accused Product. The Accused Product’s layout facilitates uniformity of planarization during manufacture of the device.

65. Kioxia’s Accused Processes also determine an active interconnect feature density for each of a plurality of layout regions of the interconnect layout. Kioxia does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, to determine an active interconnect feature density for each of a plurality of layout regions of the interconnect layout of its Accused Product.

66. Kioxia’s Accused Processes also add dummy fill features to each layout region to obtain a desired density of active interconnect features and dummy fill features to facilitate uniformity

of planarization during manufacturing of the semiconductor device, the adding comprising defining a minimum dummy fill feature lateral dimension based upon a dielectric layer deposition bias for a dielectric layer to be deposited over the interconnect layer.

67. Kioxia does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, to add dummy fill features to each layout region to obtain a desired density of active interconnect features and dummy fill features to facilitate uniformity of planarization during manufacturing of the semiconductor device. The adding of dummy fill through the use of these design tools comprises defining a minimum dummy fill feature lateral dimension based upon a dielectric layer deposition bias for a dielectric layer to be deposited over the interconnect layer. An exemplary infringement analysis showing infringement of one or more claims of the ’807 patent is set forth in Exhibit E. The declaration of Lloyd Linder, an expert in the field of semiconductor device design, is attached at Exhibit F and further describes Kioxia’s infringement of the ’807 patent.

68. Kioxia’s Accused Processes infringe and continue to infringe one or more claims of the ’807 patent during the pendency of the ’807 patent.

69. On information and belief, Kioxia has and continues to infringe pursuant to 35 U.S.C. § 271, *et. seq.*, directly, either literally or under the doctrine of equivalents, by using the Accused Processes in violation of one or more claims of the ’807 patent. Kioxia has and continues to infringe pursuant to 35 U.S.C. § 271, *et. seq.*, directly, either literally or under the doctrine of equivalents, by making, selling, or offering to sell in the United States, or importing into the United States products manufactured or otherwise produced using the Accused Processes in violation of one or more claims of the ’807 patent.

70. Kioxia’s infringement of the ’807 patent is exceptional and entitles Bell Semic to attorneys’ fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

71. Bell Semic has been damaged by Kioxia’s infringement of the ’807 patent and will continue to be damaged unless Kioxia is enjoined by this Court. Bell Semic has suffered and continues to suffer irreparable injury for which there is no adequate remedy at law. The balance of hardships favors Bell Semic, and public interest is not disserved by an injunction.

72. Bell Semic is entitled to recover from Kioxia all damages that Bell Semic has sustained

as a result of Kioxia's infringement of the '807 patent, including without limitation and/or not less than a reasonable royalty.

PRAYER FOR RELIEF

WHEREFORE, Bell Semic respectfully requests that this Court enter judgment in its favor as follows and award Bell Semic the following relief:

(a) a judgment declaring that Kioxia has infringed one or more claims of the '626 patent and '807 patent in this litigation pursuant to 35 U.S.C. § 271, *et seq.*;

(b) an award of damages adequate to compensate Bell Semic for infringement of the '626 patent and '807 patent by Kioxia, in an amount to be proven at trial, including supplemental post-verdict damages until such time as Kioxia ceases its infringing conduct;

(c) a permanent injunction, pursuant to 35 U.S.C. § 283, prohibiting Kioxia and its officers, directors, employees, agents, consultants, contractors, suppliers, distributors, all affiliated entities, and all others acting in privity with Kioxia from committing further acts of infringement;

(d) a judgment requiring Kioxia to make an accounting of damages resulting from Kioxia's infringement of the '626 patent and '807 patent;

(e) the costs of this action, as well as attorneys' fees as provided by 35 U.S.C. § 285;

(f) pre-judgment and post-judgment interest at the maximum amount permitted by law;

(g) all other relief, in law or equity, to which Bell Semic is entitled.

DEMAND FOR JURY TRIAL

Plaintiff hereby demands a jury trial for all issues so triable.

DATED: November 23, 2022

/s/ Michael Miguel

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