

1 RUSS, AUGUST & KABAT
Brian D. Ledahl, SBN 186579
2 bledahl@raklaw.com
Paul A. Kroeger, SBN 229074
3 pkroeger@raklaw.com
12424 Wilshire Boulevard
Twelfth Floor
4 Los Angeles, California 90025
Telephone: (310) 826-7474
5 Facsimile: (310) 826-6991

6 Attorneys for Plaintiff
LONGITUDE LICENSING LIMITED
7

8 **UNITED STATES DISTRICT COURT
CENTRAL DISTRICT OF CALIFORNIA**

9 LONGITUDE LICENSING LIMITED,

10 Plaintiff,

11 v.

12 ACER, INC. and ACER AMERICA
13 CORP.,

14 Defendants.

Case No

**COMPLAINT FOR PATENT
INFRINGEMENT**

JURY TRIAL DEMANDED

RUSS, AUGUST & KABAT

RUSS, AUGUST & KABAT

1 1. Plaintiff Longitude Licensing Limited (“Longitude” or “Plaintiff”) for its
2 Complaint against Defendants Acer, Inc. and Acer America Corp. (“Acer America”)
3 (Acer, Inc. and Acer America are collectively referred to as “Acer” or
4 “Defendants”), hereby alleges as follows:

5 **PARTIES**

6 2. Longitude is an entity formed under the laws of Ireland with its principal place
7 of business at Plaza 255 Suite 2A, Blanchardstown Corporate Park 2, Dublin D15
8 YH6H, Ireland.

9 3. On information and belief, Defendant Acer Inc. is a corporation
10 organized under the laws of Taiwan, with its principal place of business at 7F-5 No.
11 369, Fuxing N. Rd., Taipei City 10541, Taiwan. Acer Inc. does substantial business
12 on an ongoing basis in the United States, including in this State and in this District.
13 On information and belief, Acer Inc. causes and controls the sale, offer for sale, and
14 distribution of its products in the State of California and in this District.

15 4. On information and belief, Defendant Acer America is a California
16 corporation with its principal place of business at 1730 N. 1st Street, Suite 400, San
17 Jose CA 95112. Acer America is a wholly owned subsidiary of Acer, Inc., and
18 imports the accused products into the United States for Acer Inc.

19 **NATURE OF THE ACTION**

20 5. This is a civil action for the infringement of United States Patent Nos.
21 7,697,369 (the “369 patent”), 9,379,233 (the “233 patent”), and RE43,539 the
22 “539 Patent) (collectively, the “Patents-in-Suit”) under the patent laws of the United
23 States, 35 U.S.C. § 1, et seq.

24 6. This action involves Defendants’ manufacture, use, sale, offer for sale, and/or
25 importation into the United States of infringing products, methods, processes,
26 services and systems that incorporate certain memory chips and components that
27 infringe one or more of the claims of the Patents-in-Suit.
28

JURISDICTION AND VENUE

7. This Court has original jurisdiction over the subject matter of this Complaint under 28 U.S.C. §§ 1331 and 1338(a) because this action arises under the patent laws of the United States, including 35 U.S.C. §§ 271, et seq.

8. Defendants are subject to personal jurisdiction in this judicial district because Defendants regularly transact business in this judicial district by, among other things, offering Defendants’ products and services to customers, business affiliates and partners located in this judicial district. In addition, Defendants have committed acts of direct infringement of one or more of the claims of one or more of the Patents-in-Suit in this judicial district.

9. Venue in this district is proper under 28 U.S.C. §§ 1400(b) and 1391(b) and (c), because Defendants are subject to personal jurisdiction in this district and have committed acts of infringement in this district. LinkedIn profiles of several Acer America employees indicate that they reside in this District. Acer, Inc. is a foreign corporation organized under the laws of Taiwan, with a principal place of business in Taiwan. Accordingly, venue is proper in this District over Defendants.

FACTUAL BACKGROUND

10. Longitude operates in one of the most dynamic segments of the international knowledge-based economy. Longitude operates by partnering with patent owners to prosecute and license patent portfolios. The company has also formed customized arrangements that combine exclusive licensing rights and ownership positions, and it also has acquired patents outright from other global patent owners. Longitude has the licensing rights to portfolios totaling nearly 4,000 semiconductor and computer memory patents and patent applications originally filed by well-known technology companies.

11. Longitude is the owner by assignment of the patents-in-suit.

12. Longitude has licensed the patents-in-suit to a majority of the worldwide memory industry responsible for solid state memory devices used in products sold

RUSS, AUGUST & KABAT

RUSS, AUGUST & KABAT

1 in the United States, including SK Hynix, Kingston, Winbond, Micron, Samsung
2 Electronics and Kioxia (formerly the memory division of Toshiba).

3 13. One major player in the industry that has refused to license the Patent-in-Suit
4 is Western Digital Corporation (“Western Digital”). Western Digital is a computer
5 hard disk drive manufacturer and data storage company. Western Digital designs,
6 manufactures, and sells data technology products, including storage devices, data
7 center systems, and cloud storage services. Longitude is informed and believes that
8 Western Digital acquired SanDisk in 2016.

9 14. Since February 2018, Longitude has requested that Western Digital negotiate
10 licenses for patents (including the Patents-in-Suit) that it is infringing, but Western
11 Digital has refused to negotiate, claiming that Longitude may not assert its licensing
12 rights as a result of covenants in two contracts between Western Digital and third
13 parties that have never owned any of the patents-in-suit. Those contracts do not
14 apply to Longitude, but Western Digital nonetheless contended that it could only be
15 sued after every other market participant (apparently including Western Digital’s
16 customers) was sued.

17 15. Longitude initiated an arbitration claim against Western Digital for
18 declaratory relief concerning Western Digital’s interpretation of the agreements.
19 Western Digital objected to the jurisdiction of the arbitration tribunal to avoid any
20 consideration of the merits of contract arguments.

21 16. After the arbitration against Western Digital was dismissed on jurisdictional
22 grounds, Longitude gave notice to Defendants that they were infringing the patents-
23 in-suit by letter dated September 6, 2022. This letter included a table that identified
24 a number of products that were believed to infringe the patents. Among other things,
25 the letter stated:

26 A number of Acer products incorporate and use features and
27 functionality covered by Longitude patents, including, for example,
28 the patents and exemplary products identified in the attached table
 (“Table 1”). In reviewing the Table, you will note that the infringing
 products contain devices manufactured by Western Digital
 Corporation (“Western Digital”). While our normal approach is to

RUSS, AUGUST & KABAT

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28

engage with, and license, suppliers such as Western Digital rather than their customers, Western Digital has refused to engage in any licensing discussions. Consequently, we are contacting Western Digital customers who are selling products that infringe Longitude patents.

17. Defendants did not take a license following receipt of this letter and continued to infringe as stated in the letter. As of the filing of this Complaint, Defendants have not responded in any manner to Longitude.

18. Among the other products referenced in the letter was the Acer Aspire 5 and Nitro 5 computers as well as other Acer computers, laptops, and tablets having Western Digital SSDs.

THE PATENTS-IN-SUIT

19. Longitude is the owner by assignment of the Patents-in-Suit. Longitude owns all rights to the Patents-in-Suit, including the right to enforce the Patents-in-Suit.

20. All maintenance fees for the Patents-in-Suit have been timely paid, and there are no fees currently due.

21. United States Patent No. 7,697,369, entitled "System with Controller and Memory," issued on April 13, 2010 from United States Patent Application No. 11/759,862 filed on June 7, 2007.

22. United States Patent No. RE43,539, entitled "Output Buffer Circuit and Integrated Semiconductor Circuit Device With Such Output Buffer Circuit," issued on July 24, 2012 from United States Patent Application No. 11/798,773 filed on May 16, 2007. The '539 Patent is a re-issue of U.S. Patent No. 6,894,547, which issued on May 17, 2005 from United States Patent Application No. 10/320,059 filed December 16, 2002.

23. United States Patent No. 9,379,233, entitled "Semiconductor Device," issued on June 28, 2016 from United States Patent Application No. 14/872,844 filed October 1, 2015.

COUNT I

(DEFENDANTS' INFRINGEMENT OF THE '369 PATENT)

24.Paragraphs 1 through 23 are incorporated by reference as if fully restated herein.

25.United States Patent No. 7,697,369, entitled "System with Controller and Memory," issued on April 13, 2010 from United States Patent Application No. 11/759,862 filed on June 7, 2007.

26.Longitude is the owner of the '369 patent with full rights to pursue recovery of royalties for damages for infringement, including full rights to recover past and future damages.

27.Each claim of the '369 patent is valid, enforceable, and patent-eligible.

28.Longitude and its predecessors in interest have satisfied the requirements of 35 U.S.C. § 287(a) with respect to the '369 patent, and Longitude is entitled to damages for Defendants' past infringement. Among other things, Longitude provided actual notice of infringement to the component supplier, Western Digital.

29.Defendants have directly infringed (literally and equivalently) and induced others to infringe the '369 patent by making, using, selling, offering for sale, or importing products that infringe the claims of the '369 patent and by inducing others to infringe the claims of the '369 patent without a license or permission from Longitude. These products include without limitation all Acer Aspire 5 computers (e.g. model A515-56-74PH), Nitro 5 computers (e.g. model AN515055055M1) and all other Acer computers, laptops, and tablets having Western Digital PC SN530 NVMe SSDs, Western Digital SSDs, and/or Western Digital NAND memory chips and all versions and variations of them offered for sale since the issuance of the '369 patent.

30.A non-limiting example of Defendants' infringement is the Acer Aspire 5 computer which infringes at least claim 1 of the '369 patent. Exemplary photographs of the Acer Aspire 5 computer, and its packaging are set forth below:

RUSS, AUGUST & KABAT

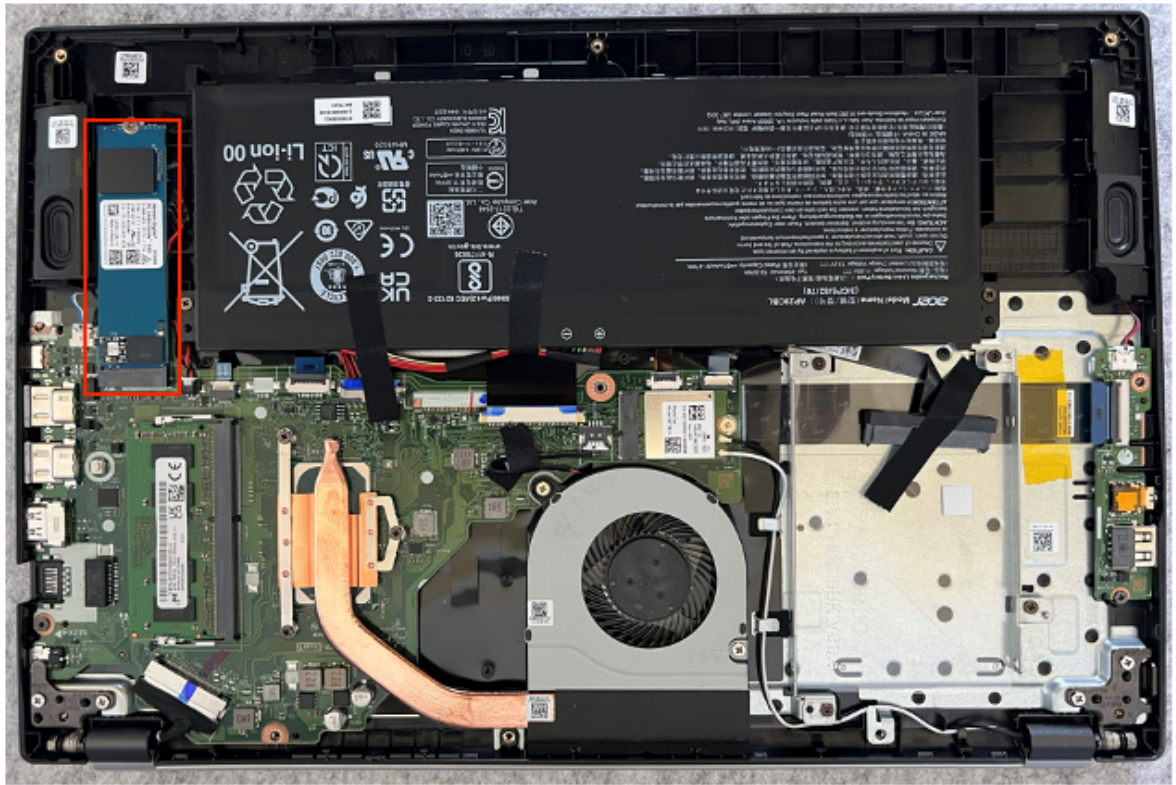
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28



31. The Acer Aspire 5 computer includes the Western Digital PC SN530 NVMe SSD as shown below:

RUSS, AUGUST & KABAT

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28



RUSS, AUGUST & KABAT

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28



32. Longitude is informed and believes that the Western Digital PC SN530 NVMe SSD Operates in Compliance with the Open NAND Flash Interface Specification, Revision 4.0 dated April 2, 2014 (ONFI Standard).

33. The Western Digital PC SN530 NVMe SSD is a system:

RUSS, AUGUST & KABAT

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28

A system [A]



34. The Western Digital PC SN530 NVMe SSD includes a controller:

SanDisk 20-82-10023-A1
SSD Controller

a controller [B]



35. The Western Digital PC SN530 NVMe SSD includes a controller that is adapted to send out a first strobe signal and a write data signal in a write operation, the write data signal being synchronized with the first data strobe signal:

RUSS, AUGUST & KABAT

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28

| Signal Name | Input / Output | Description |
|-------------------------------|----------------|---|
| ALE_x | I | Address Latch Enable The Address Latch Enable signal is one of the signals used by the host to indicate the type of bus cycle (command, address, data). Refer to section 4.3. |
| WE_x_n | I | Write Enable The Write Enable signal controls the latching of commands, addresses, and input data in the SDR data interface. The Write Enable signal controls the latching of commands and addresses in the NV-DDR2 or NV-DDR3 data interface. Data, commands, and addresses are latched on the rising edge of WE_x_n. This signal shares the same pin as CLK_x in the NV-DDR data interface. |
| CLK_x | I | Clock The Clock signal is used as the clock in the NV-DDR data interface. This signal shares the same pin as WE_x_n in the SDR, NV-DDR2, and NV-DDR3 data interface. |
| WP_x_n | I | Write Protect The Write Protect signal disables Flash array program and erase operations. See section 2.19 for requirements. |
| IO0_0 – IO7_0 (DQ0_0 – DQ7_0) | I/O | I/O Port 0, bits 0-7 The I/O port is an 8-bit wide bidirectional port for transferring address, command, and data to and from the device. Also known as DQ0_0 – DQ7_0 for the NV-DDR, NV-DDR2, and NV-DDR3 data interfaces. |
| DQS (DQS_x_t) | I/O | Data Strobe (True) The data strobe signal that indicates the data valid window for the NV-DDR and NV-DDR2 data interfaces. |
| DQS_x_c | I/O | Data Strobe Complement The Data Strobe Complement signal is the complementary signal to Data Strobe True, optionally used in the NV-DDR2 or NV-DDR3 data interface. Specifically, Data Strobe Complement has the opposite value of Data Strobe True when CE_n is low, i.e. if DQS_x_t is high then DQS_x_c is low; if DQS_x_t is low then DQS_x_c is high. |
| IO8 – IO15 | I/O | I/O Port 0, bits 8-15 These signals are used in a 16-bit wide target configuration. The signals are the upper 8 bits for the 16-bit wide bidirectional port used to transfer data to and from the device. These signals are only used in the SDR data interface. |

adapted to send out a first data strobe signal [C]

and a write data signal [D]

ONFI Standard at 30.

adapted to send out a first data strobe signal [C]

and a write data signal [D]

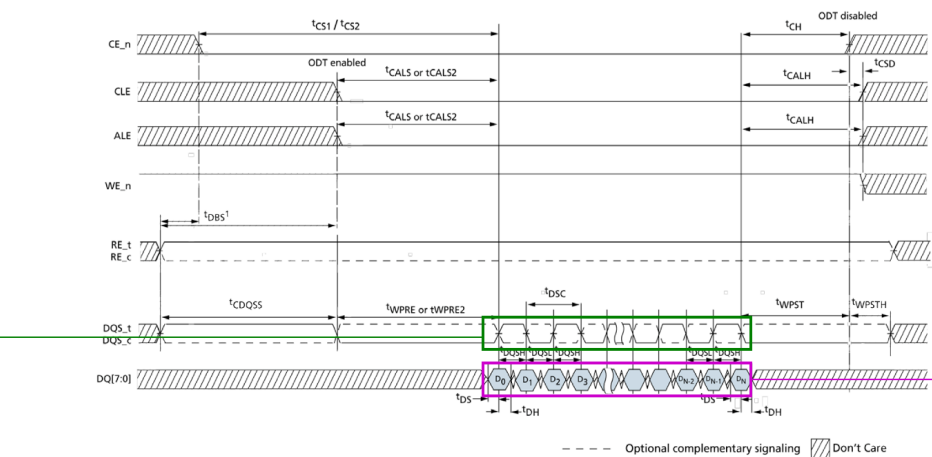


Figure 71 Data input cycle timing

in a write operation, the write data signal being synchronized with the first data strobe signal [E]

ONFI Standard at 165.

36. The Western Digital PC SN530 NVMe SSD further includes a controller being adapted in a read operation to send out a second data strobe signal and to receive a read data signal in synchronization with a read strobe signal.

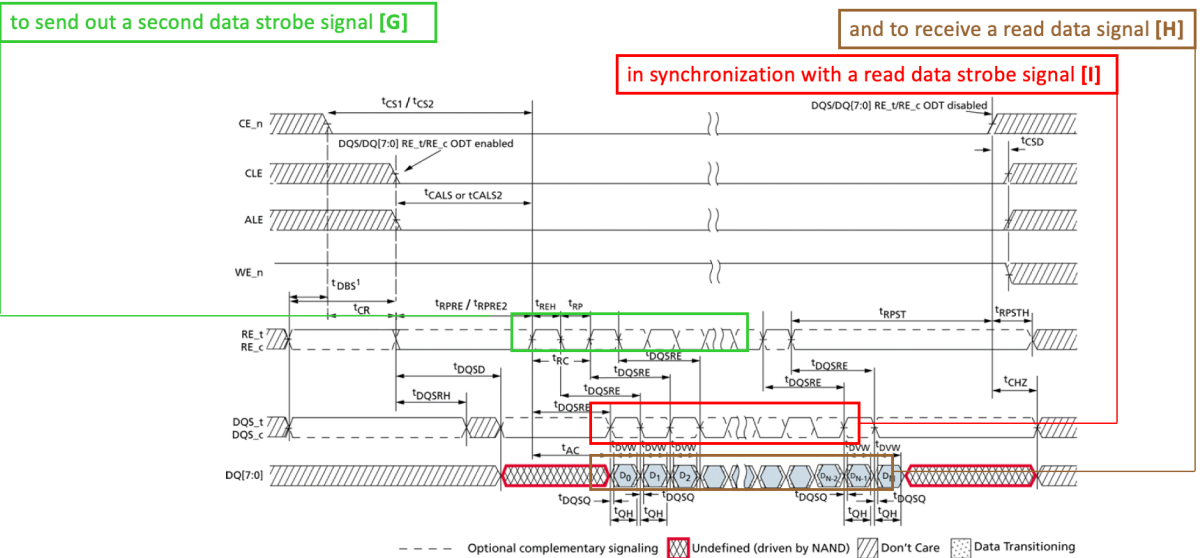


Figure 72 Data output cycle timing the controller being adapted, in a read operation [F]

ONFI Standard at 167.

37. The Western Digital PC SN530 NVMe SSD further includes the read strobe signal being received by the controller in response to the second data strobe signal:

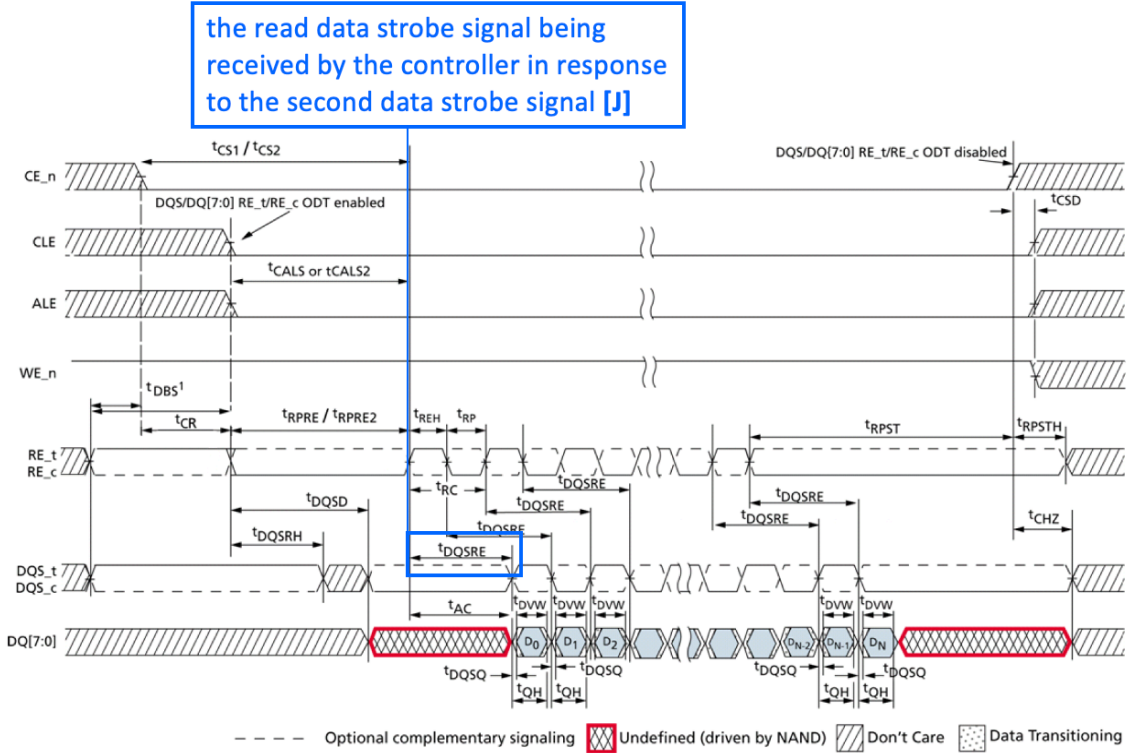


Figure 72 Data output cycle timing

ONFI Standard at 167.

38. The Western Digital PC SN530 NVMe SSD further includes a memory:

RUSS, AUGUST & KABAT

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28

a memory [K]
SanDisk 60362
512GB toggle
NAND Flash
memory



39. The Western Digital PC SN530 NVMe SSD further includes a memory adapted to receive the write data signal in synchronization with the first data strobe signal in the write operation:

adapted to receive the write data signal in synchronization with the first data strobe signal in the write operation [L]

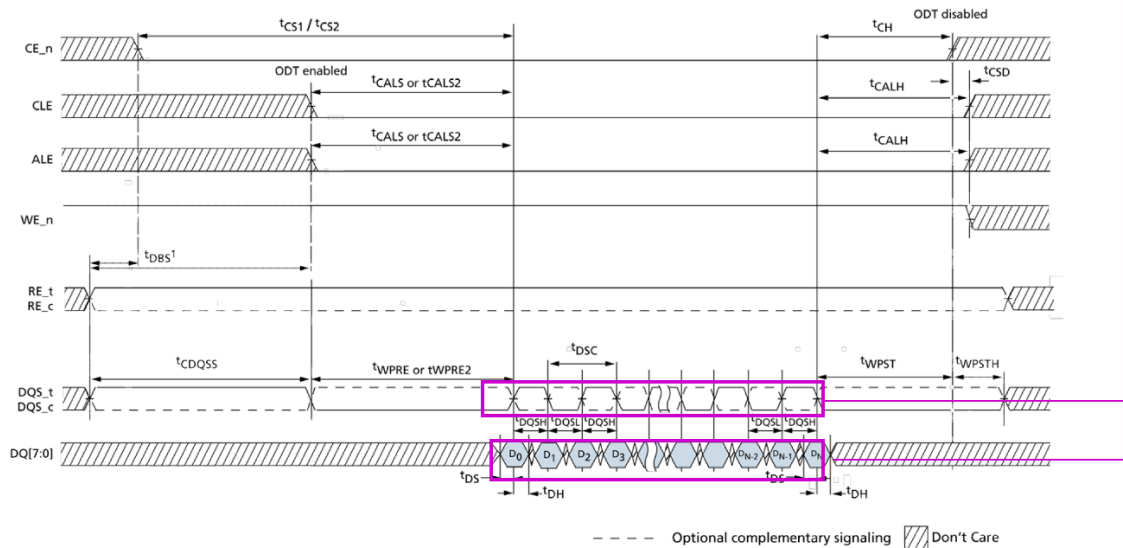


Figure 71 Data input cycle timing

RUSS, AUGUST & KABAT

1 40. The Western Digital PC SN530 NVMe SSD further includes a memory
2 adapted, in the read operation, to output the read data strobe signal in response to the
3 second data strobe signal and to send the read data signal synchronized with the read
4 data strobe signal:

5 in the read operation, to output the read data strobe signal in response to the second data
6 strobe signal and to send the read data signal synchronized with the read data strobe signal [M]

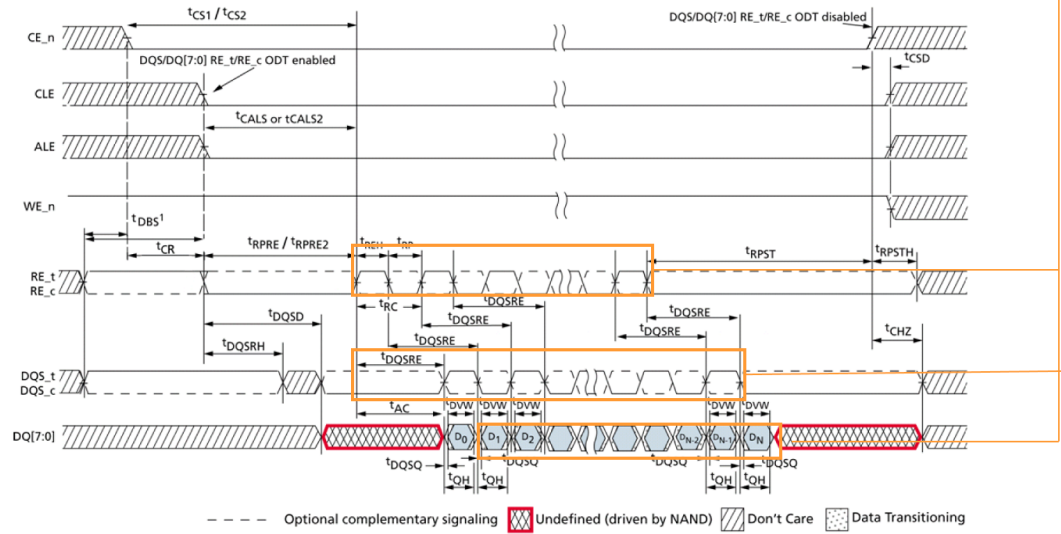


Figure 72 Data output cycle timing

17 41. Defendants actively, knowingly, and intentionally induce, and continue to
18 actively, knowingly, and intentionally induce, infringement of the '369 patent under
19 35 U.S.C. §271(b) by their customers and end users.

20 42. Defendants have had knowledge of and notice of the '369 patent and their
21 infringement since at least September 6, 2022 when Longitude gave Defendants
22 notice of their infringing actions. In any event, Defendants have had knowledge and
23 notice of the '369 patent since at least the filing of this complaint.

24 43. Defendants have induced their customers and end users to infringe the '369
25 patent by using their products as shown above. For example, Defendants encourage
26 their customers and end users to perform infringing methods by the very nature of
27 the products.
28

RUSS, AUGUST & KABAT

1 44. Defendants specifically intend their customers and/or end users infringe the
2 ‘369 patent, either literally or by the doctrine of equivalents, because Defendants
3 have known about the ‘369 patent and how Defendants' products infringe the claims
4 of the ‘369 patent but Defendants have not taken steps to prevent infringement by
5 their customers and/or end users. Accordingly, Defendants have acted with the
6 specific intent to induce infringement of the ‘369 patent.

7 45. Accordingly, Defendants have induced, and continue to induce, infringement
8 of the ‘369 patent under 35 U.S.C. §271(b).

9 46. As discussed above, Defendants have had knowledge of and notice of the ‘369
10 patent and its infringement since at least September 6, 2022. Despite this
11 knowledge, Defendants continue to commit tortious conduct by way of patent
12 infringement.

13 47. Defendants have been and continue to infringe one or more of the claims of
14 the ‘369 patent through the aforesaid acts.

15 48. Defendants have committed these acts of infringement without license or
16 authorization.

17 49. Plaintiff is entitled to recover damages adequate to compensate for the
18 infringement.

19 50. Defendants have and continue to infringe the ‘369 patent, acting with an
20 objectively high likelihood that their actions constitute infringement of the ‘369
21 patent. Defendants have known or should have known of this risk at least as early
22 as September 6, 2022. Accordingly, Defendants’ infringement of the ‘369 patent has
23 been and continues to be willful.

24 **COUNT II**

25 **(DEFENDANTS' INFRINGEMENT OF THE '539 PATENT)**

26 51. Paragraphs 1 through 50 are incorporated by reference as if fully restated
27 herein.

28

RUSS, AUGUST & KABAT

1 52. United States Patent No. RE43,539, entitled “Output Buffer Circuit and
2 Integrated Semiconductor Circuit Device With Such Output Buffer Circuit,” issued
3 on July 24, 2012 from United States Patent Application No. 11/798,773 filed on May
4 16, 2007. The ‘539 Patent is a re-issue of U.S. Patent No. 6,894,547, which issued
5 on May 17, 2005 from United States Patent Application No. 10/320,059 filed
6 December 16, 2002.

7 53. Longitude is the owner of the ‘539 patent with full rights to pursue recovery
8 of royalties for damages for infringement, including full rights to recover past and
9 future damages.

10 54. Each claim of the ‘539 patent is valid, enforceable, and patent-eligible.

11 55. Longitude and its predecessors in interest have satisfied the requirements of
12 35 U.S.C. § 287(a) with respect to the ‘539 patent, and Longitude is entitled to
13 damages for Defendants’ past infringement. Among other things, Longitude
14 provided actual notice of infringement to the component supplier, Western Digital.

15 56. Defendants have directly infringed (literally and equivalently) and induced
16 others to infringe the ‘539 patent by making, using, selling, offering for sale, or
17 importing products that infringe the claims of the ‘539 patent and by inducing others
18 to infringe the claims of the ‘539 patent without a license or permission from
19 Longitude. These products include without limitation all Acer Aspire 5 computers
20 (e.g. model A515-56-74PH), Nitro 5 computers (e.g. model AN515055055M1) and
21 all other Acer computers, laptops, and tablets having Western Digital PC SN530
22 NVMe SSDs, Western Digital SSDs, and/or Western Digital NAND memory chips
23 and all versions and variations of them offered for sale since the issuance of the ‘369
24 patent.

25 57. A non-limiting example of Defendants’ infringement is the Acer Aspire 5
26 computer which infringes at least claim 1 of the ‘539 patent. Exemplary photographs
27 of the Acer Aspire 5, and its packaging are set forth below:
28

RUSS, AUGUST & KABAT

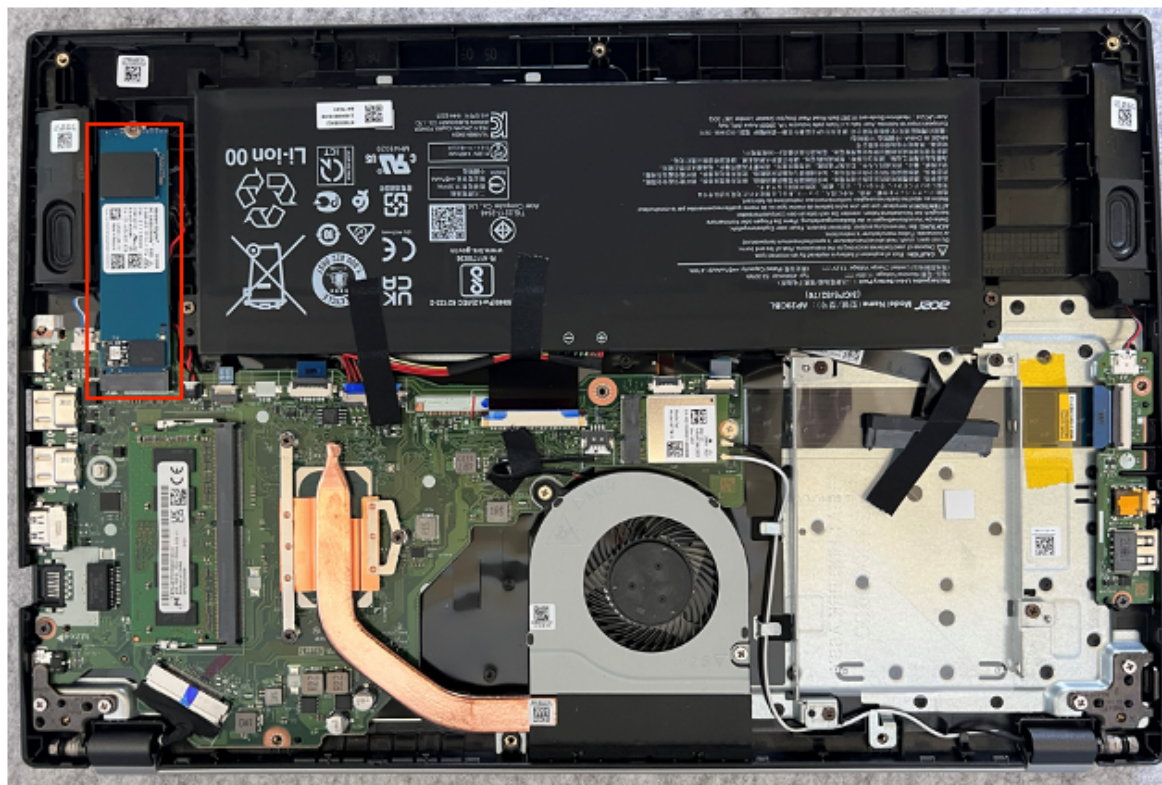
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28



58. The Acer Aspire 5 includes the Western Digital PC SN530 NVMe SSD as shown below:

RUSS, AUGUST & KABAT

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28



Acer Aspire

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28

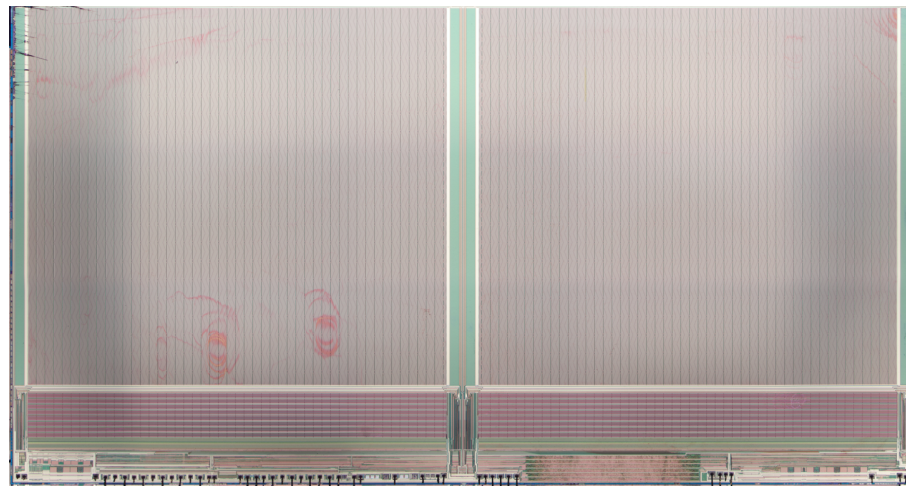
RUSS, AUGUST & KABAT



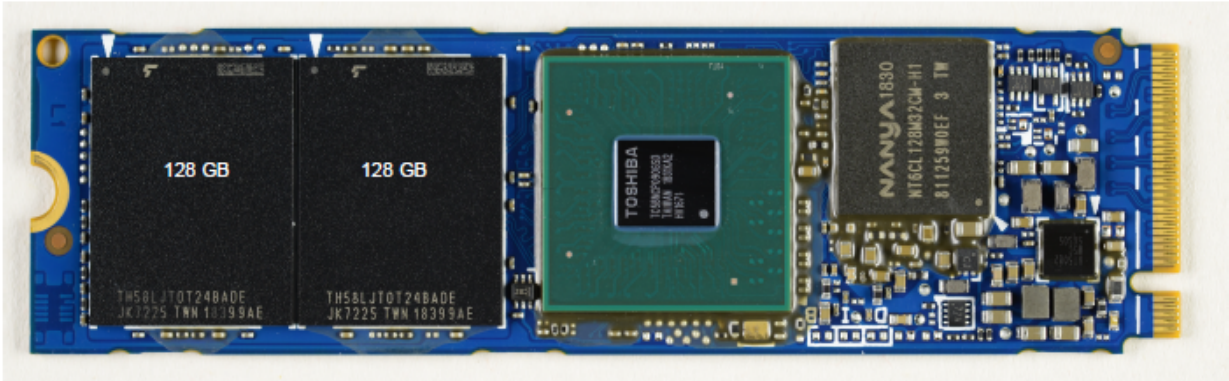
59. The below image shows the pin layout and corners of the SanDisk memory chip used in the Western Digital PC SN530 NVMe SSD:

RUSS, AUGUST & KABAT

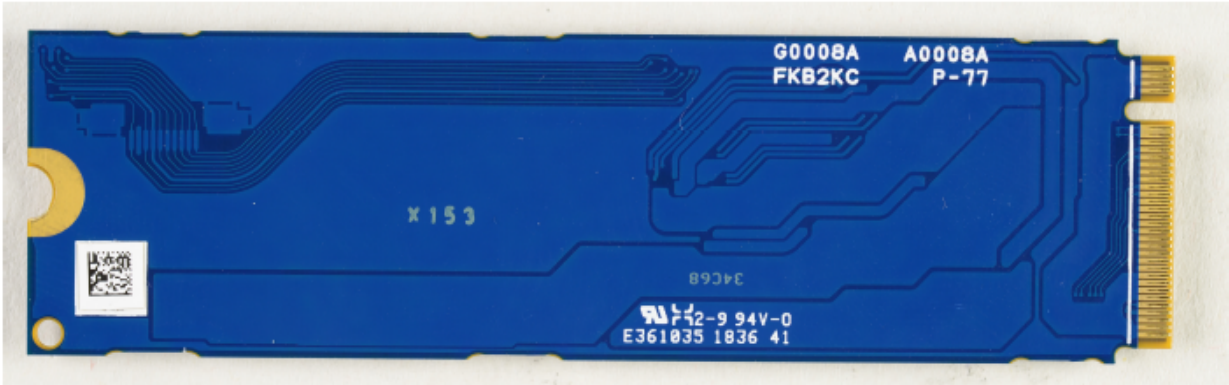
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28



60. On information and belief, the Western Digital PC SN530 NVMe SSD used in the Acer Aspire 5 computer is substantially similar to the Toshiba KXG60ZNV256G SSD Package (“Toshiba SSD”) for all matters relevant to this complaint. The Toshiba SSD is depicted below:



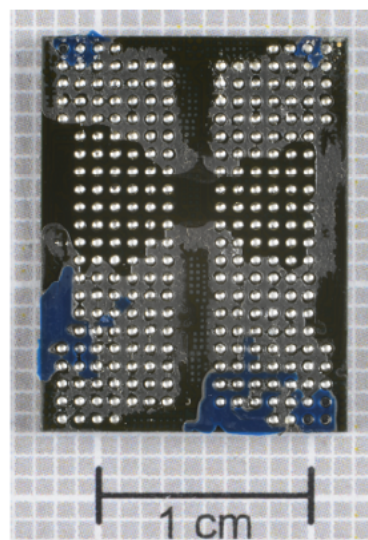
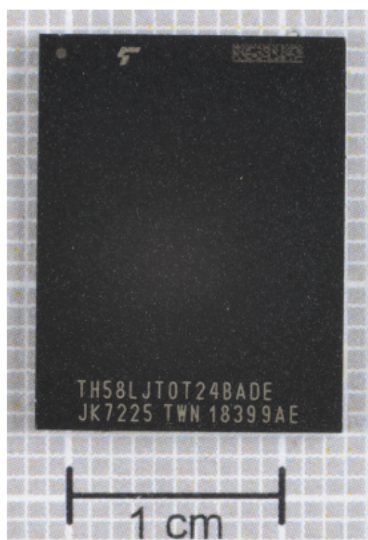
Toshiba KXG60ZNV256G SSD Package – Top



Toshiba KXG60ZNV256G SSD Package – Bottom

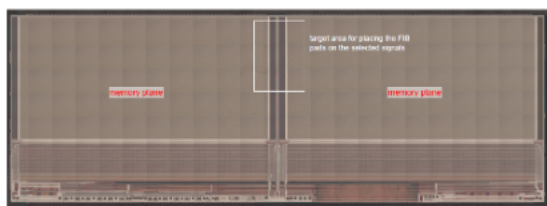
61. The memory chip of the Toshiba SSD, the Toshiba TH58LJT0T24BADE Package is depicted in the images below:

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28

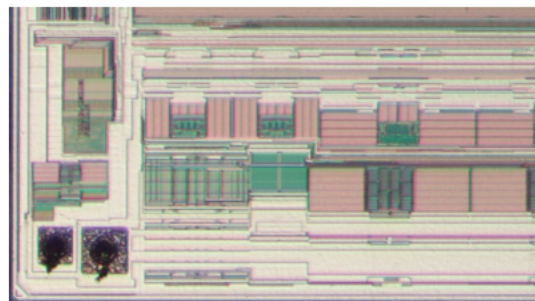
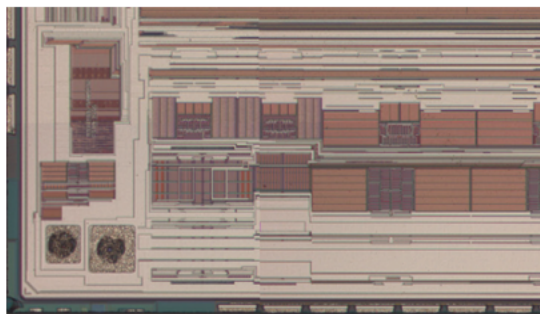
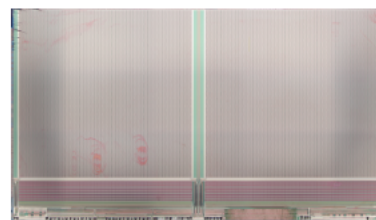


Toshiba 256 Gb 96L 3D NAND Flash Memory Die Photograph

62. A side-by-side comparison of the SanDisk memory chip used in the Western Digital PC SN530 NVMe SSD and the Toshiba TH58LJT0T24BADE Package used in the Toshiba SSD is depicted below:



Toshiba 256 Gb 96L 3D NAND Flash Memory Die Photograph

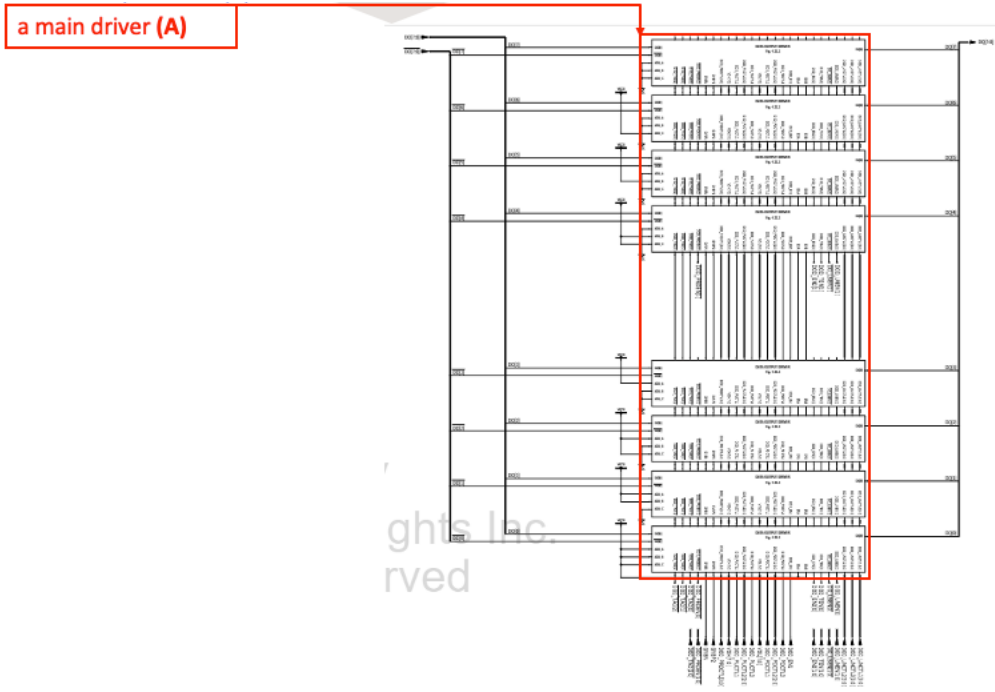


11 63. Based at least on the above, Longitude is informed and believes, that
 12 the corners of the dies of the SanDisk memory chip used in the Western Digital PC
 13 SN530 NVMe SSD and the Toshiba TH58LJT0T24BADE Package are substantially
 14 the same. Among other things, the corners are substantially the same. Accordingly,
 15 Longitude is informed and believes that the various I/Os and peripheral circuits are
 16 the same between the Toshiba and Western Digital/SanDisk chips. Furthermore,
 17 Longitude is informed and believes that Toshiba and Western Digital shared the
 18 designs for 96 layer chips. Accordingly, the SanDisk memory chip is substantially
 19 the same as the Western Digital PC SN530 NVMe SSD and the Toshiba
 20 TH58LJT0T24BADE Package. For this reason, Longitude is informed and believes
 21 that technical documents and other analysis concerning the Toshiba
 22 TH58LJT0T24BADE Package also describe the layout and functionality of the
 23 Western Digital PC SN530 NVMe SSD.

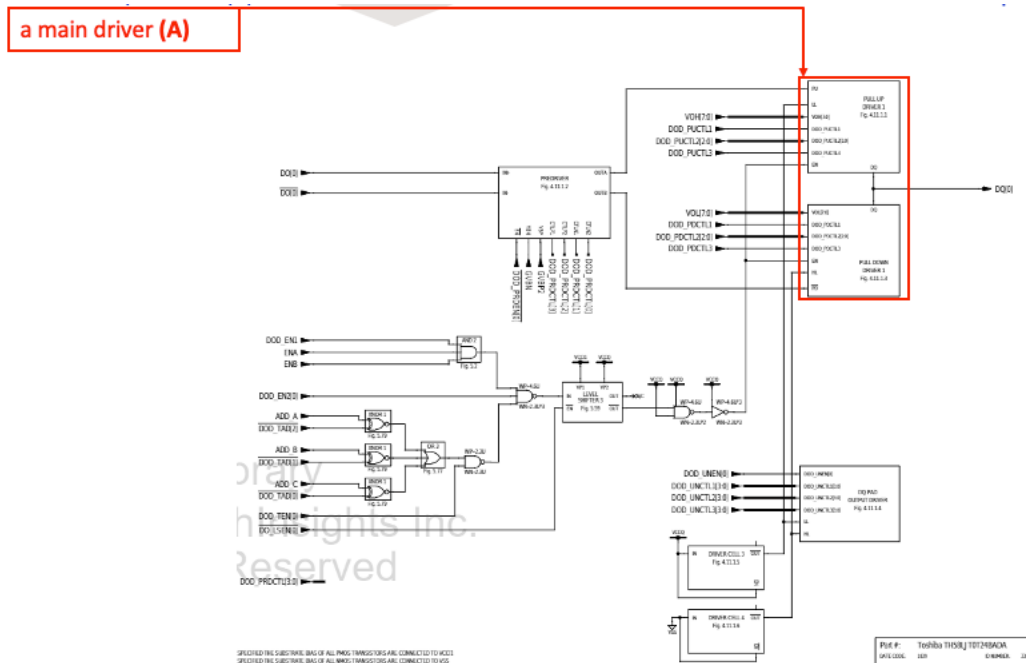
24 64. The Western Digital PC SN530 NVMe SSD used in the Acer Aspire 5
 25 computer includes an output buffer circuit for outputting data in the form of an input
 26 pulse train at a predetermined output impedance and slew rate comprising a main
 27 driver:
 28

RUSS, AUGUST & KABAT

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28



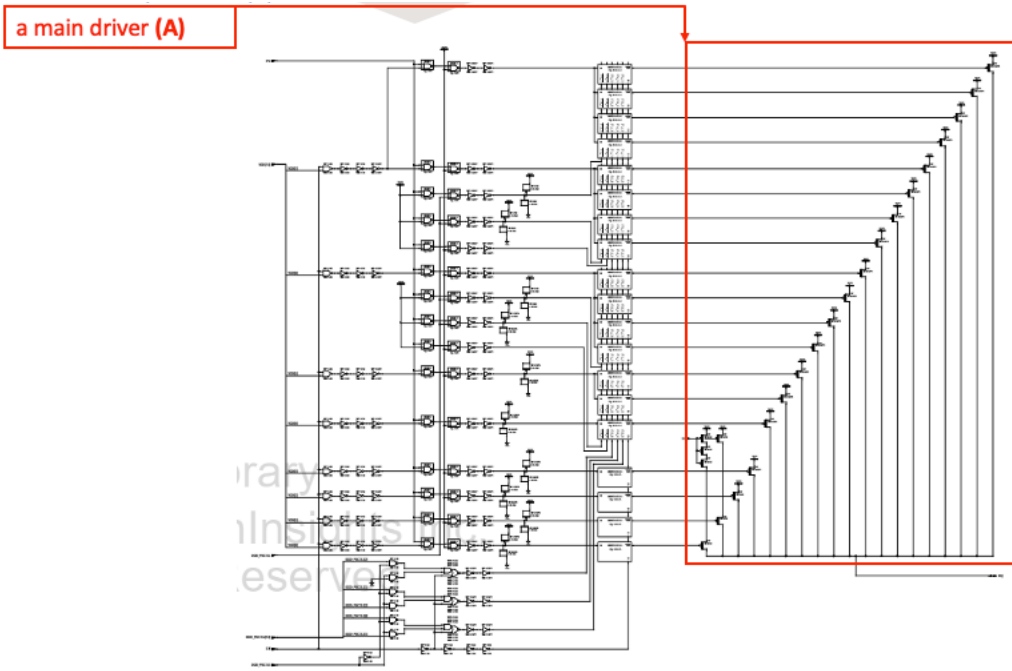
Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11 DATA OUTPUT DRIVERS



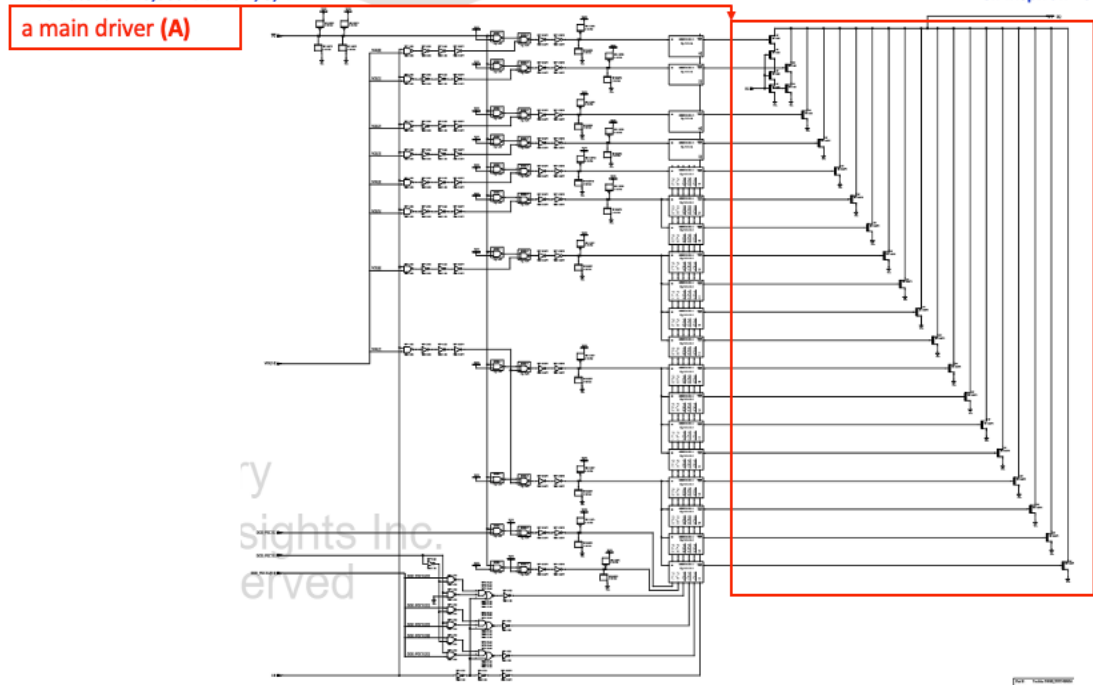
Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1 DATA OUTPUT DRIVER

RUSS, AUGUST & KABAT

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28



Source: TechInsights Report ID#: CAR-1902-801 Figure 41111 PULL UP DRIVER1

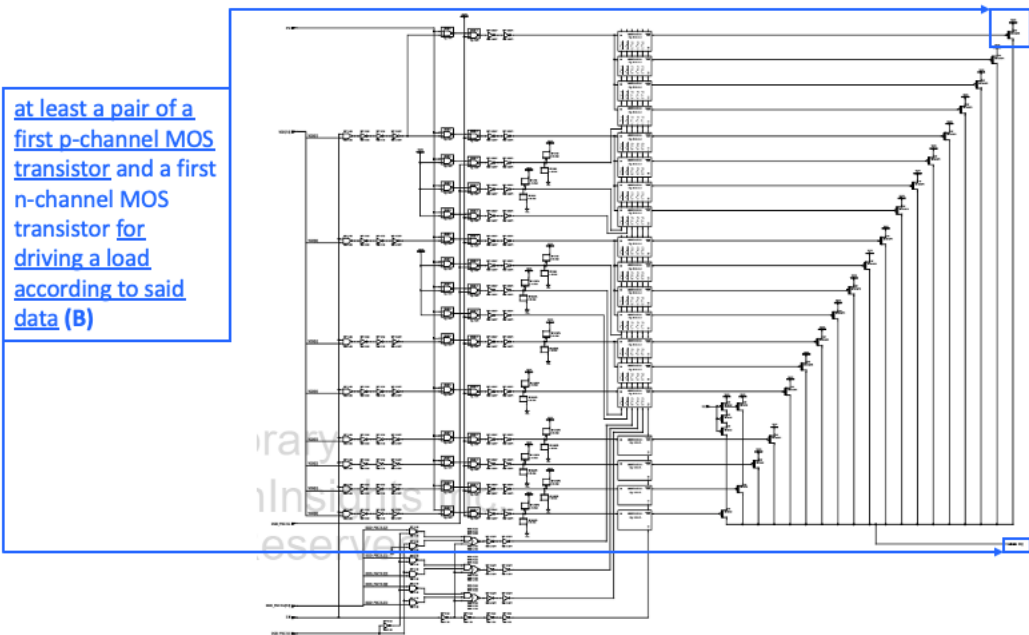


Source: TechInsights Report ID#: CAR-1902-801 Figure 41113 PULL DOWN DRIVER1

65. The Western Digital PC SN530 NVMe SSD used in the Acer Aspire 5 computer further includes at least a pair of a first p-channel MOS transistor and a first n-channel MOS transistor for driving a load according to said data:

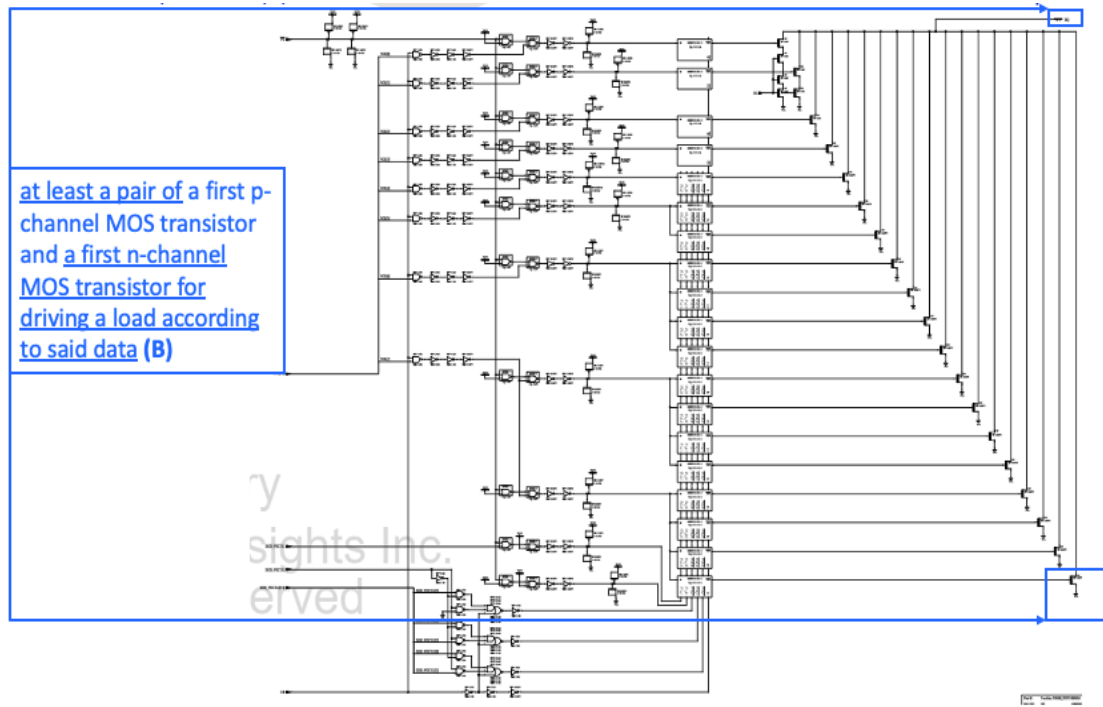
RUSS, AUGUST & KABAT

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28



at least a pair of a first p-channel MOS transistor and a first n-channel MOS transistor for driving a load according to said data (B)

Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.11 PULL UP DRIVER1



at least a pair of a first p-channel MOS transistor and a first n-channel MOS transistor for driving a load according to said data (B)

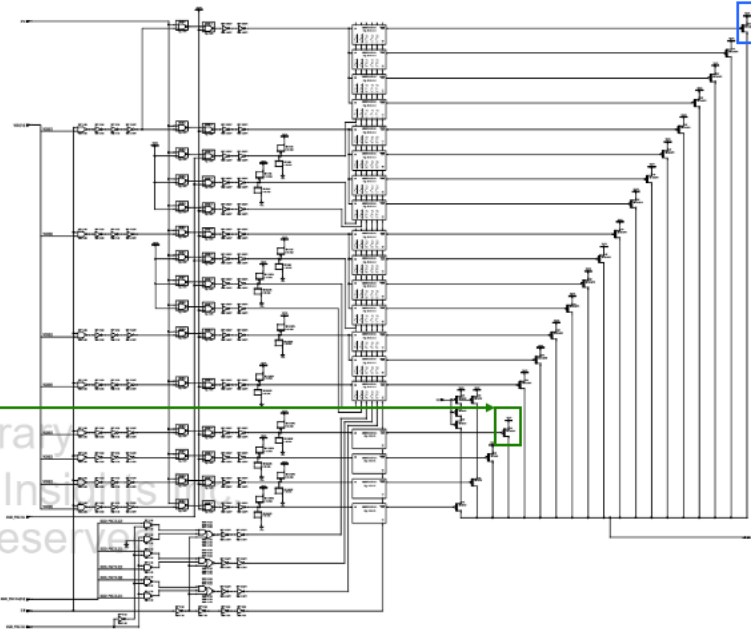
Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.13 PULL DOWN DRIVER1

66. The Western Digital PC SN530 NVMe SSD used in the Acer Aspire 5 computer further includes at least a pair of a second p-channel MOS transistor and a second n-channel MOS transistor for driving said load in coaction with said first p-channel MOS transistor and said first n-channel MOS transistor:

RUSS, AUGUST & KABAT

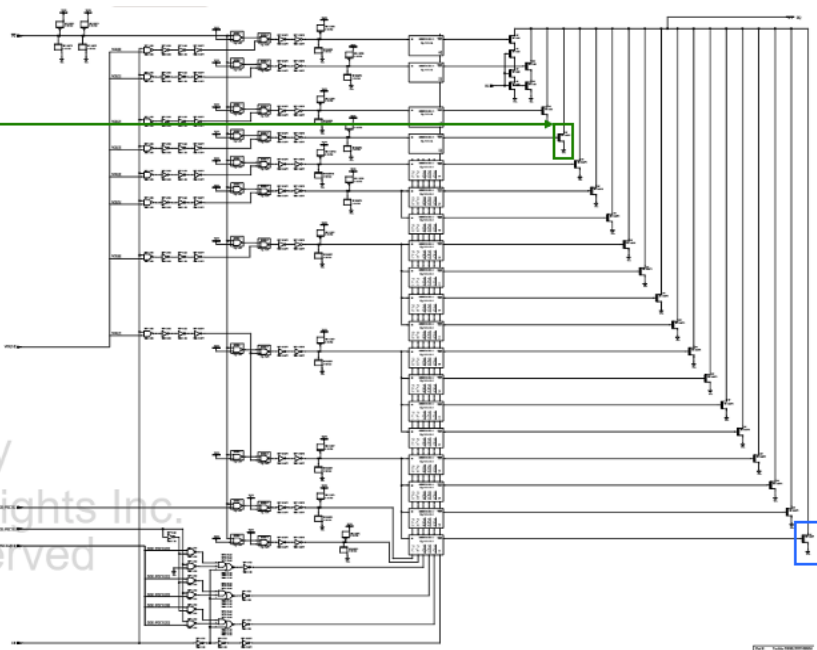
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28

at least a pair of a second p-channel MOS transistor and a second n-channel MOS transistor for driving said load in coaction with said first p-channel MOS transistor and said first n-channel MOS transistor (C)



Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.11 PULL UP DRIVER 1

at least a pair of a second p-channel MOS transistor and a second n-channel MOS transistor for driving said load in coaction with said first p-channel MOS transistor and said first n-channel MOS transistor (C)



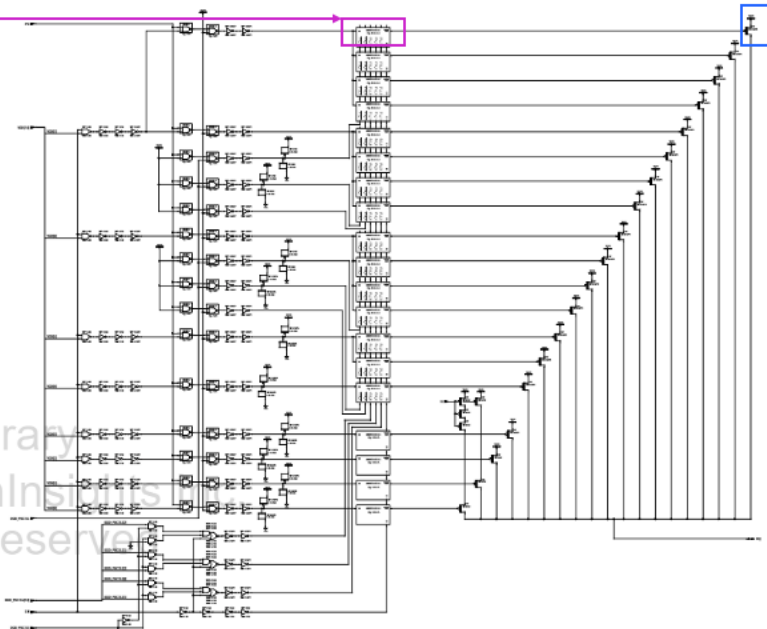
Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.13 PULL DOWN DRIVER 1

67. The Western Digital PC SN530 NVMe SSD used in the Acer Aspire 5 computer includes a predriver with outputs for driving only said first n-channel MOS transistor and only said first p-channel MOS transistor:

RUSS, AUGUST & KABAT

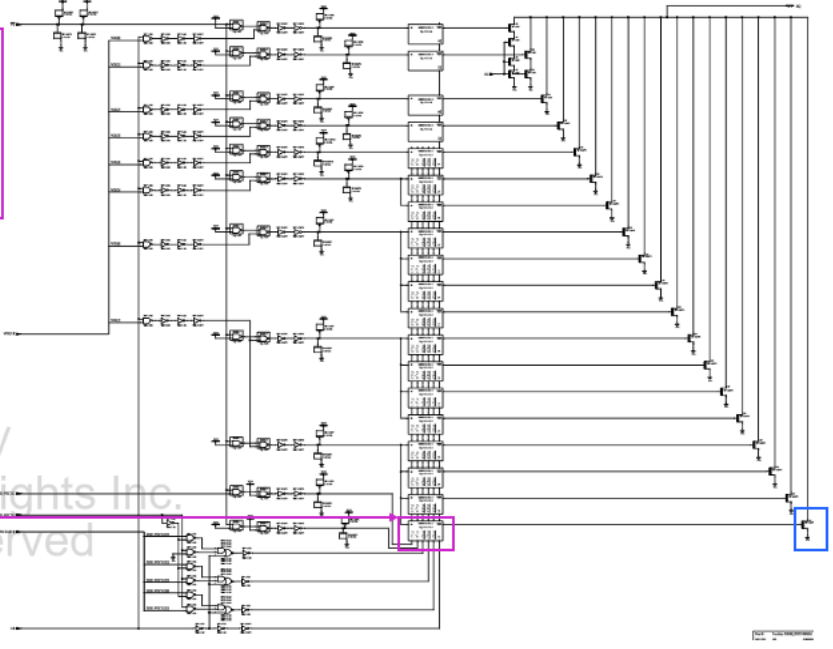
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28

a predriver with outputs for driving only said first n-channel MOS transistor and only said first p-channel MOS transistor (D)



Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.1 PULL UP DRIVER 1

a predriver with outputs for driving only said first n-channel MOS transistor and only said first p-channel MOS transistor (D)



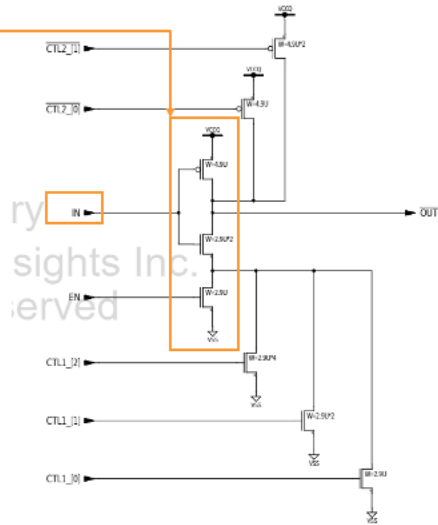
Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.3 PULL DOWN DRIVER 1

68. The Western Digital PC SN530 NVMe SSD used in the Acer Aspire 5 computer further comprises at least a pair of a third p-channel MOS transistor and a third n-channel MOS transistor for driving said first p-channel MOS transistor according to said data:

RUSS, AUGUST & KABAT

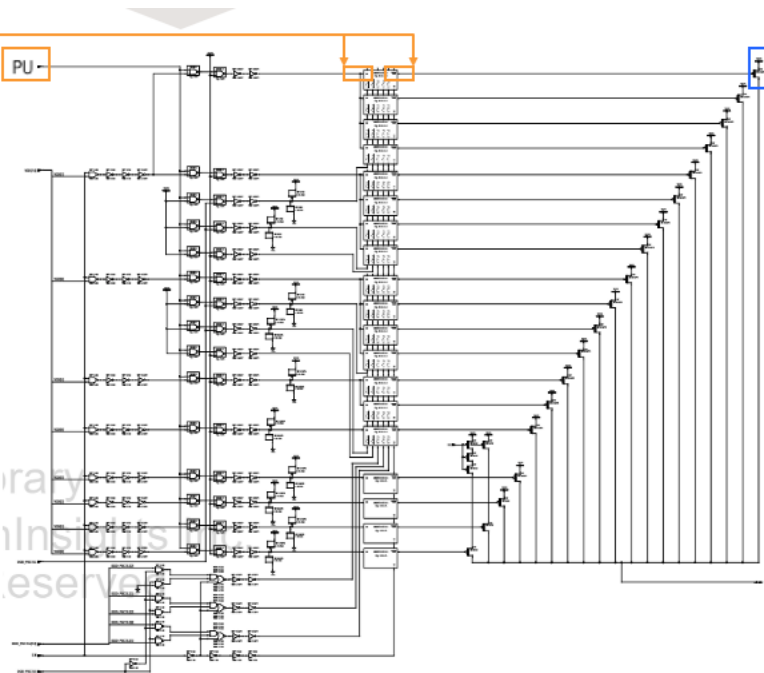
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28

at least a pair of a third p-channel MOS transistor and a third n-channel MOS transistor for driving said first p-channel MOS transistor according to said data (E)



Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.1 DRIVER CELL 1

at least a pair of a third p-channel MOS transistor and a third n-channel MOS transistor for driving said first p-channel MOS transistor according to said data (E)

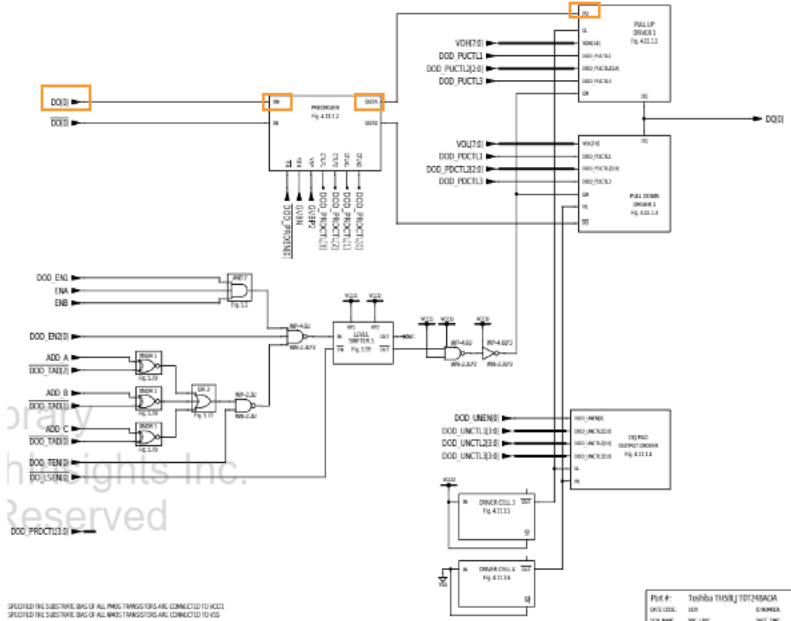


Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.1 PULLUP DRIVER 1

RUSS, AUGUST & KABAT

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28

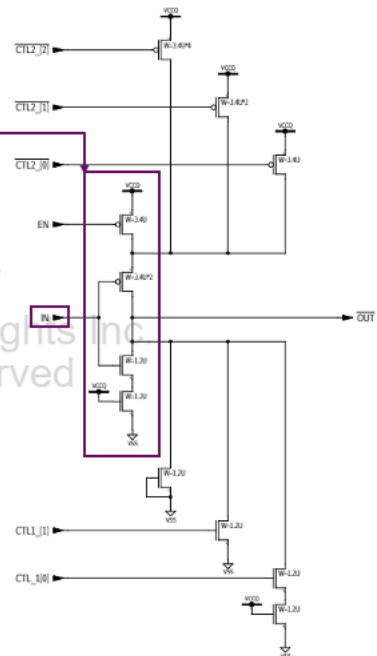
at least a pair of a third p-channel MOS transistor and a third n-channel MOS transistor for driving said first p-channel MOS transistor according to said data (E)



Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.1 PULL UP DRIVER 1

69. The Western Digital PC SN530 NVMe SSD used in the Acer Aspire 5 computer further includes at least a pair of fourth p-channel MOS transistor and a fourth n-channel MOS transistor for driving said first n-channel MOS transistor according to said data:

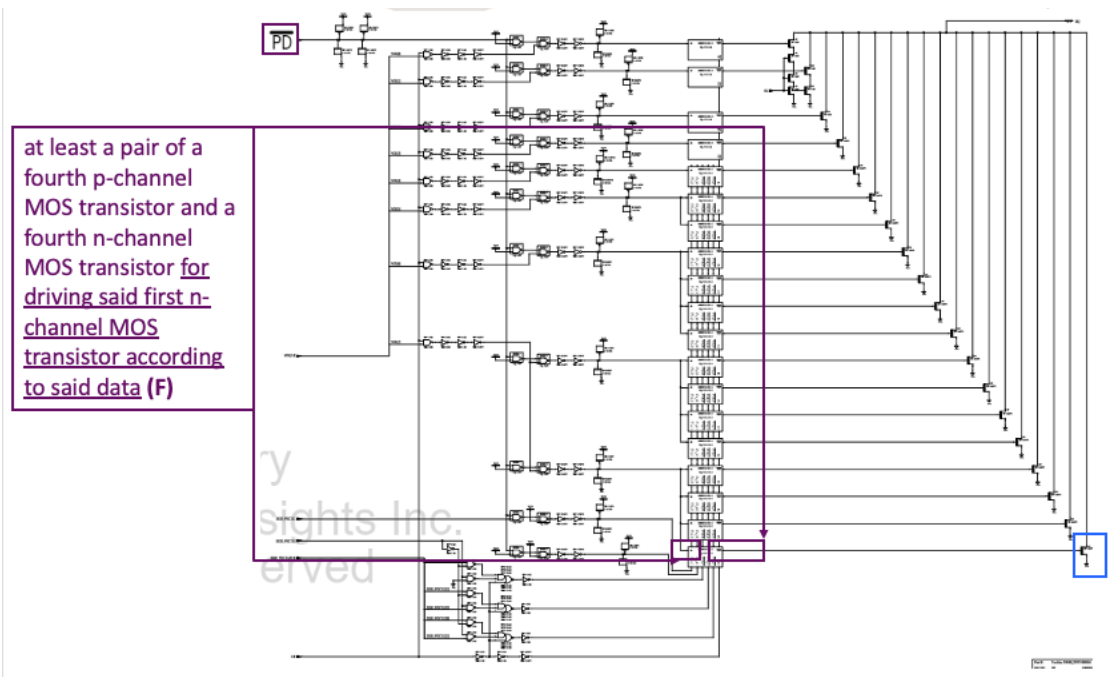
at least a pair of a fourth p-channel MOS transistor and a fourth n-channel MOS transistor for driving said first n-channel MOS transistor according to said data (F)



Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.3.1 DRIVER CELL 2

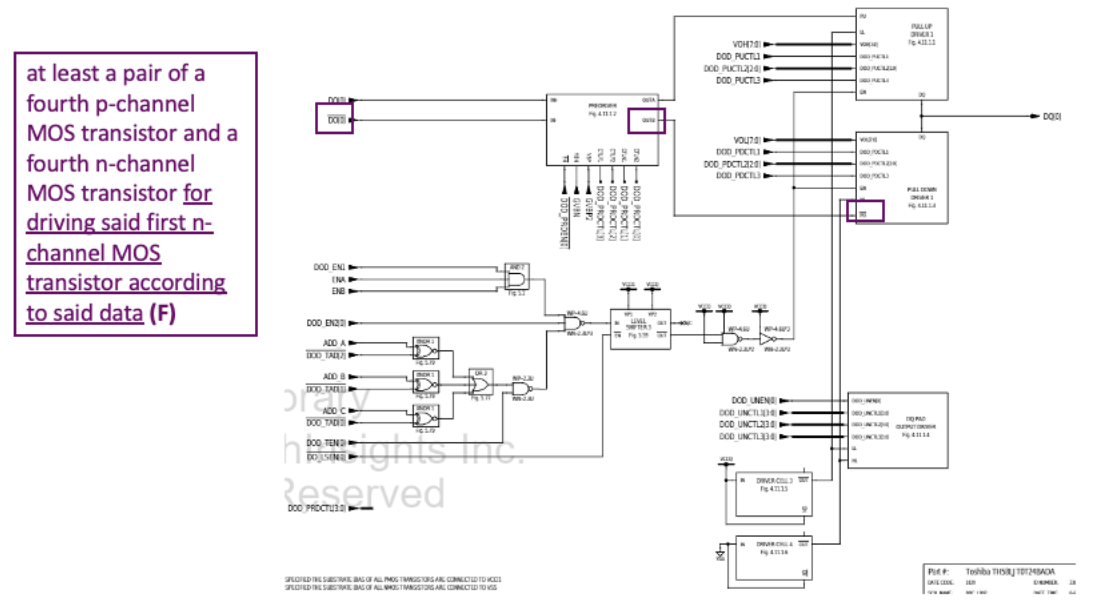
RUSS, AUGUST & KABAT

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28



at least a pair of a fourth p-channel MOS transistor and a fourth n-channel MOS transistor for driving said first n-channel MOS transistor according to said data (F)

Source: TechInsights Report ID#: CAR-1902-801 Figure 4.111.3 PULL DOWN DRIVER 1



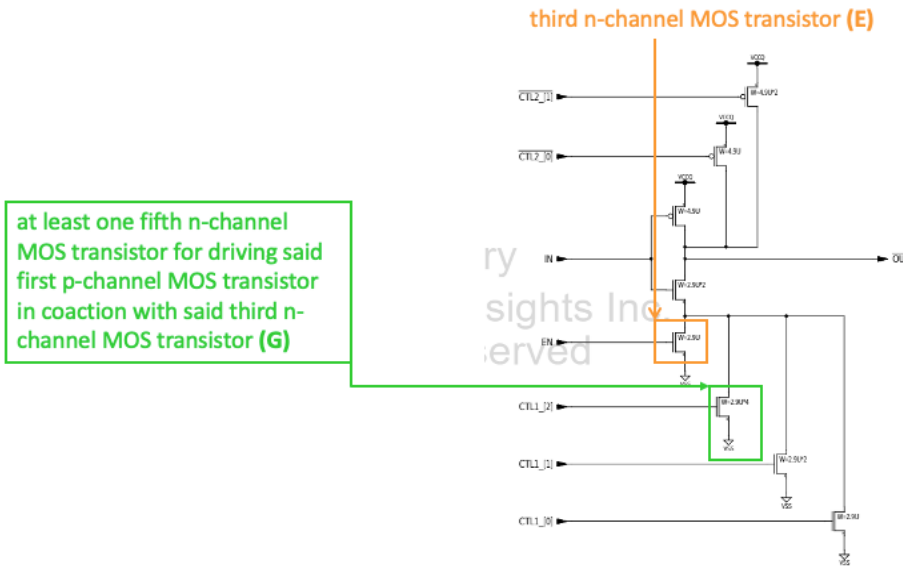
at least a pair of a fourth p-channel MOS transistor and a fourth n-channel MOS transistor for driving said first n-channel MOS transistor according to said data (F)

Source: TechInsights Report ID#: CAR-1902-801 Figure 4.111.1 PULL UP DRIVER 1

70. The Western Digital PC SN530 NVMe SSD used in the Acer Aspire 5 computer further includes at least one fifth n-channel MOS transistor for driving said first p-channel MOS transistor in coaction with said third n-channel MOS transistor:

RUSS, AUGUST & KABAT

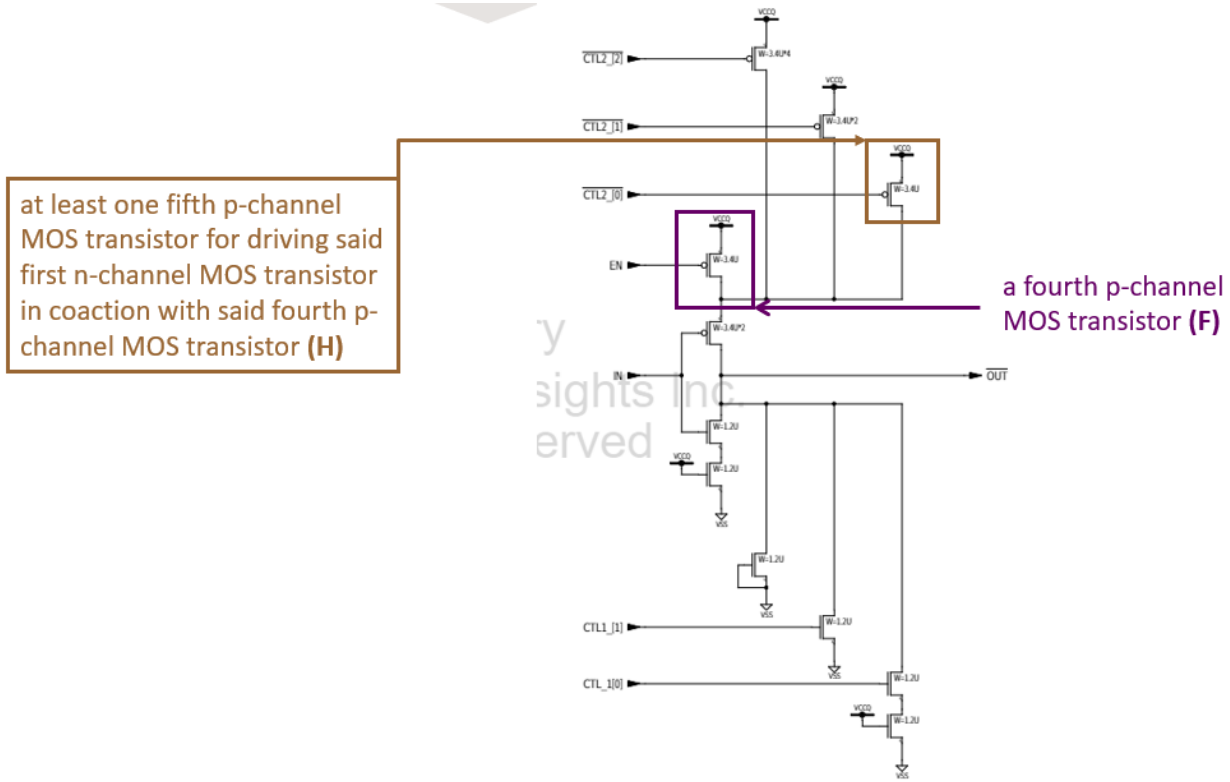
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28



at least one fifth n-channel MOS transistor for driving said first p-channel MOS transistor in coaction with said third n-channel MOS transistor (G)

Source: [TechInsights Report ID#: CAR-1902-801](#) Figure 4.11.1.1 DRIVER CELL 1

71. The Western Digital PC SN530 NVMe SSD used in the Acer Aspire 5 computer further includes at least one fifth p-channel MOS transistor in coaction with said fourth p-channel MOS transistor:

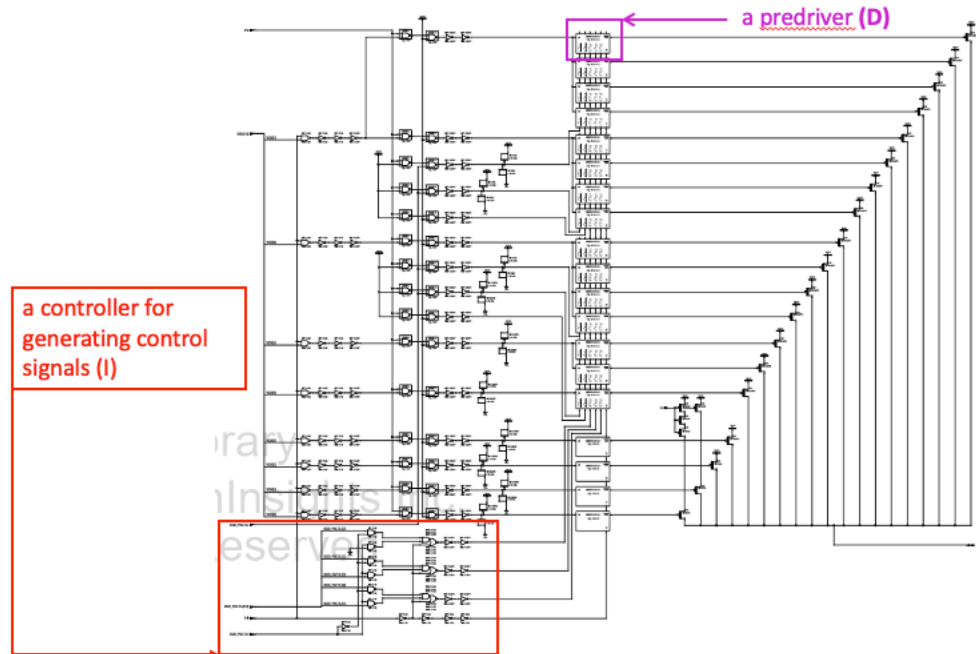


at least one fifth p-channel MOS transistor for driving said first n-channel MOS transistor in coaction with said fourth p-channel MOS transistor (H)

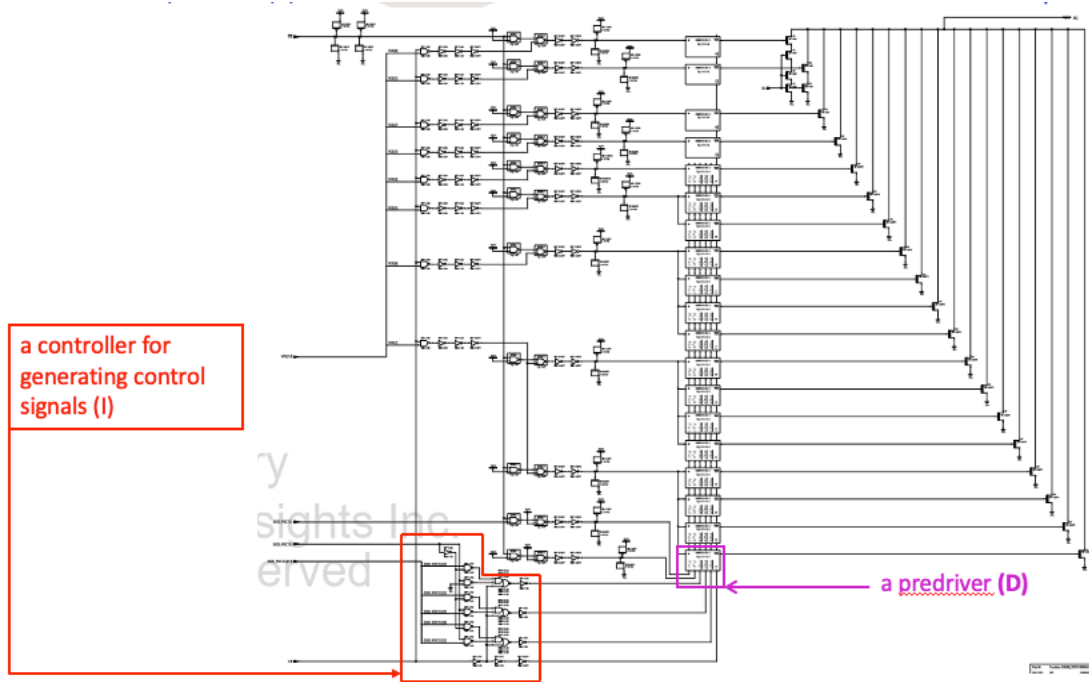
a fourth p-channel MOS transistor (F)

Source: [TechInsights Report ID#: CAR-1902-801](#) Figure 4.11.1.31 DRIVER CELL 2

72. The Western Digital PC SN530 NVMe SSD used in the Acer Aspire 5 computer further includes a controller for generating control signals:



Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.1 PULL UP DRIVER 1



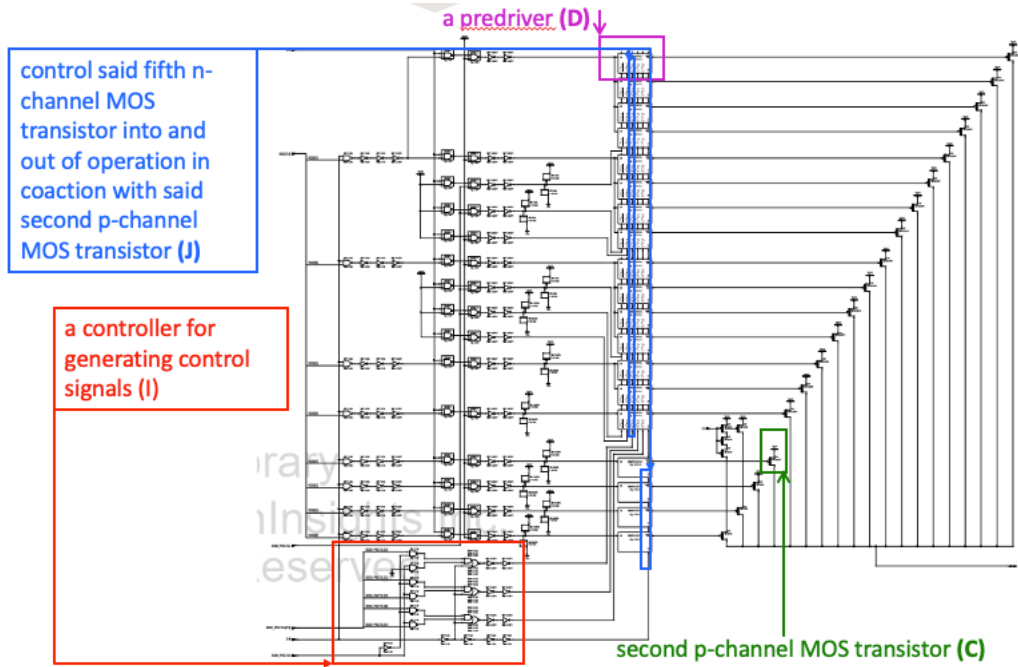
Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.1.3 PULL DOWN DRIVER 1

73. The Western Digital PC SN530 NVMe SSD used in the Acer Aspire 5 computer further includes a controller for generating control signals to control said

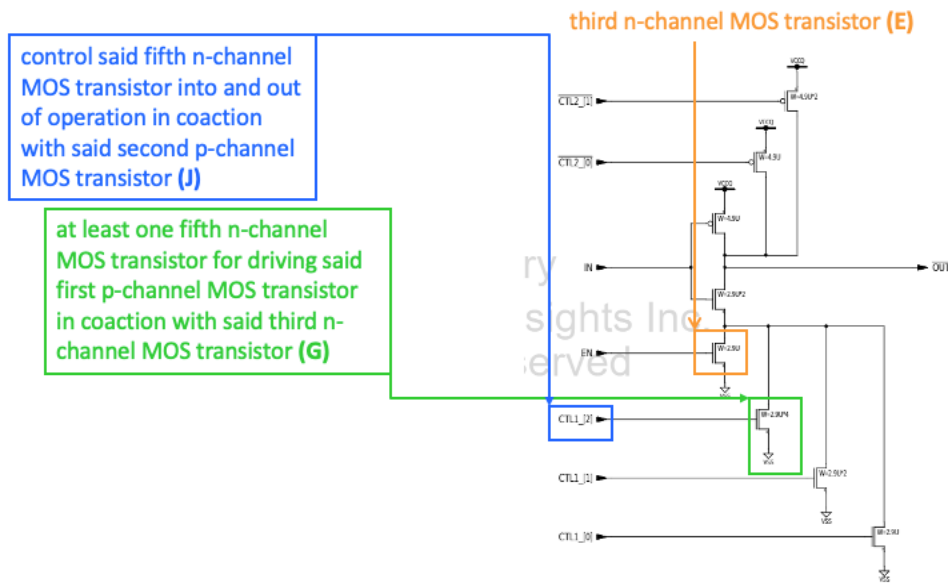
RUSS, AUGUST & KABAT

RUSS, AUGUST & KABAT

1 fifth n-channel MOS transistor into and out of operation in coaction with said second
 2 p-channel MOS transistor:



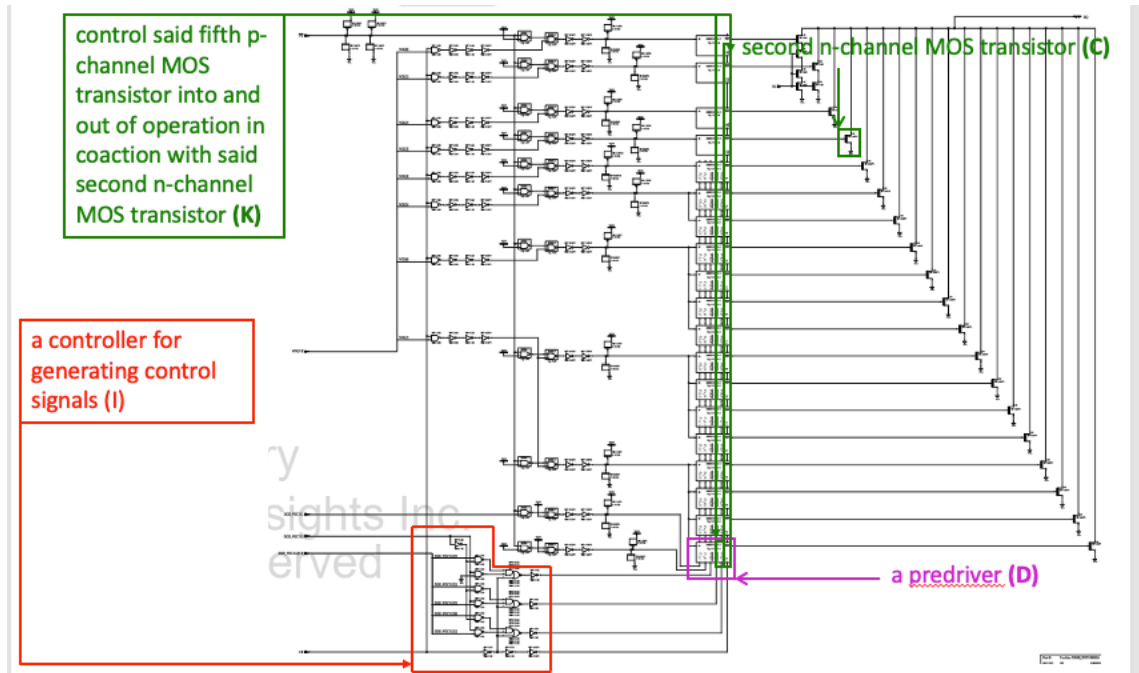
Source: TechInsights Report ID#: CAR-1902-801 Figure 411.1.1 PULL UP DRIVER



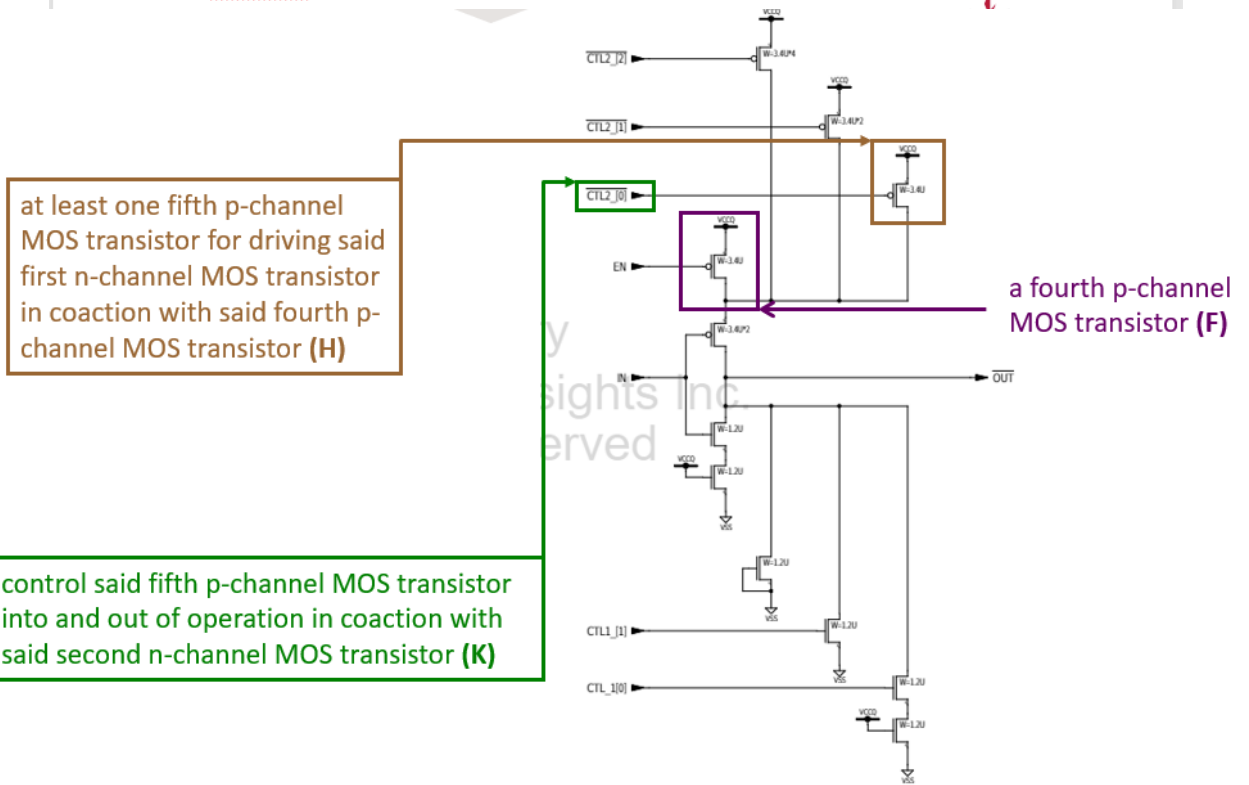
Source: TechInsights Report ID#: CAR-1902-801 Figure 411.1.1.1 DRIVER CELL 1

26 74. The Western Digital PC SN530 NVMe SSD used in the Acer Aspire 5
 27 computer further includes a controller for generating control signals to control said
 28

fifth p-channel MOS transistor into and out of operation in coaction with said second n-channel MOS-transistor:



Source: [TechInsights Report ID#: CAR-1902-801](#) Figure 4.11.1.3 PULL DOWN DRIVER 1

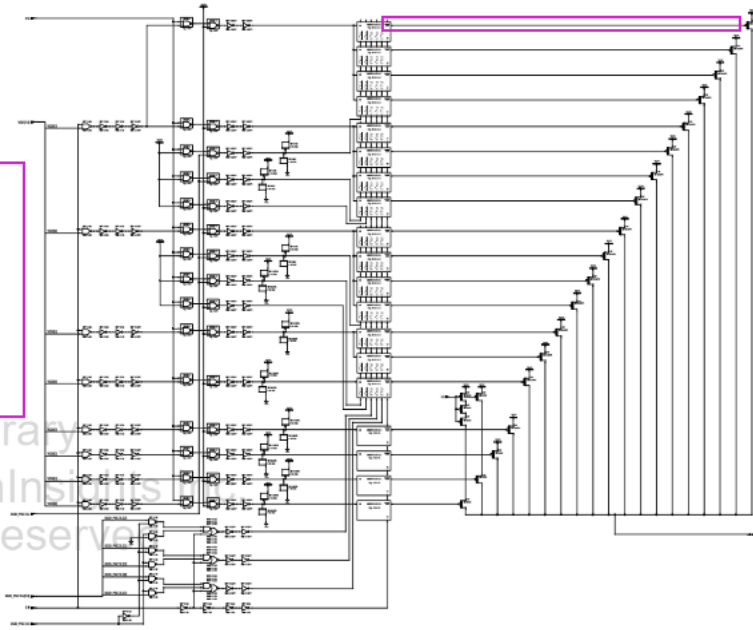


Source: [TechInsights Report ID#: CAR-1902-801](#) Figure 4.11.1.3.1 DRIVER CELL 2

RUSS, AUGUST & KABAT

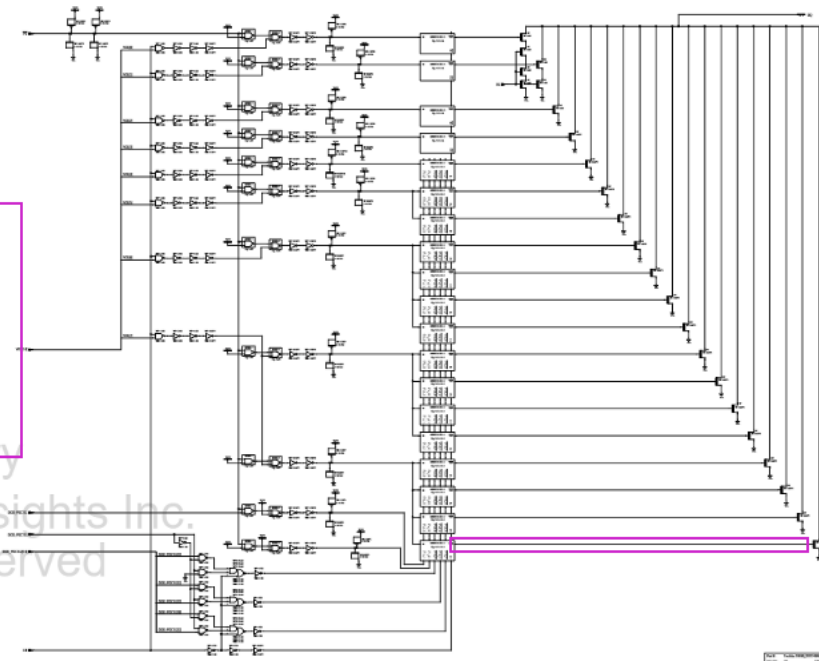
75. The Western Digital PC SN530 NVMe SSD used in Acer Aspire 5 computer further includes a controller wherein the output of the predriver is directly connected only to said first p-channel MOS transistor and said first n-channel MOS transistor of said main driver:

the output of the predriver is directly connected only to said first p-channel MOS transistor and said first n-channel MOS transistor of said main driver (L)



Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.11 PULL UP DRIVER 1

the output of the predriver is directly connected only to said first p-channel MOS transistor and said first n-channel MOS transistor of said main driver (L)



Source: TechInsights Report ID#: CAR-1902-801 Figure 4.11.13 PULL DOWN DRIVER 1

RUSS, AUGUST & KABAT

RUSS, AUGUST & KABAT

1 76. Defendants actively, knowingly, and intentionally induce, and continue
2 to actively, knowingly, and intentionally induce, infringement of the '539 patent
3 under 35 U.S.C. §271(b) by their customers and end users.

4 77. Defendants have had knowledge of and notice of the '539 patent and their
5 infringement since at least September 6, 2022 when Longitude gave Defendants
6 notice of their infringing actions. In any event, Defendants have had knowledge and
7 notice of the '539 patent since at least the filing of this complaint.

8 78. Defendants have induced their customers and end users to infringe the '539
9 patent by using their products as shown above. For example, Defendants encourage
10 their customers and end users to perform infringing methods by the very nature of
11 the products.

12 79. Defendants specifically intend their customers and/or end users infringe the
13 '539 patent, either literally or by the doctrine of equivalents, because Defendants
14 have known about the '539 patent and how Defendants' products infringe the claims
15 of the '539 patent but Defendants have not taken steps to prevent infringement by
16 their customers and/or end users. Accordingly, Defendants have acted with the
17 specific intent to induce infringement of the '369 patent.

18 80. Accordingly, Defendants have induced, and continue to induce, infringement
19 of the '539 patent under 35 U.S.C. §271(b).

20 81. As discussed above, Defendants have had knowledge of and notice of the '539
21 patent and its infringement since at least September 6, 2022. Despite this
22 knowledge, Defendants continue to commit tortious conduct by way of patent
23 infringement.

24 82. Defendants have been and continue to infringe one or more of the claims of
25 the '539 patent through the aforesaid acts.

26 83. Defendants have committed these acts of infringement without license or
27 authorization.
28

1 84.Plaintiff is entitled to recover damages adequate to compensate for the
2 infringement.

3 85.Defendants have and continue to infringe the '539 patent, acting with an
4 objectively high likelihood that their actions constitute infringement of the '539
5 patent. Defendants have known or should have known of this risk at least as early
6 as September 6, 2022. Accordingly, Defendants' infringement of the '539 patent has
7 been and continues to be willful.

8 **COUNT III**

9 **(DEFENDANTS' INFRINGEMENT OF THE '233 PATENT)**

10 86.Paragraphs 1 through 85 are incorporated by reference as if fully restated
11 herein.

12 87.United States Patent No. 9,379,233, entitled "Semiconductor Device," issued
13 on June 28, 2016 from United States Patent Application No. 14/872,844 filed
14 October 1, 2015.

15 88.Longitude is the owner of the '233 patent with full rights to pursue recovery
16 of royalties for damages for infringement, including full rights to recover past and
17 future damages.

18 89.Each claim of the '233 patent is valid, enforceable, and patent-eligible.

19 90.Longitude and its predecessors in interest have satisfied the requirements of
20 35 U.S.C. § 287(a) with respect to the '233 patent, and Longitude is entitled to
21 damages for Defendants' past infringement. Among other things, Longitude
22 provided actual notice of infringement to the component supplier, Western Digital.

23 91.Defendants have directly infringed (literally and equivalently) and induced
24 others to infringe the '233 patent by making, using, selling, offering for sale, or
25 importing products that infringe the claims of the '233 patent and by inducing others
26 to infringe the claims of the '233 patent without a license or permission from
27 Longitude. These products include without limitation all Acer Aspire 5 computers
28 (e.g. model A515-56-74PH), Nitro 5 computers (e.g. model AN515055055M1) and

1 all other Acer computers, laptops, and tablets having Western Digital PC SN530
 2 NVMe SSDs, Western Digital SSDs, and/or Western Digital 3D NAND memory
 3 chips and all versions and variations of them offered for sale since the issuance of
 4 the '369 patent.

5 92. A non-limiting example of Defendants' infringement is the SanDisk memory
 6 chip contained within the Acer Aspire 5 computer which infringes at least claim 1
 7 of the '369 patent. Exemplary photographs of the Acer Aspire 5, and its packaging
 8 are set forth below:

RUSS, AUGUST & KABAT



1 93. The Acer Aspire 5 includes the Western Digital PC SN530 NVMe SSD as
2 shown below:
3
4



RUSS, AUGUST & KABAT

28



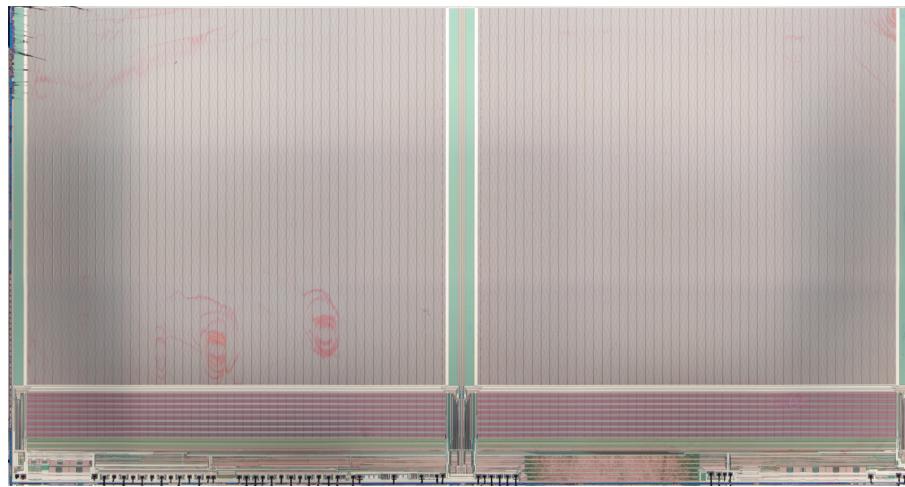
RUSS, AUGUST & KABAT

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28

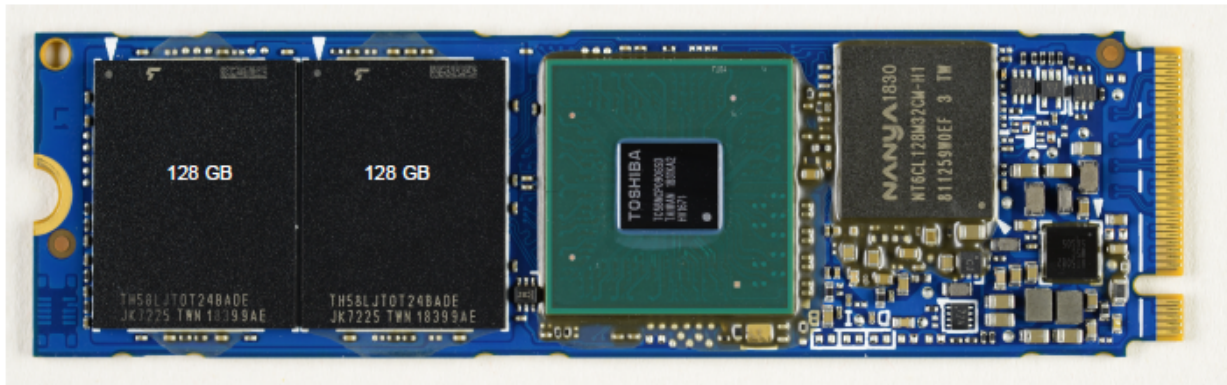
94. The below image shows the pin layout and corners of the SanDisk memory chip used in the Western Digital PC SN530 NVMe SSD:

RUSS, AUGUST & KABAT

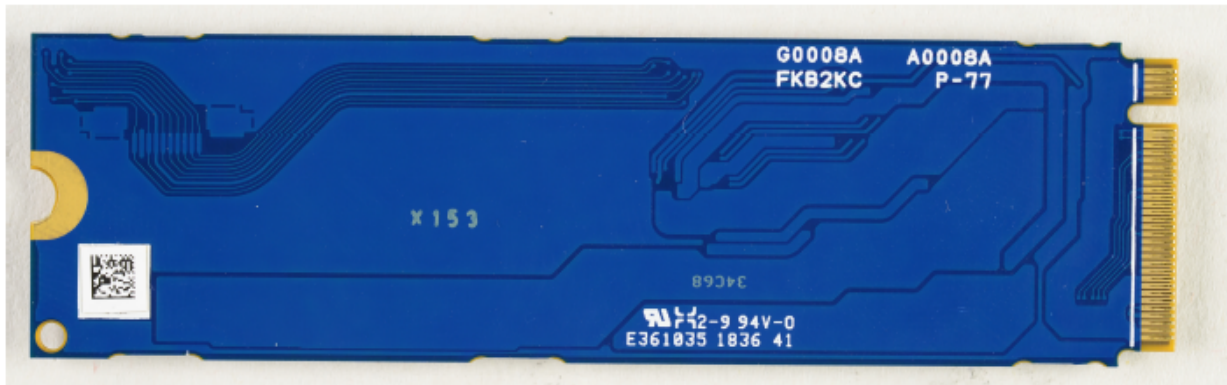
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28



95. On information and belief, the Western Digital PC SN530 NVMe SSD used in the Acer Aspire 5 is substantially similar to the Toshiba KXG60ZNV256G SSD Package (“Toshiba SSD”) for all matters relevant to this complaint. The Toshiba SSD is depicted below:



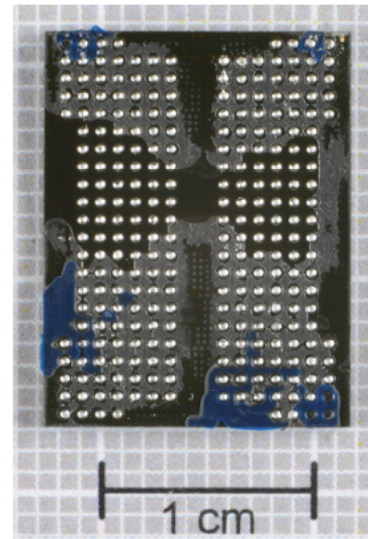
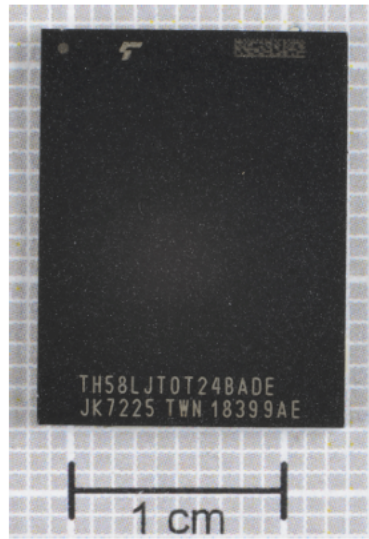
Toshiba KXG60ZNV256G SSD Package – Top



Toshiba KXG60ZNV256G SSD Package – Bottom

96. The memory chip of the Toshiba SSD, the Toshiba TH58LJT0T24BADE Package, is depicted in the images below:

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28

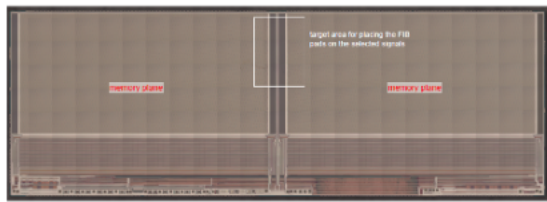


Toshiba 256 Gb 96L 3D NAND Flash Memory Die Photograph

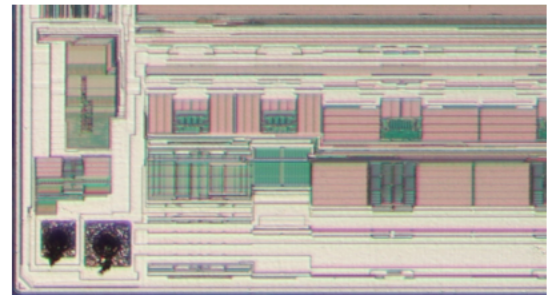
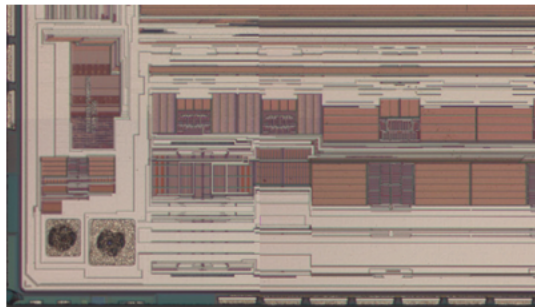
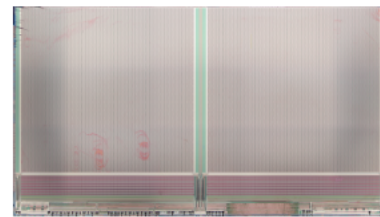
97. A side-by-side comparison of the SanDisk memory chip used in the Western Digital PC SN530 NVMe SSD and the Toshiba TH58LJT0T24BADE Package used in the Toshiba SSD is depicted below:

RUSS, AUGUST & KABAT

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28



Toshiba 256 Gb 96L 3D NAND Flash Memory Die Photograph

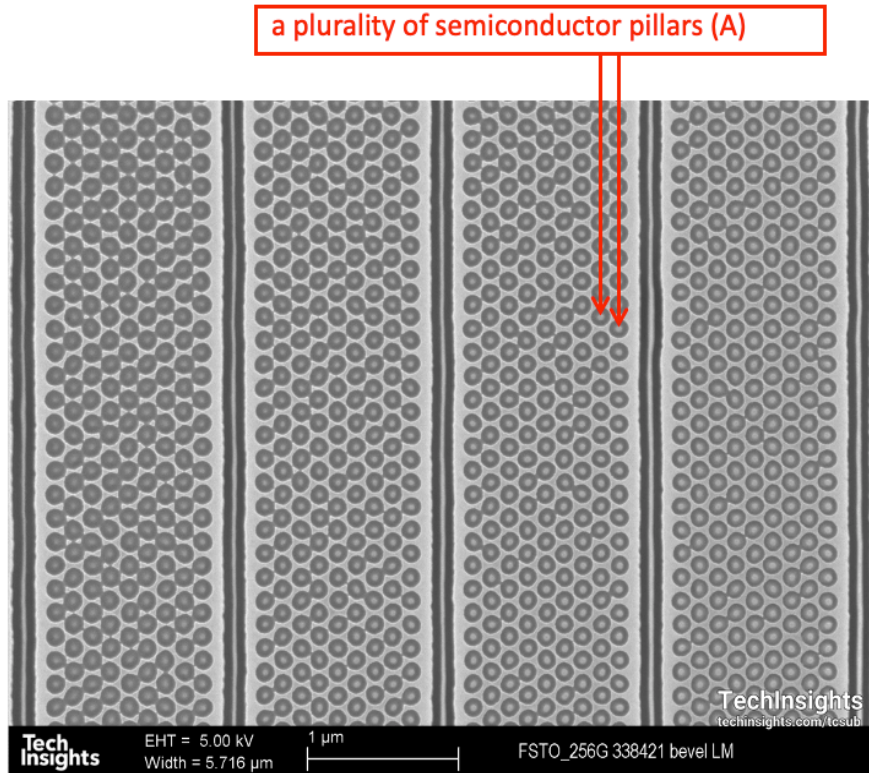
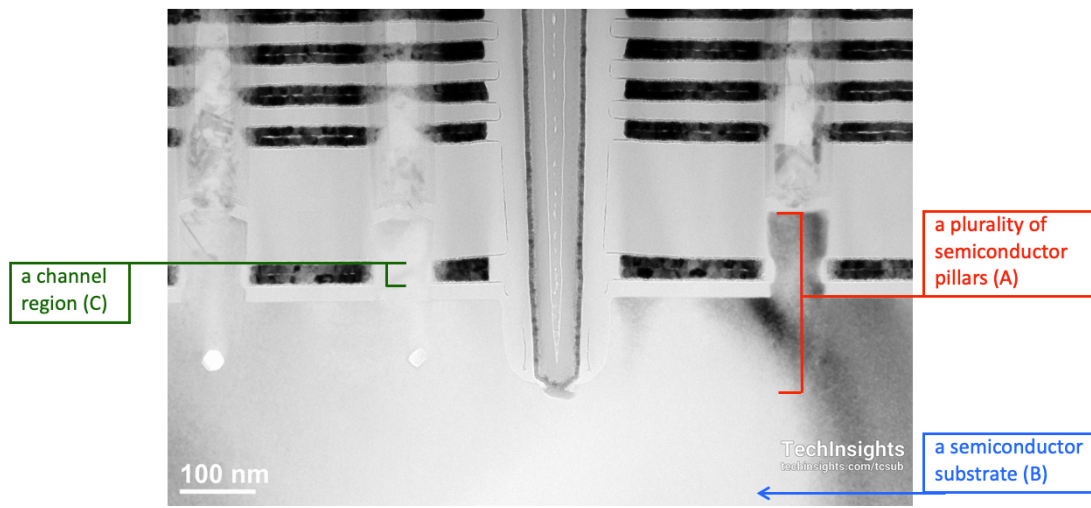


98. Based at least on the above, Longitude is informed and believes that the corners of the dies of the SanDisk memory chip used in the Western Digital PC SN530 NVMe SSD and the Toshiba TH58LJT0T24BADE Package are substantially the same. Accordingly, Longitude is informed and believes that the various I/Os and peripheral circuits are the same between the Toshiba and Western Digital/SanDisk chips. Furthermore, Longitude is informed and believes that Toshiba and Western Digital shared the designs for 96 layer chips. As shown above, the SanDisk memory chip is substantially the same as the Western Digital PC SN530 NVMe SSD and the Toshiba TH58LJT0T24BADE Package. For this reason, Longitude is informed and believes that technical documents and other analysis concerning the Toshiba TH58LJT0T24BADE Package also describe the layout and functionality of the Western Digital PC SN530 NVMe SSD and the SanDisk memory chip therein.

99. The SanDisk memory chip used in the Western Digital PC SN530 NVMe SSD is a semiconductor device comprising a plurality of semiconductor pillars provided to stand from a semiconductor substrate, each of the semiconductor pillars comprising a channel region:

RUSS, AUGUST & KABAT

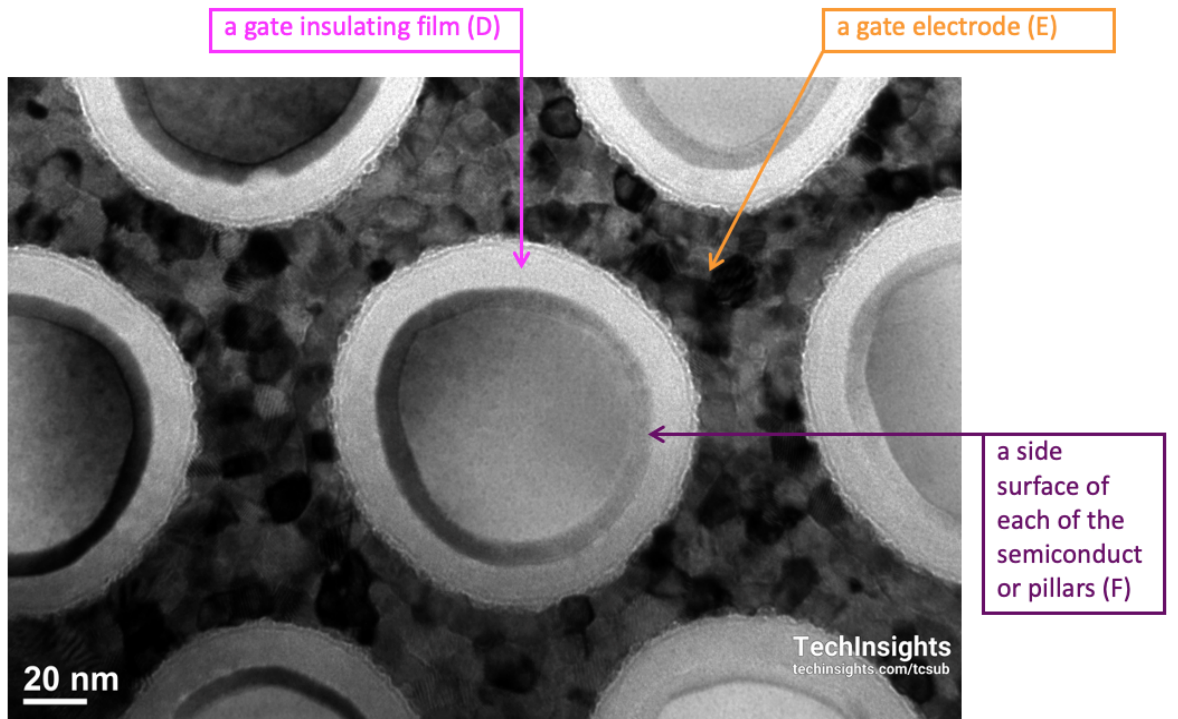
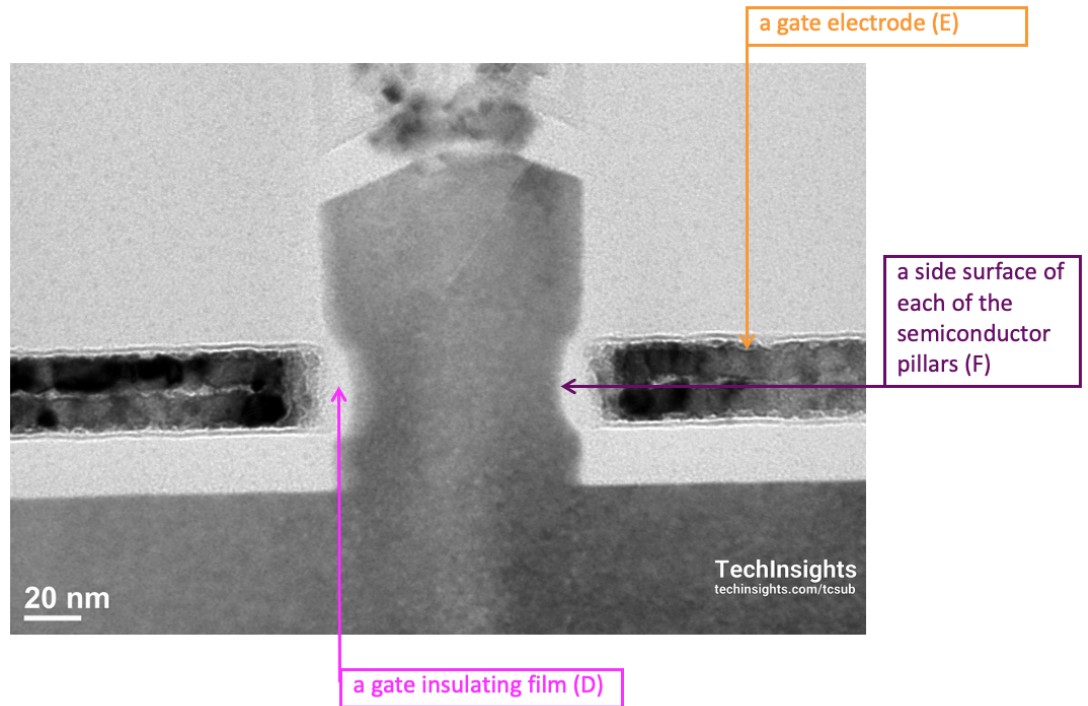
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28



100. The SanDisk memory chip used in the Western Digital PC SN530 NVMe SSD is a semiconductor device comprising a gate insulating film and a gate electrode provided over a side surface of each of the semiconductor pillars:

RUSS, AUGUST & KABAT

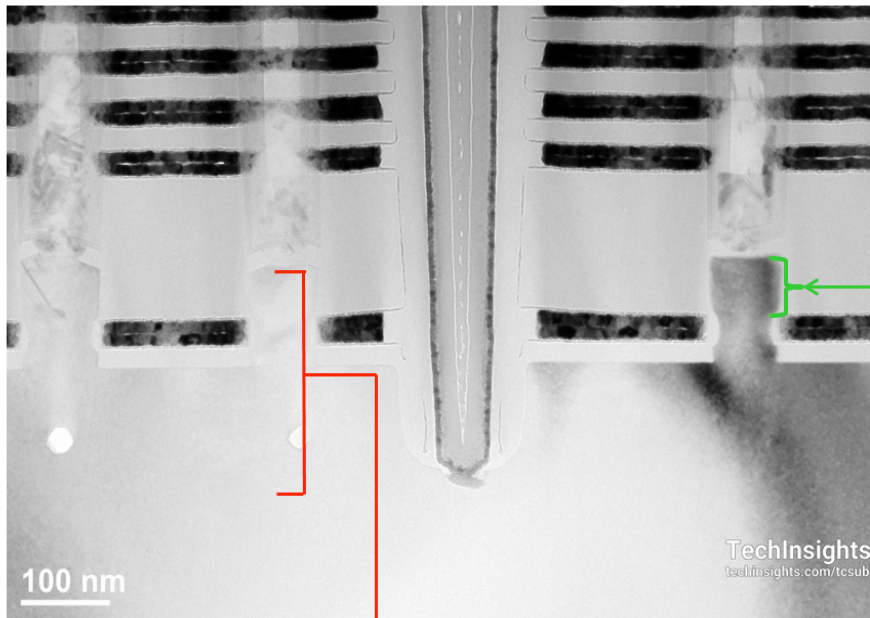
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28



101. The SanDisk memory chip used in the Western Digital PC SN530 NVMe SSD is a semiconductor device comprising an upper diffusion layer provided at an upper end of each of the semiconductor pillars to serve as one of a source and a drain:

RUSS, AUGUST & KABAT

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28



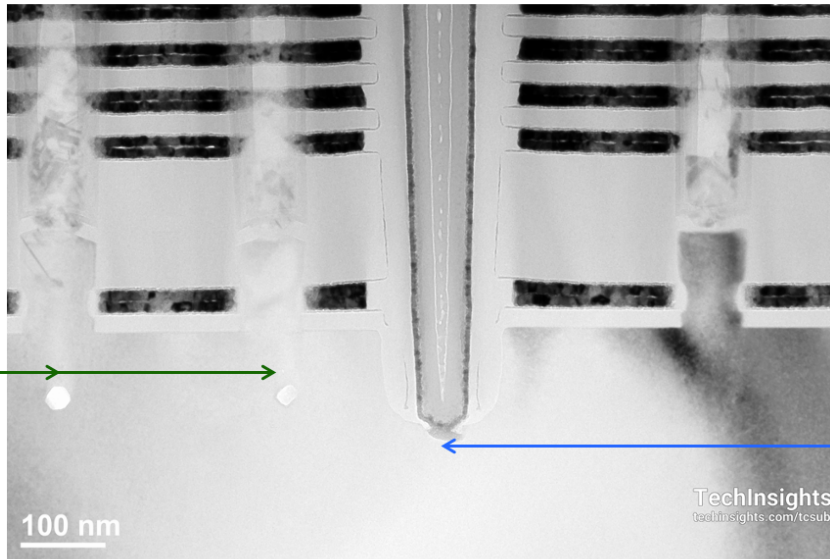
an upper end of each of the semiconductor pillars (H)

an upper diffusion layer (G)

one of a source and a drain (I)

a plurality of semiconductor pillars (A)

102. The SanDisk memory chip used in the Western Digital PC SN530 NVMe SSD is a semiconductor device comprising a lower diffusion layer operatively coupled to a lower end of each of the semiconductor pillars to serve as the other of the source and the drain:



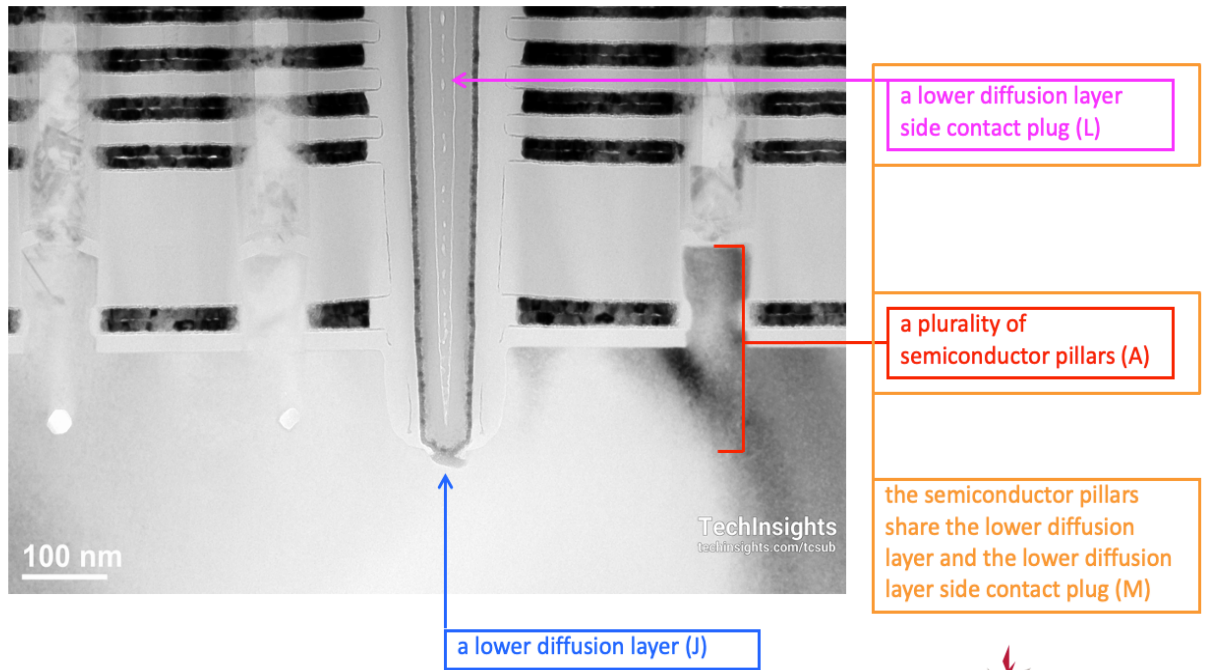
a lower end of each of the semiconductor pillars (K)

a lower diffusion layer (J)

RUSS, AUGUST & KABAT

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28

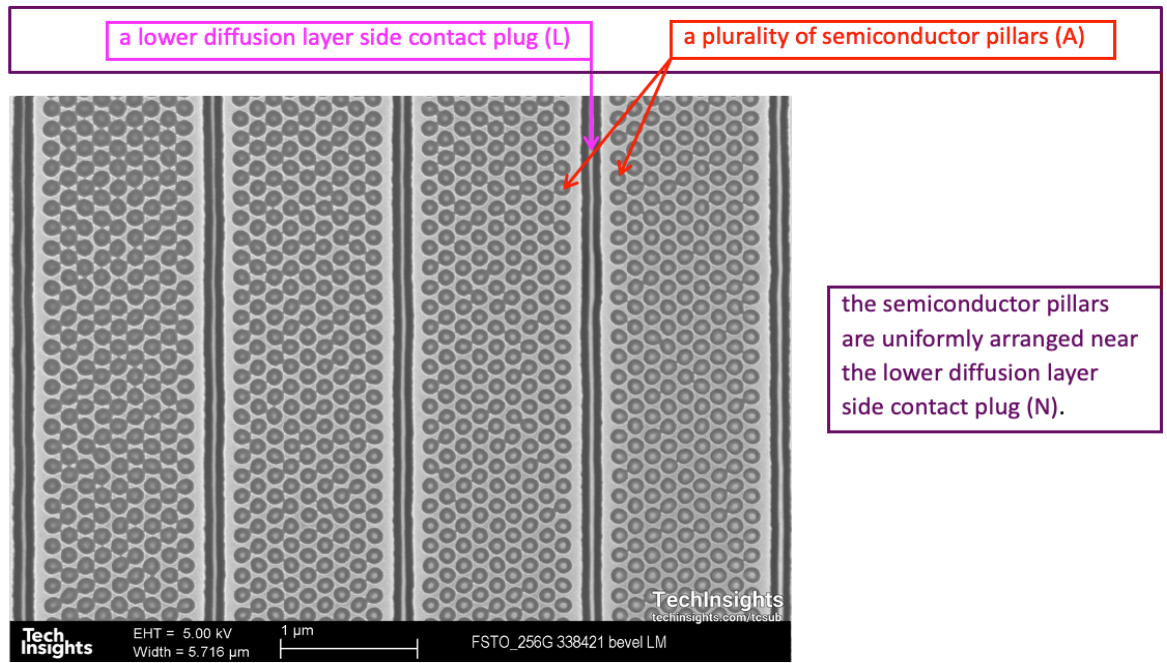
103. The SanDisk memory chip used in the Western Digital PC SN530 NVMe SSD is a semiconductor device comprising a lower diffusion layer side contact plug connected to the lower diffusion layer, wherein the semiconductor pillars share the lower diffusion layer and the lower diffusion layer side contact plug:



104. The SanDisk memory chip used in the Western Digital PC SN530 NVMe SSD is a semiconductor device wherein the semiconductor pillars are uniformly arranged near the lower diffusion side contact:

RUSS, AUGUST & KABAT

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28



105. Defendants actively, knowingly, and intentionally induce, and continue to actively, knowingly, and intentionally induce, infringement of the '233 patent under 35 U.S.C. §271(b) by their customers and end users.

106. Defendants have had knowledge of and notice of the '233 patent and their infringement since at least September 6, 2022 when Longitude gave Defendants notice of their infringing actions. In any event, Defendants have had knowledge and notice of the '233 patent since at least the filing of this complaint.

107. Defendants have induced their customers and end users to infringe the '233 patent by using their products as shown above. For example, Defendants encourage their customers and end users to perform infringing methods by the very nature of the products.

108. Defendants specifically intend their customers and/or end users infringe the '233 patent, either literally or by the doctrine of equivalents, because Defendants have known about the '233 patent and how Defendants' products infringe the claims of the '233 patent but Defendants have not taken steps to prevent infringement by their customers and/or end users. Accordingly, Defendants have acted with the specific intent to induce infringement of the '233 patent.

RUSS, AUGUST & KABAT

1 109. Accordingly, Defendants have induced, and continue to induce,
2 infringement of the '233 patent under 35 U.S.C. §271(b).

3 110. As discussed above, Defendants have had knowledge of and notice of
4 the '233 patent and its infringement since at least September 6, 2022. Despite this
5 knowledge, Defendants continue to commit tortious conduct by way of patent
6 infringement.

7 111. Defendants have been and continue to infringe one or more of the
8 claims of the '233 patent through the aforesaid acts.

9 112. Defendants have committed these acts of infringement without license
10 or authorization.

11 113. Plaintiff is entitled to recover damages adequate to compensate for the
12 infringement.

13 114. Defendants have and continue to infringe the '233 patent, acting with
14 an objectively high likelihood that their actions constitute infringement of the '233
15 patent. Defendants have known or should have known of this risk at least as early
16 as September 6, 2022. Accordingly, Defendants' infringement of the '233 patent has
17 been and continues to be willful.

18 **PRAYER FOR RELIEF**

19 Wherefore, Longitude, respectfully requests the following relief:

- 20 a) A judgment that Defendants have infringed the '369 patent;
21 b) A judgment that Defendants have infringed the '539 patent;
22 c) A judgement that Defendants have infringed the '233 patent;
23 d) A judgment that awards Plaintiff all appropriate damages under 35 U.S.C. §
24 284 for Defendants' past infringement, and any continuing or future
25 infringement of the Patents-in-Suit, up until the date such judgment is entered,
26 including interest, costs, and disbursements as justified under 35 U.S.C. § 284
27 to adequately compensate Plaintiff for Defendants' infringement;
28

RUSS, AUGUST & KABAT

- 1 e) An adjudication that Defendants' infringement of the Patents-in-Suit has been
- 2 willful and deliberate;
- 3 f) An adjudication that Plaintiff be awarded treble damages and pre-judgment
- 4 interest under 35 U.S.C. § 284 as a result of Defendants' willful and deliberate
- 5 infringement of the Patents-in-Suit;
- 6 g) An adjudication that this case is exceptional within the meaning of 35 U.S.C.
- 7 § 285;
- 8 h) An adjudication that Plaintiff be awarded the attorneys' fees, costs, and
- 9 expenses it incurs in prosecuting this action; and
- 10 i) An adjudication that Plaintiff be awarded such further relief at law or in equity
- 11 as the Court deems just and proper.

JURY TRIAL DEMANDED

Plaintiff hereby demands a trial by jury of all issues so triable.

Respectfully submitted,

DATED: January 9, 2023

RUSS, AUGUST & KABAT

/s/ Brian D. Ledahl

Brian D. Ledahl, SBN 186579

bledahl@raklaw.com

Paul A. Kroeger, SBN 229074

pkroeger@raklaw.com

12424 Wilshire Boulevard

Twelfth Floor

Los Angeles, California 90025

Telephone: (310) 826-7474

Facsimile: (310) 826-6991

*Attorneys for Plaintiff
Longitude Licensing, Ltd.*