**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

WINTERSPRING DIGITAL LLC,	§ § § §	
	§	Case No.
Plaintiff,	§ §	**JURY TRIAL DEMANDED**
v.	§ §	
	§	
MICROCHIP TECHNOLOGY INC.,	§ §	
	§	
Defendant.	§ §	
	§	

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Winterspring Digital LLC ("Winterspring" or "Plaintiff") for its Complaint against Microchip Technology Inc. ("Microchip" or "Defendant") alleges as follows:

THE PARTIES

1.   Winterspring is a limited liability company organized and existing under the laws of the State of Texas, with its principal place of business located at 104 East Houston Street, Marshall, Texas 75670

2.   Upon information and belief, Microchip is a corporation organized and existing under the laws of Delaware, with a regular and established place of business in this Judicial District, located at 2805 Dallas Parkway, Plano, Texas. Upon information and belief, Microchip does business in Texas and in the Eastern District of Texas, directly or through intermediaries.

JURISDICTION

3.   This is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. §§ 1, *et seq*. This Court has jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and 1338(a).

4.   This Court has personal jurisdiction over Defendant. Defendant regularly conducts business and has committed acts of patent infringement and/or has induced acts of patent infringement by others in this Judicial District and/or has contributed to patent infringement by others in this Judicial District, the State of Texas, and elsewhere in the United States.

5.   Venue is proper in this Judicial District as to Defendant Oracle pursuant to 28 U.S.C. §§ 1391 and 1400(b). Microchip has a regular and established place of business in this Judicial District, including in Collin County, and is deemed to reside in this Judicial District. Upon information and belief, Microchip has committed acts of infringement in this Judicial District, and/or has purposely transacted business involving the accused devices in this Judicial District including providing sales and technical support for the products accused of infringement herein.

6.   Defendant is subject to this Court's jurisdiction pursuant to due process and/or the Texas Long Arm Statute due at least to its substantial business in this State and Judicial District, including (a) at least part of its past infringing activities, (b) regularly doing or soliciting business in Texas, and/or (c) engaging in persistent conduct and/or deriving substantial revenue from goods and services provided to customers in Texas.

PATENTS-IN-SUIT

7.   On January 16, 2007, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 7,164,692 (the "'692 Patent") entitled "Apparatus and Method for

Transmitting 10 Gigabit Ethernet LAN Signals Over a Transport System." A true and correct copy

of the '692 Patent is available at http://pdfpiw.uspto.gov/.piw?docid=7164692.

8.   On September 2, 2008, the United States Patent and Trademark Office duly and

legally issued U.S. Patent No. 7,420,975 (the "'975 Patent") entitled "Method and Apparatus For

High-Speed Frame Tagger."   A true and correct copy of the '975 Patent is available at

http://pdfpiw.uspto.gov/.piw?docid=7420975.

9.   On August 10, 2010, the United States Patent and Trademark Office duly and

legally issued U.S. Patent No. 7,774,468 (the "'468 Patent") entitled "Network Traffic Admission

Control."   A   true   and   correct   copy   of   the   '468   Patent   is   available   at

http://pdfpiw.uspto.gov/.piw?docid=7774468.

10.   Winterspring is the sole and exclusive owner of all right, title, and interest in the

'692, '975, and '468, Patents (the "Patents-in-Suit") and holds the exclusive right to take all actions

necessary to enforce its rights to the Patent-in-Suit, including the filing of this patent infringement

lawsuit.   Winterspring also has the right to recover all damages for past, present, and future

infringement of the Patents-in-Suit and to seek injunctive relief as appropriate under the law.

FACTUAL ALLEGATIONS

11.   The Patents-in-Suit generally cover systems and methods for routing data over a

network.

12.   The '692 Patent generally discloses an apparatus and method for transmitting LAN

signals over a transport system. A system sends or receives a signal to or from a transport system,

converts the signal to an intermediate form, re-clocks the intermediate signal, reconverts and then

transmits the signal. The technology described in the '692 Patent was developed by Jeffrey Lloyd

Cox and Samir Satish Seth. By way of example, this technology is implemented today in microchips, SoCs and ASICs that receive, convert, monitor, and send 10-Gigabit LAN signals.

13.   The '975 Patent discloses an apparatus and methods for examining a packet, determining a protocol type and tagging the packet. The technology described in the '975 Patent was developed by Velamur Krishnamachari and Dinesh Annayya from Cypress Semiconductor Corporation. By way of example, this technology is implemented today in microchips, SoCs and ASICs which implement packet tagging.

14.   The '468 Patent discloses systems and methods for traffic admission control using real time bandwidth allocation. The technology described in the '468 Patent was developed by Siddhartha Nag, and Srikanth S. Kumar. By way of example, this technology is implemented today in microchips, SoCs, and ASICs that perform traffic admission control using real time bandwidth allocation.

15.   Microchip has infringed and is continuing to infringe the Patents-in-Suit by making, using, offering to sell, selling, and/or importing network switches, routers, and software which implement the technology disclosed in the above patents-in-suit.

COUNT I
(Infringement of the '692 Patent)

16.   Paragraphs 1 through 15 are incorporated by reference as if fully set forth herein.

17.   Winterspring has not licensed or otherwise authorized Defendant to make, use, offer for sale, sell, or import any products that embody the inventions of the '692 Patent.

18.   Defendant has and continues to directly infringe the '692 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States products that satisfy each and every limitation of one or more claims of the '692 Patent. Such products include ethernet

switches, ethernet PHYs, and transceivers, that receive, convert, monitor, and send 10GE LAN signals, including but not limited to the VSC7436, VSC7437; the SparX-IV Family of L2/L3 enterprise Gigabit Ethernet Switches with 10 Gbps Links, including, but not limited to, the VSC7440, VSC7444, VSC7448, and VSC7449; the SparX-5 Family of L2/L3 Enterprise 10G Ethernet Switches, including, but not limited to, the VSC7549, VSC7552, VSC7556, VSC7558, and VSC7546; the SparX-5i L2/L3 TSN-Enabled Industrial Ethernet Switches, including, but not limited to, the VSC7546TSN, VSC7549TSN, VSC7552TSN, VSC7556TSN, and VSC7558TSN; Ethernet transceivers, including, but not limited to, the VSC8489, VSC8490, and VSC8491 family.

19.   For example, Defendant has and continues to directly infringe at least claim 10 of the '692 Patent by making, using, offering to sell, selling, and/or importing into the United States products that receive, convert, monitor, and send 10GE LAN signals.

20.   For example, the Microchip VSC8491 transceiver performs a method transferring 10GE LAN client signals from a transport system to a client system comprising receiving the 10GE LAN client signal transmitted over the transport system, converting the 10GE LAN client signal to an intermediate signal, recovering clock data from the intermediate signal, recovering a data stream from the intermediate signal, reconverting the intermediate signal to the 10GE LAN client signal; transferring the 10GE LAN client signal to a client system; and monitoring the intermediate form with a monitoring device wherein the monitoring device is a 10GE LAN media access controller.

VSC8491 ☆

1 Port 10GbE XFI/SFI to (R)XAUI 1588 MACsec

Status: In Production.

⬇ **Download Data Sheet**   📄 **Documentation**   ∨ **Symbols**

VSC8489, VSC8490, and VSC8491 family of single-port and dual-port 10G Ethernet transceivers provides a highly flexible solution ideal for electrical backplane and optical module host card applications. Designed to meet all SFP+ SR/LR/ER/ZR Fiber, EDC compensated MMF, and direct attached cable host requirements (in accordance with the SFF-8431 specifications), the devices compensate for optical impairments in SFP+ applications along with degradations of the PCB. The VSC8489/90/91 device family also provides full 10GBASE-KR support (including Clause 73 auto-negotiation and Clause 72 transmit training), as well as highly flexible clocking options for Ethernet LAN and WAN operations and Synchronous Ethernet (Sync-E). [1]

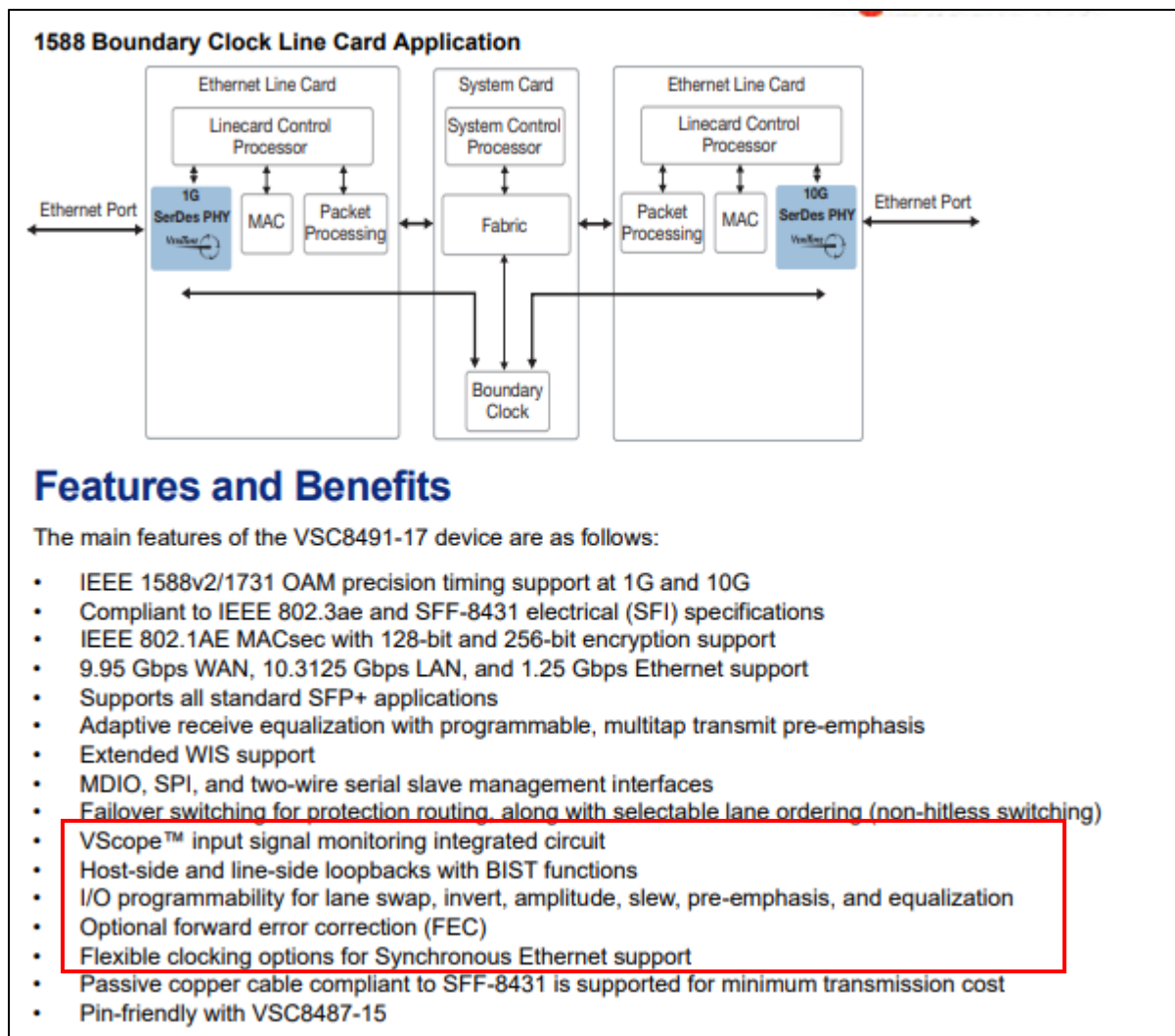The following illustrations show the various applications for the VSC8491-17 device.

Figure 2 •   SFP/SFP+ Application

[2]

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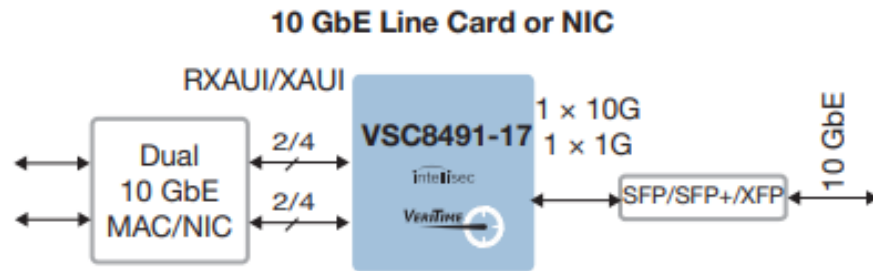
[1] https://www.microchip.com/en-us/product/VSC8491.

[2] "VSC8491-17 Datasheet WAN/LAN/Backplane RXAUI/XAUI to SFP+/KR 10 GbE SerDes PHY with IntelliSec™ and VeriTime™" (Pg. 4). Available at: https://ww1.microchip.com/downloads/en/DeviceDoc/VMDS-10506.pdf

1588 Boundary Clock Line Card Application

Features and Benefits

The main features of the VSC8491-17 device are as follows:

- IEEE 1588v2/1731 OAM precision timing support at 1G and 10G
- Compliant to IEEE 802.3ae and SFF-8431 electrical (SFI) specifications
- IEEE 802.1AE MACsec with 128-bit and 256-bit encryption support
- 9.95 Gbps WAN, 10.3125 Gbps LAN, and 1.25 Gbps Ethernet support
- Supports all standard SFP+ applications
- Adaptive receive equalization with programmable, multitap transmit pre-emphasis
- Extended WIS support
- MDIO, SPI, and two-wire serial slave management interfaces
- Failover switching for protection routing, along with selectable lane ordering (non-hitless switching)
- VScope™ input signal monitoring integrated circuit
- Host-side and line-side loopbacks with BIST functions
- I/O programmability for lane swap, invert, amplitude, slew, pre-emphasis, and equalization
- Optional forward error correction (FEC)
- Flexible clocking options for Synchronous Ethernet support
- Passive copper cable compliant to SFF-8431 is supported for minimum transmission cost
- Pin-friendly with VSC8487-15

[3]

21.   Defendant has and continues to indirectly infringe one or more claims of the '692

Patent by knowingly and intentionally inducing others, including Microchip customers and end-

users, to directly infringe, either literally or under the doctrine of equivalents, by making, using,

offering to sell, selling and/or importing into the United States microchips, SoCs, ASICs and other

products that receive, convert, monitor, and send 10GE LAN signals.

22.   Defendant, with knowledge that these products, or the use thereof, infringe the '692

Patent at least as of the date of this Complaint, knowingly and intentionally induced, and continues

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[3] *Id*. at 5.

to knowingly and intentionally induce, direct infringement of the '692 Patent by providing these products to end users for use in an infringing manner.

23.   Defendant induced infringement by others, including end users, with the intent to cause infringing acts by others or, in the alternative, with the belief that there was a high probability that others, including end users, infringe the '692 Patent, but while remaining willfully blind to the infringement.

24.   Winterspring has suffered damages as a result of Defendant's direct and indirect infringement of the '692 Patent in an amount to be proved at trial.

25.   Winterspring has suffered, and will continue to suffer, irreparable harm as a result of Defendant's infringement of the '692 Patent, for which there is no adequate remedy at law, unless Defendant's infringement is enjoined by this Court.

COUNT II
(Infringement of the '975 Patent)

26.   Paragraphs 1 through 15 are incorporated by reference as if fully set forth herein.

27.   Winterspring has not licensed or otherwise authorized Defendant to make, use, offer for sale, sell, or import any products that embody the inventions of the '975 Patent.

28.   Defendant has directly infringed the '975 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States products that satisfy each and every limitation of one or more claims of the '975 Patent. Such products include but are not limited to ethernet switches that implement packet tagging, including. but not limited to the VSC7410, VSC7415, VSC7414, VSC7416, VSC7418, VSC7420, VSC7421, VSC7422, VSC7423, VSC7424, VSC7425, VSC7426, VSC7427, VSC7428, VSC7429, VSC7439, VSC7431, VSC7432, VSC7434, VSC7435, VSC7436, VSC7437, VSC7438, VSC7440, VSC7442,

VSC7444, VSC7448, VSC7449, VSC7460, VSC7462, VSC7464, VSC7468, VSC7511, VSC7512, VSC7513, VSC7515, as well as the SparX-5 Family of L2/L3 Enterprise 10G Ethernet Switches.

29.   For example, Defendant has directly infringed at least claim 5 of the '975 Patent by making, using, offering to sell, selling, and/or importing into the United States products that perform packet tagging, including, but not limited, to Microchip Ethernet Switches.

30.   For example, the Microchip VSC7546 ethernet switch includes an apparatus comprising a network processor interface suitable for coupling to a network processor and a central processor interface suitable for coupling to a central processor. Upon information and belief, the Microchip VSC7546 ethernet switch further includes a protocol determination logic block to determine a protocol type of data in a packet, wherein the protocol determination logic compares the protocol information in a first pass to predetermined values to procedure a first result and, if the first result is positive, compares the protocol information in a second pass to predetermined values to produce a second result, the first and second results forming a set of results. Upon information and belief, the Microchip VSC7546 ethernet switch further comprises a tag select logic block to apply a tag to the packet indicating that the packet has an unknown protocol type if the first result is negative and if the first result is positive, the packet should be sent to either the central processor interface or the network processor interface based on the set of results.

Features

This section lists the key device features and benefits.

- Layer 2 and Layer 3 Forwarding
    – IEEE®802.1Q switch with 4K VLANs and 32K MAC table entries
    – Push/pop/translate up to three VLAN tags on ingress and egress
    – RSTP and MSTP support
    – Fully nonblocking wire-speed switching performance for all frame sizes
    – Link aggregation and DRNI per IEEE 802.1AX
    – External bridge port extender role per IEEE 802.1BR
    – IPv4/IPv6 unicast and multicast Layer 2 switching with up to 32K groups and 2K port masks
    – IPv4/IPv6 unicast and multicast Layer 3 forwarding (routing) with reverse path forwarding (RPF) support
    – IGMPv2, IGMPv3, MLDv1, and MLDv2 support

[4]

3.3   Enterprise Ethernet Flows

The Microchip flow-aware architecture enables a rich set of Enterprise Ethernet features using multiple lookups into VCAP classification matching (CLM). Up to 64 ingress DSCP mapping tables (64 entries each) can be used for more efficient TCAM utilization. Enterprise Ethernet flow policy attributes include:

- Mapping to a dual-rate policer. Multiple flows can map to one policer. Up to eight policers can be assigned per flow to implement the per-COS per-flow bandwidth profiles.
- Mapping to a VLAN (MAC table) resource and a flow-specific port map.
- Mapping to flow-specific arrival and departure frame modification instructions.
- Flow-specific QoS handling instructions including remarking and hierarchical QoS treatment.
- Per-flow arrival, departure, and discard statistics. Multiple flows can map to one statistics set. Up to eight statistics sets can be assigned to a flow to implement the per-CoS per-flow bandwidth profiles.

The overall processing architecture is shown in the following figure.

[5]

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[4] "Microchip SparX-5 Family of L2/L3 Enterprise 10g Ethernet Switches" (Pg. 1) available at: https://ww1.microchip.com/downloads/en/DeviceDoc/SparX-5_Family_L2L3_Enterprise_10G_Ethernet_Switches_Datasheet_00003822E.pdf.
[5] *Id*. At 13.

Layer 2 Forwarding

After the policers, the Layer 2 forwarding block of the analyzer handles all fundamental Layer 2 forwarding operations and maintains the associated MAC table, the VLAN table, and the aggregation table. The device implements a 32K MAC table and a 4K VLAN table.

The main task of the analyzer is to determine the destination port set of each frame. The Layer 2 forwarding decision is based on various information such as the frame's ingress port, source MAC address, destination MAC address, and the VLAN identifier, as well as the frame's VCAP actions, mirroring, and the destination port's link aggregation configuration.

Layer 2 forwarding of unicast and Layer 2 multicast frames is based on the destination MAC address and the VLAN.

The switch can also L2-forward IPv4 and IPv6 multicast frames using additional Layer-3 information, such as the source IP address. The latter enables source-specific IPv4 multicast forwarding (IGMPv3) and source-specific IPv6 multicast forwarding (MLDv2). This process of L2-forwarding multicast frames using Layer 3 information is called "snooping", which is different from L3-forwarding (routing) of multicast frames. [6]

Layer 3 Forwarding

The device supports Layer 3 forwarding (routing), which is performed by the analyzer. With Layer 3 forwarding, the IPv4 or IPv6 addresses determine the destination port set and Layer 3 processing is performed on IP header. The Layer 3 forwarding process also replaces the arrival Layer-2 Ethernet header (including MAC addresses and VLAN tags) with a new Layer 2 Ethernet header after departure from the switch.

The analyzer supports 511 router legs, and supports virtual router redundancy protocol (VRRP). Ingress router legs are addressed using classified arrival VLAN and DMAC address.

If an arrival frame is determined to belong to an ingress router leg and routing is enabled, Layer 3 forwarding is applied. Note that this is in addition to any Layer 2 forwarding, so for example, an arrival multicast frame may be Layer 2 forwarded on the classified arrival VLAN and also Layer 3 forwarded to one or more additional VLANs. A Layer 3 forwarded frame is always Layer 2 forwarded in the departure VLAN.

Layer 3 forwarding first checks the IP header for validity. IP header checks include IP version, header length, and header checksum. The time-to-live (TTL) or Hop Limit values are also checked for validity and decremented if the packet is forwarded.
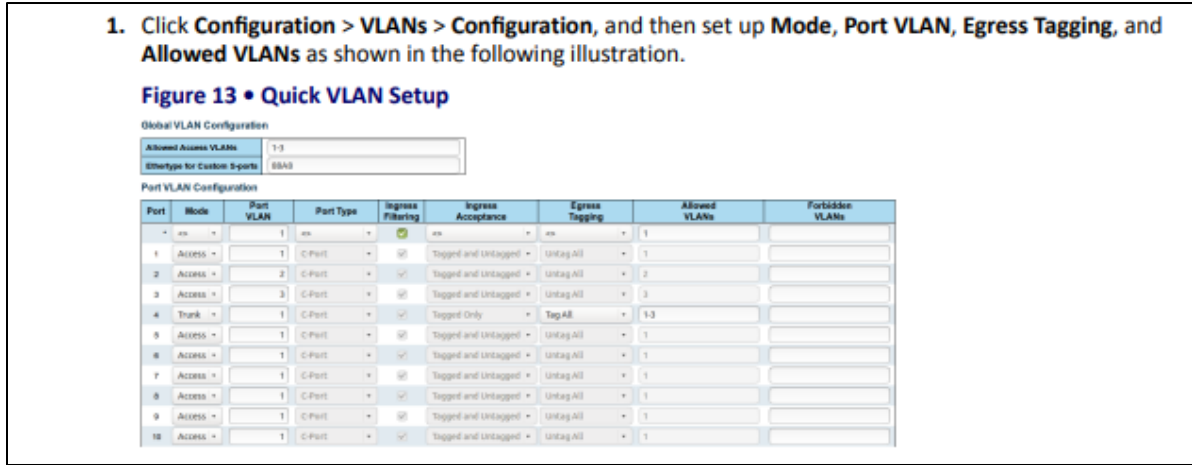
The analyzer then searches the longest prefix match (LPM) table for an exact match of the destination IP address. If there is not an exact match, the table is searched for the best partial match. If there is no partial match in the LPM table, the frame is Layer 3 forwarded to the location of the default gateway. [7]

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[6] *Id*. At 15.
[7] *Id*. At 16.

31.   Defendant has indirectly infringed one or more claims of the '975 Patent by knowingly and intentionally inducing others, including Microchip customers and end-users, to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling and/or importing into the United States microchips, SoCs, ASICs and other products that implement packet tagging.

32.   Defendant, with knowledge that these products, or the use thereof, infringed the '975 Patent at least as of the date of this Complaint, knowingly and intentionally induced, and continues to knowingly and intentionally induce, direct infringement of the '975 Patent by providing these products to end users for use in an infringing manner.

33.   Defendant induced infringement by others, including end users, with the intent to cause infringing acts by others or, in the alternative, with the belief that there was a high probability that others, including end users, infringe the '975 Patent, but while remaining willfully blind to the infringement.

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[8] "ENT-AN1115-4.3 Application Note Layer 2 Protocol Configuration Guide: January 2018" (Pg. 10). Available at: https://ww1.microchip.com/downloads/en/Appnotes/ENT-AN1115_4.3VPPD-04297.pdf.

COUNT III
(Infringement of the '468 Patent)

34.   Paragraphs 1 through 15 are incorporated by reference as if fully set forth herein.

35.   Winterspring has not licensed or otherwise authorized Defendant to make, use, offer for sale, sell, or import any products that embody the inventions of the '468 Patent.

36.   Defendant has and continues to directly infringe the '468 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States products that satisfy each and every limitation of one or more claims of the '468 Patent. Such products include which allow for traffic admission control using real time bandwidth allocation, including, but not limited to, the USB to Ethernet SoCs, including but not limited to USB to Ethernet bridges, including, but not limited to, the LAN7430, LAN7431, LAN7500, LAN7800, LAN7801; ethernet controllers, including, but not limited to, the ENC28J60, KSZ8441, LAN9115; ethernet switches, including, but not limited to, VSC7410, VSC7415, VSC7414, VSC7416, VSC7418, VSC7558; ethernet PHY, including, but not limited to, KSZ8001, LAN8670, and VSC8211; network interface controllers, including, but not limited to, OS8104A, OS81050, and OS81060.

37.   For example, Defendant has and continues to directly infringe at least claim 1 of the '468 Patent by making, using, offering to sell, selling, and/or importing into the United States products that hardware and software which allow for traffic admission control using real time bandwidth allocation, including but not limited to the VSC7558 enterprise switch.

38.   For example, the VSC7558 enterprise switch performs a method of a first edge node requesting from a director node, an amount of bandwidth over a first of a plurality of paths in a network between the first edge node and a second edge node, wherein the director node is configured to maintain information indicative of bandwidth available along each of the plurality
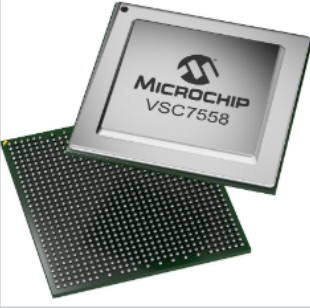
of paths. Upon information and belief, in response to the requested amount of bandwidth being available along the first path, the VSC7558 enterprise switch performs the step of the first edge node receiving, from the director node, an allocation of bandwidth as a real-time bandwidth pool associated with network resources in the first path. Upon information and belief, the VSC7558 enterprise switch performs the step of the first edge node receiving a connection request to establish a first real-time communication session between one of a first plurality of communication devices coupled to the first edge node and one of a second plurality of communication devices coupled to the second edge node. Upon information and belief, in response to determining that network resources in the real-time bandwidth pool are available to permit communication over the first path, the VSC7558 enterprise switch performs the step of the first edge node responding to the connection request by allocating a portion of the real-time bandwidth pool to the first real-time communication session.

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[9] https://www.microchip.com/en-us/solutions/ethernet-technology/consumer/broadband-gateway.
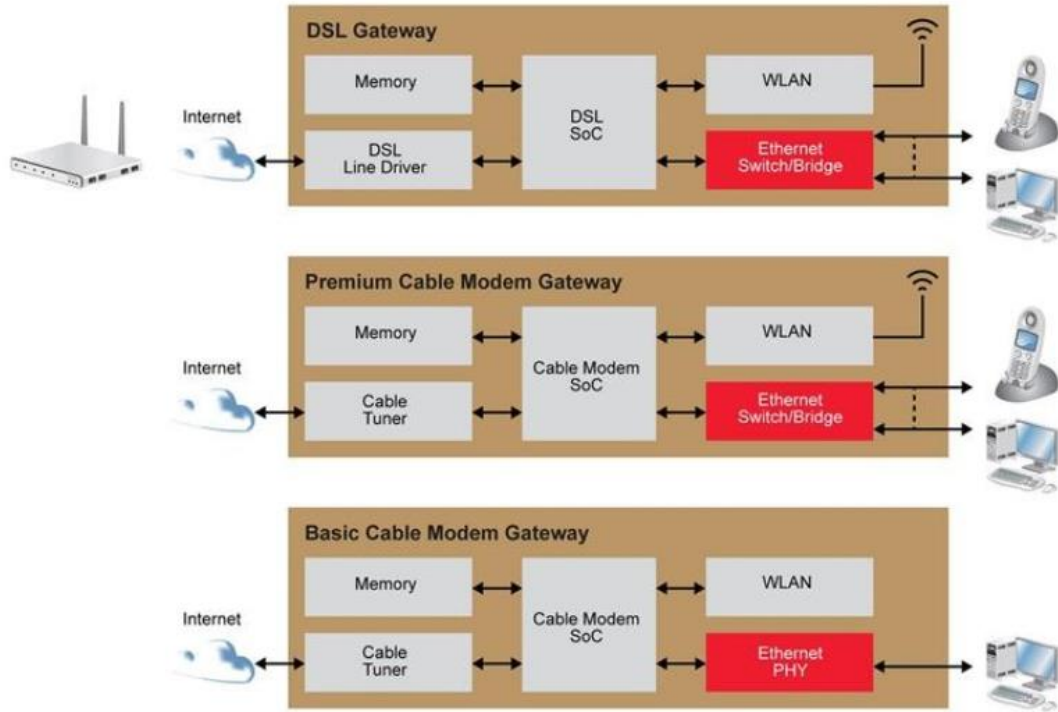
VSC7558 ☆

200G Enterprise Switch

Status: In Production.

🔻 Download Data Sheet   📄 Documentation   ∨ Symbols

🚗 Recommended for Automotive Design

The VSC7558 SparX-5-200 is a 200 Gbps SMB/SME Ethernet Switch supporting a combination of 1G, 2.5G, 5G, 10G, and 25G Ethernet ports.

The device provides a rich set of enterprise Ethernet switching features. Using multistage versatile content aware processor

(VCAP) technology, it delivers VLAN and QoS processing that enables delivery of differentiated services, security through intelligent frame processing and flexible frame manipulation.

[10]

Port policers can be configured to operate on logical ports instead of physical ports (ANA_AC_POL::POL_ALL_CFG.LPORT_POLICE_ENA), and thereby, allow policing of aggregated port bandwidth.

Traffic dropped by a policer can be counted by the port statistic block.

The following port policer debug events are available.

- Bypass of policer due to pipeline handling can be identified (ANA_AC_POL:POL_ALL_CFG:POL_STICKY.POL_PORT_PT_BYPASS_STICKY).
- Bypass of policer due to DP bypass level can be identified (ANA_AC_POL:POL_ALL_CFG:POL_STICKY.POL_PORT_BYPASS_STICKY).
- Dropping of traffic towards CPU due to policer can be identified (ANA_AC_POL:POL_ALL_CFG:POL_STICKY.POL_PORT_DROP_CPU_STICKY).
- Dropping of traffic towards front port due to policer can be identified (ANA_AC_POL:POL_ALL_CFG:POL_STICKY.POL_PORT_DROP_FWD_STICKY).
- Policers that are active, but not closed can be identified per policer (ANA_AC_POL:POL_ALL_CFG:POL_STICKY.POL_PORT_ACTIVE_STICKY).
- Policer triggering flow control can be identified (ANA_AC_POL:POL_ALL_CFG:POL_STICKY.POL_PORT_FC_STICKY).
- Policer leaving flow control state can be identified (ANA_AC_POL:POL_ALL_CFG:POL_STICKY.POL_PORT_FC_CLEAR_STICKY).

[11]

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[10] https://www.microchip.com/en-us/product/VSC7558.

[11] "Microchip SparX-5 Family of L2/L3 Enterprise 25G Ethernet Switches (Pg. 284) Available at:
https://ww1.microchip.com/downloads/aemDocuments/documents/UNG/ProductDocuments/DataSheets/SparX-5_Family_L2L3_Enterprise_25G_Ethernet_Switches_Datasheet_00003823D.pdf

39.   Defendant has and continues to indirectly infringe one or more claims of the '468 Patent by knowingly and intentionally inducing others, including Microchip customers and end-users, to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling and/or importing into the United States microchips, SoCs, ASICs, and other products which allow for traffic admission control using real time bandwidth allocation.

40.   Defendant, with knowledge that these products, or the use thereof, infringe the '468 Patent at least as of the date of this Complaint, knowingly and intentionally induced, and continues to knowingly and intentionally induce, direct infringement of the '468 Patent by providing these products to end users for use in an infringing manner.

41.   Defendant induced infringement by others, including end users, with the intent to cause infringing acts by others or, in the alternative, with the belief that there was a high probability that others, including end users, infringe the '468 Patent, but while remaining willfully blind to the infringement.

42.   Winterspring has suffered damages as a result of Defendant's direct and indirect infringement of the '468 Patent in an amount to be proved at trial.

43.   Winterspring has suffered, and will continue to suffer, irreparable harm as a result of Defendant's infringement of the '468 Patent, for which there is no adequate remedy at law, unless Defendant's infringement is enjoined by this Court.

DEMAND FOR JURY TRIAL

Plaintiff hereby demands a jury for all issues so triable.

PRAYER FOR RELIEF

WHEREFORE, Winterspring prays for relief against Defendant as follows:

a.   Entry of judgment declaring that Defendant has directly and/or indirectly infringed

one or more claims of the Patents-in-Suit;

b.   An order pursuant to 35 U.S.C. § 283 permanently enjoining Defendant, its officers, agents, servants, employees, attorneys, and those persons in active concert or participation with it, from further acts of infringement of one or more of the Patents-in-Suit;

c.   An order awarding damages sufficient to compensate Winterspring for Defendant's infringement of the Patents-in-Suit, but in no event less than a reasonable royalty, together with interest and costs;

d.   Entry of judgment declaring that this case is exceptional and awarding Winterspring its costs and reasonable attorney fees under 35 U.S.C. § 285; and,

e.   Such other and further relief as the Court deems just and proper.

Dated: January 13, 2023   Respectfully submitted,

                                                    /s/ *Vincent J. Rubino, III*
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