James R. Patterson, SBN 211102
jim@pattersonlawgroup.com
Jennifer M. French, SBN 265422
jenn@pattersonlawgroup.com
PATTERSON LAW GROUP, APC
1350 Columbia Street, Unit 603
San Diego, California 92101
Telephone: (619) 756-6990
Facsimile: (619) 756-6991

Alan Block (SBN 143783)
ablock@mckoolsmith.com
MCKOOL SMITH, P.C.
300 South Grand Avenue, Suite 2900
Los Angeles, California 90071
Telephone: (213) 694-1200
Facsimile: (213) 694-1234

Christopher R. Clayton* (MO SBN 69692)
DEVLIN LAW FIRM LLC
1526 Gilpin Avenue
Wilmington, Delaware 19806
Telephone: (302) 449-9010
Facsimile: (302) 353-4251
* *Admitted pro hac vice*

Attorneys for Plaintiff

IN THE UNITED STATES DISTRICT COURT

FOR THE SOUTHERN DISTRICT OF CALIFORNIA

BELL SEMICONDUCTOR, LLC Plaintiff, v. NXP USA, INC. Defendant.	**Case No. 3:22-cv-00594-H-KSC** **SECOND AMENDED COMPLAINT** **JURY TRIAL DEMANDED**

Plaintiff Bell Semiconductor, LLC ("Bell Semic" or "Plaintiff") brings this Complaint against Defendant NXP USA, Inc. ("NXP") for infringement of U.S. Patent No. 7,007,259 ("the '259 patent") and U.S. Patent No. 6,436,807 ("the '807 patent"). Plaintiff, on personal knowledge of its own acts, and on information and belief as to all others based on investigation, alleges as follows:

SUMMARY OF THE ACTION

1. This is a patent infringement suit relating to NXP's unauthorized and unlicensed use of the '259 and '807 patents. The circuit design methodologies claimed in the '259 and '807 patents are used by NXP in the production of one or more of its semiconductor chips, including at least the NXP LS1043A Quad-Core Networking Processor devices ("NXP Accused Product").

2. Semiconductor devices include different kinds of materials to function as intended. For example, these devices typically include both metal (*i.e.*, conductor) and insulator materials, which are deposited or otherwise processed sequentially in layers to form the final device. These layers—and the interconnects and components formed within them—have gotten much smaller over time, increasing the performance of these devices dramatically. As a result, it has become even more important to keep the layers planar as the device is being built because defects and warpage can cause fabrication issues and malfunctioning of the device. Manufacturers use a process called Chemical Mechanical Planarization/Polishing ("CMP") to smooth out the surface of the device to prepare the device for further processing, such as deposition of another layer. This allows subsequent layers to be built and connected more easily with fewer opportunities for short circuits or other errors that render the device defective. CMP functions best when there is a certain density and variance of the same material on the surface of the chip. This is because different materials will be "polished" away at different rates, leading to erosion or dishing on the surface. To reduce this problem "dummy" material, also known as "dummy fill," is typically inserted into low-density regions of the device

to increase the overall uniformity of the structures on the surface of the layer and reduce the density variability across the surface of the device. However, dummy fill can increase capacitance if it is placed too close to signal wires, which slows the transmission speed of signals and degrades the overall performance of the device.

3. Prior to development of the methodology described in the ’807 patent, the placement of dummy fill in the open areas of the interconnect layer was performed based upon a predetermined set density. However, use of predetermined set densities was not ideal because it often resulted in unnecessary placement of dummy fill and increased capacitance. For example, if the density of an active interconnect feature was high in relation to an adjacent open area, then it would not be necessary to place dummy fill in the corresponding open area at the predetermined density.

4. Recognizing these drawbacks, as well as the importance of having a flat or planarized surface on the devices, Donald Cwynar, Sudhanshu Misra, Dennis Ouma, Vivek Saxena, and John Sharpe (“the ’807 Inventors”), the inventors of the ’807 patent, set out to develop a design process that would achieve uniform density throughout the interconnect layer.

5. The ’807 Inventors ultimately conceived of a method for making the layout for an interconnect layout that allows for uniform density throughout the layer and facilitates planarization during manufacturing of the device. The claimed invention begins by determining an active interconnect feature density for each of a plurality of layout regions of the interconnect layout. Dummy fill is then added to each layout region in order to obtain a desired density of active interconnect features and dummy fill features in order to facilitate uniformity of planarization. In order to add dummy fill in this manner, one must define a minimum dummy fill feature lateral dimension based upon a dielectric layer deposition bias for a dielectric layer to be deposited over the interconnect layer.

6. The inventions disclosed in the ’807 patent provide many advantages over the prior art. In particular, having a uniform density for each layout region facilitates uniformity of planarization during manufacturing of the semiconductor device. *See* Ex. D at 3:3–5, 5:9–12. Furthermore, adding dummy fill features to obtain a desired density of active interconnect features and dummy fill features also helps ensure that dummy fill features are not unnecessarily added. *Id.* at 2:63–67, 5:19–22. Avoiding unnecessary dummy fill features is desirable because it deceases the parasitic capacitance of the interconnect layer. *Id.* at 2:67–3:2, 5:22-24. The invention claimed in the ’807 patent also provides for the selective positioning of dummy fill features, which minimizes parasitic capacitance. *Id.* at 5:28–33. These significant advantages are achieved through the use of the patented inventions and thus the ’807 patent presents significant commercial value for companies like NXP.

7. The development of the design methodology claimed in the ’259 patent represented another important advancement related to the design of semiconductor devices. Prior to development of the methodology described in the ’259 patent, the most widely implemented technology for insertion of dummy metal into a circuit design required hardcoding a large “stay–away” distance between the dummy metal and clock nets, which led to less space available for dummy metal insertion. This methodology often made it impossible to insert enough dummy metal to meet the required minimum density. The traditional dummy fill tools would often complete their run without reaching the minimum density, thus requiring at least a second run of the tool for the problem areas. In each problem area, the “stay-away” distance was reduced manually. And if there were more than one problem area, the manufacturer would have to make multiple runs of the tool, as it would have to address one problem area at a time. This was an involved, iterative process that had the potential to negatively impact the fabrication schedule and potentially the yield of the run, causing costs to go up.

8. Vikram Shrowty and Santhanakrishnan Raman ("the '259 Inventors"), the inventors of the '259 patent, understood the drawbacks of this "stay-away" design process and set out to develop a more efficient method for inserting dummy metal into a circuit design. The '259 Inventors ultimately conceived of a dummy fill procedure that minimizes the negative timing impact of dummy metal on clock nets, while still achieving minimum density in a single run. The claimed invention begins by identifying free spaces on each layer of the circuit design suitable for dummy metal insertion as dummy regions. The dummy regions are then prioritized such that the dummy regions located adjacent to clock nets are filled with dummy metal last, thereby minimizing any timing impact on the clock nets.

9. The inventions disclosed in the '259 patent provide many advantages over the prior art. In particular, they provide a simple and efficient method for dummy metal insertion that minimizes the timing impact to clock nets and at the same time guarantees reaching minimum density in a single pass. *See* Ex. A at 6:11–15. As mentioned above, the patented invention results in the dummy regions being prioritized such that the dummy regions located adjacent to clock nets are filled with dummy metal last, thereby minimizing the timing impact on the clock nets. *See* Ex. A at 2:29–47. Additionally, some embodiments of the patented invention further prioritize the dummy regions such that the dummy regions adjacent to wider clock nets are filled with dummy metal after dummy regions that are located adjacent to narrower clock nets. *See* Ex. A at 2:35–39. These significant advantages are achieved through the use of the patented inventions and thus the '259 patent presents significant commercial value for companies like NXP.

10. Bell Semic brings this action to put a stop to NXP's unauthorized and unlicensed use of the inventions claimed in the '259 and '807 patents.

THE PARTIES

11. Plaintiff Bell Semic is a limited liability company organized under the laws of the State of Delaware with a place of business at One West Broad Street, Suite 901, Bethlehem, PA 18018.

12. Bell Semic stems from a long pedigree that began at Bell Labs. Bell Labs sprung out of the Bell System as a research and development laboratory, and eventually became known as one of America's greatest technology incubators. Bell Labs employees invented the transistor in 1947 in Murray Hill, New Jersey. It was widely considered one of the most important technological breakthroughs of the time, earning the inventors the Nobel Prize in Physics. Bell Labs made the first commercial transistors at a plant in Allentown, Pennsylvania. For decades, Bell Labs licensed its transistor patents to companies throughout the world, creating a technological boom that led to the use of transistors in the semiconductor devices prevalent in most electronic devices today.

13. Bell Semic, a successor to Bell Labs' pioneering efforts, owns over 1,900 worldwide patents and applications, approximately 1,500 of which are active United States patents. This patent portfolio of semiconductor–related inventions was developed over many years by some of the world's leading semiconductor companies, including Bell Labs, Lucent Technologies, Agere Systems, and LSI Logic and LSI Corporation ("LSI"). This portfolio reflects technology that underlies many important innovations in the development of semiconductors and integrated circuits for high–tech products, including smartphones, computers, wearables, digital signal processors, IoT devices, automobiles, broadband carrier access, switches, network processors, and wireless connectors.

14. The principals of Bell Semic all worked at Bell Labs' Allentown facility, and have continued the rich tradition of innovating, licensing, and helping the industry at large since those early days at Bell Labs. For example, Bell Semic's CTO was a LSI

Fellow and Broadcom Fellow. He is known throughout the world as an innovator with more than 300 patents to his name, and he has a sterling reputation for helping semiconductor fabs improve their efficiency. Bell Semic's CEO took a brief hiatus from the semiconductor world to work with Nortel Networks in the telecom industry during its bankruptcy. His efforts saved the pensions of tens of thousands of Nortel retirees and employees. In addition, several Bell Semic executives previously served as engineers at many of these companies and were personally involved in creating the ideas claimed throughout Bell Semic's extensive patent portfolio.

15. On information and belief, NXP has its principal place of business and headquarters at 6501 William Cannon Drive West, Austin, TX 78735.

16. On information and belief, NXP develops, designs, and/or manufactures products in the United States, including in this District, according to the '259 and '807 patented processes/methodologies; and/or uses the '259 and '807 patented processes/methodologies in the United States, including in this District, to make products; and/or distributes, markets, sells, or offers to sell in the United States and/or imports products into the United States, including in this District, that were manufactured or otherwise produced using the patented process. Additionally, NXP introduces those products into the stream of commerce knowing that they will be sold and/or used in this District and elsewhere in the United States.

JURISDICTION AND VENUE

17. This is an action for patent infringement arising under the Patent Laws of the United States, Title 35 of the United States Code. Accordingly, this Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

18. This Court has personal jurisdiction over NXP under the laws of the State of California, due at least to its substantial business in California and in this District. NXP has purposefully and voluntarily availed itself of the privileges of conducting business in the United States, in the State of California, and in this District by

continuously and systematically placing goods into the stream of commerce through an established distribution channel with the expectation that they will be purchased by consumers in this District. In the State of California and in this District, NXP, directly: (i) performs at least a portion of the infringements alleged herein; (ii) develops, designs, and/or manufactures products according to the '259 and '807 patented processes/methodologies; (iii) distributes, markets, sells, or offers to sell products formed according to the '259 and '807 patented processes/methodologies; and/or (iv) imports products formed according to the '259 and '807 patented processes/methodologies.

19. On information and belief, venue is proper in this Court pursuant to 28 U.S.C. §§ 1391 and 1400 because NXP has committed, and continues to commit, acts of infringement in this District and has a regular and established place of business in this District. For example, NXP maintains a regular and established place of business in the District at Innovation Drive, Suite 150, San Diego, CA 92128. On information and belief, NXP current employs more than 75 engineers in the San Diego area. *See* Search Results for Current NXP Employees, LinkedIn (available at https://www.linkedin.com/search/results/people/?currentCompany=%5B%221088%22%5D&geoUrn=%5B%22103918656%22%2C%2290010472%22%5D&keywords=engineer&origin=FACETED_SEARCH&sid=or8) (last visited January 6, 2022).

20. Currently, on information and belief, NXP is advertising jobs in the San Diego area. These positions include those that relate to the '259 and '807 patented technologies, such as a position for an MCU/MPU Engineering Quality and Infrastructure PM. *See NXP Job Listings,* NXP (https://nxp.wd3.myworkdayjobs.com/careers?Location_Country=bc33aa3152ec42d4995f4791a106ed09&locations=98d67abaaa8a100fa6344859d7d49369) (last visited January 6, 2022).

21. Venue is also convenient in this District. This is at least true because of this District's close ties to this case—including the technology, relevant witnesses, and sources of proof noted above—and its ability to quickly and efficiently move this case to resolution.

22. On information and belief, Bell Semic's cause of action arises directly from NXP's circuit design work and other activities in this District. Moreover, on information and belief, NXP has derived substantial revenues from its infringing acts occurring within the State of California and within this District.

U.S. PATENT NO. 7,007,259

23. Bell Semiconductor is the owner by assignment of the '259 patent. The '259 patent is titled "Method for Providing Clock-Net Aware Dummy Metal Using Dummy Regions."

24. A true and correct copy of the '259 patent is attached as Exhibit A.

25. The inventors of the '259 patent are Vikram Shrowty and Santhanakrishnan Raman.

26. The application that resulted in issuance of the '259 patent was filed on July 31, 2003. The '259 patent claims priority to July 31, 2003.

27. The '259 patent generally relates to "methods for patterning dummy metal to achieve planarity for chemical-mechanical polishing of integrated circuits, and more particularly to a dummy fill software tool that provides clock-net aware dummy metal using dummy regions." Ex. A at 1:7–11.

28. The background section of the '259 patent identifies the shortcomings of the prior art. More specifically, the specification describes that the prior circuit design methodology was disadvantageous because it was "often impossible to insert enough dummy metal into a tile to meet the required minimum density without reducing the large dummy-to-clock distance." Ex. A at 2:3–10. Use of this design process meant that a second run of the metal-fill tool was often required in order to meet the density

requirements for all of the tiles. Ex. A at 2:10–14. Having to rerun the tool to meet the density requirements made the design process an "involved, iterative process[,]" which could "significantly impact the design schedule." Ex. A at 2:14–18.

29. In light of the drawbacks of the prior art, the '259 Inventors recognized the need to "minimize[] the negative timing impact of dummy metal on clock nets, while at the same time achieving minimum density in a single run." Ex. A at 2:19–23. The inventions claimed in the '259 patent addresses this need.

30. The '259 patent contains three independent claims and 37 total claims, covering a method and computer readable medium for circuit design. Claim 1 reads:

> 1. A method for inserting dummy metal into a circuit design, the circuit design including a plurality of objects and clock nets, the method comprising:
>
> (a) identifying free spaces on each layer of the circuit design suitable for dummy metal insertion as dummy regions, and
>
> (b) prioritizing the dummy regions such that the dummy regions located adjacent to clock nets are filled with dummy metal last, thereby minimizing any timing impact on the clock nets.

31. This claim, as a whole, provides significant as a whole, provides significant benefits and improvements to the function of the semiconductor device, *e.g.*, minimizing the negative timing impact of dummy metal on clock nets while also reducing the opportunity for dishing and erosion that could result in inaccurate transfer of patterns during lithography, suboptimal layouts/designs, inaccurate timing, reduced signal integrity, crosstalk delay, noise issues increased probability of failure, and ultimately defective or underperforming devices. *See, e.g.*, Ex. A at 6:11–15.

32. The claims of the '259 patent also recite inventive concepts that improve the functioning of the fabrication process, particularly as to dummy filling. The claims of the '259 patent disclose a new and novel solution to specific problems related to

improving semiconductor fabrication. As explained in detail above and in the ’259 patent specification, the claimed inventions improve upon the prior art processes by prioritizing dummy regions such that the dummy regions located adjacent to clock nets are filled with dummy metal last. This has the advantage of reducing the impact of dummy metal on signal and clock lines and increasing the efficiency, yield, and design/layout miniaturization and flexibility of the manufacturing process. The claimed inventive processes also increase performance and signal integrity, while reducing crosstalk delay, noise issues, probability of failure, and defective and/or underperforming devices.

U.S. PATENT NO. 6,436,807

33. Bell Semic is the owner by assignment of the ’807 patent. The ’807 patent is titled “Method for Making an Interconnect Layer and a Semiconductor Device Including the Same.” The ’807 patent issued on August 20, 2002. A true and correct copy of the ’807 patent is attached as Exhibit D.

34. The inventors of the ’807 patent are Donald Cwynar, Sudhanshu Misra, Dennis Ouma, Vivek Saxena, and John Sharpe.

35. The application that resulted in the issuance of the ’807 patent was filed on January 18, 2000. The ’807 patent claims priority to January 18, 2000.

36. The ’807 patent generally relates to “a method for making a layout for an interconnect layer that has uniform density throughout to facilitate planarization during manufacturing of a semiconductor device.” Ex. D at 2:43–46. The background section of the ’807 patent identifies the shortcomings of the prior art. More specifically, the specification describes that the prior circuit design methodology was disadvantageous because it could lead to “protrusions[] in the upper surface of the dielectric material[] above respective active interconnect features[.]” *Id.* at 1:40–42. The specification states that “if pattern density variations of the active interconnect features[] are large, CMP is not adequate to sufficiently planarize the interconnect layer[.]” *Id.* at 1:67–2:2.

Although "[c]onventional layout algorithms" were typically used to place dummy fill features in open areas of the interconnect layer, those algorithms placed dummy metal "based upon a predetermined set density." *Id.* at 2:17–21. Relying on "predetermined set densit[ies]" could lead to the unnecessary placement of dummy fill features, which in turn could increase the parasitic capacitance of the interconnect layer. *Id.* at 2:31–33. The specification notes that "variations in the density of the interconnect layer [could] cause deviations when the interconnect layer [was] planarized." *Id.* at 2:35–37.

37. In light of the drawbacks of the prior art, the '807 Inventors recognized "a need for making a layout for an interconnect layer that determines placement of dummy fill features for achieving a uniform density throughout the interconnect layer." Ex. D at 2:37–40. The inventions claimed in the '807 patent address this need.

38. The '807 patent contains two independent claims and 18 total claims. Claim 1 reads:

> 1. A method for making a layout for an interconnect layer of a semiconductor device to facilitate uniformity of planarization during manufacture of the semiconductor device, the method comprising the steps of:
>
> (a) determining an active interconnect feature density for each of a plurality of layout regions of the interconnect layout; and
>
> (b) adding dummy fill features to each layout region to obtain a desired density of active interconnect features and dummy fill features to facilitate uniformity of planarization during manufacturing of the semiconductor device, the adding comprising defining a minimum dummy fill feature lateral dimension based upon a dielectric layer deposition bias for a dielectric layer to be deposited over the interconnect layer.

39. This claim, as a whole, provides significant benefits and improvements to the function of the semiconductor device, *e.g.*, uniform planarization during

manufacturing, avoidance of adding unnecessary dummy fill features, and minimizing parasitic capacitance. *See, e.g.*, Ex. D at 5:9–34.

40. The claims of the ’807 patent also recite inventive concepts that improve the functioning of the fabrication process, particularly as to dummy filling. The claims of the ’807 patent disclose a new and novel solution to specific problems related to improving semiconductor fabrication. As explained in detail above and in the ’807 patent specification, the claimed inventions improve upon the prior art processes by determining an active interconnect feature density for each of a plurality of layout regions of the interconnect layout and adding dummy fill to each layout region to obtain a desired density of active interconnect features and dummy fill features to facilitate uniformity of planarization. This has advantages such as avoiding the unnecessary adding of dummy fill features and minimizing the parasitic capacitance of the interconnect layer.

COUNT I – INFRINGEMENT OF U.S. PATENT NO. 7,007,259

41. Bell Semic re-alleges and incorporates by reference the allegations of the foregoing paragraphs as if fully set forth herein.

42. The ’259 patent is valid and enforceable under the United States Patent Laws.

43. Bell Semic owns, by assignment, all right, title, and interest in and to the ’259 patent, including the right to collect for past damages.

44. A copy of the ’259 patent is attached at Exhibit A.

45. On information and belief, NXP has and continues to directly infringe pursuant to 35 U.S.C. § 271(a) one or more claims of the ’259 patent by using the patented methodology to design one or more semiconductor devices, including as one example the NXP Accused Product, in the United States.

46. On information and belief, NXP employs a variety of design tools, for example, Cadence, Synopsys, and/or Siemens tools, to insert dummy metal into a

circuit design (the "'259 Accused Processes") as recited in the '259 patent claims. As one example, NXP's Accused Processes perform a method for inserting dummy metal into a circuit design, where the circuit design includes a plurality of objects and clock nets as required by claim 1 of the '259 patent. NXP does so by employing a design tool, such as at least one of a Cadence, Synopsys, and/or Siemens tool, to insert dummy metal into a circuit design for the NXP Accused Product. The NXP Accused Product's design includes a plurality of objects, such as cells, interconnects, signal nets, and clock nets.

47. NXP's '259 Accused Processes also identify free spaces on each layer of the circuit design suitable for dummy metal insertion as dummy regions. NXP does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, to identify free spaces on each layer of the NXP Accused Product's circuit designs suitable for dummy metal insertion as dummy regions.

48. NXP's '259 Accused Processes also prioritize the dummy regions such that the dummy regions located adjacent to clock nets are filled with dummy metal last, thereby minimizing any timing impact on the clock nets. NXP does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, to prioritize dummy regions such that those adjacent to clock nets are filled with dummy metal last. For example, the '259 Accused Processes assign a "high cost" to adding metal fill near the clock nets and "lower cost" to adding metal fill near signal, power, and ground nets. Assigning "cost" in this way fills dummy regions adjacent to clock nets last and minimizes any timing impact on the clock nets.

49. An exemplary infringement analysis showing infringement of one or more claims of the '259 patent is set forth in Exhibit B. The declaration of Lloyd Linder, an expert in the field of semiconductor device design, is attached at Exhibit C and further describes NXP's infringement of the '259 patent.

50. NXP's '259 Accused Processes infringe and continue to infringe one or more claims of the '259 patent during the pendency of the '259 patent.

51. On information and belief, NXP has and continues to infringe directly pursuant to 35 U.S.C. § 271, *et. seq.*, either literally or under the doctrine of equivalents, by using the '259 Accused Processes in violation of one or more claims of the '259 patent. NXP has and continues to infringe directly pursuant to 35 U.S.C. § 271, *et. seq.*, either literally or under the doctrine of equivalents, by making, selling, or offering to sell in the United States, or importing into the United States products manufactured or otherwise produced using the '259 Accused Processes in violation of one or more claims of the '259 patent.

52. NXP's infringement of the '259 patent is exceptional and entitles Bell Semic to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

53. Bell Semic has been damaged by NXP's infringement of the '259 patent and will continue to be damaged unless NXP is enjoined by this Court. Bell Semic has suffered and continues to suffer irreparable injury for which there is no adequate remedy at law. The balance of hardships favors Bell Semic, and public interest is not disserved by an injunction.

54. Bell Semic is entitled to recover from NXP all damages that Bell Semic has sustained as a result of NXP's infringement of the '259 patent, including without limitation and/or not less than a reasonable royalty.

COUNT II – INFRINGEMENT OF U.S. PATENT NO. 6,436,807

55. Bell Semic re-alleges and incorporates by reference the allegations of the foregoing paragraphs as if fully set forth herein.

56. The '807 patent is valid and enforceable under the United States Patent Laws.

57. Bell Semic owns, by assignment, all right, title, and interest in and to the ’807 patent, including the right to collect for past damages.

58. A copy of the ’807 patent is attached at Exhibit D.

59.On information and belief, NXP has and continues to directly infringe pursuant to 35 U.S.C. § 271(a) one or more claims of the ’807 patent by using the patented methodology to design one or more semiconductor devices, including as one example the NXP Accused Product, in the United States.

60. On information and belief, NXP employs a variety of design tools, for example, Cadence, Synopsys, and/or Siemens tools, to make a layout for an interconnect layer of a semiconductor device (the “’807 Accused Processes”) as recited in the ’807 patent claims. As one example, NXP’s ’807 Accused Processes perform a method for making a layout for an interconnect layer of a semiconductor device, where the layout facilitates uniformity of planarization during manufacture of the semiconductor device as required by claim 1 of the ’807 patent. NXP does so by employing a design tool, such as at least one of a Cadence, Synopsys, and/or Siemens tool, to make a layout for the interconnect layer of its NXP Accused Product. The NXP Accused Product layout facilitates uniformity of planarization during manufacture of the device.

61. NXP’s ’807 Accused Processes also determine an active interconnect feature density for each of a plurality of layout regions of the interconnect layout. NXP does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, to determine an active interconnect feature density for each of a plurality of layout regions of the interconnect layout of its Accused Product.

62. NXP’s ’807 Accused Processes also add dummy fill features to each layout region to obtain a desired density of active interconnect features and dummy fill features to facilitate uniformity of planarization during manufacturing of the semiconductor device, the adding comprising defining a minimum dummy fill feature

lateral dimension based upon a dielectric layer deposition bias for a dielectric layer to be deposited over the interconnect layer.

63. NXP does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, to add dummy fill features to each layout region to obtain a desired density of active interconnect features and dummy fill features to facilitate uniformity of planarization during manufacturing of the semiconductor device. The adding of dummy fill through the use of these design tools comprises defining a minimum dummy fill feature lateral dimension based upon a dielectric layer deposition bias for a dielectric layer to be deposited over the interconnect layer. An exemplary infringement analysis showing infringement of one or more claims of the ’807 patent is set forth in Exhibit E. The declaration of Lloyd Linder, an expert in the field of semiconductor device design, is attached at Exhibit C and further describes NXP’s infringement of the ’807 patent.

64. NXP’s ’807 Accused Processes infringe and continue to infringe one or more claims of the ’807 patent during the pendency of the ’807 patent.

65. On information and belief, NXP has and continues to infringe directly pursuant to 35 U.S.C. § 271, *et. seq.*, either literally or under the doctrine of equivalents, by using the ’807 Accused Processes in violation of one or more claims of the ’807 patent. NXP has and continues to infringe directly pursuant to 35 U.S.C. § 271, *et. seq.*, either literally or under the doctrine of equivalents, by making, selling, or offering to sell in the United States, or importing into the United States products manufactured or otherwise produced using the ’807 Accused Processes in violation of one or more claims of the ’807 patent.

66. NXP’s infringement of the ’807 patent is exceptional and entitles Bell Semic to attorneys’ fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

67. Bell Semic is entitled to recover from NXP all damages that Bell Semic has sustained as a result of NXP's infringement of the '807 patent, including without limitation and/or not less than a reasonable royalty.

PRAYER FOR RELIEF

WHEREFORE, Bell Semic respectfully requests that this Court enter judgment in its favor as follows and award Bell Semic the following relief:

(a) a judgment declaring that NXP has infringed one or more claims of the '259 and '807 patents in this litigation pursuant to 35 U.S.C. § 271, *et seq.*;

(b) an award of damages adequate to compensate Bell Semic for infringement of the '259 and '807 patents by NXP, in an amount to be proven at trial, including supplemental post-verdict damages until such time as NXP ceases its infringing conduct;

(c) a permanent injunction, pursuant to 35 U.S.C. § 283, prohibiting NXP and its officers, directors, employees, agents, consultants, contractors, suppliers, distributors, all affiliated entities, and all others acting in privity with NXP, from committing further acts of infringement with respect to the '259 patent;

(d) a judgment requiring NXP to make an accounting of damages resulting from NXP's infringement of the '259 and '807 patents;

(e) the costs of this action, as well as attorneys' fees as provided by 35 U.S.C. § 285;

(f) pre-judgment and post-judgment interest at the maximum amount permitted by law;

(g) all other relief, in law or equity, to which Bell Semic is entitled.

Dated: January 31, 2023

/s/ Alan Block

Alan Block (SBN 143783)
ablock@mckoolsmith.com
MCKOOL SMITH, P.C.
300 South Grand Avenue, Suite 2900
Los Angeles, California 90071
Telephone: (213) 694-1200
Facsimile: (213) 694-1234

James R. Patterson, SBN 211102
jim@pattersonlawgroup.com
Jennifer M. French, SBN 265422
jenn@pattersonlawgroup.com
PATTERSON LAW GROUP, APC
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Telephone: (619) 756-6990
Facsimile: (619) 756-6991

Christopher R. Clayton* (MO SBN 69692)
DEVLIN LAW FIRM LLC
1526 Gilpin Avenue
Wilmington, Delaware 19806
Telephone: (302) 449-9010
Facsimile: (302) 353-4251
* *Admitted pro hac vice*

Attorneys for Plaintiff Bell Semiconductor, LLC

DEMAND FOR JURY TRIAL

Plaintiff hereby demands a jury trial for all issues so triable.

Dated: January 31, 2023

/s/ Alan Block

Alan Block (SBN 143783)
ablock@mckoolsmith.com
MCKOOL SMITH, P.C.
300 South Grand Avenue, Suite 2900
Los Angeles, California 90071
Telephone: (213) 694-1200
Facsimile: (213) 694-1234

James R. Patterson, SBN 211102
jim@pattersonlawgroup.com
Jennifer M. French, SBN 265422
jenn@pattersonlawgroup.com
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1350 Columbia Street, Unit 603
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Telephone: (619) 756-6990
Facsimile: (619) 756-6991

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DEVLIN LAW FIRM LLC
1526 Gilpin Avenue
Wilmington, Delaware 19806
Telephone: (302) 449-9010
Facsimile: (302) 353-4251
* *Admitted pro hac vice*

Attorneys for Plaintiff Bell Semiconductor, LLC