IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
SHERMAN DIVISION

BELL SEMICONDUCTOR, LLC Plaintiff, v. TEXAS INSTRUMENTS, INCORPORATED Defendant.	**Civil Action No. ______________** **JURY TRIAL DEMANDED**

ORIGINAL COMPLAINT

Plaintiff Bell Semiconductor, LLC ("Bell Semic" or "Plaintiff") brings this Complaint against Defendant Texas Instruments Incorporated ("Defendant" or "TI") for infringement of U.S. Patent Nos. 7,007,259 ("the '259 patent"), 6,436,807 ("the '807 patent"), 7,149,989 ("the '989 patent"), 7,260,803 ("the '803 patent"), No. 7,231,626 ("the '626 patent") and U.S. Patent No. 7,396,760 ("the '760 patent") (collectively, the "Asserted Patents"). Plaintiff, on personal knowledge of its own acts, and on information and belief as to all others based on investigation, alleges as follows:

SUMMARY OF THE ACTION

1. This is a patent infringement suit relating to TI's unauthorized and unlicensed use of the Asserted Patents. The circuit design methodology claimed in the Asserted Patents is used by TI in the production of one or more of its devices, including but not limited to its exemplary TI 66AH2H12 Multicore DSP+ARM KeyStone II SoC, ADS1261, DRV2614, RM48L952, and TM4C123GH6PGE ("Exemplary Accused Products").

2. Semiconductor devices include different kinds of materials to function as intended. For example, these devices typically include both metal (i.e., conductor) and insulator materials, which are deposited or otherwise processed sequentially in layers to form the final device. These layers—and the interconnects and components formed within them—have gotten much smaller over time, increasing the performance of these devices dramatically. As a result, it has become even more important to keep the layers planar as the device is being built because defects and warpage can cause fabrication issues and malfunctioning of the device.

3. Manufacturers use a process called Chemical Mechanical Planarization/Polishing ("CMP") to smooth out the surface of the device periodically between deposition and/or etching of each layer. This allows subsequent layers to be built and connected more easily with fewer opportunities for short circuits or other errors that render the device defective. CMP functions best when there is a certain density and variance of the same material on the surface of the chip. This is because different materials will be "polished" away at different rates, leading to erosion or dishing on the surface. To reduce this problem "dummy" material, also known as "dummy fill," is typically inserted into low- density regions of the device to increase the overall uniformity of the structures on the surface of the layer and reduce the density variability across the surface of the device. Dummy fill is most effective at avoiding dishing if its minimum lateral dimension is based on the deposition bias of the dielectric material deposited over the dummy fill and active features.

4. However, dummy fill can increase capacitance if it is placed too close to signal wires, which slows the transmission speed of signals and degrades the overall performance of the device. Dummy fill can also undesirably increase capacitance from interaction of elements across adjacent layers. While certain elements (such as signal lines and power lines) cannot be

easily moved without affecting circuit performance, there is substantially more flexibility regarding placement, positioning, and spacing of non-signal carrying features such as dummy fill, even when certain quantities of dummy fill are needed within layers and portions of layers to meet processing requirements.

5. Traditionally, the process flow for IC design is highly linear, with each phase of the design process depending on the previous steps. Accordingly, when revisions to portions of the physical design are made, as typically happens numerous times during the design process, all the subsequent steps typically need to be redone in their entirety for at least the layer, if not the entire device. This is because regardless of the size or extent of the revision to the physical design, the changes must be merged into a much larger integrated circuit design and then the remaining steps of the design process flow re-run.

6. The performance demands of modern integrated circuit devices have also resulted in much more complex layouts. The complexity of these layouts can result in errors that, if not caught early, can require restarting the layout process almost from scratch due to the interdependence of elements within and even across layers of the devices. This complexity, and the need to fix layout errors or otherwise perform revisions to the design, has also resulted in more changes to layouts that arise during the design process. These revisions, called engineering change orders or "ECOs" often require re-routing of wires during layout and/or revisions to dummy fill placement.

7. Bell Semic brings this action to put a stop to TI's unauthorized and unlicensed use of the inventions claimed in the Asserted Patents.

THE PARTIES

8. Plaintiff Bell Semic is a limited liability company organized under the laws of the State of Delaware with a place of business at One West Broad Street, Suite 901, Bethlehem, PA 18018.

9. Bell Semic stems from a long pedigree that began at Bell Labs. Bell Labs sprung out of the Bell System as a research and development laboratory, and eventually became known as one of America's greatest technology incubators. Bell Labs employees invented the transistor in 1947 in Murray Hill, New Jersey. It was widely considered one of the most important technological breakthroughs of the time, earning the inventors the Nobel Prize in Physics. Bell Labs made the first commercial transistors at a plant in Allentown, Pennsylvania. For decades, Bell Labs licensed its transistor patents to companies throughout the world, creating a technological boom that led to the use of transistors in the semiconductor devices prevalent in most electronic devices today.

10. Bell Semic, a successor to Bell Labs' pioneering efforts, owns over 1,900 worldwide patents and applications, approximately 1,500 of which are active United States patents. This patent portfolio of semiconductor–related inventions was developed over many years by some of the world's leading semiconductor companies, including Bell Labs, Lucent Technologies, Agere Systems, and LSI Logic and LSI Corporation ("LSI"). This portfolio reflects technology that underlies many important innovations in the development of semiconductors and integrated circuits for high–tech products, including smartphones, computers, wearables, digital signal processors, IoT devices, automobiles, broadband carrier access, switches, network processors, and wireless connectors.

11. The principals of Bell Semic all worked at Bell Labs' Allentown facility, and have continued the rich tradition of innovating, licensing, and helping the industry at large since

those early days at Bell Labs. For example, Bell Semic's CTO was a LSI Fellow and Broadcom Fellow. He is known throughout the world as an innovator with more than 300 patents to his name, and he has a sterling reputation for helping semiconductor fabs improve their efficiency. Bell Semic's CEO took a brief hiatus from the semiconductor world to work with Nortel Networks in the telecom industry during its bankruptcy. His efforts saved the pensions of tens of thousands of Nortel retirees and employees. In addition, several Bell Semic executives previously served as engineers at many of these companies and were personally involved in creating the ideas claimed throughout Bell Semic's extensive patent portfolio.

12. On information and belief, Defendant TI is a corporation organized and existing under the laws of Delaware, with its principal place of business at 12500 TI Boulevard, Dallas, Texas 75243. TI is registered with the State of Texas and may be served with process through its registered agent, CT Corporation System, 1999 Bryan Street, Suite 900, Dallas, TX 75201. On information and belief, TI has a regular and established place of business in this District, including at least 6412 US-75, Sherman, Texas 75090.

13. On information and belief, TI develops, designs, and/or manufactures products in the United States, including in this District, according to the Asserted Patents' patented processes/methodologies; and/or uses the Asserted Patents' patented processes/methodologies in the United States, including in this District, to make products; and/or distributes, markets, sells, or offers to sell in the United States and/or imports products into the United States, including in this District, that were manufactured or otherwise produced using the Asserted Patents' patented processes. Additionally, TI introduces those products into the stream of commerce knowing that they will be sold and/or used in this District and elsewhere in the United States.

JURISDICTION AND VENUE

14. This is an action for patent infringement arising under the Patent Laws of the United States, Title 35 of the United States Code. Accordingly, this Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

15. Defendant TI is subject to this Court's general personal jurisdiction at least because TI is a resident of Texas as defined by Texas law. On information and belief, TI is headquartered in Texas.

16. Defendant TI is additionally subject to this Court's general and specific personal jurisdiction because TI has sufficient minimum contacts within the State of Texas and this District, pursuant to due process and/or the Texas Long Arm Statute, Tex. Civ. Prac. & Rem. Code § 17.042. On information and belief, Defendant TI contracted with one or more Texas residents in this District and one or both parties performed the contract at least in part in the State of Texas and this District; TI committed the tort of patent infringement in State of Texas and this District; TI purposefully availed itself of the privileges of conducting business in the State of Texas and in this District; TI regularly conducts and solicits business within the State of Texas and within this District; TI recruits residents of the State of Texas and this District for employment inside or outside the State of Texas; Plaintiff's causes of action arise directly from TI's business contacts and other activities in the State of Texas and this District; and TI distributes, makes available, imports, sells and offers to sell products and services throughout the United States, including in this judicial District, and introduces infringing products and services that into the stream of commerce knowing that they would be used and sold in this judicial district and elsewhere in the United States.

17. This Court has specific personal jurisdiction over TI pursuant to due process and/or the Texas Long Arm Statute, at least in part, because (i) TI has conducted and continue to

conduct business in this District and (ii) Bell Semic's causes of action arise, at least in part, from TI's contacts with and activities in the State of Texas and this District. Upon information and belief, TI has committed acts of infringement within the State of Texas and this District by, *inter alia*, directly using, testing, selling, offering to sell, or importing products that infringe one or more claims of each of the Asserted Patents in this District and/or importing Accused Products, including but not limited to the Exemplary Accused Products, into this District, and/or committing at least a portion of any other infringements alleged herein. In the State of Texas and in this District, TI, directly: (i) performs at least a portion of the infringements alleged herein; (ii) develops, designs, and/or manufactures products according to each of the Asserted Patents' patented processes/methodologies; (iii) distributes, markets, sells, or offers to sell products formed according to each of the Asserted Patents' patented processes/methodologies; and/or (iv) imports products formed according to the Asserted Patents' patented processes/methodologies.

18. On information and belief, venue is proper in this Court pursuant to 28 U.S.C. §§ 1391 and 1400 because TI has committed, and continues to commit, acts of infringement in this District and has a regular and established place of business in this District. For example, on information and belief, TI has a regular and established place of business in this District, including at least at 6412 US-75, Sherman, TX 75090. On information and belief, TI's acts of infringement have taken place within this District. On information and belief, TI's presence in this District is substantial, including at least at 6412 US-75, Sherman, TX 75090. TI's presence in this District includes an 80,000 square foot, 150 mm fabrication facility that produces over 4,500 device types, including at least semiconductors for use in multiple automotive, commercial, military, and space applications.

19. Additionally, TI—directly or through intermediaries (including distributors, retailers, and others), subsidiaries, alter egos, and/or agents—ships, distributes, offers for sale, and/or sells its products and services in the United States and this District. TI has purposefully and voluntarily placed one or more of its products into the stream of commerce through the accused instrumentalities that infringe the patents asserted in this action with the awareness and/or intent that they will be purchased by consumers in this District. TI knowingly and purposefully ships infringing products into, and within, this District. These infringing products have been, and continue to be, purchased by consumers and businesses in this District.Currently, on information and belief, TI is seeking more than 43 engineers in the Richardson [[TI Job listings for designers]]

20. Venue is also convenient in this District. This is at least true because of this District's close ties to this case—including the technology, relevant witnesses, and sources of proof noted above—and its ability to quickly and efficiently move this case to resolution.

21. On information and belief, Bell Semic's cause of action arises directly from TI's circuit design work and other activities in this District. Moreover, on information and belief, TI has derived substantial revenues from its infringing acts occurring within the State of Texas and within this District.

U.S. PATENT NO. 7,007,259

22. Bell Semic is the owner by assignment of the '259 patent. The '259 patent is titled "Method for Providing Clock-Net Aware Dummy Metal Using Dummy Regions." The '259 patent issued on February 28, 2006. A true and correct copy of the '259 patent is attached as Exhibit A.

23. The inventors of the '259 patent are Vikram Shrowty and Santhanakrishnan Raman ("the '259 Inventors").

24. The application that resulted in the issuance of the ’259 patent was filed on July 31, 2003. The ’259 patent claims priority to July 31, 2003.

25. The ’259 patent generally relates to “methods for patterning dummy metal to achieve planarity for chemical-mechanical polishing of integrated circuits, and more particularly to a dummy fill software tool that provides clock-net aware dummy metal using dummy regions.” Ex. A at 1:7–11.

26. Prior to the development of the methodology described in the ’259 patent, the most widely implemented technology for insertion of dummy metal into a circuit design required hardcoding a large “stay-away” distance between the dummy metal and clock nets, which led to less space available for dummy metal insertion. This methodology often made it impossible to insert enough dummy metal to meet the required minimum density. The traditional dummy fill tools would often complete their run without reaching the minimum density, thus requiring at least a second run of the tool for the problem areas. In each problem area, the “stay-away” distance was reduced manually. And if there was more than one problem area, the manufacturer would have to make multiple runs of the tool, as it would have to address one problem area at a time. This was an involved, iterative process that had the potential to negatively impact the fabrication schedule and potentially the yield of the run, causing costs to go up.

27. The background section of the ’259 patent identifies the shortcomings of the prior art. More specifically, the specification describes that the prior circuit design methodology was disadvantageous because it was “often impossible to insert enough dummy metal into a tile to meet the required minimum density without reducing the large dummy-to-clock distance.” Ex. A at 2:3–10. Use of this design process meant that a second run of the metal-fill tool was often required in order to meet the density requirements for all of the tiles. *Id.* at 2:10–14. Having to

rerun the tool to meet the density requirements made the design process an "involved, iterative process[,]" which could "significantly impact the design schedule." *Id.* at 2:14–18.

28. The '259 Inventors understood the drawbacks of this "stay-away" design process and set out to develop a more efficient method for inserting dummy metal into a circuit design. The Inventors ultimately conceived of a dummy fill procedure that minimizes the negative timing impact of dummy metal on clock nets, while still achieving minimum density in a single run. The claimed invention begins by identifying free spaces on each layer of the circuit design suitable for dummy metal insertion as dummy regions. The dummy regions are then prioritized such that the dummy regions located adjacent to clock nets are filled with dummy metal last, thereby minimizing any timing impact on the clock nets.

29. In light of the drawbacks of the prior art, the Inventors recognized the need to "minimize[] the negative timing impact of dummy metal on clock nets, while at the same time achieving minimum density in a single run." Ex. A at 2:19–23. The inventions claimed in the '259 patent addresses this need.

30. The inventions disclosed in the '259 patent provide many advantages over the prior art. In particular, they provide a simple and efficient method for dummy metal insertion that minimizes the timing impact to clock nets and at the same time guarantees reaching minimum density in a single pass. *See* Ex. A at 6:11–15. As mentioned above, the patented invention results in the dummy regions being prioritized such that the dummy regions located adjacent to clock nets are filled with dummy metal last, thereby minimizing the timing impact on the clock nets. *See* Ex. A at 2:29–47. Additionally, some embodiments of the patented invention further prioritize the dummy regions such that the dummy regions adjacent to wider clock nets are filled with dummy metal after dummy regions that are located adjacent to narrower clock

nets. *See* Ex. A at 2:35–39. These significant advantages are achieved through the use of the patented inventions and thus the ’259 patent presents significant commercial value for companies like TI.

31. The ’259 patent contains three independent claims and 37 total claims, covering a method and computer readable medium for circuit design. Claim 1 reads:

> 1. A method for inserting dummy metal into a circuit design, the circuit design including a plurality of objects and clock nets, the method comprising:
>
> (a) identifying free spaces on each layer of the circuit design suitable for dummy metal insertion as dummy regions, and
>
> (b) prioritizing the dummy regions such that the dummy regions located adjacent to clock nets are filled with dummy metal last, thereby minimizing any timing impact on the clock nets.

32. This claim, as a whole, provides significant benefits and improvements to the function of the semiconductor device, *e.g.*, minimizing the negative timing impact of dummy metal on clock nets while also reducing the opportunity for dishing and erosion that could result in inaccurate transfer of patterns during lithography, suboptimal layouts/designs, inaccurate timing, reduced signal integrity, crosstalk delay, noise issues, increased probability of failure, and ultimately defective or underperforming devices. *See, e.g.*, Ex. A at 6:11–15.

33. The claims of the ’259 patent also recite inventive concepts that improve the functioning of the fabrication process, particularly as to dummy filling. The claims of the ’259 patent disclose a new and novel solution to specific problems related to improving semiconductor fabrication. As explained in detail above and in the ’259 patent specification, the claimed inventions improve upon the prior art processes by prioritizing dummy regions such that the dummy regions located adjacent to clock nets are filled with dummy metal last. This has the advantage of reducing the impact of dummy metal on signal and clock lines and increasing the

efficiency, yield, and design/layout miniaturization and flexibility of the manufacturing process. The claimed inventive processes also increase performance and signal integrity, while reducing crosstalk delay, noise issues, probability of failure, and defective and/or underperforming devices.

U.S. PATENT NO. 6,436,807

34. Bell Semic is the owner by assignment of the ’807 patent. The ’807 patent is titled “Method for Making an Interconnect Layer and a Semiconductor Device Including the Same.” The ’807 patent issued on August 20, 2002. A true and correct copy of the ’807 patent is attached as Exhibit B.

35. The inventors of the ’807 patent are Donald Cwynar, Sudhanshu Misra, Dennis Ouma, Vivek Saxena, and John Sharpe (“the ’807 Inventors”).

36. The application that resulted in the issuance of the ’807 patent was filed on January 18, 2000. The ’807 patent claims priority to January 18, 2000.

37. The ’807 patent generally relates to “a method for making a layout for an interconnect layer that has uniform density throughout to facilitate planarization during manufacturing of a semiconductor device.” Ex. B at 2:43–46.

38. The background section of the ’807 patent identifies the shortcomings of the prior art. More specifically, the specification describes that the prior circuit design methodology was disadvantageous because it could lead to “protrusions[] in the upper surface of the dielectric material[] above respective active interconnect features[.]” *Id.* at 1:40–42. The specification states that “if pattern density variations of the active interconnect features[] are large, CMP is not adequate to sufficiently planarize the interconnect layer[.]” *Id.* at 1:67–2:2. Although “[c]onventional layout algorithms” were typically used to place dummy fill features in open areas of the interconnect layer, those algorithms placed dummy metal “based upon a

predetermined set density." *Id.* at 2:17–21. Relying on "predetermined set densit[ies]" could lead to the unnecessary placement of dummy fill features, which in turn could increase the parasitic capacitance of the interconnect layer. *Id.* at 2:31–33. The specification notes that "variations in the density of the interconnect layer [could] cause deviations when the interconnect layer [was] planarized." *Id.* at 2:35–37.

39. Prior to development of the methodology described in the '807 patent, the placement of dummy fill in the open areas of the interconnect layer was performed based upon a predetermined set density. However, use of predetermined set densities was not ideal because it often resulted in unnecessary placement of dummy fill and increased capacitance. For example, if the density of an active interconnect feature was high in relation to an adjacent open area, then it would not be necessary to place dummy fill in the corresponding open area at the predetermined density.

40. In light of the drawbacks of the prior art as well as the importance of having a flat or planarized surface on each layer of the devices, the '807 Inventors recognized "a need for making a layout for an interconnect layer that determines placement of dummy fill features for achieving a uniform density throughout the interconnect layer." Ex. B at 2:37–40. The'807 Inventors set out to develop a design process that would achieve uniform density throughout the interconnect layer.

41. The inventions claimed in the '807 patent address this need. The '807 Inventors ultimately conceived of a method for making the layout for an interconnect layout that allows for uniform density throughout the layer and facilitates planarization during manufacturing of the device. The claimed invention begins by determining an active interconnect feature density for each of a plurality of layout regions of the interconnect layout. Dummy fill is then added to each

layout region in order to obtain a desired density of active interconnect features and dummy fill features in order to facilitate uniformity of planarization. In order to add dummy fill in this manner, one must define a minimum dummy fill feature lateral dimension based upon a dielectric layer deposition bias for a dielectric layer to be deposited over the interconnect layer.

42. The inventions disclosed in the ’807 patent provide many advantages over the prior art. In particular, having a uniform density for each layout region facilitates uniformity of planarization during manufacturing of the semiconductor device. *See* Ex. B at 3:3–5, 5:9–12. Furthermore, adding dummy fill features to obtain a desired density of active interconnect features and dummy fill features also helps ensure that dummy fill features are not unnecessarily added. Id. at 2:63–67, 5:19–22. Avoiding unnecessary dummy fill features is desirable because it deceases the parasitic capacitance of the interconnect layer. *Id.* at 2:67–3:2, 5:22–24. The inventions claimed in the ’807 patent also provides for the selective positioning of dummy fill features, which minimizes parasitic capacitance. *Id.* at 5:28–33. These significant advantages are achieved through the use of the patented inventions and thus the ’807 patent presents significant commercial value for companies like TI.

43. The ’807 patent contains two independent claims and 18 total claims. Claim 1 reads:

> 1. A method for making a layout for an interconnect layer of a semiconductor device to facilitate uniformity of planarization during manufacture of the semiconductor device, the method comprising the steps of:
>
> (a) determining an active interconnect feature density for each of a plurality of layout regions of the interconnect layout; and
>
> (b) adding dummy fill features to each layout region to obtain a desired density of active interconnect features and dummy fill features to facilitate uniformity of planarization during manufacturing of the semiconductor device, the adding comprising defining a minimum dummy fill feature lateral dimension based upon a dielectric layer

> deposition bias for a dielectric layer to be deposited over the interconnect layer.

44. This claim, as a whole, provides significant benefits and improvements to the function of the semiconductor device, *e.g.,* uniform planarization during manufacturing, avoidance of adding unnecessary dummy fill features, and minimizing parasitic capacitance. *See, e.g.*, Ex. B at 5:9–34.

45. The claims of the ’807 patent also recite inventive concepts that improve the functioning of the fabrication process, particularly as to dummy filling. The claims of the ’807 patent disclose a new and novel solution to specific problems related to improving semiconductor fabrication. As explained in detail above and in the ’807 patent specification, the claimed inventions improve upon the prior art processes by determining an active interconnect feature density for each of a plurality of layout regions of the interconnect layout and adding dummy fill to each layout region to obtain a desired density of active interconnect features and dummy fill features to facilitate uniformity of planarization. This has advantages such as avoiding the unnecessary adding of dummy fill features and minimizing the parasitic capacitance of the interconnect layer.

U.S. PATENT NO. 7,260,803

46. Bell Semic is the owner by assignment of the ’803 patent. The ’803 patent is titled “Incremental Dummy Metal Insertions.” The ’803 patent issued on August 21, 2007. A true and correct copy of the ’803 patent is attached as Exhibit C.

47. The inventors of the ’803 patent are Viswanathan Lakshmanan, Richard Blinne, Vikram Shrowty, and Lena Montecillo (“the ’803 Inventors”).

48. The application that resulted in the issuance of the ’803 patent was filed on October 10, 2003. The ’803 patent claims priority to October 10, 2003.

49. The ’803 patent generally relates to “a method for performing dummy metal insertion that avoids having to rerun the dummy fill software tool after the integrated circuit design is changed.” Ex. C at 1:6–10.

50. Prior to development of the methodology described in the ’803 patent, if a designer requested even a small change to a semiconductor device, the dummy fill pattern must be thrown out. This is problematic because it can take up to 30 hours to run the dummy fill tool to create the dummy fill pattern. By starting over, the entire device design layout could be delayed by 30 hours or more. This issue is exacerbated with every subsequent change that again causes the dummy fill process to begin again from scratch. Such an iterative, time-consuming process negatively impacts the fabrication schedule and causes costs to go up.

51. The ’803 patent identifies the shortcomings of the prior art. More specifically, the specification describes that the prior dummy fill methodologies were disadvantageous because, when a customer requests a change, “the results of the dummy fill tool are thrown out, and the dummy fill tool is rerun in order to ensure that no dummy metal intersects with any of the design objects.” Ex. C at 1:51–59. Unfortunately, this “may delay completion of the design by another 30 hours” and may “significantly impact the design schedule and result in cost overruns. *Id.* at 1:60–65. This is especially true when multiple changes are requested.

52. The ’803 Inventors understood the drawbacks of this process and set out to develop a more efficient method for inserting dummy metal into a circuit design after portion(s) of it have changed. In light of the drawbacks of the prior art, the ’803 Inventors recognized the need to “insert[] dummy metal into an integrated circuit design after an ECO [Engineering Change Order] without requiring reruns of the dummy fill tool.” Ex. C at 1:66–2:1. The inventions claimed in the ’803 patent address this need.

53. The ’803 Inventors ultimately conceived of a dummy fill insertion procedure that did not require having to rerun the dummy fill tool whenever any change was made to the layout. The claimed invention, after a portion of the design data has changed, first performs a check to determining whether any dummy metal objects intersect with any other objects in the design data. Then any intersecting dummy metal objects are deleted from the design data, thereby avoiding having to rerun the dummy fill tool. This design process “saves time on overall design execution” and helps manufacturers “meet aggressive design schedules.” Ex. C at 2:15–22, 4:52–57.

54. The inventions disclosed in the ’803 patent provide many advantages over the prior art. In particular, they provide a simple and efficient method for ensuring dummy metal does not intersect other components such that the dummy fill tool does not have to be rerun. *See* Ex. C at 2:6–22. As mentioned above, this is very beneficial as it substantially reduces the run time of the dummy fill tool, shortens the overall design timeline, and avoids cost overruns and delays, making it less costly to make changes later in the design process. *See id.* at 1:51–65. Given the aforementioned increased complexity of circuit designs and the corresponding delays from ECOs and layout changes, these efficiency gains have become more and more important in completing the design process without affecting time-to-market. These significant advantages are achieved through the use of the patented inventions and thus the ’803 patent presents significant commercial value for companies like TI.

55. The ’803 patent contains two independent claims and 22 total claims, covering a method and computer readable medium for performing dummy metal insertion. Claim 1 reads:

> 1. A method for performing dummy metal insertion in design data for an integrated circuit, which includes dummy metal objects inserted by a dummy fill tool, comprising:

> (a) after a portion of the design data is changed, performing a check to determine whether any dummy metal objects intersect with any other objects in the design data; and
>
> (b) deleting the intersecting dummy metal objects from the design data, thereby avoiding having to rerun the dummy fill tool.

56. This claim, as a whole, provides significant benefits and improvements to the function of the semiconductor device, *e.g.*, minimizing the potential for design-based short circuits, increasing the efficiency of the design process, and ensuring that devices meet their minimum density requirements, which reduces the probability of short circuits or other defects that render devices inoperable. *See, e.g.*, Ex. C at 1:24–42.

57. The claims of the ’803 patent also recite inventive concepts that improve the functioning of the fabrication process, particularly dummy fill processes. The claims of the ’803 patent disclose a new and novel solution to specific problems related to rerunning dummy fill tools after a change order is received. As explained in detail above and in the ’803 patent specification, the claimed inventions improve upon the prior art processes by deleting dummy metal objects if a change order results in dummy metal objects that intersect with other objects in the design data. This has the advantage of maintaining minimum metal density without having to rerun the dummy fill tool, and results in substantially reducing the time needed to finalize a circuit design due to the ability to make late-stage ECOs and incremental changes in layout without needing to re-run the dummy fill tool for the entire layer.

U.S. PATENT NO. 7,149,989

58. Bell Semic is the owner by assignment of the ’989 patent. The ’989 patent is titled “Method of Early Physical Design Validation and Identification of Texted Metal Short Circuits in an Integrated Circuit Design.” The ’989 patent issued on December 12, 2006. A true and correct copy of the ’989 patent is attached as Exhibit D.

59. The inventors of the ’989 patent are Viswanathan Lakshmanan, Alan Holesovsky, Lisa Miller, and Jonathan Kuppinger (“the ’989 Inventors”).

60. The application that resulted in the issuance of the ’989 patent was filed on September 22, 2004. The ’989 patent claims priority to September 22, 2004.

61. The ’989 patent generally relates to “methods of verifying an integrated circuit design to ensure adherence to process rules and overall manufacturability of the integrated circuit design for a specific technology.” Ex. D at 1:10–15.

62. The ’989 patent addresses another way to minimize short circuits and malfunctioning devices. When creating a semiconductor device, designers typically create layout designs that contain the topological information used to identify structures within several layers of the semiconductor device. These layout designs are ultimately used as blueprints to create the physical semiconductor device. Prior to development of the methodology described in the ’989 patent, the designs would be validated at the very end of the design cycle, when all components have been placed and routed. However, if the validation process detects a design fault, like a short circuit, at the very end of the design cycle, then the timing of the entire integrated circuit design may have to be reset. In some cases, the design may have to be re-floorplanned and the entire design cycle may have to be reiterated, causing delays on of several weeks or months, depending on the overall complexity of the design and the process node. Similarly, it is not possible to simply run the validation check early in the process to avoid this issue. Doing so would cause the validation process to incorrectly identify a large number of errors because the circuit design is incomplete in early stages.

63. The ’989 patent identifies the shortcomings of the prior art. More specifically, the specification describes that the prior validation methodology was disadvantageous because “a

design fault detected so late might reset the time schedule for the entire integrated circuit design." Ex. D at 2:42–44. In some cases, this means the "design may have to be re-floorplanned, and the entire design cycle may have to be reiterated." *Id.* at 2:44–46. Existing early design validation processes resulted in "substantial amount[s] of computer processing time that would severely impact the product turnaround time." *Id.* at 2:50–54. In addition, it would "falsely report" a large number of design errors "due to the incomplete circuit design, making it difficult to sort out the design errors that need to be corrected before the circuit design is completed." *Id.* at 2:54–58.

64. In light of the drawbacks of the prior art, the Inventors recognized the need to "provide[] design rules that may be used in conjunction with a design rule check tool and/or a layout vs. schematic tool in an early stage of the physical design to detect design rule violations in floorplanning, including input/output cell placement and construction and power distribution and power map structure." Ex. D at 2:64–3:3. Moreover, "texted metal short circuits may be identified most advantageously in the early or evolutionary aspects of the design flow," which reduc[es] the computer processing time required to validate an integrated circuit design," such as once layout design is complete. *Id.* at 3:3–11. The inventions claimed in the '989 patent address this need.

65. The '989 Inventors understood the drawbacks of both late-stage and early-stage validation processes and decided to create something better. The '989 Inventors ultimately conceived of a validation procedure that specifies validation checks on certain physical design rules that are specific to texted metal short circuits between different signal sources in addition to power and ground. The claimed invention receives a representation of an integrated circuit design and a physical design rule deck that specifies rule checks to be performed on the

integrated circuit design. The claimed invention generates a specific rule deck from the physical design rule deck, where the specific rule deck is a subset that includes only physical design rules that are specific to texted metal short circuits between different signal sources in addition to power and ground in the integrated circuit design. A physical design validation is performed on the integrated circuit design from the specific rule deck to identify texted metal short circuits between different signal sources in addition to power and ground in the integrated circuit design.

66. The inventions disclosed in the ’989 patent provide many advantages over the prior art. In particular, they provide the ability to perform an early validation process that does not falsely identify a number of unfounded errors in the early stage of the design. *See* Ex. D at 2:47–58. For instance, in early stages, the patented processes can identify texted metal shorts, violations in floorplanning, and errors in power map structure. *See id.* at 2:64–3:7. Early defect detection saves computer processing time, avoids severe voltage droop, and allows for correction in early stages, each of which would otherwise result in costly schedule delays and unacceptable turnaround time. *See id.* at 3:7–20. Moreover, this allows high-level power and signal-routing such that individual blocks with defined pins can be finalized by the responsible members of design team in parallel, at substantial decrease in design time and overall gains in efficiency. These significant advantages are achieved through the use of the patented inventions and thus the ’989 patent presents significant commercial value for companies like TI.

67. The ’989 patent contains two independent claims and 12 total claims, covering a method and computer program product. Claim 1 reads:

> 1. A method comprising the steps of:
>
> (a) receiving as input a representation of an integrated circuit design;
>
> (b) receiving as input a physical design rule deck that specifies rule checks to be performed on the integrated circuit design;

> (c) generating a specific rule deck from the physical design rule deck wherein the specific rule deck includes only physical design rules that are specific to texted metal short circuits between different signal sources in addition to power and ground in the integrated circuit design; and
>
> (d) performing a physical design validation on the integrated circuit design from the specific rule deck to identify texted metal short circuits between different signal sources in addition to power and ground in the integrated circuit design.

68. This claim, as a whole, provides significant benefits and improvements to the function of the semiconductor device, *e.g.*, minimizing the potential for design-based short circuits, ensuring overall manufacturability of devices, reducing probability of failure, and ultimately lessening the likelihood of defective devices. *See, e.g.*, Ex. D at 1:11–15, 3:3–19.

69. The claims of the ’989 patent also recite inventive concepts that improve the functioning of the fabrication process, particularly validation processes. The claims of the ’989 patent disclose a new and novel solution to specific problems related to end-stage validation. As explained in detail above and in the ’989 patent specification, the claimed inventions improve upon the prior art processes by performing early-stage validation on texted metal short circuits. This has the advantage of ensuring manufacturability of devices, lessening the likelihood of short circuits and other defects, as well as substantially reducing the time needed to finalize a circuit design. This allows high-level power and signal-routing such that individual blocks with defined pins can be finalized by the responsible members of design team in parallel, at substantial decrease in design time and overall gains in efficiency.

U.S. PATENT NO. 7,231,626

70. Bell Semiconductor owns by assignment the entire right, title, and interest in the ’626 patent, entitled “Method Of Implementing An Engineering Change Order In An Integrated Circuit Design By Windows.”

71. A true and correct copy of the ’626 patent is attached as Exhibit E.

72. The ’626 patent issued to inventors Jason K. Hoff, Viswanathan Lakshmanan, Michael Josephides, Daniel W. Prevedel, Richard D. Blinne, and Johathan P. Kuppinger (“the ’626 Inventors”).

73. The application that resulted in issuance of the’626 patent, United States Patent Application No. 11/015,123, was filed December 17, 2004. It issued on June 12, 2007 and expires on July 26, 2025.

74. The ’626 patent generally relates to “methods of implementing an engineering change order (ECO) in an integrated circuit design.” Ex. E at 1:1–13.

75. Before the inventions claimed in the ’626 patent, the typical turnaround time for implementing a change to the physical design for cutting edge devices was approximately one week regardless of the size of the change. This is extremely inefficient in most instances where the change relates to only a small fraction of the overall design. *See* Ex. E at 3:16–18 & Fig. 1.

76. The background section of the ’626 patent identifies the shortcomings of the prior art. More specifically, the specification describes that the prior circuit design methodology was disadvantageous because “[i]n previous methods for implementing an engineering change order (ECO) request in an integrated circuit design, design tools are run for the entire integrated circuit design, even though the engineering change order typically is only a small fraction of the size of the integrated circuit design” Ex. E at 2:15–19.

77. The ’626 patent elaborates that because “cell placement, routing, design rule check validation, and timing closure run times typically scale with the size of the entire integrated circuit design,” Ex. E at 2:20–22, this produced a “typical turnaround time” of “about one week regardless of the size of the engineering change order. . . . because although the

engineering change order may only have a size of a few cells, it must be merged with an integrated circuit design that typically has a much greater size." *Id.* at 2:37–44. Certain of these steps "may be especially time consuming and resource intensive." *Id.* at 3:16–17.

78. The '626 patent's inventors solved this problem by defining a window that encloses a change specified by the revision to physical design. The window defines an area that is less than the area of the entire circuit design. Only the nets within that window are routed pursuant to the revision, leaving the remaining nets in the design unaffected. Then, the results of that incremental routing are inserted into a copy of the original IC design to produce a revised IC design that effects the physical design change without needing to redo the entire process flow.

79. The inventions disclosed in the '626 patent provide many advantages over the prior art. In particular, they provide a simple and efficient method for ensuring that revisions to the physical design of the IC do not unduly delay the completion of the design process. As the '626 patent explains, "significant savings in the resources required to perform routing, design rule check verification, net delay calculation, and parasitic extraction may be realized by creating windows in the integrated circuit design that include only the incremental changes to the overall integrated circuit design." Ex. E at 3:19–23.

80. As mentioned above, this is very beneficial because it substantially reduces the run time of the routing tools and related follow-on steps of the layout portion of the design process flow (such as calculation of net delay, design rule check, and parasitic extraction). Thus, it shortens the overall design timeline, and avoids cost overruns and delays, making it less costly to make changes later in the design process or more often. *See id.*

81. Given the aforementioned increased complexity of circuit designs and the corresponding delays from design changes, these efficiency gains have become more and more

important in completing the design process without affecting time-to-market. These significant advantages are achieved through the use of the patented inventions and thus the ’626 patent presents significant commercial value for chip designers.

82. In light of the drawbacks of the prior art, the ’626 patent’s inventors recognized the need for a circuit design methodology in which the time required to implement an ECO “depend[s] on the number of net changes in the [ECO] rather than on the total number of nets in the entire integrated circuit design.” Ex. E at 2:51–53. The inventions claimed in the’626 patent address this need.

83. The ’626 patent contains two independent claims and 8 total claims, covering a method and computer readable medium for implementing a change order in an integrated circuit design. Claim 1 reads:

> 1. A method comprising steps of:
>
> > (a) receiving as input an integrated circuit design;
> >
> > (b) receiving as input an engineering change order to the integrated circuit design;
> >
> > (c) creating at least one window in the integrated circuit design that encloses a change to the integrated circuit design introduced by the engineering change order wherein the window is bounded by coordinates that define an area that is less than an entire area of the integrated circuit design;
> >
> > (d) performing an incremental routing of the integrated circuit design only for each net in the integrated circuit design that is enclosed by the window;
> >
> > (e) replacing an area in a copy of the integrated circuit design that is bounded by the coordinates of the window with results of the incremental routing to generate a revised integrated circuit design; and
> >
> > (f) generating as output the revised integrated circuit design.

84. This claim, as a whole, provides significant benefits and improvements to the function of the semiconductor device design process, *e.g.*, providing a novel and substantially more efficient process flow in which only the affected nets would be considered in the incremental routing. This results in substantial reduction in the expected time of the design portion of producing semiconductor devices.

85. The claims of the ’626 patent also recite inventive concepts that improve the functioning of the fabrication process, particularly as to post-ECO routing. The claims of the ’626 patent disclose a new and novel solution to specific problems related to improving semiconductor fabrication. As explained in detail above and in the ’626 patent specification, the claimed inventions improve upon the prior art processes by ignoring nets that are unaffected by an ECO in performing routing following the ECO. This has the advantage of substantially reducing the impact on design schedule of ECOs and other layout changes, thus increasing the efficiency of the design process and making it easier to improve the design and fix design errors without unduly delaying time-to-market. By making it easier to fix errors as they are found, and causing substantially less incremental delay upon finding and fixing errors, the claimed inventive processes also increase the performance and reliability of the finished product. Because of the claimed inventive processes, individual less impactful design issues that still impact design performance (albeit not on a critical scale) can be caught and fixed without costing the same delay as more substantial errors.

U.S. PATENT NO. 7,396,760

86. Bell Semic is the owner by assignment of the ’760 patent. The ’760 patent is titled “Method and System for Reducing Inter-Layer Capacitance in Integrated Circuits.”

87. A true and correct copy of the ’760 patent is attached as Exhibit F.

88. The inventors of the ’760 patent are Kunal Taravade, Neal Callan, and Paul Filseth (“the ’760 Inventors”).

89. The ’760 patent issued on July 8, 2008 from an application filed on November 17, 2004.

90. The ’760 patent generally relates to “a method for reducing inter-layer capacitance” in integrated circuits “through dummy fill methodology.” Ex. F at 1:8–10.

91. Prior to development of the methodology described in the ’760 patent, the placement of dummy fill in the open areas of the interconnect layer was performed based primarily upon meeting density requirements. To the extent that timing and capacitance effects were considered in dummy fill dimensions, orientation, positioning, or otherwise in dummy fill placement, the conventional dummy fill tools at the time only considered intralayer effects—i.e., interactions between dummy fill features and other elements (such as signal nets) on that same layer. However, use of dummy fill that overlapped on successive layers could and often did create a substantial interlayer bulk capacitive effect that had a negative impact on circuit timing and performance, and which was not considered by the conventional dummy fill tools at the time even when they considered certain intralayer timing effects. *See* Ex. F at 1:43–2:6, 4:11–16.

92. The background section of the ’760 patent identifies the shortcomings of the prior art. More specifically, the specification describes that the prior dummy fill methodologies were disadvantageous because they typically focused on achieving uniformity of feature density and failed to sufficiently address adverse effects of the dummy fill on electric field and unwanted bulk capacitance. *See* Ex. F at 1:62–66. In addition, these dummy fill methodologies only considered intralayer effects of dummy fill, to the extent that they considered timing impact at all. *See* Ex. F at 1:66–2:3. Thus, placement of dummy fill, even if advantageous on each

individual layer, could create problems when it overlapped with dummy fill features on successive layers, introducing an additional bulk capacitance component that could be substantial. *See id.* at 4:11–17, 4:25–28. These methodologies failed to consider interlayer effects such as those caused by the overlap of dummy fill features in successive layers, which could have a substantial negative impact on timing. *See id.* at 2:3–6.

93. Recognizing these drawbacks, as well as the importance of having a flat or planarized surface on the devices, the inventors of the ’760 patent set out to develop a design process that would also consider the interlayer bulk capacitance created by overlapping dummy fill and consider those intralayer effects in arranging dummy fill in the chip layout so as to minimize the unwanted bulk capacitance created by overlapping dummy fill features.

94. In light of the drawbacks of the prior art, the inventors of the ’760 patent recognized a need for “intelligent dummy fill placement to reduce interlayer capacitance caused by overlaps of dummy fill area on successive layers,” which would also “treat[] each consecutive pair of layers together when the intelligent dummy filling placement is performed.” Ex. F at 2:7–13. The inventions claimed in the ’760 patent address this need.

95. The inventors of the ’760 patent ultimately conceived of a method for addressing the interlayer capacitive effects of dummy fill by treating each successive set of layers as a pair and then rearranging the dummy fill in one or both layers so as to minimize their overlap. This was particularly advantageous in “intelligent dummy fill placement,” i.e., when timing impact is considered when placing dummy fill. *See* Ex. F at 2:10–19.

96. The inventions disclosed in the ’760 patent provide many advantages over the prior art. In particular, rearranging the dummy fill features such that they do not align vertically in successive layers can reduce unwanted bulk capacitance introduced by dummy fill and thus

minimize the interlayer capacitance. *See* Ex. F at 2:45–48, 2:47–59, 3:30–33, 5:19–39. This removed unwanted bulk capacitance that would otherwise slow down signals in the circuit and adversely affect timing in the IC, thus improving its speed and performance. *See id.* at 2:3–6. These significant advantages are achieved through the use of the patented inventions and thus the ’760 patent presents significant commercial value for companies like TI.

97. The ’760 patent contains two independent claims and 19 total claims. Claim 1 reads:

> 1. A method for placing dummy fill patterns in an integrated circuit fabrication process, comprising:
>
> > obtaining layout information of the integrated circuit, the integrated circuit including a plurality of layers;
> >
> > obtaining a first dummy fill space for a first layer based on the layout information;
> >
> > obtaining a second dummy fill space for a second layer, the second layer being placed successively to the first layer;
> >
> > determining an overlap between the first dummy fill space and the second dummy fill space; and
> >
> > minimizing the overlap by re-arranging a plurality of first dummy fill features and a plurality of second dummy fill features,
> >
> > wherein the first dummy fill space includes non-signal carrying lines on the first layer and the second dummy fill space includes non-signal carrying lines on the second layer.

98. This claim, as a whole, provides significant benefits and improvements to the function of the semiconductor device, *e.g.*, minimizing interlayer bulk capacitance and thus improving the timing characteristics and performance of the IC while meeting interconnect density requirements during processing. *See, e.g.*, Ex. F at 1:37–55, 5:19–39.

99. The claims of the ’760 patent also recite inventive concepts that improve the functioning of the fabrication process, particularly as to dummy filling. The claims of the ’760

patent disclose a new and novel solution to specific problems related to improving semiconductor fabrication. As explained in detail above and in the ’760 patent specification, the claimed inventions improve upon the prior art processes by considering successive layers rather than each layer on its own, and then determining the overlap between dummy fill features on successive layers before rearranging them to minimize their overlap and thus reduce interlayer bulk capacitance. This has advantages such as minimizing the parasitic capacitance of the interconnect layers, especially the bulk capacitance contributed by the interlayer effects of overlapping dummy fill features, while maintaining necessary interconnect density to meet fabrication requirements.

COUNT I – INFRINGEMENT OF U.S. PATENT NO. 7,007,259

100. Bell Semic re-alleges and incorporates by reference the allegations of the foregoing paragraphs as if fully set forth herein.

101. The ’259 patent is valid and enforceable under the United States Patent Laws.

102. Bell Semic owns, by assignment, all right, title, and interest in and to the ’259 patent, including the right to collect for past damages.

103. On information and belief, TI has and continues to directly infringe pursuant to 35 U.S.C. § 271(a) one or more claims of the ’259 patent by using the patented methodology to design one or more semiconductor devices, including, by way of example, the Exemplary Accused Products, in the United States.

104. On information and belief, TI employs a variety of design tools, for example, Cadence, Synopsys, and/or Siemens tools, to insert dummy metal into a circuit design (the "’259 Accused Processes") as recited in the ’259 patent claims. As one example, TI’s ’259 Accused Processes perform a method for inserting dummy metal into a circuit design, where the circuit design includes a plurality of objects and clock nets as required by claim 1 of the ’259 patent. TI

does so by employing a design tool, such as at least one of a Cadence, Synopsys, and/or Siemens tool, to insert dummy metal into a circuit design for each of its Accused Products. The design of each Accused Product includes a plurality of objects, such as cells, interconnects, signal nets, and clock nets.

105. TI's '259 Accused Processes also identify free spaces on each layer of the circuit design suitable for dummy metal insertion as dummy regions. TI does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, to identify free spaces on each layer of the circuit designs for each of its Accused Products suitable for dummy metal insertion as dummy regions.

106. TI's '259 Accused Processes also prioritize the dummy regions such that the dummy regions located adjacent to clock nets are filled with dummy metal last, thereby minimizing any timing impact on the clock nets. TI does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, to prioritize dummy regions such that those adjacent to clock nets are filled with dummy metal last. For example, the '259 Accused Processes assign a "high cost" to adding metal fill near the clock nets and "lower cost" to adding metal fill near signal, power, and ground nets. Assigning "cost" in this way fills dummy regions adjacent to clock nets last and minimizes any timing impact on the clock nets. An exemplary infringement analysis showing infringement of one or more claims of the '259 patent by the TI 66AK2H12 Exemplary Accused Product is set forth in Exhibit G. The declaration of Lloyd Linder, an expert in the field of semiconductor device design, is attached at Exhibit M and further describes TI's infringement of the '259 patent.

107. TI's '259 Accused Processes infringe and continue to infringe one or more claims of the '259 patent during the pendency of the '259 patent.

108. On information and belief, TI has and continues to infringe pursuant to 35 U.S.C. § 271, *et seq.*, directly, either literally or under the doctrine of equivalents, by using the ’259 Accused Processes in violation of one or more claims of the ’259 patent. TI has and continues to infringe pursuant to 35 U.S.C. § 271, *et seq.*, directly, either literally or under the doctrine of equivalents, by making, selling, or offering to sell in the United States, or importing into the United States products manufactured or otherwise produced using the ’259 Accused Processes in violation of one or more claims of the ’259 patent.

109. TI’s infringement of the ’259 patent is exceptional and entitles Bell Semic to attorneys’ fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

110. Bell Semic is entitled to recover from TI all damages that Bell Semic has sustained as a result of TI’s infringement of the ’259 patent, including without limitation and/or not less than a reasonable royalty.

COUNT II – INFRINGEMENT OF U.S. PATENT NO. 6,436,807

111. Bell Semic re-alleges and incorporates by reference the allegations of the foregoing paragraphs as if fully set forth herein.

112. The ’807 patent is valid and enforceable under the United States Patent Laws.

113. Bell Semic owns, by assignment, all right, title, and interest in and to the ’807 patent, including the right to collect for past damages.

114. On information and belief, TI directly infringed pursuant to 35 U.S.C. § 271(a) one or more claims of the ’807 patent by using the patented methodology to design one or more semiconductor devices, including as one example the TI 66AK2H12 Exemplary Accused Product, in the United States.

115. On information and belief, TI employs a variety of design tools, for example, Cadence, Synopsys, and/or Siemens tools, to make a layout for an interconnect layer of a

semiconductor device (the "'807 Accused Processes") as recited in the '807 patent claims. As one example, TI's '807 Accused Processes perform a method for making a layout for an interconnect layer of a semiconductor device, where the layout facilitates uniformity of planarization during manufacture of the semiconductor device as required by claim 1 of the '807 patent. TI does so by employing a design tool, such as at least one of a Cadence, Synopsys, and/or Siemens tool, to make a layout for the interconnect layer of its Accused Products, including the TI 66AK2H12 Exemplary Accused Product. The layout of each Accused Product facilitates uniformity of planarization during manufacture of the device. TI's '807 Accused Processes also determine an active interconnect feature density for each of a plurality of layout regions of the interconnect layout. TI does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, to determine an active interconnect feature density for each of a plurality of layout regions of the interconnect layout of each of its Accused Products.

116. TI's '807 Accused Processes also add dummy fill features to each layout region to obtain a desired density of active interconnect features and dummy fill features to facilitate uniformity of planarization during manufacturing of the semiconductor device, the adding comprising defining a minimum dummy fill feature lateral dimension based upon a dielectric layer deposition bias for a dielectric layer to be deposited over the interconnect layer.

117. TI does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, to add dummy fill features to each layout region to obtain a desired density of active interconnect features and dummy fill features to facilitate uniformity of planarization during manufacturing of the semiconductor device. The adding of dummy fill through the use of these design tools comprises defining a minimum dummy fill feature lateral

dimension based upon a dielectric layer deposition bias for a dielectric layer to be deposited over the interconnect layer. An exemplary infringement analysis showing infringement of one or more claims of the ’807 patent is set forth in Exhibit H. The declaration of Lloyd Linder, an expert in the field of semiconductor device design, is attached at Exhibit M and further describes TI’s infringement of the ’807 patent.

118. TI’s ’807 Accused Processes infringed one or more claims of the ’807 patent during the pendency of the ’807 patent.

119. On information and belief, TI infringed pursuant to 35 U.S.C. § 271, *et. seq.*, directly, either literally or under the doctrine of equivalents, by using the ’807 Accused Processes in violation of one or more claims of the ’807 patent during the pendency of the ’807 patent. TI has infringed pursuant to 35 U.S.C. § 271, *et. seq.*, directly, either literally or under the doctrine of equivalents, by making, selling, or offering to sell in the United States, or importing into the United States products manufactured or otherwise produced using the ’807 Accused Processes in violation of one or more claims of the ’807 patent during its pendency.

120. TI’s infringement of the ’807 patent was exceptional and entitles Bell Semic to attorneys’ fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

121. Bell Semic has been damaged by TI’s infringement of the ’807 patent. Bell Semic is entitled to recover from TI all damages that Bell Semic has sustained as a result of TI’s infringement of the ’807 patent, including without limitation and/or not less than a reasonable royalty.

COUNT III – INFRINGEMENT OF U.S. PATENT NO. 7,260,803

122. Bell Semic re-alleges and incorporates by reference the allegations of the foregoing paragraphs as if fully set forth herein.

123. The ’803 patent is valid and enforceable under the United States Patent Laws.

124. Bell Semic owns, by assignment, all right, title, and interest in and to the ’803 patent, including the right to collect for past damages.

125. On information and belief, TI has and continues to directly infringe pursuant to 35 U.S.C. § 271(a) one or more claims of the ’803 patent by using the patented methodology to design one or more devices, including for example the TI 66AK2H12 Exemplary Accused Product, in the United States.

126. On information and belief, TI employs a variety of design tools, for example, Cadence, Synopsys, and/or Siemens tools, to delete intersecting dummy metal objects from its circuit designs (the "’803 Accused Processes") as recited in the ’803 patent claims. As one example, TI’s ’803 Accused Processes perform a method of dummy metal insertion in design data for an integrated circuit, which includes dummy metal objects inserted by a dummy fill tool as required by claim 1 of the ’803 patent. TI does so by employing a design tool, such as at least one of a Cadence, Synopsys, and/or Siemens tool, that performs this dummy metal process for the layout of its Accused Products, including but not limited to the Exemplary Accused Products. The Accused Products, including the TI 66AK2H12 Exemplary Accused Product, include dummy metal objects inserted by a dummy fill tool, such as an "integrated" or "in-design" flow.

127. After a portion of the design data is changed, TI’s ’803 Accused Processes perform a check to determine whether any dummy metal objects intersect with any other objects in the design data. When TI receives an Engineering Change Order ("ECO"), it employs a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, to perform a Design Rule Check ("DRC") to determine whether there are any rule violations, including those related to metal fill geometries and layout changes, in the design data for the Accused Products, including but not limited to the TI 66AK2H12 Exemplary Accused Product.

128. TI's '803 Accused Processes also delete the intersecting dummy metal objects from the design data, thereby avoiding having to rerun the dummy fill tool. TI does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, that repairs DRC violations associated with shorts caused by dummy fill geometries intersecting with other objects in the design data. For example, the '803 Accused Processes allow designers to trim metal fill geometries that cause the short or DRC violation. An exemplary infringement analysis showing infringement of one or more claims of the '803 patent by the processing of the TI 66AK2H12 Exemplary Accused Product is set forth in Exhibit I. The declaration of Lloyd Linder, an expert in the field of semiconductor device design, is attached at Exhibit M and further describes TI's infringement of the '803 patent.

129. TI's '803 Accused Processes infringe and continue to infringe one or more claims of the '803 patent during the pendency of the '803 patent.

130. On information and belief, TI has and continues to infringe pursuant to 35 U.S.C. § 271, *et seq.*, directly, either literally or under the doctrine of equivalents, by using the '803 Accused Processes in violation of one or more claims of the '803 patent. TI has and continues to infringe pursuant to 35 U.S.C. § 271, *et seq.*, directly, either literally or under the doctrine of equivalents, by making, selling, or offering to sell in the United States, or importing into the United States products manufactured or otherwise produced using the '803 Accused Processes in violation of one or more claims of the '803 patent, including but not limited to the Exemplary Accused Products.

131. TI's infringement of the '803 patent is exceptional and entitles Bell Semic to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

132. Bell Semic is entitled to recover from TI all damages that Bell Semic has sustained as a result of TI's infringement of the '803 patent, including without limitation and/or not less than a reasonable royalty.

COUNT IV – INFRINGEMENT OF U.S. PATENT NO. 7,149,989

133. Bell Semic re-alleges and incorporates by reference the allegations of the foregoing paragraphs as if fully set forth herein.

134. The '989 patent is valid and enforceable under the United States Patent Laws.

135. Bell Semic owns, by assignment, all right, title, and interest in and to the '989 patent, including the right to collect for past damages.

136. On information and belief, TI has and continues to directly infringe pursuant to 35 U.S.C. § 271(a) one or more claims of the '989 patent by using at least one of the patented methodologies to design one or more devices, including for example the TI 66AK2H12 Exemplary Accused Product in the United States.

137. On information and belief, TI employs a variety of design tools, for example, Cadence, Synopsys, and/or Siemens tools, to validate its circuit designs (the "'989 Accused Processes") as recited in the '989 patent claims. As one example, TI's '989 Accused Processes perform a method that receives as input a representation of an integrated circuit design as required by claim 1 of the '989 patent. TI does so by employing a design tool, such as at least one of a Cadence, Synopsys, and/or Siemens tool, into which a circuit design for its TI 66AK2H12 Exemplary Accused Product is imported.

138. TI's '989 Accused Processes also receive as input a physical design rule deck that specifies rule checks to be performed on the integrated circuit design. TI does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, that receives

various in-design verification processes for concurrent physical design and verification of the TI 66AK2H12 Exemplary Accused Product's circuit designs.

139. TI's '989 Accused Processes also generate a specific rule deck from the physical design rule deck wherein the specific rule deck includes only physical design rules that are specific to texted metal short circuits between different signal sources in addition to power and ground in the integrated circuit design. TI does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, that includes a "short finder," "short locator," or similar functionality that identifies texted metal short circuits. For example, the '989 Accused Processes allow designers to select texted metal short circuits, which are shown by cell, text, net, layer and position. The nets may include ground, power, and other signal nets. An exemplary infringement analysis showing infringement of one or more claims of the '989 patent is set forth in Exhibit J. The declaration of Lloyd Linder, an expert in the field of semiconductor device design, is attached at Exhibit M and further describes TI's infringement of the '989 patent.

140. TI's '989 Accused Processes infringe and continue to infringe one or more claims of the '989 patent during the pendency of the '989 patent.

141. On information and belief, TI has and continues to infringe pursuant to 35 U.S.C. § 271, *et seq.*, directly, either literally or under the doctrine of equivalents, by using the '989 Accused Processes in violation of one or more claims of the '989 patent. TI has and continues to infringe pursuant to 35 U.S.C. § 271, *et seq.*, directly, either literally or under the doctrine of equivalents, by making, selling, or offering to sell in the United States, or importing into the United States products manufactured or otherwise produced using the '989 Accused Processes in

violation of one or more claims of the ’989 patent, including but not limited to the Exemplary Accused Products.

142. TI’s infringement of the ’989 patent is exceptional and entitles Bell Semic to attorneys’ fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

143. Bell Semic is entitled to recover from TI all damages that Bell Semic has sustained as a result of TI’s infringement of the ’989 patent, including without limitation and/or not less than a reasonable royalty.

COUNT V – INFRINGEMENT OF U.S. PATENT NO. 7,231,626

144. Bell Semic re-alleges and incorporates by reference the allegations of the foregoing paragraphs as if fully set forth herein.

145. The ’626 patent is valid and enforceable under the United States Patent Laws.

146. Bell Semic owns, by assignment, all right, title, and interest in and to the ’626 patent, including the right to collect for past damages.

147. On information and belief, TI has and continues to directly infringe pursuant to 35 U.S.C. § 271(a) one or more claims of the ’626 patent by using the patented methodology to design one or more semiconductor devices, including as one example the TI 66AK2H12 Exemplary Accused Product, in the United States.

148. On information and belief, TI employs a variety of design tools, for example, Cadence, Synopsys, and/or Siemens tools, to perform incremental routing in implementing an ECO (the “’626 Accused Processes”) as recited in the ’626 patent claims. As one example, TI’s ’626 Accused Processes perform a method for only routing the nets affected by the ECO and merging that changed area into the overall circuit layout as required by claim 1 of the ’626 patent. TI does so by employing a design tool, such as at least one of a Cadence, Synopsys,

and/or Siemens tool, to perform incremental routing as part of implementing an ECO for the TI 66AK2H12 Exemplary Accused Product to generate a revised integrated circuit design.

149. TI's '626 Accused Processes also calculate and perform a parasitic extraction only for each net in the IC design enclosed by the window defining the ECO. (This parasitic extraction is also how the '626 Accused Processes further calculate a net delay only for each net in the IC design enclosed by the window defining the ECO.) TI does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, to perform the incremental routing during implementation of the ECO for the Accused Products' (including but not limited to the Exemplary Accused Products') circuit designs.

150. TI's '626 Accused Processes also perform a design rule check only for each net in the IC design enclosed by the ECO window. TI does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, perform the incremental ECO and automatically perform a DRC for those nets to ensure that the ECO did not violate any design rules when it fixed other issues.

151. An exemplary infringement analysis showing infringement of one or more claims of the '626 patent is set forth in Exhibit K. The declaration of Lloyd Linder, an expert in the field of semiconductor device design, is attached at Exhibit M and further describes TI's infringement of the '626 patent.

152. TI's '626 Accused Processes infringe and continue to infringe one or more claims of the '626 patent during the pendency of the '626 patent.

153. On information and belief, TI has and continues to infringe pursuant to 35 U.S.C. § 271, *et. seq.*, directly, either literally or under the doctrine of equivalents, by using the '626 Accused Processes in violation of one or more claims of the '626 patent. TI has and continues to

infringe pursuant to 35 U.S.C. § 271, *et. seq.*, directly, either literally or under the doctrine of equivalents, by making, selling, or offering to sell in the United States, or importing into the United States products manufactured or otherwise produced using the Accused Processes in violation of one or more claims of the ’626 patent.

154. TI’s infringement of the ’626 patent is exceptional and entitles Bell Semic to attorneys’ fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

155. Bell Semic is entitled to recover from TI all damages that Bell Semic has sustained as a result of TI’s infringement of the ’626 patent, including without limitation and/or not less than a reasonable royalty.

COUNT VI – INFRINGEMENT OF U.S. PATENT NO. 7,396,760

156. Bell Semic re-alleges and incorporates by reference the allegations of the foregoing paragraphs as if fully set forth herein.

157. The ’760 patent is valid and enforceable under the United States Patent Laws.

158. Bell Semic owns, by assignment, all right, title, and interest in and to the ’760 patent, including the right to collect for past damages.

159. On information and belief, TI has and continues to directly infringe pursuant to 35 U.S.C. § 271(a) one or more claims of the ’760 patent by using the patented methodology to design one or more semiconductor devices, including as one example the TI 66AK2H12 Exemplary Accused Product, in the United States.

160. On information and belief, TI employs a variety of design tools, for example, Cadence, Synopsys, and/or Siemens tools, to rearrange dummy fill to minimize its overlap in successive layers (the “’760 Accused Processes”) as recited in the ’760 patent claims. As one example, TI’s ’760 Accused Processes allow arrangement and rearrangement of dummy fill in a timing aware fashion, including with the ability to stagger the dummy fill in successive layers so

as to minimize the interlayer bulk capacitance after determining their overlap as required by claim 1 of the '760 patent. TI does so by employing a design tool, such as at least one of a Cadence, Synopsys, and/or Siemens tool, rearrange the dummy fill features in successive layers of the Accused Products, including but not limited to the Exemplary Accused Products.

161. TI's '760 Accused Processes also form the dummy fill features in a grid within one or more of the successive layers, provide square-shaped dummy fill features in one or more of the successive layers, determine the dummy fill space based on a local pattern density in one or more of the successive layers, and minimize total bulk capacitance and/or certain of its components. TI does so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or Siemens tools, to implement dummy fill functionality in a timing-aware fashion and with consideration of interlayer capacitive effects in creation and design of its Accused Products, including but not limited to the Exemplary Accused Products.

162. An exemplary infringement analysis showing infringement of one or more claims of the '760 patent is set forth in Exhibit L. The declaration of Dhaval Brahmbhatt, an expert in the field of semiconductor device design, is attached at Exhibit N and further describes TI's infringement of the '760 patent.

163. TI's '760 Accused Processes infringe and continue to infringe one or more claims of the '760 patent during the pendency of the '760 patent.

164. On information and belief, TI has and continues to infringe pursuant to 35 U.S.C. § 271, *et. seq.*, directly, either literally or under the doctrine of equivalents, by using the '760 Accused Processes in violation of one or more claims of the '760 patent. TI has and continues to infringe pursuant to 35 U.S.C. § 271, *et. seq.*, directly, either literally or under the doctrine of equivalents, by making, selling, or offering to sell in the United States, or importing into the

United States products manufactured or otherwise produced using the ’760 Accused Processes in violation of one or more claims of the ’760 patent.

165. TI’s infringement of the ’760 patent is exceptional and entitles Bell Semic to attorneys’ fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

166. Bell Semic is entitled to recover from TI all damages that Bell Semic has sustained as a result of TI’s infringement of the ’760 patent, including without limitation and/or not less than a reasonable royalty.

PRAYER FOR RELIEF

WHEREFORE, Bell Semic respectfully requests that this Court enter judgment in its favor as follows and award Bell Semic the following relief:

(a) a judgment declaring that TI has infringed one or more claims of each of the Asserted Patents in this litigation pursuant to 35 U.S.C. § 271, *et seq.*;

(b) an award of damages adequate to compensate Bell Semic for infringement of the each of the Asserted Patents by TI, in an amount to be proven at trial, including (for each Asserted Patent other than the ’807 patent) supplemental post-verdict damages until such time as TI ceases its infringing conduct;

(c) a permanent injunction, pursuant to 35 U.S.C. § 283, prohibiting TI and its officers, directors, employees, agents, consultants, contractors, suppliers, distributors, all affiliated entities, and all others acting in privity with TI , from committing further acts of infringement, with respect each Asserted Patent other than the ’807 patent;

(d) a judgment requiring TI to make an accounting of damages resulting from TI’s infringement of each of the Asserted Patents;

(e) the costs of this action, as well as attorneys’ fees as provided by 35 U.S.C. § 285;

(f) pre-judgment and post-judgment interest at the maximum amount permitted by law;

(g) all other relief, in law or equity, to which Bell Semic is entitled.

DEMAND FOR JURY TRIAL

Plaintiff hereby demands a jury trial for all issues so triable.

Dated: February 17, 2023

/s/ Clifford Chad Henson

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