**IN THE UNITED STATES DISTRICT COURT**
**FOR THE EASTERN DISTRICT OF TEXAS**
**MARSHALL DIVISION**

| | | |
|---|---|---|
| XUESHAN TECHNOLOGIES, INC.,<br><br>Plaintiff,<br><br>v.<br><br>RENESAS ELECTRONICS CORPORATION,<br><br>Defendant. | §<br>§<br>§<br>§<br>§<br>§<br>§<br>§<br>§<br>§<br>§<br>§ | CIVIL ACTION NO. 2:23-cv-91<br><br>**JURY TRIAL DEMANDED** |

**PLAINTIFF'S COMPLAINT FOR PATENT INFRINGEMENT**

Plaintiff Xueshan Technologies Inc. ("XTI") files this Complaint against Defendant Renesas Electronics Corporation ("Renesas") for infringement of U.S. Patent No. 7,490,321 (the "'321 Patent"), U.S. Patent No. 7,689,749, (the "'749 Patent"), U.S. Patent No. 8,125,565 (the "'565 Patent"), U.S. Patent No. 8,332,623 (the "'623 Patent"), and U.S. Patent No. 9,166,475 (the "'475 Patent"), collectively, the "Asserted Patents."

**THE PARTIES**

1. Xueshan Technologies Inc. is a Delaware corporation having a principal place of business in the Eastern District of Texas.

2. On information and belief, Renesas Electronics Corporation is a corporation organized under the laws of Japan, having a principal place of business at Toyosu Foresia, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan. Renesas is a leading manufacturer and seller of semiconductors, integrated circuits, microcontrollers ("MCUs"), microprocessors ("MPUs"), and System on a Chip products ("SoCs") in the United States and the world, generally. Renesas conducts business in Texas and, particularly, the Eastern District of Texas, directly or through

intermediaries (including subsidiaries, distributors, affiliates, retailers, suppliers, integrators, customers, and others).

3. Renesas is engaged in making, using, selling, offering for sale, and/or importing products, such as semiconductors, integrated circuits, MCUs, MPUs, and SoCs, to and throughout the United States, including this District. Renesas also induces its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, and customers in the making, using, selling, offering for sale, and/or importing such products to and throughout the United States, including this District. To this end, Renesas and its foreign and U.S.-based subsidiaries—which act together as part of Renesas' global network of sales and manufacturing emissaries—have operated as agents of and for one another and have otherwise acted vicariously for Renesas as elements of the same business group and/or enterprise. Indeed, they work in concert and in orchestrated fashion, subject to agreements that are far nearer than arm's length, in order to implement a distribution channel of infringing products within this District and the United States.

4. Renesas maintains a substantial corporate presence in the United States via at least its U.S.-based sales subsidiaries, including Renesas Electronics America Inc. ("REA"). REA is a corporation organized under the laws of the State of California, having a principal place of business at 6024 Silver Creek Valley Road, San Jose, California 95138. REA is a wholly-owned subsidiary of Renesas. REA is responsible for Renesas' domestic sales, offers for sale, importation, marketing, and support in North America. REA is Renesas' agent, operating at Renesas' direction and control. Subject to such direction and control, Renesas' U.S.-based sales subsidiaries including, REA, import and sell infringing products, such as semiconductors, integrated circuits, MCUs, MPUs, and SoCs, in the United States and this District.

5. Alone and through at least the activities of its U.S.-based sales subsidiaries (e.g., REA), Renesas conducts business in the United States and this District, including importing, distributing, and selling semiconductors, integrated circuits, MCUs, MPUs, and SoCs that incorporate devices, systems, and processes that infringe the Asserted Patents. *See Trois v. Apple Tree Auction Center, Inc.*, 882 F.3d 485, 490 (5th Cir. 2018) ("A defendant may be subject to personal jurisdiction because of the activities of its agent within the forum state…."); *see also Cephalon, Inc. v. Watson Pharmaceuticals, Inc.*, 629 F. Supp. 2d 338, 348 (D. Del. 2009) ("The agency theory may be applied not only to parents and subsidiaries, but also to companies that are 'two arms of the same business group,' operate in concert with each other, and enter into agreements with each other that are nearer than arm's length.").

6. Through importation, offers to sell, sales, distributions, and related agreements to transfer ownership of Renesas' products (e.g., semiconductors, integrated circuits, MCUs, MPUs, and SoCs) with distributors and customers operating in and maintaining significant business presences in the United States, Renesas conducts extensive business in the United States, this State, and this District.

## JURISDICTION AND VENUE

7. This is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. §§ 1, *et seq*. This Court has jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and 1338(a) and 1367.

8. This Court has specific and personal jurisdiction over Renesas consistent with the requirements of the Due Process Clause of the United States Constitution and the Texas Long Arm Statute because, among other things, (i) Renesas has done and continues to do business in Texas, and (ii) Renesas has committed and continues to commit, directly or through intermediaries

(including subsidiaries, distributors, affiliates, retailers, suppliers, integrators, customers, and others), acts of patent infringement in this State. Such acts of infringement include making, using, offering to sell, and/or selling Accused Products (as more particularly identified and described throughout this Complaint) in this State and this District and/or importing Accused Products into this State and/or inducing others to commit acts of patent infringement in this State. Indeed, Renesas has purposefully and voluntarily placed, and is continuing to place, one or more Accused Products into the stream of commerce through established distribution channels (including the Internet) with the expectation and intent that such products will be sold to and purchased by consumers in the United States, this State, and this District; and with the knowledge and expectation that such products (whether in standalone form or as integrated in downstream products) will be imported into the United States, this State, and this District.

9. Renesas has derived substantial revenues from its infringing acts occurring within this State and this District. It has substantial business in this State and this District, including: (i) at least part of its infringing activities alleged herein; and (ii) regularly doing or soliciting business, engaging in other persistent conduct, and/or deriving substantial revenue from infringing goods offered for sale, sold, and imported, and services provided to Texas residents vicariously through and/or in concert with its alter egos, intermediaries, agents, distributors, importers, customers, subsidiaries, and/or consumers.

10. This Court has personal jurisdiction over Renesas, directly or through intermediaries (e.g., subsidiaries, distributors, affiliates, retailers, suppliers, integrators, customers, and others), including its U.S.-based sales subsidiaries, e.g., REA. Through direction and control of such subsidiaries, Renesas has committed acts of direct and/or indirect patent infringement within this State and elsewhere within the United States giving rise to this action and/or has

established minimum contacts with this forum such that the exercise of personal jurisdiction over Renesas would not offend traditional notions of fair play and substantial justice. REA is a wholly-owned subsidiary of Renesas. The primary business of REA is the marketing, support, and sale of Renesas' electronic products in the United States. Upon information and belief, Renesas compensates REA for marketing, support, and sales services in the United States. As such, Renesas has a direct financial interest in its U.S.-based subsidiaries, and vice versa.

11. Renesas controls and otherwise directs and authorizes all activities of its U.S.-based sales subsidiaries, including REA. Such directed and authorized activities include, the U.S.-based subsidiaries using, offering for sale, selling, and/or importing the Accused Products, their components, and/or products containing the same that incorporate and/or perform the fundamental technologies covered by the Asserted Patents. Renesas' U.S.-based sales subsidiaries (including REA), are expressly authorized to import, distribute, offer to sell, and sell the Accused Products on behalf of Renesas. For example, Renesas researches, designs, develops, and manufactures semiconductors, integrated circuits, MCUs, MPUs, and SoCs, and then directs its U.S.-based sales subsidiaries to import, distribute, offer for sale, and sell the Accused Products in the United States. *See, e.g., United States v. Hui Hsiung*, 778 F.3d 738, 743 (9th Cir. 2015) (finding that the sale of infringing products to third parties rather than for direct import into the U.S. did not "place [defendants'] conduct beyond the reach of United States law [or] escape culpability under the rubric of extraterritoriality"). Renesas' U.S.-based sales subsidiaries also provide, on Renesas' behalf, marketing and technical support services for the Accused Products from their facilities in the United States. For example, REA helps maintain a website that advertises the Accused Products, including identifying the applications for which they can be used and providing related specifications. *See, e.g.*, https://www.renesas.com/us/en/. The referenced website also contains

user manuals, product documentation, and other materials related to Renesas' products. For example, the website includes: (i) reference designs (https://www.renesas.com/us/en/products/software-tools/boards-and-kits/reference-designs.html) spanning analog products, power management products, and microprocessor and microcontrollers, (ii) complimentary design review services such as EDA schematic symbols, PCB footprints, and simulation models in industry-standard formats to help shorten development time (https://www.renesas.com/us/en/support/technical-resources/eda-data.html); (iii) robust customer support through REA's online support platforms including REA's Synergy Platform (https://www.renesas.com/us/en/support/contact.html); and (iv) REA's Knowledgebase (https://en-support.renesas.com/knowledgeBase). Thus, Renesas' U.S.-based sales subsidiaries, including REA, conduct infringing activities on Renesas' behalf.

12. On information and belief, because Renesas' U.S.-based sales subsidiaries are authorized by Renesas to import, distribute, offer to sell, and sell Accused Products and/or to perform the fundamental technologies covered by the Asserted Patents, Renesas' U.S.-based sales subsidiaries' corporate presences in the United States give Renesas substantially the same business advantages it would enjoy if it conducted its business through its own offices and personnel.

13. In addition, Renesas has knowingly induced, and continues to knowingly induce, infringement within this District by advertising, marketing, offering for sale and/or selling Accused Products (such as semiconductors, integrated circuits, MCUs, MPUs, and SoCs) that incorporate the fundamental technologies covered by the Asserted Patents. Such advertising, marketing, offering for sale and/or selling of Accused Products is directed to manufacturers, integrators, suppliers, distributors, resellers, partners, consumers, customers, and/or end users, and this includes providing instructions, user manuals, advertising, and/or marketing materials

facilitating, directing and encouraging use of infringing functionality with Renesas' knowledge thereof.

14. Renesas has, thus, in the multitude of ways described above, availed itself of the benefits and privileges of conducting business in this State and willingly subjected itself to the exercise of this Court's personal jurisdiction. Indeed, Renesas has sufficient minimum contacts with this forum through its transaction of substantial business in this State and this District and its commission of acts of patent infringement as alleged in this Complaint that are purposefully directed towards this State and District.

15. Alternatively, the Court maintains personal jurisdiction over Renesas under Federal Rule of Civil Procedure 4(k)(2).

16. Venue is proper in this District pursuant to 28 U.S.C. § 1391 because, among other things, Renesas is not a resident of the United States, and thus may be sued in any judicial district, including this one, pursuant to 28 U.S.C. § 1391(c)(3). *See In re HTC Corp.*, 889 F.3d 1349, 1357 (Fed. Cir. 2018) (holding that "[t]he Court's recent decision in *TC Heartland* does not alter" the alien-venue rule.).

## THE PATENTS-IN-SUIT

17. XTI is the sole and exclusive owner of all right, title, and interest in the'321 Patent, the '749 Patent, the '565 Patent, the '623 Patent, and the '475 Patent and holds the exclusive right to take all actions necessary to enforce its rights in, and to, the Asserted Patents, including the filing of this patent infringement lawsuit. XTI also has the right to recover all damages for past, present, and future infringements of the Asserted Patents and to seek injunctive relief as appropriate under the law.

18. The ’321 Patent is titled, “Method for updating firmware via determining program code.” The ’321 Patent lawfully issued on Feb. 10, 2009, and stems from U.S. Patent Application No. 10/904,378, which was filed on November 7, 2004.

19. The ’749 Patent is titled, “Interrupt control function adapted to control the execution of interrupt requests of differing criticality.” The ’749 Patent lawfully issued on March 30, 2010, and stems from U.S. Patent Application No. 11/665,544, which was filed on October 17, 2005.

20. The ’565 Patent is titled, “Image processing circuit and method thereof.” The ’565 Patent lawfully issued on February 28, 2012, and stems from U.S. Patent Application No. 12/339,909, which was filed on December 19, 2008.

21. The ’623 Patent is titled, “Embedded electronic device and booting method thereof.” The ’623 Patent lawfully issued on December 11, 2012, and stems from U.S. Patent Application No. 12/472,755, which was filed on May 27, 2009.

22. The ’475 Patent is titled, “Voltage regulator with fast and slow switching control.” The ’475 Patent lawfully issued on October 20, 2015, and stems from U.S. Patent Application No. 13/623,969, which was filed on September 21, 2012.

23. XTI and its predecessors complied with the requirements of 35 U.S.C. § 287, to the extent necessary, such that XTI may recover pre-suit damages.

24. The claims of the patents-in-suit are directed to patent eligible subject matter under 35 U.S.C. § 101. They are not directed to an abstract idea, and the technologies covered by the claims comprise systems and/or consist of ordered combinations of features and functions that, at the time of invention, were not, alone or in combination, well-understood, routine, or conventional.

## DEFENDANT’S PRE-SUIT KNOWLEDGE OF ITS INFRINGEMENT

25. Prior to the filing of the Complaint, XTI repeatedly attempted to engage Renesas and/or its agents in licensing discussions related to its portfolio including the Asserted Patents. After XTI's letters to Renesas from March 2021, May 2021, and February 2022 were ignored, XTI was left with no other choice but to seek relief through patent enforcement litigation and filed suit in this district in Case No. 2:22-cv-157-JRG-RSP (E.D. Tex.). *See* Dkt. 1 at ¶¶24-25.

26. XTI subsequently sent another letter to Renesas on prior to the filing of the Complaint identifying the Asserted Patents as being infringed by exemplary Renesas products, and further included claim charts demonstrating how the identified products infringe the Asserted Patents.

27. The Accused Products addressed in the Counts below include, but are not limited to, the exemplary products identified in XTI's letter to Renesas. Renesas' past and continuing sales of the Accused Products (i) willfully infringe the Asserted Patents, and (ii) impermissibly usurp the significant benefits of XTI's patented technologies without fairly compensating XTI.

## COUNT I

(INFRINGEMENT OF U.S. PATENT NO. 7,490,321)

28. Plaintiff incorporates the preceding paragraphs herein by reference.

29. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

30. XTI is the owner of all substantial rights, title, and interest in and to the '321 Patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

31. The '321 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on February 10, 2009, after full and fair examination.

32. Renesas has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the ’321 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, Renesas products, their components and processes, and/or products containing the same that incorporate the fundamental technologies covered by the ’321 Patent, including, but not limited to, the Renesas RL78 Microcontrollers (collectively, the “’321 Accused Products”).

***Direct Infringement (35 U.S.C. § 271(a))***

33. Renesas has directly infringed and continues to directly infringe one or more claims of the’321 Patent in this District and elsewhere in Texas and the United States.

34. Renesas has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 1 of the ’321 Patent[1] as set forth under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing the ’321 Accused Products. Furthermore, Renesas makes and sells the ’321 Accused Products outside of the United States and either delivers those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivers the ’321 Accused Products outside of the United States, it does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the ’321 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013). Furthermore, Renesas directly infringes the ’321 Patent through its direct involvements in, and

[1] Throughout this Complaint, wherever XTI identifies specific claims of the Asserted Patents infringed by Renesas, XTI expressly reserves the right to identify additional claims and products in its infringement contentions in accordance with applicable local rules and the Court’s case management order. Specifically identified claims throughout this Complaint are provided for notice pleading only.

control of, the activities of its subsidiaries, including REA. Subject to Renesas' direction and control, such subsidiaries conduct activities that constitute direct infringement of the '321 Patent under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing '321 Accused Products. Renesas receives direct financial benefit from such infringements of its U.S.-based sales subsidiaries, including REA.

35. By way of illustration only, the '321 Accused Products perform each and every element of claim 1 of the '321 Patent. The '321 Accused Products perform "[a] method for updating program code stored in a memory module having a normal firmware section in an electronic device." For example, the '321 Accused Products perform a process for "Updating Firmware by Using UART Communication and Boot Swapping" as outlined in the Renesas Application note[2] excerpted and annotated below that reflects updating program code (purple box) stored in a memory module (blue box) having a normal firmware section (orange box) in an electronic device (light blue box), in this example the RL78 microcontroller:

[2] *See* https://www.renesas.com/us/en/document/apn/rl78g23-updating-firmware-using-uart-communication-and-boot-swapping-rev100 (last visited September 30, 2022)

RENESAS Application Note

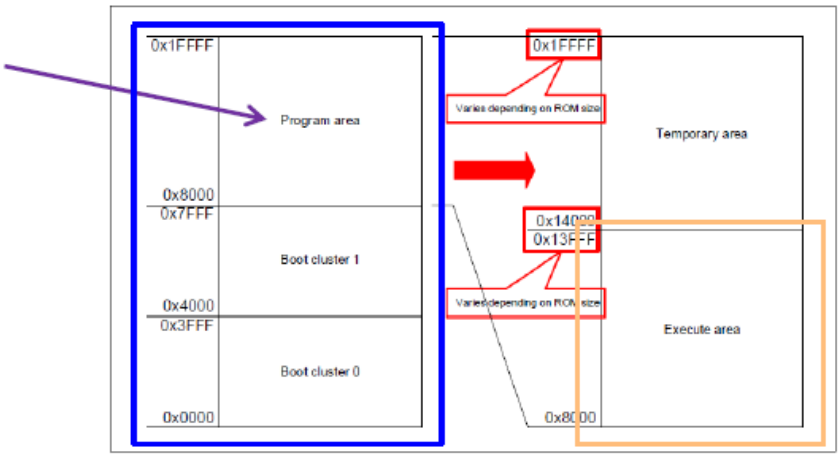
RL78/G23

Updating Firmware by Using UART Communication and Boot Swapping

**1.1.2 Code Flash Memory**

The program area (from address 08000H to the last address) is divided into two areas and the sample program covered in this application note uses these two areas. The first area (from address 08000H to the boundary) is called the Execute area and the second area (from the boundary to the last address) is called the Temporary area. The address of the boundary and the last address differ depending on the size of the ROM. The update program is written in boot cluster 1 and the Temporary area. Therefore, if you write a user program, make sure that it is stored within boot cluster 0 and the Execute area.

**Figure 1-2 Code Flash Memory Map**




RL78/G23 Application Note[3]

Further, Renesas directs or controls the performance of the method for updating program code stored in a memory module having a normal firmware section in an electronic device by others, such as end users of the device. For example, Renesas includes instructions and directives, such as firmware and source code, in the Accused Products that cause the device to perform the claimed method.

36. In the '321 Accused Products, the process for updating firmware comprises before updating a first program segment (red underline) stored in the memory module, setting values of

[3] *See* https://www.renesas.com/us/en/document/apn/rl78g23-updating-firmware-using-uart-communication-and-boot-swapping-rev100, pages 1, 6, 7 (last visited September 30, 2022)

at least one specific address (green underline) according to a second rule (dark green underline) as shown, for example, in the annotated excerpts from the RL78/G23 Application Note below. That is, as reflected at the orange underline, the copy flag is initialized to non-AAAA5555h value during erase.

### 1.2.8 Copy Flag

The sample program covered in this application note uses a 4-byte area at the end of the Execute area as the copy flag section in which to set a copy flag.

If a program is normally written, this copy flag is set to AAAA5555H. The copy flag is initialized when the Execute area is erased immediately before data is copied from the Temporary area to the Execute area. If a reset occurs (due to a temporary blackout) while data is being written, the copy flag is set to a value other than AAAA5555H because the write processing does not terminate normally.

When the sample program starts, it checks the copy flag. If the value of the copy flag is not AAAA5555H, the sample program writes data and then performs swapping.

The following table shows the start and end addresses of the Execute area and the address of the copy flag section according to the ROM size.

Table 1-8 Location of the Copy Flag Section According to the ROM Size

| ROM Size | Execute Area | Address of the Copy Flag Section |
|---|---|---|
| 96KB | 08000H to FFFFH | FFFCH |
| 128KB | 08000H to 13FFFH | 13FFCH |
| 192KB | 08000H to 1BFFFH | 1BFFCH |
| 256KB | 08000H to 23FFFH | 23FFCH |
| 384KB | 08000H to 33FFFH | 33FFCH |
| 512KB | 08000H to 43FFFH | 43FFCH |
| 768KB | 08000H to 63FFFH | 63FFCH |

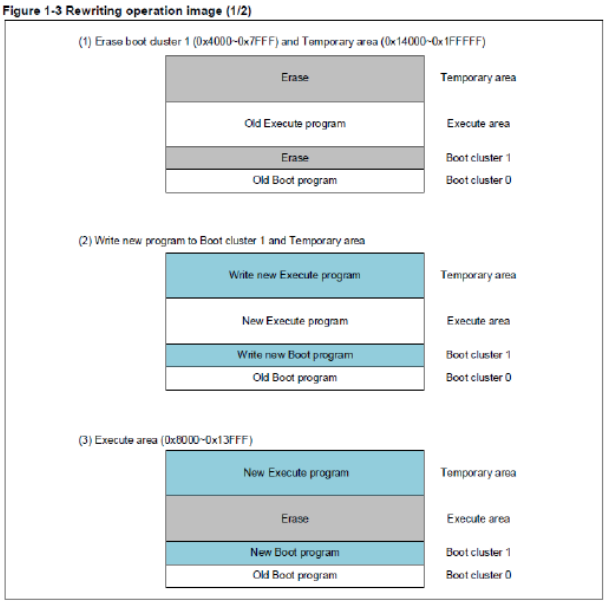
RL78/G23 Application Note[4]

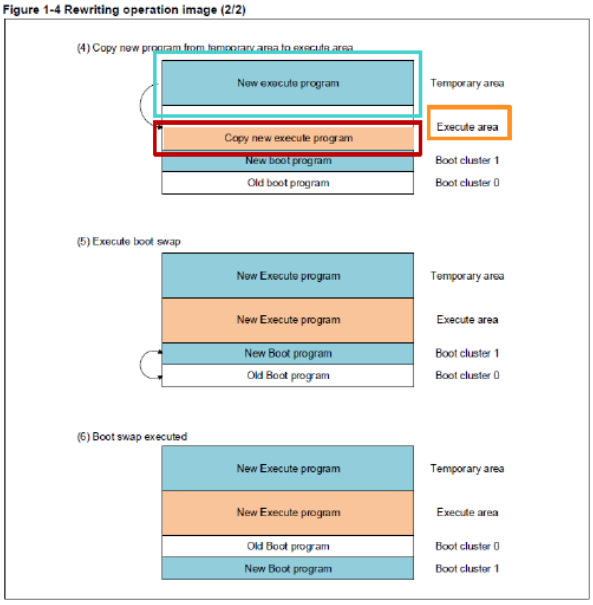
Further, Renesas directs or controls this step by including instructions and directives, such as firmware and source code, in the Accused Products that cause this to occur.

37. The process for updating firmware in the ’321 Accused Products further comprises replacing the first program segment (red box) stored in the normal firmware section (orange box)

[4] *See* https://www.renesas.com/us/en/document/apn/rl78g23-updating-firmware-using-uart-communication-and-boot-swapping-rev100, page 16 (last visited September 30, 2022)

with a second program segment (blue box) as shown, for example, in the annotated excerpts from the RL78/G23 Application Note below.




RL78/G23 Application Note5

Further, Renesas directs or controls this step by including instructions and directives, such as firmware and source code, in the Accused Products that cause this to occur.

38. In the process for updating firmware in the ’321 Accused Products, the second rule (dark green underline) is a mutually exclusive condition of the first rule (red underline), the first rule represents that the normal firmware section (orange underline and box) has been updated successfully, the second rule represents that the normal firmware section has not been updated successfully, and the values stored in the specific addresses (green underline and box) are employed to verify the correctness of updated program (purple underline) code in the normal firmware section as shown, for example, in the annotated excerpts from the RL78/G23 Application Note below:

[5] *See* https://www.renesas.com/us/en/document/apn/rl78g23-updating-firmware-using-uart-communication-and-boot-swapping-rev100, pages 9-10 (last visited September 30, 2022)

### 1.2.8 Copy Flag

The sample program covered in this application note uses a 4-byte area at the end of the Execute area as the copy flag section in which to set a copy flag.

If a program is normally written, this copy flag is set to AAAA5555H. The copy flag is initialized when the Execute area is erased immediately before data is copied from the Temporary area to the Execute area. If a reset occurs (due to a temporary blackout) while data is being written, the copy flag is set to a value other than AAAA5555H because the write processing does not terminate normally.

When the sample program starts, it checks the copy flag. If the value of the copy flag is not AAAA5555H, the sample program writes data and then performs swapping.

The following table shows the start and end addresses of the Execute area and the address of the copy flag section according to the ROM size.

Table 1-8 Location of the Copy Flag Section According to the ROM Size

| ROM Size | Execute Area | Address of the Copy Flag Section |
|---|---|---|
| 96KB | 08000H to FFFFH | FFFCH |
| 128KB | 08000H to 13FFFH | 13FFCH |
| 192KB | 08000H to 1BFFFH | 1BFFCH |
| 256KB | 08000H to 23FFFH | 23FFCH |
| 384KB | 08000H to 33FFFH | 33FFCH |
| 512KB | 08000H to 43FFFH | 43FFCH |
| 768KB | 08000H to 63FFFH | 63FFCH |

RL78/G23 Application Note[6]

Further, Renesas directs or controls this step by including instructions and directives, such as firmware and source code, in the Accused Products that cause this to occur.

***Indirect Infringement (Inducement – 35 U.S.C. § 271(b))***

39. In addition and/or in the alternative to its direct infringements, Renesas has indirectly infringed and continues to indirectly infringe one or more claims of the '321 Patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by

[6] *See* https://www.renesas.com/us/en/document/apn/rl78g23-updating-firmware-using-uart-communication-and-boot-swapping-rev100, page 16 (last visited September 30, 2022)

making, using, offering to sell, selling and/or importing into the United States the '321 Accused Products.

40. At a minimum, Renesas has knowledge of the '321 Patent since being served with this Complaint. Renesas also has knowledge of the '321 Patent since receiving detailed correspondence from XTI prior to the filing of the Complaint, alerting Renesas to its infringements. Since receiving notice of its infringements, Renesas has actively induced the direct infringements of its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Such inducements have been committed with the knowledge, or with willful blindness to the fact, that the acts induced constitute infringement of the '321 Patent. Indeed, Renesas has intended to cause, continues to intend to cause, and has taken, and continues to take affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the '321 Accused Products;[7] creating and/or maintaining established distribution channels for the '321 Accused Products into and within the United States; manufacturing the '321 Accused Products in conformity with U.S. laws and regulations; distributing or making available videos, training, tools and resources supporting use of the '321 Accused Products that promote their features, specifications, and applications;[8] providing technical documentation and tools for the '321 Accused Products, including white papers, brochures, and manuals;[9] promoting the

[7] *See, e.g.*, https://www.renesas.com/us/en/products/microcontrollers-microprocessors/renesas-synergy-platform-mcus; https://www.renesas.com/us/en/products/microcontrollers-microprocessors/rl78-low-power-8-16-bit-mcus (last visited October 4, 2022).

[8] *See, e.g.*, https://www.renesas.com/us/en/products/microcontrollers-microprocessors/rl78-low-power-8-16-bit-mcus#videos_training (last visited October 4, 2022).

[9] *See, e.g.*, RL78 Family Selection Guide, available at https://www.renesas.com/us/en/document/bro/rl78-family-selection-guide?language=en&r=469291 (last visited October 4, 2022); RL78 Family Microcontrollers

incorporation of the '321 Accused Products into end-user products through the development of Renesas' Partner programs;[10] and by providing technical support and/or related services for these products to purchasers in the United States through Renesas' online support platforms including RenesasRulz forum[11] further explaining how to use Renesas' products.

***Damages***

41. On information and belief, despite having knowledge of the '321 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the '321 Patent, Renesas has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. Renesas' infringing activities relative to the '321 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, characteristic of a pirate, and an egregious case of misconduct beyond typical infringement such that XTI is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

42. XTI has been damaged as a result of Renesas' infringing conduct described in this Count. Renesas is, thus, liable to XTI in an amount that adequately compensates XTI for Renesas' infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

**COUNT II**

(INFRINGEMENT OF U.S. PATENT NO. 7,689,749)

43. Plaintiff incorporates the preceding paragraphs herein by reference.

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Brochure, https://www.renesas.com/us/en/document/fly/rl78-family-microcontrollers-brochure?language=en&r=469291 (last visited October 4, 2022).

[10] *See* https://www.renesas.com/us/en/support/partners/preferred-partners (last visited October 4, 2022).

[11] *See* https://renesasrulz.com/ (last visited October 4, 2022).

44. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

45. XTI is the owner of all substantial rights, title, and interest in and to the '749 Patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

46. The '749 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on March 30, 2010, after full and fair examination.

47. Renesas has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the '749 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, Renesas products, their components and processes, and/or products containing the same that incorporate the fundamental technologies covered by the '749 Patent, including, but not limited to, the Renesas ARM Cortex-M series processors, including RA Series,[12] RE Series,[13] and Synergy Series,[14] and Renesas ARM Cortex Cortex-A series processors, including RZ Series,[15] (collectively, the "'749 Accused Products").

***Direct Infringement (35 U.S.C. § 271(a))***

48. Renesas has directly infringed and continues to directly infringe one or more claims of the'749 Patent in this District and elsewhere in Texas and the United States.

[12] **RA Series –** RA2A1, RA2E1, RA2L1, RA4M1, RA4M2, RA4M3, RA4W1, RA5M1, RA6M2, RA6M3, RA6M4, RA6M5, RA6T1.
[13] **RE Series –** RE01 1500KB, RE01 256KB, RE01B.
[14] **Synergy Series –** S124, S128, S1JA, S3A1, S3A3, S3A6, S3A7, S5D3, S5D5, S5D9, S7G2.
[15] **RZ Series –** RZ/A1H, RZ/A1L, RZ/A1LC RZ/A1LU, RZ/A1M, RZ/A2M, RZ/G1C, RZ/G1E, RZ/G1H, RZ/G1M, RZ/G1N, RZ/G2E, RZ/G2H, RZ/G2L, RZ/G2LC, RZ/G2M, RZ/G2N, RZ/G2UL, RZ/N1D, RZ/N1L, RZ/N1S, RZ/V2L, RZ/V2M.

49. Renesas has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 1 of the '749 Patent as set forth under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing, the '749 Accused Products. Furthermore, Renesas makes and sells the '749 Accused Products outside of the United States and either, delivers those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivers the '749 Accused Products outside of the United States, it does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the '749 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013). Furthermore, Renesas directly infringes the '749 Patent through its direct involvements in, and control of, the activities of its subsidiaries, including REA. Subject to Renesas' direction and control, such subsidiaries conduct activities that constitute direct infringement of the '749 Patent under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing '749 Accused Products. Renesas receives direct financial benefit from such infringements of its U.S.-based sales subsidiaries, including REA.

50. By way of illustration only, the '749 Accused Products include each and every element of claim 1 of the '749 Patent.

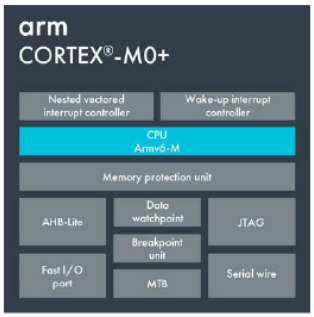
51. The '749 Accused Products include "[a]n interrupt control function adapted to control the execution of interrupt requests of differing criticality by a processor which is required to execute tasks of differing criticality under the control of a computer operating system." For example, the '749 Accused Products comprise an ARM processor and interrupt control function as shown below:

## Specifications

**The Arm Cortex-M0+ processor is the most energy-efficient Arm processor available for constrained embedded applications.**

The Cortex-M0+ processor builds on the very successful Cortex-M0 processor, retaining full instruction set and tool compatibility, while further reducing energy consumption and increasing performance.

The exceptionally small silicon area, low power and minimal code footprint of Cortex-M0+ enables developers to achieve 32-bit performance at an 8-bit price point, bypassing the step to 16-bit devices. The Cortex-M0+ processor comes with a wide selection of options to provide flexible development.




Arm Cortex-M0+ processor

| | |
|---|---|
| **Architecture** | Armv6-M |
| **Bus Interface** | AMBA AHB-Lite, Von Neumann bus architecture with optional single-cycle I/O interface |
| **ISA Support** | Thumb/Thumb-2 subset |
| **Pipeline** | 2-stage |
| **Memory Protection** | Optional 8 region MPU with sub regions and background region |
| **Bit Manipulation** | Bit banding region can be implemented with Corstone Foundation IP |
| **Interrupts** | Non-maskable Interrupt (NMI) + 1 to 32 physical interrupts |

ARM Cortex-M0+ Specifications[16]

## About the NVIC

External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and the Cortex-M0+ processor core are closely coupled, providing low latency interrupt processing and efficient processing of late arriving interrupts.

All NVIC registers are only accessible using word transfers. Any attempt to read or write a halfword or byte individually is Unpredictable.

NVIC registers are always little-endian. Processor accesses are correctly handled regardless of the endian configuration of the processor.

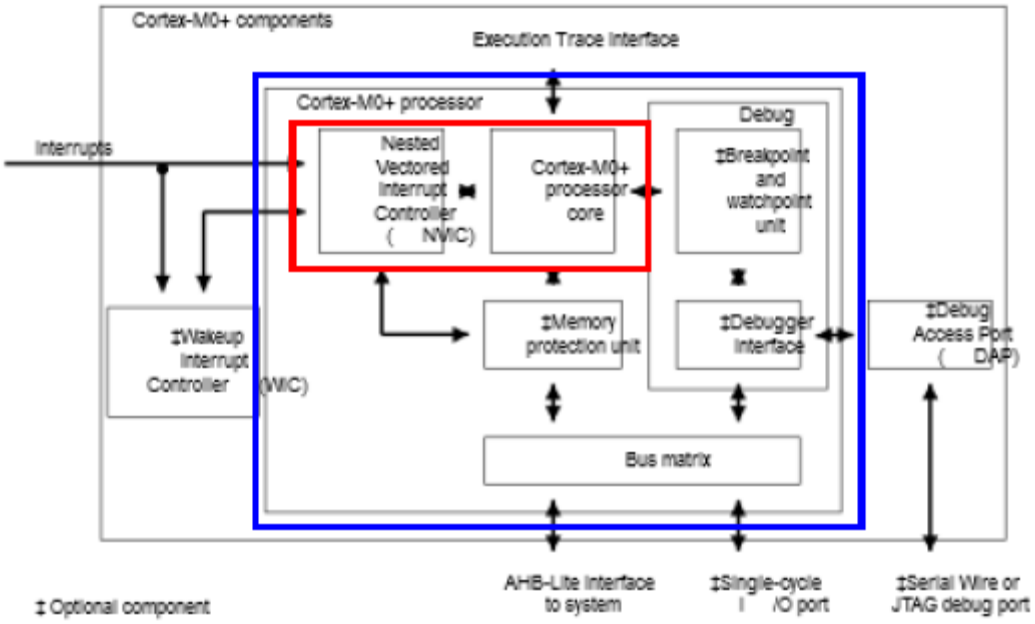
Processor exception handling is described in *Exceptions*.

ARM Cortex-M0+ Technical Reference Manual[17]

52. In the ’749 Accused Products, the interrupt control function (red box) is adapted to control the execution of interrupt requests of differing criticality (underlined in purple and pink) by a processor which is required to execute tasks (blue box and underlining) of differing criticality under the control of a computer operating system, for example as shown below:

[16] https://developer.arm.com/ip-products/processors/cortex-m/cortex-m0-plus (last visited February 27, 2023).
[17] https://developer.arm.com/documentation/ddi0484/c/Nested-Vectored-Interrupt-Controller/About-the-NVIC (last visited February 27, 2023).

## Figure 2.1. Functional block diagram




ARM Cortex-M0+ Technical Reference Manual[18]

[18] https://developer.arm.com/documentation/ddi0484/c/Functional-Description/About-the-functions (last visited February 27, 2023).

## B1.1 Introduction to the system level

The ARM architecture defines a hierarchy for software operation:

- The lowest level is the application level, described in part A of this manual. In particular, Chapter A2 *Application Level Programmers' Model* describes the programmers' model for applications. Application-level software is largely independent of the architecture profile.
- The higher level is the system level, that includes support for the applications. The system level features and how they are supported, are significantly different between the different architecture profiles.

Part B of this manual describes the ARMv6-M architecture at the system level.

As stated in *Privileged execution* on page A2-30, ARMv6-M supports unprivileged and privileged operation, or privileged operation only, depending on whether the implementation includes the Unprivileged/Privileged Extension. System level support requires privileged access, giving system software the access permissions required to configure and control the resources. Typically, an operating system provides system services to the applications, either transparently, or through application initiated supervisor calls. The operating system is also responsible for servicing interrupts and other system events, making exceptions a key component of the system level programmers' model. In a system that supports only privileged execution, application code can raise a supervisor call using SVC, or handle system access and control directly. ARMv6-M with the Unprivileged/Privileged Extension also supports a software model of unprivileged applications running under a privileged OS.

The ARMv6-M Debug Extension supports a Debug state, halting debug, and associated control and configuration registers, see Chapter C1 *ARMv6-M Debug* for more information.

The optional ARMv6-M *Protected Memory System Architecture* (PMSA) Extension and its *Memory Protection Unit* (MPU) protects the system memory space, see *Protected Memory System Architecture, PMSAv6* on page B3-289

ARMv6-M also supports an optional system timer, SysTick, see *The system timer, SysTick* on page B3-275.

ARMv6-M Architecture Reference Manual[19]

[19] http://115.28.165.193/down/arm/arch/ARMv6-M_Architecture_Reference_Manual.pdf (last visited February 27, 2023).

### B1.5.1 Overview of the exceptions supported

The ARMv6-M profile supports the following exceptions:

**NMI** *NMI* (Non Maskable Interrupt) is the highest priority exception other than reset. It is permanently enabled with a fixed priority of -2.

Hardware can generate an NMI, or software can set the NMI exception to the Pending state, see *Interrupt Control State Register, ICSR* on page B3-265, or hardware.

**Interrupts** The ARMv6-M profile supports two system level interrupts and up to 32 external interrupts. Each interrupt has a configurable priority. The system-level interrupts are:

### B1.5.4 Exception priorities and preemption

In the ARMv6-M priority model, lower numbers take precedence. That is, the lower the assigned priority value, the higher the priority level. The priority order for exceptions with the same priority level is fixed, and is determined by their exception number.

Reset, NMI, and HardFault execute at fixed priorities of -3, -2, and -1 respectively. Software can set the priority of all other exceptions using registers in the SCS. A reset clears these software-configured priority settings. Software-assigned priority values start at 0, so Reset, NMI, and HardFault always have higher priorities than any other exception.

When multiple pending exceptions have the same priority number, the pending exception with the lowest exception number takes precedence. When an exception is active, only an exception with a higher priority can preempt it.

ARMv6-M supports 2-bit priority fields, providing four priority levels.

**Table B1-3 Exception numbers**

| Exception number | Exception |
|---|---|
| 1 | Reset |
| 2 | NMI |
| 3 | HardFault |
| 4-10 | Reserved |
| 11 | SVCall |
| 12-13 | Reserved |
| 14 | PendSV |
| 15 | SysTick, optional |
| 16 | External Interrupt(0) |
| ... | ... |
| 16 + N | External Interrupt(N) |

ARMv6-M Architecture Reference Manual[20]

### B1.5.1 Overview of the exceptions supported

The ARMv6-M profile supports the following exceptions:

**HardFault** HardFault is the generic fault that exists for all classes of fault that cannot be handled by any of the other exception mechanisms. Typically, HardFault is used for unrecoverable system failures, although this is not required, and some uses of HardFault might be recoverable. HardFault is permanently enabled with a fixed priority of -1.

HardFault is used for all fault conditions on ARMv6-M.

**SVCall** This supervisor call handles the exception caused by the SVC instruction. SVCall is permanently enabled and has a configurable priority.

**Supervisor call (SVCall)**

An exception caused explicitly by the SVC instruction. Application software uses the SVC instruction to make a call to an underlying operating system. This is called a Supervisor call. The SVC instruction enables the application to issue a Supervisor call that requires privileged access to the system and executes in program order relative to the application. ARMv6-M also supports an interrupt-driven Supervisor calling mechanism PendSV. See *Interrupts* in *Overview of the exceptions supported* on page B1-218 for more information.

### B1.5.4 Exception priorities and preemption

In the ARMv6-M priority model, lower numbers take precedence. That is, the lower the assigned priority value, the higher the priority level. The priority order for exceptions with the same priority level is fixed, and is determined by their exception number.

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| 15 | SysTick, optional |
| 16 | External Interrupt(0) |
| ... | ... |
| 16 + N | External Interrupt(N) |

[20] http://115.28.165.193/down/arm/arch/ARMv6-M_Architecture_Reference_Manual.pdf (last visited February 27, 2023).

ARMv6-M Architecture Reference Manual[21]

53. The '749 Products comprise the interrupt control function being adapted to recognise critical and non-critical interrupt requests originating from different interrupt sources (green underline), and to recognise when the processor is required to execute each of critical and non critical tasks, for example as shown below (pink underline):

### B3.2.1 About the System Control Block

In an ARMv6-M a *System Control Block* (SCB) in the SCS provides key status information and control features for the processor. The SCB supports:

- Software reset control at various levels
- Base address management for the exception model, by controlling table pointers
- System exception management, including:
  - exception enables
  - setting the status of an exception to pending, or removing the pending status from an exception
  - showing the status of each exception status as inactive, pending, or active
  - setting the priority of the configurable system exceptions
  - providing miscellaneous control functions, and status information.

This excludes external interrupt handling. The NVIC handles all external interrupts.

### B3.2.4 Interrupt Control State Register, ICSR

| Bits | Type | Name | Function |
|---|---|---|---|
| [31] | RW | NMIPENDSET | Activates an NMI exception or reads back the current state:<br>**0** Do not activate.<br>**1** Activate NMI exception.<br>Because NMI is the highest priority exception, it activates as soon as it is registered. |

ARMv6-M Architecture Reference Manual[22]

[21] http://115.28.165.193/down/arm/arch/ARMv6-M_Architecture_Reference_Manual.pdf (last visited February 27, 2023).
[22] http://115.28.165.193/down/arm/arch/ARMv6-M_Architecture_Reference_Manual.pdf (last visited February 27, 2023).

### B1.5.1 Overview of the exceptions supported

The ARMv6-M profile supports the following exceptions:

**HardFault** HardFault is the generic fault that exists for all classes of fault that cannot be handled by any of the other exception mechanisms. Typically, HardFault is used for unrecoverable system failures, although this is not required, and some uses of HardFault might be recoverable. HardFault is permanently enabled with a fixed priority of -1.

HardFault is used for all fault conditions on ARMv6-M.

**SVCall** This supervisor call handles the exception caused by the SVC instruction. SVCall is permanently enabled and has a configurable priority.

**Supervisor call (SVCall)**

An exception caused explicitly by the SVC instruction. Application software uses the SVC instruction to make a call to an underlying operating system. This is called a Supervisor call. The SVC instruction enables the application to issue a Supervisor call that requires privileged access to the system and executes in program order relative to the application. ARMv6-M also supports an interrupt-driven Supervisor calling mechanism PendSV. See *Interrupts* in *Overview of the exceptions supported* on page B1-218 for more information.

### B1.5.4 Exception priorities and preemption

In the ARMv6-M priority model, lower numbers take precedence. That is, the lower the assigned priority value, the higher the priority level. The priority order for exceptions with the same priority level is fixed, and is determined by their exception number.

Reset, NMI, and HardFault execute at fixed priorities of -3, -2, and -1 respectively. Software can set the priority of all other exceptions using registers in the SCS. A reset clears these software-configured priority settings. Software-assigned priority values start at 0, so Reset, NMI, and HardFault always have higher priorities than any other exception.

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| 4-10 | Reserved |
| 11 | SVCall |
| 12-13 | Reserved |
| 14 | PendSV |
| 15 | SysTick, optional |
| 16 | External Interrupt(0) |
| ... | ... |
| 16 + N | External Interrupt(N) |

ARMv6-M Architecture Reference Manual[23]

54. The ’749 Products comprise the interrupt control function being further adapted to pass critical interrupt requests to the processor for execution in preference to non-critical interrupt requests (orange underline), to block non critical interrupt requests to the processor when they coexist with critical interrupt requests or the processor is required to execute critical tasks (green underline), and to pass non critical interrupt requests to the processor when they do not coexist with any critical interrupt requests and the processor has no critical tasks to be executed (aqua underline and box), for example as shown below:

[23] http://115.28.165.193/down/arm/arch/ARMv6-M_Architecture_Reference_Manual.pdf (last visited February 27, 2023).

### B1.5.1 Overview of the exceptions supported

The ARMv6-M profile supports the following exceptions:

**NMI** *NMI* (Non Maskable Interrupt) is the highest priority exception other than reset. It is permanently enabled with a fixed priority of -2.

Hardware can generate an NMI, or software can set the NMI exception to the Pending state, see *Interrupt Control State Register, ICSR* on page B3-265, or hardware.

**Interrupts** The ARMv6-M profile supports two system level interrupts and up to 32 external interrupts. Each interrupt has a configurable priority. The system-level interrupts are:

### B1.5.4 Exception priorities and preemption

In the ARMv6-M priority model, lower numbers take precedence. That is, the lower the assigned priority value, the higher the priority level. The priority order for exceptions with the same priority level is fixed, and is determined by their exception number.

Reset, NMI, and HardFault execute at fixed priorities of -3, -2, and -1 respectively. Software can set the priority of all other exceptions using registers in the SCS. A reset clears these software-configured priority settings. Software-assigned priority values start at 0, so Reset, NMI, and HardFault always have higher priorities than any other exception.

When multiple pending exceptions have the same priority number, the pending exception with the lowest exception number takes precedence. When an exception is active, only an exception with a higher priority can preempt it.

ARMv6-M supports 2-bit priority fields, providing four priority levels.

**Table B1-3 Exception numbers**

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| 4-10 | Reserved |
| 11 | SVCall |
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| 14 | PendSV |
| 15 | SysTick, optional |
| 16 | External Interrupt(0) |
| ... | ... |
| 16 + N | External Interrupt(N) |

ARMv6-M Architecture Reference Manual[24]

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| 15 | SysTick, optional |
| 16 | External Interrupt(0) |
| ... | ... |
| 16 + N | External Interrupt(N) |

### B1.5.4 Exception priorities and preemption

In the ARMv6-M priority model, lower numbers take precedence. That is, the lower the assigned priority value, the higher the priority level. The priority order for exceptions with the same priority level is fixed, and is determined by their exception number.

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When multiple pending exceptions have the same priority number, the pending exception with the lowest exception number takes precedence. When an exception is active, only an exception with a higher priority can preempt it.

ARMv6-M supports 2-bit priority fields, providing four priority levels.

ARMv6-M Architecture Reference Manual[25]

[24] http://115.28.165.193/down/arm/arch/ARMv6-M_Architecture_Reference_Manual.pdf (last visited February 27, 2023).
[25] http://115.28.165.193/down/arm/arch/ARMv6-M_Architecture_Reference_Manual.pdf (last visited February 27, 2023).

**B1.5.4 Exception priorities and preemption**

In the ARMv6-M priority model, lower numbers take precedence. That is, the lower the assigned priority value, the higher the priority level. The priority order for exceptions with the same priority level is fixed, and is determined by their exception number.

Reset, NMI, and HardFault execute at fixed priorities of -3, -2, and -1 respectively. Software can set the priority of all other exceptions using registers in the SCS. A reset clears these software-configured priority settings. Software-assigned priority values start at 0, so Reset, NMI, and HardFault always have higher priorities than any other exception.

When multiple pending exceptions have the same priority number, the pending exception with the lowest exception number takes precedence. When an exception is active, only an exception with a higher priority can preempt it.

ARMv6-M supports 2-bit priority fields, providing four priority levels.

**Table B1-3 Exception numbers**

| Exception number | Exception |
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| 4-10 | Reserved |
| 11 | SVCall |
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| 14 | PendSV |
| 15 | SysTick, optional |
| 16 | External Interrupt(0) |
| ... | ... |
| 16 + N | External Interrupt(N) |

ARMv6-M Architecture Reference Manual[26]

***Indirect Infringement (Inducement – 35 U.S.C. § 271(b))***

55. In addition and/or in the alternative to its direct infringements, Renesas has indirectly infringed and continues to indirectly infringe one or more claims of the '749 Patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the '749 Accused Product.

56. At a minimum, Renesas has knowledge of the '749 Patent since being served with this Complaint. Renesas also has knowledge of the '749 Patent since receiving detailed correspondence from XTI prior to the filing of the Complaint, alerting Renesas to its infringements. Since receiving notice of its infringements, Renesas has actively induced the direct infringements of its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Indeed, Renesas has intended to cause, continues to intend to cause, and has taken, and continues to take affirmative steps to induce

[26] http://115.28.165.193/down/arm/arch/ARMv6-M_Architecture_Reference_Manual.pdf (last visited February 27, 2023).

infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the '749 Accused Products; creating and/or maintaining established distribution channels for the '749 Accused Products into and within the United States; manufacturing the '749 Accused Products in conformity with U.S. laws and regulations; distributing or making available videos, training, tools and resources supporting use of the '749 Accused Products that promote their features, specifications, and applications; providing technical documentation and tools for the '749 Accused Products, including white papers, brochures, and manuals; promoting the incorporation of the '749 Accused Products into end-user products through the development of Renesas' Partner programs; and by providing technical support and/or related services for these products to purchasers in the United States through Renesas' online support platforms including RenesasRulz forum further explaining how to use Renesas' products.[27]

***Damages***

57. On information and belief, despite having knowledge of the '749 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the '749 Patent, Renesas has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. Renesas' infringing activities relative to the '749 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, characteristic of a pirate, and an egregious case of misconduct beyond typical infringement such that XTI is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

[27] *See, e.g.*, https://www.renesas.com/us/en/products/microcontrollers-microprocessors/rz-mpus#featured_products (last visited October 7, 2022).

58. XTI has been damaged as a result of Renesas' infringing conduct described in this Count. Renesas is, thus, liable to XTI in an amount that adequately compensates XTI for Renesas' infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

**COUNT III**

(INFRINGEMENT OF U.S. PATENT NO. 8,125,565)

59. Plaintiff incorporates the preceding paragraphs herein by reference.

60. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

61. XTI is the owner of all substantial rights, title, and interest in and to the '565 Patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

62. The '565 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on February 28, 2012, after full and fair examination.

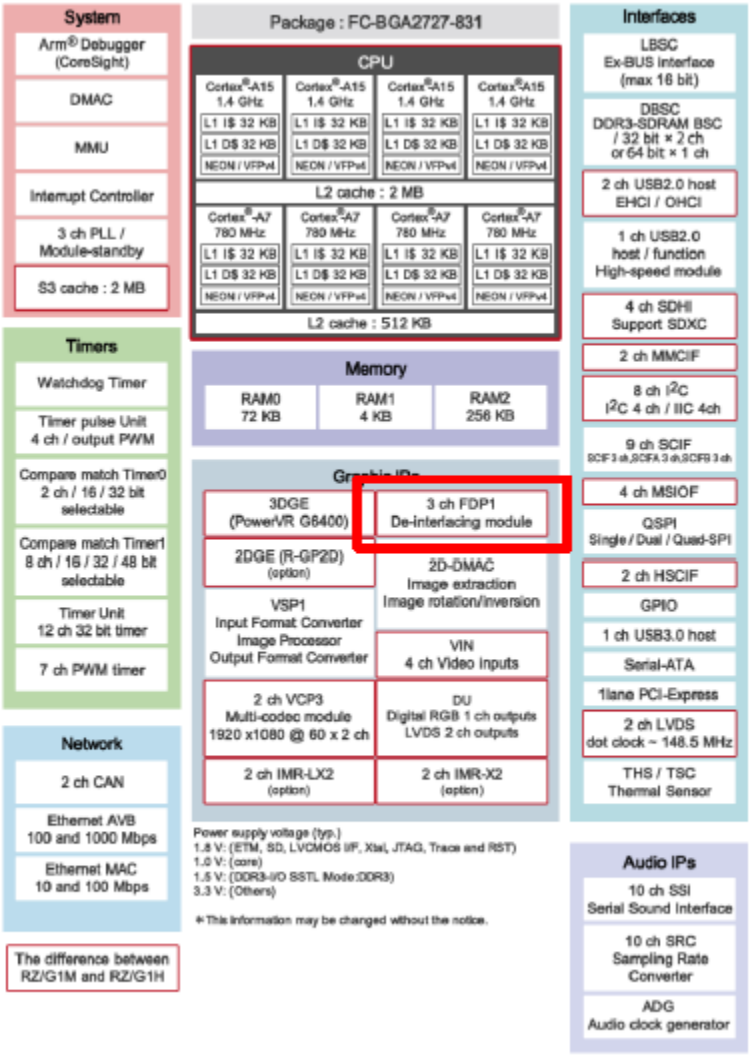
63. Renesas has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the '565 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, Renesas products, their components and processes, and/or products containing the same that incorporate the fundamental technologies covered by the '565 Patent, including, but not limited to, the Renesas RZ/G1 32-bit MPUs (collectively, the "'565 Accused Products").

***Direct Infringement (35 U.S.C. § 271(a))***

64. Renesas has directly infringed and continues to directly infringe one or more claims of the'565 Patent in this District and elsewhere in Texas and the United States.

65. Renesas has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 10 of the '565 Patent as set forth under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing, the '565 Accused Products. Furthermore, Renesas makes and sells the '565 Accused Products outside of the United States and either, delivers those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivers the '565 Accused Products outside of the United States, it does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the '565 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013). Furthermore, Renesas directly infringes the '565 Patent through its direct involvements in, and control of, the activities of its subsidiaries, including REA. Subject to Renesas' direction and control, such subsidiaries conduct activities that constitute direct infringement of the '565 Patent under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing '565 Accused Products. Renesas receives direct financial benefit from such infringements of its U.S.-based sales subsidiaries, including REA.

66. By way of illustration only, the '565 Accused Products include each and every element of claim 10 of the '565 Patent. The '575 Accused Products include an image processing circuit (red box) for generating an output frame (blue box) for example as indicated in the annotated block diagrams for the RZ/G1H below:




RZ/G1H Block Diagram

Renesas RZ/G1Ho Overview[28]

[28] *See* https://www.renesas.com/us/en/products/microcontrollers-microprocessors/rz-mpus/rzg1h-ultra-high-performancemicroprocessors-quad-core-arm-cortex-a15-and-quad-core-arm-cortex-a7-cpus-3d (last visited October 4, 2022).

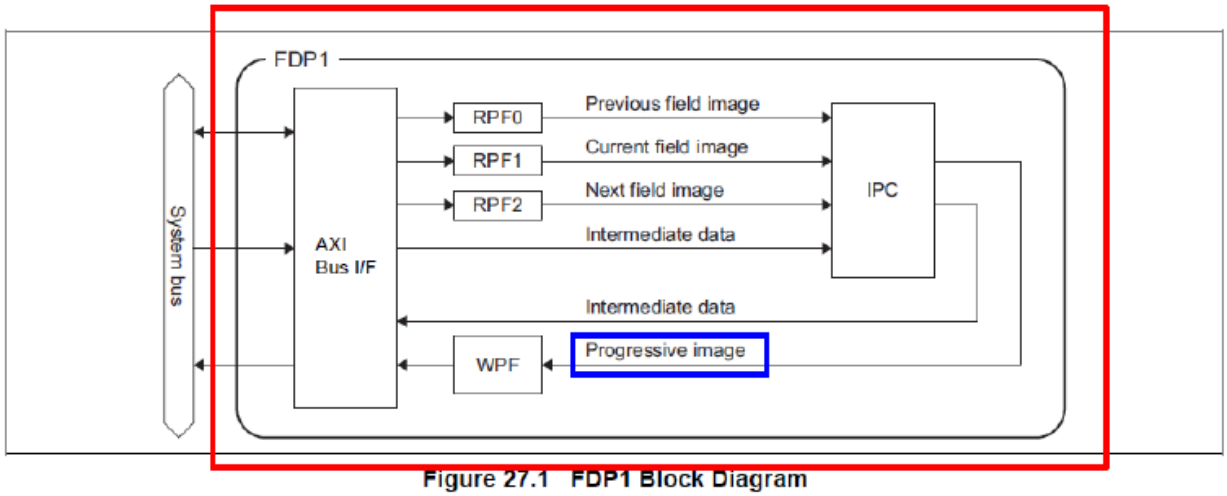



**Figure 27.1 FDP1 Block Diagram**

RZ/G Series User's Manual: Hardware[29]

67. The '565 Accused Products further include a memory unit for storing (red underline box) a first field, a second field, and a third field in time sequence (orange underline and box) as shown, for example in the annotated block diagram below for the for the RZ/G1H:

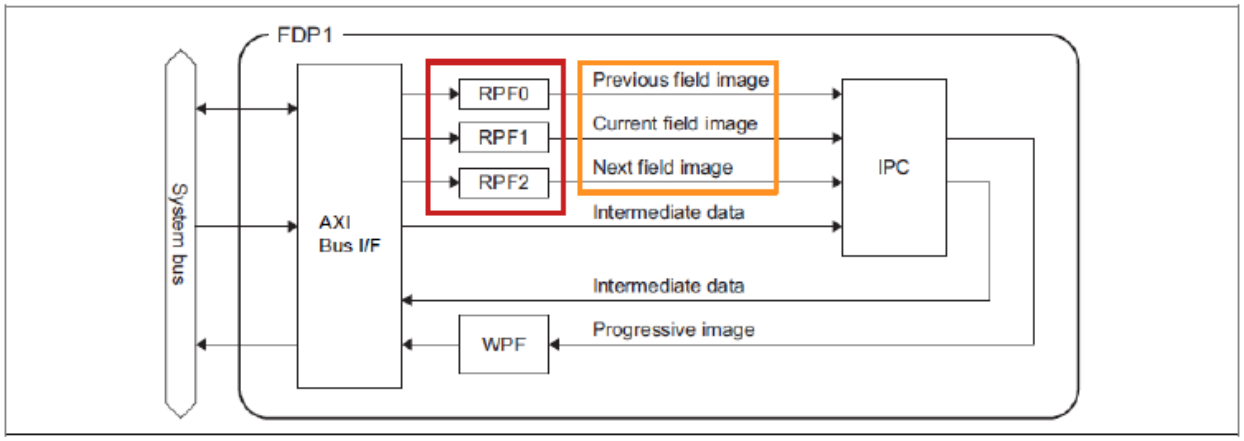



**Figure 27.1 FDP1 Block Diagram**

[29] *See* RZ/G Series User's Manual: Hardware, p.27 https://www.renesas.com/us/en/products/microcontrollers-microprocessors/rz-mpus/rzg1h-ultra-high-performance-microprocessors-quad-core-arm-cortex-a15-and-quad-core-arm-cortex-a7-cpus-3d (last visited October 4, 2022).

**(2) RPF (Read Pixel Formatter)**

The RPF reads image data from the external memory through the ABI, unpacks data according to the specified format, and outputs the resultant data to the IPC. The input format unpacking unit expands the image data input from the ABI into the image format for internal processing.

The FDP1 provides three RPF modules (RPF0 to RPF2). RPF0 reads the previous field, RPF1 reads the current field and RPF2 reads the next field for processing de-interlacing operation.

RZ/G Series User's Manual: Hardware[30]

68. The '565 Accused Products further include a de-interlacing unit for generating a de-interlaced frame (blue underline and arrow) according to the first field, the second field, and the third field (orange underline and box) as shown, for example in the annotated block diagram below for the for the RZ/G1H:

**(2) RPF (Read Pixel Formatter)**

The RPF reads image data from the external memory through the ABI, unpacks data according to the specified format, and outputs the resultant data to the IPC. The input format unpacking unit expands the image data input from the ABI into the image format for internal processing.

The FDP1 provides three RPF modules (RPF0 to RPF2). RPF0 reads the previous field, RPF1 reads the current field and RPF2 reads the next field for processing de-interlacing operation.

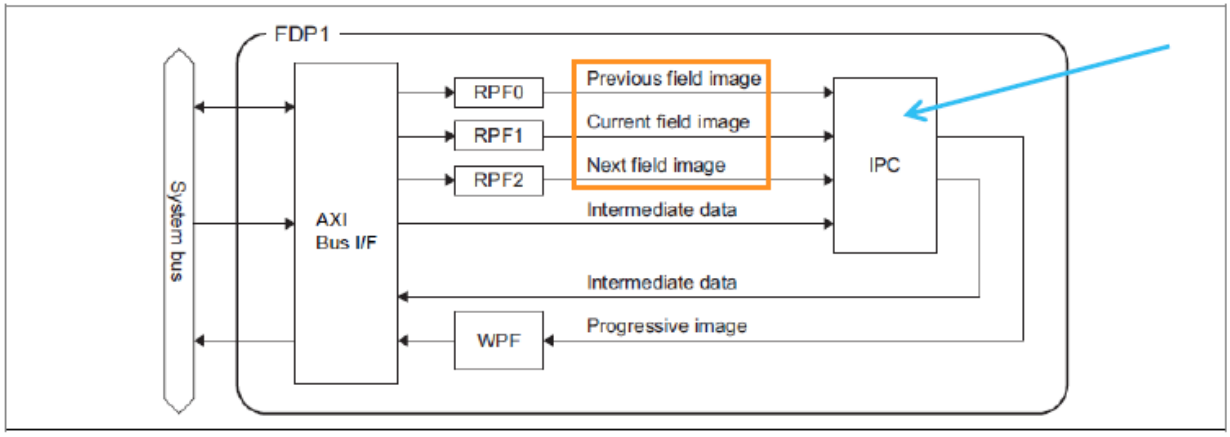



**Figure 27.1 FDP1 Block Diagram**

[30] *See* RZ/G Series User's Manual: Hardware, p.27-1 to 27-2 https://www.renesas.com/us/en/products/microcontrollers-microprocessors/rz-mpus/rzg1h-ultra-high-performance-microprocessors-quad-core-arm-cortex-a15-and-quad-core-arm-cortex-a7-cpus-3d (last visited October 4, 2022).

RZ/G Series User's Manual: Hardware[31]

**(3) IPC (Interlace to Progressive Converter)**

The IPC is the de-interlacing module which reads the field image through RPFn and writes back the progressive image to the external memory through WPF. The IPC uses the motion adaptive algorithm which enhances the image resolution of still pixels compared with conventional 2D de-interlacing.

Note: Only the luma component is used in the motion adaptive algorithm. The chroma components are still used in conventional 2D de-interlacing.

**Interlace to Progressive Converter (IPC)**

| | | | |
|---|---|---|---|
| De-interlacing | Mode | Frame rate | Equal rate (60i to 60p) |
| | | | Half rate (60i to 30p) |
| | | Interpolation (luma) | 2D-3D adaptive*2 |
| | | | 2D fixed |
| | | | 3D fixed*2 |
| | | Interpolation (chroma) | 2D fixed |
| | Algorithm | | Motion adaptive (luma only) |
| Diagonal line interpolation | | | Supported (luma only) |

Notes: 1. PL: Planar, SP: Semi-planar, ILV: Interleaved
2. Source picture structures (field-structure or frame-structure) should be the same structure among the all input pictures.
3. In processing by RPF0 and RPF2, the chroma components (Cb and Cr, or U and V) are not read from the system bus when the format is planar or semi-planar. The chroma components are discarded once they are read in combination with the luma components when the format is interleaved because the RPF0 and RPF2 only handle fixed 2D de-interlacing of the luma components, and so do not require the chroma components.

RZ/G Series User's Manual: Hardware[32]

69. The '565 Accused Products further include a motion interpolation unit for generating an interpolated frame (purple underline and arrow) according the first field, the second field, and the third field (orange underline and box) as shown, for example in the annotated block diagram below for the for the RZ/G1H:

[31] *See* RZ/G Series User's Manual: Hardware, p.27-1 to 27-2 https://www.renesas.com/us/en/products/microcontrollers-microprocessors/rz-mpus/rzg1h-ultra-high-performance-microprocessors-quad-core-arm-cortex-a15-and-quad-core-arm-cortex-a7-cpus-3d (last visited October 4, 2022).
[32] *See* RZ/G Series User's Manual: Hardware, p.27-2 to 27-4 https://www.renesas.com/us/en/products/microcontrollers-microprocessors/rz-mpus/rzg1h-ultra-high-performance-microprocessors-quad-core-arm-cortex-a15-and-quad-core-arm-cortex-a7-cpus-3d (last visited October 4, 2022).

**(2) RPF (Read Pixel Formatter)**

The RPF reads image data from the external memory through the ABI, unpacks data according to the specified format, and outputs the resultant data to the IPC. The input format unpacking unit expands the image data input from the ABI into the image format for internal processing.

The FDP1 provides three RPF modules (RPF0 to RPF2). RPF0 reads the previous field, RPF1 reads the current field and RPF2 reads the next field for processing de-interlacing operation.

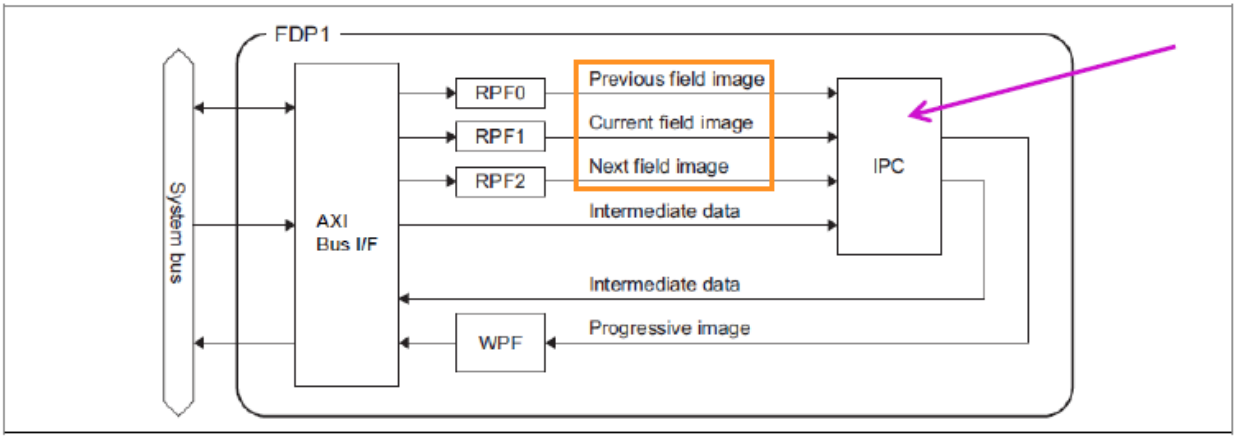



**Figure 27.1 FDP1 Block Diagram**

RZ/G Series User's Manual: Hardware[33]

[33] *See* RZ/G Series User's Manual: Hardware, p.27-1 to 27-2 https://www.renesas.com/us/en/products/microcontrollers-microprocessors/rz-mpus/rzg1h-ultra-high-performance-microprocessors-quad-core-arm-cortex-a15-and-quad-core-arm-cortex-a7-cpus-3d (last visited October 4, 2022).

**(3) IPC (Interlace to Progressive Converter)**

The IPC is the de-interlacing module which reads the field image through RPFn and writes back the progressive image to the external memory through WPF. The IPC uses the motion adaptive algorithm which enhances the image resolution of still pixels compared with conventional 2D de-interlacing.

Note: Only the luma component is used in the motion adaptive algorithm. The chroma components are still used in conventional 2D de-interlacing.

**Interlace to Progressive Converter (IPC)**

| | | | |
|---|---|---|---|
| De-interlacing | Mode | Frame rate | Equal rate (60i to 60p) |
| | | | Half rate (60i to 30p) |
| | | Interpolation (luma) | 2D-3D adaptive*2 |
| | | | 2D fixed |
| | | | 3D fixed*2 |
| | | Interpolation (chroma) | 2D fixed |
| | Algorithm | | Motion adaptive (luma only) |
| Diagonal line interpolation | | | Supported (luma only) |

Notes: 1. PL: Planar, SP: Semi-planar, ILV: Interleaved
2. Source picture structures (field-structure or frame-structure) should be the same structure among the all input pictures.
3. In processing by RPF0 and RPF2, the chroma components (Cb and Cr, or U and V) are not read from the system bus when the format is planar or semi-planar. The chroma components are discarded once they are read in combination with the luma components when the format is interleaved because the RPF0 and RPF2 only handle fixed 2D de-interlacing of the luma components, and so do not require the chroma components.

RZ/G Series User's Manual: Hardware[34]

70. The '565 Accused Products further include a frame processing unit for generating the output frame according to the de-Interlaced and the interpolated frame (aqua arrow and box) as shown, for example in the annotated block diagram below for the for the RZ/G1H:

[34] *See* RZ/G Series User's Manual: Hardware, p.27-2 to 27-4 https://www.renesas.com/us/en/products/microcontrollers-microprocessors/rz-mpus/rzg1h-ultra-high-performance-microprocessors-quad-core-arm-cortex-a15-and-quad-core-arm-cortex-a7-cpus-3d (last visited October 4, 2022).

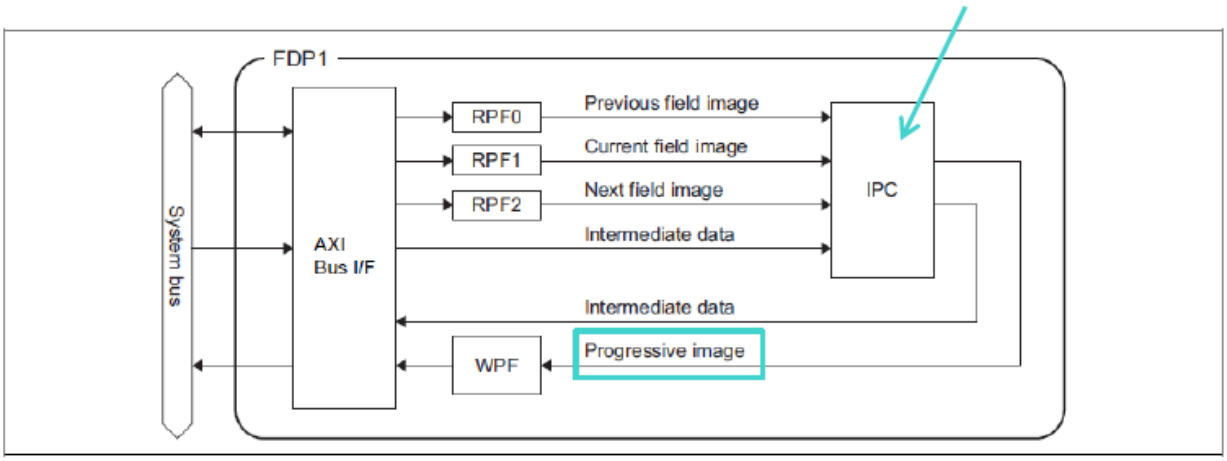



**Figure 27.1 FDP1 Block Diagram**

RZ/G Series User's Manual: Hardware[35]

***Indirect Infringement (Inducement – 35 U.S.C. § 271(b))***

71. In addition and/or in the alternative to its direct infringements, Renesas has indirectly infringed and continues to indirectly infringe one or more claims of the '565 Patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the '565 Accused Products.

72. At a minimum, Renesas has knowledge of the '565 Patent since being served with this Complaint. Renesas also has knowledge of the '565 Patent since receiving detailed correspondence from XTI prior to the filing of the Complaint, alerting Renesas to its infringements. Since receiving notice of its infringements, Renesas has actively induced the direct

[35] *See* RZ/G Series User's Manual: Hardware, p.27-1 to 27-2 https://www.renesas.com/us/en/products/microcontrollers-microprocessors/rz-mpus/rzg1h-ultra-high-performance-microprocessors-quad-core-arm-cortex-a15-and-quad-core-arm-cortex-a7-cpus-3d (last visited October 4, 2022).

infringements of its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Indeed, Renesas has intended to cause, continues to intend to cause, and has taken, and continues to take affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the '565 Accused Products; creating and/or maintaining established distribution channels for the '565 Accused Products into and within the United States; manufacturing the '565 Accused Products in conformity with U.S. laws and regulations; distributing or making available videos, training, tools and resources supporting use of the '565 Accused Products that promote their features, specifications, and applications; providing technical documentation and tools for the '565 Accused Products, including white papers, brochures, and manuals; promoting the incorporation of the '565 Accused Products into end-user products through the development of Renesas' Partner programs; and by providing technical support and/or related services for these products to purchasers in the United States through Renesas' online support platforms including RenesasRulz forum further explaining how to use Renesas' products.[36]

***Damages***

73. On information and belief, despite having knowledge of the '565 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the '565 Patent, Renesas has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. Renesas' infringing activities relative to the '565 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant,

[36] *See, e.g.*, https://www.renesas.com/us/en/products/microcontrollers-microprocessors/rz-mpus#featured_products (last visited October 7, 2022).

characteristic of a pirate, and an egregious case of misconduct beyond typical infringement such that XTI is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

74. XTI has been damaged as a result of Renesas' infringing conduct described in this Count. Renesas is, thus, liable to XTI in an amount that adequately compensates XTI for Renesas' infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

## COUNT IV

(INFRINGEMENT OF U.S. PATENT NO. 8,332,623)

75. Plaintiff incorporates the preceding paragraphs herein by reference.

76. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

77. XTI is the owner of all substantial rights, title, and interest in and to the '623 Patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

78. The '623 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on December 11, 2012, after full and fair examination.

79. Renesas has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the '623 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, Renesas products, their components and processes, and/or products containing the same that incorporate the fundamental technologies

covered by the '623 Patent, including, but not limited to, the Renesas RZ MPU Family (collectively, the "'623 Accused Products").[37]

***Direct Infringement (35 U.S.C. § 271(a))***

80. Renesas has directly infringed and continues to directly infringe one or more claims of the'623 Patent in this District and elsewhere in Texas and the United States.

81. Renesas has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 1 of the '623 Patent as set forth under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing, the '623 Accused Products. Furthermore, Renesas makes and sells the '623 Accused Products outside of the United States and either, delivers those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivers the '623 Accused Products outside of the United States, it does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the '623 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013). Furthermore, Renesas directly infringes the '623 Patent through its direct involvements in, and control of, the activities of its subsidiaries, including REA. Subject to Renesas' direction and control, such subsidiaries conduct activities that constitute direct infringement of the '623 Patent under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing '623 Accused Products. Renesas receives direct financial benefit from such infringements of its U.S.-based sales subsidiaries, including REA.

[37] **Renesas RZ MPU Family** – RZ/G1H, RZ/G2E, RZ/G2H, RZ/G2M, RZ/G2N, RZ/G1C, RZ/G1E, RZ/G1M & RZ/G1N.

82. By way of illustration only, the '623 Accused Products include each and every element of claim 1 of the '623 Patent.

83. The '623 Accused Products include "[a]n embedded electronic device, for downloading an initiation image from one of a plurality of initiation image source devices." For example, the '623 Accused Products comprise a boot memory, for storing a boot code (red underline) and a plurality of initiation image source sequence tables (green box) as shown below in the annotated excerpt of the RZ/G2L/C Group User's Manual:

## 4. Boot Mode

### 4.1 Overview

Once this LSI is released from the system reset state, the clock pulse generator (CPG) executes a specified sequence, and then Cortex-A55 Core 0 is started first to boot from the device selected according to the settings through the MD_BOOT2 to MD_BOOT0 pins. The values of the MD_BOOT2 to MD_BOOT0 pins are read once the LSI is released from the system reset state. After the LSI is booted up, the user program should enable or disable the operation of Cortex-A55 Core 0, Cortex-A55 Core 1, and Cortex-M33 as required.

Table 4.1 Selection of Boot Mode

| MD_BOOT2 to MD_BOOT0 | | | Boot Mode | Interface Module | Connected Device | Reference Section |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Boot mode 0 | SDHI0 | eSD (3.3 V at startup) | **4.2.1** |
| 0 | 0 | 1 | Boot mode 1 | SDHI0 | 1.8-V eMMC | **4.2.2** |
| 0 | 1 | 0 | Boot mode 2 | SDHI0 | 3.3-V eMMC | **4.2.3** |
| 0 | 1 | 1 | Boot mode 3 | SPIBSC | 1.8-V Single, Quad, or Octal serial flash memory | **4.2.4** |
| 1 | 0 | 0 | Boot mode 4 | SPIBSC | 3.3-V Single or Quad serial flash memory | **4.2.5** |
| 1 | 0 | 1 | Boot mode 5 | SCIF0 | Downloading through SCIF | **4.2.6** |
| 1 | 1 | 0 | Reserved | — | Reserved | — |
| 1 | 1 | 1 | Reserved | — | Reserved | — |

RZ/G2L/C Group User's Manual[38]

[38]RZ/G2L/C Group User's Manual, p.105, https://www.renesas.com/us/en/products/microcontrollers-microprocessors/rz-mpus/rzg2l-general-purpose-microprocessorsdual-core-arm-cortex-a55-12-ghz-cpus-and-single-core-arm-cortex-m33#document (last visited October 5, 2022).

84. The ’623 Accused Products further comprise a microprocessor (purple underline), for executing the boot code (orange underline) and downloading the initiation image (aqua box) according to one of the initiation image source sequence tables (blue underline), for example, as shown below in the annotated excerpt of the RZ/G2L/C Group User’s Manual:

## 4. Boot Mode

### 4.1 Overview

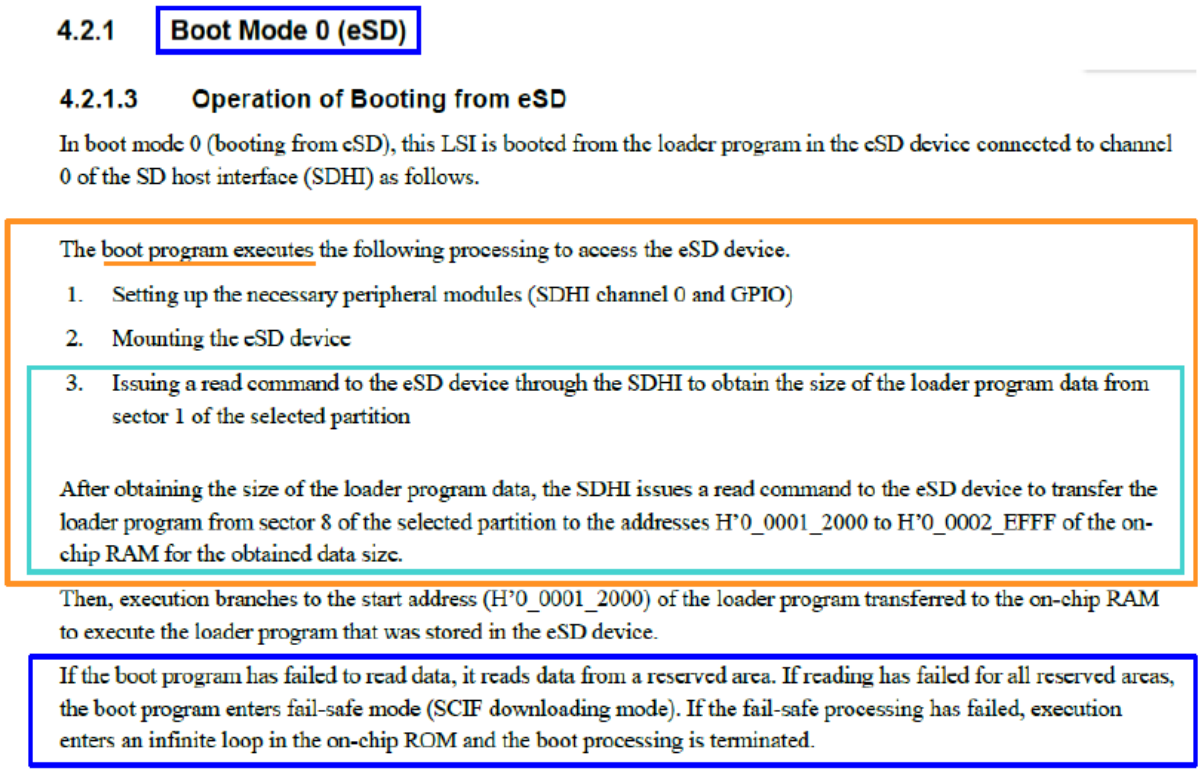
Once this LSI is released from the system reset state, the clock pulse generator (CPG) executes a specified sequence, and then Cortex-A55 Core 0 is started first to boot from the device selected according to the settings through the MD_BOOT2 to MD_BOOT0 pins. The values of the MD_BOOT2 to MD_BOOT0 pins are read once the LSI is released from the system reset state. After the LSI is booted up, the user program should enable or disable the operation of Cortex-A55 Core 0, Cortex-A55 Core 1, and Cortex-M33 as required.

Table 4.1 Selection of Boot Mode

| MD_BOOT2 to MD_BOOT0 | | | Boot Mode | Interface Module | Connected Device | Reference Section |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Boot mode 0 | SDHI0 | eSD (3.3 V at startup) | **4.2.1** |
| 0 | 0 | 1 | Boot mode 1 | SDHI0 | 1.8-V eMMC | **4.2.2** |
| 0 | 1 | 0 | Boot mode 2 | SDHI0 | 3.3-V eMMC | **4.2.3** |
| 0 | 1 | 1 | Boot mode 3 | SPIBSC | 1.8-V Single, Quad, or Octal serial flash memory | **4.2.4** |
| 1 | 0 | 0 | Boot mode 4 | SPIBSC | 3.3-V Single or Quad serial flash memory | **4.2.5** |
| 1 | 0 | 1 | Boot mode 5 | SCIF0 | Downloading through SCIF | **4.2.6** |
| 1 | 1 | 0 | Reserved | — | Reserved | — |
| 1 | 1 | 1 | Reserved | — | Reserved | — |

RZ/G2L/C Group User’s Manual[39]

[39]RZ/G2L/C Group User’s Manual, p.105, https://www.renesas.com/us/en/products/microcontrollers-microprocessors/rz-mpus/rzg2l-general-purpose-microprocessorsdual-core-arm-cortex-a55-12-ghz-cpus-and-single-core-arm-cortex-m33#document (last visited October 5, 2022).



4.2.1 Boot Mode 0 (eSD)

4.2.1.3 Operation of Booting from eSD

In boot mode 0 (booting from eSD), this LSI is booted from the loader program in the eSD device connected to channel 0 of the SD host interface (SDHI) as follows.

The boot program executes the following processing to access the eSD device.

1. Setting up the necessary peripheral modules (SDHI channel 0 and GPIO)
2. Mounting the eSD device
3. Issuing a read command to the eSD device through the SDHI to obtain the size of the loader program data from sector 1 of the selected partition

After obtaining the size of the loader program data, the SDHI issues a read command to the eSD device to transfer the loader program from sector 8 of the selected partition to the addresses H'0_0001_2000 to H'0_0002_EFFF of the on-chip RAM for the obtained data size.

Then, execution branches to the start address (H'0_0001_2000) of the loader program transferred to the on-chip RAM to execute the loader program that was stored in the eSD device.

If the boot program has failed to read data, it reads data from a reserved area. If reading has failed for all reserved areas, the boot program enters fail-safe mode (SCIF downloading mode). If the fail-safe processing has failed, execution enters an infinite loop in the on-chip ROM and the boot processing is terminated.

RZ/G2L/C Group User's Manual[40]

85. The '623 Accused Products further comprise a register, for storing (green underline and box) a status of an option pin (red underline), for example, as shown below in the annotated excerpt of the RZ/G2L/C Group User's Manual:

[40]RZ/G2L/C Group User's Manual, pp.106 & 108, https://www.renesas.com/us/en/products/microcontrollers-microprocessors/rz-mpus/rzg2l-general-purpose-microprocessorsdual-core-arm-cortex-a55-12-ghz-cpus-and-single-core-arm-cortex-m33#document (last visited October 5, 2022).

### 6.3.41 LSI Mode Signal Register (SYS_LSI_MODE)

This register indicates the state of the MD_BOOT terminal, the DEBUGEN terminal, the MD_CLKS terminal, and the MD_OSCDRV terminal.

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — |
| R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

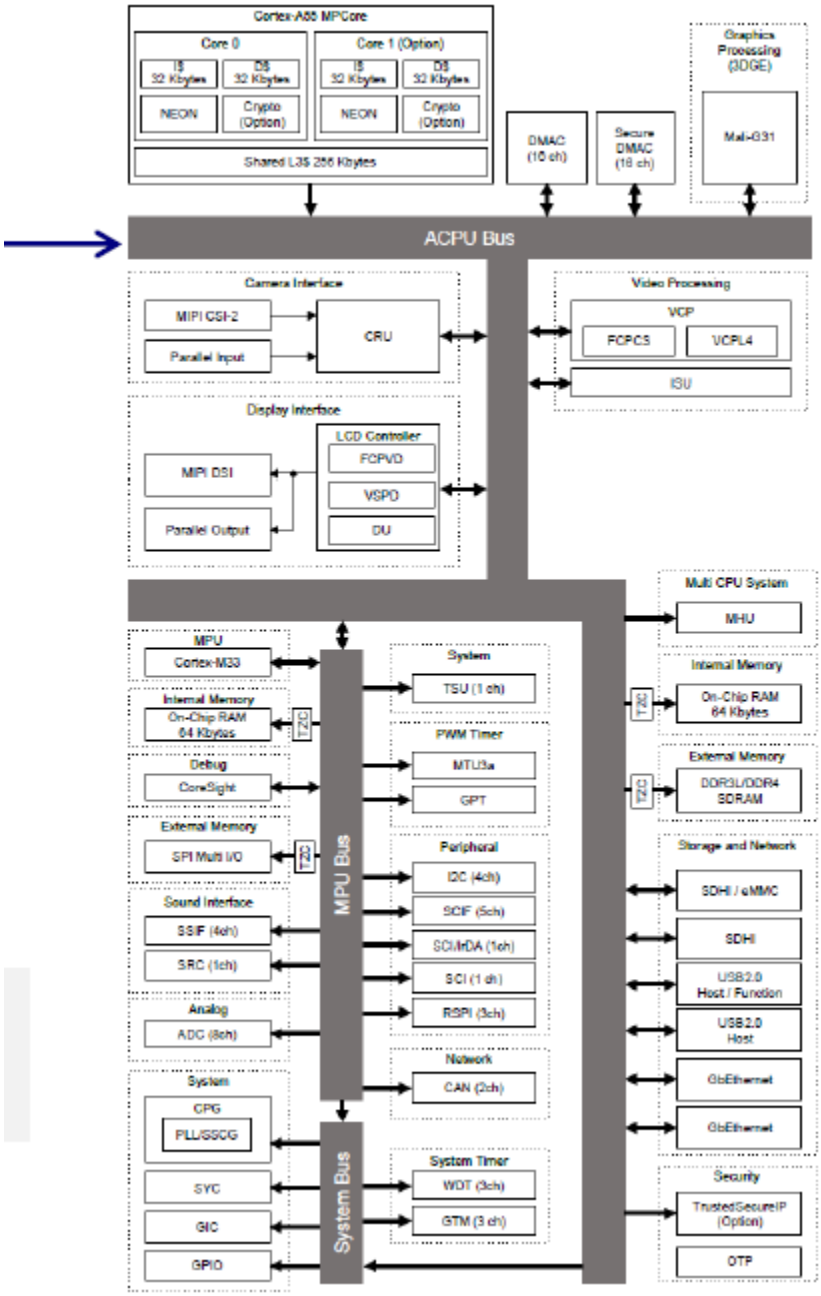
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | STAT_MD_OSCDRV[1:0] | | — | STAT_MD_CLKS | — | — | STAT_DEBUGEN | — | — | — | — | — | — | STAT_MD_BOOT[2:0] | | |
| Initial Value | — | — | 0 | — | 0 | 0 | — | 0 | 0 | 0 | 0 | 0 | 0 | — | — | — |
| R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

| | | | | |
|---|---|---|---|---|
| 2 to 0 | STAT_MD_BOOT[2:0] | — | R | Indicates the terminal state of the external terminal MD_BOOT[2:0].<br>The value is updated at the rising edge of PRST#.<br>If a reset occurs inside the LSI, this register is not updated. |

RZ/G2L/C Group User's Manual[41]

86. The '623 Accused Products further comprise a bus, coupled to the boot memory, the microprocessor, and the register, for transmitting data between the boot memory, the microprocessor, and the register (blue arrow), for example, as shown below in the annotated excerpt of the RZ/G2L/C Group User's Manual:

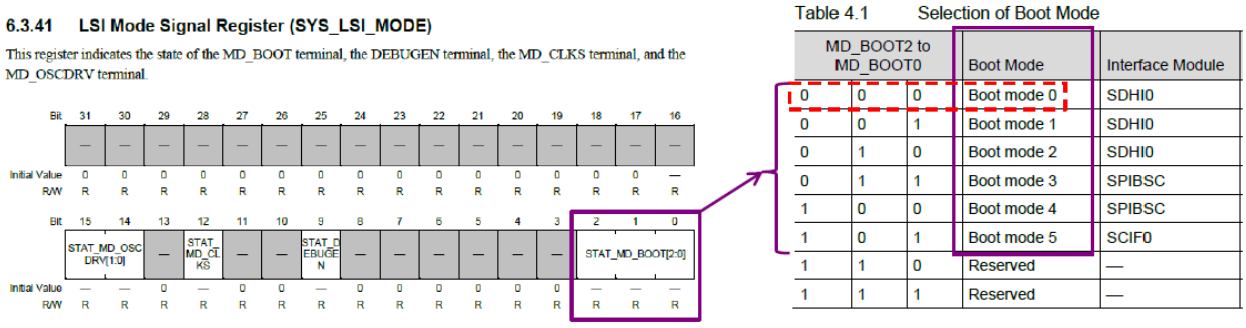
[41] RZ/G2L/C Group User's Manual, pp.203 & 167, https://www.renesas.com/us/en/products/microcontrollers-microprocessors/rz-mpus/rzg2l-general-purpose-microprocessorsdual-core-arm-cortex-a55-12-ghz-cpus-and-single-core-arm-cortex-m33#document (last visited October 5, 2022).




RZ/G2L/C Group User's Manual[42]

[42]RZ/G2L/C Group User's Manual, p.141, https://www.renesas.com/us/en/products/microcontrollers-microprocessors/rz-mpus/rzg2l-general-purpose-microprocessorsdual-core-arm-cortex-a55-12-ghz-cpus-and-single-core-arm-cortex-m33#document (last visited October 5, 2022).

87. In the '623 Accused Products, the initiation image source sequence table is selected according to the status stored in the register (purple boxes), and the sequence of the initiation image source devices accessed by the microprocessor is determined according to the initiation image source sequence table (dashed red box), for example, as shown below in the annotated excerpt of the RZ/G2L/C Group User's Manual:



**6.3.41 LSI Mode Signal Register (SYS_LSI_MODE)**

This register indicates the state of the MD_BOOT terminal, the DEBUGEN terminal, the MD_CLKS terminal, and the MD_OSCDRV terminal.

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — |
| R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | STAT_MD_OSCDRV[1:0] | | — | STAT_MD_CLKS | — | — | STAT_DEBUGEN | — | — | — | — | — | — | STAT_MD_BOOT[2:0] | | |
| Initial Value | — | — | 0 | — | 0 | 0 | — | 0 | 0 | 0 | 0 | 0 | 0 | — | — | — |
| R/W | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

Table 4.1 Selection of Boot Mode

| MD_BOOT2 to MD_BOOT0 | | | Boot Mode | Interface Module |
|---|---|---|---|---|
| 0 | 0 | 0 | Boot mode 0 | SDHI0 |
| 0 | 0 | 1 | Boot mode 1 | SDHI0 |
| 0 | 1 | 0 | Boot mode 2 | SDHI0 |
| 0 | 1 | 1 | Boot mode 3 | SPIBSC |
| 1 | 0 | 0 | Boot mode 4 | SPIBSC |
| 1 | 0 | 1 | Boot mode 5 | SCIF0 |
| 1 | 1 | 0 | Reserved | — |
| 1 | 1 | 1 | Reserved | — |

RZ/G2L/C Group User's Manual[43]

[43]RZ/G2L/C Group User's Manual, pp.105 & 203, https://www.renesas.com/us/en/products/microcontrollers-microprocessors/rz-mpus/rzg2l-general-purpose-microprocessorsdual-core-arm-cortex-a55-12-ghz-cpus-and-single-core-arm-cortex-m33#document (last visited October 5, 2022).

### 4.2.1 Boot Mode 0 (eSD)

#### 4.2.1.3 Operation of Booting from eSD

In boot mode 0 (booting from eSD), this LSI is booted from the loader program in the eSD device connected to channel 0 of the SD host interface (SDHI) as follows.

The boot program executes the following processing to access the eSD device.

1. Setting up the necessary peripheral modules (SDHI channel 0 and GPIO)
2. Mounting the eSD device
3. Issuing a read command to the eSD device through the SDHI to obtain the size of the loader program data from sector 1 of the selected partition

After obtaining the size of the loader program data, the SDHI issues a read command to the eSD device to transfer the loader program from sector 8 of the selected partition to the addresses H'0_0001_2000 to H'0_0002_EFFF of the on-chip RAM for the obtained data size.

Then, execution branches to the start address (H'0_0001_2000) of the loader program transferred to the on-chip RAM to execute the loader program that was stored in the eSD device.

If the boot program has failed to read data, it reads data from a reserved area. If reading has failed for all reserved areas, the boot program enters fail-safe mode (SCIF downloading mode). If the fail-safe processing has failed, execution enters an infinite loop in the on-chip ROM and the boot processing is terminated.

RZ/G2L/C Group User's Manual[44]

***Indirect Infringement (Inducement – 35 U.S.C. § 271(b))***

88. In addition and/or in the alternative to its direct infringements, Renesas has indirectly infringed and continues to indirectly infringe one or more claims of the '623 Patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the '623 Accused Product.

[44]RZ/G2L/C Group User's Manual, pp.106 & 108, https://www.renesas.com/us/en/products/microcontrollers-microprocessors/rz-mpus/rzg2l-general-purpose-microprocessorsdual-core-arm-cortex-a55-12-ghz-cpus-and-single-core-arm-cortex-m33#document (last visited October 5, 2022).

89. At a minimum, Renesas has knowledge of the '623 Patent since being served with this Complaint. Renesas also has knowledge of the '623 Patent since receiving detailed correspondence from XTI prior to the filing of the Complaint, alerting Renesas to its infringements. Since receiving notice of its infringements, Renesas has actively induced the direct infringements of its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Indeed, Renesas has intended to cause, continues to intend to cause, and has taken, and continues to take affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the '623 Accused Products; creating and/or maintaining established distribution channels for the '623 Accused Products into and within the United States; manufacturing the '623 Accused Products in conformity with U.S. laws and regulations; distributing or making available videos, training, tools and resources supporting use of the '623 Accused Products that promote their features, specifications, and applications; providing technical documentation and tools for the '623 Accused Products, including white papers, brochures, and manuals; promoting the incorporation of the '623 Accused Products into end-user products through the development of Renesas' Partner programs; and by providing technical support and/or related services for these products to purchasers in the United States through Renesas' online support platforms including RenesasRulz forum further explaining how to use Renesas' products.[45]

[45] *See, e.g.*, https://www.renesas.com/us/en/products/microcontrollers-microprocessors/rz-mpus#featured_products (last visited October 7, 2022).

***Damages***

90. On information and belief, despite having knowledge of the '623 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the '623 Patent, Renesas has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. Renesas' infringing activities relative to the '623 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant, characteristic of a pirate, and an egregious case of misconduct beyond typical infringement such that XTI is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

91. XTI has been damaged as a result of Renesas' infringing conduct described in this Count. Renesas is, thus, liable to XTI in an amount that adequately compensates XTI for Renesas' infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

**COUNT V**

(INFRINGEMENT OF U.S. PATENT NO. 9,166,475)

92. Plaintiff incorporates the preceding paragraphs herein by reference.

93. This cause of action arises under the patent laws of the United States, and, in particular, 35 U.S.C. §§ 271, *et seq*.

94. XTI is the owner of all substantial rights, title, and interest in and to the '475 Patent including the right to exclude others and to enforce, sue, and recover damages for past and future infringements.

95. The '475 Patent is valid, enforceable, and was duly and legally issued by the United States Patent and Trademark Office on October 20, 2015, after full and fair examination.

96. Renesas has and continues to directly and/or indirectly infringe (by inducing infringement) one or more claims of the ’475 Patent in this District and elsewhere in Texas and the United States by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, Renesas products, their components and processes, and/or products containing the same that incorporate the fundamental technologies covered by the ’475 Patent, including, but not limited to, the Renesas RAA23022x DC/DC Converters (collectively, the “’475 Accused Products”).

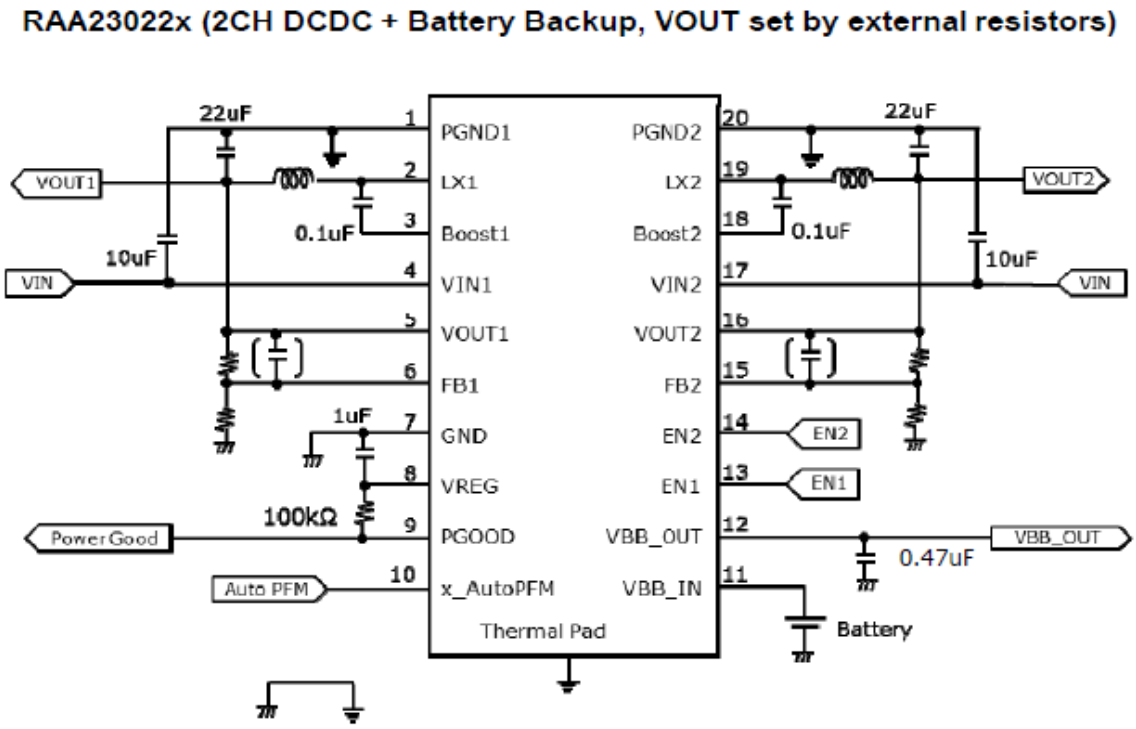
***Direct Infringement (35 U.S.C. § 271(a))***

97. Renesas has directly infringed and continues to directly infringe one or more claims of the ’475 Patent in this District and elsewhere in Texas and the United States.

98. Renesas has directly infringed and continues to directly infringe, either by itself or via its agent(s), at least Claim 1 of the ’475 Patent as set forth under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing, the ’475 Accused Products. Furthermore, Renesas makes and sells the ’475 Accused Products outside of the United States and either, delivers those products to its customers, distributors, and/or subsidiaries in the United States, or, in the case that it delivers the ’475 Accused Products outside of the United States, it does so intending and/or knowing that those products are destined for the United States and/or designed and designated for sale in the United States, thereby directly infringing the ’475 Patent. *See, e.g., Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013). Furthermore, Renesas directly infringes the ’475 Patent through its direct involvements in, and control of, the activities of its subsidiaries, including REA. Subject to Renesas’ direction and control, such subsidiaries conduct activities that constitute direct infringement of the ’475 Patent under 35 U.S.C. § 271(a) by making, offering for sale, selling, and/or importing ’475 Accused

Products. Renesas receives direct financial benefit from such infringements of its U.S.-based sales subsidiaries, including REA.

99. By way of illustration only, the '475 Accused Products include each and every element of claim 1 of the '475 Patent. The '642 Accused Products comprise "[a] switching regulator, configured to control a supply of power from a power source to a power load," for example, as shown in the diagram below for the RAA23033x DC/DC converter:

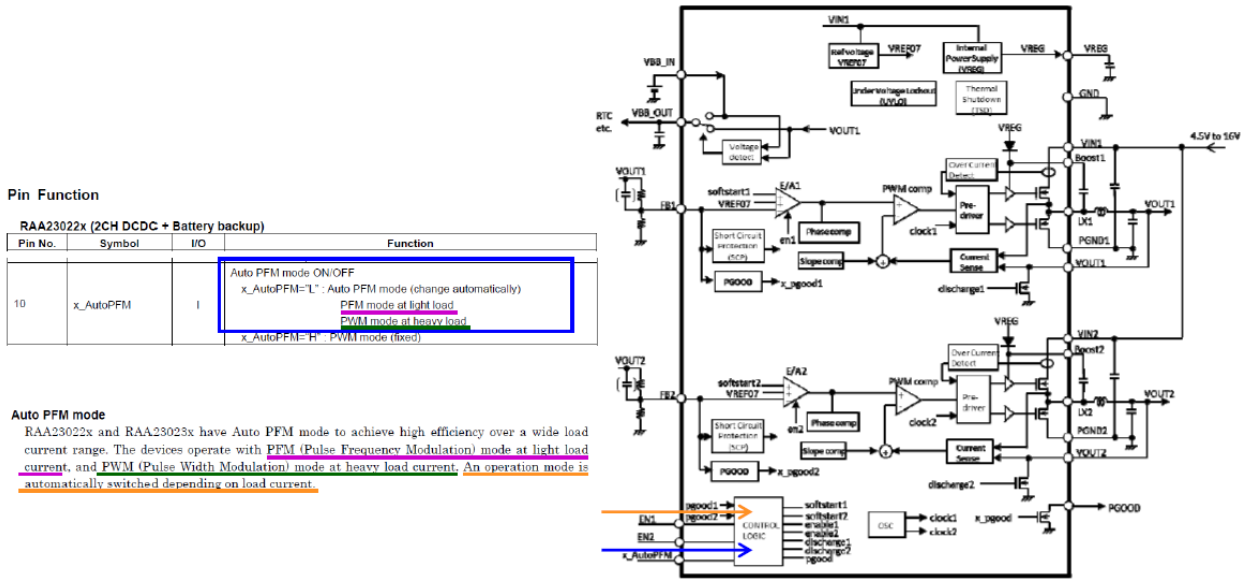



RAA23033x Datasheet[46]

100. The '475 Accused Products further comprise a control configuration select unit (blue box and arrow), for selecting between a high power mode (green underline) and a low power mode (purple underline) in response to a control signal which depends on a state of the power load,

[46] RAA23033x Datasheet, p.3, https://www.renesas.com/us/en/document/dst/raa23022x-raa23023x-datasheet?language=en&r=529721 (last visited October 7, 2022).

the control signal being received from a controller associated with the power load (orange underline and arrow), for example, as shown in the annotated sections below from the datasheet for the RAA23033x DC/DC converter:



Pin Function

RAA23022x (2CH DCDC + Battery backup)

| Pin No. | Symbol | I/O | Function |
|---|---|---|---|
| 10 | x_AutoPFM | I | Auto PFM mode ON/OFF<br>x_AutoPFM="L" : Auto PFM mode (change automatically)<br>PFM mode at light load<br>PWM mode at heavy load<br>x_AutoPFM="H" : PWM mode (fixed) |

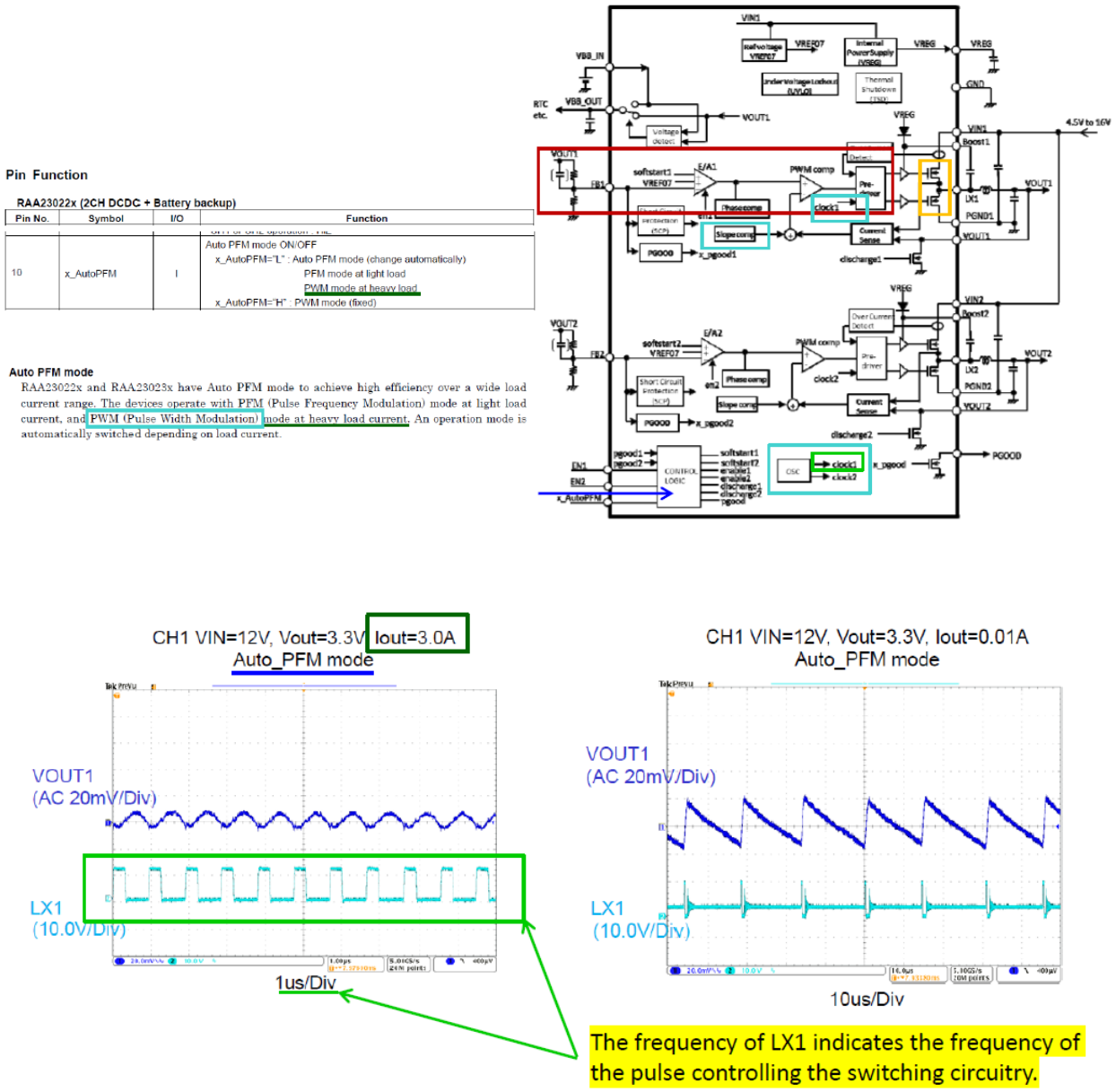
**Auto PFM mode**

RAA23022x and RAA23023x have Auto PFM mode to achieve high efficiency over a wide load current range. The devices operate with PFM (Pulse Frequency Modulation) mode at light load current, and PWM (Pulse Width Modulation) mode at heavy load current. An operation mode is automatically switched depending on load current.

RAA23033x Datasheet[47]

101. The '475 Accused Products further comprise a first control unit (aqua box), enabled by the control configuration select unit (blue arrow and underline) when selecting the high power mode (dark green underline and box), the first control unit comprising a fast clock (light green box) that is configured to drive a pulse control unit (red box) to deliver pulses to switching circuitry (orange box), for example, as shown in the annotated sections below from the datasheet for the RAA23033x DC/DC converter:

[47] RAA23033x Datasheet, pp.4, 6, & 16, https://www.renesas.com/us/en/document/dst/raa23022x-raa23023x-datasheet?language=en&r=529721 (last visited October 7, 2022).




RAA23033x Datasheet[48]

102. The '475 Accused Products further comprise a second control unit (dark purple box), enabled by the control configuration select unit (blue box) when selecting the low power mode (light purple underline and box), the second control unit comprising a slow clock (dashed

[48] RAA23033x Datasheet, pp.4, 6, 12 & 16, https://www.renesas.com/us/en/document/dst/raa23022x-raa23023x-datasheet?language=en&r=529721 (last visited October 7, 2022).

red box), wherein a frequency of the slow clock is lower than a frequency of the fast clock (dashed blue box), the slow clock configured to cause the switching circuitry to switch at a lower rate than the fast clock, for example, as shown in the annotated sections below from the datasheet for the RAA23033x DC/DC converter:

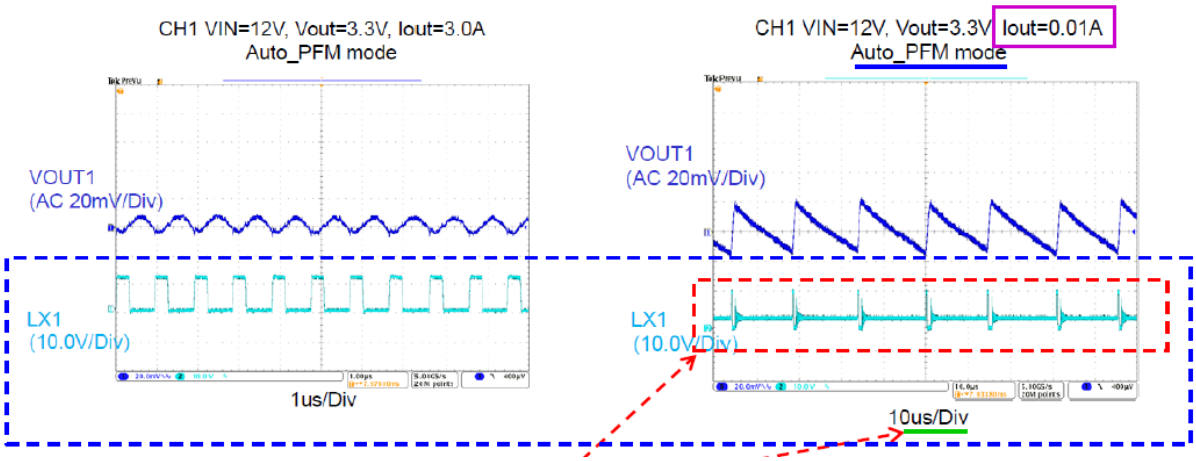
**Pin Function**

**RAA23022x (2CH DCDC + Battery backup)**

| Pin No. | Symbol | I/O | Function |
|---|---|---|---|
| 10 | x_AutoPFM | I | Auto PFM mode ON/OFF<br>x_AutoPFM="L" : Auto PFM mode (change automatically)<br>PFM mode at light load<br>PWM mode at heavy load<br>x_AutoPFM="H" : PWM mode (fixed) |

**Auto PFM mode**

RAA23022x and RAA23023x have Auto PFM mode to achieve high efficiency over a wide load current range. The devices operate with PFM (Pulse Frequency Modulation) mode at light load current, and PWM (Pulse Width Modulation) mode at heavy load current. An operation mode is automatically switched depending on load current.




RAA23033x Datasheet[49]

103. In the '475 Accused Products, the first control unit is enabled the second control unit is disabled, and when the second control unit is enabled the first control unit is disabled (dashed green underline and box), for example, as shown in the annotated sections below from the datasheet for the RAA23033x DC/DC converter:

[49] RAA23033x Datasheet, pp.6, 12 & 16, https://www.renesas.com/us/en/document/dst/raa23022x-raa23023x-datasheet?language=en&r=529721 (last visited October 7, 2022).

**Pin Function**

**RAA23022x (2CH DCDC + Battery backup)**

| Pin No. | Symbol | I/O | Function |
|---|---|---|---|
| 10 | x_AutoPFM | I | Auto PFM mode ON/OFF<br>x_AutoPFM="L" : Auto PFM mode (change automatically)<br>PFM mode at light load<br>PWM mode at heavy load<br>x_AutoPFM="H" : PWM mode (fixed) |

**Auto PFM mode**

RAA23022x and RAA23023x have Auto PFM mode to achieve high efficiency over a wide load current range. The devices operate with PFM (Pulse Frequency Modulation) mode at light load current, and PWM (Pulse Width Modulation) mode at heavy load current. An operation mode is automatically switched depending on load current.

RAA23033x Datasheet[50]

***Indirect Infringement (Inducement – 35 U.S.C. § 271(b))***

104. In addition and/or in the alternative to its direct infringements, Renesas has indirectly infringed and continues to indirectly infringe one or more claims of the '475 Patent by knowingly and intentionally inducing others, including its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers, to directly infringe by making, using, offering to sell, selling and/or importing into the United States the '475 Accused Products.

105. At a minimum, Renesas has knowledge of the '475 Patent since being served with this Complaint. Renesas also has knowledge of the '475 Patent since receiving detailed correspondence from XTI prior to the filing of the Complaint, alerting Renesas to its infringements. Since receiving notice of its infringements, Renesas has actively induced the direct

[50] RAA23033x Datasheet, pp.6 & 16, https://www.renesas.com/us/en/document/dst/raa23022x-raa23023x-datasheet?language=en&r=529721 (last visited October 7, 2022).

infringements of its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, importers, customers, and/or consumers as set forth under U.S.C. § 271(b). Indeed, Renesas has intended to cause, continues to intend to cause, and has taken, and continues to take affirmative steps to induce infringement by, among other things, creating and disseminating advertisements and instructive materials that promote the infringing use of the '475 Accused Products; creating and/or maintaining established distribution channels for the '475 Accused Products into and within the United States; manufacturing the '475 Accused Products in conformity with U.S. laws and regulations; distributing or making available videos, training, tools and resources supporting use of the '475 Accused Products that promote their features, specifications, and applications; providing technical documentation and tools for the '475 Accused Products, including white papers, brochures, and manuals; promoting the incorporation of the '475 Accused Products into end-user products through the development of Renesas' Partner programs; and by providing technical support and/or related services for these products to purchasers in the United States through Renesas' online support platforms including RenesasRulz forum further explaining how to use Renesas' products.[51]

***Damages***

106. On information and belief, despite having knowledge of the '475 Patent and knowledge that it is directly and/or indirectly infringing one or more claims of the '475 Patent, Renesas has nevertheless continued its infringing conduct and disregarded an objectively high likelihood of infringement. Renesas' infringing activities relative to the '475 Patent have been, and continue to be, willful, wanton, malicious, in bad-faith, deliberate, consciously wrongful, flagrant,

[51] *See, e.g.*, https://www.renesas.com/us/en/products/power-power-management/dc-dc-converters/step-down-buck/buck-regulators-integrated-fets/raa230231gsb-16v-input-3a-dual-step-down-dcdc-converter-battery-backup (last visited October 7, 2022).

characteristic of a pirate, and an egregious case of misconduct beyond typical infringement such that XTI is entitled to enhanced damages under 35 U.S.C. § 284 up to three times the amount found or assessed.

107. XTI has been damaged as a result of Renesas' infringing conduct described in this Count. Renesas is, thus, liable to XTI in an amount that adequately compensates XTI for Renesas' infringements, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

## CONCLUSION

108. XTI is entitled to recover from Renesas the damages sustained by XTI as a result of Renesas' wrongful acts, and willful infringements, in an amount subject to proof at trial, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court.

109. XTI has incurred and will incur attorneys' fees, costs, and expenses in the prosecution of this action. The circumstances of this dispute may give rise to an exceptional case within the meaning of 35 U.S.C. § 285, and XTI is entitled to recover its reasonable and necessary attorneys' fees, costs, and expenses.

## JURY DEMAND

110. XTI hereby requests a trial by jury pursuant to Rule 38 of the Federal Rules of Civil Procedure.

## PRAYER FOR RELIEF

111. XTI respectfully requests that the Court find in its favor and against Renesas, and that the Court grant XTI the following relief:

(i) A judgment that one or more claims of the Asserted Patents have been infringed, either literally and/or under the doctrine of equivalents, by Renesas;

(ii) A judgment that one or more claims of the Asserted Patents have been willfully infringed, either literally and/or under the doctrine of equivalents, by Renesas;

(iii) A judgment that Renesas account for and pay to XTI all damages and costs incurred by Plaintiff because of Renesas's infringing activities and other conduct complained of herein, including an accounting for any sales or damages not presented at trial;

(iv) A judgment that Renesas account for and pay to XTI a reasonable, ongoing, post judgment royalty because of Renesas's infringing activities, including continuing infringing activities, and other conduct complained of herein;

(v) A judgment that XTI be granted pre-judgment and post judgment interest on the damages caused by Renesas's infringing activities and other conduct complained of herein;

(vi) A judgment that this case is exceptional under the provisions of 35 U.S.C. § 285 and award enhanced damages; and

(vii) Such other and further relief as the Court deems just and equitable.

Dated: March 6, 2023

Respectfully submitted,

*/s/ Edward R. Nelson III*
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