UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

INTELLECTUAL VENTURES I LLC and INTELLECTUAL VENTURES II LLC, Plaintiff, v. ZEBRA TECHNOLOGIES CORPORATION, Defendant.	Civil Action No. 6:23-cv-292 **JURY TRIAL DEMANDED**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiffs, Intellectual Ventures I ("Intellectual Ventures I") and Intellectual Ventures II LLC ("Intellectual Ventures II") (together "IV"), for its complaint against Defendant Zebra Technologies Corporation ("Zebra") hereby allege:

THE PARTIES

1. Intellectual Ventures I is a Delaware limited liability company having its principal place of business located at 3150 139th Avenue SE, Bellevue, Washington 98005.

2. Intellectual Ventures II is a Delaware limited liability company having its principal place of business located at 3150 139th Avenue SE, Bellevue, Washington 98005.

3. Upon information and belief, Zebra is a Delaware corporation having its principal place of business located at 3 Overlook Point, Lincolnshire, Illinois 60069.

4. Upon information and belief, Zebra also has a principal place of business at 507 E. Howard Lane, Bldg 1, Austin, Texas 78753.

5. Upon information and belief, Zebra can be served with process through its registered agent, located at 350 N. St. Paul St., Dallas, Texas 75201.

NATURE OF THE ACTION, JURISDICTION, AND VENUE

6. IV brings this action for patent infringement pursuant to 35 U.S.C. § 271, *et seq.* This Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

7. This Court has general jurisdiction over Zebra because Zebra is engaged in substantial and not isolated activity at its regular and established places of business within this judicial district. This Court has specific jurisdiction over Zebra because Zebra has committed acts of infringement giving rise to this action within this judicial district and has established more than minimum contacts within this judicial district, such that the exercise of jurisdiction over Zebra in this Court would not offend traditional notions of fair play and substantial justice.

8. Venue is proper in this District under 28 U.S.C. §§ 1391(b)-(c) and 1400(b) because Zebra maintains regular and established places of business and has committed acts of patent infringement within this judicial district.

FACTUAL BACKGROUND

9. Intellectual Ventures Management, LLC ("Intellectual Ventures") was founded in 2000. Intellectual Ventures fosters inventions and facilitates the filing of patent applications for those inventions; collaborates with others to develop and patent inventions; and acquires and licenses patents from individual inventors, universities, corporations, and other institutions. A significant aspect of Intellectual Ventures' business is managing the plaintiffs in this case, Intellectual Ventures I and Intellectual Ventures II.

10. One founder of Intellectual Ventures is Nathan Myhrvold, who worked at Microsoft from 1986 until 2000 in a variety of executive positions, culminating in his appointment as the

company's first Chief Technology Officer ("CTO") in 1996. While at Microsoft, Dr. Myhrvold founded Microsoft Research in 1991 and was one of the world's foremost software experts. Between 1986 and 2000, Microsoft became the world's largest technology company.

11. Under Dr. Myhrvold's leadership, Intellectual Ventures acquired thousands of patents covering many important inventions of the Internet era, including many pertaining to the networked computers that comprise the Internet. Many of these inventions coincided with Dr. Myhrvold's successful tenure at Microsoft.

Cyclic Diversity

12. A further area of importance in today's computing environments is that as wireless communications systems are widely deployed to provide various types of communications, demand for increased data rates has skyrocketed. This has led wireless system providers to develop new techniques for increasing data rates within the limited available radio frequency (RF) spectrum. One of these advancements has been the use of orthogonal frequency division multiplexing (OFDM) transmission. In OFDM transmissions, a radio channel is divided into a large number of closely spaced subchannels, an outgoing bitstream representing data to be transmitted is divided into multiple sub-bitstreams, and each sub-bitstream is transmitted over a subchannel in parallel with other sub-bitstreams that are each transmitted over their respective subchannels. Each such sub-bitstream is comprised of a series of symbols, that is, a waveform of the communication channel that persists for a fixed period of time, and from which data can be extracted by taking samples (i.e., measuring segments) of that waveform. Each of the symbols is separated by a guard interval (a gap in time between successive symbols that provides a buffer making transmission channels more resilient against the effects of a multipath propagation). The

main advantages of OFDM is its ability to cope with severe channel conditions (e.g., signal fading, echoes, and interference).

13. As technology continued to advance, demand for increased speed and reduced interference resulted in the implementation of further improvements such as using multiple antennas in a single device, sometimes referred to as multiple input, multiple output (MIMO), which enables simultaneous or substantially simultaneous transmission of multiple bitstreams/sub-bitstreams in the same RF spectrum. When combined with OFDM, MIMO increases speed and improves reliability, however, it also introduces challenges, particularly when a multi-antenna MIMO enabled transmitter is communicating with a single antenna single input, single output (SISO), receiver device. For example, signals transmitted from the MIMO transmitter may follow direct paths and multipaths to the SIS receiver, which can result in constructive interference (when multiple signals interact with one another to increase their amplitudes) or destructive interference (when multiple signals interact with one another to decrease their amplitudes), thus increasing packet error rates and causing other unwanted behavior that degraded the network quality.

14. One way that prior art systems addressed these inefficiencies was by implementing linear diversity schemes in which the transmission of one signal from a MIMO system is delayed relative to another signal from the MIMO system. Linear diversity schemes tend to reduce constructive and destructive interference by temporally decorrelating the transmissions of two signals, but they resulted in other problems such as one of the signals occupying the other's guard interval.

15. To address the inefficiencies set out above, cyclic diversity schemes were implemented (e.g., the cyclic-delay diversity scheme). In the cyclic-delay diversity scheme each of two or more transmitters send the same data in a respective stream of symbols, but cyclically

offset one spatial stream vis-a-vis the other by a defined number of samples resulting in a circular shift of all the samples in a particular symbol (or part thereof). By introducing a relatively small cyclic delay to a first transmitted MIMO signal relative to a second transmitted MIMO signals, those of skill in the art were able to substantially reduce the problems set out above. But, by introducing a small cyclic delay between the first and second MIMO signals, upon receipt sometimes the receiver would be unable to determine whether the cyclic delay was intentional or caused by environmental or other factors. This inability in turn led to the receiver incorrectly assuming an attempt by the transmitter to beamform, which occurs when antennas are intentionally electronically steered to adjust the phase and amplitude of a transmitted digital signal at each antenna, such that the signals combine constructively in the desired direction and destructively in the other directions. That is, small cyclic delays were causing unintentional beamforming.

16. To address these and other problems in the art Mark Webster and Michael Seals, at the time engineers for Conexant Systems, developed improved systems and methods of wireless communication, which include, but are not limited to, an improved signal transmitting system capable of manipulating OFDM data packets and data streams using a cyclic diversity scheme based on cyclic advancement rather than cyclic delay, thereby improving packet reception performance and reducing packet error rates, among other benefits.

17. Defendant makes, uses, and sells devices that include embedded wireless 802.11n, 802.11ac and 802.11ax compliant chipsets configured to use MIMO and OFDMA with a cyclic shift diversity feature compliant with the respective 802.11 standard, such as the Zebra ET40-HC/ET 45-HC family of tablets.

Intra-cycle Timing Relationships in Integrated Circuits

18. An additional area of continued importance is the design and fabrication of high-performance signaling mechanisms for digital integrated circuit devices. For example, with respect to high-performance memory integrated circuit devices (e.g., Double Data Rate ("DDR")) memory, ensuring the reliability in the design and fabrication of high-performance memory modules had become problematic for many OEMs by 2003. The slower memory bus speeds prior to 2003 had allowed significant specification margins in the design and fabrication of a given memory module. As memory bus speeds began approaching those supported by the Double Data Rate 2 ("DDR2") standard in 2003 however, the industry recognized that their designs required ever more exacting control of critical timing specifications, and design parameters had to be even more strictly maintained to keep the entire system in balance. A stable DDR memory module had to provide reliability, speed, and proper timing to ensure the overall system (e.g., CPU, bridge components, peripheral busses, etc.) operated at peak performance.

19. Transmeta Corporation ("Transmeta"), a fabless semiconductor company, was founded in 1995 to help address problems such as the ones identified above. Among other things, Transmeta developed low power x86 compatible microprocessors based on a VLIW core and a software layer called Code Morphing Software. Transmeta's initial public offering on November 7, 2000, was the last of the great high-tech IPOs up through 2000, with its opening-day performance not being surpassed until Google Inc.'s IPO in 2004.

20. Transmeta launched its first product, the Crusoe processor, in January 2000, and its second processor, the Efficeon, in October 2003.

21. In October 2006, Transmeta sued Intel Corporation for infringement of ten Transmeta patents covering computer architecture and power efficiency technologies by making, using and selling a variety of microprocessors, including Intel's Pentium III, Pentium 4, Pentium

M, Core and Core 2 product lines. One year later, in October 2007, Transmeta and Intel settled the case, with Intel agreeing to pay Transmeta $150,000,000 up front and an additional $20,000,000 per year for five years.

22. Transmeta was acquired by Novafor Inc. in January 2009 for $255,600,000. Intellectual Ventures acquired much of the patent portfolio—including one of the asserted patents discussed below—the following month.

23. Defendant makes, uses, and sells electronic and mobile devices, such as the ET40-HC/ET45-HC family of tablets that include Qualcomm processors and LPDDR4, LPDDR4X or LPDDR5 memory.

THE PATENTS-IN-SUIT

24. On November 24, 2009, the United States Patent and Trademark Office issued United States Patent No. 7,623,439 ("the '439 patent"), titled CYCLIC DIVERSITY SYSTEMS AND METHODS. The '439 patent is valid and enforceable. A copy of the '439 patent is attached as Exhibit A.

25. Intellectual Ventures I LLC is the owner and assignee of all rights, title, and interest in the '439 patent, including the rights to grant licenses, to exclude others, and to recover past damages for infringement of that patent.

26. The '439 patent is directed to a system and method for transmitting OFDM signals from a multiple antenna transmitting device. The system is able to manipulate an OFDM signal using a cyclic advancement scheme whereby a portion of sampled symbol data from packets comprising the OFDM signal are shifted (advanced) into the guard interval of the packet relative to a first non-shifted version of the packet. The system and method then allow for the substantially

simultaneous transmission of the respective packets from different antenna in the transmitting device, thereby allowing a receiver to more easily acquire and correlate the received data.

27. The inventions claimed in the '439 patent were conceived by Mark Webster and Michael Seals, both of whom were engineers at Conexant Systems, a well-known software developer and fabless semiconductor company specializing in, among other things, developing technology for voice and audio processing. Mr. Webster is currently employed by L3Harris Technologies as a Senior Scientist, while Mr. Seals is a Principal Systems Engineer at Thales Group.

28. On January 12, 2010, the United States Patent and Trademark Office issued United States Patent No. 7,646,835 ("the '835 patent"), titled METHOD AND SYSTEM FOR AUTOMATICALLY CALIBRATING INTRA-CYCLE TIMING RELATIONSHIPS FOR SAMPLING SIGNALS FOR AN INTEGRATED CIRCUIT DEVICE. The '835 patent is valid and enforceable. A copy of the '835 patent is attached as Exhibit B.

29. Intellectual Ventures II LLC is the owner and assignee of all rights, title, and interest in the '835 patent, including the rights to grant licenses, to exclude others, and to recover past damages for infringement of that patent.

30. The '835 patent is directed to the automatic calibration of intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, including the generation of command signals to access an integrated circuit component; the accessing of data signals to convey data for the integrated circuit component; the accessing of sampling signals to control sampling of the data signals; and systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals

to determine a valid operation range of the integrated circuit device, wherein the valid operation range includes an optimal operation point for the integrated circuit device.

31. The inventions claimed in the '835 patent were conceived by Guillermo J. Rozas during his time at Transmeta Corporation.

COUNT I
(Defendant's Infringement of U.S. Patent No. 7,623,439)

32. The preceding paragraphs are reincorporated by reference as if fully set forth herein.

33. The '439 patent claims and teaches, *inter alia*, an improved signal transmitting system capable of manipulating OFDM data packets and data streams using improved cyclic diversity schemes, thereby improving packet reception performance when compared to conventional packet diversity mechanisms by reducing packet error rates, among other benefits.

34. The inventions improved upon then-existing cyclic diversity schemes in wireless communication by enabling a cyclic diversity scheme by which a portion of an OFDM packet's symbol data is cyclically advanced into the guard interval with respect to the original OFDM signal and then each signal is sent to a receiver device at substantially the same time from two respective antennas. This allowed for improved acquisition and correlation at the receiver while at the same time keeping intersymbol interference and unintentional beamforming to a minimum.

35. Unlike in prior art systems and methods, the cyclic diversity taught by the '439 patent uses cyclic advancement as opposed to delay. Doing so substantially reduces the probability of unintentional beamforming.

36. More specifically, one exemplary embodiment comprises an improved cyclic diversity system in which a logic circuit is configured to cyclically advance samples of a symbol data portion of an OFDM packet to be transmitted on a first antenna, relative to the samples of a

symbol data portion of another OFDM packet to be transmitted on another antenna. The duration of the cyclic advance is less than the duration of a guard interval portion of the OFDM packet. By using a cyclic advance as described above, the symbol data portions of the two different transmitted signals are better decorrelated, thus reducing the probability of unintentional beamforming. The performance of wireless networks is thereby improved by the technologies disclosed and claimed in the ’439 patent.

37. The system and methods covered by the asserted claims, therefore, differs markedly from prior art systems in use at the time of this invention, which lacked the claimed combination of cyclically advancing a first OFDM packet by shifting the samples in a first direction an amount less than a sample duration of the guard interval portion to generate a shifted version of the first OFDM packet in which at least a non-zero number of samples from the symbol data portion of the first OFDM packet are shifted into the guard interval portion of the shifted version, and a same non-zero number of samples from the guard interval portion of the first OFDM packet are shifted out of the guard interval portion of the shifted version. And, further where both versions are substantially simultaneously transmitted.

38. Defendant has directly infringed and continues to directly infringe at least claim 1 of the ’439 patent by making, using, selling, offering for sale, or importing products and/or services covered by the ’439 patent. Defendant’s products and/or services that infringe the ’439 patent include all wireless communication products that support IEEE 802.11n, 802.11ac and 802.11ax, including the transmission of multiple spatial streams, which requires a cyclic diversity shift when transmitting OFDM packets, that are made, used, sold, or offered for sale by or on behalf of Defendant and/or its subsidiaries or parent companies (cumulatively, “the ’439 Accused Products”), including but not limited to, the ET40-HC/ET45-HC family of tablets.

39. Claim 1 of the ’439 patent is reproduced below:

1. A method for transmitting orthogonal frequency division multiplexing (OFDM) signals comprising:

generating a first OFDM packet for transmission including a guard interval portion and a symbol data portion each comprised of a plurality of samples;

cyclically advancing the first OFDM packet by shifting the samples in a first direction an amount less than a sample duration of the guard interval portion to generate a shifted version of the first OFDM packet for transmission in which at least a non-zero number of the samples from the symbol data portion of the first OFDM packet are shifted into the guard interval portion of the shifted version and a same non-zero number of samples from the guard interval portion of the first OFDM packet are shifted out of the guard interval portion of the shifted version; and

substantially simultaneously transmitting the first OFDM packet and the shifted version of the OFDM packet.

40. The ’439 Accused Products are configured to perform a method for transmitting OFDM signals. As one example, the ET40-HC/ET 45-HC family of tablets supports the IEEE 802.11n standard, including the transmission of multiple spatial streams, which requires a forward shift diversity feature for transmitting OFDM signals:

ET40-HC/ET45-HC TABLET

Wireless Communications

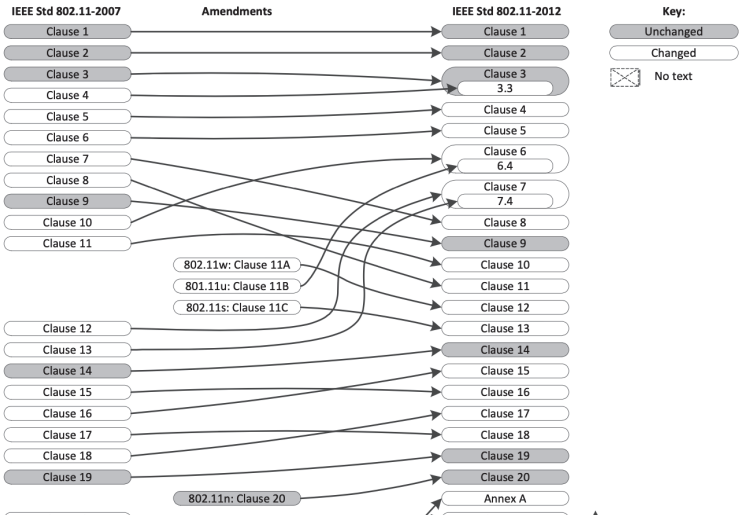
Wi-Fi (WLAN)	IEEE 802.11 a/b/g/n/ac/d/h/i/r/k/v/w/mc/ax 2x2 MU-MIMO; Wi-Fi® certified; IPv4, IPv6 (Wi-Fi 6)

Performance Characteristics

CPU	Qualcomm Snapdragon™ SM6375 Octa-Core (8): 2.2 GHz (2) and 1.8 GHz (6)

Source: https://www.zebra.com/us/en/products/spec-sheets/tablets/et40-hc-et45-hc.html

Source: https://www.qualcomm.com/content/dam/qcomm-martech/dm-assets/documents/product_brief_-_snapdragon_695_5g_mobile_platform.pdf



Source: IEEE 802.11-2012.

20. High Throughput (HT) PHY specification

20.1 Introduction

20.1.1 Introduction to the HT PHY

Clause 20 specifies the PHY entity for a high throughput (HT) orthogonal frequency division multiplexing (OFDM) system.

In addition to the requirements found in Clause 20, an HT STA shall be capable of transmitting and receiving frames that are compliant with the mandatory PHY specifications defined as follows:

- In Clause 18 when the HT STA is operating in a 20 MHz channel width in the 5 GHz band
- In Clause 17 and Clause 19 when the HT STA is operating in a 20 MHz channel width in the 2.4 GHz band

The HT PHY is based on the OFDM PHY defined in Clause 18, with extensibility up to four spatial streams, operating in 20 MHz bandwidth. Additionally, transmission using one to four spatial streams is defined for operation in 40 MHz bandwidth. These features are capable of supporting data rates up to 600 Mb/s (four spatial streams, 40 MHz bandwidth).

The HT PHY data subcarriers are modulated using binary phase shift keying (BPSK), quadrature phase shift keying (QPSK), 16-quadrature amplitude modulation (16-QAM), or 64-QAM. Forward error correction (FEC) coding (convolutional coding) is used with a coding rate of 1/2, 2/3, 3/4, or 5/6. LDPC codes are added as an optional feature.

Source: IEEE Std 802.11-2012 pp. 1669.

20.1.2 Scope

The services provided to the MAC by the HT PHY consist of two protocol functions, defined as follows:

a) A PHY convergence function, which adapts the capabilities of the physical medium dependent (PMD) system to the PHY service. This function is supported by the physical layer convergence procedure (PLCP), which defines a method of mapping the PSDUs into a framing format (PPDU) suitable for sending and receiving PSDUs between two or more STAs using the associated PMD system.

Source: IEEE Std 802.11-2012 pp. 1669.

20.1.4 PPDU formats

The structure of the PPDU transmitted by an HT STA is determined by the TXVECTOR FORMAT, CH_BANDWIDTH, CH_OFFSET, and MCS parameters as defined in Table 20-1. The effect of the CH_BANDWIDTH, CH_OFFSET, and MCS parameters on PPDU format is described in 20.2.3.

The FORMAT parameter determines the overall structure of the PPDU as follows:

- *Non-HT format* (**NON_HT**): Packets of this format are structured according to the Clause 18 (OFDM) or Clause 19 (ERP) specification. Support for non-HT format is mandatory.
- *HT-mixed format* (**HT_MF**): Packets of this format contain a preamble compatible with Clause 18 and Clause 19 receivers. The non-HT-STF (L-STF), the non-HT-LTF (L-LTF), and the non-HT SIGNAL field (L-SIG) are defined so they can be decoded by non-HT Clause 18 and Clause 19 STAs. The rest of the packet cannot be decoded by Clause 18 or Clause 19 STAs. Support for HT-mixed format is mandatory.
- *HT-greenfield format* (**HT_GF**): HT packets of this format do not contain a non-HT compatible part. Support for HT-greenfield format is optional. An HT STA that does not support the reception of an HT-greenfield format packet shall be able to detect that an HT-greenfield format packet is an HT transmission (as opposed to a non-HT transmission). In this case, the receiver shall decode the HT-SIG and determine whether the HT-SIG cyclic redundancy check (CRC) passes.

Source: IEEE Std. 802.11-2012, pp. 1669-70.

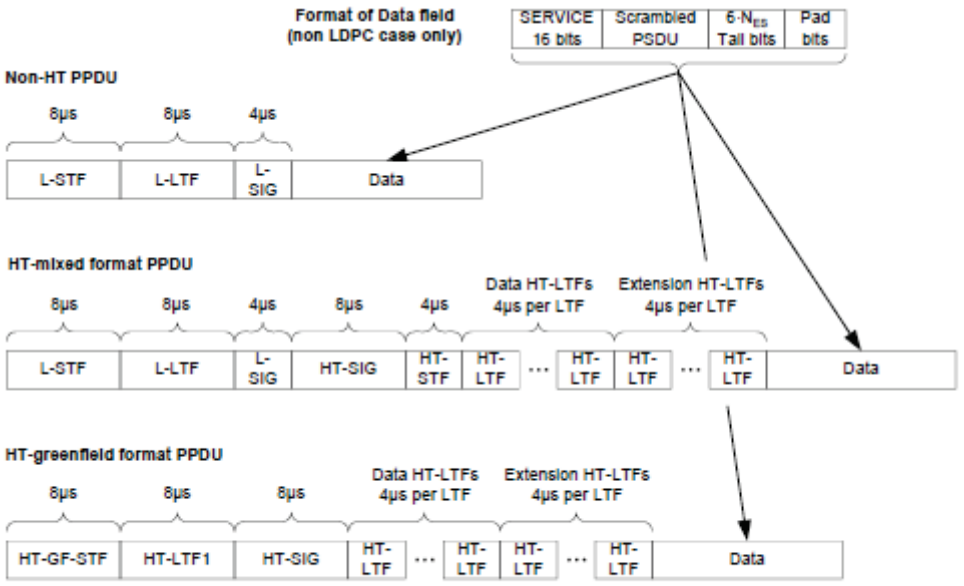


Figure 20-1—PPDU format

Source: IEEE Std. 802.11-2012, pp. 1682.

The HT portion of the HT-mixed format preamble enables estimation of the MIMO channel to support demodulation of the HT data by HT STAs. The HT portion of the HT-mixed format preamble also includes the HT-SIG field, which supports HT operation. The SERVICE field is prepended to the PSDU.

Source: IEEE Std. 802.11-2012, pp. 1682.

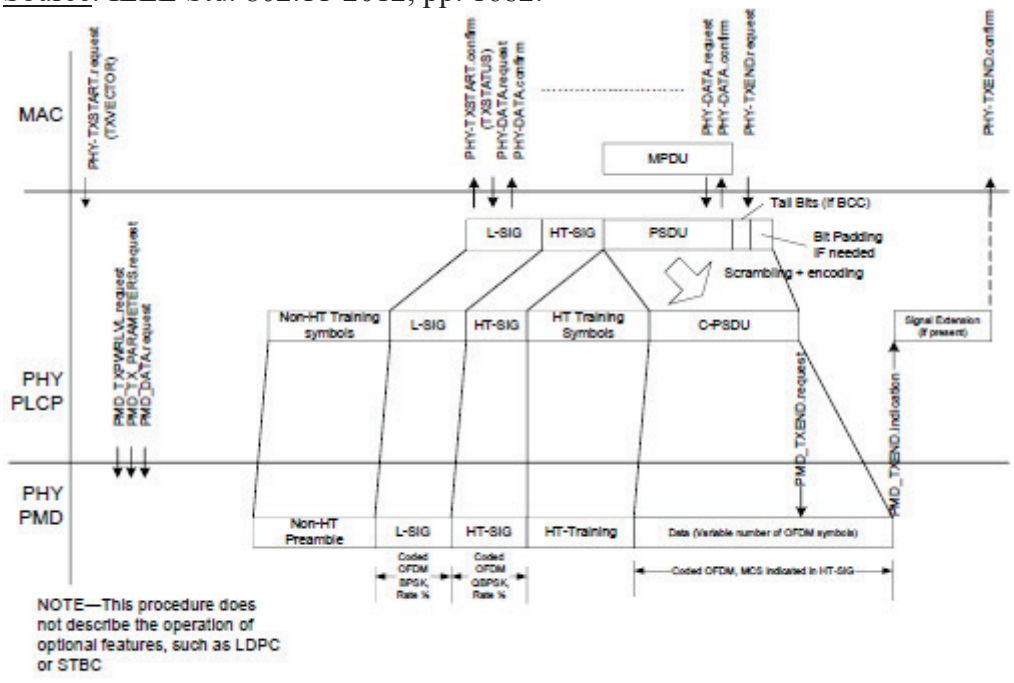


Figure 20-22—PLCP transmit procedure (HT-mixed format PPDU)

Source: IEEE Std. 802.11-2012, p. 1748.

41. The method practiced by the '439 Accused Products includes generating a first OFDM packet for transmission including a guard interval portion and a symbol data portion each comprised of a plurality of samples. For instance, the 802.11 transmitter in the Accused Products creates an OFDM packet, known as an HT-SIG OFDM packet, which includes a symbol data portion comprised of a plurality of samples and a guard interval portion comprised of a plurality of samples as seen below:

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— In Clause 18 when the HT STA is operating in a 20 MHz channel width in the 5 GHz band
— In Clause 17 and Clause 19 when the HT STA is operating in a 20 MHz channel width in the 2.4 GHz band

The HT PHY is based on the OFDM PHY defined in Clause 18, with extensibility up to four spatial streams, operating in 20 MHz bandwidth. Additionally, transmission using one to four spatial streams is defined for operation in 40 MHz bandwidth. These features are capable of supporting data rates up to 600 Mb/s (four spatial streams, 40 MHz bandwidth).

The HT PHY data subcarriers are modulated using binary phase shift keying (BPSK), quadrature phase shift keying (QPSK), 16-quadrature amplitude modulation (16-QAM), or 64-QAM. Forward error correction (FEC) coding (convolutional coding) is used with a coding rate of 1/2, 2/3, 3/4, or 5/6. LDPC codes are added as an optional feature.

Source: IEEE Std 802.11-2012 pp. 1669.

20.1.2 Scope

The services provided to the MAC by the HT PHY consist of two protocol functions, defined as follows:

a) A PHY convergence function, which adapts the capabilities of the physical medium dependent (PMD) system to the PHY service. This function is supported by the physical layer convergence procedure (PLCP), which defines a method of mapping the PSDUs into a framing format (PPDU) suitable for sending and receiving PSDUs between two or more STAs using the associated PMD system.

Source: IEEE Std 802.11-2012 pp. 1669.

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The structure of the PPDU transmitted by an HT STA is determined by the TXVECTOR FORMAT, CH_BANDWIDTH, CH_OFFSET, and MCS parameters as defined in Table 20-1. The effect of the CH_BANDWIDTH, CH_OFFSET, and MCS parameters on PPDU format is described in 20.2.3.

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— *HT-greenfield format* **(HT_GF)**: HT packets of this format do not contain a non-HT compatible part. Support for HT-greenfield format is optional. An HT STA that does not support the reception of an HT-greenfield format packet shall be able to detect that an HT-greenfield format packet is an HT transmission (as opposed to a non-HT transmission). In this case, the receiver shall decode the HT-SIG and determine whether the HT-SIG cyclic redundancy check (CRC) passes.

Source: IEEE Std. 802.11-2012, pp. 1669-70.

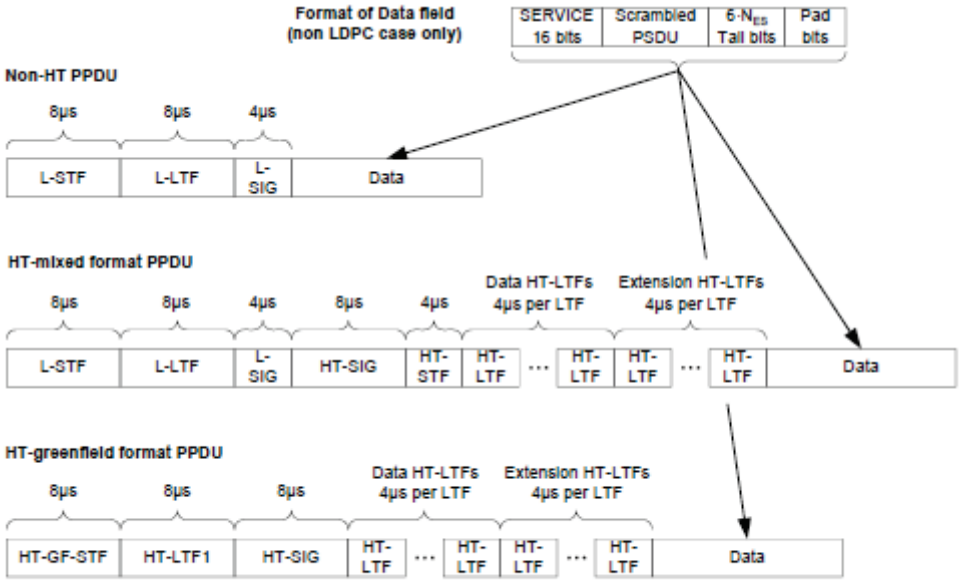


Figure 20-1—PPDU format

Source: IEEE Std. 802.11-2012, pp. 1682.

The HT portion of the HT-mixed format preamble enables estimation of the MIMO channel to support demodulation of the HT data by HT STAs. The HT portion of the HT-mixed format preamble also includes the HT-SIG field, which supports HT operation. The SERVICE field is prepended to the PSDU.

Source: IEEE Std. 802.11-2012, pp. 1682.

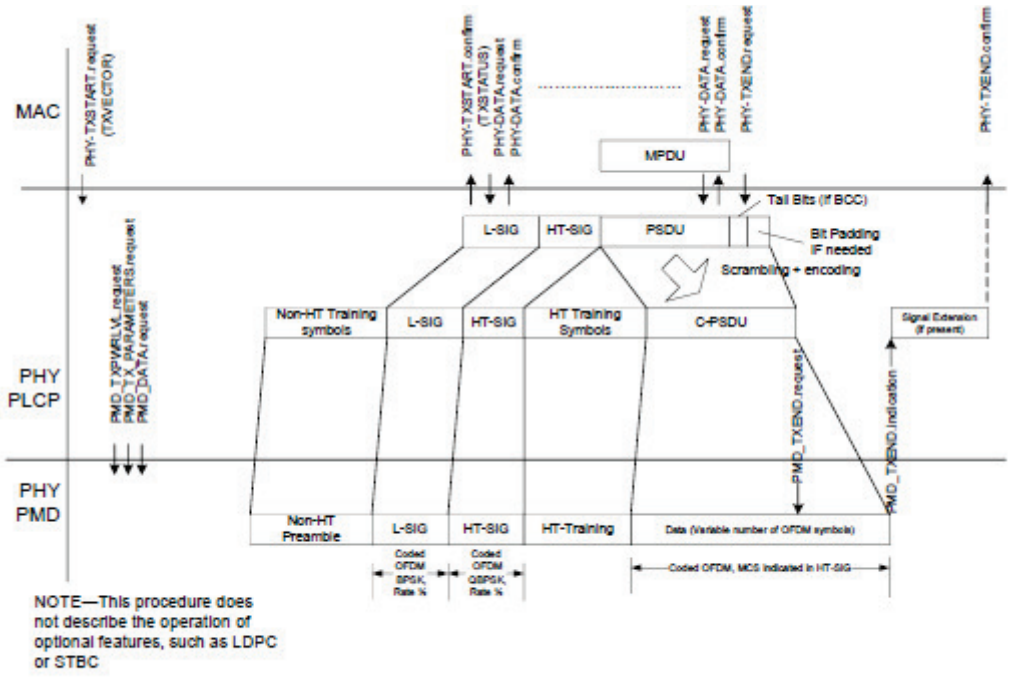


Figure 20-22—PLCP transmit procedure (HT-mixed format PPDU)

Source: IEEE Std. 802.11-2012, p. 1748.

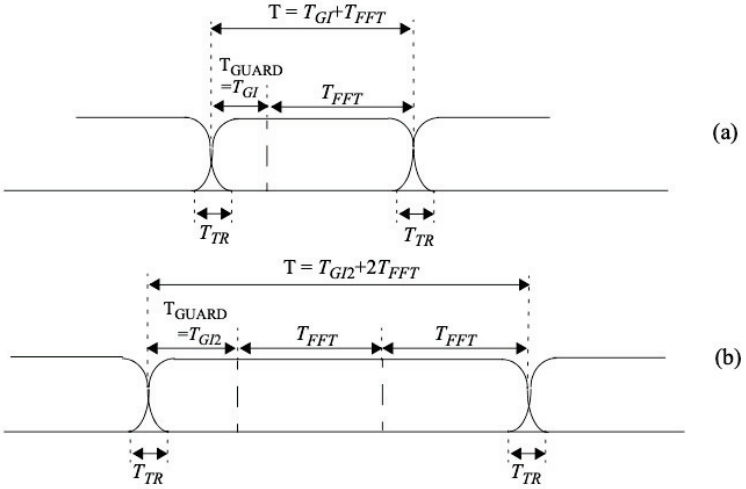


Figure 18-2—Illustration of OFDM frame with cyclic extension and windowing for (a) single reception or (b) two receptions of the FFT period

Source: IEEE Std. 802.11-2012, p. 1592.

T_{FFT}: Inverse Fast Fourier Transform (IFFT) / Fast Fourier Transform (FFT) period	3.2 µs ($1/\Delta_F$)
T_{SIGNAL}: Duration of the SIGNAL BPSK-OFDM symbol	4.0 µs ($T_{GI} + T_{FFT}$)
T_{GI}: GI duration	0.8 µs ($T_{FFT}/4$)

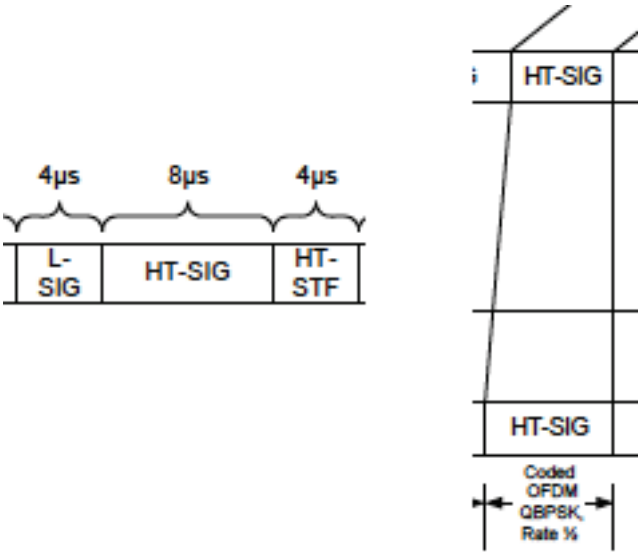
Source: IEEE Std. 802.11-2012, p. 1590-91.

20.3.9.4.3 HT-SIG definition

The HT-SIG is used to carry information required to interpret the HT packet formats. The fields of the HT-SIG are described in Table 20-11.

Table 20-11—HT-SIG fields

Field	Number of bits	Explanation and coding
Modulation and Coding Scheme	7	Index into the MCS table. See NOTE 1.
CBW 20/40	1	Set to 0 for 20 MHz or 40 MHz upper/lower. Set to 1 for 40 MHz.
HT Length	16	The number of octets of data in the PSDU in the range of 0 to 65 535.



Source: IEEE Std. 802.11-2012, p. 1682, 1748, 1699.

The HT-SIG is composed of two parts, HT-SIG$_1$ and HT-SIG$_2$, each containing 24 bits, as shown in Figure 20-6. All the fields in the HT-SIG are transmitted LSB first, and HT-SIG$_1$ is transmitted before HT-SIG$_2$.

The HT-SIG parts shall be encoded at R = 1/2, interleaved, and mapped to a BPSK constellation, and they have pilots inserted following the steps described in 18.3.5.6, 18.3.5.7, 18.3.5.8, and 18.3.5.9, respectively. The BPSK constellation is rotated by 90° relative to the L-SIG in order to accommodate detection of the start of the HT-SIG. The stream of 96 complex numbers generated by these steps is divided into two groups of 48 complex numbers: $d_{k,n}$, $0 \le k \le 47$, $n = 0, 1$. The time domain waveform for the HT-SIG in an HT-mixed format packet in a 20 MHz transmission shall be as shown in Equation (20-16).

$$r_{HT-SIG}^{i_{TX}}(t) = \frac{1}{\sqrt{N_{TX} \cdot N_{HT-SIG}^{Tone}}} \sum_{n=0}^{1} w_{T_{SYM}}(t - nT_{SYM}) \cdot \sum_{k=-26}^{26} (jD_{k,n} + p_{n+1}P_k)\exp(j2\pi k\Delta_F(t - nT_{SYM} - T_{GI} - T_{CS}^{i_{TX}})) \quad (20\text{-}16)$$

Source: IEEE Std. 802.11-2012, p. 1700.

18.3.2.6 Discrete time implementation considerations

The following descriptions of the discrete time implementation are informational.

In a typical implementation, the windowing function is represented in discrete time. As an example, when a windowing function with parameters T = 4.0 µs and a T_{TR} = 100 ns is applied, and the signal is sampled at 20 Msample/s, it becomes

$$w_T[n] = w_T(nT_S) = \begin{Bmatrix} 1 & 1 \le n \le 79 \\ 0.5 & 0, 80 \\ 0 & otherwise \end{Bmatrix} \quad (18\text{-}5)$$

Source: IEEE Std. 802.11-2012, p. 1593.

Figure 20-2 and Figure 20-3 show example transmitter block diagrams. In particular, Figure 20-2 shows the transmitter blocks used to generate the HT-SIG of the HT-mixed format PPDU. These transmitter blocks are

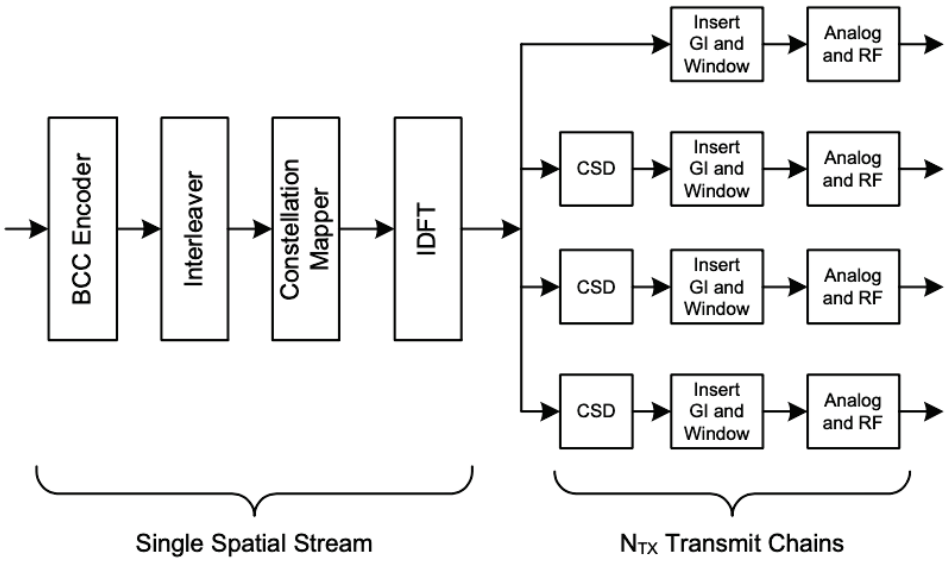


Figure 20-2—Transmitter block diagram 1

Source: IEEE Std. 802.11-2012, p. 1684-85.

20.3.3 Transmitter block diagram

HT-mixed format and HT-greenfield format transmissions can be generated using a transmitter consisting of the following blocks:

a) *Scrambler* scrambles the data to reduce the probability of long sequences of 0s or 1s; see 20.3.11.3.

b) *Encoder parser*, if BCC encoding is to be used, demultiplexes the scrambled bits among N_{ES} (number of BCC encoders for the Data field) BCC encoders, in a round robin manner.

c) *FEC encoders* encode the data to enable error correction. An FEC encoder may include a binary convolutional encoder followed by a puncturing device, or it may include an LDPC encoder.

d) *Stream parser* divides the outputs of the encoders into blocks that are sent to different interleaver and mapping devices. The sequence of the bits sent to an interleaver is called a *spatial stream*.

e) *Interleaver* interleaves the bits of each spatial stream (changes order of bits) to prevent long sequences of adjacent noisy bits from entering the BCC decoder. Interleaving is applied only when BCC encoding is used.

f) *Constellation mapper* maps the sequence of bits in each spatial stream to constellation points (complex numbers).

g) *STBC* encoder spreads constellation points from N_{SS} spatial streams into N_{STS} space-time streams using a space-time block code. STBC is used only when $N_{SS} < N_{STS}$; see 20.3.11.9.2.

h) *Spatial mapper* maps space-time streams to transmit chains. This may include one of the following:
   1) *Direct mapping*: Constellation points from each space-time stream are mapped directly onto the transmit chains (one-to-one mapping).
   2) *Spatial expansion*: Vectors of constellation points from all the space-time streams are expanded via matrix multiplication to produce the input to all the transmit chains.
   3) *Beamforming*: Similar to spatial expansion, each vector of constellation points from all the space-time streams is multiplied by a matrix of steering vectors to produce the input to the transmit chains.

i) *Inverse discrete Fourier transform (IDFT)* converts a block of constellation points to a time domain block.

Source: IEEE Std. 802.11-2012, p. 1683-84.

42. The method practiced by the '439 Accused Products includes cyclically advancing the first OFDM packet by shifting the samples in a first direction an amount less than a sample duration of the guard interval portion to generate a shifted version of the first OFDM packet for transmission. For example, the Accused Products cyclically shift the symbol data portion of the HT_SIG by -200 ns up to -50 ns, which is less than its guard interval's total length of 0.8 us, to generate a shifted version for transmission as seen below:

20.3.3 Transmitter block diagram

HT-mixed format and HT-greenfield format transmissions can be generated using a transmitter consisting of the following blocks:

a) *Scrambler* scrambles the data to reduce the probability of long sequences of 0s or 1s; see 20.3.11.3.
b) *Encoder parser*, if BCC encoding is to be used, demultiplexes the scrambled bits among N_{ES} (number of BCC encoders for the Data field) BCC encoders, in a round robin manner.
c) *FEC encoders* encode the data to enable error correction. An FEC encoder may include a binary convolutional encoder followed by a puncturing device, or it may include an LDPC encoder.
d) *Stream parser* divides the outputs of the encoders into blocks that are sent to different interleaver and mapping devices. The sequence of the bits sent to an interleaver is called a *spatial stream*.
e) *Interleaver* interleaves the bits of each spatial stream (changes order of bits) to prevent long sequences of adjacent noisy bits from entering the BCC decoder. Interleaving is applied only when BCC encoding is used.
f) *Constellation mapper* maps the sequence of bits in each spatial stream to constellation points (complex numbers).
g) *STBC* encoder spreads constellation points from N_{SS} spatial streams into N_{STS} space-time streams using a space-time block code. STBC is used only when $N_{SS} < N_{STS}$; see 20.3.11.9.2.

h) *Spatial mapper* maps space-time streams to transmit chains. This may include one of the following:
   1) *Direct mapping*: Constellation points from each space-time stream are mapped directly onto the transmit chains (one-to-one mapping).
   2) *Spatial expansion*: Vectors of constellation points from all the space-time streams are expanded via matrix multiplication to produce the input to all the transmit chains.
   3) *Beamforming*: Similar to spatial expansion, each vector of constellation points from all the space-time streams is multiplied by a matrix of steering vectors to produce the input to the transmit chains.

i) *Inverse discrete Fourier transform (IDFT)* converts a block of constellation points to a time domain block.

Source: IEEE Std. 802.11-2012, p. 1683-84.

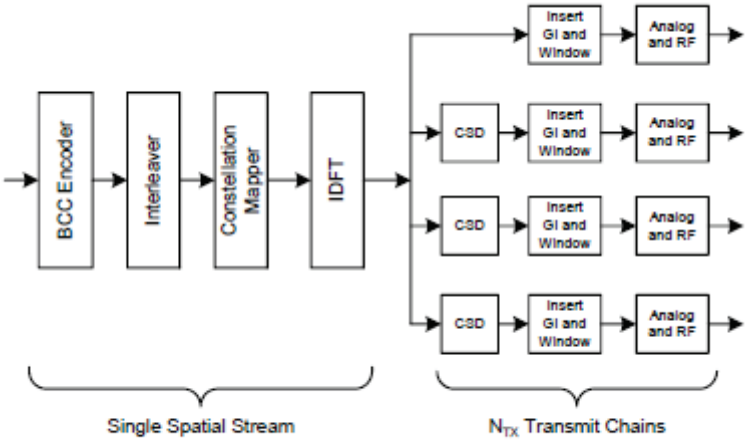


Figure 20-2—Transmitter block diagram 1

Source: IEEE Std. 802.11-2012, p. 1685.

20.3.9.3.2 Cyclic shift definition

The cyclic shift values defined in this subclause apply to the non-HT fields in the HT-mixed format preamble and the HT-SIG in the HT-mixed format preamble.

Cyclic shifts are used to prevent unintentional beamforming when the same signal or scalar multiples of one signal are transmitted through different spatial streams or transmit chains. A cyclic shift of duration T_{CS} on a signal $s(t)$ on interval $0 \le t \le T$ is defined as follows, where T is defined as T_{DFT} as referenced in Table 20-6.

With $T_{CS} \le 0$, replace $s(t)$ with $s(t - T_{CS})$ when $0 \le t < T + T_{CS}$ and with $s(t - T_{CS} - T)$ when $T + T_{CS} \le t \le T$. The cyclic-shifted signal is defined as shown in Equation (20-7).

$$s_{CS}(t;T_{CS})\big|_{T_{CS}<0} = \begin{cases} s(t - T_{CS}) & 0 \le t < T + T_{CS} \\ s(t - T_{CS} - T) & T + T_{CS} \le t \le T \end{cases} \quad (20\text{-}7)$$

The cyclic shift is applied to each OFDM symbol in the packet separately. Table 20-9 specifies the values for the cyclic shifts that are applied in the L-STF (in an HT-mixed format packet), the L-LTF, and L-SIG. It also applies to the HT-SIG in an HT-mixed format packet.

Source: IEEE Std. 802.11-2012, p. 1694-95.

Table 20-9—Cyclic shift for non-HT portion of packet

T_{CS}^{iTX} values for non-HT portion of packet				
Number of transmit chains	Cyclic shift for transmit chain 1 (ns)	Cyclic shift for transmit chain 2 (ns)	Cyclic shift for transmit chain 3 (ns)	Cyclic shift for transmit chain 4 (ns)
1	0	—	—	—
2	0	–200	—	—
3	0	–100	–200	—
4	0	–50	–100	–150

Source: IEEE Std. 802.11-2012, p. 1695.

Table 20-5—Timing-related constants *(continued)*

T_{DFT}: IDFT/DFT period	3.2 μs
T_{GI}: Guard interval duration	0.8 μs= T_{DFT}/4

Source: IEEE Std. 802.11n-2009, p. 266.

20.3.4 Overview of the PPDU encoding process

The encoding process is composed of the steps described below. The following overview is intended to facilitate an understanding of the details of the convergence procedure:

b) Construct the PLCP preamble SIGNAL fields from the appropriate fields of the TXVECTOR by adding tail bits, applying convolutional coding, formatting into one or more OFDM symbols, applying cyclic shifts, applying spatial processing, calculating an inverse Fourier transform for each OFDM symbol and transmit chain, and prepending a cyclic prefix or GI to each OFDM symbol in each transmit chain. The number and placement of the PLCP preamble SIGNAL fields depend on the frame format being used. Refer to 20.3.9.3.5, 20.3.9.4.3, and 20.3.9.5.4.

r) For each group of N_{ST} subcarriers and each of the N_{TX} transmit chains, convert the subcarriers to time domain using IDFT. Prepend to the Fourier-transformed waveform a circular extension of itself, thus forming a GI, and truncate the resulting periodic waveform to a single OFDM symbol length by applying time domain windowing. Determine the length of the GI according to the GI_TYPE parameter of the TXVECTOR. Refer to 20.3.11.11 and 20.3.11.12 for details. When beamforming is not used, it is sometimes possible to implement the cyclic shifts in the time domain.

Source: IEEE Std. 802.11-2012, p. 1684, 1688.

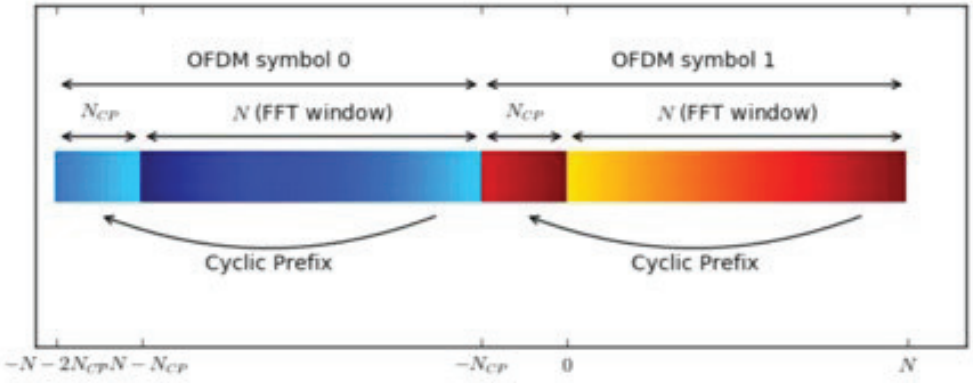
The Cyclic Prefix for OFDM

In a previous post, we have elaborated about the building blocks of OFDM.

There, we have stated two benefits of using a cyclic prefix between subsequent OFDM symbols:

- The CP isolates different OFDM blocks from each other when the wireless channel contains multiple paths, i.e. is frequency-selective.
- The CP turns the linear convolution with the channel into a circular convolution. Only with a circular convolution, we can use the single-tap equalization OFDM is so famous for.

As we see, the CP of an OFDM symbol is obtained by prepending a copy of the last N_{CP} samples from the end of the OFDM signal to its beginning. This way we obtain a circular signal structure, i.e. the first N_{CP} and last N_{CP} samples are equal in each OFDM symbol.



In the above figure, we see two subsequent OFDM symbols, each having a dedicated CP. The colors encode the signal value. The cyclic prefix at the beginning of each OFDM symbol shows a copy of the color of end of the OFDM symbol. When the signal is demodulated, the N-point FFT is taken at the position after the CP, which is indicated with *FFT window*.

Source: *https://dspillustrations.com/pages/posts/misc/the-cyclic-prefix-cp-in-ofdm.html*

The HT-SIG is composed of two parts, HT-SIG$_1$ and HT-SIG$_2$, each containing 24 bits, as shown in Figure 20-6. All the fields in the HT-SIG are transmitted LSB first, and HT-SIG$_1$ is transmitted before HT-SIG$_2$.

The HT-SIG parts shall be encoded at R = 1/2, interleaved, and mapped to a BPSK constellation, and they have pilots inserted following the steps described in 18.3.5.6, 18.3.5.7, 18.3.5.8, and 18.3.5.9, respectively. The BPSK constellation is rotated by 90° relative to the L-SIG in order to accommodate detection of the start of the HT-SIG. The stream of 96 complex numbers generated by these steps is divided into two groups of 48 complex numbers: $d_{k,n}$, $0 \le k \le 47$, $n = 0, 1$. The time domain waveform for the HT-SIG in an HT-mixed format packet in a 20 MHz transmission shall be as shown in Equation (20-16).

$$r_{HT-SIG}^{i_{TX}}(t) = \frac{1}{\sqrt{N_{TX} \cdot N_{HT-SIG}^{Tone}}} \sum_{n=0}^{1} w_{T_{SYM}}(t - nT_{SYM}) \cdot \sum_{k=-26}^{26} (jD_{k,n} + p_{n+1}P_k) \exp(j2\pi k\Delta_F(t - nT_{SYM} - T_{GI} - T_{CS}^{i_{TX}})) \quad (20\text{-}16)$$

where

$$D_{k,n} = \begin{cases} 0, k = 0, \pm 7, \pm 21 \\ d_{M'(k),n}, \text{otherwise} \end{cases}$$

$M'(k)$ is defined in 20.3.9.3

P_k and p_n are defined in 18.3.5.10

N_{HT-SIG}^{Tone} has the value given in Table 20-8

$T_{CS}^{i_{TX}}$ represents the cyclic shift for transmit chain i_{TX} and is defined by Table 20-9 for HT-mixed format PPDUs.

Source: IEEE Std. 802.11-2012, pp. 1700-1701.

T_{GI2}: Double guard interval	1.6 µs	1.6 µs	1.6 µs

Source: IEEE Std. 802.11-2012, p. 1689.

43. In the method practiced by the '439 Accused Products, a number of samples from the symbol data portion of the first OFDM packet are shifted into the guard interval portion of the shifted version of the first OFDM packet, and the same number of samples from the guard interval portion of the first OFDM packet are shifted out of the guard interval portion of the shifted version of the first OFDM packet. For example, the Accused Products cyclically advance the number of samples corresponding to the time duration of $|T_{CS}|$ out of the symbol portion of the shifted OFDM packet and into the guard interval portion of the packet, while the same number of samples corresponding to the time duration of $|T_{CS}|$ are shifted out of the guard interval portion of the shifted OFDM packet, as illustrated below:

20.3.3 Transmitter block diagram

HT-mixed format and HT-greenfield format transmissions can be generated using a transmitter consisting of the following blocks:

a) *Scrambler* scrambles the data to reduce the probability of long sequences of 0s or 1s; see 20.3.11.3.

b) *Encoder parser*, if BCC encoding is to be used, demultiplexes the scrambled bits among N_{ES} (number of BCC encoders for the Data field) BCC encoders, in a round robin manner.

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d) *Stream parser* divides the outputs of the encoders into blocks that are sent to different interleaver and mapping devices. The sequence of the bits sent to an interleaver is called a *spatial stream*.

e) *Interleaver* interleaves the bits of each spatial stream (changes order of bits) to prevent long sequences of adjacent noisy bits from entering the BCC decoder. Interleaving is applied only when BCC encoding is used.

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Source: IEEE Std. 802.11-2012, p. 1683-84.

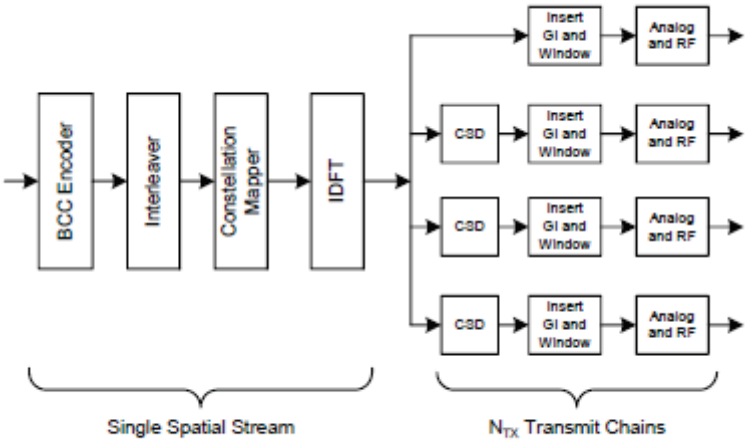

Figure 20-2—Transmitter block diagram 1

Source: IEEE Std. 802.11-2012, p. 1685.

20.3.9.3.2 Cyclic shift definition

The cyclic shift values defined in this subclause apply to the non-HT fields in the HT-mixed format preamble and the HT-SIG in the HT-mixed format preamble.

Cyclic shifts are used to prevent unintentional beamforming when the same signal or scalar multiples of one signal are transmitted through different spatial streams or transmit chains. A cyclic shift of duration T_{CS} on a signal $s(t)$ on interval $0 \le t \le T$ is defined as follows, where T is defined as T_{DFT} as referenced in Table 20-6.

With $T_{CS} \le 0$, replace $s(t)$ with $s(t - T_{CS})$ when $0 \le t < T + T_{CS}$ and with $s(t - T_{CS} - T)$ when $T + T_{CS} \le t \le T$. The cyclic-shifted signal is defined as shown in Equation (20-7).

$$s_{CS}(t;T_{CS})\big|_{T_{CS}<0} = \begin{cases} s(t - T_{CS}) & 0 \le t < T + T_{CS} \\ s(t - T_{CS} - T) & T + T_{CS} \le t \le T \end{cases} \quad (20\text{-}7)$$

The cyclic shift is applied to each OFDM symbol in the packet separately. Table 20-9 specifies the values for the cyclic shifts that are applied in the L-STF (in an HT-mixed format packet), the L-LTF, and L-SIG. It also applies to the HT-SIG in an HT-mixed format packet.

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Source: IEEE Std. 802.11-2012, p. 1695.

Table 20-5—Timing-related constants *(continued)*

T_{DFT}: IDFT/DFT period	3.2 μs
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Source: IEEE Std. 802.11n-2009, p. 266.

20.3.4 Overview of the PPDU encoding process

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r) For each group of N_{ST} subcarriers and each of the N_{TX} transmit chains, convert the subcarriers to time domain using IDFT. Prepend to the Fourier-transformed waveform a circular extension of itself, thus forming a GI, and truncate the resulting periodic waveform to a single OFDM symbol length by applying time domain windowing. Determine the length of the GI according to the GI_TYPE parameter of the TXVECTOR. Refer to 20.3.11.11 and 20.3.11.12 for details. When beamforming is not used, it is sometimes possible to implement the cyclic shifts in the time domain.

Source: IEEE Std. 802.11-2012, p. 1684, 1688.

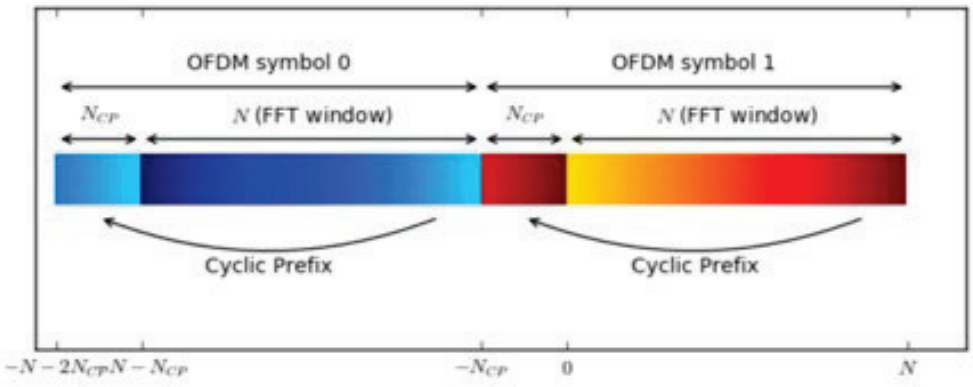
The Cyclic Prefix for OFDM

In a previous post, we have elaborated about the building blocks of OFDM.

There, we have stated two benefits of using a cyclic prefix between subsequent OFDM symbols:

- The CP isolates different OFDM blocks from each other when the wireless channel contains multiple paths, i.e. is frequency-selective.
- The CP turns the linear convolution with the channel into a circular convolution. Only with a circular convolution, we can use the single-tap equalization OFDM is so famous for.

As we see, the CP of an OFDM symbol is obtained by prepending a copy of the last N_{CP} samples from the end of the OFDM signal to its beginning. This way we obtain a circular signal structure, i.e. the first N_{CP} and last N_{CP} samples are equal in each OFDM symbol.



In the above figure, we see two subsequent OFDM symbols, each having a dedicated CP. The colors encode the signal value. The cyclic prefix at the beginning of each OFDM symbol shows a copy of the color of end of the OFDM symbol. When the signal is demodulated, the N-point FFT is taken at the position after the CP, which is indicated with *FFT window*.

Source: *https://dspillustrations.com/pages/posts/misc/the-cyclic-prefix-cp-in-ofdm.html*

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The HT-SIG parts shall be encoded at R = 1/2, interleaved, and mapped to a BPSK constellation, and they have pilots inserted following the steps described in 18.3.5.6, 18.3.5.7, 18.3.5.8, and 18.3.5.9, respectively. The BPSK constellation is rotated by 90° relative to the L-SIG in order to accommodate detection of the start of the HT-SIG. The stream of 96 complex numbers generated by these steps is divided into two groups of 48 complex numbers: $d_{k,n}$, $0 \le k \le 47$, $n = 0, 1$. The time domain waveform for the HT-SIG in an HT-mixed format packet in a 20 MHz transmission shall be as shown in Equation (20-16).

$$r_{HT-SIG}^{i_{TX}}(t) = \frac{1}{\sqrt{N_{TX} \cdot N_{HT-SIG}^{Tone}}} \sum_{n=0}^{1} w_{T_{SYM}}(t - nT_{SYM}) \cdot \sum_{k=-26}^{26} (jD_{k,n} + p_{n+1}P_k)\exp(j2\pi k\Delta_F(t - nT_{SYM} - T_{GI} - T_{CS}^{i_{TX}})) \quad (20\text{-}16)$$

where

$$D_{k,n} = \begin{cases} 0, k = 0, \pm 7, \pm 21 \\ d_{M'(k),n}, \text{otherwise} \end{cases}$$

$M'(k)$ is defined in 20.3.9.3

P_k and p_n are defined in 18.3.5.10

N_{HT-SIG}^{Tone} has the value given in Table 20-8

$T_{CS}^{i_{TX}}$ represents the cyclic shift for transmit chain i_{TX} and is defined by Table 20-9 for HT-mixed format PPDUs.

Source: IEEE Std. 802.11-2012, pp. 1700-1701.

T_{GI2}: Double guard interval	1.6 µs	1.6 µs	1.6 µs

Source: IEEE Std. 802.11-2012, p. 1689.

2.7.4 Mixed Mode Preamble

The mixed mode preamble is needed for compatibility with IEEE 802.11a/g. It starts with the 802.11a/g preamble. The 802.11n mixed mode preamble for two spatial streams is shown in Figure 2.34. The legacy short training field (L-STF) is identical to 802.11a/g except that different transmitters use different cyclic delays (CDs). This also applies to the legacy long training field (L-LTF). The STFs from different transmitters have low cross-correlation. For example, a CD of –400 ns (or a cyclic advance of 400 ns) minimizes correlation between two different transmitted short symbols. The L-STF uses a CD of only –200 ns for two transmitters, since legacy 802.11a/g receivers may not be able to cope with larger CD values.

Source: B. Bing, Broadband Wireless Multimedia Networks, Wiley, 2013, p. 120.

With $T_{CS} \le 0$, replace $s(t)$ with $s(t - T_{CS})$ when $0 \le t < T + T_{CS}$ and with $s(t - T_{CS} - T)$ when $T + T_{CS} \le t \le T$. The cyclic-shifted signal is defined as shown in Equation (20-7).

$$s_{CS}(t;T_{CS})\big|_{T_{CS}<0} = \begin{cases} s(t - T_{CS}) & 0 \le t < T + T_{CS} \\ s(t - T_{CS} - T) & T + T_{CS} \le t \le T \end{cases} \quad (20\text{-}7)$$

Source: IEEE Std. 802.11-2012, pp. 1700-1701.

44. The method practiced by the '439 Accused Products includes substantially simultaneously transmitting the first OFDM packet and the shifted version of the OFDM packet. For example, the signals transmitted from different transmit chains are aligned and synchronized in the time domain, as seen below:

Figure 20-2 and Figure 20-3 show example transmitter block diagrams. In particular, Figure 20-2 shows the transmitter blocks used to generate the HT-SIG of the HT-mixed format PPDU.

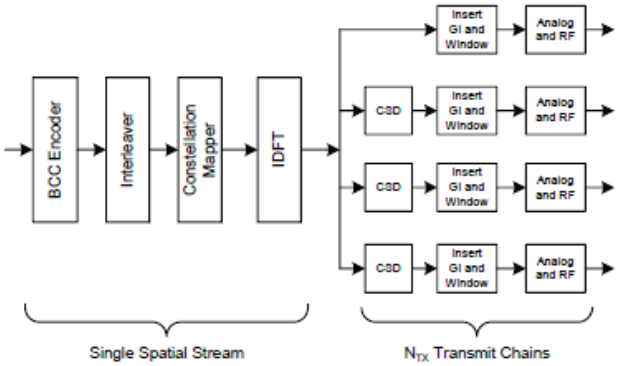


Figure 20-2—Transmitter block diagram 1

Source: IEEE Std. 802.11-2012, pp. 1684-85.

Radio Chains

Between the operating system and antenna, an 802.11 radio interface has to perform several tasks. When transmitting a frame, the main tasks are the inverse Fourier transform to turn the frequency-domain encoded signal into a time-domain signal, and amplification right before the signal hits the antenna so it has reasonable range. On the receive side, the process must be reversed. Immediately after entering the antenna, an amplifier boosts the faint signal received into something substantial enough to work with, and performs a Fourier transform to extract the subcarriers. In an 802.11 interface, these components are linked together and called a *radio chain*. Selecting the components to make up the radio chain is an important task for system designers, especially

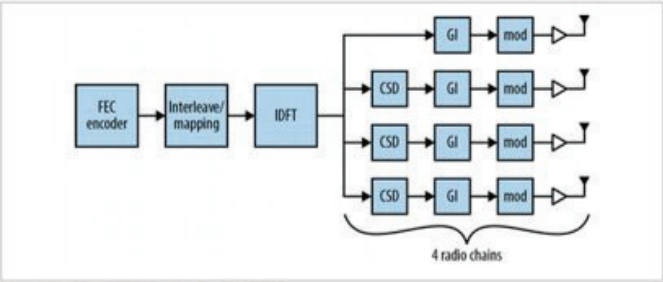


Figure 2-3. 4x4 802.11n interface block diagram

Source: Gast, Matthew, S., 802.11n A Survival Guide, O'Reilly, 2012, pp. 13-14.

45. Additionally, Defendant has been and currently is an active inducer of infringement of the '439 patent under 35 U.S.C. § 271(b) and a contributory infringer of the '439 patent under 35 U.S.C. § 271(c).

46. Defendant has actively induced, and continues to actively induce, infringement of the '439 patent by causing others to use, offer for sale, or sell in the United States, products or services covered by the '439 patent, including but not limited to the '439 Accused Products and any other products or services that include WiFi chipsets compliant with 802.11n, 802.11ac and/or 802.11ax, having the cyclic shift advance functionality described above. Defendant provides these products and services to others, such as customers, resellers, partners, and end-users, who, in turn, use, provision for use, offer for sale, or sell those products and services, which directly infringe the '439 patent as described above. Defendant's inducement includes requiring WiFi chipsets within the Accused Products to be compliant with the IEEE 802.11n, 802.11ac and 802.11ax standard, in which the cyclic advance diversity scheme described above is mandatory, and advertising and promoting such compliance to its customers, partners, re-sellers and the like, including the promotion, directions and instructions found at one or more of the following links, the provision of which is on-going as of the filing of this Complaint and much of the content of which is specifically illustrated above:

- https://www.zebra.com/us/en/products/spec-sheets/tablets/et40-hc-et45-hc.html

- https://www.zebra.com/us/en/products/spec-sheets/mobile-computers/handheld/tc51-tc56.html
- https://www.zebra.com/us/en/products/spec-sheets/mobile-computers/handheld/mc9300.html
- https://www.zebra.com/us/en/products/spec-sheets/mobile-computers/handheld/tc52-tc57.html
- https://www.zebra.com/content/dam/zebra_new_ia/en-us/solutions-verticals/product/Mobile_Computers/GENERAL/brochures/mobile-computing-at-a-glance-brochure.pdf
- https://www.zebra.com/us/en/products/spec-sheets/mobile-computers/handheld/mc3300x.html
- https://www.zebra.com/us/en/products/spec-sheets/mobile-computers/handheld/tc8300.html
- https://www.wi-fi.org/product-finder-results?keywords=Zebra&sort_by=certified&sort_order=desc&op=Search&form_build_id=form-KFEIchuNba7bGspjOd9nwDeKXtCYWWgoE3SAB6MoMx0&form_id=wifi_cert_api_simple_search_form

47. Defendant has contributed to, and continues to contribute to, the infringement of the ’439 patent by others by knowingly providing one or more components, for example the 802.11 WiFi chipset with cyclic shift (advance) functionality included in the Accused Products, a portion thereof, and/or the software/hardware modules responsible for the accused functionality described herein, that, when installed, configured, and used result in systems that, as intended by Defendant described above, directly infringe one or more claims of the ’439 patent.

48. Defendant knew of the ’439 patent, or should have known of the ’439 patent, but was willfully blind to its existence. Upon information and belief, Defendant had actual knowledge of the ’439 patent since at least as early as early as Defendant received a copy of this Complaint, or alternatively, at least as early as the service upon Defendant of the Complaint in this action..

49. By the time of trial, Defendant will or should have known and intended (since receiving such notice) that its continued actions would infringe and would actively induce and contribute to the infringement of the ’439 patent.

50. Defendant has committed, and continues to commit, contributory infringement by selling products and services that directly infringe the '439 patent when used by a third party, such as the Accused '439 Products, and that are a material part of the invention, knowing them to be especially made or adapted for use in infringement of the '439 patent and not staple articles or commodities of commerce suitable for substantial non-infringing use.

51. As a result of Defendant's acts of infringement, IV has suffered and will continue to suffer damages in an amount to be determined at trial.

COUNT II

(Defendant's Infringement of U.S. Patent No. 7,646,835).

52. The preceding paragraphs are reincorporated by reference as if fully set forth herein.

53. The '835 patent claims and teaches, *inter alia*, an improved way to input and output signaling for digital integrated circuit devices, by way of automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device.

54. The inventions improved upon the then-existing manual calibration techniques that were used on high-speed integrated circuit device memory systems, and other types of high-performance integrated circuit devices that require precisely aligned signals for their input and output. As was well-known, the design and certification of high-speed DDR memory modules had become a significant challenge for many system manufacturers. Practically all of the integral features of a given DDR dual in-line memory module ("DIMM"), such as the particular type of silicon used, the routing and thickness of the printed circuit board ("PCB"), and the signal integrity performance under stressed conditions (e.g., temperature, voltage, etc.), have an impact on the overall system performance and reliability. Failure to properly account for these variables can

result in single or multi-bit errors, read/write command sequencing failures, failure of the system to attain rated performance, and the like.

55. The automatic calibration process as provided by the inventions of the ’835 patent add a significant amount of “extra margin” to the specifications of a memory system. For example, for integrated circuit devices such as DDR DRAMs, the DDR timing specifications are so stringent that even slight variations (e.g., between motherboards, devices from different lots, etc.) can have an impact on overall system performance and cause intermittent timing-related DIMM failures. These failures can be the most difficult types of failures to detect and correct. The extra margin provided by the automatic calibration inventions of the ’835 patent increase the reliability rate of computer systems incorporating such high-performance integrated circuit devices. The extra margin provided by embodiments of the ’835 patent can be used to increase the maximum obtainable performance of such computer systems.

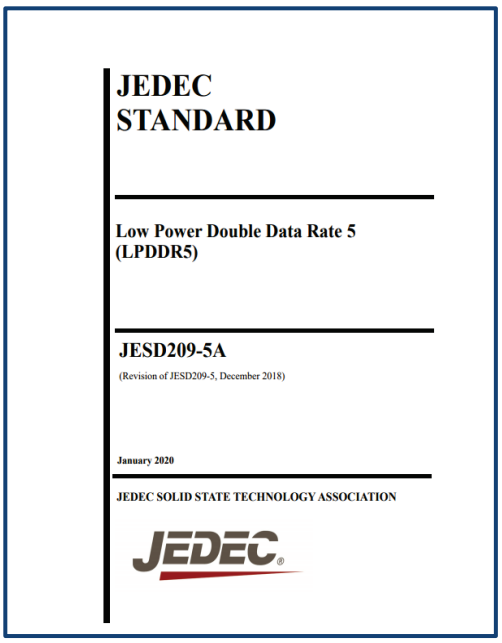
56. More specifically, the claims of the ’835 patent recite automatic calibration of intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, including the generation of command signals to access an integrated circuit component; the accessing of data signals to convey data for the integrated circuit component; the accessing of sampling signals to control sampling of the data signals; and systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device, wherein the valid operation range includes an optimal operation point for the integrated circuit device.

57. The systems and methods covered by the asserted claims, therefore, differs markedly from the prior systems in use at the time of this invention, which lacked the claimed

combination of automatic calibration of intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, including the generation of command signals to access an integrated circuit component; the accessing of data signals to convey data for the integrated circuit component; the accessing of sampling signals to control sampling of the data signals; and systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device, wherein the valid operation range includes an optimal operation point for the integrated circuit device.

58. Defendant has directly infringed and continues to directly infringe at least claim 1 of the ’835 patent by making, using, testing, selling, offering for sale, and importing into the United States products and services covered by the ’835 patent. Defendant’s products and services that infringe the ’835 patent include all mobile devices, laptops and tablets that include Qualcomm-based processors and LPDDR4, LPDDR4X or LPDDR5 memory, (together the “Accused ’835 Products” or “Accused Products”). Specific examples of the Accused Products include, but are not limited to, the Zebra ET40-HC/ET 45-HC family of tablets.

59. LPDDR4, LPDDR4X and LPDDR5 memory (including that within the Accused Products), are required to follow the JEDEC Solid State Technology Association’s standard for Low Power Double Data Rate 4, 4X and 5. Upon information and belief, memory labeled with the designations LPDDR4, LPDDR4X and LPDDR5 are claiming conformance with the standard by using such designations. The JEDEC standards for LPDDR4, LPDDR4X and LPDDR5 operate substantially the same with respect to the accused functionality (as seen below), and therefore, the LPDDR5 standard will be used as exemplary.



JEDEC STANDARD

Low Power Double Data Rate 5 (LPDDR5)

JESD209-5A

(Revision of JESD209-5, December 2018)

January 2020

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

JEDEC

1 Scope

This document defines the LPDDR5 standard, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this specification is to define the minimum set of requirements for a JEDEC compliant x16 one channel SDRAM device and x8 one channel SDRAM device. LPDDR5 device density ranges from 2 Gb through 32 Gb. This document was created using aspects of the following standards: DDR2 (JESD79-2), DDR3 (JESD79-3), DDR4 (JESD79-4), LPDDR (JESD209), LPDDR2 (JESD209-2), LPDDR3 (JESD209-3) and LPDDR4 (JESD209-4).

Each aspect of the standard was considered and approved by committee ballot(s). The accumulation of these ballots was then incorporated to prepare the LPDDR5 standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Source: JEDEC Standard No. 209-5A - Cover Page; p.1 and Notice Page.

I/O Signal Trainings

There are multiple trainings provided by LPDDR4 to align or re-adjust the delays introduced on the I/O signals with respect to CLK or other signals. As per standard physical interface definition of LPDDR4, there are CLK, CS, CA, DQ and DQS signals which need proper alignment for successful data transfers. As the CA line is sampled at the CLK signal, there should be a proper phase relationship between CA and CLK. Similarly, DQ gets sampled on DQS signal, so again there should be a phase relationship between the two. To maintain these phase relationships, LPDDR4 proposes training mechanisms. Let's look at those:

- Command Bus Training (CBT): This is used to align the CS and CA signals with respect to the CLK signal. At power-up the receivers get configured for low speed operations. When operating at high frequencies, the receivers must be trained. The timing margins need to be readjusted per the higher clock frequency which is achieved with the CBT procedure. The entry and exit of the CBT mode are controlled by the mode register write command. In CBT mode, DRAM will switch to the FSP_OP settings, which it will also need to be trained on. DRAM samples the CA bus at CS signal and provides feedback of the sampled signals to the controller for timing adjustments on CS and CA signals.
- Write Leveling: This is used to adjust the delays on DQS input signals with respect to the CLK signal. The entry and exit of the write leveling training mode are controlled by the mode register write command. DQS signal gets driven by the controller and DRAM samples the CLK signal at the DQS edge. DRAM responds to the controller by providing feedback on the captured CLK level on DQ. This feedback identifies the leading or lagging of DQS, with respect to the CLK, so that controller can readjust the delays accordingly.
- Write Training (DQS-DQ Training): This is used to align the DQ input signal delays with respect to the DQS input signal. When entering write training mode, MPC WR_DQ_FIFO command must be issued by the controller. This command writes a user defined data in DRAM, then the controller issues MPC RD_DQ_FIFO command to read back the data from the same location and compare both the written and read data to re-adjust the delay on DQ line.

Source: https://blogs.synopsys.com/vip-central/2017/10/03/lpddr4-the-total-package-for-mobile-soc-ram/

Low Power Double Data Rate 5 (LPDDR5) **JESD209-5A**

(Revision of JESD209-5, December 2018)

4.2.2 Command Bus Training

The LPDDR5 SDRAM command bus must be trained before enabling termination for high-frequency or mid-frequency operation. LPDDR5 SDRAM provides an internal VREF(CA) that default level is suitable for un-terminated, low-frequency operation, however the VREF(CA) must be trained to achieve suitable receiver voltage margin for terminated, high-frequency or mid-frequency operation. The training mode described here centers the internal VREF(CA) in the CA data eye and at the same time allows for timing adjustments of the CS and CA signals to meet their Rx Mask requirements. For the training sequence simplicity and difficulty to capture CA inputs prior to training the CA inputs, the training mode described here uses a minimum of external commands to enter, train, and exit the Command Bus Training.

4.2.5 WCK2CK Leveling

4.2.5.1 WCK2CK Leveling Mode (write-leveling called in LPDDR4)

To adjust CK-to-WCK relationship and guarantee WCK2CK-Sync. operation, the LPDDR5 SDRAM provides a WCK2CK Leveling feature to compensate CK-to-WCK timing skew affecting WCK2CK-Sync. operation. The SDRAM compares the phase of the rising edge of WCK and the rising edge of CK, then asynchronously feeds back to the memory controller for the WCK2CK phase detection result. After finishing WCK2CK Leveling, tWCK2CK which means CK-to-WCK relationship is determined and WCK2CK-Sync. operation will be performed with the optimized margin.

4.2.9 WCK-DQ Training

The LPDDR5 SDRAM uses an un-matched WCK-DQ path to enable high speed performance and save power in the SDRAM. As a result, WCK is required to be trained to arrive at the DQ latch center-aligned with the Data eye. The SDRAM DQ receiver is located at the DQ pad and has a shorter internal delay in the SDRAM than does the WCK signal. The SDRAM DQ receiver will latch the data present on the DQ bus when WCK reaches the latch, and training is accomplished by delaying the DQ signals relative to WCK such that the Data eye arrives at the receiver latch centered on the WCK transition.

Source: JEDEC Standard No. 209-5A at 46, 75 & 90.

60. Claim 1 of the ’835 patent is reproduced below:

1. A method for automatically calibrating intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device, the method comprising:

generating command signals to access an integrated circuit component;

accessing data signals to convey data for the integrated circuit component;

accessing sampling signals to control sampling of the data signals; and

systematically altering a phase shift of the command signals, a phase shift of the data signals, and a phase shift of the sampling signals to determine a valid operation range of the integrated circuit device, wherein the valid operation range includes an optimal operation point for the integrated circuit device.

61. The Accused '835 Products each automatically calibrate intra-cycle timing relationships between command signals, data signals, and sampling signals for an integrated circuit device. For example, the Qualcomm Snapdragon 695 5G Mobile Platform requires LPDDR4X training of command, clocking and data symbols during initialization to establish critical timing relationships prior to normal operation, as seen below:

Low Power Double Data Rate 5 (LPDDR5) **JESD209-5A**

(Revision of JESD209-5, December 2018)

4.2.2 Command Bus Training

The LPDDR5 SDRAM command bus must be trained before enabling termination for high-frequency or mid-frequency operation. LPDDR5 SDRAM provides an internal VREF(CA) that default level is suitable for un-terminated, low-frequency operation, however the VREF(CA) must be trained to achieve suitable receiver voltage margin for terminated, high-frequency or mid-frequency operation. The training mode described here centers the internal VREF(CA) in the CA data eye and at the same time allows for timing adjustments of the CS and CA signals to meet their Rx Mask requirements. For the training sequence simplicity and difficulty to capture CA inputs prior to training the CA inputs, the training mode described here uses a minimum of external commands to enter, train, and exit the Command Bus Training.

4.2.5 WCK2CK Leveling

4.2.5.1 WCK2CK Leveling Mode (write-leveling called in LPDDR4)

To adjust CK-to-WCK relationship and guarantee WCK2CK-Sync. operation, the LPDDR5 SDRAM provides a WCK2CK Leveling feature to compensate CK-to-WCK timing skew affecting WCK2CK-Sync. operation. The SDRAM compares the phase of the rising edge of WCK and the rising edge of CK, then asynchronously feeds back to the memory controller for the WCK2CK phase detection result. After finishing WCK2CK Leveling, tWCK2CK which means CK-to-WCK relationship is determined and WCK2CK-Sync. operation will be performed with the optimized margin.

4.2.9 WCK-DQ Training

The LPDDR5 SDRAM uses an un-matched WCK-DQ path to enable high speed performance and save power in the SDRAM. As a result, WCK is required to be trained to arrive at the DQ latch center-aligned with the Data eye. The SDRAM DQ receiver is located at the DQ pad and has a shorter internal delay in the SDRAM than does the WCK signal. The SDRAM DQ receiver will latch the data present on the DQ bus when WCK reaches the latch, and training is accomplished by delaying the DQ signals relative to WCK such that the Data eye arrives at the receiver latch centered on the WCK transition.

Prior to normal operation, the LPDDR5 SDRAM is required to be initialized. The Power-Up, Initialization, and Power-off Procedure section provides detailed information covering device initialization.

Source: JEDEC Standard No. 209-5A at pp. 2, 46, 75 & 90.

62. Furthermore, the Accused '835 Products generate command signals to access an integrated circuit component. For example, the JEDEC LPDDR5 specification, JESD209-5A, specifies CA (command signals), DQ (data signals), and WCK (sampling signals) are used to

access a standard LPDDR5 memory, the CA signals providing the command and address input according to the Command Truth Table, as illustrated below:

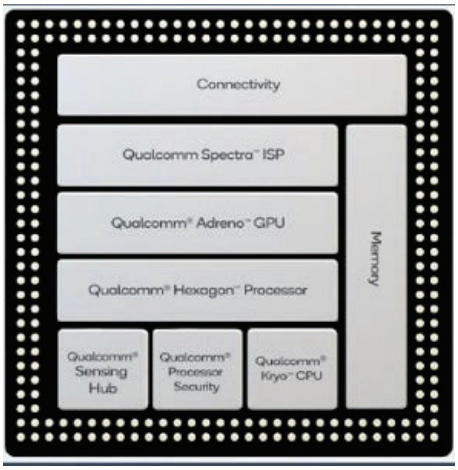
2.2.1 Pad Definition and Description

Table 1 — Pad Definition and Description

Symbol	Type	Description	Note
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) Command/Address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising(falling) edge of CK_t (CK_c) and second crossing point is falling(rising) edge of CK_t (CK_c). Single Data Rate (SDR) inputs, CS is sampled on the crossing point that is the rising(falling) edge of CK_t (CK_c).	
CS	Input	**Chip Select:** CS is part of the command code and is sampled on the rising(falling) edge of CK_t (CK_c) unless the device is in power-down or Deep Sleep mode where it becomes an asynchronous signal.	
CA[6:0]	Input	**Command/Address Inputs:** CA signals provide the Command and Address input according to the Command Truth Table	
DQ[15:0]	I/O	**Data Input/Output:** Bi-direction data bus.	
WCK[1:0]_t WCK[1:0]_c	Input	**Data Clocks:** WCK_t and WCK_c are differential clocks used for WRITE data capture and READ data output.	

SDRAM COMMAND
DESELECT (DES)
NO OPERATION (NOP)
POWER DOWN ENTRY (PDE)
ACTIVATE-1 (ACT-1)
ACTIVATE-2 (ACT-2)
PRECHARGE (PRE) (Per Bank, All Banks)
REFRESH (REF) (Per Bank, All Banks)
MASK WRITE (MWR)
WRITE (WR16 or WR)
WRITE32 (WR32)
READ (RD16 or RD)
READ32 (RD32)

Source: JEDEC Standard No. 209-5A at pp. 3, 165.



Source: https://www.dealntech.com/snapdragon-690-vs-snapdragon-765g/

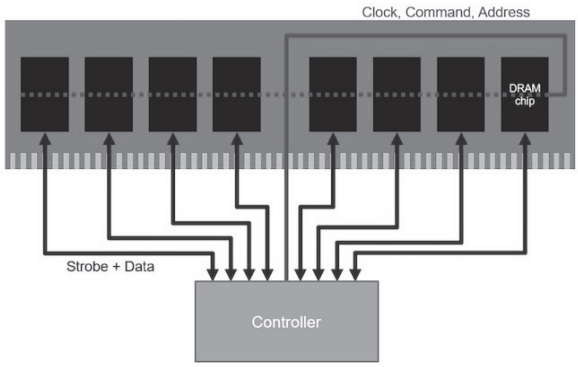
63. The Accused '835 Products access data signals to convey data for the integrated circuit component. For example, the Accused '835 Products, including the ET 40-HC/ET 45-HC family of tablets (with the Qualcomm Snapdragon 695 5G Mobile Platform), support LPDDR4X memory and access data I/O via a bi-directional data bus to convey data for the LPDDR4X memory, as seen below:

2.2.1 Pad Definition and Description

Table 1 — Pad Definition and Description

Symbol	Type	Description	Note
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) Command/Address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising(falling) edge of CK_t (CK_c) and second crossing point is falling(rising) edge of CK_t (CK_c). Single Data Rate (SDR) inputs, CS is sampled on the crossing point that is the rising(falling) edge of CK_t (CK_c).	
CS	Input	**Chip Select:** CS is part of the command code and is sampled on the rising(falling) edge of CK_t (CK_c) unless the device is in power-down or Deep Sleep mode where it becomes an asynchronous signal.	
CA[6:0]	Input	**Command/Address Inputs:** CA signals provide the Command and Address input according to the Command Truth Table	
DQ[15:0]	I/O	**Data Input/Output:** Bi-direction data bus.	
WCK[1:0]_t WCK[1:0]_c	Input	**Data Clocks:** WCK_t and WCK_c are differential clocks used for WRITE data capture and READ data output.	

Source: JEDEC Standard No. 209-5A at 3.



Source: https://www.signalintegrityjournal.com/blogs/8-for-good-measure/post/473-ddr-memory-interface-basics

4.2.9 WCK-DQ Training

The LPDDR5 SDRAM uses an un-matched WCK-DQ path to enable high speed performance and save power in the SDRAM. As a result, WCK is required to be trained to arrive at the DQ latch center-aligned with the Data eye. The SDRAM DQ receiver is located at the DQ pad and has a shorter internal delay in the SDRAM than does the WCK signal. The SDRAM DQ receiver will latch the data present on the DQ bus when WCK reaches the latch, and training is accomplished by delaying the DQ signals relative to WCK such that the Data eye arrives at the receiver latch centered on the WCK transition.

Source: JEDEC Standard No. 209-5A at p. 90

64. The Accused '835 Products access sampling signals to control sampling of the data signals. For example, the Accused '835 Products, including the ET 40-HC/ET 45-HC family of tablets (with the Qualcomm Snapdragon 695 5G Mobile Platform), support LPDDR4X memory and utilize WCK2CK Leveling, which accesses sampling signals to control sampling of the data signals, as illustrated below:

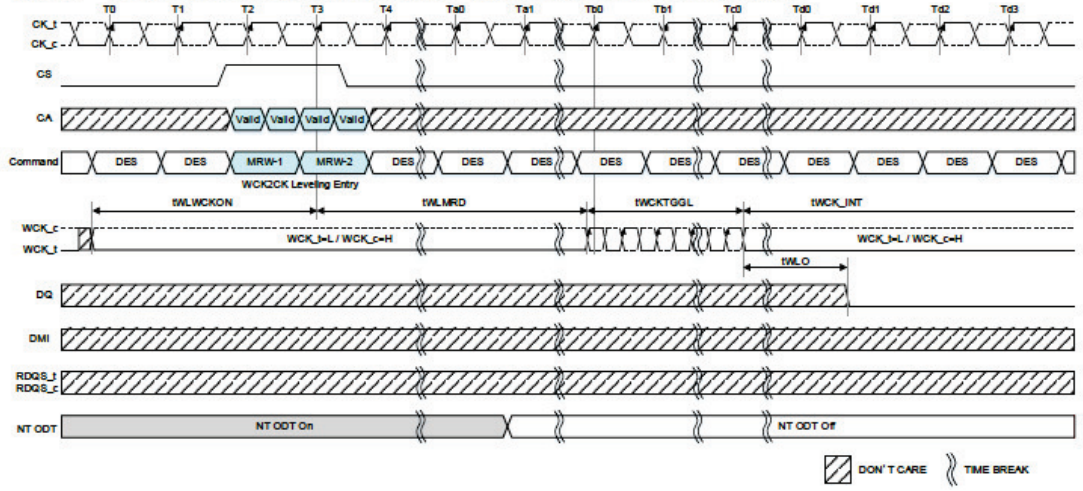
2.2.1 Pad Definition and Description

Table 1 — Pad Definition and Description

Symbol	Type	Description	Note
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) Command/Address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising(falling) edge of CK_t (CK_c) and second crossing point is falling(rising) edge of CK_t (CK_c). Single Data Rate (SDR) inputs, CS is sampled on the crossing point that is the rising(falling) edge of CK_t (CK_c).	
CS	Input	**Chip Select:** CS is part of the command code and is sampled on the rising(falling) edge of CK_t (CK_c) unless the device is in power-down or Deep Sleep mode where it becomes an asynchronous signal.	
CA[6:0]	Input	**Command/Address Inputs:** CA signals provide the Command and Address input according to the Command Truth Table	
DQ[15:0]	I/O	**Data Input/Output:** Bi-direction data bus.	
WCK[1:0]_t WCK[1:0]_c	Input	**Data Clocks:** WCK_t and WCK_c are differential clocks used for WRITE data capture and READ data output.	

Source: JEDEC Standard No. 209-5A at p. 3.

4.2.5.2 WCK2CK Leveling Procedure and Related AC parameters



Source: JEDEC Standard No. 209-5A at p. 76.

4.2.5 WCK2CK Leveling

4.2.5.1 WCK2CK Leveling Mode (write-leveling called in LPDDR4)

To adjust CK-to-WCK relationship and guarantee WCK2CK-Sync. operation, the LPDDR5 SDRAM provides a WCK2CK Leveling feature to compensate CK-to-WCK timing skew affecting WCK2CK-Sync. operation. The SDRAM compares the phase of the rising edge of WCK and the rising edge of CK, then asynchronously feeds back to the memory controller for the WCK2CK phase detection result. After finishing WCK2CK Leveling, tWCK2CK which means CK-to-WCK relationship is determined and WCK2CK-Sync. operation will be performed with the optimized margin.

Source: JEDEC Standard No. 209-5A at p. 75.

65. The Accused '835 Products systematically alter a phase shift of the command signals. For example, the Accused '835 Products, including the ET 40-HC/ET 45-HC family of tablets (with the Qualcomm Snapdragon 695 5G Mobile Platform), follow the JEDEC 209-5A standard, which explains that the Command Bus training (CA training) requires phase adjustments of the CS and CA signals to be implemented at initialization (i.e., powerup), prior to normal operation, as seen below:

4.2.2 Command Bus Training

The LPDDR5 SDRAM command bus must be trained before enabling termination for high-frequency or mid-frequency operation. LPDDR5 SDRAM provides an internal VREF(CA) that default level is suitable for un-terminated, low-frequency operation, however the VREF(CA) must be trained to achieve suitable receiver voltage margin for terminated, high-frequency or mid-frequency operation. The training mode described here centers the internal VREF(CA) in the CA data eye and at the same time allows for timing adjustments of the CS and CA signals to meet their Rx Mask requirements. For the training sequence simplicity and difficulty to capture CA inputs prior to training the CA inputs, the training mode described here uses a minimum of external commands to enter, train, and exit the Command Bus Training.

Once LPDDR5 SDRAM has entered CBT mode by MRW, only DES and MRW for exiting CBT mode are allowed.

The LPDDR5 SDRAM supports two Command Bus Training modes and their feature is as follows. CBT mode is selected by MR13 OP[6] (CBT mode1: MR13 OP[6] = 0_B, CBT mode2: MR13 OP[6] =1_B)

In multi-rank/channel system sharing the CA bus, the terminated die should be trained first, followed by the nonterminated die(s). See 7.6.4 for more information. For the WCK ODT setting in multi-rank/channel system, only one of SDRAM connected to a common WCK signal can set to CBT mode, the MR of Non-CBT trained SDRAM(s) is required to be set MR18 OP[2:0]=000_B.

The Corresponding DQ pins in this definition may differ depending on the package configuration. For example, in case of a package which contains Byte-mode devices, DQ[15:8] and DMI[1] balls can be connected to DQ[7:0] and DMI[0] pads of byte-mode device.

Source: JEDEC Standard No. 209-5A at p. 46.

Prior to normal operation, the LPDDR5 SDRAM is required to be initialized. The Power-Up, Initialization, and Power-off Procedure section provides detailed information covering device initialization.

Source: JEDEC Standard No. 209-5A at p. 2.

4.1.1 Voltage Ramp and Device Initialization (Cont'd)

7) Since LPDDR5 initial ZQ calibration is done automatically after ramp up, ZQ Latch command should be issued. After tZQLAT is satisfied (Th) the command bus (internal VREF(CA), CS, and CA) should be trained for high-speed operation by issuing MRW command (Command Bus Training Mode). This command is used to calibrate the SDRAM's internal VREF and align CS/CA with CK for high-speed operation. The LPDDR5 SDRAM will power-up with receivers configured for low-speed operations, and VREF(CA) set to a default factory setting. Normal SDRAM operation at clock speeds higher than tCKb may not be possible until command bus training has been completed.

Source: JEDEC Standard No. 209-5A at p. 28.

66. The Accused '835 Products systematically alter a phase shift of the data signals. For example, the Accused '835 Products, including the ET 40-HC/ET 45-HC family of tablets (with the Qualcomm Snapdragon 695 5G Mobile Platform), follow the JEDEC 209-5A standard, which explains that WCK-DQ training adjusts the timing (phase) of the data bus (data signals) during initialization (i.e., powerup), prior to normal operation, as illustrated below:

4.2.9 WCK-DQ Training

The LPDDR5 SDRAM uses an un-matched WCK-DQ path to enable high speed performance and save power in the SDRAM. As a result, WCK is required to be trained to arrive at the DQ latch center-aligned with the Data eye. The SDRAM DQ receiver is located at the DQ pad and has a shorter internal delay in the SDRAM than does the WCK signal. The SDRAM DQ receiver will latch the data present on the DQ bus when WCK reaches the latch, and training is accomplished by delaying the DQ signals relative to WCK such that the Data eye arrives at the receiver latch centered on the WCK transition.

The LPDDR5 SDRAM provides a Command-based FIFO Write/Read training operation using user specific pattern. Basically, DMI will be treated the same as DQs. It means that the Write Data send to FIFO for DMI by WFF command and these data can be read-out from FIFO for DMI by RFF command. On the other hand, DMI behavior is not same as DQs in some cases. Refer to the details about the special DMI behavior which are to be described later in this section.

Source: JEDEC Standard No. 209-5A at p. 90.

Prior to normal operation, the LPDDR5 SDRAM is required to be initialized. The Power-Up, Initialization, and Power-off Procedure section provides detailed information covering device initialization.

Source: JEDEC Standard No. 209-5A at p. 2.

4.1.1 Voltage Ramp and Device Initialization (Cont'd)

7) Since LPDDR5 initial ZQ calibration is done automatically after ramp up, ZQ Latch command should be issued. After tZQLAT is satisfied (Th) the command bus (internal VREF(CA), CS, and CA) should be trained for high-speed operation by issuing MRW command (Command Bus Training Mode). This command is used to calibrate the SDRAM's internal VREF and align CS/CA with CK for high-speed operation. The LPDDR5 SDRAM will power-up with receivers configured for low-speed operations, and VREF(CA) set to a default factory setting. Normal SDRAM operation at clock speeds higher than tCKb may not be possible until command bus training has been completed.

Source: JEDEC Standard No. 209-5A at p. 28.

67. The Accused '835 Products systematically alter a phase shift of the sampling signals. For example, the Accused '835 Products, including the ET 40-HC/ET 45-HC family of

tablets (with the Qualcomm Snapdragon 695 5G Mobile Platform), follow the JEDEC 209-5A standard, which explains that WCK2CK Leveling adjusts the timing (phase) of the WCK (sampling signals) during device initialization, prior to normal operation, as illustrated below:

4.2.5.1 WCK2CK Leveling Mode (write-leveling called in LPDDR4)

To adjust CK-to-WCK relationship and guarantee WCK2CK-Sync. operation, the LPDDR5 SDRAM provides a WCK2CK Leveling feature to compensate CK-to-WCK timing skew affecting WCK2CK-Sync. operation. The SDRAM compares the phase of the rising edge of WCK and the rising edge of CK, then asynchronously feeds back to the memory controller for the WCK2CK phase detection result. After finishing WCK2CK Leveling, tWCK2CK which means CK-to-WCK relationship is determined and WCK2CK-Sync. operation will be performed with the optimized margin.

The memory controller references WCK2CK-Sync feedback to adjust CK-to-WCK relationship for each WCK_t/WCK_c signal pair. All data bits (DQ[7:0] for WCK_t[0]/WCK_c[0], and DQ[15:8] for WCK_t[1]/WCK_c[1]) carry the training feedback to the controller.

CKR mode is required to be set 2:1 prior to entering WCK2CK leveling.

The LPDDR5 SDRAM enters into WCK2CK Leveling mode when mode register MR18-OP[6] is set HIGH. When WCK2CK Leveling mode is entered, the state of the DQ pins is undefined. During WCK2CK Leveling mode, only DESELECT commands are allowed, or MRW command to exit the WCK2CK Leveling operation. Upon completion of the WCK2CK Leveling, the SDRAM exits from WCK2CK Leveling mode when MR18-OP[6] is reset LOW.

WCK2CK Leveling should be performed before write training.

WCK2CK Leveling examples are shown in Figure 42 and Figure 43, and the specific descriptions for the figures will be provided in the following section.

Source: JEDEC Standard No. 209-5A at p. 75.

Prior to normal operation, the LPDDR5 SDRAM is required to be initialized. The Power-Up, Initialization, and Power-off Procedure section provides detailed information covering device initialization.

Source: JEDEC Standard No. 209-5A at p. 2.

4.1.1 Voltage Ramp and Device Initialization (Cont'd)

7) Since LPDDR5 initial ZQ calibration is done automatically after ramp up, ZQ Latch command should be issued. After tZQLAT is satisfied (Th) the command bus (internal VREF(CA), CS, and CA) should be trained for high-speed operation by issuing MRW command (Command Bus Training Mode). This command is used to calibrate the SDRAM's internal VREF and align CS/CA with CK for high-speed operation. The LPDDR5 SDRAM will power-up with receivers configured for low-speed operations, and VREF(CA) set to a default factory setting. Normal SDRAM operation at clock speeds higher than tCKb may not be possible until command bus training has been completed.

Source: JEDEC Standard No. 209-5A at p. 28.

68. The Accused '835 Products systematically alter the phase shift of the command signals, the phase shift of the data signals, and the phase shift of the sampling signals to determine a valid operation range of the integrated circuit device, wherein the valid operation range includes an optimal operation point for the integrated circuit device. For example, the Accused '835 Products, including the ET 40-HC/ET 45-HC family of tablets (with the Qualcomm Snapdragon

695 5G Mobile Platform), use LPDDR4X memory operating at a maximum speed of 2200 MHz and requires LPDDR4X signal training to meet the tighter timing requirements of the LPDDR4X standard, notwithstanding delays in the memory controller and memory components introduced by myriad factors such as variations inherent in manufacturing processes, and varying conditions such as temperature and voltage. The training flow includes command bus training (including altering a phase shift of the command signals), WCK2CK Leveling (including altering a phase shift of the sampling signals) and WCK-DQ training (including altering a phase shift of the data signals).

4.2.2 Command Bus Training

4) At time tCAENT later, LPDDR5 SDRAM can accept to input CA training pattern via CA bus.
5) To verify that the receiver has the correct VREF(CA) setting and to further train the CA eye relative to clock(CK), values latched at the receiver on the CA bus are asynchronously output to the DQ bus.
6) To exit Command Bus Training mode, drive DQ[7] LOW and after time tDQ7LWCK + tVREFCA_LONG issue the MRW command to set MR16 OP[5:4] = 00_B. After time tMRD the LPDDR5 SDRAM is ready for normal operation. After training exit, the LPDDR5 SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training.

4.2.5.2 WCK2CK Leveling Procedure

4. Toggle WCK signal 7.5 cycles for WCK2CK phase detection. SDRAM may or may not capture the first rising edge of WCK_t due to an unstable first rising edge. Hence providing exactly 7.5 cycles of WCK signal input is required in every WCK input signal during WCK2CK training mode. SDRAM provides asynchronous feedback of last captured WCK2CK phase information during WCK toggles, on all the DQ bits after time tWLO. DQ output is low if WCK phase is earlier than CK phase and high if WCK phase is later than CK phase. The controller must sample the phase relation result on DQ after satisfying tWLO.
5. The feedback provided by the SDRAM is referenced by the controller to increment or decrement the WCK_t and WCK_c delay setting. The controller can adjust the WCK delay setting only when it drives WCK_t LOW and WCK_c HIGH to prevent any glitches in WCK signal. WCK search range from controller is defined as tWCK2CK_leveling ac parameter. Refer to the tWCK2CK_leveling value in Table 30.
6. Repeat step 4 through step 5 until the proper WCK_t/WCK_c delay is established.

4.2.9 WCK-DQ Training

The LPDDR5 SDRAM uses an un-matched WCK-DQ path to enable high speed performance and save power in the SDRAM. As a result, WCK is required to be trained to arrive at the DQ latch center-aligned with the Data eye. The SDRAM DQ receiver is located at the DQ pad and has a shorter internal delay in the SDRAM than does the WCK signal. The SDRAM DQ receiver will latch the data present on the DQ bus when WCK reaches the latch, and training is accomplished by delaying the DQ signals relative to WCK such that the Data eye arrives at the receiver latch centered on the WCK transition.

Source: JEDEC Standard No. 209-5A at 46-47, at pp. 77 & 90.

Prior to normal operation, the LPDDR5 SDRAM is required to be initialized. The Power-Up, Initialization, and Power-off Procedure section provides detailed information covering device initialization.

4.1.1 Voltage Ramp and Device Initialization

The following sequence shall be used to power up the LPDDR5 SDRAM. Unless specified otherwise, these steps are mandatory.

4.1.1 Voltage Ramp and Device Initialization (Cont'd)

7) Since LPDDR5 initial ZQ calibration is done automatically after ramp up, ZQ Latch command should be issued. After tZQLAT is satisfied (Th) the command bus (internal VREF(CA), CS, and CA) should be trained for high-speed operation by issuing MRW command (Command Bus Training Mode). This command is used to calibrate the SDRAM's internal VREF and align CS/CA with CK for high-speed operation. The LPDDR5 SDRAM will power-up with receivers configured for low-speed operations, and VREF(CA) set to a default factory setting. Normal SDRAM operation at clock speeds higher than tCKb may not be possible until command bus training has been completed.

   NOTE 1 The command bus training MRW command uses the CA bus as inputs for the calibration data stream, and outputs the results asynchronously on the DQ bus. See 4.2.2 for information on how to enter/exit the training mode.

8) After command bus training, DRAM controller must perform WCK2CK leveling. WCK2CK leveling mode is enabled when MR18-OP[6] is high (Ti). See 4.2.5.2 for detailed description of WCK2CK leveling entry and exit sequence. After finishing WCK2CK Leveling, tWCK2CK which means CK-to-WCK relationship is determined and WCK2CK-Sync. operation will be performed with the optimized margin.

9) After WCK2CK leveling, the DQ Bus (internal VREF(DQ), WCK, and DQ) should be trained for high-speed operation using the training commands (RD FIFO / WT FIFO / RD DQ Calibration) described in command truth table and by issuing MRW commands to adjust VREF(DQ)(Ti). The LPDDR5 SDRAM will power-up with receivers configured for low-speed operations and VREF(DQ) set to a default factory setting. Normal SDRAM operation at clock speeds higher than tCKb should not be attempted until DQ Bus training has been completed. The Read DQ Calibration command is used together with FIFO Write/Read commands to train DQ bus without disturbing the memory array contents. See 4.2.9 for detailed DQ Bus Training sequence.

Source: JEDEC Standard No. 209-5A at 46-47, at pp. 2, 28.

69. Additionally, Defendant has been, and currently is, an active inducer of infringement of the '835 patent under 35 U.S.C. § 271(b) and a contributory infringer of the '835 patent under 35 U.S.C. § 271(c).

70. Defendant has actively induced, and continues to actively induce, infringement of the '835 patent by causing others to use, offer for sale, or sell in the United States, products or services covered by the '835 patent, including but not limited to the '835 Accused Products and any other products or services that include Qualcomm processors and LPDDR4, LPDDR4X, or LPDDR5 memory, or products and services with the same or substantially similar functionality to that described above. Defendant provides these products and services to others, such as customers, resellers, partners, and end-users, who, in turn, use, provision for use, offer for sale, or sell those products and services, which directly infringe the '835 patent as described above. Defendant's inducement includes requiring memory chips within the Accused Products to be compliant with

the JESD209-5A JEDEC standard for Low Power Double Data Rate 5 (LPDDR5), in which the calibration of timing relationships between command signals, data signals and sampling signals described above is mandatory, and advertising and promoting such compliance to its customers, partners, re-sellers and the like, including the promotion, directions and instructions found at one or more of the following links, the provision of which is on-going as of the filing of this Complaint and much of the content of which is specifically illustrated above:

- https://www.zebra.com/us/en/products/spec-sheets/tablets/et40-hc-et45-hc.html
- https://www.zebra.com/us/en/products/spec-sheets/mobile-computers/handheld/tc51-tc56.html
- https://www.zebra.com/us/en/products/spec-sheets/mobile-computers/handheld/mc9300.html
- https://www.zebra.com/us/en/products/spec-sheets/mobile-computers/handheld/tc52-tc57.html
- https://www.zebra.com/content/dam/zebra_new_ia/en-us/solutions-verticals/product/Mobile_Computers/GENERAL/brochures/mobile-computing-at-a-glance-brochure.pdf
- https://www.zebra.com/us/en/products/spec-sheets/mobile-computers/handheld/mc3300x.html
- https://www.zebra.com/us/en/products/spec-sheets/mobile-computers/handheld/tc8300.html

71. Defendant has contributed to, and continues to contribute to, the infringement of the ’835 patent by others by knowingly providing one or more components, for example the Qualcomm processors and LPDDR4, LPDDR4X and LPDDR5 complaint memory included in the Accused Products, a portion thereof, and/or the software/hardware modules responsible for the accused functionality described herein, that, when installed, configured, and used result in systems that, as intended by Defendant described above, directly infringe one or more claims of the ’835 patent.

72. Defendant knew of the ’835 patent, or should have known of the ’835 patent, but was willfully blind to its existence. Upon information and belief, Defendant had actual knowledge

of the ’835 patent at least as early as early as Defendant received a copy of this Complaint, or alternatively, at least as early as the service upon Defendant of the Complaint in this action.

73. By the time of trial, Defendant will or should have known and intended (since receiving such notice) that its continued actions would infringe and would actively induce and contribute to the infringement of the ’835 patent.

74. Defendant has committed, and continues to commit, contributory infringement by selling products and services that directly infringe the ’835 patent when used by a third party, such as the Accused ’835 Products, and that are a material part of the invention, knowing them to be especially made or adapted for use in infringement of the ’835 patent and not staple articles or commodities of commerce suitable for substantial non-infringing use.

75. As a result of Defendant’s acts of infringement, IV has suffered and will continue to suffer damages in an amount to be determined at trial.

PRAYER FOR RELIEF

IV requests that the Court enter judgment as follows:

(A) that Defendant has infringed the ’439 patent;

(B) that Defendant has infringed the ’835 patent;

(C) awarding damages sufficient to compensate IV for Defendant’s infringement under 35 U.S.C. § 284;

(D) finding this case exceptional under 35 U.S.C. § 285 and awarding IV its reasonable attorneys’ fees;

(E) awarding IV its costs and expenses incurred in this action;

(F) awarding IV prejudgment and post-judgment interest; and

(G) granting IV such further relief as the Court deems just and appropriate.

DEMAND FOR JURY TRIAL

IV demands trial by jury of all claims so triable under Federal Rule of Civil Procedure 38.

Dated: April 20, 2023.

Respectfully submitted,

/s/Karl Rupp

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