UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

INTELLECTUAL VENTURES I LLC and INTELLECTUAL VENTURES II LLC, Plaintiff, v. TCL ELECTRONICS HOLDINGS LTD. and TCL INDUSTRIES HOLDINGS CO., LTD., Defendant.	Civil Action No. 6:23-cv-293 **JURY TRIAL DEMANDED**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiffs, Intellectual Ventures I LLC ("Intellectual Ventures I") and Intellectual Ventures II LLC ("Intellectual Ventures II") (together "IV"), for its complaint against Defendants TCL Electronics Holdings Ltd. and TCL Industries Holdings Co., Ltd (together "TCL"), hereby allege:

THE PARTIES

1. Intellectual Ventures II is a Delaware limited liability company having its principal place of business located at 3150 139th Avenue SE, Bellevue, Washington 98005.

2. Defendant TCL Electronics Holdings Limited ("TCL Electronics") is a limited liability company organized and existing under the laws of the Cayman Islands with a principal place of business located at 9 Floor, TCL Electronics Holdings Limited Building, TCL International E City, #1001 Zhongshan Park Road, Nanshan District, Shenzhen, Guangdong, 518067 P.R. China. Upon information and belief, TCL Electronics Holdings Limited also has a location at 7/F, TCL Building, 22 Science Park E, Hong Kong Science Park, Shatin, New Territories, Hong Kong, S.A.R. TCL Electronics may also be served with process by serving the

Texas Secretary of State, 1019 Brazos Street, Austin, Texas 78701, as its agent for service because it engages in business in Texas but has not designated or maintained a resident agent for service of process in Texas as required by statute. This action arises out of that business.

3. Defendant TCL Industries Holdings Co., Ltd. ("TCL Industries") is a Chinese company with a principal place of business at 13/F, TCL Tower, 8 Tai Chung Road Tsuen Wan, New Territories, Hong Kong, SAR. TCL Electronics may also be served with process by serving the Texas Secretary of State, 1019 Brazos Street, Austin, Texas 78701, as its agent for service because it engages in business in Texas but has not designated or maintained a resident agent for service of process in Texas as required by statute. This action arises out of that business.

4. TCL Electronics and TCL Industries are part of an interrelated group of companies which together comprise one of the world's largest manufacturers of televisions and smartphones and one of the leading sellers of televisions and smartphones in the United States, including the TCL brands. TCL, which refers to the company and its subsidiaries as the "Group," describes itself as one of the "world's leading consumer electronics company"[1] and states that the Group is "mainly involved in the manufacture and sale of television ('TV') sets, smart mobile, smart connective devices and services, smart commercial display and smart home products and provision of Internet platform operating services.[2]

5. TCL Electronics and TCL Industries and their affiliates are part of the same corporate structure and distribution chain for the making, importing, offering to sell, selling, and using of the accused devices in the United States, including in the State of Texas generally and this judicial district in particular.

[1] TCL Electronics Holdings Limited Annual Report 2020, at 5/319, https://doc.irasia.com/listco/hk/tclelectronics/annual/2020/ar2020.pdf.
[2] *See supra* note 1, at 141/319.

6. Upon information and belief, TCL Electronics, TCL Industries and each member of the "Group" share the same management, common ownership, advertising platforms, facilities, distribution chains and platforms, and have acted in concert with respect to the facts alleged herein such that any action of TCL Electronics or TCL Industries is attributable to every member of the "Group" and vice versa.

NATURE OF THE ACTION, JURISDICTION, AND VENUE

7. IV brings this action for patent infringement pursuant to 35 U.S.C. § 271, *et seq.* This Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

8. This Court has personal jurisdiction over TCL. TCL conducts business and has committed acts of direct and indirect infringement in this District, the State of Texas, and elsewhere in the United States. Moreover, TCL actively directs its activities to customers located in the State of Texas and this District.

9. For example, on information and belief TCL Group members, acting at the direction of TCL, sell within this District, the State of Texas and elsewhere in the United States products accused of infringement in this case.

10. Venue is proper in this District under 28 U.S.C. § 1391(c) because TCL is a foreign corporation. In addition, TCL has committed acts of patent infringement in this District and IV has suffered harm in this District.

FACTUAL BACKGROUND

11. Intellectual Ventures Management, LLC ("Intellectual Ventures") was founded in 2000. Intellectual Ventures fosters inventions and facilitates the filing of patent applications for those inventions; collaborates with others to develop and patent inventions; and acquires and licenses patents from individual inventors, universities, corporations, and other institutions. A

significant aspect of Intellectual Ventures' business is managing the plaintiffs in this case, Intellectual Ventures I and Intellectual Ventures II.

12. One founder of Intellectual Ventures is Nathan Myhrvold, who worked at Microsoft from 1986 until 2000 in a variety of executive positions, culminating in his appointment as the company's first Chief Technology Officer ("CTO") in 1996. While at Microsoft, Dr. Myhrvold founded Microsoft Research in 1991 and was one of the world's foremost software experts. Between 1986 and 2000, Microsoft became the world's largest technology company.

13. Under Dr. Myhrvold's leadership, Intellectual Ventures acquired thousands of patents covering many important inventions of the Internet era, including many pertaining to the networked computers that comprise the Internet. Many of these inventions coincided with Dr. Myhrvold's successful tenure at Microsoft.

Microprocessor Clocking

14. One area of particular and continuing importance in the computer era is that, as microprocessors grow in frequency and dimension, microprocessor clocks have become increasingly limited by wire delays. For example, the Pentium III microprocessor broke the 1 GHz barrier in 2000, and speeds have continued to increase ever since. At the same time, due to issues of reliability and performance, wire dimensions have been scaled in successive process generations more conservatively than transistor dimensions. The result of these frequency and dimensional trends is that microprocessor clock speeds became increasingly limited by wire delays, so much so that some of the subsequent microprocessors, e.g., the Pentium IV, had pipeline stages solely dedicated to moving clock signals across the chip.

15. Furthermore, a growing challenge has been to distribute the clock across a progressively larger die to increasing numbers of latches while meeting a decreasing clock skew

budget. Researchers concluded that in order to continue the pace of clock frequency increases, microprocessor designers would be forced to abandon singly clocked globally synchronous systems in favor of some form of asynchrony.

16. Although purely asynchronous systems have the potential for higher performance and lower power compared to their synchronous counterparts, major corporations in the early 2000s were initially reluctant to fully migrate to asynchronous design methodologies. Two major reasons for this reluctance were the immaturity of asynchronous design tools relative to those in the synchronous domain, and the cost and risk of moving away from the mature design infrastructures rooted in synchronous systems that have been successfully used to create many generations of microprocessor products.

17. To address the issues identified above, David H. Albonesi led a team of professors and graduate students at the University of Rochester in developing a multiple clock domain microarchitecture that uses a globally asynchronous, locally synchronous clocking style.

18. Defendant makes, uses, and sells devices that include embedded ARM Cortex-Axx processors, as well as purpose-built software that supports operation of those processors.

Cyclic Diversity

19. A further area of importance in today's computing environments is that as wireless communications systems are widely deployed to provide various types of communications, demand for increased data rates has skyrocketed. This has led wireless system providers to develop new techniques for increasing data rates within the limited available radio frequency (RF) spectrum. One of these advancements has been the use of orthogonal frequency division multiplexing (OFDM) transmission. In OFDM transmissions, a radio channel is divided into a large number of closely spaced subchannels, an outgoing bitstream representing data to be

transmitted is divided into multiple sub-bitstreams, and each sub-bitstream is transmitted over a subchannel in parallel with other sub-bitstreams that are each transmitted over their respective subchannels. Each such sub-bitstream is comprised of a series of symbols, that is, a waveform of the communication channel that persists for a fixed period of time, and from which data can be extracted by taking samples (i.e., measuring segments) of that waveform. Each of the symbols is separated by a guard interval (a gap in time between successive symbols that provides a buffer making transmission channels more resilient against the effects of a multipath propagation). The main advantages of OFDM is its ability to cope with severe channel conditions (e.g., signal fading, echoes, and interference).

20. As technology continued to advance, demand for increased speed and reduced interference resulted in the implementation of further improvements such as using multiple antennas in a single device, sometimes referred to as multiple input, multiple output (MIMO), which enables simultaneous or substantially simultaneous transmission of multiple bitstreams/sub-bitstreams in the same RF spectrum. When combined with OFDM, MIMO increases speed and improves reliability, however, it also introduces challenges, particularly when a multi-antenna MIMO enabled transmitter is communicating with a single antenna single input, single output (SISO), receiver device. For example, signals transmitted from the MIMO transmitter may follow direct paths and multipaths to the SIS receiver, which can result in constructive interference (when multiple signals interact with one another to increase their amplitudes) or destructive interference (when multiple signals interact with one another to decrease their amplitudes), thus increasing packet error rates and causing other unwanted behavior that degraded the network quality.

21. One way that prior art systems addressed these inefficiencies was by implementing linear diversity schemes in which the transmission of one signal from a MIMO system is delayed

relative to another signal from the MIMO system. Linear diversity schemes tend to reduce constructive and destructive interference by temporally decorrelating the transmissions of two signals, but they resulted in other problems such as one of the signals occupying the other's guard interval.

22. To address the inefficiencies set out above, cyclic diversity schemes were implemented (e.g., the cyclic-delay diversity scheme). In the cyclic-delay diversity scheme each of two or more transmitters send the same data in a respective stream of symbols, but cyclically offset one spatial stream vis-a-vis the other by a defined number of samples resulting in a circular shift of all the samples in a particular symbol (or part thereof). By introducing a relatively small cyclic delay to a first transmitted MIMO signal relative to a second transmitted MIMO signals, those of skill in the art were able to substantially reduce the problems set out above. But, by introducing a small cyclic delay between the first and second MIMO signals, upon receipt sometimes the receiver would be unable to determine whether the cyclic delay was intentional or caused by environmental or other factors. This inability in turn led to the receiver incorrectly assuming an attempt by the transmitter to beamform, which occurs when antennas are intentionally electronically steered to adjust the phase and amplitude of a transmitted signal at each antenna, such that the signals combine constructively in the desired direction and destructively in other directions. That is, small cyclic delays were causing unintentional beamforming.

23. To address these and other problems in the art Mark Webster and Michael Seals, at the time engineers for Conexant Systems, developed improved systems and methods of wireless communication, which include, but are not limited to, an improved signal transmitting system capable of manipulating OFDM data packets and data streams using a cyclic diversity scheme

based on cyclic advancement rather than cyclic delay, thereby improving packet reception performance and reducing packet error rates, among other benefits.

24. Defendant makes, uses, and sells devices that include embedded wireless 802.11n, 802.11ac and 802.11ax compliant chipsets configured to use MIMO and OFDMA with a cyclic shift diversity feature compliant with the respective 802.11 standard, such as the TCL 30 V 5G smartphones.

THE PATENTS-IN-SUIT

25. On August 8, 2006, the United States Patent and Trademark Office issued United States Patent No. 7,089,443 ("the '443 patent"), titled MULTIPLE CLOCK DOMAIN MICROPROCESSOR. The '443 patent is valid and enforceable.

26. Intellectual Ventures II LLC is the exclusive licensee of the '443 patent and has the right to sue and recover damages for any current or past infringement of the '443 patent.

27. The '443 patent is directed to a multiple clock domain ("MCD") microarchitecture. In an MCD microprocessor, each functional block operates with a separately generated clock, while synchronizing circuits ensure reliable inter-domain communication.

28. The inventions claimed in the '443 patent were conceived by David Albonesi, Greg Semeraro, Grigorios Magklis, Michael L. Scott, Rajeev Balasubramonian and Sandhya Dwarkadas at the University of Rochester. The first named inventor, Dr. Albonesi, is currently a full professor and the Associate Director of the School of Electrical and Computer Engineering at Cornell University, where he focuses on power-efficient computer architecture.

29. On November 24, 2009, the United States Patent and Trademark Office issued United States Patent No. 7,623,439 ("the '439 patent"), titled CYCLIC DIVERSITY SYSTEMS AND METHODS. The '439 patent is valid and enforceable.

30. Intellectual Ventures I LLC is the owner and assignee of all rights, title, and interest in the '439 patent, including the rights to grant licenses, to exclude others, and to recover past damages for infringement of that patent.

31. The '439 patent is directed to a system and method for transmitting OFDM signals from a multiple antenna transmitting device. The system is able to manipulate an OFDM signal using a cyclic advancement scheme whereby a portion of sampled symbol data from packets comprising the OFDM signal are shifted (advanced) into the guard interval of the packet relative to a first non-shifted version of the packet. The system and method then allow for the substantially simultaneous transmission of the respective packets from different antenna in the transmitting device, thereby allowing a receiver to more easily acquire and correlate the received data.

32. The inventions claimed in the '439 patent were conceived by Mark Webster and Michael Seals, both of whom were engineers at Conexant Systems, a well-known software developer and fabless semiconductor company specializing in, among other things, developing technology for voice and audio processing. Mr. Webster is currently employed by L3Harris Technologies as a Senior Scientist, while Mr. Seals is a Principal Systems Engineer at Thales Group.

COUNT I

(Defendant's Infringement of U.S. Patent No. 7,089,443)

33. The preceding paragraphs are reincorporated by reference as if fully set forth herein.

34. The'443 patent claims and teaches, *inter alia*, an improved way to provide for future frequency increases, while maintaining a synchronous design methodology and exploiting the trend towards making functional blocks more autonomous.

35. The inventions improved upon then-existing microprocessor design by creating a MCD microarchitecture which uses a globally asynchronous locally synchronous clocking style. This microarchitecture afforded a number of technical solutions to unsolved, technical problems, with notable advantages over a singly and globally clocked design, more fully discussed below.

36. The inventions claimed in the ’443 patent allowed for more autonomous functional blocks operating under more independent local domain clocks, which implies less onerous global clock distribution requirements, permitting potentially higher frequencies within each domain and greater scalability in future process generations.

37. The inventions claimed in the ’443 patent further allowed for the designers of each domain to no longer be as constrained by the speeds of critical paths in other domains, affording them greater freedom in each domain to optimize the tradeoffs among clock speed, latency, and the exploitation of application parallelism via complex hardware structures.

38. The inventions claimed in the ’443 patent further allowed for the use of separate voltage inputs, external voltage regulators, and controllable clock frequency circuits in each clock domain, which in turned allowed for finer-grained dynamic voltage and frequency scaling, and thus lower energy, than could be achieved with single clock, single-core-voltage systems.

39. The inventions claimed in the ’443 patent further allowed for the ability to dynamically alter the clock speed in each domain, which in turn meant that the clock rate tradeoff could be tailored to application characteristics within each individual domain, thereby improving both performance and energy efficiency.

40. More specifically, the claims of the ’443 patent recite a multiple-clock-domain microprocessor. The system covered by the asserted claims includes a plurality of domains. It further includes, for each of the plurality of domains, a clock for separately generating a clock

signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains. And it includes, for each of the plurality of domains, a voltage input for receiving a voltage which is dynamically changeable independently of the voltages applied to said others of the plurality of domains.

41. The system covered by the asserted claims, therefore, differs markedly from the prior systems in use at the time of this invention, which lacked the claimed combination of the plurality of domains with clocks generating clock signals at frequencies for each of the domains, wherein the frequency is dynamically changeable independently of the frequencies for the clock signals generated in the other domains; and the plurality of domains with voltage input for receiving voltage which is dynamically changeable independently of the voltages applied in the other domains.

42. Defendant has directly infringed, and continues to directly infringe, at least claim 1 of the ’443 patent by making, using, testing, selling, offering for sale, and importing products and services covered by the ’443 patent. Defendant’s products and services that infringe the ’443 patent include all products and services that include Arm Cortex-Axx processors, such as the TCL 30 V 5G smartphones, and any other TCL devices that include an ARM-based processor with substantially the same functionality as described below, (together the “Accused ’443 Products” or “Accused Products”).

43. Claim 1 of the ’443 patent is reproduced below:

> *1. A multiple clock domain microprocessor comprising:*
>
> *a plurality of domains;*
>
> *for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being*

dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains; and

for each of the plurality of domains, a voltage input for receiving a voltage which is dynamically changeable independently of the voltages applied to said others of the plurality of domains.

44. The Accused '443 Products each provide an MCD microprocessor. As one example, the Accused '443 Products are products that include a MCD microprocessor, such as the TCL 30 V 5G, which includes an Octa-Core Processor with a combination of Arm Cortex A-76 and Arm Cortex A-55 cores in a scalable DynamIQ big.LITTLE configuration, as seen below:

MODEL T781S-2AUHUS11

30 V 5G

★★★★★ 5.0 (3) Write a review

- 6.67" FHD+ NXTVISION display
- 50MP AI triple rear camera system
- 16MP front-facing camera featuring AI Color mode for breathtaking portraits.
- Up to 128GB of internal memory, expandable up to 1TB via microSD™ card (sold separately).
- 4500mAh quick-charging battery provides up to 24 hours of usage on one charge.
- Qualcomm® Snapdragon™ 480 5G Chipset, Octa-core processor, and 4GB of RAM for a smooth performance.
- Facial Unlock and a quick-launching fingerprint sensor for fast and secure access to your favorite apps.

Source: https://www.tcl.com/us/en/products/mobile/tcl-30-series/tcl-30-v-5g

The SD480 is manufactured in the modern 8nm process and should be very energy efficient.

Series	Qualcomm Snapdragon
Codename	Cortex-A76 / 55
Series: Snapdragon Cortex-A76 / 55	
Qualcomm Snapdragon 480 Plus 5G	1.8 - 2.2 GHz 8 / 8 Cortex-A76 / 55
Qualcomm Snapdragon 480 5G «	1.8 - 2 GHz 8 / 8 Cortex-A76 / 55
Clock Rate	1800 - 2000 MHz
Number of Cores / Threads	8 / 8
Manufacturing Technology	8 nm
Features	Adreno 619 GPU, X51 5G Modem, FastConnect Wi-Fi 6 2x2, Spectra 345 ISP, Quick Charge 4+
GPU	Qualcomm Adreno 619
64 Bit	64 Bit support
Architecture	ARM
Announcement Date	01/04/2021 = 789 days old
Product Link (external)	Qualcomm Snapdragon SD 480

Source: https://www.notebookcheck.net/Qualcomm-Snapdragon-480-5G-Processor-Benchmarks-and-Specs.537294.0.html

Specifications

The Arm Cortex-A76 CPU delivers laptop-class performance with smartphone efficiency, bringing the same experience to all classes of intelligent mobile compute devices.

The second generation premium core built on DynamIQ technology. Paired with a Cortex-A55 CPU in a scalable DynamIQ big.LITTLE configuration, Cortex-A76 delivers laptop-class performance with mobile efficiency, bringing the mobile experience (fast responsiveness, always on, always connected) into all classes of intelligent mobile compute devices. With superior energy efficiency and far greater single-threaded performance, Cortex-A76 CPU extends battery life and improves user experience for sustained high performance across even the most complex compute tasks.

Source: https://developer.arm.com/ip-products/processors/cortex-a/cortex-a76

A1.1 About the core

The Cortex-A76 core is a high-performance and low-power Arm product that implements the Armv8-A architecture.

The Cortex-A76 core supports:

- The Armv8.2-A extension.
- The RAS extension.
- The Load acquire (LDAPR) instructions introduced in the Armv8.3-A extension
- The Dot Product support instructions introduced in the Armv8.4-A extension.
- The PSTATE *Speculative Store Bypass Safe* (SSBS) bit and the speculation barriers (CSDB, SSBB, PSSBB) instructions introduced in the Armv8.5-A extension.

The Cortex-A76 core has a *Level 1* (L1) memory system and a private, integrated *Level 2* (L2) cache. It also includes a superscalar, variable-length, out-of-order pipeline.

The Cortex-A76 core is implemented inside the *DynamIQ Shared Unit* (DSU) cluster. For more information, see the *Arm® DynamIQ™ Shared Unit Technical Reference Manual*.

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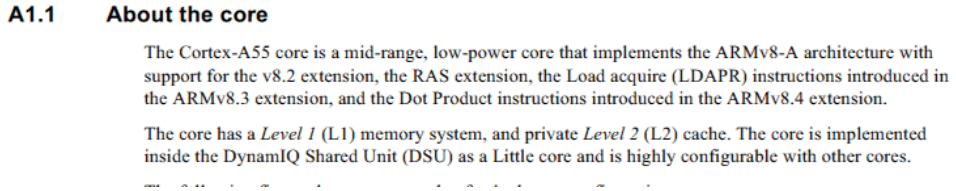


A1.1 About the core

The Cortex-A55 core is a mid-range, low-power core that implements the ARMv8-A architecture with support for the v8.2 extension, the RAS extension, the Load acquire (LDAPR) instructions introduced in the ARMv8.3 extension, and the Dot Product instructions introduced in the ARMv8.4 extension.

The core has a *Level 1* (L1) memory system, and private *Level 2* (L2) cache. The core is implemented inside the DynamIQ Shared Unit (DSU) as a Little core and is highly configurable with other cores.

Source: https://documentation-service.arm.com/static/5e7e1405b471823cb9de57ae?token=

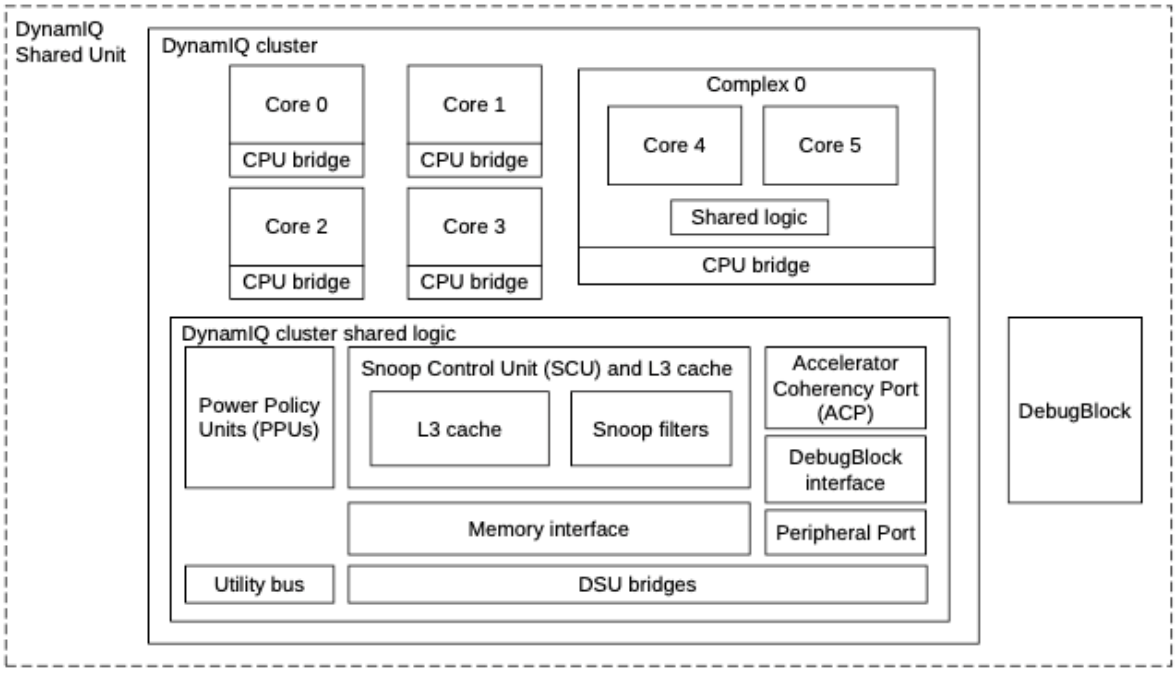
Feature	Cortex-A55	Cortex-A76
Architecture	Armv8.2-A	Armv8.2-A (AArch32 at EL0 only)

Source: https://developer.arm.com/documentation/102826/latest/

45. Furthermore, the Accused '443 Products each comprise a MCD microprocessor with plurality of domains. For example, the Accused Products include a MCD microprocessor with multiple domains, such as any one of the individual cores and its CPU bridge (e.g., Core 0 and its CPU bridge) from the DynamIQ cluster ("User Core"), in combination with the DynamIQ cluster shared logic/unit ("DSU") including the L3 cache and snoop filters, which collectively comprise an MCD microprocessor. That MCD processor has a domain that includes Core 0 and another domain that includes the DSU.

The *DynamIQ™ Shared Unit-110* (DSU-110) provides a shared L3 memory system, snoop control and filtering, and other control logic to support a cluster of A-class architecture cores. The cluster is called the DSU-110 DynamIQ™ cluster. Additionally, all the external interfaces to *System on Chip* (SoC) are provided through the DSU-110.

Figure 2-1: DSU-110 DynamIQ™ cluster



A DSU-110 DynamIQ™ cluster consists of between one and eight cores, with up to three different types of cores in the same cluster. Cores can be configured for various performance points during macrocell implementation and run at different frequencies and voltages.

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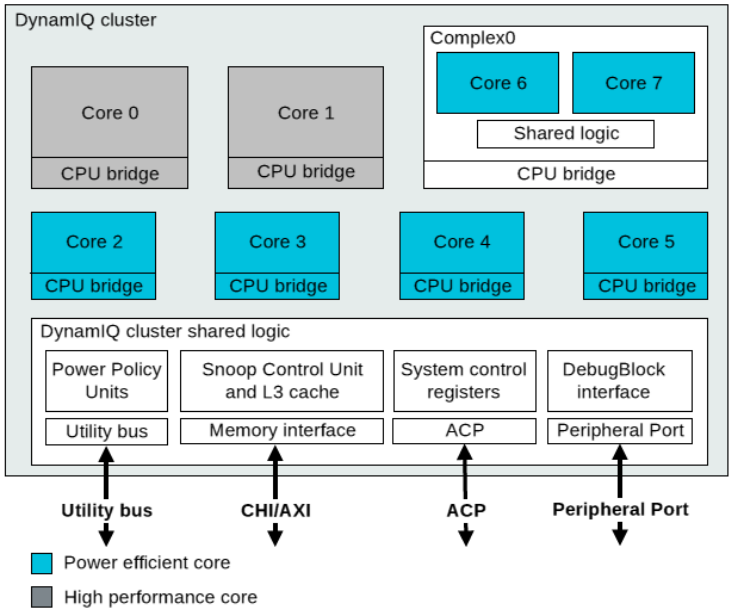
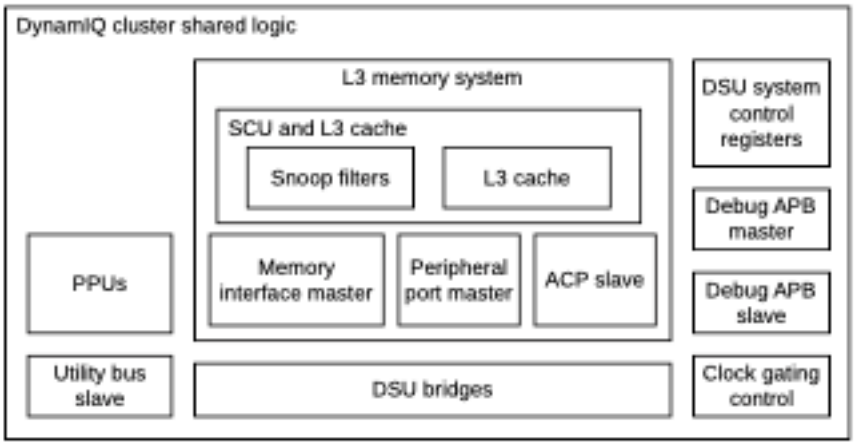


Figure 3-2: DynamIQ™ cluster shared logic components



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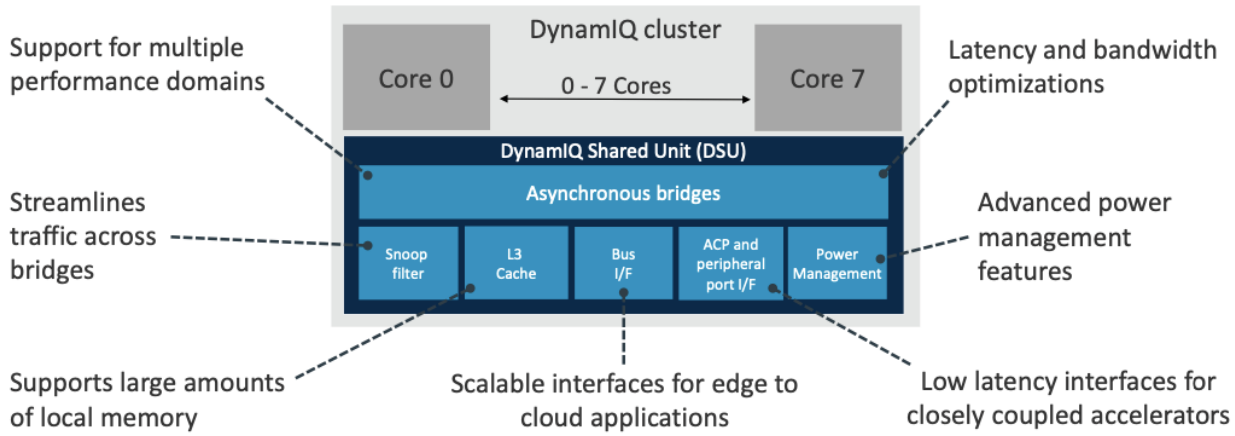
DynamIQ Shared Unit (DSU)



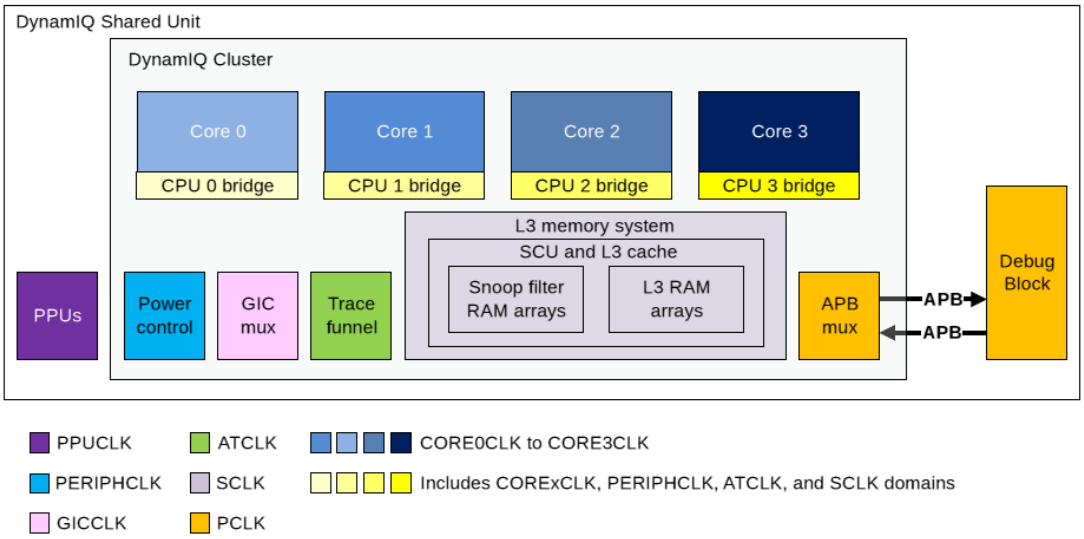
Source: https://old.hotchips.org/wp-content/uploads/hc_archives/hc29/HC29.22-Tuesday-Pub/HC29.22.80-Architectdure-Pub/HC29,22,820-DynamiQ-Greenhaigh-ARM.pdf

46. The Accused '443 Products further include, for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain. For example, there is a clock for separately generating a clock signal at a frequency for any one of the User Cores (e.g., Core 0 and its CPU bridge) of the DynamIQ cluster, and another clock for separately generating another clock signal at another frequency for the DSU.

The *DynamIQ™ Shared Unit-110* (DSU-110) has multiple clock domains. Each core or complex can be implemented in a separate clock domain.

The following figure shows the clock domains for an example cluster with four standalone cores.

Figure 4-1: DSU-110 clock domains



The cluster contains several clock domains for functionality that is likely to be connected to different clocks in the system. Within each core, the CPU bridge contains asynchronous bridges for all crossings between the core and cluster clock domains. Each CPU bridge is split, with one half of each bridge in the core clock domain and the other half in the relevant cluster domain. At the cluster level, there is the *Snoop Control Unit* (SCU) bridge which contains crossings between the cluster clock domains as required.

4.1 Clocks

The *DynamIQ™ Shared Unit-110* (DSU-110) has a separate clock signal for each standalone core or complex. There are also separate clocks for the internal logic, and some of the external interfaces.

The following table describes the clock signals of the DSU-110.

Table 4-1: DSU-110 clock signals

Signal	Description
COREXCLK	The clocks for each of the cores in the cluster that are not part of a complex. x is the core instance number, for example, **CORE0CLK** is the clock for core 0. These signals clock all core logic, including L1 and L2 caches.
COMPLEXxCLK	The clocks for each complex in the cluster. Each clock is connected to all cores in the respective complex. x is the complex instance number, for example, **COMPLEX0CLK** is the clock for complex 0.
SCLK	This clock is used for the *Snoop Control Unit* (SCU), L3 memory system, and all the external interfaces, including AXI, CHI, and *Accelerator Coherency Port* (ACP). It is also used for cores that are configured to run synchronously with the DSU-110.

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47. In the Accused ’443 Products, the frequency of the clock signal of a domain is dynamically changeable independent of the frequencies of the clock signals generated for other domains. For example, the frequency of the clock signal of any one of the User Cores of the DynamIQ cluster is dynamically changeable independent of the frequencies of the clock signals of the DSU.

Clock management

Clock gating is supported through Q-Channel requests from an external clock controller to the DSU-110. The Q-Channels allow individual control of the following clock input signals:

- **ATCLK**
- **COREx**CLK where x is the core instance number
- **COMPLEXx**CLK where x is the complex instance number
- **GICCLK**
- **PCLK**
- **PERIPHCLK**
- **PPUCLK**
- **SCLK**

All clocks can be driven fully asynchronously to each other. The DSU-110 contains all the necessary synchronizing logic for crossing between clock domains. There are no clock dividers and no latches in the design. The entire design is rising-edge triggered.

While there is no functional requirement for any of the clocks to have any relationship to any of the others, the DSU-110 is designed with the following expectations to achieve an acceptable performance:

- The **COREx**CLK or **COMPLEXx**CLK can be dynamically scaled to match the performance requirements of that core.
- **SCLK** is recommended to run between the maximum **COREx**CLK or **COMPLEXx**CLK frequency and approximately half of the maximum **COREx**CLK or **COMPLEXx**CLK frequency.

L3 cache system can be clocked at a rate synchronous to the external system interconnect or at integer multiples

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3.1.1 Integration of the cores in the cluster

When you implement a DSU-110 DynamIQ™ cluster, all interfacing between the cores, complexes, and the *DynamIQ™ Shared Unit-110* (DSU-110) is implemented automatically. All the external signal inputs and outputs pass through the DSU-110. The DSU-110 buffers and resynchronizes many of these signals to allow cores to be clocked at different speeds.

The memory interfacing of each core is internally connected to the DSU-110 L3 memory system. Where necessary, the DSU-110 implements additional buffering to compensate for different clock rates of the core and DSU-110 L3 memory system.

Each core has an external clock interface, which is routed through the DSU-110 to the respective core.

Power management and clock gating

The DebugBlock implements two Q-Channel interfaces, one for requests to gate the PCLK clock, and a second for requests to control the Debug power domain.

4.1 Clocks

The *DynamIQ™ Shared Unit-110* (DSU-110) has a separate clock signal for each standalone core or complex. There are also separate clocks for the internal logic, and some of the external interfaces.

Cluster features

The DSU-110 has the following cluster features:

- Support for cores running independently at different frequencies and voltages known as *Dynamic Voltage Frequency Scaling* (DVFS). For cores in a complex, DVFS is only possible for the whole complex not for individual cores.

Source: https://documentation-service.arm.com/static/611e9446d5c3af0155491bf8?token=

A4.8 Clock, voltage, and power domains

The DynamIQ cluster microarchitecture supports multiple clock, voltage, and power domains.

The number of domains that are implemented depends on the choices made by the SoC implementer. There might be fewer in your SoC.

The following diagram shows the clock, voltage, and power domains supported by the DSU and cores.

- Voltage domains are indicated by dashed outlines.
- Blocks that are in the same power domain have the same color.

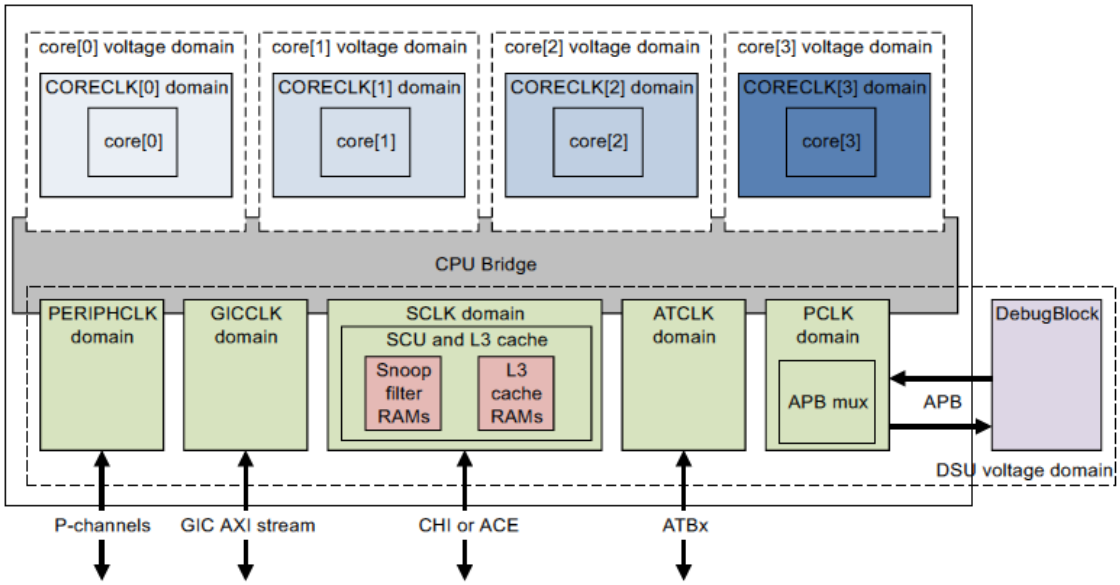


Figure A4-2 DSU Clock, voltage, and power domains

Clock domains

Each core can be implemented in a separate clock domain. The DSU has multiple clock domains.

The CPU Bridge contains all asynchronous bridges for crossing clock domains, and is split with one half of each bridge in the core clock domain and the other half in the relevant cluster domain. Each core can be implemented with or without an asynchronous bridge. If the asynchronous bridge is not implemented, the core is in the SCLK clock domain.

Source: https://documentation-service.arm.com/static/611e9446d5c3af0155491bf8?token=

The following diagram shows a cluster that is composed of two sets of cores in a DynamIQ big.LITTLE configuration.

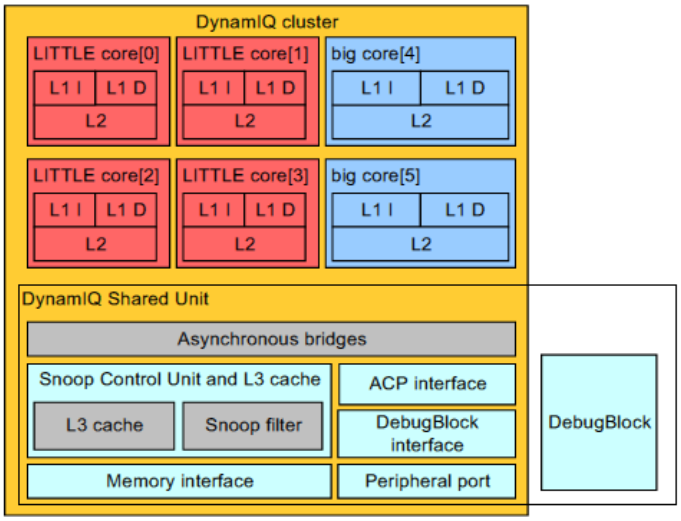


Figure A1-1 DynamIQ cluster

Within the DSU, are the L3 cache, the *Snoop Control Unit* (SCU), internal interfaces to the cores, and external interfaces to the SoC.

- The shared L3 cache simplifies process migration between the cores.

  Note

  Some cores can be configured without L2 caches. To these cores, the shared L3 cache appears as an L2 cache. The term 'L3 cache' is used throughout this document to describe the shared cache.

- The *Snoop Control Unit* (SCU) maintains coherency between caches in the cores and L3. The SCU includes a Snoop Filter to optimize coherency maintenance operations.
- Internal interfaces to the cores are configured during macrocell implementation and are not directly visible.
- External interfaces are connected to the SoC.

Each core can be configured either to be run synchronously with the DSU, sharing the clock, or asynchronously, with an independent clock.

Source: https://documentation-service.arm.com/static/5e7e16e0b2608e4d7f0a3030

A3.1 Clocks

The DSU requires clock signals for each of the cores, internal logic, and external interfaces.

The following table describes the clocks.

Table A3-1 DSU clock signals

Signal	Description
CORECLK[CN:0]	The per-core clocks for all core logic including L1 and L2 caches.
SCLK	The clock for the SCU and L3 memory system, including the ACE or CHI master interface. **SCLK** is also used for any cores that are configured to run synchronously to the DSU.
PCLK	The clock for the DebugBlock and DSU debug APB interfaces. **Note** The DebugBlock and cluster both have **PCLK** inputs. You might choose to connect these to the same clock. Alternatively, you might choose to place an asynchronous bridge between the two clock inputs, in which case they might be different clocks.
ATCLK	The clock for the ATB trace buses output from the DSU. **Note** All ATB buses output from the DSU share the same clock.
GICCLK	The clock for the GIC AXI-stream interface between the DSU and an external GIC.
PERIPHCLK	The clock for peripheral logic inside the DSU such as timers, and clock and power management logic.

All clocks can be driven fully asynchronously to each other. The DSU contains all the necessary synchronizing logic for crossing between clock domains. There are no clock dividers and no latches in the design. The entire design is rising edge triggered.

Source: https://documentation-service.arm.com/static/5e7e16e0b2608e4d7f0a3030

ARM DynamIQ

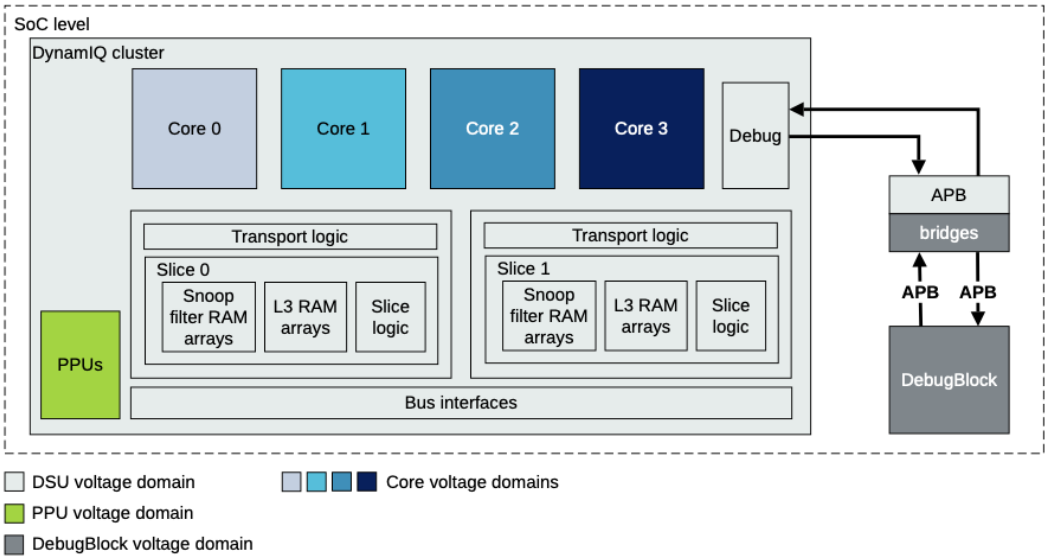
- ARM DynamIQ technology
  - Different microarchitectures can exist within same cluster.
  - Share the same last level of cache (L3), i.e. DSU (DynamIQ shared unit).
  - Different compute capacity and frequency domains for big and LITTLE.

- All the entities can do DVFS: big, LITTLE and DSU.
- Same voltage domain possible for DSU and big or/and LITTLE CPUs.
- DSU controls the cache bandwidth available to CPUs.
- DSU bandwidth configured based on requirements from CPUs.

Source: http://retis.sssup.it/luca/ospm-summit/2018/Downloads/Device_notifications_and_improved_efficiency.pdf

48. The Accused '443 Products further include, for each of the plurality of domains, a voltage input for receiving a voltage. For example, any one of the User Cores of the DynamIQ cluster and the DSU, each have a voltage input for receiving a voltage.

Figure 5-6: DSU-110 voltage domains



Having each core in a separate voltage domain allows *Dynamic Voltage Frequency Scaling* (DVFS) to be applied to each core.

Cluster features

The DSU-110 has the following cluster features:

- Support for Arm®v9.0-A architecture cores
- Support for up to three types of core, and a maximum of eight cores in the cluster
- *Power Policy Units* (PPUs) providing autonomous power management of the L3 cache and the cores
- Support for cores running independently at different frequencies and voltages known as *Dynamic Voltage Frequency Scaling* (DVFS). For cores in a complex, DVFS is only possible for the whole complex not for individual cores.

Source: https://documentation-service.arm.com/static/611e9446d5c3af0155491bf8?token=

49. In the Accused '443 Products, for each of the voltage inputs for each of the plurality of domains, the voltage is dynamically changeable independent of the voltages applied to said others of the plurality of domains. For example, any one of the User Cores of the DynamIQ cluster and the DSU, each have their own independent voltage domains which are dynamically changeable independent of the voltages applied to the other voltage domains.

A4.1 About DSU power management

The DSU supports a range of low-power modes and cache RAM powerdown modes.

The DSU supports the following power modes:

On

On mode is the normal mode of operation where all the core and DSU functionality is available. The DSU individually disables internal clocks, and inputs to unused functional blocks. Only the logic that is in use consumes dynamic power.

Functional retention

Functional retention allows the L3 cache and snoop filter RAMs to be put temporarily in to a retention state while the L3 cache is not being accessed. The contents of the cache RAMs are retained.

Memory retention

Memory retention mode allows the L3 cache and snoop filter RAMs to be held in retention while the rest of the cluster is powered down. Keeping the RAMs in retention reduces the energy cost of writing dirty lines back to memory and reduces the cluster response time on powerup. It is not possible to snoop the cache in this mode, so it is important that no other external coherent agents are active (for example, cores external to the cluster, or other coherent devices). In practice, this mode can only be used in a coherent system when the cluster is the only active agent.

Off

In off mode, power is removed completely, and no state is retained. To avoid losing data, the cores within the cluster, and the cluster itself must first be taken out of coherence.

The DSU supports clock, voltage, and power domains that can be controlled by external logic. The cluster, in conjunction with power management software, gives operating requirement hints to an external power controller. The power controller is responsible for coordinating power management with the rest of the SoC, switching and isolating power and voltage domains, and controlling clock gating cells.

Source: https://documentation-service.arm.com/static/5e7e16e0b2608e4d7f0a3030

A4.8 Clock, voltage, and power domains

The DynamIQ cluster microarchitecture supports multiple clock, voltage, and power domains.

The number of domains that are implemented depends on the choices made by the SoC implementer. There might be fewer in your SoC.

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- Blocks that are in the same power domain have the same color.

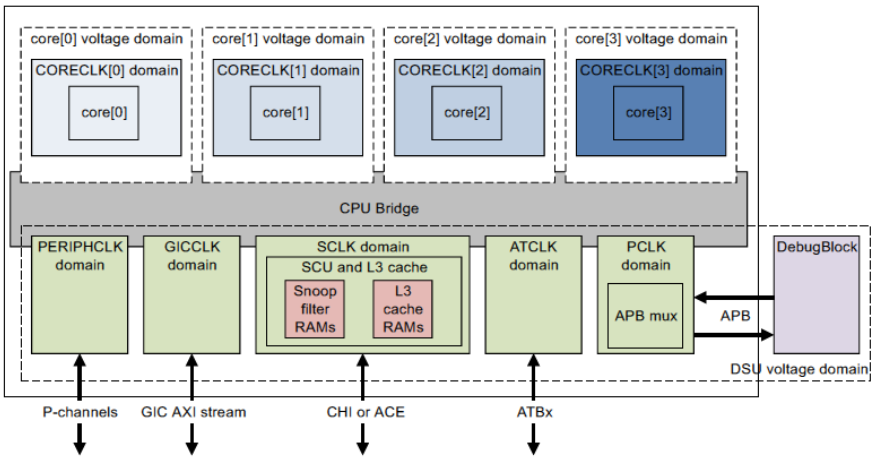

Figure A4-2 DSU Clock, voltage, and power domains

Voltage domains

Each core can be implemented in a separate voltage domain. The DSU has a single separate voltage domain, allowing, for example, the DSU to be in the same voltage domain as the SoC interconnect and other system components.

Source: https://documentation-service.arm.com/static/5e7e16e0b2608e4d7f0a3030

ARM DynamIQ

- ARM DynamIQ technology
  - Different microarchitectures can exist within same cluster.
  - Share the same last level of cache (L3), i.e. DSU (DynamIQ shared unit).
  - Different compute capacity and frequency domains for big and LITTLE.

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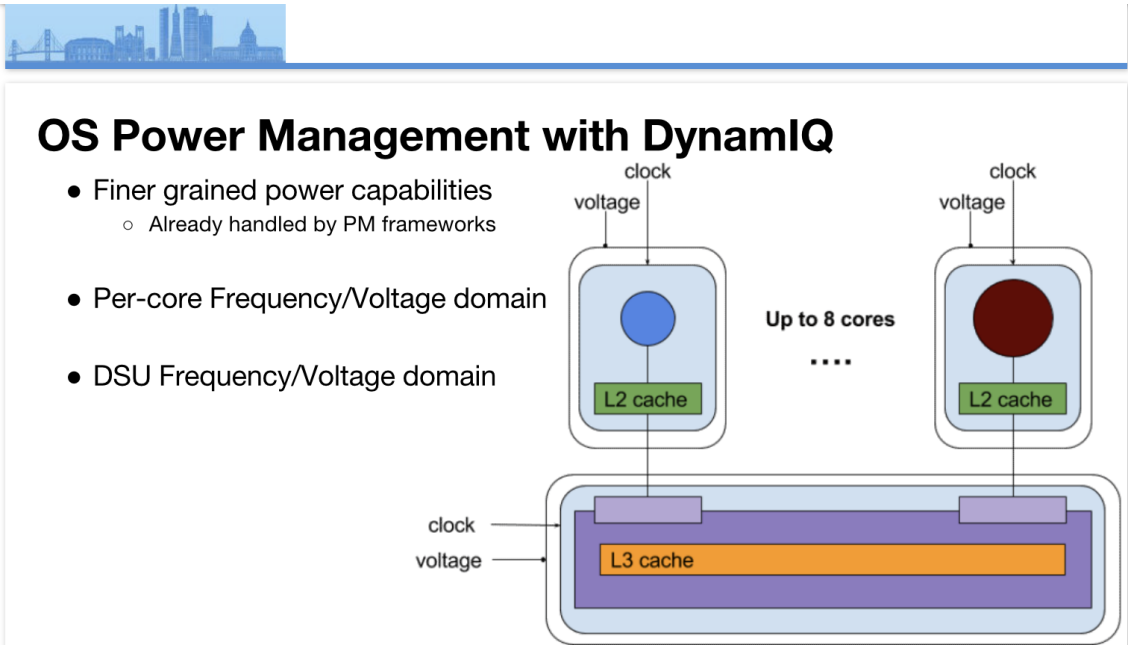
- DSU controls the cache bandwidth available to CPUs.
- DSU bandwidth configured based on requirements from CPUs.

Source: http://retis.sssup.it/luca/ospm-summit/2018/Downloads/Device_notifications_and_improved_efficiency.pdf



Source: https://vdocuments.net/enabling-arm-dynamiq-dynamiq-introduction-dynamiq-and-arm-trusted-firmware.html?page=14

50. Additionally, Defendant has been, and currently is, an active inducer of infringement of the ’443 patent under 35 U.S.C. § 271(b) and a contributory infringer of the ’443 patent under 35 U.S.C. § 271(c).

51. Defendant has actively induced, and continues to actively induce, infringement of the ’443 patent by causing others to use, offer for sale, or sell in the United States, products or services covered by the ’443 patent, including but not limited to the ’443 Accused Products and any other products or services that include ARM-based processors with the functionality described above. Defendant provides these products and services to others, such as customers, resellers, partners, and end-users, who, in turn, use, provision for use, offer for sale, or sell those products and services, which directly infringe the ’443 patent as described above. Defendant’s inducement includes the directions and instructions found at one or more of the following links, the provision of which is on-going as of the filing of this Complaint and much of the content of which is specifically illustrated above:

- https://www.tcl.com/us/en/products/mobile/tcl-30-series/tcl-30-v-5g
- https://www.tcl.com/global/en/mobile/tcl-20-5g/performance
- https://www.tcl.com/ro/ro/mobile/tcl20-5g/performance
- https://www.tcl.com/us/en/products/mobile/tcl-a-series/tcl-signa
- https://www.tcl.com/us/en/press-releases/tcl-expands-10-series-mobile-lineup
- https://www.tcl.com/global/en/mobile/tcl-20l/performance
- https://developer.arm.com/Processors/Cortex-A76
- https://www.arm.com/products/silicon-ip-cpu/cortex-a/cortex-a76
- https://documentation-service.arm.com/static/611e9446d5c3af0155491bf8?token=

52. Defendant has contributed to, and continues to contribute to, the infringement of the ’443 patent by others by knowingly providing one or more components, for example the ARM-Cortex-Axx-based CPU included in the Accused Products, a portion thereof, and/or the software/hardware modules responsible for the accused functionality described herein, that, when

installed, configured, and used result in systems that, as intended by TCL described above, directly infringe one or more claims of the ’443 patent.

53. Defendant knew of the ’443 patent, or should have known of the ’443 patent, but was willfully blind to its existence. Upon information and belief, Defendant had actual knowledge of the ’443 patent at least as early as Defendant received a copy of this Complaint, or alternatively, at least as early as the service upon Defendant of the Complaint in this action.

54. By the time of trial, Defendant will or should have known and intended (since receiving such notice) that its continued actions would infringe and would actively induce and contribute to the infringement of the ’443 patent.

55. Defendant has committed, and continues to commit, contributory infringement by selling products and services that directly infringe the ’443 patent when used by a third party, such as the Accused ’443 Products, and that are a material part of the invention, knowing them to be especially made or adapted for use in infringement of the ’443 patent and not staple articles or commodities of commerce suitable for substantial non-infringing use.

56. As a result of Defendant’s acts of infringement, IV has suffered and will continue to suffer damages in an amount to be determined at trial.

COUNT II

(Defendant’s Infringement of U.S. Patent No. 7,623,439)

57. The preceding paragraphs are reincorporated by reference as if fully set forth herein.

58. The ’439 patent claims and teaches, *inter alia*, an improved signal transmitting system capable of manipulating OFDM data packets and data streams using improved cyclic diversity schemes, thereby improving packet reception performance when compared to conventional packet diversity mechanisms by reducing packet error rates, among other benefits.

59. The inventions improved upon then-existing cyclic diversity schemes in wireless communication by enabling a cyclic diversity scheme by which a portion of an OFDM packet's symbol data is cyclically advanced into the guard interval with respect to the original OFDM signal and then each signal is sent to a receiver device at substantially the same time from two respective antennas. This allowed for improved acquisition and correlation at the receiver while at the same time keeping intersymbol interference and unintentional beamforming to a minimum.

60. Unlike in prior art systems and methods, the cyclic diversity taught by the '439 patent uses cyclic advancement as opposed to delay. Doing so substantially reduces the probability of unintentional beamforming.

61. More specifically, one exemplary embodiment comprises an improved cyclic diversity system in which a logic circuit is configured to cyclically advance samples of a symbol data portion of an OFDM packet to be transmitted on a first antenna, relative to the samples of a symbol data portion of another OFDM packet to be transmitted on another antenna. The duration of the cyclic advance is less than the duration of a guard interval portion of the OFDM packet. By using a cyclic advance as described above, the symbol data portions of the two different transmitted signals are better decorrelated, thus reducing the probability of unintentional beamforming. The performance of wireless networks is thereby improved by the technologies disclosed and claimed in the '439 patent.

62. The system and methods covered by the asserted claims, therefore, differs markedly from prior art systems in use at the time of this invention, which lacked the claimed combination of cyclically advancing a first OFDM packet by shifting the samples in a first direction an amount less than a sample duration of the guard interval portion to generate a shifted version of the first OFDM packet in which at least a non-zero number of samples from the symbol data portion of the

first OFDM packet are shifted into the guard interval portion of the shifted version, and a same non-zero number of samples from the guard interval portion of the first OFDM packet are shifted out of the guard interval portion of the shifted version. And, further where both versions are substantially simultaneously transmitted.

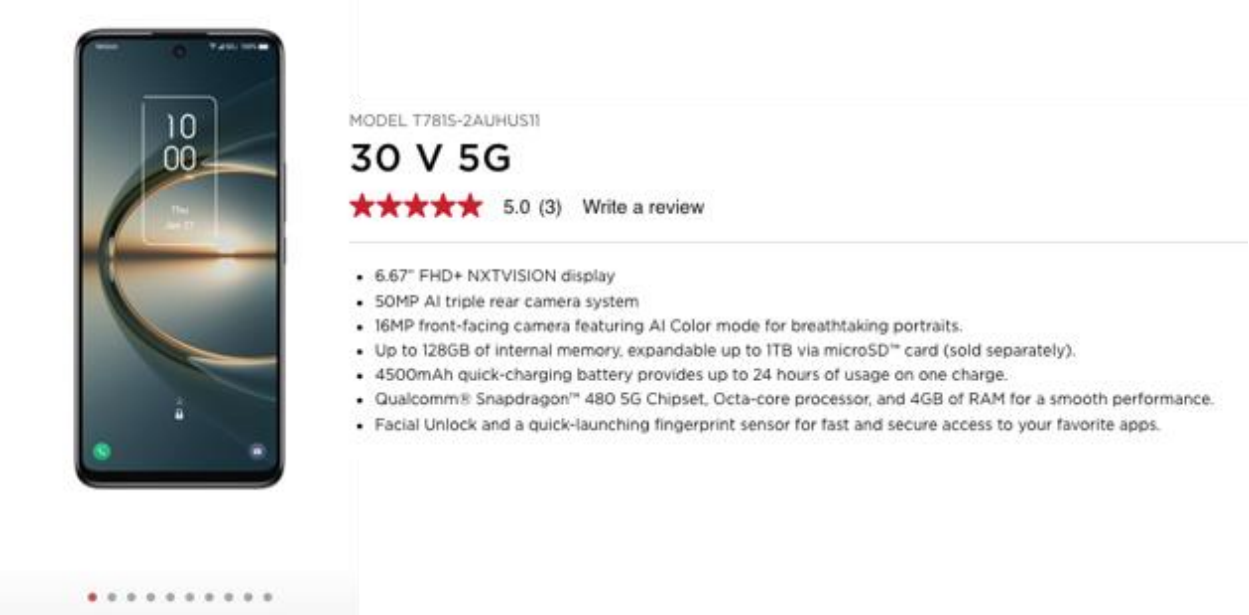
63. Defendant has directly infringed and continues to directly infringe at least claim 1 of the '439 patent by making, using, selling, offering for sale, or importing products and/or services covered by the '439 patent. Defendant's products and/or services that infringe the '439 patent include all wireless communication products that support IEEE 802.11n, 802.11ac and 802.11ax, including the transmission of multiple spatial streams, which requires a cyclic diversity shift when transmitting OFDM packets, that are made, used, sold, or offered for sale by or on behalf of Defendant and/or its subsidiaries or parent companies (cumulatively, "the '439 Accused Products"), including but not limited to, the TCL 30 V 5G smartphone.

64. Claim 1 of the '439 patent is reproduced below:

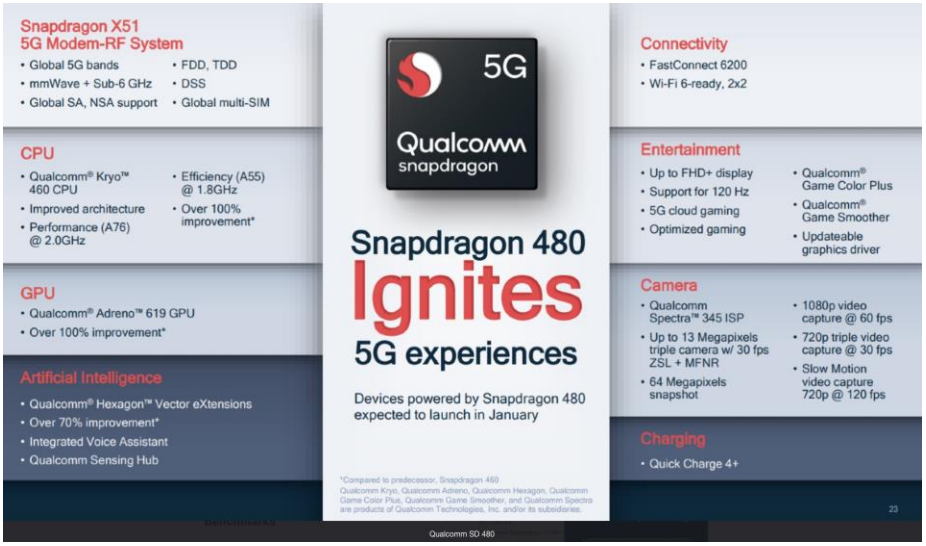
> *1. A method for transmitting orthogonal frequency division multiplexing (OFDM) signals comprising:*
>
> *generating a first OFDM packet for transmission including a guard interval portion and a symbol data portion each comprised of a plurality of samples;*
>
> *cyclically advancing the first OFDM packet by shifting the samples in a first direction an amount less than a sample duration of the guard interval portion to generate a shifted version of the first OFDM packet for transmission in which at least a non-zero number of the samples from the symbol data portion of the first OFDM packet are shifted into the guard interval portion of the shifted version and a same non-zero number of samples from the guard interval portion of the first OFDM packet are shifted out of the guard interval portion of the shifted version; and*
>
> *substantially simultaneously transmitting the first OFDM packet and the shifted version of the OFDM packet.*

65. The '439 Accused Products are configured to perform a method for transmitting OFDM signals. As one example, the TCL 30 V 5G supports the IEEE 802.11n standard, including

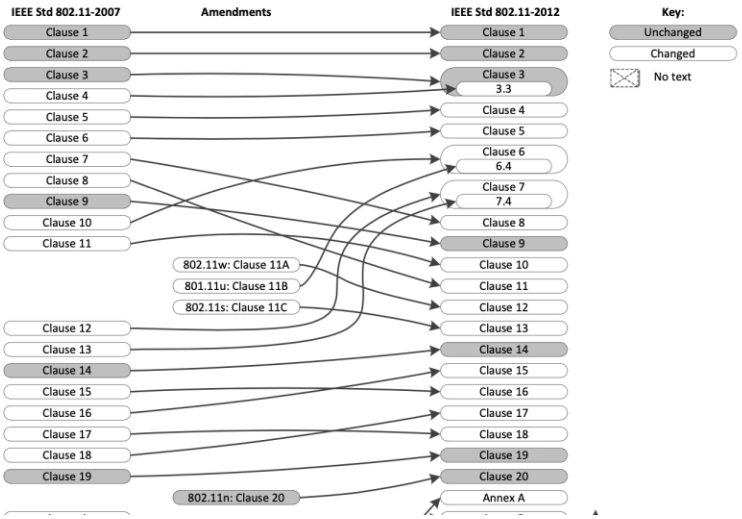
the transmission of multiple spatial streams, which requires a forward shift diversity feature for transmitting OFDM signals:



Source: https://www.tcl.com/us/en/products/mobile/tcl-30-series/tcl-30-v-5g



Source: https://www.notebookcheck.net/Qualcomm-Snapdragon-480-5G-Processor-Benchmarks-and-Specs.537294.0.html#device_img



Source: IEEE 802.11-2012.

20. High Throughput (HT) PHY specification

20.1 Introduction

20.1.1 Introduction to the HT PHY

Clause 20 specifies the PHY entity for a high throughput (HT) orthogonal frequency division multiplexing (OFDM) system.

In addition to the requirements found in Clause 20, an HT STA shall be capable of transmitting and receiving frames that are compliant with the mandatory PHY specifications defined as follows:

— In Clause 18 when the HT STA is operating in a 20 MHz channel width in the 5 GHz band

— In Clause 17 and Clause 19 when the HT STA is operating in a 20 MHz channel width in the 2.4 GHz band

The HT PHY is based on the OFDM PHY defined in Clause 18, with extensibility up to four spatial streams, operating in 20 MHz bandwidth. Additionally, transmission using one to four spatial streams is defined for operation in 40 MHz bandwidth. These features are capable of supporting data rates up to 600 Mb/s (four spatial streams, 40 MHz bandwidth).

The HT PHY data subcarriers are modulated using binary phase shift keying (BPSK), quadrature phase shift keying (QPSK), 16-quadrature amplitude modulation (16-QAM), or 64-QAM. Forward error correction (FEC) coding (convolutional coding) is used with a coding rate of 1/2, 2/3, 3/4, or 5/6. LDPC codes are added as an optional feature.

Source: IEEE Std 802.11-2012 pp. 1669.

20.1.2 Scope

The services provided to the MAC by the HT PHY consist of two protocol functions, defined as follows:

a) A PHY convergence function, which adapts the capabilities of the physical medium dependent (PMD) system to the PHY service. This function is supported by the physical layer convergence procedure (PLCP), which defines a method of mapping the PSDUs into a framing format (PPDU) suitable for sending and receiving PSDUs between two or more STAs using the associated PMD system.

Source: IEEE Std 802.11-2012 pp. 1669.

20.1.4 PPDU formats

The structure of the PPDU transmitted by an HT STA is determined by the TXVECTOR FORMAT, CH_BANDWIDTH, CH_OFFSET, and MCS parameters as defined in Table 20-1. The effect of the CH_BANDWIDTH, CH_OFFSET, and MCS parameters on PPDU format is described in 20.2.3.

The FORMAT parameter determines the overall structure of the PPDU as follows:

— *Non-HT format* **(NON_HT)**: Packets of this format are structured according to the Clause 18 (OFDM) or Clause 19 (ERP) specification. Support for non-HT format is mandatory.

— *HT-mixed format* **(HT_MF)**: Packets of this format contain a preamble compatible with Clause 18 and Clause 19 receivers. The non-HT-STF (L-STF), the non-HT-LTF (L-LTF), and the non-HT SIGNAL field (L-SIG) are defined so they can be decoded by non-HT Clause 18 and Clause 19 STAs. The rest of the packet cannot be decoded by Clause 18 or Clause 19 STAs. Support for HT-mixed format is mandatory.

— *HT-greenfield format* **(HT_GF)**: HT packets of this format do not contain a non-HT compatible part. Support for HT-greenfield format is optional. An HT STA that does not support the reception of an HT-greenfield format packet shall be able to detect that an HT-greenfield format packet is an HT transmission (as opposed to a non-HT transmission). In this case, the receiver shall decode the HT-SIG and determine whether the HT-SIG cyclic redundancy check (CRC) passes.

Source: IEEE Std. 802.11-2012, pp. 1669-70.

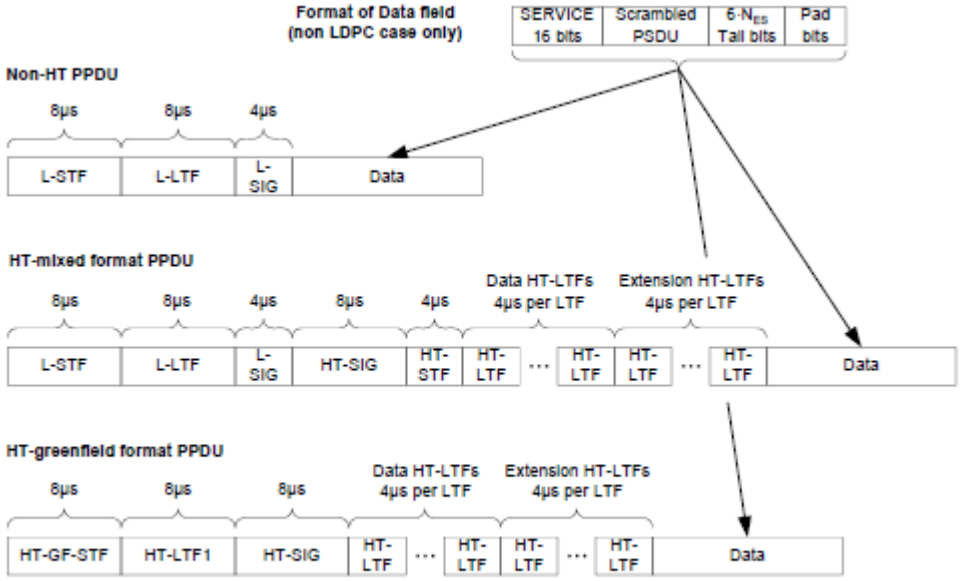


Figure 20-1—PPDU format

Source: IEEE Std. 802.11-2012, pp. 1682.

The HT portion of the HT-mixed format preamble enables estimation of the MIMO channel to support demodulation of the HT data by HT STAs. The HT portion of the HT-mixed format preamble also includes the HT-SIG field, which supports HT operation. The SERVICE field is prepended to the PSDU.

Source: IEEE Std. 802.11-2012, pp. 1682.

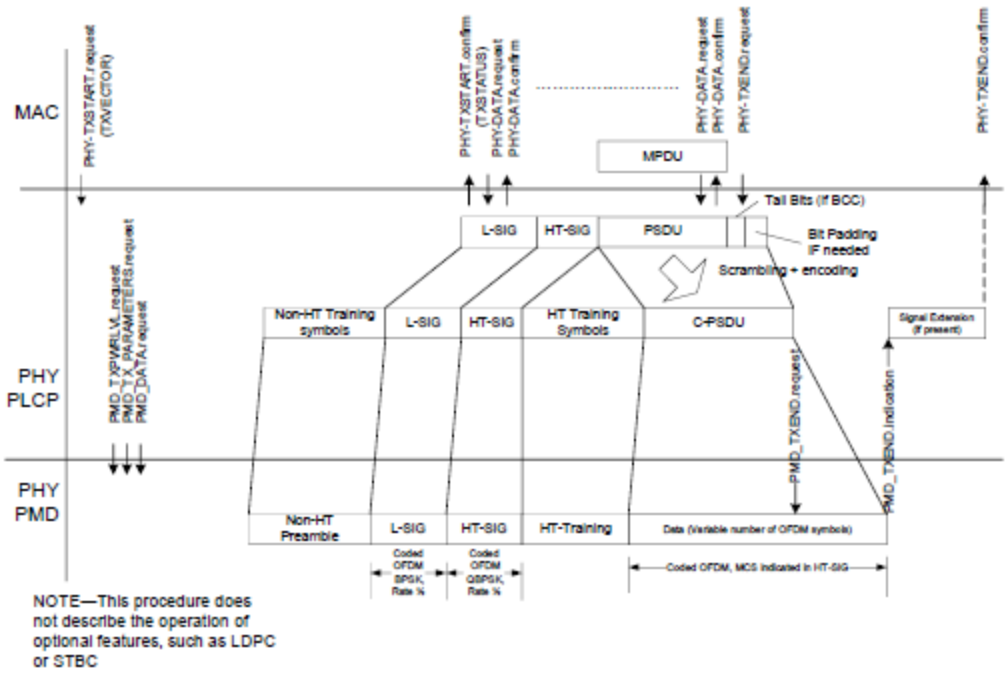


Figure 20-22—PLCP transmit procedure (HT-mixed format PPDU)

Source: IEEE Std. 802.11-2012, p. 1748.

66. The method practiced by the '439 Accused Products includes generating a first OFDM packet for transmission including a guard interval portion and a symbol data portion each comprised of a plurality of samples. For instance, the 802.11 transmitter in the Accused Products creates an OFDM packet, known as an HT-SIG OFDM packet, which includes a symbol data portion comprised of a plurality of samples and a guard interval portion comprised of a plurality of samples as seen below:

20. High Throughput (HT) PHY specification

20.1 Introduction

20.1.1 Introduction to the HT PHY

Clause 20 specifies the PHY entity for a high throughput (HT) orthogonal frequency division multiplexing (OFDM) system.

In addition to the requirements found in Clause 20, an HT STA shall be capable of transmitting and receiving frames that are compliant with the mandatory PHY specifications defined as follows:

- In Clause 18 when the HT STA is operating in a 20 MHz channel width in the 5 GHz band
- In Clause 17 and Clause 19 when the HT STA is operating in a 20 MHz channel width in the 2.4 GHz band

The HT PHY is based on the OFDM PHY defined in Clause 18, with extensibility up to four spatial streams, operating in 20 MHz bandwidth. Additionally, transmission using one to four spatial streams is defined for operation in 40 MHz bandwidth. These features are capable of supporting data rates up to 600 Mb/s (four spatial streams, 40 MHz bandwidth).

The HT PHY data subcarriers are modulated using binary phase shift keying (BPSK), quadrature phase shift keying (QPSK), 16-quadrature amplitude modulation (16-QAM), or 64-QAM. Forward error correction (FEC) coding (convolutional coding) is used with a coding rate of 1/2, 2/3, 3/4, or 5/6. LDPC codes are added as an optional feature.

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20.1.2 Scope

The services provided to the MAC by the HT PHY consist of two protocol functions, defined as follows:

a) A PHY convergence function, which adapts the capabilities of the physical medium dependent (PMD) system to the PHY service. This function is supported by the physical layer convergence procedure (PLCP), which defines a method of mapping the PSDUs into a framing format (PPDU) suitable for sending and receiving PSDUs between two or more STAs using the associated PMD system.

Source: IEEE Std 802.11-2012 pp. 1669.

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The structure of the PPDU transmitted by an HT STA is determined by the TXVECTOR FORMAT, CH_BANDWIDTH, CH_OFFSET, and MCS parameters as defined in Table 20-1. The effect of the CH_BANDWIDTH, CH_OFFSET, and MCS parameters on PPDU format is described in 20.2.3.

The FORMAT parameter determines the overall structure of the PPDU as follows:

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Source: IEEE Std. 802.11-2012, pp. 1669-70.

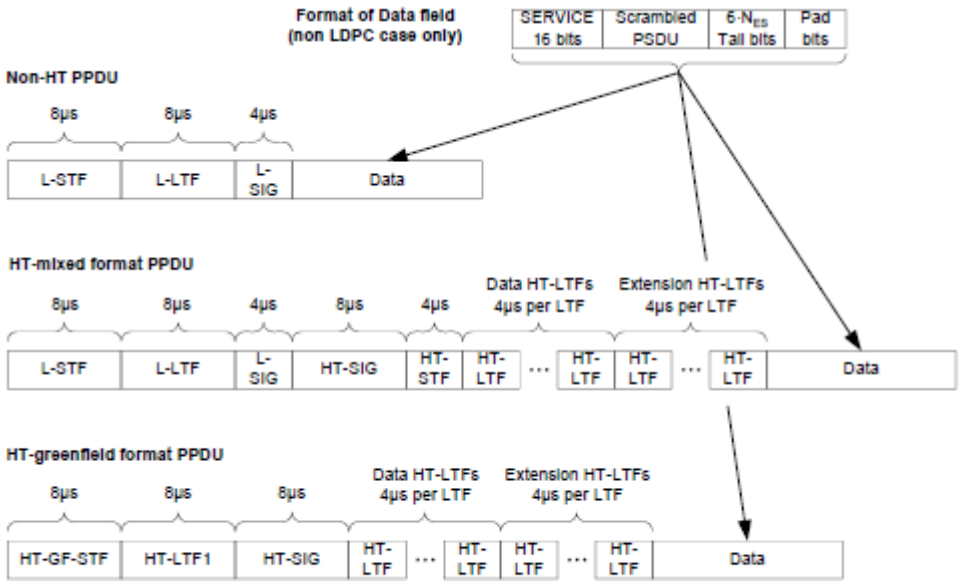


Figure 20-1—PPDU format

Source: IEEE Std. 802.11-2012, pp. 1682.

The HT portion of the HT-mixed format preamble enables estimation of the MIMO channel to support demodulation of the HT data by HT STAs. The HT portion of the HT-mixed format preamble also includes the HT-SIG field, which supports HT operation. The SERVICE field is prepended to the PSDU.

Source: IEEE Std. 802.11-2012, pp. 1682.

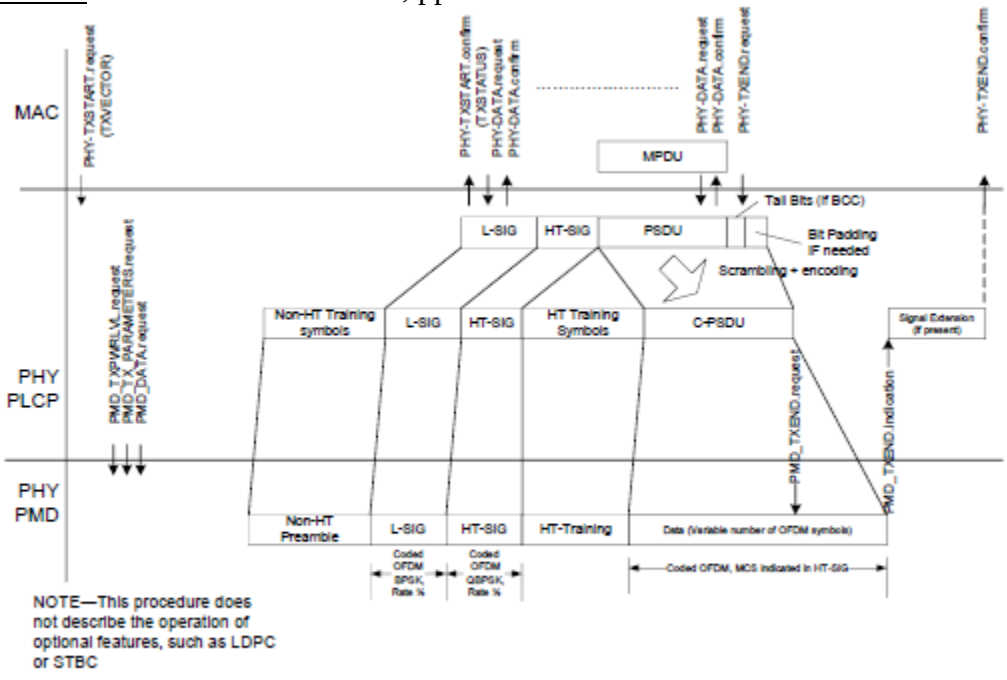


Figure 20-22—PLCP transmit procedure (HT-mixed format PPDU)

Source: IEEE Std. 802.11-2012, p. 1748.

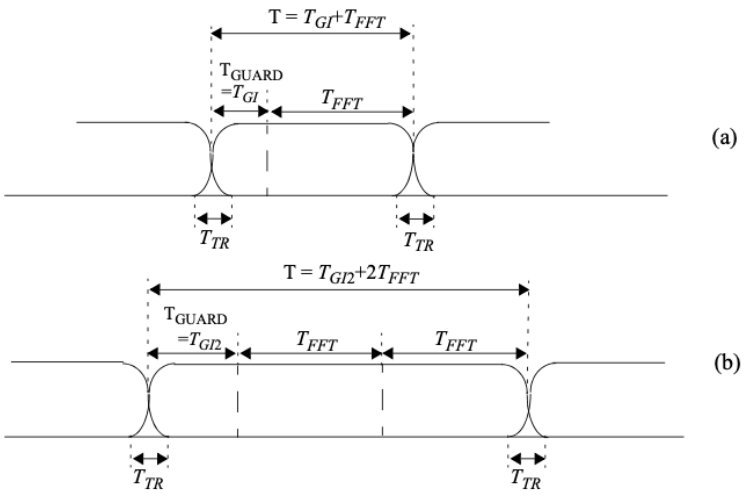


Figure 18-2—Illustration of OFDM frame with cyclic extension and windowing for (a) single reception or (b) two receptions of the FFT period

Source: IEEE Std. 802.11-2012, p. 1592.

T_{FFT}: Inverse Fast Fourier Transform (IFFT) / Fast Fourier Transform (FFT) period	3.2 µs ($1/\Delta_F$)
T_{SIGNAL}: Duration of the SIGNAL BPSK-OFDM symbol	4.0 µs ($T_{GI} + T_{FFT}$)
T_{GI}: GI duration	0.8 µs ($T_{FFT}/4$)

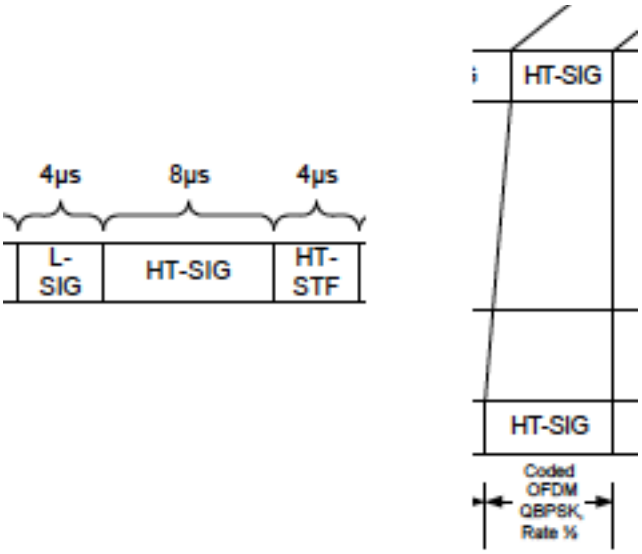
Source: IEEE Std. 802.11-2012, p. 1590-91.

20.3.9.4.3 HT-SIG definition

The HT-SIG is used to carry information required to interpret the HT packet formats. The fields of the HT-SIG are described in Table 20-11.

Table 20-11—HT-SIG fields

Field	Number of bits	Explanation and coding
Modulation and Coding Scheme	7	Index into the MCS table. See NOTE 1.
CBW 20/40	1	Set to 0 for 20 MHz or 40 MHz upper/lower. Set to 1 for 40 MHz.
HT Length	16	The number of octets of data in the PSDU in the range of 0 to 65 535.



Source: IEEE Std. 802.11-2012, p. 1682, 1748, 1699.

The HT-SIG is composed of two parts, HT-SIG$_1$ and HT-SIG$_2$, each containing 24 bits, as shown in Figure 20-6. All the fields in the HT-SIG are transmitted LSB first, and HT-SIG$_1$ is transmitted before HT-SIG$_2$.

The HT-SIG parts shall be encoded at R = 1/2, interleaved, and mapped to a BPSK constellation, and they have pilots inserted following the steps described in 18.3.5.6, 18.3.5.7, 18.3.5.8, and 18.3.5.9, respectively. The BPSK constellation is rotated by 90° relative to the L-SIG in order to accommodate detection of the start of the HT-SIG. The stream of 96 complex numbers generated by these steps is divided into two groups of 48 complex numbers: $d_{k,n}$, $0 \le k \le 47$, $n = 0, 1$. The time domain waveform for the HT-SIG in an HT-mixed format packet in a 20 MHz transmission shall be as shown in Equation (20-16).

$$r^{i_{TX}}_{HT-SIG}(t) = \frac{1}{\sqrt{N_{TX} \cdot N^{Tone}_{HT-SIG}}} \sum_{n=0}^{1} w_{T_{SYM}}(t - nT_{SYM}) \cdot \sum_{k=-26}^{26} (jD_{k,n} + p_{n+1}P_k)\exp(j2\pi k\Delta_F(t - nT_{SYM} - T_{GI} - T^{i_{TX}}_{CS})) \quad (20\text{-}16)$$

Source: IEEE Std. 802.11-2012, p. 1700.

18.3.2.6 Discrete time implementation considerations

The following descriptions of the discrete time implementation are informational.

In a typical implementation, the windowing function is represented in discrete time. As an example, when a windowing function with parameters T = 4.0 µs and a T_{TR} = 100 ns is applied, and the signal is sampled at 20 Msample/s, it becomes

$$w_T[n] = w_T(nT_S) = \begin{Bmatrix} 1 & 1 \le n \le 79 \\ 0.5 & 0, 80 \\ 0 & otherwise \end{Bmatrix} \quad (18\text{-}5)$$

Source: IEEE Std. 802.11-2012, p. 1593.

Figure 20-2 and Figure 20-3 show example transmitter block diagrams. In particular, Figure 20-2 shows the transmitter blocks used to generate the HT-SIG of the HT-mixed format PPDU. These transmitter blocks are

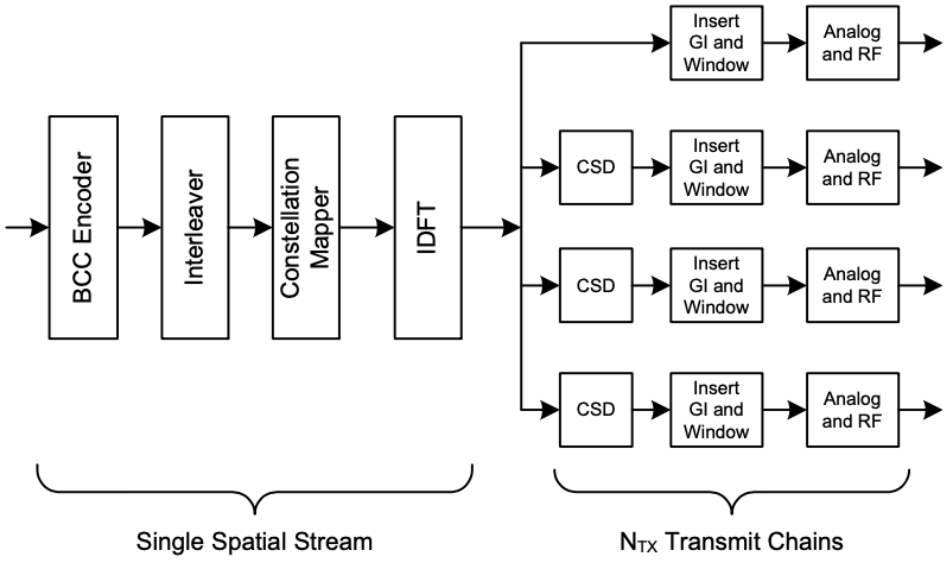


Figure 20-2—Transmitter block diagram 1

Source: IEEE Std. 802.11-2012, p. 1684-85.

20.3.3 Transmitter block diagram

HT-mixed format and HT-greenfield format transmissions can be generated using a transmitter consisting of the following blocks:

a) *Scrambler* scrambles the data to reduce the probability of long sequences of 0s or 1s; see 20.3.11.3.

b) *Encoder parser*, if BCC encoding is to be used, demultiplexes the scrambled bits among N_{ES} (number of BCC encoders for the Data field) BCC encoders, in a round robin manner.

c) *FEC encoders* encode the data to enable error correction. An FEC encoder may include a binary convolutional encoder followed by a puncturing device, or it may include an LDPC encoder.

d) *Stream parser* divides the outputs of the encoders into blocks that are sent to different interleaver and mapping devices. The sequence of the bits sent to an interleaver is called a *spatial stream*.

e) *Interleaver* interleaves the bits of each spatial stream (changes order of bits) to prevent long sequences of adjacent noisy bits from entering the BCC decoder. Interleaving is applied only when BCC encoding is used.

f) *Constellation mapper* maps the sequence of bits in each spatial stream to constellation points (complex numbers).

g) *STBC* encoder spreads constellation points from N_{SS} spatial streams into N_{STS} space-time streams using a space-time block code. STBC is used only when $N_{SS} < N_{STS}$; see 20.3.11.9.2.

h) *Spatial mapper* maps space-time streams to transmit chains. This may include one of the following:
   1) *Direct mapping*: Constellation points from each space-time stream are mapped directly onto the transmit chains (one-to-one mapping).
   2) *Spatial expansion*: Vectors of constellation points from all the space-time streams are expanded via matrix multiplication to produce the input to all the transmit chains.
   3) *Beamforming*: Similar to spatial expansion, each vector of constellation points from all the space-time streams is multiplied by a matrix of steering vectors to produce the input to the transmit chains.

i) *Inverse discrete Fourier transform (IDFT)* converts a block of constellation points to a time domain block.

Source: IEEE Std. 802.11-2012, p. 1683-84.

67. The method practiced by the '439 Accused Products includes cyclically advancing the first OFDM packet by shifting the samples in a first direction an amount less than a sample duration of the guard interval portion to generate a shifted version of the first OFDM packet for transmission. For example, the Accused Products cyclically shift the symbol data portion of the HT_SIG by -200 ns up to -50 ns, which is less than its guard interval's total length of 0.8 us, to generate a shifted version for transmission as seen below:

20.3.3 Transmitter block diagram

HT-mixed format and HT-greenfield format transmissions can be generated using a transmitter consisting of the following blocks:

a) *Scrambler* scrambles the data to reduce the probability of long sequences of 0s or 1s; see 20.3.11.3.
b) *Encoder parser*, if BCC encoding is to be used, demultiplexes the scrambled bits among N_{ES} (number of BCC encoders for the Data field) BCC encoders, in a round robin manner.
c) *FEC encoders* encode the data to enable error correction. An FEC encoder may include a binary convolutional encoder followed by a puncturing device, or it may include an LDPC encoder.
d) *Stream parser* divides the outputs of the encoders into blocks that are sent to different interleaver and mapping devices. The sequence of the bits sent to an interleaver is called a *spatial stream*.
e) *Interleaver* interleaves the bits of each spatial stream (changes order of bits) to prevent long sequences of adjacent noisy bits from entering the BCC decoder. Interleaving is applied only when BCC encoding is used.
f) *Constellation mapper* maps the sequence of bits in each spatial stream to constellation points (complex numbers).
g) *STBC* encoder spreads constellation points from N_{SS} spatial streams into N_{STS} space-time streams using a space-time block code. STBC is used only when $N_{SS} < N_{STS}$; see 20.3.11.9.2.

h) *Spatial mapper* maps space-time streams to transmit chains. This may include one of the following:
   1) *Direct mapping*: Constellation points from each space-time stream are mapped directly onto the transmit chains (one-to-one mapping).
   2) *Spatial expansion*: Vectors of constellation points from all the space-time streams are expanded via matrix multiplication to produce the input to all the transmit chains.
   3) *Beamforming*: Similar to spatial expansion, each vector of constellation points from all the space-time streams is multiplied by a matrix of steering vectors to produce the input to the transmit chains.

i) *Inverse discrete Fourier transform (IDFT)* converts a block of constellation points to a time domain block.

Source: IEEE Std. 802.11-2012, p. 1683-84.

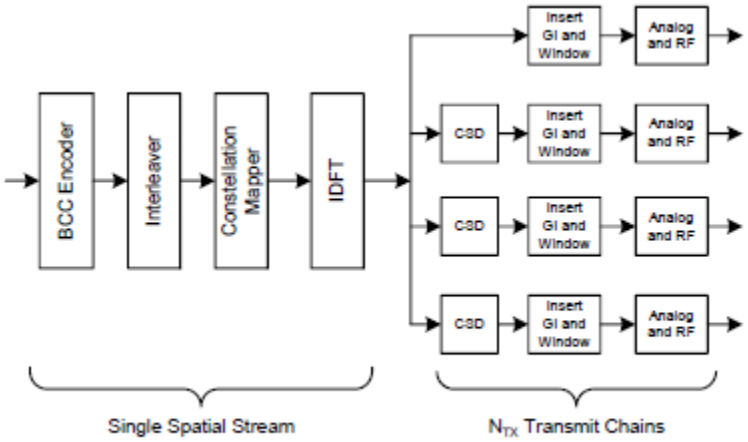


Figure 20-2—Transmitter block diagram 1

Source: IEEE Std. 802.11-2012, p. 1685.

20.3.9.3.2 Cyclic shift definition

The cyclic shift values defined in this subclause apply to the non-HT fields in the HT-mixed format preamble and the HT-SIG in the HT-mixed format preamble.

Cyclic shifts are used to prevent unintentional beamforming when the same signal or scalar multiples of one signal are transmitted through different spatial streams or transmit chains. A cyclic shift of duration T_{CS} on a signal $s(t)$ on interval $0 \le t \le T$ is defined as follows, where T is defined as T_{DFT} as referenced in Table 20-6.

With $T_{CS} \le 0$, replace $s(t)$ with $s(t - T_{CS})$ when $0 \le t < T + T_{CS}$ and with $s(t - T_{CS} - T)$ when $T + T_{CS} \le t \le T$. The cyclic-shifted signal is defined as shown in Equation (20-7).

$$s_{CS}(t;T_{CS})\big|_{T_{CS}<0} = \begin{cases} s(t - T_{CS}) & 0 \le t < T + T_{CS} \\ s(t - T_{CS} - T) & T + T_{CS} \le t \le T \end{cases} \quad (20\text{-}7)$$

The cyclic shift is applied to each OFDM symbol in the packet separately. Table 20-9 specifies the values for the cyclic shifts that are applied in the L-STF (in an HT-mixed format packet), the L-LTF, and L-SIG. It also applies to the HT-SIG in an HT-mixed format packet.

Source: IEEE Std. 802.11-2012, p. 1694-95.

Table 20-9—Cyclic shift for non-HT portion of packet

T_{CS}^{iTX} values for non-HT portion of packet				
Number of transmit chains	Cyclic shift for transmit chain 1 (ns)	Cyclic shift for transmit chain 2 (ns)	Cyclic shift for transmit chain 3 (ns)	Cyclic shift for transmit chain 4 (ns)
1	0	—	—	—
2	0	–200	—	—
3	0	–100	–200	—
4	0	–50	–100	–150

Source: IEEE Std. 802.11-2012, p. 1695.

Table 20-5—Timing-related constants *(continued)*

T_{DFT}: IDFT/DFT period	3.2 μs
T_{GI}: Guard interval duration	0.8 μs= T_{DFT}/4

Source: IEEE Std. 802.11n-2009, p. 266.

20.3.4 Overview of the PPDU encoding process

The encoding process is composed of the steps described below. The following overview is intended to facilitate an understanding of the details of the convergence procedure:

b) Construct the PLCP preamble SIGNAL fields from the appropriate fields of the TXVECTOR by adding tail bits, applying convolutional coding, formatting into one or more OFDM symbols, applying cyclic shifts, applying spatial processing, calculating an inverse Fourier transform for each OFDM symbol and transmit chain, and prepending a cyclic prefix or GI to each OFDM symbol in each transmit chain. The number and placement of the PLCP preamble SIGNAL fields depend on the frame format being used. Refer to 20.3.9.3.5, 20.3.9.4.3, and 20.3.9.5.4.

r) For each group of N_{ST} subcarriers and each of the N_{TX} transmit chains, convert the subcarriers to time domain using IDFT. Prepend to the Fourier-transformed waveform a circular extension of itself, thus forming a GI, and truncate the resulting periodic waveform to a single OFDM symbol length by applying time domain windowing. Determine the length of the GI according to the GI_TYPE parameter of the TXVECTOR. Refer to 20.3.11.11 and 20.3.11.12 for details. When beamforming is not used, it is sometimes possible to implement the cyclic shifts in the time domain.

Source: IEEE Std. 802.11-2012, p. 1684, 1688.

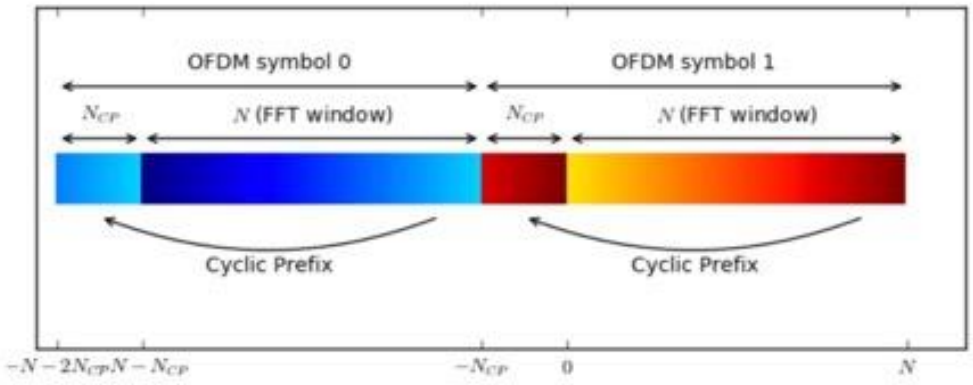
The Cyclic Prefix for OFDM

In a previous post, we have elaborated about the building blocks of OFDM.

There, we have stated two benefits of using a cyclic prefix between subsequent OFDM symbols:

- The CP isolates different OFDM blocks from each other when the wireless channel contains multiple paths, i.e. is frequency-selective.
- The CP turns the linear convolution with the channel into a circular convolution. Only with a circular convolution, we can use the single-tap equalization OFDM is so famous for.

As we see, the CP of an OFDM symbol is obtained by prepending a copy of the last N_{CP} samples from the end of the OFDM signal to its beginning. This way we obtain a circular signal structure, i.e. the first N_{CP} and last N_{CP} samples are equal in each OFDM symbol.



In the above figure, we see two subsequent OFDM symbols, each having a dedicated CP. The colors encode the signal value. The cyclic prefix at the beginning of each OFDM symbol shows a copy of the color of end of the OFDM symbol. When the signal is demodulated, the N-point FFT is taken at the position after the CP, which is indicated with *FFT window*.

Source: *https://dspillustrations.com/pages/posts/misc/the-cyclic-prefix-cp-in-ofdm.html*

The HT-SIG is composed of two parts, HT-SIG$_1$ and HT-SIG$_2$, each containing 24 bits, as shown in Figure 20-6. All the fields in the HT-SIG are transmitted LSB first, and HT-SIG$_1$ is transmitted before HT-SIG$_2$.

The HT-SIG parts shall be encoded at R = 1/2, interleaved, and mapped to a BPSK constellation, and they have pilots inserted following the steps described in 18.3.5.6, 18.3.5.7, 18.3.5.8, and 18.3.5.9, respectively. The BPSK constellation is rotated by 90° relative to the L-SIG in order to accommodate detection of the start of the HT-SIG. The stream of 96 complex numbers generated by these steps is divided into two groups of 48 complex numbers: $d_{k,n}$, $0 \le k \le 47$, $n = 0, 1$. The time domain waveform for the HT-SIG in an HT-mixed format packet in a 20 MHz transmission shall be as shown in Equation (20-16).

$$r_{HT-SIG}^{i_{TX}}(t) = \frac{1}{\sqrt{N_{TX} \cdot N_{HT-SIG}^{Tone}}} \sum_{n=0}^{1} w_{T_{SYM}}(t - nT_{SYM}) \cdot \sum_{k=-26}^{26} (jD_{k,n} + p_{n+1}P_k)\exp(j2\pi k\Delta_F(t - nT_{SYM} - T_{GI} - T_{CS}^{i_{TX}})) \quad (20\text{-}16)$$

where

$$D_{k,n} = \begin{cases} 0, k = 0, \pm 7, \pm 21 \\ d_{M'(k),n}, \text{otherwise} \end{cases}$$

$M'(k)$ is defined in 20.3.9.3

P_k and p_n are defined in 18.3.5.10

N_{HT-SIG}^{Tone} has the value given in Table 20-8

$T_{CS}^{i_{TX}}$ represents the cyclic shift for transmit chain i_{TX} and is defined by Table 20-9 for HT-mixed format PPDUs.

Source: IEEE Std. 802.11-2012, pp. 1700-1701.

T_{GI2}: Double guard interval	1.6 μs	1.6 μs	1.6 μs

Source: IEEE Std. 802.11-2012, p. 1689.

68. In the method practiced by the '439 Accused Products, a number of samples from the symbol data portion of the first OFDM packet are shifted into the guard interval portion of the shifted version of the first OFDM packet, and the same number of samples from the guard interval portion of the first OFDM packet are shifted out of the guard interval portion of the shifted version of the first OFDM packet. For example, the Accused Products cyclically advance the number of samples corresponding to the time duration of $|T_{CS}|$ out of the symbol portion of the shifted OFDM packet and into the guard interval portion of the packet, while the same number of samples corresponding to the time duration of $|T_{CS}|$ are shifted out of the guard interval portion of the shifted OFDM packet, as illustrated below:

20.3.3 Transmitter block diagram

HT-mixed format and HT-greenfield format transmissions can be generated using a transmitter consisting of the following blocks:

a) *Scrambler* scrambles the data to reduce the probability of long sequences of 0s or 1s; see 20.3.11.3.

b) *Encoder parser*, if BCC encoding is to be used, demultiplexes the scrambled bits among N_{ES} (number of BCC encoders for the Data field) BCC encoders, in a round robin manner.

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Source: IEEE Std. 802.11-2012, p. 1683-84.

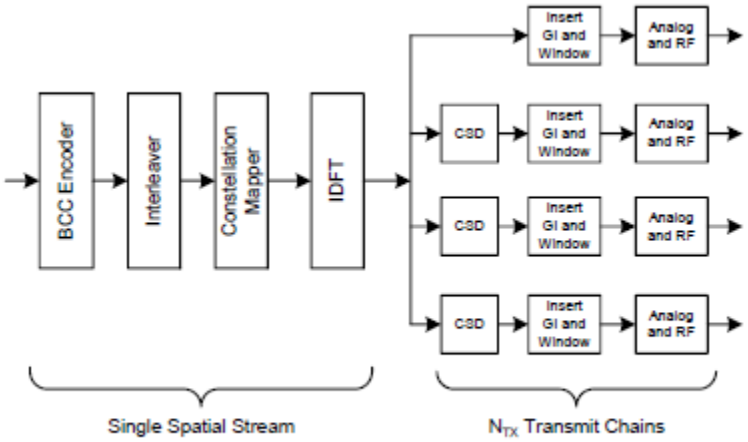

Figure 20-2—Transmitter block diagram 1

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20.3.9.3.2 Cyclic shift definition

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Cyclic shifts are used to prevent unintentional beamforming when the same signal or scalar multiples of one signal are transmitted through different spatial streams or transmit chains. A cyclic shift of duration T_{CS} on a signal $s(t)$ on interval $0 \le t \le T$ is defined as follows, where T is defined as T_{DFT} as referenced in Table 20-6.

With $T_{CS} \le 0$, replace $s(t)$ with $s(t - T_{CS})$ when $0 \le t < T + T_{CS}$ and with $s(t - T_{CS} - T)$ when $T + T_{CS} \le t \le T$. The cyclic-shifted signal is defined as shown in Equation (20-7).

$$s_{CS}(t;T_{CS})\big|_{T_{CS}<0} = \begin{cases} s(t - T_{CS}) & 0 \le t < T + T_{CS} \\ s(t - T_{CS} - T) & T + T_{CS} \le t \le T \end{cases} \quad (20\text{-}7)$$

The cyclic shift is applied to each OFDM symbol in the packet separately. Table 20-9 specifies the values for the cyclic shifts that are applied in the L-STF (in an HT-mixed format packet), the L-LTF, and L-SIG. It also applies to the HT-SIG in an HT-mixed format packet.

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Source: IEEE Std. 802.11-2012, p. 1695.

Table 20-5—Timing-related constants *(continued)*

T_{DFT}: IDFT/DFT period	3.2 μs
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Source: IEEE Std. 802.11n-2009, p. 266.

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r) For each group of N_{ST} subcarriers and each of the N_{TX} transmit chains, convert the subcarriers to time domain using IDFT. Prepend to the Fourier-transformed waveform a circular extension of itself, thus forming a GI, and truncate the resulting periodic waveform to a single OFDM symbol length by applying time domain windowing. Determine the length of the GI according to the GI_TYPE parameter of the TXVECTOR. Refer to 20.3.11.11 and 20.3.11.12 for details. When beamforming is not used, it is sometimes possible to implement the cyclic shifts in the time domain.

Source: IEEE Std. 802.11-2012, p. 1684, 1688.

The Cyclic Prefix for OFDM

In a previous post, we have elaborated about the building blocks of OFDM.

There, we have stated two benefits of using a cyclic prefix between subsequent OFDM symbols:

- The CP isolates different OFDM blocks from each other when the wireless channel contains multiple paths, i.e. is frequency-selective.
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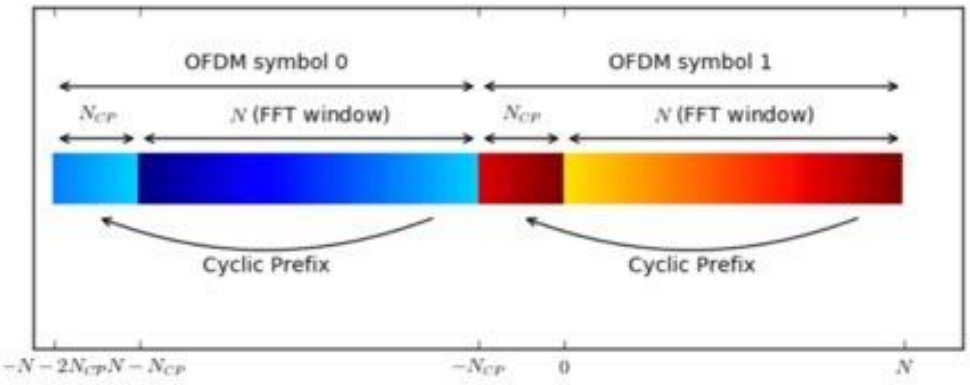
As we see, the CP of an OFDM symbol is obtained by prepending a copy of the last N_{CP} samples from the end of the OFDM signal to its beginning. This way we obtain a circular signal structure, i.e. the first N_{CP} and last N_{CP} samples are equal in each OFDM symbol.



In the above figure, we see two subsequent OFDM symbols, each having a dedicated CP. The colors encode the signal value. The cyclic prefix at the beginning of each OFDM symbol shows a copy of the color of end of the OFDM symbol. When the signal is demodulated, the N-point FFT is taken at the position after the CP, which is indicated with *FFT window*.

Source: *https://dspillustrations.com/pages/posts/misc/the-cyclic-prefix-cp-in-ofdm.html*

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$$r_{HT-SIG}^{i_{TX}}(t) = \frac{1}{\sqrt{N_{TX} \cdot N_{HT-SIG}^{Tone}}} \sum_{n=0}^{1} w_{T_{SYM}}(t - nT_{SYM}) \cdot \sum_{k=-26}^{26} (jD_{k,n} + p_{n+1}P_k)\exp(j2\pi k\Delta_F(t - nT_{SYM} - T_{GI} - T_{CS}^{i_{TX}})) \quad (20\text{-}16)$$

where

$$D_{k,n} = \begin{cases} 0, k = 0, \pm 7, \pm 21 \\ d_{M^r(k),n}, \text{otherwise} \end{cases}$$

$M^r(k)$ is defined in 20.3.9.3

P_k and p_n are defined in 18.3.5.10

N_{HT-SIG}^{Tone} has the value given in Table 20-8

$T_{CS}^{i_{TX}}$ represents the cyclic shift for transmit chain i_{TX} and is defined by Table 20-9 for HT-mixed format PPDUs.

Source: IEEE Std. 802.11-2012, pp. 1700-1701.

T_{GI2}: Double guard interval	1.6 µs	1.6 µs	1.6 µs

Source: IEEE Std. 802.11-2012, p. 1689.

2.7.4 Mixed Mode Preamble

The mixed mode preamble is needed for compatibility with IEEE 802.11a/g. It starts with the 802.11a/g preamble. The 802.11n mixed mode preamble for two spatial streams is shown in Figure 2.34. The legacy short training field (L-STF) is identical to 802.11a/g except that different transmitters use different cyclic delays (CDs). This also applies to the legacy long training field (L-LTF). The STFs from different transmitters have low cross-correlation. For example, a CD of –400 ns (or a cyclic advance of 400 ns) minimizes correlation between two different transmitted short symbols. The L-STF uses a CD of only –200 ns for two transmitters, since legacy 802.11a/g receivers may not be able to cope with larger CD values.

Source: B. Bing, Broadband Wireless Multimedia Networks, Wiley, 2013, p. 120.

With $T_{CS} \le 0$, replace $s(t)$ with $s(t - T_{CS})$ when $0 \le t < T + T_{CS}$ and with $s(t - T_{CS} - T)$ when $T + T_{CS} \le t \le T$. The cyclic-shifted signal is defined as shown in Equation (20-7).

$$s_{CS}(t;T_{CS})\big|_{T_{CS}<0} = \begin{cases} s(t - T_{CS}) & 0 \le t < T + T_{CS} \\ s(t - T_{CS} - T) & T + T_{CS} \le t \le T \end{cases} \quad (20\text{-}7)$$

Source: IEEE Std. 802.11-2012, pp. 1700-1701.

69. The method practiced by the '439 Accused Products includes substantially simultaneously transmitting the first OFDM packet and the shifted version of the OFDM packet. For example, the signals transmitted from different transmit chains are aligned and synchronized in the time domain, as seen below:

Figure 20-2 and Figure 20-3 show example transmitter block diagrams. In particular, Figure 20-2 shows the transmitter blocks used to generate the HT-SIG of the HT-mixed format PPDU.

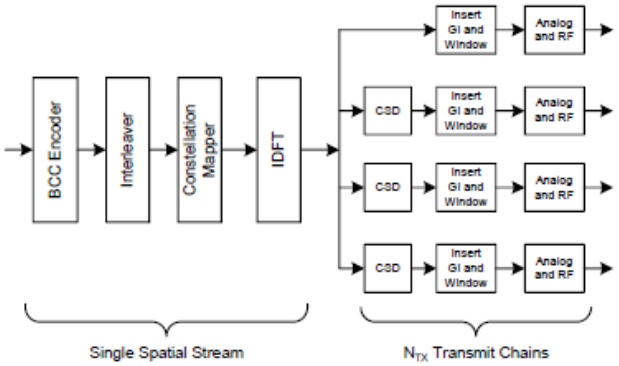

Figure 20-2—Transmitter block diagram 1

Source: IEEE Std. 802.11-2012, pp. 1684-85.

Radio Chains

Between the operating system and antenna, an 802.11 radio interface has to perform several tasks. When transmitting a frame, the main tasks are the inverse Fourier transform to turn the frequency-domain encoded signal into a time-domain signal, and amplification right before the signal hits the antenna so it has reasonable range. On the receive side, the process must be reversed. Immediately after entering the antenna, an amplifier boosts the faint signal received into something substantial enough to work with, and performs a Fourier transform to extract the subcarriers. In an 802.11 interface, these components are linked together and called a *radio chain*. Selecting the components to make up the radio chain is an important task for system designers, especially

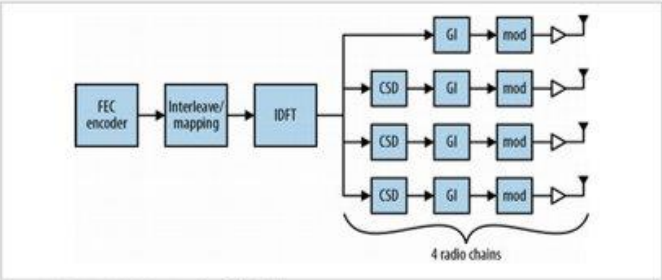

Figure 2-3. 4x4 802.11n interface block diagram

Source: Gast, Matthew, S., 802.11n A Survival Guide, O'Reilly, 2012, pp. 13-14.

70. Additionally, Defendant has been and currently is an active inducer of infringement of the '439 patent under 35 U.S.C. § 271(b) and a contributory infringer of the '439 patent under 35 U.S.C. § 271(c).

71. Defendant has actively induced, and continues to actively induce, infringement of the '439 patent by causing others to use, offer for sale, or sell in the United States, products or services covered by the '439 patent, including but not limited to the '439 Accused Products and any other products or services that include WiFi chipsets compliant with 802.11n, 802.11ac and/or 802.11ax, having the cyclic shift advance functionality described above. Defendant provides these products and services to others, such as customers, resellers, partners, and end-users, who, in turn, use, provision for use, offer for sale, or sell those products and services, which directly infringe the '439 patent as described above. Defendant's inducement includes requiring WiFi chipsets within the Accused Products to be compliant with the IEEE 802.11n, 802.11ac and 802.11ax standard, in which the cyclic advance diversity scheme described above is mandatory, and advertising and promoting such compliance to its customers, partners, re-sellers and the like, including the promotion, directions and instructions found at one or more of the following links, the provision of which is on-going as of the filing of this Complaint and much of the content of which is specifically illustrated above:

- https://www.tcl.com/us/en/products/mobile/tcl-30-series/tcl-30-v-5g

- https://www.tcl.com/global/en/mobile/tcl-20-5g/performance
- https://www.tcl.com/ro/ro/mobile/tcl20-5g/performance
- https://www.tcl.com/us/en/products/mobile/tcl-a-series/tcl-signa
- https://www.tcl.com/us/en/press-releases/tcl-expands-10-series-mobile-lineup
- https://www.tcl.com/global/en/mobile/tcl-20l/performance

72. Defendant has contributed to, and continues to contribute to, the infringement of the '439 patent by others by knowingly providing one or more components, for example the 802.11 WiFi chipset with cyclic shift (advance) functionality included in the Accused Products, a portion thereof, and/or the software/hardware modules responsible for the accused functionality described herein, that, when installed, configured, and used result in systems that, as intended by Defendant described above, directly infringe one or more claims of the '439 patent.

73. Defendant knew of the '439 patent, or should have known of the '439 patent, but was willfully blind to its existence. Upon information and belief, Defendant had actual knowledge of the '439 patent at least as early as Defendant received a copy of this Complaint, or alternatively, at least as early as the service upon Defendant of the Complaint in this action.

74. By the time of trial, Defendant will or should have known and intended (since receiving such notice) that its continued actions would infringe and would actively induce and contribute to the infringement of the '439 patent.

75. Defendant has committed, and continues to commit, contributory infringement by selling products and services that directly infringe the '439 patent when used by a third party, such as the Accused '439 Products, and that are a material part of the invention, knowing them to be especially made or adapted for use in infringement of the '439 patent and not staple articles or commodities of commerce suitable for substantial non-infringing use.

76. As a result of Defendant's acts of infringement, IV has suffered and will continue to suffer damages in an amount to be determined at trial.

PRAYER FOR RELIEF

IV requests that the Court enter judgment as follows:

(A) that Defendant has infringed the ’443 patent;

(B) that Defendant has infringed the ’439 patent;

(C) awarding damages sufficient to compensate IV for Defendant’s infringement under 35 U.S.C. § 284;

(D) finding this case exceptional under 35 U.S.C. § 285 and awarding IV its reasonable attorneys’ fees;

(E) awarding IV its costs and expenses incurred in this action;

(F) awarding IV prejudgment and post-judgment interest; and

(G) granting IV such further relief as the Court deems just and appropriate.

DEMAND FOR JURY TRIAL

IV demands trial by jury of all claims so triable under Federal Rule of Civil Procedure 38.

Dated: April 20, 2023.

Respectfully submitted,

/s/Karl Rupp

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