IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

DEEPWELL IP LLC,		§	Case No.
	Plaintiff,	§	**JURY TRIAL DEMANDED**
v.		§	
MEDIATEK INC.,		§	
	Defendant.	§	

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Deepwell IP LLC ("Deepwell" or "Plaintiff") for its Complaint against Defendant MediaTek Inc. ("MediaTek" or "Defendant") alleges as follows:

THE PARTIES

1. Deepwell is a limited liability company organized and existing under the laws of the State of Texas, with a place of business located at 100 W. Houston Street, Marshall, Texas 75670.

2. Upon information and belief, Defendant MediaTek Inc. is a Taiwanese corporation with its principal place of business located at No. 1, Dusing 1st Road, Hsinchu Science Park, Hsinchu City 30078 Taiwan, Republic of China and may be served pursuant to the provisions of the Hague Convention. Upon information and belief, MediaTek does business in Texas, directly or through intermediaries, and maintains its principal place of business in Taiwan.

JURISDICTION AND VENUE

3. This is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. §§ 1, *et seq*. This Court has subject matter jurisdiction over this action pursuant to 28 U.S.C. §§ 1331, 1332, 1338, and 1367.

4. This Court has specific and personal jurisdiction over the Defendant consistent with the requirements of the Due Process Clause of the United States Constitution and the Texas Long Arm Statute. Upon information and belief, the Defendant has sufficient minimum contacts with the forum because Defendant transacts substantial business in the State of Texas and in this Judicial District. Further, Defendant has, directly or through subsidiaries or intermediaries, committed and continues to commit acts of patent infringement in the State of Texas and in this Judicial District as alleged in this Complaint, as alleged more particularly below. For example, on information and belief, the Accused Products are available for purchase in this Judicial District.

5. Venue is proper in this Judicial District pursuant to 28 U.S.C. §1391(b) and (c) because the Defendant is a foreign company that may be sued in any Judicial District, including the Eastern District of Texas. The Defendant is subject to personal jurisdiction in this Judicial District and has committed acts of patent infringement in this Judicial District. On information and belief, the Defendant through its own acts and/or through the acts of others, makes, uses, sells, and/or offers to sell infringing products within this Judicial District, regularly does and solicits business in this Judicial District, and has the requisite minimum contacts with the Judicial District such that this venue is a fair and reasonable one. Further, upon information and belief, the Defendant has admitted or not contested proper venue in this Judicial District in other patent infringement actions.

PATENTS-IN-SUIT

6. On December 12, 2006, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 7,149,851 (the "'851 Patent") entitled "Method And System For Conservatively Managing Store Capacity Available To A Processor Issuing Stores." A true and correct copy of the '851 Patent is available at https://image-ppubs.uspto.gov/dirsearch-public/print/downloadPdf/7149851.

7. On January 12, 2010, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 7,645,664 (the "'664 Patent") entitled "Layout Pattern For Deep Well Region To Facilitate Routing Body-bias Voltage." A true and correct copy of the '664 Patent is available at https://image-ppubs.uspto.gov/dirsearch-public/print/downloadPdf/7645664.

8. On April 9, 2013, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 8,415,730 (the "'730 Patent") entitled "Selective Coupling Of Voltage Feeds For Body Bias Voltage In An Integrated Circuit Device." A true and correct copy of the '730 Patent is available at https://image-ppubs.uspto.gov/dirsearch-public/print/downloadPdf/8415730.

9. On February 19, 2013, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. RE44,025 (the "'025 Patent") entitled "Apparatus And Method For Integrated Circuit Power Management." A true and correct copy of the '025 Patent is available at https://image-ppubs.uspto.gov/dirsearch-public/print/downloadPdf/RE44025.

10. Deepwell is the sole and exclusive owner of all right, title, and interest to and in the '851 Patent, '664 Patent, '730 Patent, and '025 Patent (together, the "Patents-in-Suit"), and holds the exclusive right to take all actions necessary to enforce its rights to the Patents-in-Suit, including the filing of this patent infringement lawsuit. Deepwell also has the right to recover all damages

for past, present, and future infringement of the Patents-in-Suit and to seek injunctive relief as appropriate under the law.

INFRINGEMENT ALLEGATIONS

11. The Patents-in-Suit generally cover integrated circuits that have adaptive body bias ("ABB") capabilities. The technology was developed by Transmeta Corporation. In some embodiments of the inventions, the layout of the integrated circuits will have deep well voltage distribution. In other embodiments, Bias Network Coupling can be detected via ABB capabilities and then if the bias voltage pin(s) can be left unconnected or floating as an allowed configuration. These techniques are incorporated into chips made by numerous manufacturers, including MediaTek.

12. MediaTek has manufactured, used, marketed, distributed, sold, offered for sale, exported from, and imported into the United States, products that infringe the Patents-in-Suit. Upon information and belief, these products include all MediaTek SoCs with ARM cores, including at least the MT8186 and Dimensity 1050 SoCs. For example, on information and belief, the MT8186 SoC is sold in the United States and incorporated by others into products sold in the United States, such as the Lenovo Chromebook. For example, on information and belief, the Dimensity 1050 SoC is sold in the United States and incorporated by others into products sold in the United States, such as the Motorola Edge 2022.

13. Deepwell has at all times complied with the marking provisions of 35 U.S.C. § 287 with respect to the Patents-in-Suit.

COUNT I
(Infringement of the '851 Patent)

14. Paragraphs 1 through 13 are incorporated by reference as if fully set forth herein.

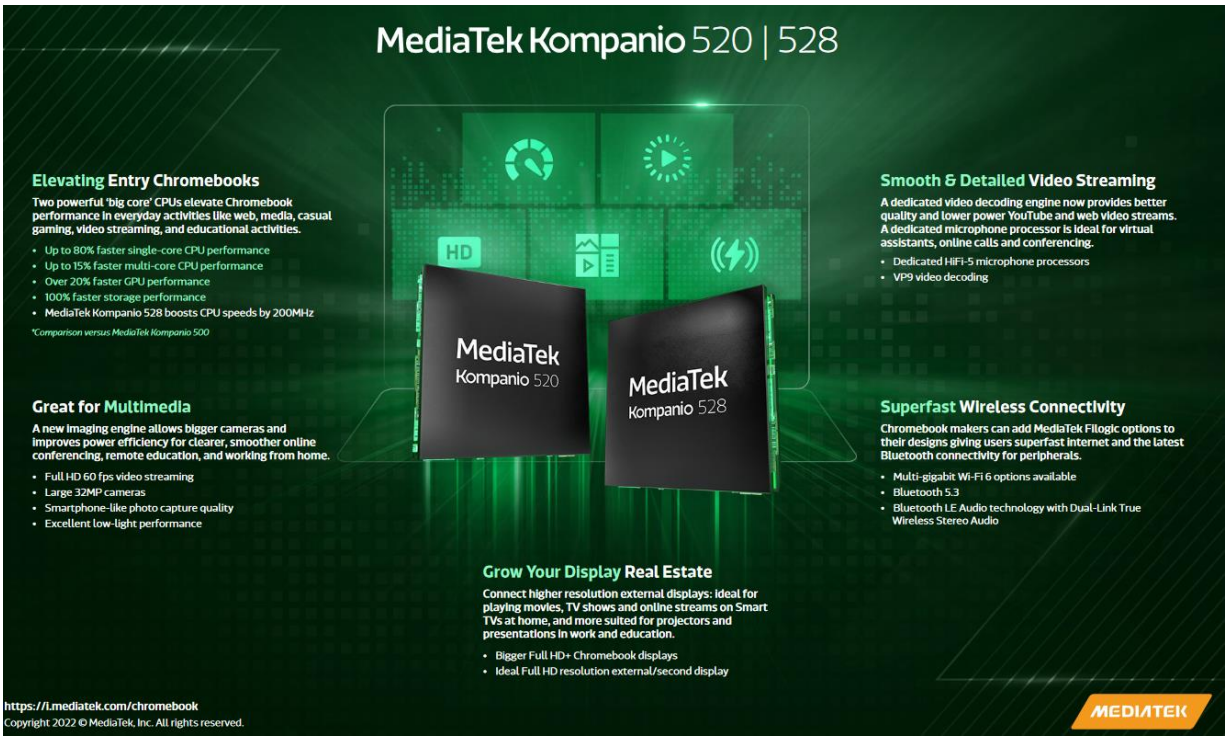
15. Deepwell has not licensed or otherwise authorized MediaTek to make, use, offer for sale, sell, or import any products that embody the inventions of the ’851 Patent.

16. Defendant has and continues to directly infringe the ’851 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States products that satisfy each and every limitation of one or more claims of the ’851 Patent. Upon information and belief, these products include all MediaTek SoCs with ARM cores, including at least the MT8186 SoC, which are sold in the United States and incorporated by others into products sold in the United States, such as the Lenovo Chromebook.

17. For example, Defendant has and continues to directly infringe at least claim 35 of the ’851 Patent by making, using, offering to sell, selling, and/or importing into the United States products that practice a method of conservatively managing a store capacity of a store container receiving issued stores from a processor having a counter mechanism, said method comprising: incrementing said counter mechanism when a store is issued; decrementing said counter mechanism for each decrementing condition occurring relative to said store capacity; and when a value of said counter mechanism equals a predetermined value, executing a response to determine whether said store capacity has been exceeded.

18. The Accused Products practice a method of conservatively managing a store capacity of a store container receiving issued stores from a processor having a counter mechanism. For example, upon information and belief, the MT8186 and the Lenovo Chromebook comprises the processor store buffer that handles multiple entries with an embedded counter used to handle/indicate the capacity of the store buffer. For example, upon information and belief, the MT8186 and the Lenovo Chromebook comprise ARM core processors that have a cache controller

which includes a Store buffer (*i.e.*, store container) to hold the data before writing into the cache RAMs. Store buffers are responsible for storing the write requests (*i.e.*, issue stores) from the processors.



[1]

8.5.1 Store buffer

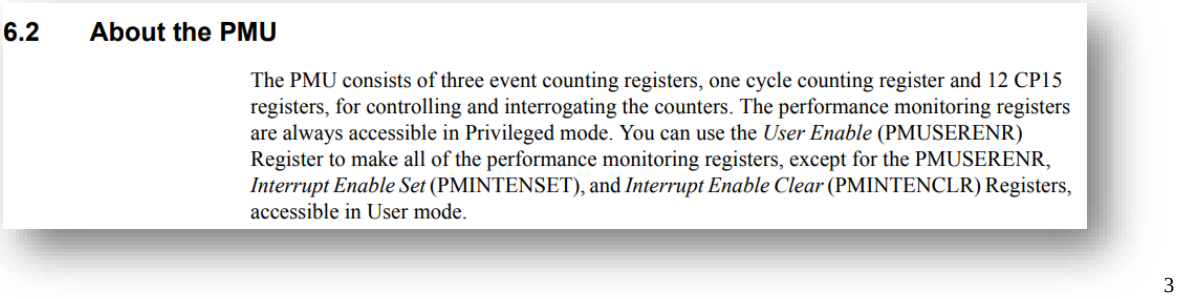
The cache controller includes a store buffer to hold data before it is written to the cache RAMs or passed to the AXI master interface. The store buffer has four entries. Each entry can contain up to 64 bits of data and a 32-bit address. All write requests from the data side that are not to a TCM interface are stored in the store buffer.

[2]

[1] https://mediatek-marketing.files.svdcdn.com/production/documents/MediaTek_Kompanio_520-528_infographic.pdf?dm=1684470677. Upon information and belief, the MediaTek MT8186 is also known as the MediaTek Kompanio 520. *See* https://chromeunboxed.com/chromebook-tablet-mediatek-kompanio-520-starmie/; https://www.phoronix.com/news/Panfrost-Linux-6.4-New-Hardware

[2] https://documentation-service.arm.com/static/5fbd26f271eff94ef49c7020?token=

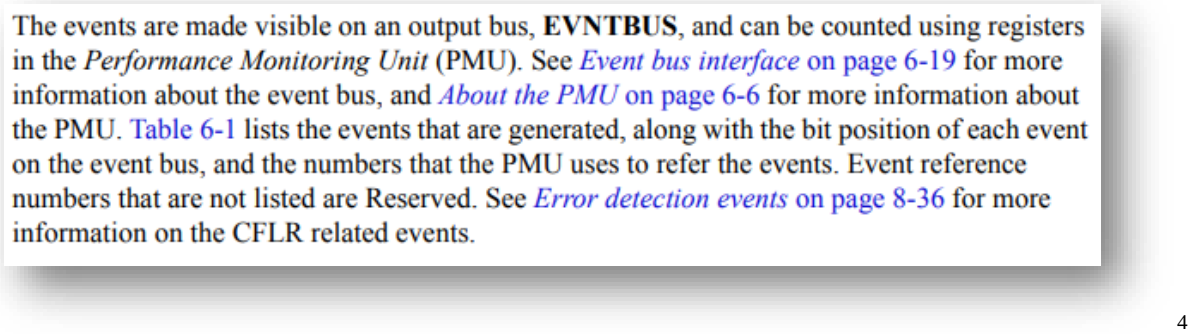
19. For example, upon information and belief, the Performance Monitoring Unit (PMU) primarily consists of multiple monitors and event counters. Different types of events are made visible on an output bus, EVNTBUS, and can be counted using registers in the Performance Monitoring Unit (PMU) (*i.e.*, a counter mechanism).



6.2 About the PMU

The PMU consists of three event counting registers, one cycle counting register and 12 CP15 registers, for controlling and interrogating the counters. The performance monitoring registers are always accessible in Privileged mode. You can use the *User Enable* (PMUSERENR) Register to make all of the performance monitoring registers, except for the PMUSERENR, *Interrupt Enable Set* (PMINTENSET), and *Interrupt Enable Clear* (PMINTENCLR) Registers, accessible in User mode.

[3]



The events are made visible on an output bus, **EVNTBUS**, and can be counted using registers in the *Performance Monitoring Unit* (PMU). See *Event bus interface* on page 6-19 for more information about the event bus, and *About the PMU* on page 6-6 for more information about the PMU. Table 6-1 lists the events that are generated, along with the bit position of each event on the event bus, and the numbers that the PMU uses to refer the events. Event reference numbers that are not listed are Reserved. See *Error detection events* on page 8-36 for more information on the CFLR related events.

[4]

20. For example, upon information and belief, EVNTBUS bit position [4]- "Data Write architecturally executed" in the Performance Monitor Counters is responsible for counting the data writes (*i.e.*, a counter mechanism for counting issued stores). The Performance Monitor Counter also has registers with bit positions [18] and [21] responsible for counting the number of writebacks and drains.

[3] https://documentation-service.arm.com/static/5fbd26f271eff94ef49c7020?token=
[4] https://documentation-service.arm.com/static/5fbd26f271eff94ef49c7020?token=

Table 6-1 Event bus interface bit functions

EVNTBUS bit position	Description	CFLR update	Event Ref. Value
N/A	Software increment. The register is incremented only on writes to the Software Increment Register. See *c9, Software Increment Register* on page 6-12.	-	0x00
[0]	Instruction cache miss. Each instruction fetch from normal cacheable memory that causes a refill from the L2 memory system generates this event. Accesses that do not cause a new cache refill, but are satisfied from refilling data of a previous miss are not counted. Where instruction fetches consist of multiple instructions, these accesses count as single events. CP15 cache maintenance operations do not count as events.	-	0x01
[1]	Data cache miss. Each data read from or write to normal cacheable memory that causes a refill from the L2 memory system generates this event. Accesses that do not cause a new cache refill, but are satisfied from refilling data of a previous miss are not counted. Each access to a cache line to normal cacheable memory that causes a new linefill is counted, including the multiple transactions of an LDM and STM. Write-through writes that hit in the cache do not cause a linefill and so are not counted. CP15 cache maintenance operations do not count as events.	-	0x03
[2]	Data cache access. Each access to a cache line is counted including the multiple transactions of an LDM, STM, or other operations. CP15 cache maintenance operations do not count as events.	-	0x04
[3]	Data Read architecturally executed. This event occurs for every instruction that explicitly reads data, including SWP.	-	0x06
[4]	Data Write architecturally executed. This event occurs for every instruction that explicitly writes data, including SWP.	-	0x07

[5]

[18]	Data cache write-back. This event occurs once for each line that is written back from the cache.	-	0x42
[19]	External memory request. Examples of this are cache refill, Non-cacheable accesses, write-through writes, cache line evictions (write-back).	-	0x43
[20]	Stall because of LSU being busy. This event takes place each clock cycle where the condition is met. A high incidence of this event indicates the pipeline is often waiting for transactions to complete on the external bus.	-	0x44
[21]	Store buffer was forced to drain completely. Examples of this are DMB, Strongly-ordered memory access, or similar events.	-	0x45

[6]

[5] https://documentation-service.arm.com/static/5fbd26f271eff94ef49c7020?token=
[6] https://documentation-service.arm.com/static/5fbd26f271eff94ef49c7020?token=

Figure 6-5 shows the PMSWINC bit assignments.

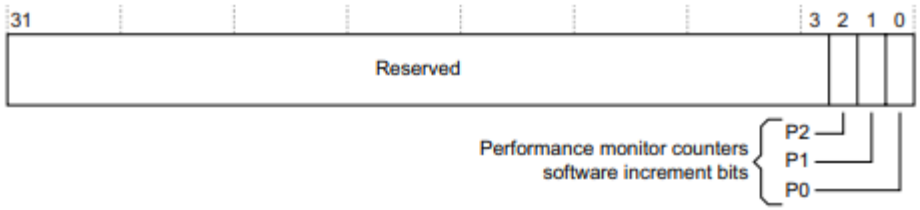


Figure 6-5 PMSWINC Register bit assignments

Table 6-6shows the PMSWINC bit assignments.

Table 6-6 PMSWINC Register bit assignments

Bits	Name	Function
[31:3]	-	RAZ on reads, SBZP on writes
[2]	P2	Increment Counter 2
[1]	P1	Increment Counter 1
[0]	P0	Increment Counter 0

To access the PMSWINC Register, read or write CP15 with:

```
MRC p15, 0, <Rd>, c9, c12, 4 ; Read  PMSWINC Register
MCR p15, 0, <Rd>, c9, c12, 4 ; Write PMSWINC Register
```

[7]

6.3.6 c9, Performance Counter Selection Register

The PMSELR Register characteristics are:

Purpose

- selects an Event Count Register.
- determines which count register is accessed or controlled by accesses to the Event Type Selection Register and the Event Count Register.

[8]

[7] https://documentation-service.arm.com/static/5fbd26f271eff94ef49c7020?token=
[8] https://documentation-service.arm.com/static/5fbd26f271eff94ef49c7020?token=

Figure 6-6 shows the PMSELR bit assignments.

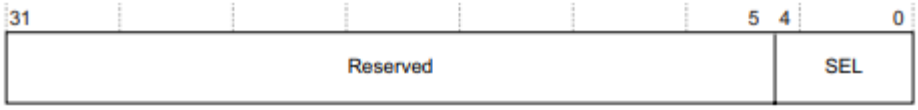


Figure 6-6 PMSELR Register bit assignments

Table 6-7 shows the PMSELR bit assignments.

Table 6-7 PMSELR Register bit assignments

Bits	Name	Function
[31:5]	-	RAZ on reads, SBZP on writes
[4:0]	SEL	Counter select: b00000 = selects counter 0 b00001 = selects counter 1 b00010 = selects counter 2.

Any values programmed in the PMSELR Register other than those specified in Table 6-7 are Unpredictable.

To access the PMSELR Register, write CP15 with:

```
MCR p15, 0, <Rd>, c9, c12, 5 ; Write PMSELR Register
```

[9]

21. Further, in addition to the above, the Programmer Guide for ARM v8-A Instruction sets also mentions the cache controller, cache policies, and cache maintenance system which are responsible for managing the cache memory. Cache coherency can also be monitored by the built-in Performance monitoring unit (*i.e.*, counter mechanism).

[9] https://documentation-service.arm.com/static/5fbd26f271eff94ef49c7020?token=

11.2 Cache controller

The cache controller is a hardware block responsible for managing the cache memory, in a way that is largely invisible to the program. It automatically writes code or data from main memory into the cache. It takes read and write memory requests from the core and performs the necessary actions to the cache memory or the external memory.

10

11.3 Cache policies

The cache policies enable us to describe when a line should be allocated to the data cache and what should happen when a store instruction is executed that hits in the data cache.

The cache allocation policies are:

Write allocation (WA)

A cache line is allocated on a write miss. This means that executing a store instruction on the processor might cause a burst read to occur. There is a linefill to obtain the data for the cache line, before the write is performed. The cache contains the whole line, which is its smallest loadable unit, even if you are only writing to a single byte within the line.

Read allocation (RA)

A cache line is allocated on a read miss.

The cache update policies are:

Write-back (WB)

A write updates the cache only and marks the cache line as dirty. External memory is updated only when the line is evicted or explicitly cleaned.

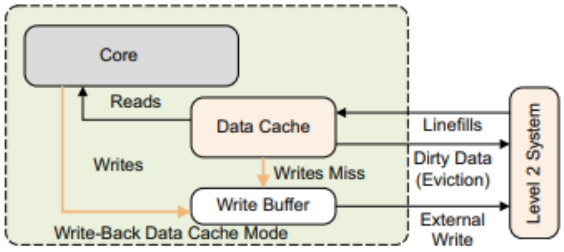
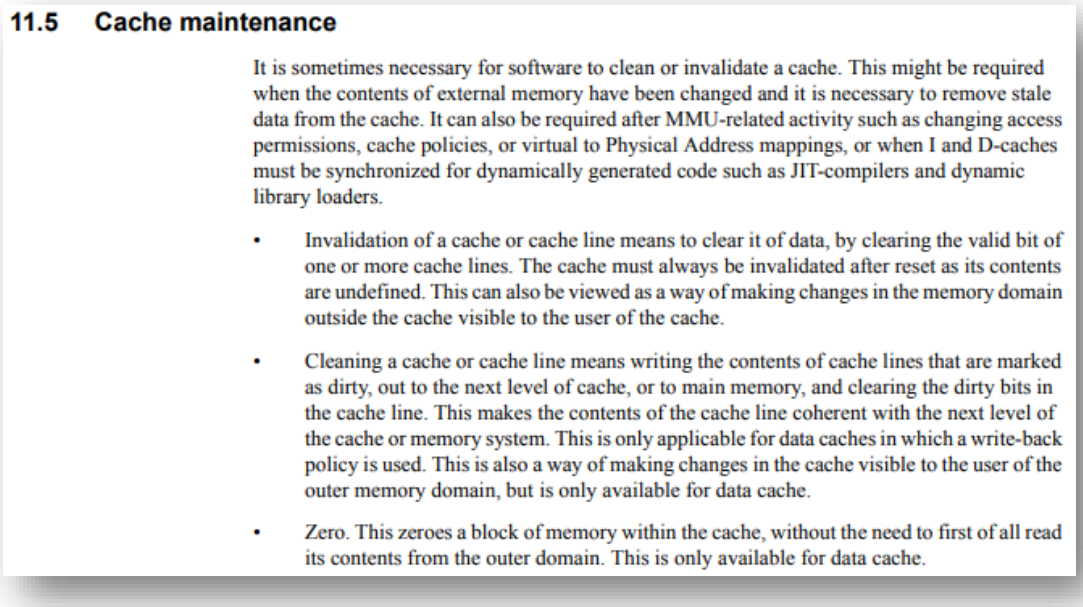


Figure 11-8 Write-back

11

[10] https://documentation-service.arm.com/static/5fbd26f271eff94ef49c7020?token=
[11] https://documentation-service.arm.com/static/5fbd26f271eff94ef49c7020?token=



11.5 Cache maintenance

It is sometimes necessary for software to clean or invalidate a cache. This might be required when the contents of external memory have been changed and it is necessary to remove stale data from the cache. It can also be required after MMU-related activity such as changing access permissions, cache policies, or virtual to Physical Address mappings, or when I and D-caches must be synchronized for dynamically generated code such as JIT-compilers and dynamic library loaders.

- Invalidation of a cache or cache line means to clear it of data, by clearing the valid bit of one or more cache lines. The cache must always be invalidated after reset as its contents are undefined. This can also be viewed as a way of making changes in the memory domain outside the cache visible to the user of the cache.
- Cleaning a cache or cache line means writing the contents of cache lines that are marked as dirty, out to the next level of cache, or to main memory, and clearing the dirty bits in the cache line. This makes the contents of the cache line coherent with the next level of the cache or memory system. This is only applicable for data caches in which a write-back policy is used. This is also a way of making changes in the cache visible to the user of the outer memory domain, but is only available for data cache.
- Zero. This zeroes a block of memory within the cache, without the need to first of all read its contents from the outer domain. This is only available for data cache.

12

22. The Accused Products further practice a method incrementing said counter mechanism when a store is issued. For example, upon information and belief, the MT8186 and the Lenovo Chromebook indicate that the counter is incremented when a store is issued. Upon information and belief, EVNTBUS bit position [4] in the Performance Monitor Counters having registers is responsible for counting the data writes (*i.e.*, issued stores), bit positions [18] and [21] responsible for counting the number of writebacks and drains (as shown above).

23. Further, upon information and belief, Performance Monitoring Unit (PMU) primarily consists of multiple monitors and event counters. These monitors are non-monotonic and can increment their value when a particular resource is allocated (*i.e.*, counter mechanism is incremented when a store is issued).

[12] https://documentation-service.arm.com/static/5fbd26f271eff94ef49c7020?token=

The CoreSight architecture provides a set of standard interfaces and programmer model views enabling partners to define CoreSight components and integrate them within the CoreSight infrastructure.

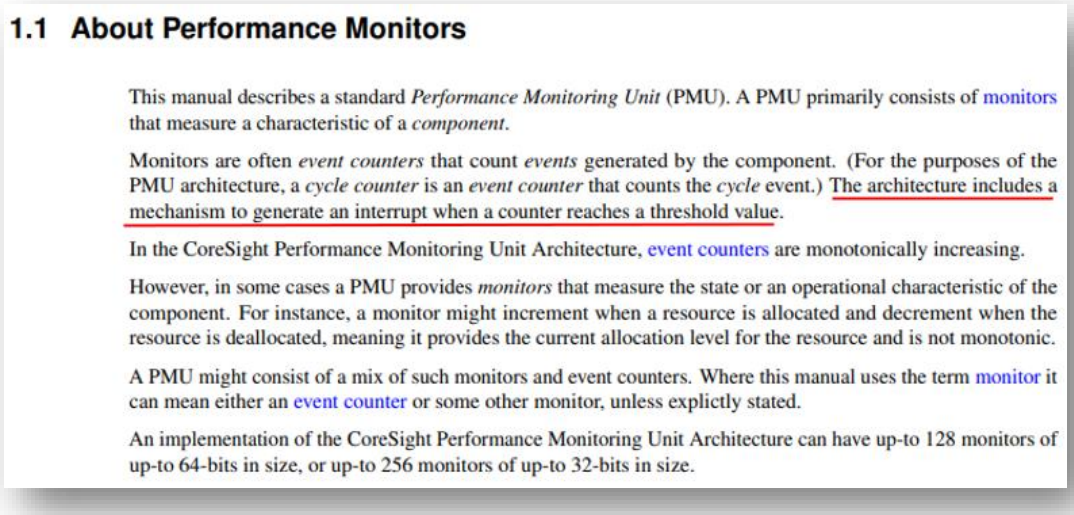
Debug Interface (ADI)	The Arm Debug Interface (ADI) defines the interface for debug components in an embedded SoC.
High Speed Serial Trace Port (HSSTP)	The HSSTP architecture defines a Serial Transmit Port (STP) as a replacement for an existing parallel data output port. It is suitable for transmitting high bandwidth data off-chip such as from the CoreSight solution.
Serial Wire Debug (SWD)	The Serial Wire Debug (SWD) provides a debug port for severely pin-limited packages. It is often used in small package microcontrollers, but also in complex ASICs where limiting pin count is critical and can be the controlling factor in device costs.
CoreSight-BSA	The CoreSight Base System Architecture (CoreSight-BSA) defines the hardware system architecture for debug functionality. It enables standard software - operating systems, debug and performance optimization software - to work seamlessly across compliant devices.
Embedded Trace Router (ETR)	The Embedded Trace Router (ETR) is a form of CoreSight Trace Memory Controller (EMC) trace sink. It acts as a bridge between the trace and memory fabrics, and its function is to write formatted trace to a buffer in memory.
Performance Monitoring Unit (PMU)	The Performance Monitoring Unit (PMU) architecture defines standard monitors such as event counters and performance monitors, used, for example, for profiling, software optimization and monitoring.

[13]

24. The Accused Products further practice a method for decrementing said counter mechanism for each decrementing condition occurring relative to said store capacity. Upon information and belief, the MT8186 and the Lenovo Chromebook decrements the counter when a store buffer entry is drained. Further, Performance Monitoring Unit (PMU) primarily consists of multiple monitors and event counters. Upon information and belief, these monitors are non-monotonic and can decrement their value when a particular resource is allocated. Upon information and belief, a counter may decrement on a condition based on store capacity (*i.e.*, counter mechanism is decremented when a store is issued).

25. The Accused Products further practice a method when a value of said counter mechanism equals a predetermined value, executing a response to determine whether said store capacity has been exceeded. Upon information and belief, the MT8186 and the Lenovo Chromebook practices a method where the monitors in the Standard PMU Architecture are event counters that count events generated by the component and generate an interrupt when a counter reaches a threshold value (*i.e.*, a predetermined value a response is executed to determine whether said store capacity has been exceeded).

[13] https://developer.arm.com/Architectures/CoreSight%20Architecture



1.1 About Performance Monitors

This manual describes a standard *Performance Monitoring Unit* (PMU). A PMU primarily consists of monitors that measure a characteristic of a *component*.

Monitors are often *event counters* that count *events* generated by the component. (For the purposes of the PMU architecture, a *cycle counter* is an *event counter* that counts the *cycle* event.) The architecture includes a mechanism to generate an interrupt when a counter reaches a threshold value.

In the CoreSight Performance Monitoring Unit Architecture, event counters are monotonically increasing.

However, in some cases a PMU provides *monitors* that measure the state or an operational characteristic of the component. For instance, a monitor might increment when a resource is allocated and decrement when the resource is deallocated, meaning it provides the current allocation level for the resource and is not monotonic.

A PMU might consist of a mix of such monitors and event counters. Where this manual uses the term monitor it can mean either an event counter or some other monitor, unless explictly stated.

An implementation of the CoreSight Performance Monitoring Unit Architecture can have up-to 128 monitors of up-to 64-bits in size, or up-to 256 monitors of up-to 32-bits in size.

14

26. Defendant has and continues to indirectly infringe one or more claims of the ’851 Patent by knowingly and intentionally inducing others, including MediaTek customers and end-users of the Accused Products and products that include the Accused Products, to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling, and/or importing into the United States products that include infringing technology, such as the MT8186 and the Lenovo Chromebook.

27. Defendant, with knowledge that these products, or the use thereof, infringe the ’851 Patent by no later than the date of this Complaint, knowingly and intentionally induced, and continues to knowingly and intentionally induce, direct infringement of the ’851 Patent by providing these products to customers and/or distributors for use in an infringing manner in the United States including, but not limited to, products that include infringing technology, such as the MT8186 and the Lenovo Chromebook. For example, MediaTek’s instruction manuals, websites, promotional materials, advertisements, and other information demonstrate to others,

[14] https://documentation-service.arm.com/static/5fbbcfacca04df4095c1d67f?token=

including customers, prospective customers, and distributors, how to use the Accused Products in an infringing manner. Upon information and belief, MediaTek is aware that the normal and customary use of the Accused Products by customers, distributors, and others would infringe the '851 Patent.

28. Defendant induced infringement by others, including customers and distributors, with the intent to cause infringing acts by others or, in the alternative, with the belief that there was a high probability that others, including end-users, infringe the '851 Patent, but while remaining willfully blind to the infringement.

29. Deepwell has suffered damages as a result of Defendant's direct and indirect infringement of the '851 Patent in an amount to be proved at trial.

30. Deepwell has suffered, and will continue to suffer, irreparable harm as a result of Defendant's infringement of the '851 Patent, for which there is no adequate remedy at law, unless Defendant's infringement is enjoined by this Court. Accordingly, Deepwell seeks a preliminary and permanent injunction enjoining MediaTek from making, using, importing, offering to sell, and/or selling the Accused Products, including, upon information and belief, all MediaTek SoCs with ARM cores, including at least the MT8186 SoC, which are sold in the United States and incorporated by others into products sold in the United States, such as the Lenovo Chromebook.

COUNT II
(Infringement of the '664 Patent)

31. Paragraphs 1 through 13 are incorporated by reference as if fully set forth herein.

32. Deepwell has not licensed or otherwise authorized MediaTek to make, use, offer for sale, sell, or import any products that embody the inventions of the '664 Patent.

33. Defendant has and continues to directly infringe the '664 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making,

using, offering to sell, selling, and/or importing into the United States products that satisfy each and every limitation of one or more claims of the '664 Patent. Upon information and belief, these products include all MediaTek SoCs with ARM cores, including at least the Dimensity 1050 SoC with mmWave capability, which are sold in the United States and incorporated by others into products sold in the United States.

[15]

34. For example, Defendant has and continues to directly infringe at least claim 1 of the '664 Patent by making, using, offering to sell, selling, and/or importing into the United States products that practice a method of routing a voltage in a semiconductor device, said method comprising: forming a plurality of well regions of a first conductivity to receive said voltage; forming a sub-surface structure of said first conductivity coupled to said well regions, wherein said

[15] https://mediatek-marketing.files.svdcdn.com/production/documents/MediaTek-Dimensity-1050-Infographic-0522.pdf?dm=1684470668

sub-surface structure comprises a portion having a depth greater than depth of said well regions; and forming at least one contact coupled to said sub-surface structure, wherein said contact receives said voltage to enable said sub-surface structure to route said voltage to said well regions.

35. The Accused Products practice a method of routing a voltage in a semiconductor device.

36. The Accused Products further practice said method forming a plurality of well regions of a first conductivity to receive said voltage.

37. The Accused Products further practice said method forming a sub-surface structure of said first conductivity coupled to said well regions, wherein said sub-surface structure comprises a portion having a depth greater than depth of said well regions.

38. The Accused Products further practice said method forming at least one contact coupled to said sub-surface structure, wherein said contact receives said voltage to enable said sub-surface structure to route said voltage to said well regions.

39. Defendant has and continues to indirectly infringe one or more claims of the ’664 Patent by knowingly and intentionally inducing others, including MediaTek customers and end-users of the Accused Products and products that include the Accused Products, to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling, and/or importing into the United States products that include infringing technology, such as the Dimensity 1050.

40. Defendant, with knowledge that these products, or the use thereof, infringe the ’664 Patent by no later than the date of this Complaint, knowingly and intentionally induced, and continues to knowingly and intentionally induce, direct infringement of the ’664 Patent by providing these products to customers and/or distributors for use in an infringing manner in the

United States including, but not limited to, products that include infringing technology, such as the Dimensity 1050 and Motorola Edge 2022. For example, MediaTek's instruction manuals, websites, promotional materials, advertisements, and other information demonstrate to others, including customers, prospective customers, and distributors, how to use the Accused Products in an infringing manner. Upon information and belief, MediaTek is aware that the normal and customary use of the Accused Products by customers, distributors, and others would infringe the '664 Patent.

41. Defendant induced infringement by others, including customers and distributors, with the intent to cause infringing acts by others or, in the alternative, with the belief that there was a high probability that others, including end-users, infringe the '664 Patent, but while remaining willfully blind to the infringement.

42. Deepwell has suffered damages as a result of Defendant's direct and indirect infringement of the '644 Patent in an amount to be proved at trial.

43. Deepwell has suffered, and will continue to suffer, irreparable harm as a result of Defendant's infringement of the '664 Patent, for which there is no adequate remedy at law, unless Defendant's infringement is enjoined by this Court. Accordingly, Deepwell seeks a preliminary and permanent injunction enjoining MediaTek from making, using, importing, offering to sell, and/or selling the Accused Products, including, upon information and belief, all MediaTek SoCs with ARM cores, including at least the Dimensity 1050 SoC, which are sold in the United States and incorporated by others into products sold in the United States, such as the Motorola Edge 2022.

COUNT III
(Infringement of the '730 Patent)

44. Paragraphs 1 through 13 are incorporated by reference as if fully set forth herein.

45. Deepwell has not licensed or otherwise authorized MediaTek to make, use, offer for sale, sell, or import any products that embody the inventions of the ’730 Patent.

46. Defendant has and continues to directly infringe the ’730 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States products that satisfy each and every limitation of one or more claims of the ’730 Patent. Upon information and belief, these products include all MediaTek SoCs with ARM cores, including at least the MT8186 SoC, which are sold in the United States and incorporated by others into products sold in the United States, such as the Lenovo Chromebook.

47. For example, Defendant has and continues to directly infringe at least claim 16 of the ’730 Patent by making, using, offering to sell, selling, and/or importing into the United States products that practice a method of providing a body bias voltage in a semiconductor device comprising: responsive to a coupling of an external body bias voltage to said semiconductor device, coupling said body bias voltage to body biasing wells of said semiconductor device.

48. The Accused Products practice a method of providing a body bias voltage in a semiconductor device. For example, upon information and belief, the MT8186 and the Lenovo Chromebook comprises a body bias distribution circuit to provide voltage.

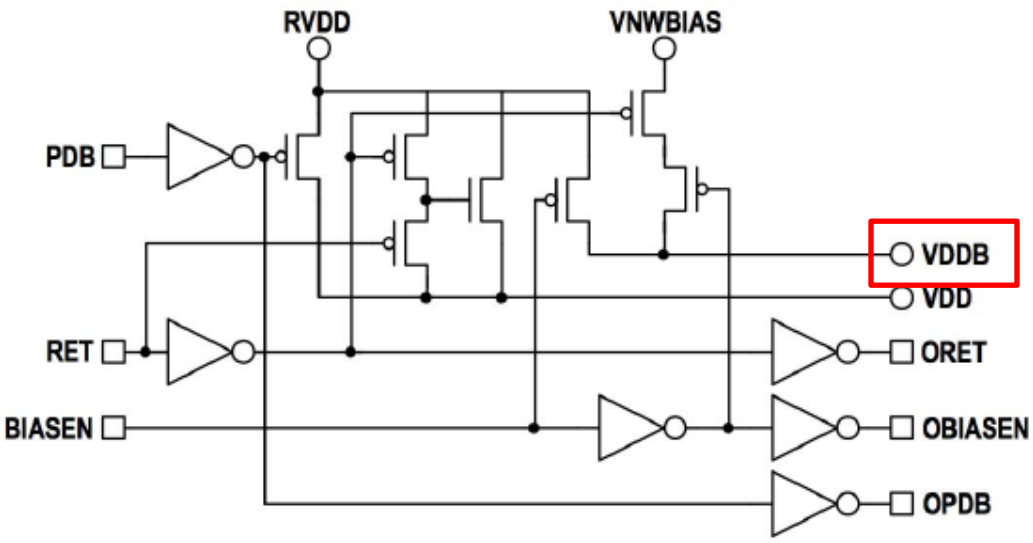


Figure 23.3.2: Hybrid power, retention, body-bias switch.

[16]

49. The Accused Products further practice a method responsive to a coupling of an external body bias voltage to said semiconductor device, coupling said body bias voltage to body biasing wells of said semiconductor device. For example, upon information and belief, the MT8186 in the Lenovo Chromebook comprises transistors that couple a power rail inside the semiconductor device to a body bias distribution depending on if voltage is applied.

[16] Hugh Mair, et al. "A Highly Integrated Smartphone SoC Featuring a 2.5GHz Octa-Core CPU with Advanced High-Performance and Low-Power Techniques," 2015 IEEE International Solid-State Circuits Conference, pp. 424-426

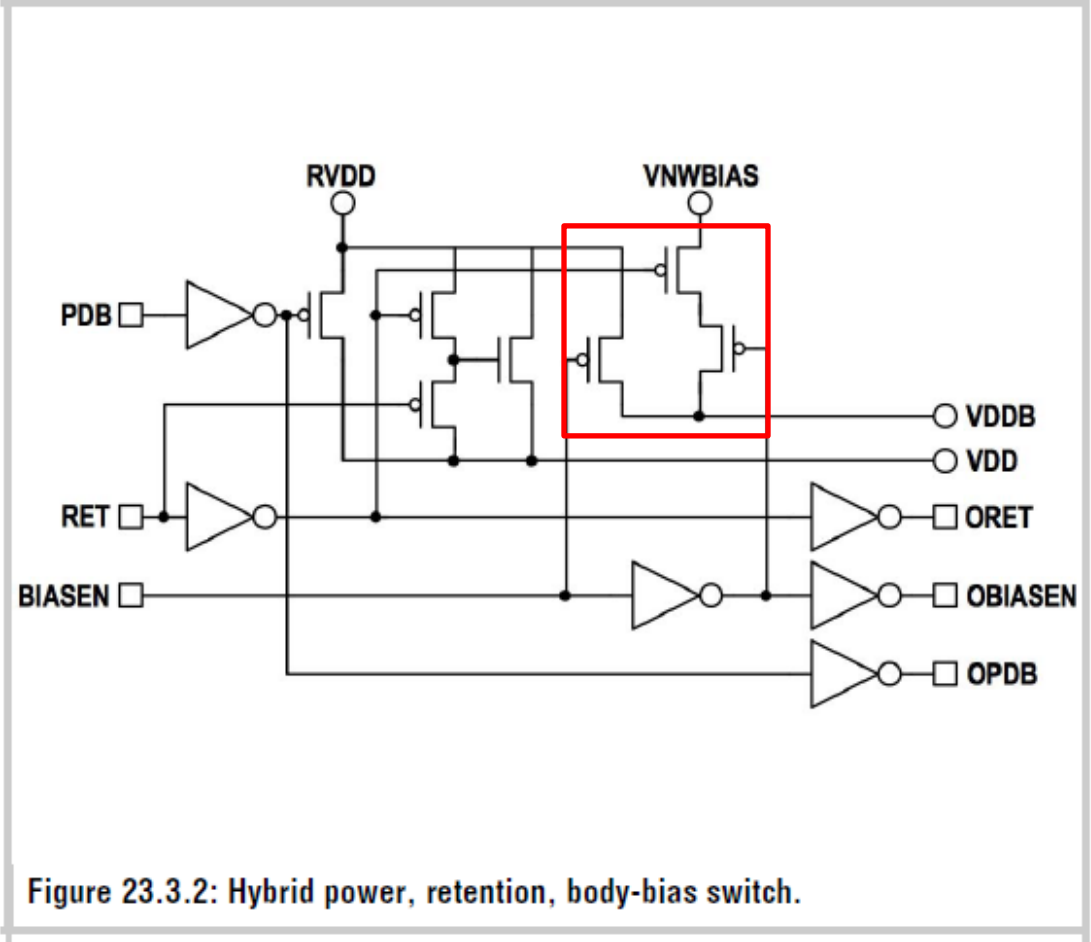


Figure 23.3.2: Hybrid power, retention, body-bias switch.

[17]

50. Defendant has and continues to indirectly infringe one or more claims of the '730 Patent by knowingly and intentionally inducing others, including MediaTek customers and end-users of the Accused Products and products that include the Accused Products, to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling, and/or importing into the United States products that include infringing technology, such as the MT8186 and the Lenovo Chromebook.

51. Defendant, with knowledge that these products, or the use thereof, infringe the '730 Patent by no later than the date of this Complaint, knowingly and intentionally induced, and

[17] Hugh Mair, et al. "A Highly Integrated Smartphone SoC Featuring a 2.5GHz Octa-Core CPU with Advanced High-Performance and Low-Power Techniques," 2015 IEEE International Solid-State Circuits Conference, pp. 424-426

continues to knowingly and intentionally induce, direct infringement of the '730 Patent by providing these products to customers and/or distributors for use in an infringing manner in the United States including, but not limited to, products that include infringing technology, such as the MT8186 and the Lenovo Chromebook. For example, MediaTek's instruction manuals, websites, promotional materials, advertisements, and other information demonstrate to others, including customers, prospective customers, and distributors, how to use the Accused Products in an infringing manner. Upon information and belief, MediaTek is aware that the normal and customary use of the Accused Products by customers, distributors, and others would infringe the '730 Patent.

52. Defendant induced infringement by others, including customers and distributors, with the intent to cause infringing acts by others or, in the alternative, with the belief that there was a high probability that others, including end-users, infringe the '730 Patent, but while remaining willfully blind to the infringement.

53. Deepwell has suffered damages as a result of Defendant's direct and indirect infringement of the '730 Patent in an amount to be proved at trial.

54. Deepwell has suffered, and will continue to suffer, irreparable harm as a result of Defendant's infringement of the '730 Patent, for which there is no adequate remedy at law, unless Defendant's infringement is enjoined by this Court. Accordingly, Deepwell seeks a preliminary and permanent injunction enjoining MediaTek from making, using, importing, offering to sell, and/or selling the Accused Products, including, upon information and belief, all MediaTek SoCs with ARM cores, including at least the MT8186 SoC, which are sold in the United States and incorporated by others into products sold in the United States, such as the Lenovo Chromebook.

COUNT IV
(Infringement of the ’025 Patent)

55. Paragraphs 1 through 13 are incorporated by reference as if fully set forth herein.

56. Deepwell has not licensed or otherwise authorized MediaTek to make, use, offer for sale, sell, or import any products that embody the inventions of the ’025 Patent.

57. Defendant has and continues to directly infringe the ’025 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States products that satisfy each and every limitation of one or more claims of the ’025 Patent. Upon information and belief, these products include all MediaTek SoCs with ARM cores, including at least the MT8186 SoC, which are sold in the United States and incorporated by others into products sold in the United States, such as the Lenovo Chromebook.

58. For example, Defendant has and continues to directly infringe at least claim 35 of the ’025 Patent by making, using, offering to sell, selling, and/or importing into the United States products that practice a method, comprising: operating logic circuits in power islands of an integrated circuit that are connected to one or more components external to the integrated circuit; and controlling passage of power to the different ones of the logic circuits by one or more power gating circuits in an I/O ring of the integrated circuit, wherein the one or more power gating circuits in the I/O ring include one or more power control transistors, wherein said controlling includes selective disconnection of power to the logic circuits, wherein the one or more power gating circuits are configured to perform a multiplex function including making available different voltage supply levels for different ones of the logic circuits of the power islands, and wherein control for the multiplex function originates from a processor.

59. The Accused Products practice a method of operating logic circuits in power islands of an integrated circuit that are connected to one or more components external to the integrated circuit. For example, upon information and belief, the MT8186 and the Lenovo Chromebook consists of logic circuits such as voltage and sensing circuit and other peripherals in the same area as that of power gating transistors (power island) connected to one or more external components.

60. The Accused Products further practice a method controlling passage of power to the different ones of the logic circuits by one or more power gating circuits in an I/O ring of the integrated circuit, wherein the one or more power gating circuits in the I/O ring include one or more power control transistors, wherein said controlling includes selective disconnection of power to the logic circuits, wherein the one or more power gating circuits are configured to perform a multiplex function including making available different voltage supply levels for different ones of the logic circuits of the power islands, and wherein control for the multiplex function originates from a processor. For example, upon information and belief, the MT8186 and the Lenovo Chromebook consists of logic circuits such as voltage and sensing circuit and other peripherals in the same area as that of power gating transistors (power island) where switchers have their different output voltage which they supply to their connected peripherals.

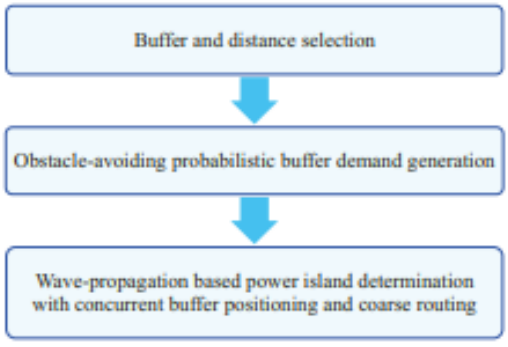


Fig. 5. Flow of wave-propagation based power island methodology.[18]

[18] https://ieeexplore.ieee.org/document/7372661

61. Defendant has and continues to indirectly infringe one or more claims of the '025 Patent by knowingly and intentionally inducing others, including MediaTek customers and end-users of the Accused Products and products that include the Accused Products, to directly infringe, either literally or under the doctrine of equivalents, by making, using, offering to sell, selling, and/or importing into the United States products that include infringing technology, such as the MT8186 and the Lenovo Chromebook.

62. Defendant, with knowledge that these products, or the use thereof, infringe the '025 Patent by no later than the date of this Complaint, knowingly and intentionally induced, and continues to knowingly and intentionally induce, direct infringement of the '025 Patent by providing these products to customers and/or distributors for use in an infringing manner in the United States including, but not limited to, products that include infringing technology, such as the MT8186 and the Lenovo Chromebook. For example, MediaTek's instruction manuals, websites, promotional materials, advertisements, and other information demonstrate to others, including customers, prospective customers, and distributors, how to use the Accused Products in an infringing manner. Upon information and belief, MediaTek is aware that the normal and customary use of the Accused Products by customers, distributors, and others would infringe the '025 Patent.

63. Defendant induced infringement by others, including customers and distributors, with the intent to cause infringing acts by others or, in the alternative, with the belief that there was a high probability that others, including end-users, infringe the '025 Patent, but while remaining willfully blind to the infringement.

64. Deepwell has suffered damages as a result of Defendant's direct and indirect infringement of the '025 Patent in an amount to be proved at trial.

65. Deepwell has suffered, and will continue to suffer, irreparable harm as a result of Defendant's infringement of the '025 Patent, for which there is no adequate remedy at law, unless Defendant's infringement is enjoined by this Court. Accordingly, Deepwell seeks a preliminary and permanent injunction enjoining MediaTek from making, using, importing, offering to sell, and/or selling the Accused Products, including, upon information and belief, all MediaTek SoCs with ARM cores, including at least the MT8186 SoC, which are sold in the United States and incorporated by others into products sold in the United States, such as the Lenovo Chromebook.

DEMAND FOR JURY TRIAL

Plaintiff hereby demands a jury for all issues so triable.

PRAYER FOR RELIEF

WHEREFORE, Deepwell prays for relief against Defendant as follows:

a. Entry of judgment declaring that Defendant has directly and/or indirectly infringed one or more claims of each of the Patents-in-Suit;

b. Entry of a preliminary injunction enjoining MediaTek from making, using, importing, offering to sell, and/or selling the Accused Products;

c. Entry of a permanent injunction enjoining MediaTek from making, using, importing, offering to sell, and/or selling the Accused Products;

d. An order awarding damages sufficient to compensate Deepwell for Defendant's infringement of the Patents-in-Suit, but in no event less than a reasonable royalty, including supplemental damages post-verdict, together with pre-judgment and post-judgment interest and costs;

e. Entry of judgment declaring that this case is exceptional and awarding Deepwell its costs and reasonable attorneys' fees under 35 U.S.C. § 285;

f. An accounting for acts of infringement;

g. Such other equitable relief which may be requested and to which the Plaintiff is entitled; and

h. Such other and further relief as the Court deems just and proper.

Dated: September 19, 2023

Respectfully submitted,

/s/ Vincent J. Rubino, III

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