IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
SHERMAN DIVISION

Bell Semiconductor, LLC **Plaintiff,** **v.** **Fortinet, Inc.** **Defendant.**	**Civil Action No. 4:23-cv-978** **JURY TRIAL DEMANDED**

COMPLAINT

Plaintiff Bell Semiconductor, LLC ("Bell Semic" or "Plaintiff") brings this Complaint against Defendant Fortinet, inc. ("Fortinet") for infringement of U.S. Patent Nos. 7,345,245 ("the '245 patent"); 8,049,340 ("the '340 patent"); and 8,288,269 ("the '269 patent") (collectively, the "Asserted Patents"). Plaintiff, on personal knowledge of its own acts, and on information and belief as to all others based on investigation, alleges as follows:

SUMMARY OF THE ACTION

1. This is a patent infringement suit relating to Fortinet's unauthorized and unlicensed use of the Asserted Patents. The semiconductor technologies claimed in the Asserted Patents are used by Fortinet in the production of one or more of its semiconductor chips and packages, including but not limited to the FortiSOC3 and the FortiASIC-CP9.

2. Bell Semiconductor brings this action to put a stop to Fortinet's unauthorized and unlicensed use of the inventions claimed in the Asserted Patents.

THE PARTIES

3. Plaintiff Bell Semic is a limited liability company organized under the laws of the State of Delaware with a place of business at One West Broad Street, Suite 901, Bethlehem, PA 18018.

4. Bell Semic stems from a long pedigree that began at Bell Labs. Bell Labs sprung out of the Bell System as a research and development laboratory, and eventually became known as one of America's greatest technology incubators. Bell Labs employees invented the transistor in 1947 in Murray Hill, New Jersey. It was widely considered one of the most important technological breakthroughs of the time, earning the inventors the Nobel Prize in Physics. Bell Labs made the first commercial transistors at a plant in Allentown, Pennsylvania. For decades, Bell Labs licensed its transistor patents to companies throughout the world, creating a technological boom that led to the use of transistors in the semiconductor devices prevalent in most electronic devices today.

5. Bell Semic, a successor to Bell Labs' pioneering efforts, owns over 1,900 worldwide patents and applications, approximately 1,500 of which are active United States patents. This patent portfolio of semiconductor–related inventions was developed over many years by some of the world's leading semiconductor companies, including Bell Labs, Lucent Technologies, Agere Systems, and LSI Logic and LSI Corporation ("LSI"). This portfolio reflects technology that underlies many important innovations in the development of semiconductors and integrated circuits for high–tech products, including smartphones, computers, wearables, digital signal processors, IoT devices, automobiles, broadband carrier access, switches, network processors, and wireless connectors.

6. The principals of Bell Semic all worked at Bell Labs' Allentown facility, and have continued the rich tradition of innovating, licensing, and helping the industry at large since those early days at Bell Labs. For example, Bell Semic's CTO was an LSI Fellow and Broadcom Fellow. He is known throughout the world as an innovator with more than 300 patents to his name, and he has a sterling reputation for helping semiconductor fabs improve their efficiency. Bell Semic's CEO took a brief hiatus from the semiconductor world to work with Nortel Networks in the telecom industry during its bankruptcy. His efforts saved the pensions of tens of thousands of Nortel retirees and employees. In addition, several Bell Semic executives previously served as engineers at many of these companies and were personally involved in creating the ideas claimed throughout Bell Semic's extensive patent portfolio.

7. On information and belief, Fortinet is a corporation organized and existing under the laws of Delaware with its principal place of business and headquarters at 899 Kifer Rd., Sunnyvale, CA 94086. Fortinet has a registered agent for service of process, Corporation Service Company (dba CSC - Lawyers Incorporating Service Company), located at 211 E. 7th Street, Suite 620, Austin, TX 78701-3218.

8. On information and belief, Fortinet develops, designs, and/or manufactures products in the United States, including in this District, that use the structures and/or methods of the Asserted Patents; and/or use structures and/or methods of the Asserted Patents in the United States, including in this District, to make products; and/or distribute, market, sells, or offers to sell in the United States and/or import products into the United States, including in this District, that were manufactured using the patented methods or include the patented structures. Additionally, Fortinet introduces those products into the stream of commerce knowing that they will be sold and/or used in this District and elsewhere in the United States.

JURISDICTION AND VENUE

9. This is an action for patent infringement arising under the Patent Laws of the United States, Title 35 of the United States Code. Accordingly, this Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

10. This Court has personal jurisdiction over Fortinet under the laws of the State of Texas, due at least to their substantial business in Texas and in this District. Fortinet has purposefully and voluntarily availed themselves of the privileges of conducting business in the United States, in the State of Texas, and in this District by continuously and systematically placing goods into the stream of commerce through an established distribution channel with the expectation that they will be purchased by consumers in this District. In the State of Texas and in this District, Fortinet, directly and/or through intermediaries: (i) performs at least a portion of the infringements alleged herein; (ii) develops, designs, and/or manufactures products according to claims of each Asserted Patent; (iii) distributes, markets, sells, or offers to sell products that embody the Asserted Patents; and/or (iv) imports products formed according to the processes/methodologies of the Asserted Patents.

11. On information and belief, venue is proper in this Court pursuant to 28 U.S.C. §§ 1391 and 1400 with respect to Fortinet because Fortinet has committed, and continues to commit, acts of infringement in this District and has a regular and established place of business in this District. For example, Fortinet maintains a regular and established place of business at 6111 W. Plano Pkwy, Plano TX 75093.

12. On information and belief, Fortinet currently employs more than 60 persons in the Eastern District of Texas and over 430 persons in or near the Eastern District of Texas throughout the Dallas-Fort Worth Metroplex, including many in positions that relate to the

Asserted Patents.[1] On information and belief, at least some of the personnel it employs in positions related to the Asserted Patents are in its Plano facility in this District.

U.S. PATENT NO. 7,345,245

13. Bell Semiconductor owns by assignment the entire right, title, and interest in the '245 patent, entitled "Robust High Density Substrate Design for Thermal Cycling Reliability," which issued on March 18, 2008.

14. The '245 patent issued to inventors Anand Govind, Zafer Kutlu, and Farshad Ghahghahi from United States Patent Application No. 10/681,554, filed October 8, 2003. A true and correct copy of the '245 patent is attached as Exhibit A.

15. Recent silicon technology advances have placed increased demand for high density signal routing on organic BGA substrates. Increased signal routing density in the substrate is obtained by using fine pitch vias through the core so that routing layers below the core can be efficiently utilized. The via pitch reduction requires the use of thin core substrates which are susceptible to warpage during thermal excursions. Typically, the regions are under the die corner are regions of stress concentration. Under cycled thermal excursions, cracks can initiate from the ball pad edges and spread into the layers above the ball pad layer.

16. The '245 patent is generally related to a semiconductor package for a die with improved thermal cycling reliability. To eliminate package failures and occurrences cracks in

[1]https://www.linkedin.com/search/results/people/?currentCompany=%5B%2262847008%22%2C%226460%22%5D&geoUrn=%5B%22100517351%22%5D&origin=FACETED_SEARCH&sid=T*C (LinkedIn results for current Fortinet employees in Plano TX) (last visited October 31, 2023);
https://www.linkedin.com/search/results/people/?currentCompany=%5B%2262847008%22%2C%226460%22%5D&geoUrn=%5B%22104194190%22%2C%2290000031%22%5D&origin=FACETED_SEARCH&sid=FL6 (LinkedIn results for current Fortinet employees in Dallas, TX and the Dallas-Fort Worth Metroplex) (last visited October 31, 2023)

signal traces, the ’245 patent teaches routing of signals away from the high stress area associated with the ball pads and the corner of the die.

17. The ’245 patent contains 2 independent claims and 12 total claims, covering an integrated circuit substrate. Claim 1 of the ’245 patent reads:

> 1. A semi-conductor package comprising:
>
> a top layer having a die mounted thereon, said die having a corner; and
>
> a plurality of layers under the top layer, said plurality of layers comprising a bottom routing layer having signal traces thereon, and a ball pad layer under the bottom routing layer, said ball pad layer having a plurality of ball pads, wherein none of the signal traces of the bottom routing layer are located over ball pads of the ball pad layer which are disposed in an area within two ball pad pitches of the corner of the die.

18. This claim, as a whole, provides significant benefits and improvements to the function of the semiconductor device, e.g., improving system reliability by avoiding functional failures from cracks in the signal traces caused by thermal cycling stresses under the die corner.

U.S. PATENT NO. 8,049,340

19. Bell Semiconductor owns by assignment the entire right, title, and interest in the ’340 patent, entitled “Device for Avoiding Parasitic Capacitance in an Integrated Circuit Package,” which issued on November 1, 2011.

20. The ’340 patent issued to inventors Jeffrey Hall, Shawn Nikoukary, Amar Amin, and Michael Jenkins from United States Patent Application No. 11/277,188, filed March 22, 2006. A true and correct copy of the ’340 patent is attached as Exhibit B.

21. The ’340 patent is directed to solving the problem of signal deterioration in integrated circuits such as a serializer/deserializer. At high frequencies, “the parasitic capacitance between transmit (Tx) and receive (Rx) contact pads in the contact pad layer and nearby metal

layers of the integrated circuit package may result in a deterioration of the signal waveform and a correspondingly reduced circuit performance." Ex. B at 2:52–60.

22. Parasitic capacitance results when parts in an electronic circuit are proximate to one another, potentially leading to interference with the input or output to a device. Reducing parasitic capacitance has become increasingly necessary as integrated circuit devices, particularly high-speed devices, have included more external connections.

23. The '340 patent identifies the shortcomings of the prior art. More specifically, the specifications describe that "metal layers that have a relatively large metal area may produce significant parasitic capacitance." Parasitic capacitance between, e.g., the ball pad and the routing metal layer or between the underlying ball pad and the ground return metal layer can produce "distortion of the switching waveform of high-frequency signals used, for example, in serializing/deserializing devices (SERDES). As a result, the maximum operating frequency that may be used in the integrated circuit is disadvantageously limited . . . ." *Id.* at 3:21–25.

24. To reduce parasitic capacitance in the multi-layer packages, the '340 patent teaches the use of cutouts over the electrical contacts in electrically conductive layers to substantially avoid overlap between the electrical contacts and metal in the electrically conductive layers.

25. The '340 patent contains 3 independent claims and 19 total claims, covering an integrated circuit substrate. Claim 1 reads:

> 1. An integrated circuit package substrate comprising:
>
> a first and a second electrically conductive layer separated from each other by an electrically insulating layer with no intermediate conductive layer therebetween;
>
> a plurality of rows of contact pads formed in the first electrically conductive layer for making a direct connection between the integrated circuit package substrate and a printed circuit board; and

> a plurality of cutouts formed in the second electrically conductive layer for reducing parasitic capacitance between the second electrically conductive layer and the first electrically conductive layer,
>
> wherein each cutout encloses an electrically insulating area within the second electrically conductive layer, and
>
> wherein each electrically insulating area completely overlaps a corresponding one of the contact pads formed in the first electrically conductive layer such that there is substantially no overlap of the rows of contact pads with metal in the second electrically conductive layer.

26. Claim 2 reads:

> 2. The integrated circuit package substrate of claim 1 further comprising transmit and receive rows of ball pads as the contact pads operable with the second electrically conductive layer for converting a serial data stream to or from a parallel data stream, the second electrically conductive layer being a routing layer including routing traces, the cutouts being arranged in rows corresponding to the rows of ball pads.

27. Claim 2, as a whole, provides significant benefits and improvements to the function of the semiconductor device, e.g., increasing the maximum operating frequency that may be used in integrated circuits relative to prior art designs.

U.S. PATENT NO. 8,288,269

28. Bell Semiconductor owns by assignment the entire right, title, and interest in the ’269 patent, entitled “Methods for Avoiding Parasitic Capacitance in an Integrated Circuit Package,” which issued on October 16, 2012.

29. The ’269 patent issued to inventors Jeffrey Hall, Shawn Nikoukary, Amar Amin, and Michael Jenkins from United States Patent Application No. 13/252,632, filed October 4, 2011. A true and correct copy of the ’269 patent is attached as Exhibit C.

30. The ’269 patent is related to and shares an identical specification with the ’340 patent. Where the ’340 patent claims apparatuses for minimizing parasitic capacitance, the ’269

patent claims methods for directed to the same general problem. More particularly, in order to reduce parasitic capacitance in the multi-layer packages, the ’269 patent teaches the use of cutouts over the electrical contacts in electrically conductive layers to eliminate substantial overlap between the electrical contacts and metal in the electrically conductive layers.

31. The ’269 patent contains 2 independent claims and 20 total claims, covering an integrated circuit substrate. Claim 1 reads:

> 1. A method, comprising steps of:
>
> forming a first electrically conductive layer including a plurality of rows of contact pads;
>
> forming an electrically insulating layer on the first electrically conductive layer; and
>
> forming a second electrically conductive layer over the electrically insulating layer such that there is no intermediate conductive layer between the first and second electrically conductive layers, the second electrically conductive layer comprising metal and a plurality of cutouts wherein each cutout encloses an electrically insulating area within the second electrically conductive layer and wherein each electrically insulating area completely overlaps a corresponding one of the contact pads such that there is substantially no overlap of the rows of contact pads with metal in the second electrically conductive layer.

32. Claim 2 reads:

> 2. The method of claim 1, further comprising:
>
> forming the contact pads as transmit and receive rows of contact pads;
>
> forming the second electrically conductive layer as a routing layer including routing traces such that the contact pads are operable with the second electrically conductive layer for converting a serial data stream to or from a parallel data stream; and
>
> forming the cutouts in rows corresponding to and aligned with the rows of contact pads.

33. Similar to the ’340 patent, this claim 2, as a whole, provides significant benefits and improvements to the function of the semiconductor device, e.g., increasing the maximum operating frequency that may be used in integrated circuits relative to prior art designs.

COUNT I – INFRINGEMENT OF U.S. PATENT NO. 7,345,245 (FORTINET)

34. Bell Semiconductor re-alleges and incorporates by reference the allegations of the foregoing paragraphs as if fully set forth herein.

35. The ’245 patent is valid and enforceable under the United States patent Laws.

36. Bell Semiconductor owns, by assignment, all right, title, and interest in and to the ’245 patent, including the right to collect for past damages.

37. On information and belief, Fortinet has infringed and continues to directly infringe, either literally or under the doctrine of equivalents, pursuant to 35 U.S.C. § 271(a), one or more claims of the ’245 patent by making, using, offering to sell, or selling within the United States, or importing into the United States, one or more semiconductor devices, including as one example the FortiASIC-CP9, in the United States.

38. A claim chart demonstrating Fortinet’s infringement of the ’245 patent is attached hereto as Exhibit D.

39. Fortinet’s Accused Products infringe and continue to infringe one or more claims of the ’245 patent during the pendency of the ’245 patent.

40. Fortinet’s infringement of the ’245 patent was, and continues to be, done with knowledge of the ’245 patent and with knowledge of Bell Semiconductor’s contention that Fortinet is infringing the ’245 patent. On or about June 30, 2023, a representative of Bell Semiconductor provided actual notice to Fortinet of the ’245 patent and its infringement by the

FortiASIC-CP9. Fortinet's infringement of the '245 patent is thus willful and deliberate, entitling Bell Semiconductor to enhanced damages and attorneys' fees.

41. Fortinet's infringement of the '245 patent is exceptional and entitles Bell Semiconductor to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

42. Bell Semiconductor has been damaged by Fortinet's infringement of the '245 patent and will continue to be damaged unless Fortinet is enjoined by this Court. Bell Semiconductor has suffered and continues to suffer irreparable injury for which there is no adequate remedy at law. The balance of hardships favors Bell Semiconductor, and public interest is not disserved by an injunction.

43. Bell Semiconductor is entitled to recover from Fortinet all damages that Bell Semiconductor has sustained as a result of Fortinet's infringement of the '245 patent, including without limitation and/or not less than a reasonable royalty.

COUNT II – INFRINGEMENT OF U.S. PATENT NO. 8,049,340 (FORTINET)

44. Bell Semiconductor re-alleges and incorporates by reference the allegations of the foregoing paragraphs as if fully set forth herein.

45. The '340 patent is valid and enforceable under the United States patent laws.

46. Bell Semiconductor owns, by assignment, all right, title, and interest in and to the '340 patent, including the right to collect for past damages.

47. On information and belief, Fortinet has and continues to directly infringe, either literally or under the doctrine of equivalents, pursuant to 35 U.S.C. § 271(a) one or more claims of the '340 patent by making, using, offering to sell, and/or selling within the United States, or importing into the United States, one or more semiconductor devices, including as one example

the or importing into the United States, one or more semiconductor devices, including as one example the FortiSOC3, and products containing the FortiSOC3 ("Hall '340 Accused Products").

48. An exemplary claim chart demonstrating Fortinet's infringement of the '340 patent by the FortiSOC3 is attached hereto as Exhibit E.

49. Fortinet's Hall '340 Accused Products infringed and continue to infringe one or more claims of the '340 patent during the pendency of the '340 patent.

50. Fortinet's infringement of the '340 patent was, and continues to be, done with knowledge of the '340 patent and with knowledge of Bell Semiconductor's contention that Fortinet is infringing the '340 patent. On June 30, 2023, a representative of Bell Semiconductor provided actual notice to Fortinet of the '340 patent and its infringement by the FortiSOC3. Fortinet's infringement of the '340 patent is thus willful and deliberate, entitling Bell Semiconductor to enhanced damages and attorneys' fees.

51. Fortinet's infringement of the '340 patent is exceptional and entitles Bell Semiconductor to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

52. Bell Semiconductor has been damaged by Fortinet's infringement of the '340 patent and will continue to be damaged unless Fortinet is enjoined by this Court. Bell Semiconductor has suffered and continues to suffer irreparable injury for which there is no adequate remedy at law. The balance of hardships favors Bell Semiconductor, and public interest is not disserved by an injunction.

53. Bell Semiconductor is entitled to recover from Fortinet all damages that Bell Semiconductor has sustained as a result of Fortinet's infringement of the '340 patent, including without limitation and/or not less than a reasonable royalty.

COUNT III – INFRINGEMENT OF U.S. PATENT NO. 8,288,269 (FORTINET)

54. Bell Semiconductor re-alleges and incorporates by reference the allegations of the foregoing paragraphs as if fully set forth herein.

55. The '269 patent is valid and enforceable under the United States patent laws.

56. Bell Semiconductor owns, by assignment, all right, title, and interest in and to the '269 patent, including the right to collect for past damages.

57. On information and belief, Fortinet has infringed and continues to directly infringe, either literally or under the doctrine of equivalents, pursuant to 35 U.S.C. § 271(g), one or more claims of the '269 patent by using, offering to sell, and/or selling within the United States, and/or importing into the United States, one or more one or more semiconductor devices, including as one example the FortiSOC3, manufactured pursuant to at least one of the methods claimed in the '269 patent ("Hall '269 Accused Products").

58. On information and belief, the Hall '269 Accused Products were made by at least one process claimed in the '269 patent.

59. The Hall '269 Accused Products are not materially changed by subsequent processes.

60. The Hall '269 Accused Products are neither trivial nor non-essential components of the downstream products into which they are incorporated. Rather, the Hall '269 Accused Products are essential for the functioning of such downstream products, and, on information and

belief, they are non-trivial components thereof because their performance characteristics enable the high performance of the downstream products that drives market demand.

61. An exemplary claim chart demonstrating Fortinet's infringement of the '269 patent by the FortiSOC3 is attached hereto as Exhibit F.

62. Fortinet's Hall '269 Accused Products infringe and continue to infringe one or more claims of the '269 patent during the pendency of the '269 patent.

63. Fortinet's infringement of the '269 patent was, and continues to be, done with knowledge of the '269 patent and with knowledge of Bell Semiconductor's contention that Fortinet is infringing the '269 patent. On June 30, 2023, a representative of Bell Semiconductor provided actual notice to Fortinet of the '269 patent and its infringement by the FortiSOC3. Fortinet's infringement of the '269 patent is thus willful and deliberate, entitling Bell Semiconductor to enhanced damages and attorneys' fees.

64. Fortinet's infringement of the '269 patent is exceptional and entitles Bell Semiconductor to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

65. Bell Semiconductor has been damaged by Fortinet's infringement of the '269 patent and will continue to be damaged unless Fortinet is enjoined by this Court. Bell Semiconductor has suffered and continues to suffer irreparable injury for which there is no adequate remedy at law. The balance of hardships favors Bell Semiconductor, and the public interest is not disserved by an injunction.

66. Bell Semiconductor is entitled to recover from Fortinet all damages that Bell Semiconductor has sustained as a result of Fortinet's infringement of the '269 patent, including without limitation and/or not less than a reasonable royalty.

PRAYER FOR RELIEF

WHEREFORE, Bell Semiconductor respectfully requests that this Court enter judgment in its favor as follows and award Bell Semiconductor the following relief:

a. a judgment declaring that Defendant has infringed one or more claims of each of the Asserted Patents in this litigation pursuant to 35 U.S.C. § 271, *et seq.*;

b. an award of damages adequate to compensate Bell Semiconductor for infringement of each of the Asserted Patents by Defendant, in an amount to be proven at trial, including supplemental post-verdict damages until such time as Defendant ceases its infringing conduct;

c. a permanent injunction, pursuant to 35 U.S.C. § 283, prohibiting Defendant and its officers, directors, employees, agents, consultants, contractors, suppliers, distributors, all affiliated entities, and all others acting in privity with Defendant, from committing further acts of infringement;

d. a judgment requiring Defendant to make an accounting of damages resulting from its infringement of the respective Asserted Patents;

e. enhanced damages for willful infringement;

f. the costs of this action, as well as attorneys' fees as provided by 35 U.S.C. § 285;

g. pre-judgment and post-judgment interest at the maximum amount permitted by law;

h. all other relief, in law or equity, to which Bell Semiconductor is entitled.

DEMAND FOR JURY TRIAL

Plaintiff hereby demands a jury trial for all issues so triable.

Dated: October 31, 2023

/s/ Clifford Chad Henson
C. Chad Henson (TX Bar No. 24087711)
DEVLIN LAW FIRM LLC
1411 North Trail Drive
Carrollton, TX 75006
Telephone: (302) 449–9010
Facsimile: (302) 353–4251
chenson@devlinlawfirm.com

Attorney for Plaintiff Bell Semiconductor, LLC