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Attorneys for Plaintiff BiTMICRO LLC

IN THE UNITED STATES DISTRICT COURT
FOR THE CENTRAL DISTRICT OF CALIFORNIA

BiTMICRO LLC, Plaintiff, v. WESTERN DIGITAL CORPORATION and WESTERN DIGITAL TECHNOLOGIES, INC., Defendants.	Civil Action No.: 8:24-cv-1903 **JURY TRIAL DEMANDED**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff BiTMICRO LLC ("Plaintiff" or "BiTMICRO"), through its attorneys, for its Complaint against Western Digital Corporation and Western Digital Technologies, Inc. (collectively, "Defendants" or "Western Digital"), demands a trial by jury and alleges as follows:

FACTUAL INTRODUCTION

1. The novel inventions disclosed in the Asserted Patents in this matter were invented by BiTMICRO Networks, Inc. ("BNI"). BNI was founded in 1995 and was a leader in enterprise storage for mission-critical computing, particularly for military applications. BNI's storage devices are best known for exceeding the extreme performance and data integrity required for enterprise, industrial, and military environments.

2. BNI made critical advances in the solid-state drive ("SSD") and integrated circuit technology that is embodied in the Asserted Patents. The Asserted Patents in this case are the result of the work of BNI engineers and developers, spanning a period of over a decade.

3. Innovation was one of the keys to the success at BNI. The company was involved with research and development projects in the SSD industry for about 20 years, over which time it accumulated over 50 U.S. patents, all of which are now owned by BiTMICRO.

THE PARTIES

4. BiTMICRO is the current owner and assignee of the Asserted Patents and holds all rights necessary to bring this action.

5. BiTMICRO is a Delaware limited liability company with its principal place of business located at 11921 Freedom Drive, Suite 550, Reston, Virginia 20190.

6. Defendant Western Digital Corporation is a Delaware Corporation with offices in this District at 3355 Michelson Drive, Suite 100, Irvine, California 92612.

Western Digital Corporation is registered with the California Secretary of State to do business in California and can be served through its registered agent, CSC - Lawyers Incorporating Service, 2710 Gateway Oaks Drive, Sacramento, California 95833.

7. Defendant Western Digital Technologies, Inc. is a subsidiary of Western Digital Corporation. Western Digital Technologies, Inc. is a Delaware Corporation with offices in this District at 3355 Michelson Drive, Suite 100, Irvine, California 92612. Western Digital Technologies, Inc. is registered with the California Secretary of State to do business in California and can be served through its registered agent, CSC - Lawyers Incorporating Service, 2710 Gateway Oaks Drive, Sacramento, California 95833.

JURISDICTION AND VENUE

8. This action arises under the patent laws of the United States, Title 35 of the United States Code. Subject matter jurisdiction is proper in this Court pursuant to 28 U.S.C. §§ 1331 and 1338(a).

9. This Court has personal jurisdiction over Western Digital because, *inter alia*, Western Digital (1) has substantial, continuous, and systematic contacts with this State and this judicial district; (2) owns, manages, and operate facilities in this State and this judicial district; (3) enjoys substantial income from its operations and sales in this State and this judicial district; (4) employs residents of this State and judicial district, and employs them in this State and this judicial district; and (5) solicits business and markets products, systems and/or services in this State and judicial district including, without limitation, those related to the infringing accused products.

10. This Court also has personal jurisdiction over Western Digital because it has committed and continues to commit acts of direct infringement in this judicial district in violation of at least 35 U.S.C. § 271(a). In particular, Western Digital has made, used, offered to sell, and/or sold the accused products in this judicial district, including through retail stores and online.

11. Venue is proper in this District pursuant to 28 U.S.C. §1319(b)-(c) and §1400(b), at least because of Western Digital's physical presence in this judicial district and because Western Digital conducts business in this judicial district, and, because Western Digital, directly or through its agents, has committed acts within this judicial district giving rise to this action, and/or has committed acts of patent infringement within this judicial district giving rise to this action.

FACTUAL ALLEGATIONS

BiTMICRO Patents

12. The BiTMICRO inventions contained in the Asserted Patents relate to groundbreaking improvements to memory controllers, mapping tables for memory devices, NVMe over Fabrics technologies, and data security as will be further described below.

U.S. Patent No. 9,135,190

13. On September 15, 2015, the U.S. Patent and Trademark Office duly and lawfully issued United States Patent No. 9,135,190 ("the '190 Patent"), entitled "Multi-profile memory controller for computing devices." A true and correct copy of the '190 Patent is attached hereto as **Exhibit A**.

14. BiTMICRO is the owner and assignee of all right, title, and interest in and to the '190 Patent, including the right to assert all causes of action arising under said patent and the right to any remedies for infringement of it.

15. The '190 Patent describes, among other things, a multi-profile memory controller for computing devices. Specifically, the '190 Patent describes a memory controller that can operate with memory locations, memory devices, or both which are associated with different memory attributes, different attribute qualifiers, or the like. For example, a non-volatile memory storage device may be portioned to allow a memory controller to treat a portion of the memory device as a temporary cache memory to store data prior to writing the data to a permanent storage location. This eliminates the need for a separate memory cache, often composed of volatile

memory. This capability has the additional advantage of maintaining the temporary data in the non-volatile cache partition in the event of an unexpected power loss.

16. Prior to the invention of the '190 Patent, memory controllers were designed to operate with memory locations and memory devices that all shared the same set of memory device characteristics, such as block size. Due to this limitation, there was no way of varying how a memory controller performed read and write operations on different memory locations or memory devices. The '190 Patent overcame this limitation by disclosing a novel multi-profile memory controller with the ability to operate differently with memory locations and memory devices based on differences between the attributes of particular memory locations and memory devices. *See* Ex. A, at 1:20-60.

17. As described in the '190 Patent, a memory store includes multiple addressable memory locations, and each location is associated with a set of memory attributes, which can include, for example, the type of memory device in which the memory location is located, the data size used by the memory device, or the memory protocol of the device. *See* Ex. A, at 2:63-3:13. These attributes are organized into device profiles that can be used by a memory controller connected to the memory store to determine how memory transactions are to be performed with each memory location. *See* Ex. A, at 3:14-4:25. By analyzing the requirements of the requested memory transaction and comparing those requirements to the device profiles, the memory controller selects the appropriate memory location for the memory transaction. The criteria used by the controller to select the optimal memory location for the memory transaction based on the stored attributes within the device profiles can be programmed in any number of ways. *See* Ex. A, at 7:60-9:48.

18. The novel features of the invention are recited in the claims. For example, claim 59 of the '190 Patent recites:

A memory controller comprising:

> an interface controller coupled to a memory device interface and an input/output (IO) device interface;
>
> a memory store;
>
> wherein the memory device interface is directly coupled to the memory store;
>
> said interface controller disposed to perform a memory transaction by addressing a first memory location in the memory store,
>
> said first memory location and a second memory location respectively associated with a first device profile and a second device profile;
>
> wherein said first device profile is optimal for a data type subject to the memory transaction, wherein said data type comprises one of a random data type or a sequential data type;
>
> said interface controller identifies command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device;
>
> said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles;
>
> said interface controller obtaining the first set of attributes after identifying the command details; and said addressing of said first memory location includes using said attributes from said first device profile;
>
> and said addressing of said first memory location includes selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.

Ex. A at 18:34-65. Claim 59 of the '190 Patent describes claim elements individually or as an ordered combination, that were non-routine and unconventional as of the priority date and an improvement over prior art, as it provided a memory controller

(not previously available) with an interface controller capable of performing memory transactions with different transfer sizes on different memory locations based on attributes associated with the different memory locations as defined in differing device profiles for those memory locations. *See* Ex. A at Abstract, 1:20-60, 2:41-62).

U.S. Patent No. 8,010,740

19. On August 30, 2011, the U.S. Patent and Trademark Office duly and lawfully issued United States Patent No. 8,010,740 ("the '740 Patent"), entitled "Optimizing memory operations in an electronic storage device." A true and correct copy of the '740 Patent is attached hereto as **Exhibit B**.

20. BiTMICRO is the owner and assignee of all right, title, and interest in and to the '740 Patent, including the right to assert all causes of action arising under said patent and the right to any remedies for infringement of it.

21. The '740 Patent describes, among other things, a mapping table for optimizing memory operations in an electronic storage device. Prior to the inventions in the '740 Patent, memory operations in solid state storage devices were subject to a number of inefficiencies. As described in the '740 specification, SSDs such as those that include NAND flash memory "suffer from write cycle limitations and to a certain degree, bad blocks. In addition, flash drives use block addressing rather than byte addressing, and these flash drives use block addresses that are usually much larger than the block address used by the host. Block addressing may impose an additional level of complexity and additional processing cycles when performing a write operation, and which in turn, may increase write operation latency. This additional level of complexity may include performing a read-modify-write transaction to complete the write operation." Ex. B at 1:42-53.

22. To address these issues and increase the speed and efficiency of memory operations in their products, SSD manufacturers tried solutions such as adding complex algorithms to handle the management of memory operations and adding more powerful processing devices to run these complex algorithms. *See id.* at 1:54-

2:10. These solutions, however, increased both the cost and design complexity of the SSDs. *See id.*

23. The '740 Patent overcame this problem by providing a solution that optimizes memory operations in a solid-state storage device while minimizing the amount of additional cost and complexity to the design of the device. *See id.* at 2:11-14. The '740 Patent achieves this through an improved mapping table that "increas[es] the likelihood that, in response to an I/O transaction initiated by a host, the operational load imposed on the storage device by these memory operations will be optimally distributed across different storage device resources, such as by interleaving or parallel memory operations, reducing memory operation latency, increasing operational device efficiency, or both." *Id.* at 2:14-21; *see also id.* at 3:12-31. For example, the '740 Patent describes a mapping table that includes a set of logical fields that represent a plurality of logical block address (LBA) sets. The mapping table also includes a set of physical block address (PBA) fields that represent a set of PBAs and access parameters for the PBAs, as well as information that associates the LBA sets with the PBA sets in a highly efficient manner. The mapping table enables the storage device to perform optimized memory operations on memory locations based on the information in the table regarding the relationship between the LBA and PBA sets and the access parameters. *See id.* at 2:27-4.

24. The novel features of the '740 inventions are recited in the claims. For example, claim 1 of the '740 Patent recites:

> A mapping table for optimizing memory operations performed by an electronic storage device in response to receiving an I/O transaction request initiated by a host, said mapping table comprising:
>
> a set of logical fields, including a first logical field and a second logical field, and said logical fields respectively disposed for representing a plurality of LBA sets, including said first logical field disposed for representing a first LBA set and said second logical field disposed for

> representing a second LBA set, said first and second LBA sets each representing a set of consecutive LBAs;
>
> a set of PBA fields, including a first PBA field and a second PBA field, said set of PBA fields respectively disposed for representing a set of PBAs, including a first PBA disposed for representing a first set of access parameters and a second PBA disposed for representing a second set of access parameters, said PBAs each associated with a physical memory location in a memory store, said set of logical fields and said set of PBA fields disposed to associate said first and second LBA sets with said first and second PBAs;
>
> and wherein, in response to receiving the I/O transaction request, said mapping table causes the electronic storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first and second LBA sets.

Ex. B at 9:64-10:24. Claim 1 of the '740 Patent describes claim elements individually or as an ordered combination, that were non-routine and unconventional as of the priority date and an improvement over prior art, as it provided a mapping table (not previously available) that enables optimized memory operations in an electronic storage device through information stored in a mapping table regarding logical fields, PBA fields, access parameters, and relationships between LBA and PBA sets. *See id.* at Abstract, 2:27-49.

U.S. Patent No. 9,875,205

25. On January 23, 2018, the U.S. Patent and Trademark Office duly and lawfully issued United States Patent No. 9,875,205 ("the '205 Patent"), entitled "Network of memory systems." A true and correct copy of the '205 Patent is attached hereto as **Exhibit C**.

26. BiTMICRO is the owner and assignee of all right, title, and interest in and to the '205 Patent, including the right to assert all causes of action arising under said patent and the right to any remedies for infringement of it.

27. The ’205 Patent describes, among other things, systems and methods enabling a large network of memory systems comprising a plurality of system controllers and flash memory modules. *See* Ex. C at Abstract. Specifically, the ’205 Patent describes a plurality of flash memory modules interconnected with other flash memory modules and to at least one system controller via a point-to-point communication bus topology. *Id.*

28. Prior to the inventions in the ’205 Patent, computing systems utilized redundancy to increase the reliability of multi-chip memory systems in which two or more controllers are provided in the system controller to serve as redundant components when failure occurs – if one controller fails, the system can still survive with another controller taking the role of the failed controller. *Id*. at 1:50-58. One disadvantage of the prior systems, however, is that in most multi-chip applications, data distribution from and to the memory chips that may reside on a module or on an adjacent memory board can become one of the major bottlenecks in high-performance system implementation. *Id*. at 1:44-49. In addition, prior to the inventions of the ’205 Patent, computing systems did not provide for a large memory system with multi-chip memory controllers and multiple flash memory modules to permit the reliability of operation possible with the distribution of flash devices/chips/die into multiple memory chips. *Id*. at 2:27-34.

29. The ’205 Patent overcame these various limitations by disclosing novel systems and methods for providing a large memory system with multi-chip memory controllers and multiple flash memory modules to permit the reliability of operation possible with the distribution of flash devices/chips/die into multiple memory chips. *Id*. at 2:27-34. These systems and methods allow the computing system to enhance redundancy – enabling the use of flash devices that function despite failure in any system controller or flash memory module. *Id*. at 2:35-38. In addition, these systems and methods provide an interconnect strategy between system controllers and flash array modules to enhance throughput and flexibility of data access. *Id*. at 2:40-43.

30. The novel features of the inventions of the '205 Patent are recited in the claims. For example, claim 1 of the '205 Patent recites:

> 1. An apparatus comprising:
>
> a communication bus interface;
>
> a flash memory module coupled to the communication bus interface via a communication bus; and
>
> a system controller coupled to the communication bus interface via an external communication bus; and
>
> wherein the system controller performs a memory transaction via the communication bus interface to the flash memory module.

Ex. C at 19:28-37. Claim 1 of the '205 Patent describes claim elements individually or as an ordered combination, that were non-routine and unconventional as of the priority date and an improvement over prior art, as it uses a plurality of flash memory modules interconnected with other flash memory modules and to at least one system controller via a point-to-point communication bus topology. *See* Ex. C at Abstract, 2:27-43.

U.S. Patent No. 7,716,389

31. On May 11, 2010, the U.S. Patent and Trademark Office duly and lawfully issued United States Patent No. 7,716,389 ("the '389 Patent"), entitled "Direct memory access controller with encryption and decryption for non-blocking high bandwidth I/O transactions." A true and correct copy of the '389 Patent is attached hereto as **Exhibit D**.

32. BiTMICRO is the owner and assignee of all right, title, and interest in and to the '389 Patent, including the right to assert all causes of action arising under said patent and the right to any remedies for infringement of it.

33. The '389 Patent describes, among other things, systems and methods

for enhancing direct memory access (DMA) operations by performing multiple encrypt and decrypt operations simultaneously using a data processing core. *See* Ex. D at Abstract. Specifically, the '389 Patent describes an architecture to provide secure and fast data transfers between I/O devices and the storage controller by performing multiple encrypt and decrypt operations simultaneously to service multiple transfer requests without a negative impact on the speed of transfer and processing. *Id*. Through the use of the systems and methods described by the '389 Patent, enhanced DMA operations between multiple I/O devices and a storage controller are accomplished by adding a data processing core and utilizing a multi-channel architecture that allows multiple requests to be serviced simultaneously. *Id*.

34. Prior to the inventions in the '389 Patent, computing systems did not include data processing cores directed, *e.g.*, to computationally intensive tasks such as encryption and decryption, especially not ones that designed to operate in tandem with direct memory access controllers (DMACs). One of the disadvantages of such systems was that they required several memory-to-memory transfers. *Id*. at 1:47-2:26.

35. The '389 Patent overcame these various limitations by disclosing novel systems and methods for enhanced DMA operations by using a data processing core for encrypting and decrypting data in conjunction with DMA requests. *Id*. at 2:27-61.

36. The novel features of the inventions of the '389 Patent are recited in the claims. For example, claim 19 of the '389 Patent recites:

> 19. A direct memory access controller for transferring data to or from a memory, and for encrypting or decrypting said data upon receiving a data processing request, the direct memory access controller comprising:
>
> a means for performing a DMA data transfer, said means for performing a DMA data transfer including at least one DMA engine configured for transferring data;
>
> a means for performing data processing coupled to said means for performing a DMA data transfer, said data processing includes

> encrypting or decrypting said data in response to a DPC hit signal by at least using a DPC channel to intercept said data, causing said data to be transferred to said means for performing data processing.

Ex. D at 10:50-63. Claim 19 of the '389 Patent describes claim elements individually or as an ordered combination, that were non-routine and unconventional as of the priority date and an improvement over prior art, as it uses a DMAC with an encryption and decryption processor that enables multiple simultaneous data transfer requests and eliminates the need for extra memory to memory transfers. *See* Ex. D at Abstract, 1:64-2:3, 2:27-35.

Western Digital's Use of the Patented Technology

37. Western Digital is a worldwide supplier of flash memory and solid-state drives (SSDs). Western Digital also supplies customers with flash memory and solid-state drives under the SanDisk and SanDisk Professional brands. Specific examples of Western Digital's infringing products made, sold, and/or offered for sale in the United States, and/or imported into the United States are discussed in further detail below.

38. Western Digital makes, uses, sells, and/or offers to sell in the United States, and/or imports into the United States (or has made, used, sold, offered for sale, and/or imported into the United States) SSDs with SLC caching capabilities, which infringe one or more claims of the '190 Patent. Such SSDs include, for example, at least Western Digital's WD Blue SN570, WD Blue SN580, WD Blue SA510 SATA M.2 2280, WD Green SATA M.2 2280, WD Blue SN5000, WD Red SN700, IX SN530, iNAND EU312, iNAND IX EM111, iNAND IX EM141, PC SA510, PC SA530, PC SN540, PC SN730, PC SN740, PC SN810, SanDisk Extreme M.2 NVMe, SanDisk Extreme M.2 NVMe PCIe Gen 4.0, SanDisk Ultra 3D, SanDisk SSD Plus, WD_BLACK SN750, WD_BLACK SN750 SE, WD_BLACK SN770, WD_BLACK SN770M, WD_BLACK SN850, WD_BLACK SN850X, WD_BLACK AN1500, AT EN610, PC SN5000S, and PC SN8000S Series SSDs.

39. Western Digital makes, uses, sells, and/or offers to sell in the United States, and/or imports into the United States (or has made, used, sold, offered for sale, and/or imported into the United States) Non-Volatile Memory Express (NVMe) SSDs, which infringe one or more claims of the '740 Patent. Such products include, for example, at least Western Digital's WD Blue SN550, WD Blue SN570, WD Blue SN580, PC SA510, PC SA530, PC SN540, PC SN730, PC SN740, PC SN810, CL SN520, WD_BLACK SN750, WD_BLACK SN750 SE, WD_BLACK SN770, WD_BLACK SN770M, WD_BLACK SN850, WD_BLACK SN850X, WD_BLACK SN850P, WD_BLACK AN1500, PC SN5000S, PC SN8000S, WD Green SN350, Ultrastar DC SN655, Ultrastar DC SN650, Ultrastar DC SN840, Ultrastar DC SN861, Ultrastar DC SA210, SanDisk Extreme M.2 NVMe, SanDisk Ultra 3D, WD Blue 3D NAND SATA, WD Red SN700, WD Red SA500, WD Blue SATA SSD M.2 2280, WD Red SA500 NAS SATA, WD Blue SN5000, IX SN530, iNAND EU312, iNAND EU552, iNAND IX EM132, iNAND IX EM122, iNAND IX EM141, AT EN610, and WD Gold Enterprise Class Series SSDs.

40. Western Digital makes, uses, sells, and/or offers to sell in the United States, and/or imports into the United States (or has made, used, sold, offered for sale, and/or imported into the United States) storage platform systems which infringe one or more claims of the '205 Patent. Such storage platform systems include, for example, at least Western Digital's OpenFlex Data24 Series NVMe-oF storage platforms.

41. Western Digital makes, uses, sells, and/or offers to sell in the United Sates, and/or imports into the United States (or has made, used, sold, offered for sale, and/or imported in the United States) SSDs with hardware encryption or self-encrypting drives, which infringe one or more claims of the '389 Patent. Such SSDs include, for example, at least Western Digital's Ultrastar DC SA210, SN540, SN640, SN650, SN655, SN840, SN861, SS530, SS540, ZN540 Series SSDs, and Transporter, the Western Digital CL SN720, AT EN610, PC SN5000S, PC

SN8000S, PC SA530 3D, PC SN730, PC SN740, PC SN810, WD_BLACK SN850X, and My Passport SSD (Blue) Series SSDs, and the SanDisk G-DRIVE, G-DRIVE ArmorLock, Extreme Portable, and Extreme PRO Portable Series SSDs.

Notice and Marking

42. As set forth below, Western Digital has been on constructive and/or actual notice of the Asserted Patents.

43. BiTMICRO has complied with 35 U.S.C. § 287 with respect to the Asserted Patents.

44. The previous owner of the Asserted Patents, BNI, also complied with 35 U.S.C. § 287, and thereby provided notice to the public, including but not limited to Western Digital, of the Asserted Patents. Specifically, to the extent BNI made, offered for sale, sold, or imported into the United States products covered by the Asserted Patents, BNI marked substantially all of such products with those patent numbers and provided an internet address at which BNI posted information associating the patented products with their corresponding patent numbers in compliance with 35 U.S.C. § 287.

45. For example, BNI's Ace Drive II products, which BNI contended were covered by the '190 Patent, were sold by BNI with a label affixed on the products listing the '190 Patent, as well as an internet address at which BNI posted a listing of additional patents it contended were practiced by that product, as shown below:

46. BNI's other products similarly included product labels identifying specific patents by number and/or an internet address at which BNI posted a listing of the patents it contended were associated with each product, including but not limited to the '190 and '740 Patents.

47. BNI's product documentation, which was provided to customers and available to the general public, also identified by number specific patents that BNI contended were practiced by the products and included an internet address at which BNI posted a listing of other patents it contended were associated with the products, pursuant to 35 U.S.C. § 287.

48. On information and belief, BNI has never made, offered for sale, sold, or imported into the United States any products that are covered by the '205 or '389 Patents. Thus, there were no BNI products that required marking of those patent numbers under 35 U.S.C. § 287.

49. BiTMICRO has not made, offered for sale, sold, or imported into the United States any products that are covered by any of the Asserted Patents. Thus, there are no BiTMICRO products that would require marking under 35 U.S.C. § 287.

50. The Asserted Patents have been widely cited by the industry and by the USPTO during the prosecution of other patents. For example, and as further described below, the '190 Patent has been cited in patents and/or applications by Western Digital, SanDisk, Micron, Huawei, Microsoft, and other well-known industry participants. The '740 Patent has been cited in patents and/or patent applications by Seagate and other well-known industry participants. And the '389 Patent has been cited in patents and/or applications by Intel, IBM, Samsung Electronics, STMicroelectronics, and other well-known industry participants.

51. Indeed, the Asserted Patents have been used by the USPTO as a basis to reject patent applications filed by well-known industry participants under 35 U.S.C. § 102 and/or § 103. For example, the '190 Patent has served as the basis for § 102/103 rejections at least three times, including against SanDisk. The '740 Patent has served as the basis for § 102/103 rejections at least four times, including against Seagate and Samsung.

52. In addition, as set forth in greater detail below, Western Digital has had actual notice of the '190 Patent since at least 2016 by virtue of Western Digital's prosecution of its own patent relating to SSD memory controllers. Western Digital has also had actual notice of the '190 Patent since at least 2018 by virtue of being served a subpoena in connection with a proceeding before the International Trade Commission, *In the Matter of Certain Solid State Storage Drives, Stacked Electronics Components, and Products Containing Same*, Inv. No. 337-TA-1097.

53. Finally, BNI approached Western Digital and/or SanDisk in or around 2016 with respect to its patents, which at that time included the '190, '740, and '389 Patents. Western Digital has had actual notice of the '190, '740, and '389 Patents since that date and has been at least willfully blind of its infringement thereof.

FIRST COUNT

(INFRINGEMENT OF U.S. PATENT NO. 9,135,190)

54. BiTMICRO incorporates by reference the allegations set forth in paragraphs 1-53 as though fully set forth herein.

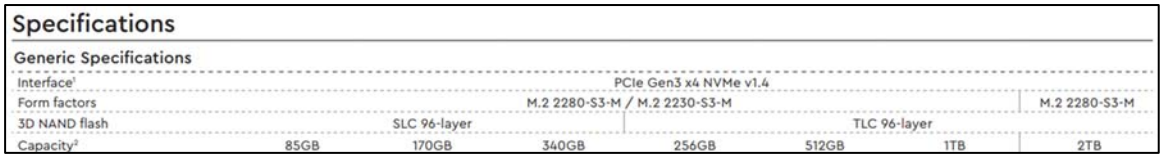
55. On information and belief, Western Digital has directly infringed and continues to directly infringe one or more claims of the '190 Patent, including at least claim 59 of the '190 Patent, in the state of California, in this judicial district, and elsewhere in the United States by, among other things, making, using, selling, offering for sale, and/or importing into the United States products that embody one or more of the inventions claimed in the '190 Patent, including but not limited to the above-identified SSDs with SLC caching, and all reasonably similar products ("the '190 Accused Products"), in violation of 35 U.S.C. § 271(a).

56. As an example, the Western Digital IX SN530 Industrial-Grade Series SSDs include "a memory controller." Specifically, the Western Digital IX SN530 Industrial-Grade Series SSDs includes a memory controller for handling read and write operations on the NAND memory cells on the drive. *See* Western Digital Product Brief, "Western Digital IX SN530 NVMe Industrial-Grade SSD",[1] at 1 ("A fully vertically integrated solid state drive, the IX SN530 is built with Western Digital's 96-layer 3D NAND technology, in-house controller and firmware development, internal validation and qualification, and extensive testing; making it idea for handling a wide variety of industrial and automotive use cases.").

57. The Western Digital IX SN530 Industrial-Grade Series SSDs include "an interface controller coupled to a memory device interface and an input/output (IO) device interface." For example, the Western Digital IX SN530 Industrial-Grade

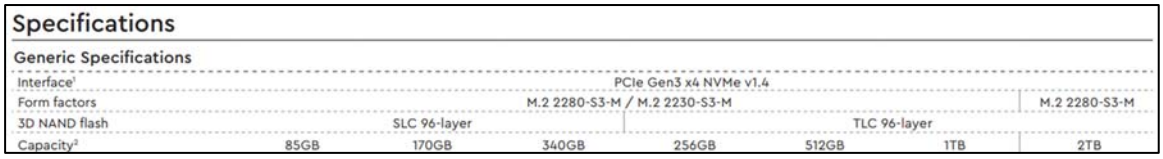
[1] Available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/ public/western-digital/product/embedded-flash/commercial-cl-nvme-ssd/product-brief-western-digital-ix-sn530-nvme-ssd.pdf.

Series SSDs include a Western Digital NVMe 1.4 compliant controller chip that serves as an interface controller:



Western Digital Product Brief, "Western Digital IX SN530 NVMe Industrial-Grade SSD"[2] at 2. Western Digital IX SN530 Industrial-Grade Series SSDs include a Western Digital controller and proprietary firmware. *See* Tom's Hardware, "Western Digital Gets Into Industrial-Grade M.2 SSDs With the IX SN530,"[3] ("The Western Digital IX SN530 is based on the company's own controller and firmware, as well as 96-layer TLC NAND memory that can work in TLC or SLC mode.").

58. The Western Digital controller chip is connected to at least one memory bus, which serves as a memory device interface. The controller chip is also connected to a PCIe interface, which serves as an input/output interface with a computing device:



Western Digital Product Brief, "Western Digital IX SN530 NVMe Industrial-Grade SSD"[4] at 2.

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[2] Available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/product/embedded-flash/commercial-cl-nvme-ssd/product-brief-western-digital-ix-sn530-nvme-ssd.pdf.

[3] Available at https://www.tomshardware.com/news/western-digital-gets-into-industrial-grade-m2-ssds-with-the-ix-sn530.

[4] Available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/product/embedded-flash/commercial-cl-nvme-ssd/product-brief-western-digital-ix-sn530-nvme-ssd.pdf.

59. The Western Digital IX SN530 Series SSDs include "a memory store." For example, the IX SN530 Series SSDs include 96-layer 3D TLC NAND memory, which constitutes a memory store. As advertised by Western Digital, "[a] fully vertically integrated solid state drive, the IX SN530 is built with Western Digital's 96-layer 3D NAND technology, in-house controller and firmware development. . ." *Id.* at 1.

60. In the Western Digital IX SN530 Series SSDs, "the memory device interface is directly coupled to the memory store." For example, the memory bus connected to the controller chip is directly coupled to the TLC NAND memory store, thereby enabling the controller to handle read and write operations to the memory store.

61. In the Western Digital IX SN530 Series SSDs, "said interface controller [is] disposed to perform a memory transaction by addressing a first memory location in the memory store." For example, in the Western Digital IX SN530 Series SSDs, a portion of the TLC NAND memory store is reserved to act as an SLC cache. Data can be written to the SLC cache at a faster rate than to other portions of the TLC NAND memory store. *Id.* at 2, ("Advanced Features: Functional: nCache 3.0 SLC tiered caching technology."); *see also* Western Digital Product Manual, "PC SN730 NVMe SSD for Generic OEM,"[5] at 11 ("The nCache 3.0 is a pool of X1 (SLC) blocks for sequential and random host operations. These X1 blocks are used as write cache to accumulate and consolidate all writes at high speed. The PC SN730 NVMe SSD utilize the nCache 3.0 tiered caching which further improves performance and power efficiently by introducing several enhancements as: Direct TLC (write) Access – improves sustain-write-access power efficiency and write throughput. Enhanced Evaluation Policy – improves the write-burst access speed. As mentioned above, the nCache 3.0 works in the background the flush them into the larger X3 (TLC) storage

[5] Available at https://downloads.sandisk.com/downloads/um/pcsn730-pm.pdf.

blocks and uses optimized write transaction sizes to maximize endurance. Once the SLC blocks are full the Drive will continue to program the TLC blocks directly, and will re-locate the data from the SLC to TLC on Idle times."). For write operations to the SLC cache, the controller chip performs a memory transaction by addressing a first memory location within the SLC cache.

62. In the Western Digital IX SN530 Series SSDs, "said first memory location and a second memory location [are] respectively associated with a first device profile and a second device profile." For example, a second memory location within the TLC NAND memory store is a TLC cell that is not a part of the SLC cache. The first memory location and second memory location are associated with a first device profile and a second device profile, respectively, that define how data is to be stored in those locations.

63. In the Western Digital IX SN530 Series SSDs, "said first device profile is optimal for a data type subject to the memory transaction, wherein said data type comprises one of a random data type or a sequential data type." *See* Western Digital Product Brief, "Western Digital IX SN530 NVMe Industrial-Grade SSD"[6] at 1-2 ("Further, by offering SLC configurations, the IX SN530 supports write-intensive applications, such as data recorder and data set management, saving the need to use multiple high-capacity TLC devices by delivering 9 times the TLC endurance and up to 5 times the TLC sustained write performance."); Western Digital Product Page, "Industrial NVMe SSD,"[7] ("Sequential Read speeds up to 2,400 MB/s and Write Speeds up to 1,950 MB/s.").

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[6] Available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/product/embedded-flash/commercial-cl-nvme-ssd/product-brief-western-digital-ix-sn530-nvme-ssd.pdf.

[7] Available at https://www.westerndigital.com/products/internal-drives/ix-sn530-nvme-ssd?sku=SDBPNPZ-256G-XI.

64. In the Western Digital IX SN530 Series SSDs, "said interface controller identifies command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device." For example, for memory transactions with the first memory device such as writing data to the SLC cache, the controller chip identifies command details for causing the memory transaction to be performed in the first memory device.

65. In the Western Digital IX SN530 Series SSDs, "said device profile represent[s] a first set of attributes of said first memory location, and said second device profile represent[s] a second set of attributes of said second memory location, and a difference exists between said first and second device profiles." For example, the first device profile (*e.g.*, the profile for the SLC cache) represents a first set of attributes (*e.g.*, data size, memory protocol, device type) associated with the first memory location (*e.g.*, a location within the SLC cache). The second device profile (*e.g.*, the profile for the non-cache portion of the TLC NAND memory store) represents a second set of attributes (*e.g.*, data size, memory protocol, device type) associated with the second memory location (*e.g.*, a location within the non-cache portion of the TLC NAND memory store). The first and second device profiles are different because the SLC cache has attributes associated with a write protocol of one bit per cell, whereas the non-cache portion of the TLC NAND memory store has attributes associated with a write protocol of three bits per cell.

66. In the Western Digital IX SN530 Series SSDs, "said interface controller obtain[s] the first set of attributes after identifying the command details; and said addressing of said first memory location includes using said attributes from said first device profile." For example, after identifying command details specifying that data is to be written to the SLC cache, the controller chip obtains the first set of attributes (*e.g.*, data size, memory protocol, device type) associated with the memory location in the SLC cache.

67. In the Western Digital IX SN530 Series SSDs, "said addressing of said first memory location includes selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes." *See* Western Digital Product Manual, "PC SN730 NVMe SSD for Generic OEM,"[8] at 11 ("The nCache 3.0 is a pool of X1 (SLC) blocks for sequential and random host operations. These X1 blocks are used as write cache to accumulate and consolidate all writes at high speed. The PC SN730 NVMe SSD utilize the nCache 3.0 tiered caching which further improves performance and power efficiently by introducing several enhancements as: Direct TLC (write) Access – improves sustain-write-access power efficiency and write throughput. Enhanced Evaluation Policy – improves the write-burst access speed. As mentioned above, the nCache 3.0 works in the background the flush them into the larger X3 (TLC) storage blocks and uses optimized write transaction sizes to maximize endurance. Once the SLC blocks are full the Drive will continue to program the TLC blocks directly, and will re-locate the data from the SLC to TLC on Idle times."). Thus, for example, after receiving a write transaction command, the controller chip obtains the attributes of the SLC cache profile and determines whether there is sufficient capacity within the SLC cache to write the data to the cache. The controller will select a transfer size to the SLC cache based on an analysis of the size of the data to be written, the remaining memory capacity within the SLC cache, and the attributes of the SLC cache profile.

68. All of the '190 Accused Products infringe the '190 Patent, including at least claim 59, in the same or similar manner as the IX SN530 Series SSDs.

69. By making, using, offering for sale, and/or selling products in the United States and/or importing products into the United States, including but not limited to the '190 Accused Products, Western Digital has injured BiTMICRO and is liable to

[8] Available at https://downloads.sandisk.com/downloads/um/pcsn730-pm.pdf.

BiTMICRO for directly infringing one or more claims of the '190 Patent, including without limitation claim 59 pursuant to 35 U.S.C. § 271(a).

70. On information and belief, Western Digital has had knowledge of the '190 Patent since at least 2016 by virtue of its prosecution of its own patent relating to SSD memory controllers. On or about April 16, 2014, SanDisk Technologies Inc. ("SanDisk") filed U.S. patent application No. 14/254,354, which eventually issued as U.S. Patent No. 9,977,628 ("the '628 Patent") on May 22, 2018. The '628 Patent is entitled "Storage Module and Method for Configuring the Storage Module with Memory Operation Parameters" and relates to methods of controlling memory operations in a storage module through a memory controller.

71. The '628 Patent has a direct relationship to the accused functionality in the '190 Accused Products. For example, the '628 Patent specifically discusses how the purported inventions in the patent can be applied to SLC cache functionality:

> As yet another example, a user can trade off between the capacity of a storage module for performance or data retention. For example, using a memory as a single level cell (SLC) memory instead of a multi-level cell (MLC) memory can provide faster write performance (e,g., from 5 MB/sec to 20 MB/sec), but can reduce the storage capacity of the memory (e.g., from 16 GB to 8 GB). Using the memory as an SLC memory also provides better data retention /endurance (longer data life).

'628 Patent, at 4:57-65.

> There are many alternatives that can be used with these embodiments. . . . For example, a memory cell may be designed as a "flex cell," in which the cell can either be used as a single-level cell (SLC) or a multi-level cell (MLC), as determined by the storage controller 110. So, to make a tradeoff between performance and endurance, the storage controller 110 can confiture the cells to SLC cells (because it is faster to write to SLC cells than MLC cells), and then, at a later time (e.g., as a background operation), move the data from the SLC cells to the MLC cells (which reduces the endurance of the storage module 100 since another program/erase cycle is used for that transfer).

Id. at 7:46-65.

72. During the prosecution of the ’628 Patent, SanDisk was acquired by Western Digital. Specifically, on or about October 21, 2015, Western Digital announced that it was acquiring SanDisk. Western Digital announced that the acquisition was completed on or about May 12, 2016.

73. During the prosecution of the ’628 Patent, the patent examiner repeatedly cited to the ’190 Patent as the basis for obviousness rejections of claims pending in the application for the ’628 Patent. Specifically, the examiner cited to the ’190 Patent as the basis for obviousness rejections of various pending claims in Office Actions sent to SanDisk/Western Digital on April 6, 2016, November 30, 2016, and June 14, 2017. SanDisk/Western Digital amended the claims in the ’354 application to overcome these rejections.

74. In addition, as set forth above, Western Digital also had knowledge of the ’190 Patent in or around 2016 by virtue of BNI approaching Western Digital and/or SanDisk at that time with respect to its patents.

75. In addition, Western Digital also had knowledge of the ’190 Patent since at least May 18, 2018, when BiTMICRO served a subpoena on Western Digital in connection with a proceeding before the International Trade Commission, *In the Matter of Certain Solid State Storage Drives, Stacked Electronics Components, and Products Containing Same*, Inv. No. 337-TA-1097 (“the ITC Action”). In the ITC Action, BiTMICRO alleged that various solid state computer drives (“SSDs”) and electronic devices that incorporate stacked electronics components sold by Samsung Electronics, SK Hynix, and other electronic device manufacturers infringed four BiTMICRO patents, including the ’190 Patent.

76. On information and belief, through its activities in the prosecution of the ’628 Patent as well as its participation in the ITC Action as described above, Western Digital had knowledge of the ’190 Patent and its relevance to the ’190 Accused Products. Despite this knowledge, Western Digital has continued to directly infringe

one or more claims of the '190 Patent as described above. Thus, on information and belief, Western Digital's infringement of the '190 Patent has been willful.

77. For the foregoing reasons, Western Digital's infringement of the '190 Patent has been and continues to be deliberate and willful, and this is therefore an exceptional case warranting an award of enhanced damages and attorneys' fees and costs pursuant to 35 U.S.C. §§ 284-285.

78. On information and belief, Western Digital will continue to infringe the '190 Patent unless enjoined by this Court.

79. As a result of Western Digital's infringement of the '190 Patent, BiTMICRO has suffered monetary damages, and seeks recovery, in an amount to be proven at trial, adequate to compensate for Western Digital's infringement, but in no event less than a reasonable royalty with interest and costs.

80. Western Digital's infringement of BiTMICRO's rights under the '190 Patent will continue to damage BiTMICRO, causing irreparable harm for which there is no adequate remedy at law, unless enjoined by this Court.

SECOND COUNT

(INFRINGEMENT OF U.S. PATENT NO. 8,010,740)

81. BiTMICRO incorporates by reference the allegations set forth in paragraphs 1-79 as though fully set forth herein.

82. On information and belief, Western Digital has directly infringed and continues to directly infringe one or more claims of the '740 Patent, including at least claim 1 of the '740 Patent, in the state of California, in this judicial district, and elsewhere in the United States by, among other things, making, using, selling, offering for sale, and/or importing into the United States products that embody one or more of the inventions claimed in the '740 Patent, including but not limited to the above-identified NVMe SSDs and all reasonably similar products ("the '740 Accused Products"), in violation of 35 U.S.C. § 271(a).

83. As an example, Western Digital's UltraStar DC SN640 Series SSDs include "a mapping table for optimizing memory operations performed by an electronic storage device in response to receiving an I/O transaction request initiated by a host." Specifically, the SSDs include a mapping table located in DRAM or other memory to map logical block addresses (LBAs) to physical block addresses (PBAs) on the memory devices within the SSD. See Western Digital White Paper, "Flash 101 and Flash Management,"[9] at 6 ("To understand Wear Leveling, one needs to understand the different addressing schemes in a system. The operating system (OS) uses Logical Block Addressing (LBA) to read and write to the device, the flash controller uses physical addresses on the flash to read and write data . . . [t]he managed NAND controller has the ability to map an LBA address to different physical locations on the flash. The controller uses a mapping table to keep track of the relationship between the logical block and the physical address.").

84. Information in the mapping table is used by a controller in the UltraStar DC SN640 Series SSDs to optimize memory operations, by for example allowing the controller to perform interleaving to optimally distribute data across multiple non-volatile memory channels, lanes, buses, devices, dies, planes, etc., thereby improving the speed and efficiency of storing and accessing the data. *See, e.g.*, Western Digital Data Sheet "UltraStar DC SN640"[10] at 1 ("The DC SN640 include Western Digital's 96-layer BiCS4 3D TLC NAND and Western Digital's NVMe 1.3c controller . . ."); *id*. at 2 (Interface . . . PCIe Gen 3.1 x4 (Compliant to NVMe 1.3c"); Tom's Hardware Blog, "WD My Passport SSD Review: Sleek, Slim, and Secure Storage,"[11] ("WD's

[9] Available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/collateral/white-paper/white-paper-sandisk-flash101-management.pdf.

[10] Available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/product/data-center-drives/ultrastar-nvme-series/data-sheet-ultrastar-dc-sn640.pdf.

[11] Available at https://www.tomshardware.com/reviews/wd-my-passport-ssd-review.

Blue SN550E is a DRAM-less M.2 2280 PCIe 3.0 x4 NVMe SSD that leverages a quad-channel controller and WD's 512 Gb 96-layer TLC flash. Sixteen flash dies are stuffed within our 1TB sample, each featuring a dual-plane design that doubles interleaving performance compared to a single-plane flash."); Western Digital Blog, "What is NVMe™ and why is it important? A Technical Guide,"[12] ("NVMe is a high-performance, NUMA (Non Uniform Memory Access) optimized, and highly scalable storage protocol, that connects the host to the memory subsystem. The protocol is relatively new, feature-rich, and designed from the group up for non-volatile memory media (NAND and Persistent Memory) directly connected to CPU via PCIe interface See diagram #1). The protocol is built on high speed PCIe lanes.")).

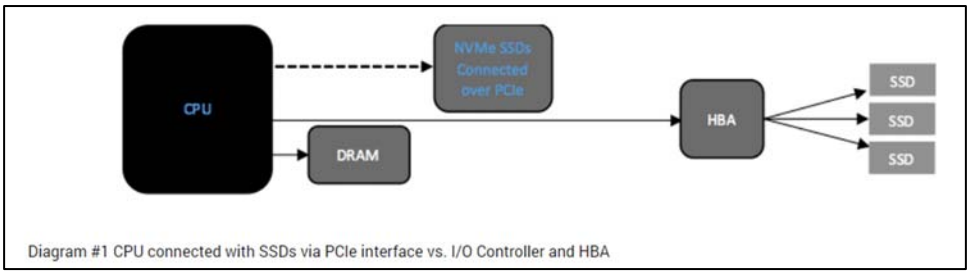

Diagram #1 CPU connected with SSDs via PCIe interface vs. I/O Controller and HBA

Id.

85. The mapping table of the UltraStar DC SN640 Series SSDs also includes "a set of logical fields, including a first logical field and a second logical field, and said logical fields respectively disposed for representing a plurality of LBA sets, including said first logical field disposed for representing a first LBA set and said second logical field disposed for representing a second LBA set, said first and second LBA sets each representing a set of consecutive LBAs." For example, the mapping table includes a set of logical fields that represent sets of consecutive LBAs. *See,*

[12] Available at https://blog.westerndigital.com/nvme-important-data-driven-businesses/.

e.g., Western Digital White Paper, "Flash 101 and Flash Management,"[13] at 6 ("Flash Management mission is to create a Logical to Physical layer that is transparent to the host and provide logical read and write services . . . [t]he managed NAND Controller has the ability to map an LBA address to different physical locations on the flash. The controller uses a mapping table to keep track of the relationship between the logical block and the physical address."); Western Digital's U.S. Pat. No. 10,565,123, "Hybrid logical to physical address translation for non-volatile storage devices with integrated compute module," at 3:62-4:2 ("In many systems the non-volatile storage is addressed internally to the memory system using physical addresses associated with one or more memory die. However, the host system will use logical addresses to address the various memory locations. This enables the host to assign data using consecutive logical addresses, while the memory system is free to store the data as it wishes among the locations of the one or more memory die.")).

86. The mapping table of the UltraStar DC SN640 Series SSDs also includes "a set of PBA fields, including a first PBA field and a second PBA field, said set of PBA fields respectively disposed for representing a set of PBAs, including a first PBA disposed for representing a first set of access parameters and a second PBA disposed for representing a second set of access parameters, said PBAs each associated with a physical memory location in a memory store, said set of logical fields and said set of PBA fields disposed to associate said first and second LBA sets with said first and second PBAs." For example, the first and second PBAs can be associated with different non-volatile memory channels, lanes, buses, devices, dies, planes, etc. within the SSD. *See, e.g.*, Western Digital White Paper, "Flash 101 and

[13] Available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/collateral/white-paper/white-paper-sandisk-flash101-management.pdf.

Flash Management,"[14] at 6 ("Flash Management mission is to create a Logical to Physical layer that is transparent to the host and provide logical read and write services . . . [t]he managed NAND Controller has the ability to map an LBA address to different physical locations on the flash. The controller uses a mapping table to keep track of the relationship between the logical block and the physical address."); See, *e.g.*, Western Digital Data Sheet "UltraStar DC SN640"[15] ("The DC SN640 include Western Digital's 96-layer BiCS4 3D TLC NAND and Western Digital's NVMe 1.3c controller . . ."); Western Digital's U.S. Pat. No. 10,565,123, "Hybrid logical to physical address translation for non-volatile storage devices with integrated compute module," at 3:62-4:2 ("In many systems the non-volatile storage is addressed internally to the memory system using physical addresses associated with one or more memory die. However, the host system will use logical addresses to address the various memory locations. This enables the host to assign data using consecutive logical addresses, while the memory system is free to store the data as it wishes among the locations of the one or more memory die.").

87. The first and second PBA fields represent these first and second PBAs, respectively, in the mapping table. Each of the PBAs has a set of access parameters defined in the mapping table, such as identifying information that allows the PBA to be associated with one or more LBAs, and the first and second LBA sets are associated with the first and second PBAs, respectively. See Western Digital White Paper, "Flash 101 and Flash Management,"[16] at 6 ("Flash Management mission is to

[14] Available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/collateral/white-paper/white-paper-sandisk-flash101-management.pdf.

[15] Available at https://www.westerndigital.com/en-kw/tools/documentRequestHandler?docPath=/content/dam/doc-library/en_us/assets/public/western-digital/product/data-center-drives/ultrastar-nvme-series/data-sheet-ultrastar-dc-sn640.pdf.

[16] Available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/collateral/white-paper/white-paper-sandisk-flash101-management.pdf.

create a Logical to Physical layer that is transparent to the host and provide logical read and write services . . . [t]he managed NAND Controller has the ability to map an LBA address to different physical locations on the flash. The controller uses a mapping table to keep track of the relationship between the logical block and the physical address."); Western Digital User Manual, "Western Digital SSD Dashboard,"[17] at 14 ("Secure Erase deletes the mapping table on the selected SSD, but it does not erase all blocks that have been written to.").

88. Also, the mapping table of the UltraStar DC SN640 Series SSDs, "in response to receiving the I/O transaction request, [] causes the electronic storage device to perform optimized memory operations on memory locations respectively associated with said first PBA and said second PBA, if the I/O transaction request is associated with said first and second LBA sets." For example, the interleaving function in the SSDs allows the products to perform optimized memory operations on memory locations associated with the first PBA and second PBA by distributing the reading and writing of data across those memory locations to increase the speed and efficiency of storing and accessing the data. This interleaving requires the use of the LBA-PBA mapping information in the mapping table by the memory controller within the SSD. Western Digital White Paper, "Top Considerations for Enterprise SSDs,"[18] at 7 ("Simulated workloads are characterized by their block sizes, their access patterns, the queue or I/O depth, and the read-to-write ratio. The block size is simply the natural I/O size for the task at hand . . . [t]his access pattern is defined as either sequential (contiguous ranges of the SSD are accessed in sequence) of random (the position of each I/O operation is independent of the prior I/Os). The queue

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[17] Available at https://wddashboarddownloads.wdc.com/wdDashboard/um/4779-705161.pdf

[18] Available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/collateral/white-paper/white-paper-top-considerations-for-enterprise-ssds.pdf.

depth, or I/O depth, is an indication of the parallelism of I/O operations, reflecting how many are in flight at any given time"; *see also* Western Digital Blog "NVM Queues Explained"[19] ("NVM Express (NVMe) is the first storage protocol designed to take advantage of modern high-performance storage media. The protocol offers parallel and scalable interface designed to reduce latencies and increase IOPS and bandwidth thanks to its ability to support more than 64K queues and 64K commands/queue . . . [w]ith PCIe and solid state media-NAND, SSDs created parallel data paths to underlying storage bits . . ."); Tom's Hardware Blog, "WD My Passport SSD Review: Sleek, Slim, and Secure Storage,"[20] ("WD's Blue SN550E is a DRAM-less M.2 2280 PCIe 3.0 x4 NVMe SSD that leverages a quad-channel controller and WD's 512 Gb 96-layer TLC flash. Sixteen flash dies are stuffed within our 1TB sample, each featuring a dual-plane design that doubles interleaving performance compared to a single-plane flash.").

89. All of the '740 Accused Products infringe the '740 Patent, including at least claim 1, in the same or similar manner as the UltraStar DC SN640 Series SSDs.

90. By making, using, offering for sale, and/or selling products in the United States and/or importing products into the United States, including but not limited to the '740 Accused Products, Western Digital has injured BiTMICRO and is liable to BiTMICRO for directly infringing one or more claims of the '740 Patent, including without limitation claim 1 pursuant to 35 U.S.C. § 271(a).

91. On information and belief, Western Digital will continue to infringe the '740 Patent unless enjoined by this Court.

92. As a result of Western Digital's infringement of the '740 Patent, BiTMICRO has suffered monetary damages, and seeks recovery, in an amount to be

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[19] Available at https://blog.westerndigital.com/nvme-queues-explained/.

[20] Available at https://www.tomshardware.com/reviews/wd-my-passport-ssd-review.

proven at trial, adequate to compensate for Western Digital's infringement, but in no event less than a reasonable royalty with interest and costs.

93. Western Digital's infringement of BiTMICRO's rights under the '740 Patent will continue to damage BiTMICRO, causing irreparable harm for which there is no adequate remedy at law, unless enjoined by this Court.

THIRD COUNT

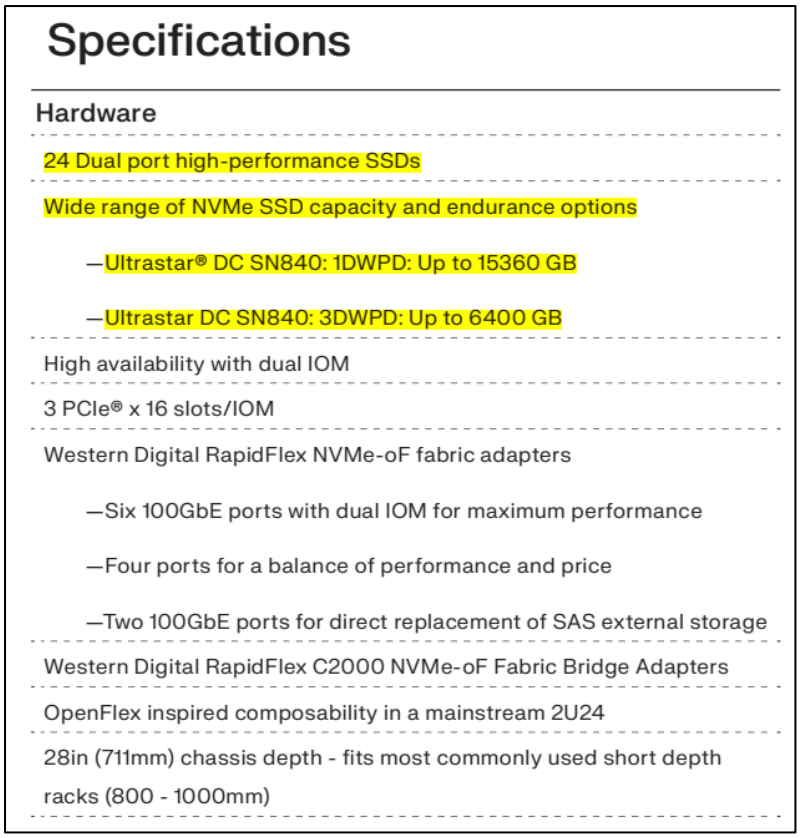
(INFRINGEMENT OF U.S. PATENT NO. 9,875,205)

94. BiTMICRO incorporates by reference the allegations set forth in paragraphs 1-92 as though fully set forth herein.

95. Western Digital has directly infringed one or more claims of the '205 Patent, including at least claim 1 of the '205 Patent, in the state of California, in this judicial district, and elsewhere in the United States by, among other things, making, using, selling, offering for sale, and/or importing into the United States products that embody one or more of the inventions claimed in the '205 Patent, including but not limited to the above-identified NVMe-oF storage platforms, and all reasonably similar products ("the '205 Accused Products"), in violation of 35 U.S.C. § 271(a).

96. As an example, the OpenFlex Data24 NVMe-oF storage platform is an "apparatus" as recited in claim 1 of the '205 Patent:

Western Digital Product Brief, "OpenFlex Data24 Series NVMe-oF Storage Platform,"[21] at 1. Each OpenFlex Data24 NVMe-oF storage platform can include up to 24 Western Digital UltraStar SSDs:



Specifications

Hardware

24 Dual port high-performance SSDs

Wide range of NVMe SSD capacity and endurance options

—Ultrastar® DC SN840: 1DWPD: Up to 15360 GB

—Ultrastar DC SN840: 3DWPD: Up to 6400 GB

High availability with dual IOM

3 PCIe® x 16 slots/IOM

Western Digital RapidFlex NVMe-oF fabric adapters

—Six 100GbE ports with dual IOM for maximum performance

—Four ports for a balance of performance and price

—Two 100GbE ports for direct replacement of SAS external storage

Western Digital RapidFlex C2000 NVMe-oF Fabric Bridge Adapters

OpenFlex inspired composability in a mainstream 2U24

28in (711mm) chassis depth - fits most commonly used short depth racks (800 - 1000mm)

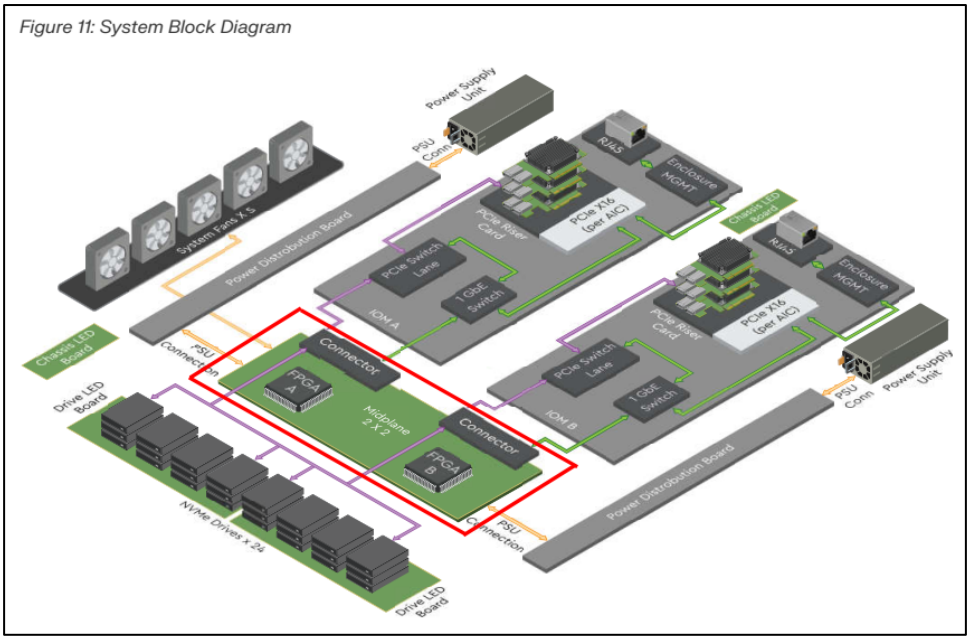
Id. at 2. *See also* Western Digital User Guide, "OpenFlex Data24 3200,"[22] at 3 ("On the front of the OpenFlex Data24 3200 there are the 24 Small Form Factor (SFF) drive slots, and the enclosure status LEDs. Each drive is individually removable/serviceable.").

97. The OpenFlex Data24 NVMe-oF storage platform includes "a communication bus interface" for facilitating communications to and from each of

[21] Available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/product/platforms/openflex/product-brief-data24-3200-nvme-of-storage-platform.pdf.

[22] Available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/product/platforms/openflex/user-guide-openflex-data24-3200.pdf.

the SSDs within the system. *See, e.g.*, Western Digital User Guide, "OpenFlex Data24 3200,"[23] at 15 (annotated in red):



Western Digital User Guide, "OpenFlex Data24 3200,"[24] at 15. *See also* Western Digital Blog, "NVMe-oF Full Speed Ahead,"[25] ("Western Digital launched its next step in NVMe and NVMe-oF with enhanced versions of its OpenFlex Data24 NVMe-oF storage platform, next-generation RapidFlex A2000 and C2000 NVMe-oF fabric bridge devices (FBDs), and the new Ultrastar DC SN655 PCIe Gen 4.0 dual-port NVMe SSDs . . . NVMe-oF takes the performance benefits of NVMe one step further by sharing flash resources among servers for improved performance, availability, and flexibility."); Western Digital Product Brief, "OpenFlex Data24 Series NVMe-oF

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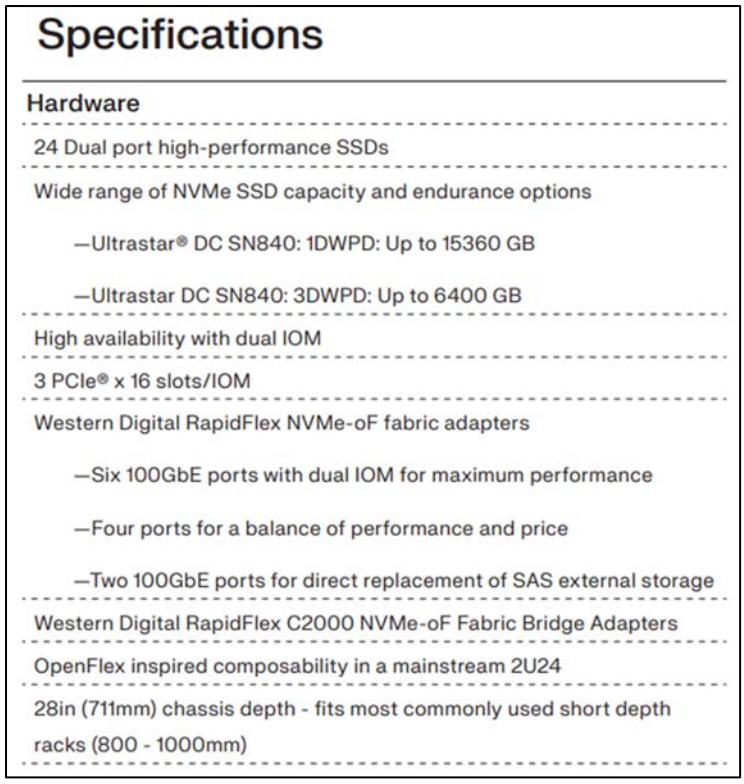
[23] Available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/product/platforms/openflex/user-guide-openflex-data24-3200.pdf.

[24] Available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/product/platforms/openflex/user-guide-openflex-data24-3200.pdf.

[25] Available at https://blog.westerndigital.com/nvme-of-full-speed-ahead/.

Storage Platform,"[26] at 1 ("Similar to the original OpenFlex Data24, it provides low-latency sharing of NVMe SSDs over a high performance Ethernet fabric to deliver similar performance to locally attached SSDs . . . OpenFlex Data24 3200 series uses Western Digital's RapidFlex C2000 Fabric Bridge Adapters to provide 2, 4, or 6-ports of 100GbE which can now connect to RDMA and/or TCP configured host ports . . . OpenFlex Data24 3200 series offers the flexibility of connecting to either RoCE or TCP host ports for optimum usage.")."



Specifications

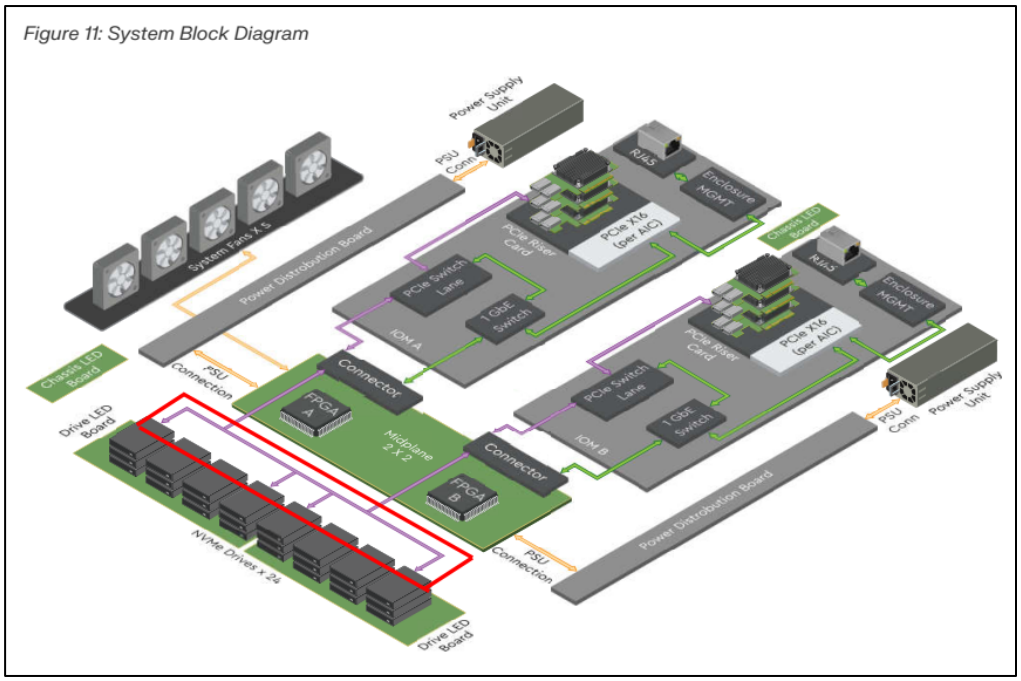
Hardware
24 Dual port high-performance SSDs
Wide range of NVMe SSD capacity and endurance options —Ultrastar® DC SN840: 1DWPD: Up to 15360 GB —Ultrastar DC SN840: 3DWPD: Up to 6400 GB
High availability with dual IOM
3 PCIe® x 16 slots/IOM
Western Digital RapidFlex NVMe-oF fabric adapters —Six 100GbE ports with dual IOM for maximum performance —Four ports for a balance of performance and price —Two 100GbE ports for direct replacement of SAS external storage
Western Digital RapidFlex C2000 NVMe-oF Fabric Bridge Adapters
OpenFlex inspired composability in a mainstream 2U24
28in (711mm) chassis depth - fits most commonly used short depth racks (800 - 1000mm)

Id. at 2.

98. The OpenFlex Data24 NVMe-oF storage platform further includes "a flash memory module coupled to the communication bus interface via a communication bus." The OpenFlex Data24 Series system includes up to 24 Western Digital Ultrastar SSDs. *Id.* Any grouping of one or more of the Ultrastar SSDs in the

[26] Available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/product/platforms/openflex/product-brief-data24-3200-nvme-of-storage-platform.pdf.

OpenFlex Data24 Series system can constitute a flash memory module. The flash memory module is coupled to the communication bus interface in the OpenFlex Data24 Series system via a communication bus. *See, e.g.*, Western Digital User Guide, "OpenFlex Data24 3200,"[27] at 15 (annotated in red):



See also Western Digital Press Release, "Western Digital Delivers New Levels of Flexibility, Scalability for the Data Center,"[28] ("In addition to RDMA over converged Ethernet (RoCE), the enhanced Data24 now features new TCP connection support. Available in a 2U 24-bay platform and backed with a 5-year warranty, the Data24 3200 is built to deliver low power, high availability and enterprise-class reliability with up to 368TB in a single platform of low-latency dual-port PCIe Gen 4.0 SSDs.").

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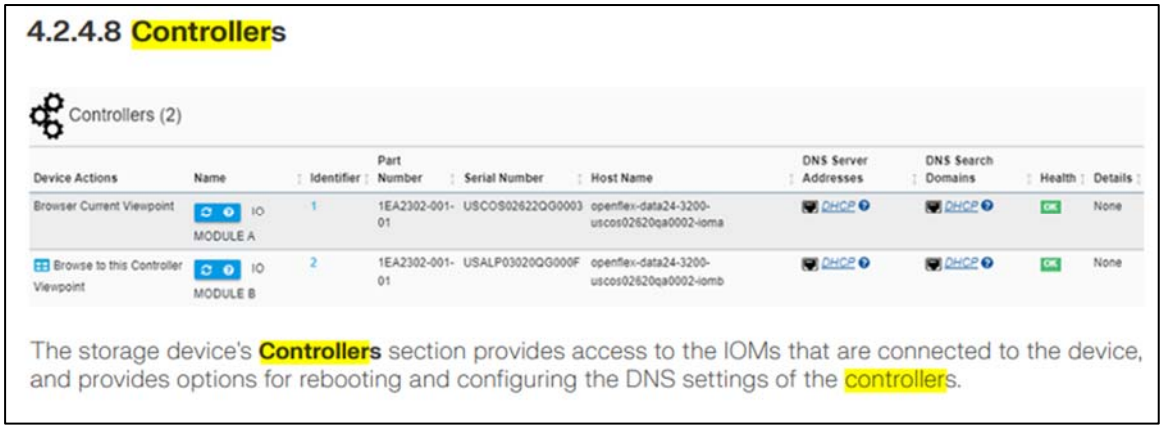
[27] Available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/product/platforms/openflex/user-guide-openflex-data24-3200.pdf.

[28] Available at https://www.westerndigital.com/company/newsroom/press-releases/2023/2023-08-08-western-digital-delivers-new-levels-of-flexibility-scalability-for-the-data-center.

99. The OpenFlex Data24 NVMe-oF storage platform further includes "a system controller coupled to the communication bus interface via an external communication bus." For example, the OpenFlex Data24 Series system includes a Western Digital RapidFlex NVMe-oF controller and a RapidFlex C2000 Fabric Bridge Adapter. Each of these components, either alone or in combination, constitute a system controller. See Western Digital Product Brief, "OpenFlex Data24 Series NVMe-oF Storage Platform,"[29] at 1 ("Unsurpassed connectivity in its class using Western Digital RapidFlex NVMe-oF controllers, allows up to six hosts to be attached without a switch, like a traditional JBOF."); *see also* Western Digital White Paper, "Western Digital OpenFlex Data24 – Shared High-Performance NVMe Storage,"[30] at 4 ("Western Digital's OpenFlex Data24 NVMe-oF storage platform provides the high-performance of server resident NVMe flash storage, along with the benefits of external, shared storage. The Data24 system provides low-latency sharing of NVMe SSDs over a high-performance Ethernet fabric to deliver similar performance to locally attached NVMe SSDs. Utilizing Western Digital Fabric adapters, the Data24 allows up to six hosts to be attached without a switch or up to 48 hosts when sharing storage through one or more switches.")). The system controller is included as part of the IO Module (IOM):

[29] Available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/product/platforms/openflex/product-brief-data24-3200-nvme-of-storage-platform.pdf.

[30] Available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/collateral/white-paper/white-paper-evaluator-group-lab-insight-western-digital-openflex-data24.pdf.



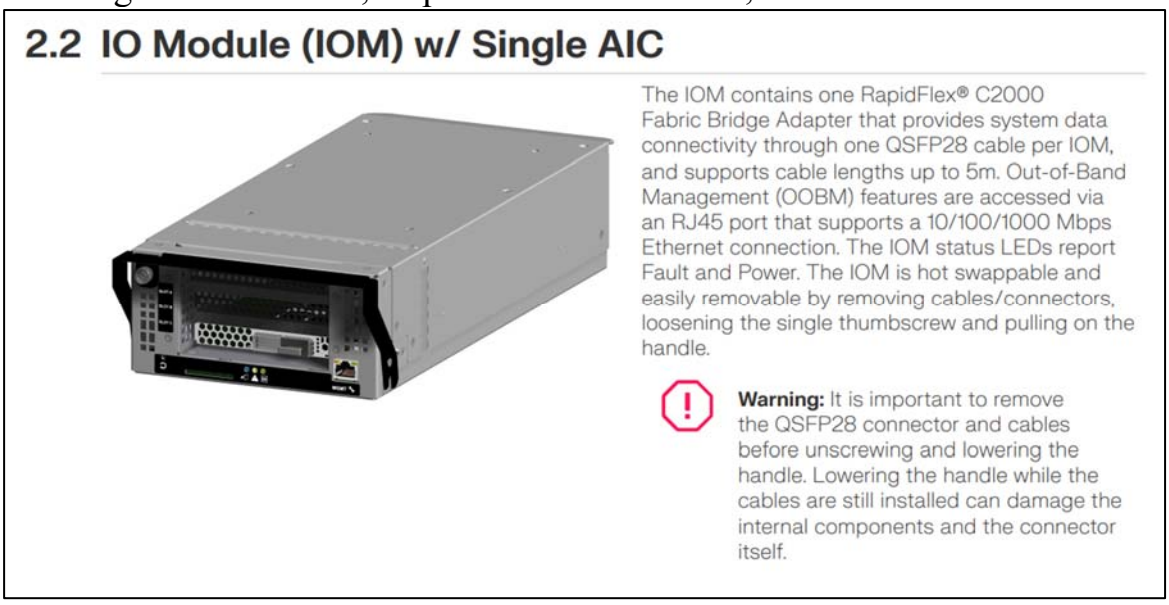
4.2.4.8 Controllers

Controllers (2)

Device Actions	Name	Identifier	Part Number	Serial Number	Host Name	DNS Server Addresses	DNS Search Domains	Health	Details
Browser Current Viewpoint	IO MODULE A	1	1EA2302-001-01	USCOS02622QG0003	openflex-data24-3200-uscos02620qa0002-ioma	DHCP	DHCP	OK	None
Browse to this Controller Viewpoint	IO MODULE B	2	1EA2302-001-01	USALP03020QG000F	openflex-data24-3200-uscos02620qa0002-iomb	DHCP	DHCP	OK	None

The storage device's Controllers section provides access to the IOMs that are connected to the device, and provides options for rebooting and configuring the DNS settings of the controllers.

Western Digital User Guide, "OpenFlex Data24 3200,"[31] at 119. *See also id.* at 27:



2.2 IO Module (IOM) w/ Single AIC

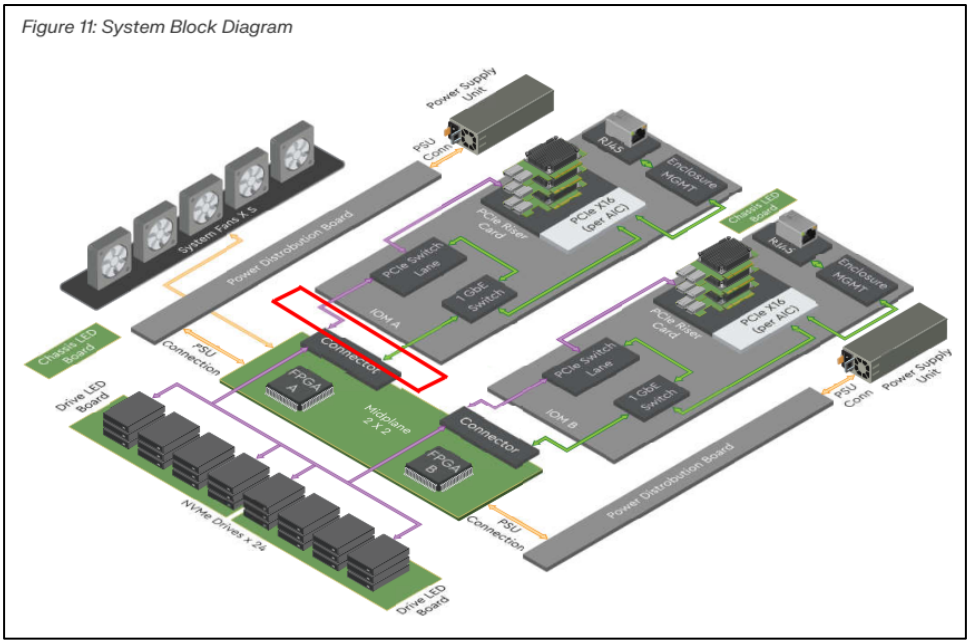
The IOM contains one RapidFlex® C2000 Fabric Bridge Adapter that provides system data connectivity through one QSFP28 cable per IOM, and supports cable lengths up to 5m. Out-of-Band Management (OOBM) features are accessed via an RJ45 port that supports a 10/100/1000 Mbps Ethernet connection. The IOM status LEDs report Fault and Power. The IOM is hot swappable and easily removable by removing cables/connectors, loosening the single thumbscrew and pulling on the handle.

Warning: It is important to remove the QSFP28 connector and cables before unscrewing and lowering the handle. Lowering the handle while the cables are still installed can damage the internal components and the connector itself.

The system controller is also coupled to the communication bus interface via an external communication bus. *See, e.g.*, Western Digital User Guide, "OpenFlex Data24 3200,"[32] at 15 (annotated in red):

[31] Available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/product/platforms/openflex/user-guide-openflex-data24-3200.pdf.

[32] Available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/product/platforms/openflex/user-guide-openflex-data24-3200.pdf.



100. The OpenFlex Data24 NVMe-oF storage platform further provides functionality "wherein the system controller performs a memory transaction via the communication bus interface to the flash memory module." The OpenFlex Data24 Series system includes a system controller which performs a memory transaction via the communication bus interface to the flash memory module. *See id.* at 2 ("OpenFlex Data24 utilizes two IOMs to provide data connectivity using QSFP28 connections through Western Digital's RapidFlex add-in cards. OpenFlex is Western Digital's architecture that supports Open Composable Infrastructure (OCI). The OpenFlex Data24 3200 is a Just-a-Bunch-Of-Flash (JBOF) platform that leverages this OCI approach in the form of disaggregated data storage using NVMe-over-Fabrics (NVMe-oF). NVMe-oF is a networked storage protocol that allows storage to be disaggregated from compute to make that storage widely available to multiple applications and hosts . . . OpenFlex does not rule out multiple fabrics, but whenever possible, Ethernet will be used as a unifying connection for both flash and disk because of its broad applicability and availability."); *see also* Western Digital Solution Brief, "Three Ways to Add Western Digital OpenFlex Data24 Storage to

OpenStack,"[33] ("They provide 24 slots for NVMe drives and a maximum capacity of 368 TB when using Western Digital Ultrastar DC SN840 15.36 TB devices. Unlike a SAS enclosure, the Data24 platforms use Western Digital RapidFlex fabric bridge adapter. These controllers allow full access to all 24 NVMe drives over up to six ports of 100 Gb Ethernet . . . [t]he OpenFlex Data24 design exposes the full performance of the NVMe SSDs to the network. With 24 Western Digital Ultrastar DC SN840 3.2 TB devices, the enclosure can achieve up to 71 GB/s of 128K bandwidth and over 16.7 MIOPS at a 4K block size.").

101. All of the '205 Accused Products infringe the '205 Patent, including at least claim 1, in the same or similar manner as the OpenFlex Data24 NVMe-oF storage platform.

102. By making, using, offering for sale, and/or selling products in the United States and/or importing products into the United States, including but not limited to the '205 Accused Products, Western Digital has injured BiTMICRO and is liable to BiTMICRO for directly infringing one or more claims of the '205 Patent, including without limitation claim 1 pursuant to 35 U.S.C. § 271(a).

103. On information and belief, Western Digital will continue to infringe the '205 Patent unless enjoined by this Court.

104. As a result of Western Digital's infringement of the '205 Patent, BiTMICRO has suffered monetary damages, and seeks recovery, in an amount to be proven at trial, adequate to compensate for Western Digital's infringement, but in no event less than a reasonable royalty with interest and costs.

105. Western Digital's infringement of BiTMICRO's rights under the '205 Patent will continue to damage BiTMICRO, causing irreparable harm for which there is no adequate remedy at law, unless enjoined by this Court.

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[33] Available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/collateral/solution-brief/solution-brief-openflex-data24-three-ways-to-add-storage-to-openstack.pdf.

FOURTH COUNT

(INFRINGEMENT OF U.S. PATENT NO. 7,716,389)

106. BiTMICRO incorporates by reference the allegations set forth in paragraphs 1-104 as though fully set forth herein.

107. Western Digital has directly infringed one or more claims of the '389 Patent, including at least claim 19 of the '389 Patent, in the state of California, in this judicial district, and elsewhere in the United States by, among other things, making, using, selling, offering for sale, and/or importing into the United States products that embody one or more of the inventions claimed in the '389 Patent, including but not limited to the above-identified SSDs with hardware encryption or self-encrypting drives, and all reasonably similar products ("the '389 Accused Products"), in violation of 35 U.S.C. § 271(a).

108. As an example, Western Digital's Ultrastar DC SN861 includes "a direct memory access controller for transferring data to or from a memory, and for encrypting or decrypting said data upon receiving a data processing request." Specifically, it includes a controller chip that can directly access memory and transfer data to or from memory locations in the SSD utilizing the NVMe protocol. *See* Western Digital Blog "What is NVMe™ and why is it important? A Technical Guide,"[34] ("NVMe is a high-performance NUMA (Non Uniform Memory Access) optimized and highly scalable storage protocol, that connects the host to the memory subsystem. The protocol is relatively new, feature-rich, and designed from the ground up for non-volatile memory media (NAND and Persistent Memory) directly connected to CPU via PCIe interface See diagram #1). The protocol is built on high

[34] Available at https://blog.westerndigital.com/nvme-important-data-driven-businesses/.

speed PCIe lanes."); Western Digital Data Sheet, "Ultrastar DC SN861"[35] ("Experience future-ready PCIe Gen5 read/write speeds . . . [d]esigned to support NVMe 2.0, and NVMe MI 1.2c, and OCP 2.0 supportive for enhanced scalability and efficiency.").

109. The controller in Western Digital's Ultrastar DC SN861 also includes built-in hardware encryption and decryption capabilities. Specifically, it features TCG security and encryption utilizing the TCG Opal 2.01 standard. *See* Western Digital website, "Ultrastar DC SN861 NVMe SSD"[36] ("Benefit from . . . TCG security and encryption . . . [s]ecurity: TCG Opal."). Other '389 Accused Products, such as Western Digital's Ultrastar DC SN840, utilize the TCG Ruby standard. Western Digital's implementation of the TCG Ruby specification functions similarly to Opal. *See* Western Digital Tech Brief, "Setting up TCG Ruby with Sedutil,"[37] at 1 ("The purpose for TCG Ruby is to provide an up-to-date enterprise Security Subsystem Class (SSC) to support NVMe datacenter drives. . . [i]t is part of the broader Opal SSC (such as Pyrite and Opalite) and has protocol compatibility with the Opal family. Western Digital's specific implementation of the TCG Ruby specification (see below for a comparison about Opal v2.01 and TCG Ruby) makes it very similar to Opal, but preboot authentication is not supported.").

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[35] Available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/product/data-center-drives/ultrastar-nvme-series/data-sheet-ultrastar-dc-sn840.pdf.

[36] Available at https://www.westerndigital.com/products/internal-drives/data-center-drives/ultrastar-dc-sn861-ssd?sku=0TS2530.

[37] Available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/collateral/tech-brief/tech-brief-setting-up-tcg-ruby-with-sedutil.pdf.

Feature	Opal V2.01	TCG Ruby
Activation and Life Cycle	Yes	Yes
Number of Admin, Users	4 Admin, 8 Users	1 Admin, 2 Users
Min Number of Required Logical Block Addressing (LBA) Ranges	Global Range +8	Global Range (+8 on Western Digital drives)
Min Datastore Size	10MB	128 KB
Min MBR Table Size	128MB	Optional: 128MB if supported
Configurable Access Control	Yes	Yes
PSID	Yes	Yes
Media Encryption	Required	Required
Crypto Erase	Revert, Revert SP, GenKey methods for device and locking range level erase granularity	Same as Opal

Id. at 1.

110. As shown below, Western Digital provides three SSD security options with user data encrypted at rest: Instant Secure Erase (ISE), Trusted Computing Group (TCG), and TCG-FIPS. *See* Western Digital website, "Protect Your Data"[38] ("ISE drives support all sanitization methods as SE drives. In addition, ISE drives have data encrypted at rest . . . TCG drives have data encrypted at rest . . . TCG-FIPS drives are identical to TCG, but are additionally validated by a NIST-approved laboratory to meet the Federal Information Processing Standard (FIPS).").

Security Type	User Data Encrypted At Rest	Data Access Control	Preferred NIST Purge-Compliant Erase	External Certification of Security Protocol
Secure Erase (SE) ⓘ Shop Now	–	ATA Security (SATA only)	Sanitize Overwrite (HDD) Sanitize Block Erase (SSD)	–
Instant Secure Erase (ISE) ⓘ Shop Now	✓	ATA Security (SATA only)	All of the above, plus Crypto Erase	–
Trusted Computing Group (TCG) ⓘ Shop Now	✓	TCG-SSC	All of the above, plus Revert	–
TCG-FIPS ⓘ Shop Now	✓	TCG-SSC	All of the above	✓ FIPS 140-2 Certification by NIST-approved labs[1]

Id.

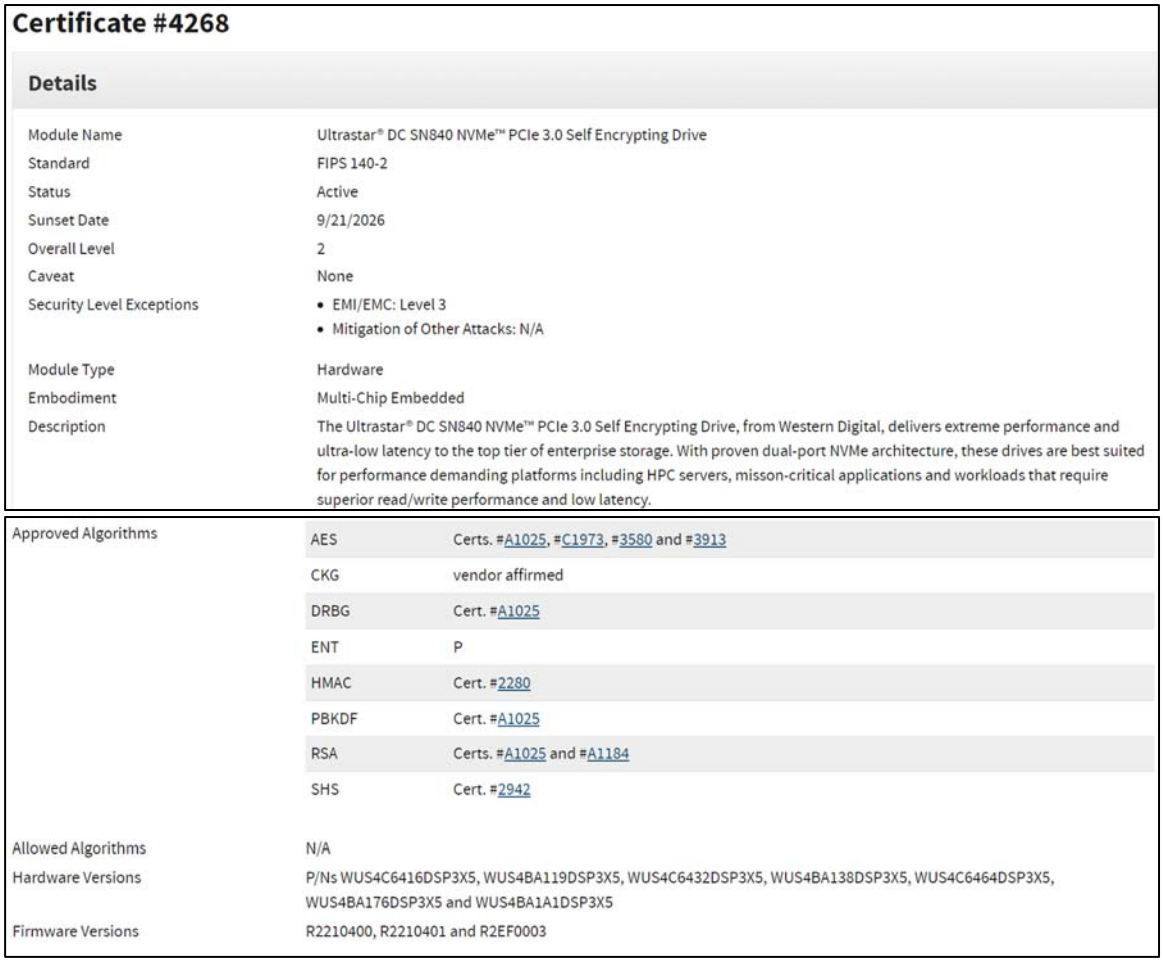
111. Encryption is a key capability of the featured in each of the '389 Accused Products. For example, Western Digital's Ultrastar DC SN861 uses the Advanced Encryption Standard (AES), scrambling data using a secret key and

[38] Available at https://www.westerndigital.com/solutions/data-security/data-protection.

encryption algorithm to automatically convert stored data into an unreadable form known as ciphertext. The algorithm encrypts files even before they are physically written onto the device, meaning the data is encrypted at rest. *See, e.g.*, Western Digital Blog, "What Are Encrypted Drives?"[39] ("Self-encrypted drives automatically convert stored data into a scrambled, unreadable form known as ciphertext, using an encryption algorithm. This algorithm encrypts created files even before they are physically written onto the device, rendering your storage drive 'encrypted at rest.' While there are many encryption algorithms, AES, the Advanced Encryption Standard, is one of the most widely adopted and recognized modern cryptographic algorithms. This algorithm uses fixed blocks of data, typically 128-bit or 256-bit, and scrambles them using a secret key . . . [a]s soon as a file is created, the algorithm begins encrypting fixed blocks of data in a series of cryptographic operations including substitution, permutation and mixing."; Western Digital Data Sheet, "Ultrastar DC SN861"[40] at 1 ("Benefit from enterprise-class features such as Power Loss Protection, End-to-End Data Path Protection, and TCG security and encryption, helping ensure data integrity and security."). Others of the '389 Accused Products, including Western Digital's Ultrastar DC SN840 NVMe PCIe 3.0 Self-Encrypting Drive have active FIPS 140-2 certification through the Cryptographic Module Validation Program of the National Institute of Standards and Technology ("NIST").

[39] Available at https://blog.westerndigital.com/what-are-encrypted-drives/.

[40] Available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/product/data-center-drives/ultrastar-nvme-series/data-sheet-ultrastar-dc-sn840.pdf.



Certificate #4268

Details

Module Name	Ultrastar® DC SN840 NVMe™ PCIe 3.0 Self Encrypting Drive
Standard	FIPS 140-2
Status	Active
Sunset Date	9/21/2026
Overall Level	2
Caveat	None
Security Level Exceptions	• EMI/EMC: Level 3 • Mitigation of Other Attacks: N/A
Module Type	Hardware
Embodiment	Multi-Chip Embedded
Description	The Ultrastar® DC SN840 NVMe™ PCIe 3.0 Self Encrypting Drive, from Western Digital, delivers extreme performance and ultra-low latency to the top tier of enterprise storage. With proven dual-port NVMe architecture, these drives are best suited for performance demanding platforms including HPC servers, misson-critical applications and workloads that require superior read/write performance and low latency.

Approved Algorithms	AES	Certs. #A1025, #C1973, #3580 and #3913
	CKG	vendor affirmed
	DRBG	Cert. #A1025
	ENT	P
	HMAC	Cert. #2280
	PBKDF	Cert. #A1025
	RSA	Certs. #A1025 and #A1184
	SHS	Cert. #2942
Allowed Algorithms	N/A	
Hardware Versions	P/Ns WUS4C6416DSP3X5, WUS4BA119DSP3X5, WUS4C6432DSP3X5, WUS4BA138DSP3X5, WUS4C6464DSP3X5, WUS4BA176DSP3X5 and WUS4BA1A1DSP3X5	
Firmware Versions	R2210400, R2210401 and R2EF0003	

NIST Cryptographic Module Validation Program, Certificate #4268[41]

112. The direct memory access controller of Western Digital's Ultrastar DC SN861 further includes "a means for performing a DMA data transfer, said means for performing a DMA data transfer including at least one DMA engine configured for transferring data." Specifically, the controller chip in Western Digital's Ultrastar DC SN861 includes a DMA engine that performs data transfers directly to and from memory locations within the SSD. *See, e.g.*, Delkin Blog, "Understanding Flash-Based SSD Drives and the Flash Controller,"[42] ("NAND flash controller hardware is made up of multiple parts: . . . Direct Memory and Flash Access: Also known as

[41] Available at https://csrc.nist.gov/projects/cryptographic-module-validation-program/certificate/4268.

[42] Available at https://www.delkin.com/blog/understanding-nand-flash-based-ssd-drives-and-the-flash-controller/.

DMA and DFA, these buffers increase throughput by allowing transfers to and from RAM and flash without intervention from the CPU."); Western Digital Data Sheet, "Ultrastar DC SN861"[43] at 1 ("With high random read speeds and low power consumption, the DC SN861 is optimized for compute-intensive AI and machine learning applications, ensuring superior read/write performance . . . [t]he DC SN861 also provides a rich feature set including NVMe® 2.0 and OCP 2.0 support. . .").

113. The direct memory access controller of Western Digital's Ultrastar DC SN861 further includes "a means for performing data processing coupled to said means for performing a DMA data transfer, said data processing includes encrypting or decrypting said data in response to a DPC hit signal by at least using a DPC channel to intercept said data, causing said data to be transferred to said means for performing data processing." For example, each of the '389 Accused Products includes a cryptographic module or engine that encrypts or decrypts data in response to a DPC hit signal by using a DPC channel of the cryptographic module. *See* Western Digital Blog, "What Are Encrypted Drives?"[44] ("Self-encrypting drives automatically convert stored data into a scrambled, unreadable form known as ciphertext, using an encryption algorithm. This algorithm encrypts created files even before they are physically written onto the device, rendering your storage drive 'encrypted at rest'. While there are many encryption algorithms, AES, the Advanced Encryption Standard, is one of the most widely adopted and recognized modern cryptographic algorithms. This algorithm uses fixed blocks of data, typically 128-bit or 256-bit, and scrambles them using a secret key . . . [a]s soon as a file is created, the algorithm begins encrypting fixed blocks of data in a series of cryptographic operations including substitution, permutation and mixing."). As an example, in the

[43] Available at https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/product/data-center-drives/ultrastar-nvme-series/data-sheet-ultrastar-dc-sn840.pdf.

[44] Available at https://blog.westerndigital.com/what-are-encrypted-drives/.

Opal-compliant '389 Accused Products, such as Western Digital's Ultrastar DC SN861, DPC hit signals are used in the selection of the appropriate media encryption key (MEK) to use for encryption/decryption for a particular locking range of the memory. *See* Trust Computing Group and NVM Express Joint White Paper: "TCG Storage, Opal, and NVMe (Aug. 2015)"[45] at 5 ("Opal SSC provides a full featured device implementation profile, which a variety of features that can be taken advantage of through Opal management software . . . [t]he Storage Device can be subdivided into multiple 'Locking Ranges.' Each of these is a range of continuous LBAs . . . [e]ach Locking Range is encrypted with a different Media Encryption Key . . . [e]ach Locking Range can be unlocked independently of the others."); Johns Hopkins Applied Physics Laboratory, "A Practical Guide to Use of Opal Drives," at iii ("Opal drives are widely deployed media that are a class of self-encrypting drives (SEDs). Based on a specification from the Trusted Computing Group (TCG), such drives have extended characteristics beyond merely self-encrypting. They have the ability to create multiple independent regions each having individual encryption keys, and read/write controls.").

114. All of the '389 Accused Products infringe the '389 Patent, including at least claim 19, in the same or similar manner as the Ultrastar DC SN861.

115. By making, using, offering for sale, and/or selling products in the United States and/or importing products into the United States, including but not limited to the '389 Accused Products, Western Digital has injured BiTMICRO and is liable to BiTMICRO for directly infringing one or more claims of the '389 Patent, including without limitation claim 19 pursuant to 35 U.S.C. § 271(a).

116. On information and belief, Western Digital will continue to infringe the '389 Patent unless enjoined by this Court.

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[45] Available at https://trustedcomputinggroup.org/wp-content/uploads/TCGandNVMe_Joint_White_Paper-TCG_Storage_Opal_and_NVMe_FINAL.pdf.

117. As a result of Western Digital's infringement of the '389 Patent, BiTMICRO has suffered monetary damages, and seeks recovery, in an amount to be proven at trial, adequate to compensate for Western Digital's infringement, but in no event less than a reasonable royalty with interest and costs.

118. Western Digital's infringement of BiTMICRO's rights under the '389 Patent will continue to damage BiTMICRO, causing irreparable harm for which there is no adequate remedy at law, unless enjoined by this Court.

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PRAYER FOR RELIEF

WHEREFORE, BiTMICRO prays for judgment and seeks relief against Western Digital as follows:

A. For judgment that Western Digital has infringed and/or continue to infringe one or more claims of the Asserted Patents;

B. For a permanent injunction against Western Digital and its respective officers, directors, agents, servants, affiliates, employees, divisions, branches, subsidiaries, parents, and all other acting in active concert therewith from infringement of the Asserted Patents;

C. For an accounting of all damages sustained by BiTMICRO as the result of Western Digital's acts of infringement;

D. For a mandatory future royalty payable on each and every future sale by Western Digital of a product that is found to infringe one or more of the Asserted Patents and on all future products which are reasonably similar to those products found to infringe;

E. For a judgment and order finding that Western Digital's infringement is willful and awarding to BiTMICRO enhanced damages pursuant to 35 U.S.C. § 284;

F. For a judgment and order requiring Western Digital to pay BiTMICRO's damages, costs, expenses, and pre- and post-judgment interest for its infringement of the Asserted Patents as provided under 35 U.S.C. § 284;

G. For a judgment and order finding that this is an exceptional case within the meaning of 35 U.S.C. § 285 and awarding to BiTMICRO its reasonable attorneys' fees; and

H. For such other and further relief in law and in equity as the Court may deem just and proper.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure, BiTMICRO hereby demands a trial by jury of this action.

Dated: September 3, 2024

Respectfully submitted,

/s/ Richard C. Lin

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