IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

TURBOCODE LLC, Plaintiff, v. **COOLPAD GROUP LIMITED,** Defendant.	C.A. No. 2:25-cv-00174 **JURY TRIAL DEMANDED** **PATENT CASE**

ORIGINAL COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff TurboCode LLC files this Original Complaint for Patent Infringement against Coolpad Group Limited, and would respectfully show the Court as follows:

I. THE PARTIES

1. Plaintiff TurboCode LLC ("TurboCode" or "Plaintiff") is a Texas limited liability company with its address at 6000 Shepherd Mountain Cove, Suite #1604, Austin, Texas 78730.

2. On information and belief, Defendant Coolpad Group Limited ("Defendant") is a corporation organized and existing under the laws of the Cayman Islands with a place of business at Coolpad Information Harbor, No.2 Mengxi Rd, Hi-Tech Ind Park(Ntrn), Nanshan District, Shenzhen, Guangdong, 518057, China. Coolpad may also be served with process by serving the Texas Secretary of State, 1019 Brazos Street, Austin, Texas 78701, as its agent for service because it engages in business in Texas but has not designated or maintained a resident agent for service of process or a regular place of business in Texas as required by statute. This action arises out of that business.

II. JURISDICTION AND VENUE

3. This action arises under the patent laws of the United States, Title 35 of the United States Code. This Court has subject matter jurisdiction of such action under 28 U.S.C. §§ 1331 and 1338(a).

4. On information and belief, Defendant is subject to this Court's specific and general personal jurisdiction, pursuant to due process and the Texas Long-Arm Statute, due at least to its business in this forum, including at least a portion of the infringements alleged herein.

5. Without limitation, on information and belief, within this state, Defendant used the patented invention thereby committing, and continuing to commit, acts of patent infringement alleged herein. In addition, on information and belief, Defendant derived revenues from its infringing acts occurring within Texas. Further, on information and belief, Defendant is subject to the Court's general jurisdiction, including from regularly doing or soliciting business, engaging in other persistent courses of conduct, and deriving substantial revenue from goods and services provided to persons or entities in Texas. Further, on information and belief, Defendant is subject to the Court's personal jurisdiction at least due to its sale of products and/or services within Texas. Defendant committed such purposeful acts and/or transactions in Texas such that it reasonably should know and expect that it could be haled into this Court as a consequence of such activity.

6. Venue is proper in this district under 28 U.S.C. § 1400(b). On information and belief, from and within this District Defendant has committed at least a portion of the infringements at issue in this case.

7. For these reasons, personal jurisdiction exists and venue is proper in this Court under 28 U.S.C. § 1400(b).

III. COUNT I
(PATENT INFRINGEMENT OF UNITED STATES PATENT NO. 6,813,742)

8. Plaintiff incorporates the above paragraphs herein by reference.

9. On November 2, 2004, the USPTO duly and legally issued U.S. Patent No. 6,813,742 ("the '742 Patent" or "Patent-in-Suit"), entitled "High Speed Turbo Codes Decoder for 3G Using Pipelined SISO Log-Map Decoders Architecture." The '742 patent was the subject of a reexamination request filed on July 13, 2006. An *Ex Parte* Reexamination Certificate was issued for the '742 patent on February 10, 2009. A true and correct copy of the '742 Patent with its *Ex Parte* Reexamination Certificate is attached hereto as Exhibit 1.

10. TurboCode is the assignee of all right, title, and interest in the '742 patent, including all rights to enforce and prosecute actions for infringement and to collect damages for all relevant times against infringers of the '742 Patent. Accordingly, TurboCode possesses the exclusive right and standing to prosecute the present action for infringement of the '742 Patent by Defendant.

11. This case generally relates to decoder architectures and processes for receiving and decoding data in communications devices.

12. **Direct Infringement.** Upon information and belief, Defendant directly infringed claim 6 of the '742 Patent in Texas, and elsewhere in the United States, by performing actions comprising using or performing the claimed method of iteratively decoding a plurality of sequences of received baseband signals by using and/or testing the products, devices, systems, and components of systems that comply with the 4G/LTE standards as disclosed in the 3rd Generation Partnership Project ("3GPP") Standard Specifications (releases 8-13) governing cellular wireless communications and that were or are designed, developed, tested, made, used, offered for sale, sold in the United States, imported into the United States, or that have a nexus to the United States. The Accused Instrumentalities include, but are not limited to, Coolpad Cool 1 Dual Coolpad Cool 2, Coolpad Cool 3 Plus, Coolpad Cool 5, Coolpad Cool M7, Coolpad Cool 20, Coolpad Legacy, Coolpad Note 3 Lite, Coolpad Note 3 Plus, Coolpad Note 3s, Coolpad Note 5, Coolpad Note 5

Lite, Coolpad Note 6, Coolpad Max, Coolpad Mega, Coolpad Mega 3, Coolpad Mega 5A, Coolpad Cool Play 8, Coolpad Cool Play 6, Coolpad Conjr, Coolpad Torino, Coolpad Tornio S, Coolpad Moderna 2, Coolpad Defiant, and Coolpad Porto S ("Accused Instrumentalities"). The products which are listed (together with support indicating that the identified product complies with relevant 4G/LTE standards and contains a baseband processor) and any products reasonably similar thereto (including, *e.g.*, products or model numbers marketed under a substantially similar name or that vary from a listed product by incorporating features that do not alter compliance with 4G/LTE standards). The Accused Instrumentality also extends to all cellular communication equipment, including eNodeBs, base stations, and related systems or devices that conform to the 4G/LTE standards. Defendant's 4G/LTE LTE-based solutions, including small cells, macro cells, and eNodeBs for private and public cellular networks are representative products because it performed iterative decoding in accordance with the 4G/LTE standards disclosed in the 3GPP Standard Specifications as do the Accused Instrumentalities.

13. Claim 6 of the '742 Patent *Ex Parte* Reexamination Certificate states:

> A method of iteratively decoding a plurality of sequences of received baseband signals, the method comprising:
>
> providing an input buffer comprising at least three shift registers, for receiving an input signal and generating first, second, and third shifted input signals;
>
> providing first and second soft decision decoders serially coupled in a circular circuit, wherein each decoder processes soft decision from the preceding decoder output data, and wherein the first decoder further receives the first and second shifted input signals from the input buffer and the second decoder further receives the third shifted input signal from the input buffer;
>
> providing at least one memory module coupled to an output of each of the first and second soft decision decoders, wherein the output of the memory module associated with the second soft decision decoder is fed back as an input of the first soft decision decoder;

processing systematic information data and extrinsic information data using the maximum a posteriori (AP) probability algorithm, and/or logarithm approximation algorithm;

generating soft decision based on the maximum a posteriori (MAP) probability algorithm, and/or logarithm approximation algorithm;

weighing and storing soft decision information into the corresponding memory module;

performing, for a predetermined number of times, iterative decoding from the first to the last of multiple decoders, wherein an output from the last soft decision decoder is fed back as an input to the first soft decision decoder, then from the first to the second decoders, and propagate to the last decoder in a circular circuit.

14. The Accused Instrumentalities provided or performed a method of iteratively decoding a plurality of sequences of received baseband signals, as shown below by their compliance with the 3G and/or 4G/LTE standards disclosed in the 3GPP Standard Specifications:

Coolpad Cool 1 Dual

Brand: Coolpad
Category: Mobiles

- **Processor**: Processor (Clock): Octa-core (4x
- **RAM**: Memory: 3GB/4GB, 993MHz
- **Storage**: Internal Storage: 32GB/64GB
- **Display**: Screen (Size & Type): 5.5 inches IPS,
- **Camera**: Camera Overview: 13 MP + 13 MP / 8
- **Battery**: Non-Removable 4,060 mAh Lithium-ion

Data

4G LTE	Yes
Speed	LTE: 1(2100) / 3(1800) / 5(850) / 7(2600) / 8(900) / 38(2600) / 39(1900) / 40(2300) / 41(2500) MHz

(*E.g.*, https://www.gizmochina.com/product/coolpad-cool-1-dual/).

Coolpad Cool 2

Operating system **Android 7.0**	Display **5.7 inch** 720x1440 pixels	Battery **3200 mAh** Li-Ion
Performance **4GB RAM** MT6750	Camera **13MP** 1080p	Storage **64GB** eMMC 5.1

NETWORK	SIM cards	Dual SIM (Nano-SIM + Nano-SIM)
	VoLTE support	Yes
	Data speed	LTE, HSPA
	2G bands	**GSM:** 850 / 900 / 1800 / 1900 MHz **CDMA:** 800 MHz
	3G bands	**HSPA:** 850 / 900 / 1900 / 2100 MHz
	4G bands	**LTE:** b1 (2100), b3 (1800), b5 (850), b7 (2600), b8 (900), b38 (2600), b39 (1900), b40 (2300), b41 (2500 MHz)

(*E.g.*, https://en.kalvo.com/coolpad-cool-2-39769.html#specs).

Coolpad Cool 3 Plus

Operating system
Android 9.0

Display
5.71 inch
720x1520 pixels

Battery
3000 mAh
Li-Ion

Performance
2/3GB RAM
Helio A22

Camera
13MP
1080p

Storage
16/32GB
eMMC 5.1

NETWORK	SIM cards	Dual SIM (Nano-SIM + Nano-SIM)
	VoLTE support	Yes
	Data speed	LTE Cat4 150/50 Mbps, HSPA 42.2/5.76 Mbps
	2G bands	**GSM:** 850 / 900 / 1800 / 1900 MHz
	3G bands	**HSPA:** 850 / 900 / 1700 / 1900 / 2100 MHz
	4G bands	**LTE:** b1 (2100), b2 (1900), b3 (1800), b4 (1700), b5 (850), b6 (800), b7 (2600), b8 (900), b19 (800), b20 (800), b28 (700 MHz)

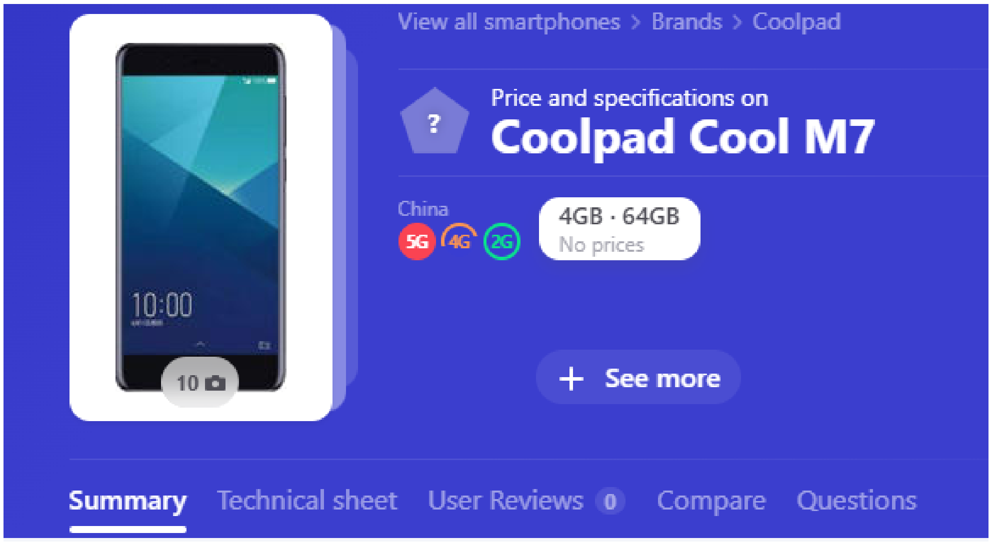
(*E.g.*, https://en.kalvo.com/coolpad-cool-3-plus-1543.html#specs).

Coolpad Cool 5

Operating system Android 9.0	Display 6.22 inch 720x1520 pixels	Battery 4000 mAh Li-Poly
Performance 4GB RAM Helio P22	Camera 13MP 1080p	Storage 64GB eMMC 5.1

NETWORK	SIM cards	Dual SIM (Nano-SIM + Nano-SIM)
	VoLTE support	Yes
	Data speed	LTE Cat4 150/50 Mbps, HSPA 42.2/5.76 Mbps
	2G bands	**GSM:** 850 / 900 / 1800 / 1900 MHz
	3G bands	**HSPA:** 850 / 900 / 2100 MHz
	4G bands	**LTE:** b1 (2100), b2 (1900), b3 (1800), b4 (1700), b5 (850), b7 (2600), b8 (900), b19 (800), b20 (800), b28 (700), b38 (2600), b40 (2300 MHz)

(*E.g.*, https://en.kalvo.com/coolpad-cool-5-1388.html#specs).



Connectivity of Coolpad Cool M7

Bands

4G LTE	B1 (2100), B3 (1800), B5 (850), B7 (2600), B38 (TDD 2600), B39 (TDD 1900), B40 (TDD 2300), B41 (TDD 2500)
3G	B1 (2100), B2 (1900), B5 (850), B8 (900), B10 (1700)
2G	CDMA BC0 (800), B2 (1900), B3 (1800), B5 (850), B8 (900)

(*E.g.*, https://www.kimovil.com/en/where-to-buy-coolpad-cool-m7).

COOLPAD COOL 20

Quick Specs

Android 11, CoolOS 2,

Performance	Display	Camera	Battery
Octa-core (2x2.0 G...	6.52 inches	48 MP	Li-Po 4500 mAh
4GB RAM	720 x 1600 pixels	1080p	

IMEI Check Results

Check your IMEI by selecting a service from the IMEI dropdown menu.

NETWORK	Technology	GSM / CDMA / HSPA / CDMA2000 / LTE
	2g bands	GSM 850 / 900 / 1800 / 1900 CDMA 800
	3g bands	HSDPA 850 / 900 / 2100 CDMA2000 1x
	4g bands	1, 3, 5, 8, 34, 39, 40, 41
	Speed	HSPA 42.2/5.76 Mbps, LTE-A

(*E.g.*, https://devicecheck.us/devices/coolpad-cool-20).

Coolpad Legacy

Info | Photos | News | Forum 3 | Hands-On ›

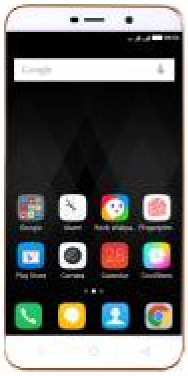
This affordable phone has a premium metal design, huge full-HD screen, fingerprint reader, and dual rear cameras. Other features include USB-C, memory card slot, 3.5mm jack, and FM radio.

Offered By:
Boost *Discontinued*
Metro *Discontinued*

Network Bands	4G LTE: 2, 4, 5, 7, 12, 13, 25, 26, 41, 66, 71 more detail WCDMA: 2, 4, 5 CDMA: 800, 850, 1900 GSM: 850, 900, 1800, 1900 only Boost (Sprint) version supports LTE 13, 25, 26, 41 and CDMA
Data Technology	LTE (Cat 6)

(*E.g.*, https://www.phonescoop.com/phones/phone.php?p=6032).

Coolpad Note 3 Lite



View Photos

Phone	Coolpad Note 3 Lite
Manufacturer	Coolpad
Status	Available
Available in India	Yes
Price (Indian Rupees)	Avg Current Market Price:Rs. 6999 Last Updated On: Place : Chennai Delhi Kolkata Mumbai
Price (USD)	$155.53
Description	Coolpad Note 3 Lite is a Smart Phone powered by Android 5.1 Lollipop with Cool UI 6.0 and a 13MP Auto Focus Camera.

Highlights

- 1.3 GHz MT6735 64-Bit Quad-Core Processor
- 3GB RAM With 16GB ROM
- 5 Inch HD IPS Display
- Dual SIM Support
- 13MP Camera With LED Flash
- 5 MP Front Camera
- 4G LTE
- Bluetooth
- FM Radio
- 2500mAh Battery

(*E.g.*, https://www.fonearena.com/coolpad-note-3-lite_7527.html).

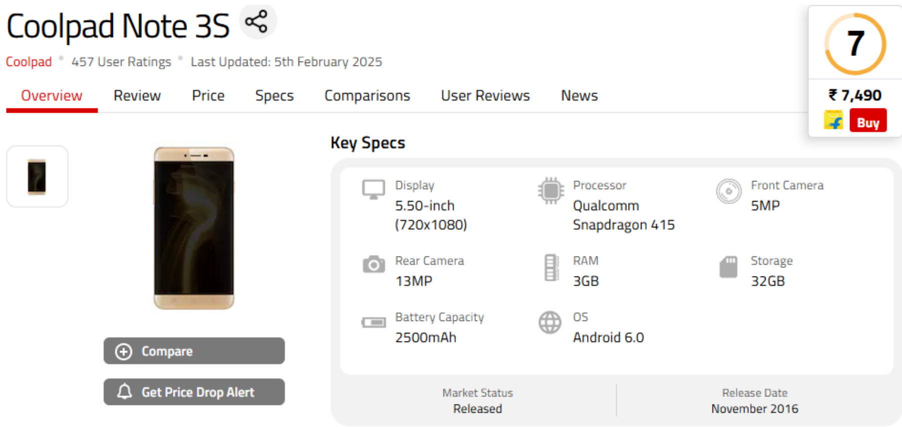
Coolpad Note 3 Plus

Phone	Coolpad Note 3 Plus
Manufacturer	Coolpad
Status	Available
Available in India	Yes
Price (Indian Rupees)	Avg Current Market Price:Rs. 8999 Last Updated On: Place : Chennai Delhi Kolkata Mumbai
Price (USD)	$199.98
Description	Coolpad Note 3 Plus is a Smart Phone powered by Android 5.1 Lollipop with Cool UI 6.0 and 13MP Auto Focus Camera.

Highlights

- 1.3 GHz MTK6753 64-Bit Octa-Core MediaTek Processor
- 3GB RAM With 16GB ROM
- 5.5 Inch FHD IPS Display With Scratch Resistant Glass Protection
- Dual SIM Support
- 13MP Primary Camera With LED Flash
- 5 MP Front Camera
- 4G LTE
- Bluetooth
- FM Radio
- 3000 MAh Batter

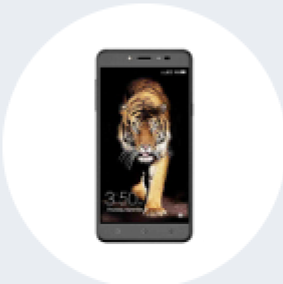
(*E.g.*, https://www.fonearena.com/coolpad-note-3_7792.html).



SIM 1	
SIM Type	Nano-SIM
3G	Yes
4G/ LTE	Yes
Supports 4G in India (Band 40)	Yes
SIM 2	
SIM Type	Nano-SIM
3G	Yes
4G/ LTE	Yes
Supports 4G in India (Band 40)	Yes

(*E.g.*, https://www.gadgets360.com/coolpad-note-3s-3900).

Coolpad Note 5 Review



Popularity

Display

Chipset

Data

2G network	GSM 850 / 900 / 1800 / 1900
3G network	HSDPA 900 / 2100
4G network	LTE 850 / 1800 / 2100 / 2300 / 2500 / 2600
Connectivity	Bluetooth WLAN
USB	Yes, microUSB 2.0

(*E.g.*, https://benchmarks.ul.com/hardware/phone/Coolpad+Note+5+review).

Coolpad Note 5 Lite

Brand: Coolpad
Category: Mobiles

Processor: Processor (Clock): Quad-Core 1.1

RAM: Memory: 3GB, 433 MHz

Storage: Internal Storage: 16GB

Display: Screen (Size & Type): 5.1 inches HD

Camera: Camera Overview: 13 Megapixels / 8

Battery: Non-Removable 2,400 mAh Lithium-Ion

Data

4G LTE	Yes
Speed	LTE : 850 / 1800 / 2100 MHz

(*E.g.*, https://www.gizmochina.com/product/coolpad-note-5-lite/).

Coolpad Note 6

Operating system Android 7.1	Display 5.5 inch 1080x1920 pixels	Battery 4070 mAh Li-Ion
Performance 3/4GB RAM Snapdragon 435	Camera 13MP 1080p	Storage 32/64GB eMMC 5.1

NETWORK	VoLTE support	Yes
	Data speed	LTE, HSPA
	2G bands	**GSM:** 850 / 900 / 1800 / 1900 MHz
	3G bands	**HSPA:** 850 / 900 / 1900 / 2100 MHz
	4G bands	**LTE:** b1 (2100), b3 (1800), b5 (850), b40 (2300 MHz)

(*E.g.*, https://en.kalvo.com/coolpad-note-6-32162.html#specs).

Coolpad Max

Phone	Coolpad Max
Manufacturer	Coolpad
Status	Available
Available in India	Yes
Price (Indian Rupees)	Avg Current Market Price:Rs. 24999 Last Updated On: Place : Chennai Delhi Kolkata Mumbai
Price (USD)	$555.53
Description	Coolpad Max is a Smart Phone powered by Android 5.1 Lollipop with Cool UI and 13MP Auto Focus Camera with LED flash.

Highlights

- 1.5GHz Octa-Core Qualcomm Snapdragon 617 Processor
- 4GB RAM With 64GB ROM
- 5.5 Inch FHD IPS Display
- Hybrid Dual SIM Support
- 13MP Primary Camera With LED Flash
- 5 MP Front Camera
- 4G LTE
- Bluetooth
- FM Radio
- 2800 MAh Batter

(*E.g.*, https://www.fonearena.com/coolpad-max_7816.html).

Coolpad Mega

Brand: Coolpad
Category: Mobiles

Processor: Processor (Clock): Quad-Core 1.0GHz

RAM: Memory: 3GB

Storage: Internal Storage: 16GB

Display: Screen (Size & Type): 5.5 inches HD

Camera: Camera Overview: 8 Megapixels / 8

Battery: Removable Lithium-Ion 2,500 mAh

Data

4G LTE	Yes
Speed	LTE : 850 /1800 MHz LTE-TDD : 2300 MHz

(*E.g.*, https://www.gizmochina.com/product/coolpad-mega/).

The Coolpad Mega 3 Dual SIM LTE supports 4 GSM bands, 3 UMTS bands, and 5 LTE bands. See the tables below for details.

LTE

Name	Interface
B1 (2100 MHz)	LTE
B3 (1800 MHz +)	LTE
B7 (2600 MHz)	LTE
B8 (900 MHz)	LTE
B20 (800 MHz DD)	LTE

Supported LTE Protocols

Name	Generation
LTE	4G
LTE 50/25	4G
LTE 75/25	4G
LTE 100/50	4G
LTE 150/50	4G

(*E.g.*, https://www.frequencycheck.com/models/A5k94/coolpad-mega-3-dual-sim-lte).

Coolpad Mega 5A

Operating system
Android 8.1

Display
5.45 inch
720x1440 pixels

Battery
2500 mAh
Li-Ion

Performance
2GB RAM
Unisoc SC9850K

Camera
8MP
1080p

Storage
16GB

NETWORK	SIM cards	Dual SIM (Nano-SIM + Nano-SIM)
	VoLTE support	Yes
	Data speed	LTE, HSPA
	2G bands	**GSM:** 850 / 900 / 1800 / 1900 MHz **CDMA:** 800 MHz
	3G bands	**HSPA:** 850 / 900 / 1900 / 2100 MHz
	4G bands	**LTE:** b1 (2100), b3 (1800), b5 (850), b40 (2300 MHz)

(*E.g.*, https://en.kalvo.com/coolpad-mega-5a-10362.html#specs).

Coolpad Cool Play 8

Operating system **Android 8.0** Cool UI 9	Display **6.2 inch** 1080x2246 pixels	Battery **4000 mAh** Li-Ion
Performance **4GB RAM** MT6750	Camera **16MP** 1080p	Storage **64GB** eMMC 5.1

NETWORK	VoLTE support	Yes
	Data speed	LTE, HSPA
	2G bands	**GSM**: 850 / 900 / 1800 / 1900 MHz
	3G bands	**HSPA**: 850 / 900 / 1900 / 2100 MHz
	4G bands	**LTE:** b1 (2100), b3 (1800), b5 (850), b40 (2300 MHz)

(*E.g.*, https://en.kalvo.com/coolpad-cool-play-8-1906.html).

Coolpad Cool Play 6 Technical Specifications

5.5"
Screen size

2160p
Camera resolution

6 GB RAM
Memory capacity

13 MP
Camera sensor

64GB storage, no card slot
Storage capacity

4060 mAh Li-Ion
Battery capacity

Network
Specifications

Technology:	GSM / CDMA / HSPA / LTE
2G bands:	GSM 850 / 900 / 1800 / 1900 - SIM 1 & SIM 2,CDMA 800 / 1900 & TD-SCDMA
3G bands:	HSDPA 850 / 900 / 1900 / 2100
4G bands:	1, 3, 5, 7, 8, 38, 39, 40, 41
Speed:	HSPA 42.2/5.76 Mbps, LTE

(*E.g.*, https://imei.org/phone-model-lookup/coolpad-cool-play-6_1945).

Coolpad Conjr

Info | Photos | News | Forum | Hands-On › | Our Review ›

This compact, affordable Android phone sports a 5-inch HD display, 13-megapixel camera, and 8-megapixel front camera with selfie flash. Key features include fingerprint reader, curved-edge front glass, memory card slot, and 3.5mm audio jack.

This phone is not currently available from any major US carrier. It is compatible with at least some US networks, and may be available unlocked from third-party retailers, and/or from smaller service brands.

Network Bands	4G LTE: 2, 4, 5, 7, 12 WCDMA: 1, 2, 4, 5 GSM: 850, 900, 1800, 1900	more detail

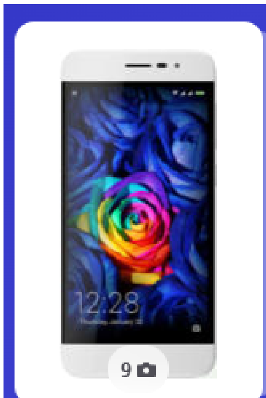
(*E.g.*, https://www.phonescoop.com/phones/phone.php?p=5388).

Coolpad Torino - description and parameters

Coolpad Torino supports frequency bands GSM , HSPA , LTE. Official announcement date is July 2016. The device is working on an Android OS, v5.1 (Lollipop) with a Octa-core (4x1.36 GHz Cortex-A53 & 4x1.0 GHz Cortex-A53) processor and 3 GB RAM memory. Coolpad Torino has 16 GB of internal memory. This device has a Qualcomm MSM8952 Snapdragon 617 chipset. The main screen size is 5.5 inches with 720 x 1280 pixels resolution. It has a 267 ppi pixel density. The screen covers about 70.8% of the device's body. This screen to body ratio is a very impressive

Network, supported bands and technologies	Technology	GSM / HSPA / LTE
	2G bands	GSM 900 / 1800 / 1900 - SIM 1 & SIM 2
	3G bands	HSDPA 900 / 2100
	4G bands	LTE band 1(2100), 3(1800), 7(2600), 20(800)
	Speed	HSPA, LTE Cat4 150/50 Mbps
	GPRS	Yes
	EDGE	Yes

(*E.g.*, https://imei24.com/description/Coolpad/Torino/).



View all smartphones > Brands > Coolpad

Price and specifications on
Coolpad Torino S

China
5G 4G 2G

2GB · 16GB
No prices

See more

Connectivity of Coolpad Torino S

Bands

4G LTE	B1 (2100), B3 (1800)
3G	B1 (2100), B8 (900)
2G	B2 (1900), B3 (1800), B8 (900)

(*E.g.*, https://www.kimovil.com/en/where-to-buy-coolpad-torino-s).

Coolpad Modena 2

The Coolpad Modena 2 released on Sep-2016 at price $ 72 in USA.

Specifications Reviews Compare

5.5 INCHES SCREEN
8 MP REAR CAMERA
2GB RAM + 16GB
2500 MAH BATTERY
ANDROID 6 (MARSHMALLOW), COOL UI 8
MALI-T720MP2

Buy on Amazon

Disclosure: As an Amazon Associate, I earn from qualifying purchases. This means th
a link to Amazon and make a purchase, I may receive a small commission at no extra

NETWORK	
Technology	GSM / HSPA / LTE
2G Band	GSM 900 / 1800 / 1900 - SIM 1 & SIM 2
3G Band	HSDPA 900 / 2100
4G Band	1, 3, 7, 8, 20

(*E.g.*, https://us.mobilekishop.net/product/coolpad-modena-2).

Coolpad Defiant

Info | Photos | News | Forum | Our Review ›

This update to the Catalyst has a faster processor and larger battery, but is otherwise similar. Key features of this affordable Android phone include a 5-inch screen, 5-megapixel camera, front camera, memory card slot, and a 3.5mm audio jack.

Offered By:
Metro *Discontinued*
T-Mobile *Discontinued*

1 of 3

Network Bands	4G LTE: 2, 4, 5, 12 WCDMA: 2, 4, 5 GSM: 850, 900, 1800, 1900	more detail

(*E.g.*, https://www.phonescoop.com/phones/phone.php?p=5507).

Coolpad Porto S - description and parameters

Coolpad Porto S - description and parameters

Coolpad Porto S supports frequency bands GSM , HSPA , LTE. Official announcement date is January 2016. The device is working on an Android OS, v5.1 (Lollipop) with a Quad-core 1.0 GHz Cortex-A53 processor and 1 GB RAM memory. Coolpad Porto S has 8 GB of internal memory. This device has a Mediatek MT6735P chipset. The main screen size is 5.0 inches with 720 x 1280 pixels resolution. It has a 294 ppi pixel density. The screen covers about 66.9% of the device's body. The result is quite good.

Network, supported bands and technologies	Technology	GSM / HSPA / LTE
	2G bands	GSM 900 / 1800 / 1900 - SIM 1 & SIM 2
	3G bands	HSDPA 900 / 2100
	4G bands	LTE band 1(2100), 3(1800), 7(2600), 20(800)
	Speed	HSPA, LTE Cat4 150/50 Mbps
	GPRS	Yes
	EDGE	Yes

(*E.g.*, https://imei24.com/description/Coolpad/Porto_S/).

15. The Accused Instrumentalities provided or performed a method of iteratively decoding a plurality of sequences of received baseband signals in accordance with the 4G/LTE standards disclosed in the 3GPP Standard Specifications.

5 Channel coding, multiplexing and interleaving

Data and control streams from/to MAC layer are encoded /decoded to offer transport and control services over the radio transmission link. Channel coding scheme is a combination of error detection, error correcting, rate matching, interleaving and transport channel or control information mapping onto/splitting from physical channels.

5.1.3 Channel coding

The bit sequence input for a given code block to channel coding is denoted by $c_0, c_1, c_2, c_3, \ldots, c_{K-1}$, where K is the number of bits to encode. After encoding the bits are denoted by $d_0^{(i)}, d_1^{(i)}, d_2^{(i)}, d_3^{(i)}, \ldots, d_{D-1}^{(i)}$, where D is the number of encoded bits per output stream and i indexes the encoder output stream. The relation between c_k and $d_k^{(i)}$ and between K and D is dependent on the channel coding scheme.

The following channel coding schemes can be applied to TrCHs:

- tail biting convolutional coding;
- turbo coding.

Usage of coding scheme and coding rate for the different types of TrCH is shown in table 5.1.3-1. Usage of coding scheme and coding rate for the different control information types is shown in table 5.1.3-2.

Usage of coding scheme and coding rate for the different types of TrCH is shown in table 5.1.3-1. Usage of coding scheme and coding rate for the different control information types is shown in table 5.1.3-2.

The values of D in connection with each coding scheme:

- tail biting convolutional coding with rate 1/3: $D = K$;
- turbo coding with rate 1/3: $D = K + 4$.

The range for the output stream index i is 0, 1 and 2 for both coding schemes.

Table 5.1.3-1: Usage of channel coding scheme and coding rate for TrCHs

TrCH	Coding scheme	Coding rate
UL-SCH	Turbo coding	1/3
DL-SCH		
PCH		
MCH		
SL-SCH		
SL-DCH		
BCH	Tail biting convolutional coding	1/3
SL-BCH		

(*See* 3GPP TS 136 212 V17.1.0 (Page:10, Section 5).

5.1.3.2 Turbo coding

5.1.3.2.1 Turbo encoder

The scheme of turbo encoder is a Parallel Concatenated Convolutional Code (PCCC) with two 8-state constituent encoders and one turbo code internal interleaver. The coding rate of turbo encoder is 1/3. The structure of turbo encoder is illustrated in figure 5.1.3-2.

The transfer function of the 8-state constituent code for the PCCC is:

$$G(D) = \left[1, \frac{g_1(D)}{g_0(D)}\right],$$

where

$$g_0(D) = 1 + D^2 + D^3,$$

5.1.3.2.3 Turbo code internal interleaver

The bits input to the turbo code internal interleaver are denoted by $c_0, c_1, \ldots, c_{K-1}$, where K is the number of input bits. The bits output from the turbo code internal interleaver are denoted by $c'_0, c'_1, \ldots, c'_{K-1}$.

The relationship between the input and output bits is as follows:

$$c'_i = c_{\Pi(i)},\ i=0, 1\ldots, (K\text{-}1)$$

where the relationship between the output index i and the input index $\Pi(i)$ satisfies the following quadratic form:

$$\Pi(i) = \left(f_1 \cdot i + f_2 \cdot i^2\right) \bmod K$$

The parameters f_1 and f_2 depend on the block size K and are summarized in Table 5.1.3-3.

(*See* 3GPP TS 136 212 V17.1.0 (Page:10, Section 5).

16. Based on information and belief, each of the Accused Instrumentalities processed received baseband digital signals in an iterative manner. The standard discloses that Turbo coding shall be used for transport blocks. The Turbo encoder consists of two 8-state constituent encoders and an internal interleaver. This means that in LTE, transport blocks at the eNodeB (Defendant's products) are encoded using Turbo coding, which consists of two constituent encoders and an interleaver. Products based on an eNodeB perform Turbo encoding at the transmitter side before sending data to the UE (User Equipment), where the Turbo decoding process occurs on the UE side, or vice versa. However, in cases where the eNodeB receives the encoded data from the UE,

it performs Turbo decoding to retrieve the original information. The eNodeB also interacts with the UE's iterative decoding through HARQ (Hybrid Automatic Repeat Request), which is a form of iterative transmission and decoding feedback. Thus, for mapping to Coolpad, we can link the Turbo encoding process at the eNodeB with the iterative Turbo decoding process at the UE and vice versa, showing how the transmitted data is encoded iteratively at the eNodeB and then decoded iteratively at the UE.

17. The Accused Instrumentalities provided processing of systematic information data and extrinsic information data using the maximum a posteriori (MAP) probability algorithm.

5.1.3.2 Turbo coding

5.1.3.2.1 Turbo encoder

The scheme of turbo encoder is a Parallel Concatenated Convolutional Code (PCCC) with two 8-state constituent encoders and one turbo code internal interleaver. The coding rate of turbo encoder is 1/3. The structure of turbo encoder is illustrated in figure 5.1.3-2.

The transfer function of the 8-state constituent code for the PCCC is:

$$G(D) = \left[1, \frac{g_1(D)}{g_0(D)}\right],$$

where

$$g_0(D) = 1 + D^2 + D^3,$$

(*See* 3GPP TS 136 212 V17.1.0 (Page:14, Section 5.1.3.2)).

$$g_1(D) = 1 + D + D^3.$$

The initial value of the shift registers of the 8-state constituent encoders shall be all zeros when starting to encode the input bits.

The output from the turbo encoder is

$$d_k^{(0)} = x_k$$

$$d_k^{(1)} = z_k$$

$$d_k^{(2)} = z'_k$$

for $k = 0,1,2,\ldots, K-1$.

If the code block to be encoded is the 0-th code block and the number of filler bits is greater than zero, i.e., $F > 0$, then the encoder shall set c_k, = 0, $k = 0,\ldots,(F\text{-}1)$ at its input and shall set $d_k^{(0)} = \lt NULL \gt$, $k = 0,\ldots,(F\text{-}1)$ and $d_k^{(1)} = \lt NULL \gt$, $k = 0,\ldots,(F\text{-}1)$ at its output.

The bits input to the turbo encoder are denoted by $c_0, c_1, c_2, c_3, \ldots c_{K-1}$, and the bits output from the first and second 8-state constituent encoders are denoted by $z_0, z_1, z_2, z_3, \ldots, z_{K-1}$ and $z'_0, z'_1, z'_2, z'_3, \ldots, z'_{K-1}$, respectively. The bits output from the turbo code internal interleaver are denoted by $c'_0, c'_1, \ldots c'_{K-1}$, and these bits are to be the input to the second 8-state constituent encoder.

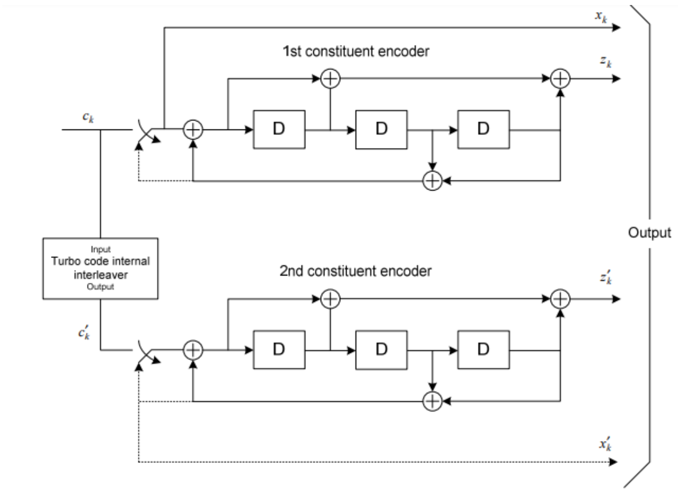


Figure 5.1.3-2: Structure of rate 1/3 turbo encoder (dotted lines apply for trellis termination only)

(*See* 3GPP TS 136 212 V17.1.0 (Page:14, Section 5.1.3.2)).

5.2.3.3 Physical Layer Implementation

The parameters of the physical layer simulation were set according to the parameters for a DCH in multipath fading conditions given in [9] for the downlink and [10] for the uplink. The TB size is 928 bits and the Turbo decoder uses the Log-MAP algorithm with 4 iterations. The rake receiver has 6 fingers at 60 possible positions.

The different channel conditions given in Tables 2, 3 and 4 were extracted from [18] (Selection procedures for the choice of radio transmission technologies of the UMTS).

(*See* 3GPP TR 126 935 V16.0.0 (Page: 15, Section 5.2.3.3).

18. Additionally, and alternatively, as discussed above, each of the Accused Instrumentalities processed received baseband digital signals in an iterative manner through its implementation of turbo encoding/decoding. Further, the soft decision generation using MAP or Log-MAP algorithm is a fundamental part of turbo encoding/decoding, which directly corresponds to the turbo encoder structure defined in 5.1.3.2.1. The MAP algorithm operates on the encoded bits generated by the 8-state constituent encoders and utilizes the interleaved parity bits for iterative decoding. While Turbo decoding is not explicitly covered in TS 36.212, the Turbo encoder structure (Section 5.1.3.2) forms the foundation for soft decision generation using MAP/Log-MAP. The claim element is mappable because the MAP-based soft decision decoding inherently relies on the encoded bit streams defined in TS 36.212

19. The Accused Instrumentalities included various 4G solutions, and products are designed to comply with LTE standards, which typically employ Turbo coding for error correction. Turbo decoding in these standards commonly utilizes the Maximum a Posteriori (MAP) probability algorithm or its logarithmic approximation (Log-MAP) to generate soft decisions

5 Channel coding, multiplexing and interleaving

Data and control streams from/to MAC layer are encoded /decoded to offer transport and control services over the radio transmission link. Channel coding scheme is a combination of error detection, error correcting, rate matching, interleaving and transport channel or control information mapping onto/splitting from physical channels.

5.1.3.2 Turbo coding

5.1.3.2.1 Turbo encoder

The scheme of turbo encoder is a Parallel Concatenated Convolutional Code (PCCC) with two 8-state constituent encoders and one turbo code internal interleaver. The coding rate of turbo encoder is 1/3. The structure of turbo encoder is illustrated in figure 5.1.3-2.

The transfer function of the 8-state constituent code for the PCCC is:

$$G(D) = \left[1, \frac{g_1(D)}{g_0(D)}\right],$$

where

$$g_0(D) = 1 + D^2 + D^3,$$

$$g_1(D) = 1 + D + D^3.$$

The initial value of the shift registers of the 8-state constituent encoders shall be all zeros when starting to encode the input bits.

The output from the turbo encoder is

$$d_k^{(0)} = x_k$$

$$d_k^{(1)} = z_k$$

$$d_k^{(2)} = z'_k$$

for $k = 0,1,2,..., K-1$.

If the code block to be encoded is the 0-th code block and the number of filler bits is greater than zero, i.e., $F > 0$, then the encoder shall set c_k, = 0, $k = 0,\ldots,(F\text{-}1)$ at its input and shall set $d_k^{(0)} = <NULL>$, $k = 0,\ldots,(F\text{-}1)$ and $d_k^{(1)} = <NULL>$, $k = 0,\ldots,(F\text{-}1)$ at its output.

The bits input to the turbo encoder are denoted by $c_0, c_1, c_2, c_3, \ldots, c_{K-1}$, and the bits output from the first and second 8-state constituent encoders are denoted by $z_0, z_1, z_2, z_3, \ldots, z_{K-1}$ and $z'_0, z'_1, z'_2, z'_3, \ldots, z'_{K-1}$, respectively. The bits output from the turbo code internal interleaver are denoted by $c'_0, c'_1, \ldots, c'_{K-1}$, and these bits are to be the input to the second 8-state constituent encoder.

(*See* 3GPP TS 136 212 V17.1.0 (Page:14, Section).

5.2.3.3 Physical Layer Implementation

The parameters of the physical layer simulation were set according to the parameters for a DCH in multipath fading conditions given in [9] for the downlink and [10] for the uplink. The TB size is 928 bits and the Turbo decoder uses the Log-MAP algorithm with 4 iterations. The rake receiver has 6 fingers at 60 possible positions.

The different channel conditions given in Tables 2, 3 and 4 were extracted from [18] (Selection procedures for the choice of radio transmission technologies of the UMTS).

(*See* 3GPP TR 126 935 V16.0.0 (Page: 15, Section 5.2.3.3)).

20. The Accused Instrumentalities implemented a Turbo encoder as specified in ETSI TS 36.212, which generates systematic and parity bits. While TS 36.212 does not explicitly disclose the Turbo decoder, Turbo decoding is commonly performed using the Maximum a Posteriori (MAP) probability algorithm and/or its logarithmic approximation (Log-MAP) to generate soft decisions. Given that Turbo encoding inherently requires a corresponding Turbo decoding process for proper data recovery, it is reasonable to infer that the Accused Instrumentalities utilized a MAP-based and/or Log-MAP-based decoding algorithm to generate soft decisions, which aligns with the claim element.

21. The Accused Instrumentalities included weighting and storing soft decision information into the corresponding memory module (*e.g.*, “Interleaver”).

5.1.4 Rate matching

5.1.4.1 Rate matching for turbo coded transport channels

The rate matching for turbo coded transport channels is defined per coded block and consists of interleaving the three information bit streams $d_k^{(0)}$, $d_k^{(1)}$ and $d_k^{(2)}$, followed by the collection of bits and the generation of a circular buffer as depicted in Figure 5.1.4-1. The output bits for each code block are transmitted as described in clause 5.1.4.1.2.

(*See* 3GPP TS 136 212 V17.1.0 (Page:17, Section 5.1.4)).

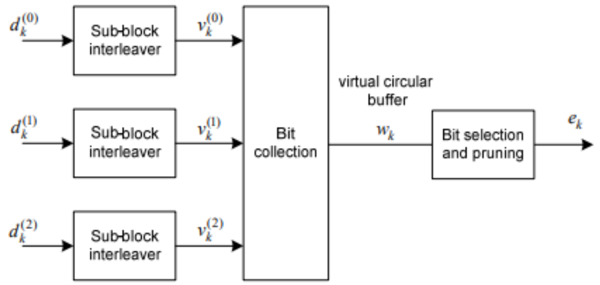


Figure 5.1.4-1. Rate matching for turbo coded transport channels

The bit stream $d_k^{(0)}$ is interleaved according to the sub-block interleaver defined in clause 5.1.4.1.1 with an output sequence defined as $v_0^{(0)}, v_1^{(0)}, v_2^{(0)}, \ldots, v_{K_\Pi - 1}^{(0)}$ and where K_Π is defined in clause 5.1.4.1.1.

The bit stream $d_k^{(1)}$ is interleaved according to the sub-block interleaver defined in clause 5.1.4.1.1 with an output sequence defined as $v_0^{(1)}, v_1^{(1)}, v_2^{(1)}, \ldots, v_{K_\Pi - 1}^{(1)}$.

The bit stream $d_k^{(2)}$ is interleaved according to the sub-block interleaver defined in clause 5.1.4.1.1 with an output sequence defined as $v_0^{(2)}, v_1^{(2)}, v_2^{(2)}, \ldots, v_{K_\Pi - 1}^{(2)}$.

The sequence of bits e_k for transmission is generated according to clause 5.1.4.1.2.

(*See* 3GPP TS 136 212 V17.1.0 (Page:17, Section 5.1.4)).

5.1.4.1.2 Bit collection, selection and transmission

The circular buffer of length $K_w = 3K_\Pi$ for the *r*-th coded block is generated as follows:

$$w_k = v_k^{(0)} \text{ for } k = 0,\ldots, K_\Pi - 1$$

$$w_{K_\Pi + 2k} = v_k^{(1)} \quad \text{for } k = 0,\ldots, K_\Pi - 1$$

$$w_{K_\Pi + 2k + 1} = v_k^{(2)} \quad \text{for } k = 0,\ldots, K_\Pi - 1$$

Denote the soft buffer size for the transport block by N_{IR} bits and the soft buffer size for the *r*-th code block by N_{cb} bits. The size N_{cb} is obtained as follows, where C is the number of code blocks computed in clause 5.1.2:

- $N_{cb} = \min\left(\left\lfloor \frac{N_{IR}}{C} \right\rfloor, K_w\right)$ for DL-SCH and PCH transport channels
- $N_{cb} = K_w$ for UL-SCH, MCH, SL-SCH and SL-DCH transport channels

(*See* 3GPP TS 136 212 V17.1.0 (Page:19, Section 5.1.4.1.2)).

6.2.5 HARQ FEC decoder

The HARQ decoder combines the demodulated and deinterleaved data signal with previously transmitted redundancy versions. For this operation it applies a two stage rate matching scheme and performs turbo decoding of the combined soft-information.

To speed up the MSD reception in adverse transmission conditions, the HARQ decoding is performed for partially received messages, starting from the second redundancy version, *rv*1. Decoding is then attempted after reception of each of the three data parts of the MSD frame (see clause 5.1.5). The decoding attempts based on partial messages is beneficial since, in many cases, the correct MSD can be decoded already after the incremental redundancy contained in the first data part D1 of *rv*1. Figure 18 summarizes the decoder algorithm.

After MSD data bits are decoded, a descrambling operation as described in clause 5.1.2 applies.

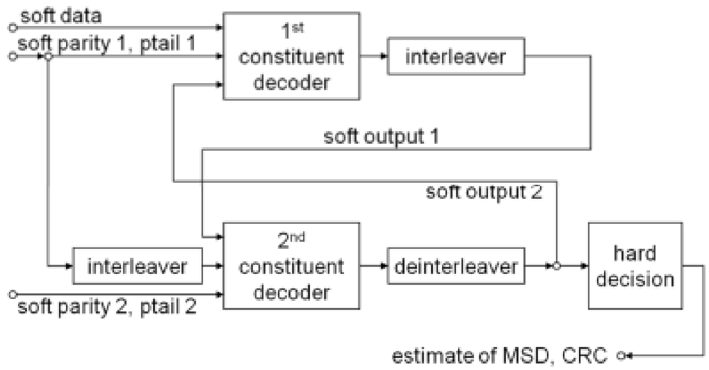


Figure 18: Turbo decoder

(*See* 3gpp TS 126 267 V17.0.0 (Page: 25, Section 6.2.5)).

22. The Accused Instrumentalities implemented a Turbo encoder as defined in TS 36.212, where systematic and parity bits are stored in interleaving buffers before transmission. Although TS 36.212 does not explicitly disclose soft decision weighting and storage, Turbo decoding—typically used to decode Turbo-encoded data—employs soft decision weighting based on Log-Likelihood Ratios (LLRs) and stores the weighted information in memory modules for iterative decoding. Given that Turbo encoding in TS 36.212 inherently requires corresponding Turbo decoding, it is reasonable to infer that the Accused Instrumentalities implemented soft decision weighting and storage in compliance with industry-standard Turbo decoding methods.

23. The Accused Instrumentalities performed iterative decoding a predetermined number of times, from the first to the last of multiple decoders, where the output from the last soft

decision decoder is fed back as input to the first soft decision decoder (*e.g.*, during the Turbo coding/decoding process).

5.1.3.2 Turbo coding

5.1.3.2.1 Turbo encoder

The scheme of turbo encoder is a Parallel Concatenated Convolutional Code (PCCC) with two 8-state constituent encoders and one turbo code internal interleaver. The coding rate of turbo encoder is 1/3. The structure of turbo encoder is illustrated in figure 5.1.3-2.

The transfer function of the 8-state constituent code for the PCCC is:

$$G(D) = \left[1, \frac{g_1(D)}{g_0(D)}\right],$$

where

$$g_0(D) = 1 + D^2 + D^3,$$

$$g_1(D) = 1 + D + D^3.$$

The initial value of the shift registers of the 8-state constituent encoders shall be all zeros when starting to encode the input bits.

The output from the turbo encoder is

$$d_k^{(0)} = x_k$$

$$d_k^{(1)} = z_k$$

$$d_k^{(2)} = z'_k$$

for $k = 0,1,2,..., K-1$.

If the code block to be encoded is the 0-th code block and the number of filler bits is greater than zero, i.e., $F > 0$, then the encoder shall set $c_k = 0$, $k = 0,\ldots,(F\text{-}1)$ at its input and shall set $d_k^{(0)} = <NULL>$, $k = 0,\ldots,(F\text{-}1)$ and $d_k^{(1)} = <NULL>$, $k = 0,\ldots,(F\text{-}1)$ at its output.

The bits input to the turbo encoder are denoted by $c_0, c_1, c_2, c_3, \ldots c_{K-1}$, and the bits output from the first and second 8-state constituent encoders are denoted by $z_0, z_1, z_2, z_3, \ldots, z_{K-1}$ and $z'_0, z'_1, z'_2, z'_3, \ldots, z'_{K-1}$, respectively. The bits output from the turbo code internal interleaver are denoted by $c'_0, c'_1, \ldots c'_{K-1}$, and these bits are to be the input to the second 8-state constituent encoder.

(*See* 3GPP TR 126 935 V16.0.0 (Page: 14, Section 5.1.3.2)).

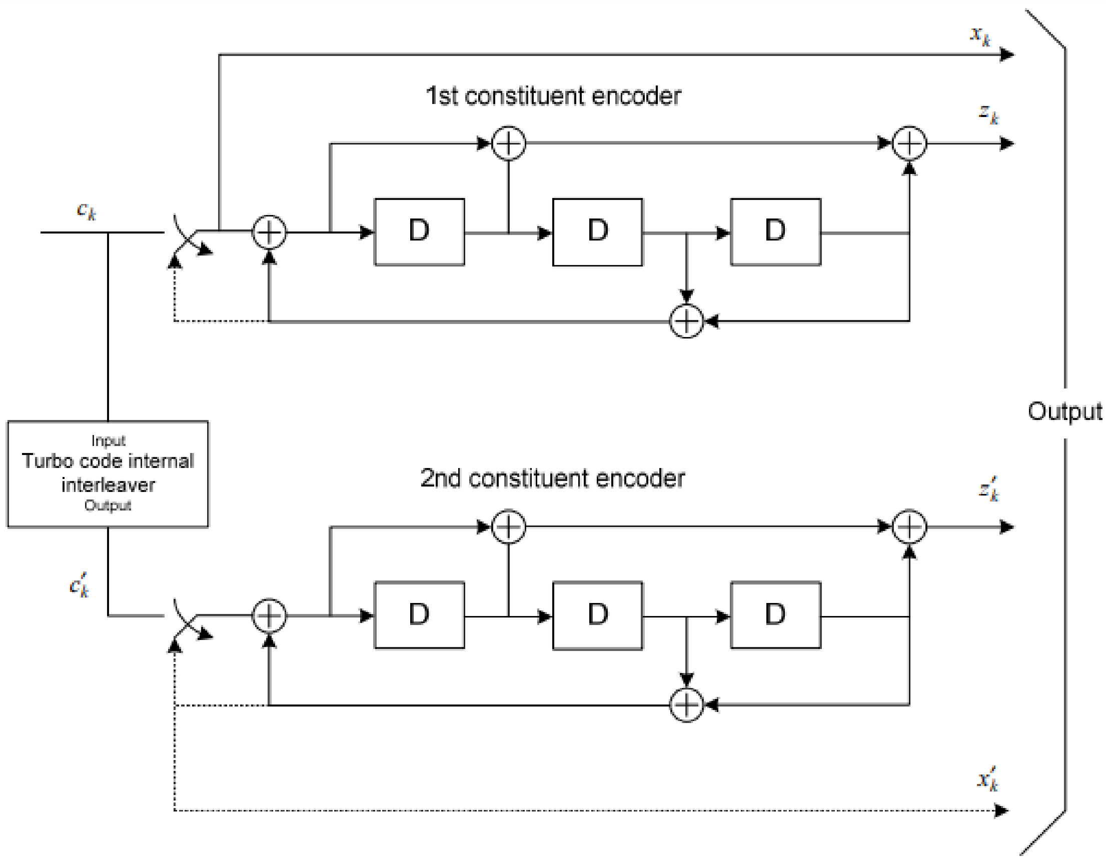


Figure 5.1.3-2: Structure of rate 1/3 turbo encoder (dotted lines apply for trellis termination only)

5.1.3.2.2 Trellis termination for turbo encoder

Trellis termination is performed by taking the tail bits from the shift register feedback after all information bits are encoded. Tail bits are padded after the encoding of information bits.

The first three tail bits shall be used to terminate the first constituent encoder (upper switch of figure 5.1.3-2 in lower position) while the second constituent encoder is disabled. The last three tail bits shall be used to terminate the second constituent encoder (lower switch of figure 5.1.3-2 in lower position) while the first constituent encoder is disabled.

The transmitted bits for trellis termination shall then be:

$$d_K^{(0)} = x_K,\ d_{K+1}^{(0)} = z_{K+1},\ d_{K+2}^{(0)} = x'_K,\ d_{K+3}^{(0)} = z'_{K+1}$$

$$d_K^{(1)} = z_K,\ d_{K+1}^{(1)} = x_{K+2},\ d_{K+2}^{(1)} = z'_K,\ d_{K+3}^{(1)} = x'_{K+2}$$

$$d_K^{(2)} = x_{K+1},\ d_{K+1}^{(2)} = z_{K+2},\ d_{K+2}^{(2)} = x'_{K+1},\ d_{K+3}^{(2)} = z'_{K+2}$$

(*See* 3GPP TR 126 935 V16.0.0 (Page: 14, Section 5.1.3.2)).

5.1.3.2.3 Turbo code internal interleaver

The bits input to the turbo code internal interleaver are denoted by $c_0, c_1, \ldots, c_{K-1}$, where K is the number of input bits. The bits output from the turbo code internal interleaver are denoted by $c'_0, c'_1, \ldots, c'_{K-1}$.

The relationship between the input and output bits is as follows:

$$c'_i = c_{\Pi(i)},\ i=0,\ 1\ldots,\ (K\text{-}1)$$

where the relationship between the output index i and the input index $\Pi(i)$ satisfies the following quadratic form:

$$\Pi(i) = \left(f_1 \cdot i + f_2 \cdot i^2\right) \bmod K$$

The parameters f_1 and f_2 depend on the block size K and are summarized in Table 5.1.3-3.

Table 5.1.3-3: Turbo code internal interleaver parameters

i	*K*	f_1	f_2	*i*	*K*	f_1	f_2	*i*	*K*	f_1	f_2	*i*	*K*	f_1	f_2
1	40	3	10	48	416	25	52	95	1120	67	140	142	3200	111	240
2	48	7	12	49	424	51	106	96	1152	35	72	143	3264	443	204
3	56	19	42	50	432	47	72	97	1184	19	74	144	3328	51	104
4	64	7	16	51	440	91	110	98	1216	39	76	145	3392	51	212
5	72	7	18	52	448	29	168	99	1248	19	78	146	3456	451	192
6	80	11	20	53	456	29	114	100	1280	199	240	147	3520	257	220
7	88	5	22	54	464	247	58	101	1312	21	82	148	3584	57	336
8	96	11	24	55	472	29	118	102	1344	211	252	149	3648	313	228
9	104	7	26	56	480	89	180	103	1376	21	86	150	3712	271	232
10	112	41	84	57	488	91	122	104	1408	43	88	151	3776	179	236
11	120	103	90	58	496	157	62	105	1440	149	60	152	3840	331	120
12	128	15	32	59	504	55	84	106	1472	45	92	153	3904	363	244
13	136	9	34	60	512	31	64	107	1504	49	846	154	3968	375	248

(*See* 3GPP TR 126 935 V16.0.0 (Page: 14, Section 5.1.3.2)).

6.2.5 HARQ FEC decoder

The HARQ decoder combines the demodulated and deinterleaved data signal with previously transmitted redundancy versions. For this operation it applies a two stage rate matching scheme and performs turbo decoding of the combined soft-information.

To speed up the MSD reception in adverse transmission conditions, the HARQ decoding is performed for partially received messages, starting from the second redundancy version, *rv*1. Decoding is then attempted after reception of each of the three data parts of the MSD frame (see clause 5.1.5). The decoding attempts based on partial messages is beneficial since, in many cases, the correct MSD can be decoded already after the incremental redundancy contained in the first data part D1 of *rv*1. Figure 18 summarizes the decoder algorithm.

After MSD data bits are decoded, a descrambling operation as described in clause 5.1.2 applies.

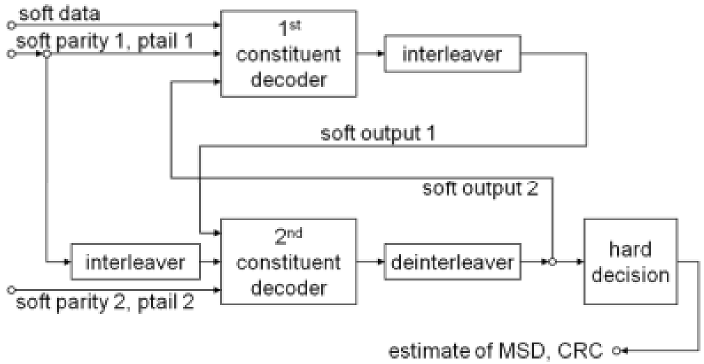


Figure 18: Turbo decoder

(*See* 3GPP TS 126 267 V17.0.0 (Page: 25, Section 6.2.5)).

24. HARQ employs a two-stage rate matching scheme and turbo decoding to combine soft information from different versions of the transmission, aligning with the concept of iterative decoding and feedback between decoders. The Accused Instrumentalities' claim of iterative decoding with feedback between decoders in a circular circuit can be mapped to sections of TS 36.212 that describe the Turbo encoder structure (Section 5.1.3.2.1), trellis termination (Section 5.1.3.2.2), and the internal interleaver (Section 5.1.3.2.3), although decoding itself is not explicitly detailed in the standard. While TS 36.212 primarily focuses on Turbo encoding and the interleaving process, the iterative nature of encoding, involving feedback loops and interleaving, conceptually mirrors the iterative decoding process used in Turbo codes. Specifically, the iterative refinement of soft decisions and feedback to previous stages in the decoding process aligns with

the circular feedback mechanism described in the claim. Thus, while Turbo decoding is not disclosed in the standard, the iterative structure and feedback loops inherent in Turbo encoding provide a basis for mapping to the claim.

25. Plaintiff has been damaged as a result of Defendant's infringing conduct. Defendant is thus liable to Plaintiff for damages in an amount that adequately compensates Plaintiff for such Defendant's infringement of the '742 Patent, *i.e.*, in an amount that by law cannot be less than would constitute a reasonable royalty for the use of the patented technology, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

26. On information and belief, Defendant has had at least constructive notice of the '742 patent by operation of law and, to the extent required (no marking is required for method claims), marking requirements have been complied with.

IV. JURY DEMAND

Plaintiff, under Rule 38 of the Federal Rules of Civil Procedure, requests a trial by jury of any issues so triable by right.

V. PRAYER FOR RELIEF

WHEREFORE, Plaintiff respectfully requests that the Court find in its favor and against Defendant, and that the Court grant Plaintiff the following relief:

a. Judgment that one or more claims of United States Patent No. 6,813,742 have been infringed, either literally and/or under the doctrine of equivalents, by Defendant;

b. Judgment that Defendant account for and pay to Plaintiff all damages to and costs incurred by Plaintiff because of Defendant's infringing activities and other conduct complained of herein;

c. That Plaintiff be granted pre-judgment and post-judgment interest on the damages caused by Defendant's infringing activities and other conduct complained of herein; and

d. That Plaintiff be granted such other and further relief as the Court may deem just and proper under the circumstances.

February 13, 2025

DIRECTION IP LAW

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