IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

TURBOCODE LLC, Plaintiff, v. **ACER INC.,** Defendant.	C.A. No. 2:25-cv-00175 **JURY TRIAL DEMANDED** **PATENT CASE**

ORIGINAL COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff TurboCode LLC files this Original Complaint for Patent Infringement against Acer Inc., and would respectfully show the Court as follows:

I. THE PARTIES

1. Plaintiff TurboCode LLC ("TurboCode" or "Plaintiff") is a Texas limited liability company with its address at 6000 Shepherd Mountain Cove, Suite #1604, Austin, Texas 78730.

2. On information and belief, Defendant Acer Inc. ("Defendant") is a corporation organized and existing under the laws of Taiwan with a place of business at 8F, No. 88, Section 1, Xin Tai 5th Road, Xizhi, New Taipei City 221, Taiwan. Acer may also be served with process by serving the Texas Secretary of State, 1019 Brazos Street, Austin, Texas 78701, as its agent for service because it engages in business in Texas but has not designated or maintained a resident agent for service of process or a regular place of business in Texas as required by statute. This action arises out of that business.

II. JURISDICTION AND VENUE

3. This action arises under the patent laws of the United States, Title 35 of the United States Code. This Court has subject matter jurisdiction of such action under 28 U.S.C. §§ 1331 and 1338(a).

4. On information and belief, Defendant is subject to this Court's specific and general personal jurisdiction, pursuant to due process and the Texas Long-Arm Statute, due at least to its business in this forum, including at least a portion of the infringements alleged herein.

5. Without limitation, on information and belief, within this state, Defendant used the patented invention thereby committing, and continuing to commit, acts of patent infringement alleged herein. In addition, on information and belief, Defendant derived revenues from its infringing acts occurring within Texas. Further, on information and belief, Defendant is subject to the Court's general jurisdiction, including from regularly doing or soliciting business, engaging in other persistent courses of conduct, and deriving substantial revenue from goods and services provided to persons or entities in Texas. Further, on information and belief, Defendant is subject to the Court's personal jurisdiction at least due to its sale of products and/or services within Texas. Defendant committed such purposeful acts and/or transactions in Texas such that it reasonably should know and expect that it could be haled into this Court as a consequence of such activity.

6. Venue is proper in this district under 28 U.S.C. § 1400(b). On information and belief, from and within this District Defendant has committed at least a portion of the infringements at issue in this case.

7. Defendant has authorized sellers and sales representatives that offer for sale and sell infringing products to consumers at various locations throughout the State of Texas and this Judicial District including, but not limited to: Best Buy, 422 West TX-281 Loop, Suite 100, Longview, Texas 75605; Best Buy, 2800 North Central Expressway, Plano, Texas 75074; Best Buy, 5514 South Broadway Avenue, Tyler, Texas 75703; Staples, 812 West McDermott Drive, Allen, Texas 75013; Walmart Supercenter, 730 West Exchange Parkway, Allen, Texas 75013; and Walmart Supercenter, 1701 East End Boulevard North, Marshall, Texas 75670.

8. For these reasons, personal jurisdiction exists and venue is proper in this Court under 28 U.S.C. § 1400(b).

III. COUNT I
(PATENT INFRINGEMENT OF UNITED STATES PATENT NO. 6,813,742)

9. Plaintiff incorporates the above paragraphs herein by reference.

10. On November 2, 2004, the USPTO duly and legally issued U.S. Patent No. 6,813,742 ("the '742 Patent" or "Patent-in-Suit"), entitled "High Speed Turbo Codes Decoder for 3G Using Pipelined SISO Log-Map Decoders Architecture." The '742 patent was the subject of a reexamination request filed on July 13, 2006. An *Ex Parte* Reexamination Certificate was issued for the '742 patent on February 10, 2009. A true and correct copy of the '742 Patent with its *Ex Parte* Reexamination Certificate is attached hereto as Exhibit A.

11. TurboCode is the assignee of all right, title, and interest in the '742 patent, including all rights to enforce and prosecute actions for infringement and to collect damages for all relevant times against infringers of the '742 Patent. Accordingly, TurboCode possesses the exclusive right and standing to prosecute the present action for infringement of the '742 Patent by Defendant.

12. This case generally relates to decoder architectures and processes for receiving and decoding data in communications devices.

13. **Direct Infringement.** Upon information and belief, Defendant directly infringed claim 6 of the '742 Patent in Texas, and elsewhere in the United States, by performing actions comprising using or performing the claimed method of iteratively decoding a plurality of sequences of received baseband signals by using and/or testing the products, devices, systems, and components of systems that comply with the 4G/LTE standards as disclosed in the 3rd Generation Partnership Project ("3GPP") Standard Specifications (releases 8-13) governing cellular wireless communications and that were or are designed, developed, tested, made, used, offered for sale,

sold in the United States, imported into the United States, or that have a nexus to the United States. The Accused Instrumentalities include, but are not limited to, TravelMate Spin P4, TravelMate P4, Travel Mate P2, Acer Iconia Talk S, Acer Liquid Z6, Acer Swift 3, and Acer Swift 7 ("Accused Instrumentalities"). The products which are listed (together with support indicating that the identified product complies with relevant 4G/LTE standards and contains a baseband processor) and any products reasonably similar thereto (including, *e.g.*, products or model numbers marketed under a substantially similar name or that vary from a listed product by incorporating features that do not alter compliance with 4G/LTE standards). The Accused Instrumentality also extends to all cellular communication equipment, including eNodeBs, base stations, and related systems or devices that conform to the 4G/LTE standards. Defendant's 4G/LTE LTE-based solutions, including small cells, macro cells, and eNodeBs for private and public cellular networks are representative products because it performed iterative decoding in accordance with the 4G/LTE standards disclosed in the 3GPP Standard Specifications as do the Accused Instrumentalities.

14. Claim 6 of the '742 Patent *Ex Parte* Reexamination Certificate states:

> A method of iteratively decoding a plurality of sequences of received baseband signals, the method comprising:
>
> providing an input buffer comprising at least three shift registers, for receiving an input signal and generating first, second, and third shifted input signals;
>
> providing first and second soft decision decoders serially coupled in a circular circuit, wherein each decoder processes soft decision from the preceding decoder output data, and wherein the first decoder further receives the first and second shifted input signals from the input buffer and the second decoder further receives the third shifted input signal from the input buffer;
>
> providing at least one memory module coupled to an output of each of the first and second soft decision decoders, wherein the output of the memory module associated with the second soft decision decoder is fed back as an input of the first soft decision decoder;

processing systematic information data and extrinsic information data using the maximum a posteriori (AP) probability algorithm, and/or logarithm approximation algorithm;

generating soft decision based on the maximum a posteriori (MAP) probability algorithm, and/or logarithm approximation algorithm;

weighing and storing soft decision information into the corresponding memory module;

performing, for a predetermined number of times, iterative decoding from the first to the last of multiple decoders, wherein an output from the last soft decision decoder is fed back as an input to the first soft decision decoder, then from the first to the second decoders, and propagate to the last decoder in a circular circuit.

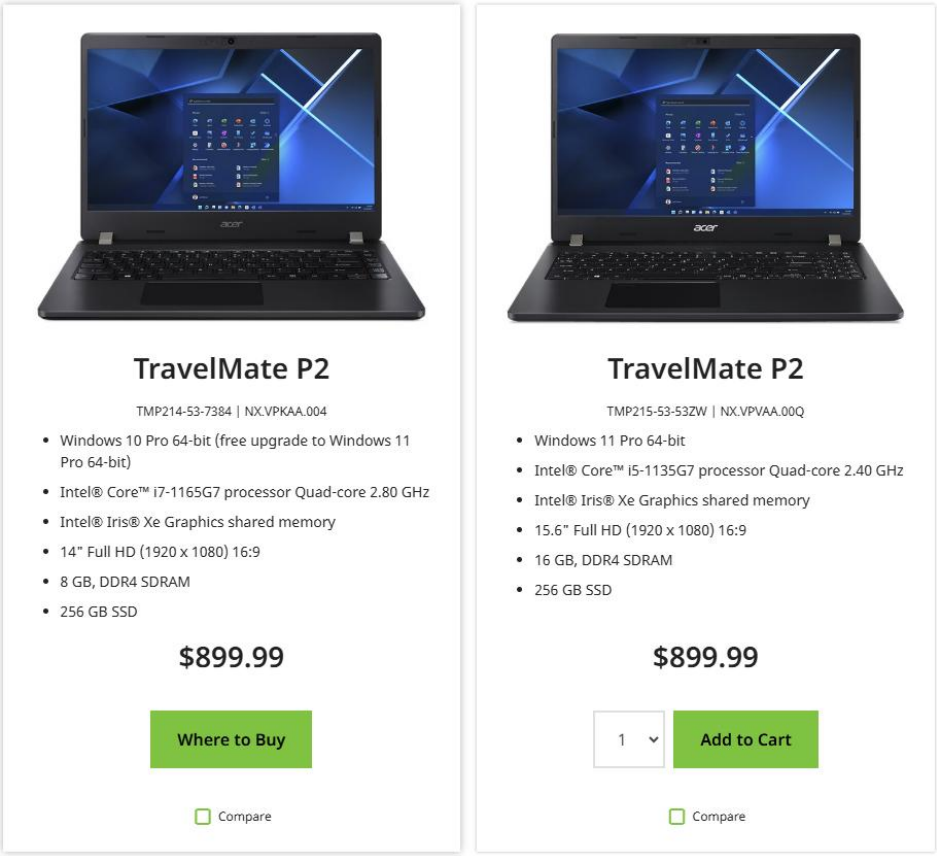
15. The Accused Instrumentalities provided or performed a method of iteratively decoding a plurality of sequences of received baseband signals, as shown below by their compliance with the 3G and/or 4G/LTE standards disclosed in the 3GPP Standard Specifications:

- All three new models have eSIM-enabled [1] 4G LTE connectivity, so business travelers can enjoy immediate connectivity to local networks
- All models meet the MIL-STD 810G [2] military durability standard, making them more than capable of withstanding the rigors of frequent travel
- Designed for portability, all of the models range from just 1.3 kg (2.87 lbs) to 1.625 kg (3.58 lbs) light and are under 20 mm thin

TAIPEI, TAIWAN (October 21, 2020) Acer today announced three new products in its TravelMate series of commercial notebooks for enterprise and business users. These include the TravelMate Spin P4 (TMP414RN-51), a convertible notebook with a touch screen; the TravelMate P4 (TMP414-51), a powerful and portable notebook for those who prefer traditional clamshell models; and the TravelMate P2 (TMP214-53), a durable notebook with enough ports and battery life to handle anything that comes up in a day's work.

(*E.g.*, https://news.acer.com/acer-unveils-3-new-products-in-the-robust-travelmate-notebook-series-for-commercial-use).

(*E.g.*, https://www.acer.com/us-en/laptops/travelmate/travelmate-spin-p4).

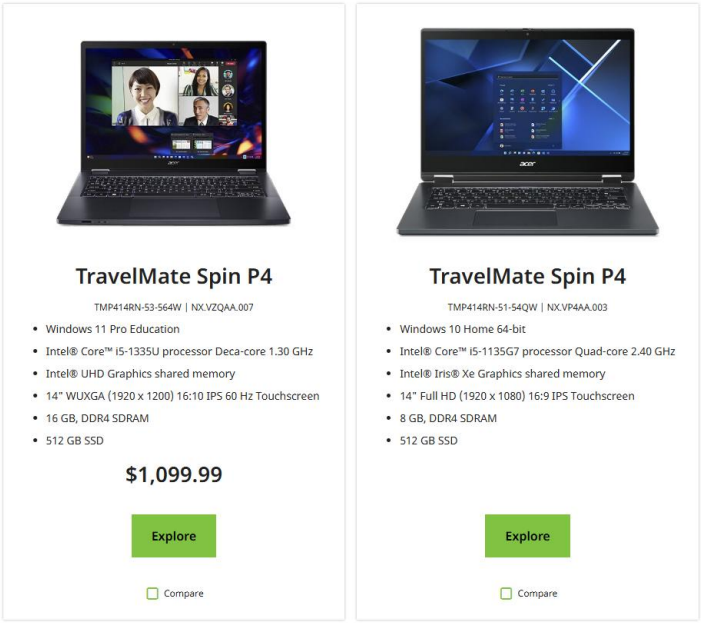


(*E.g.*, https://www.acer.com/us-en/laptops/travelmate/travelmate-p2).

(*E.g.*, https://www.acer.com/us-en/laptops/travelmate/travelmate-p4).

VSIM Virtual SIM Technology

It provides users with cost-effective, flexible, and secure 4G LTE data plans, enhancing coverage and compatibility across devices, and making it an ideal solution for international travelers, business, and remote workers.

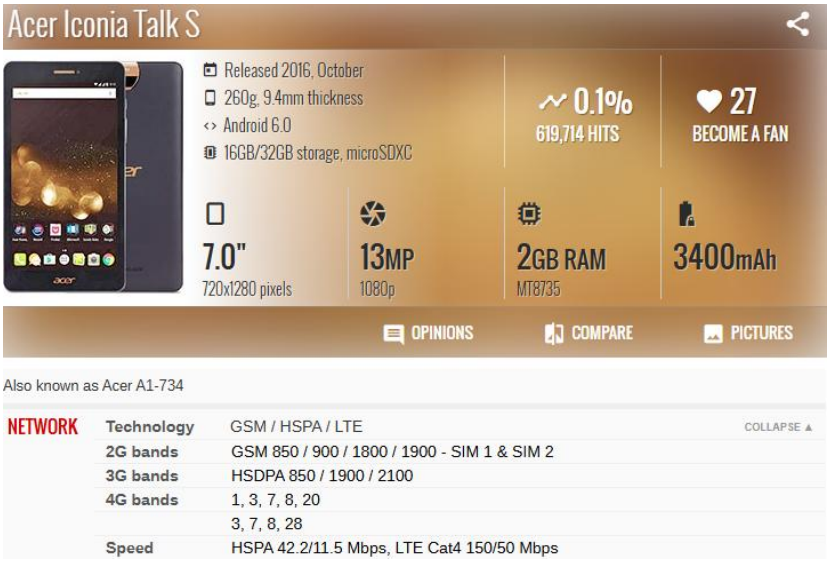


(*E.g.*, https://www.acer.com/us-en/laptops/travelmate/travelmate-p4-spin-14#features).

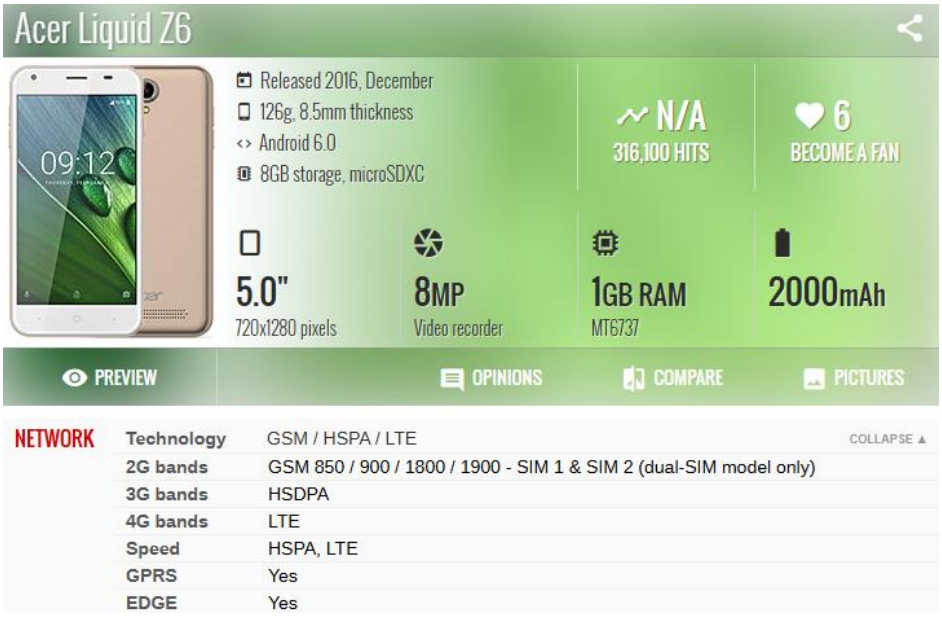
Acer Iconia Talk S

Perfect for business professionals, frequent travelers and cost-conscious consumers, the Acer Iconia Talk S is a 4G LTE tablet and phone in one. Its dual-SIM design supports two accounts (phone numbers) and offers extremely accurate and clear voice calls as well as fast text communication.

(*E.g.*, https://news.acer.com/acer-launches-intuitive-and-compact-android-devices-at-ifa-2016).



(*E.g.*, https://www.gsmarena.com/acer_iconia_talk_s-8306.php).



(*E.g.*, https://www.gsmarena.com/acer_liquid_z6-8304.php).

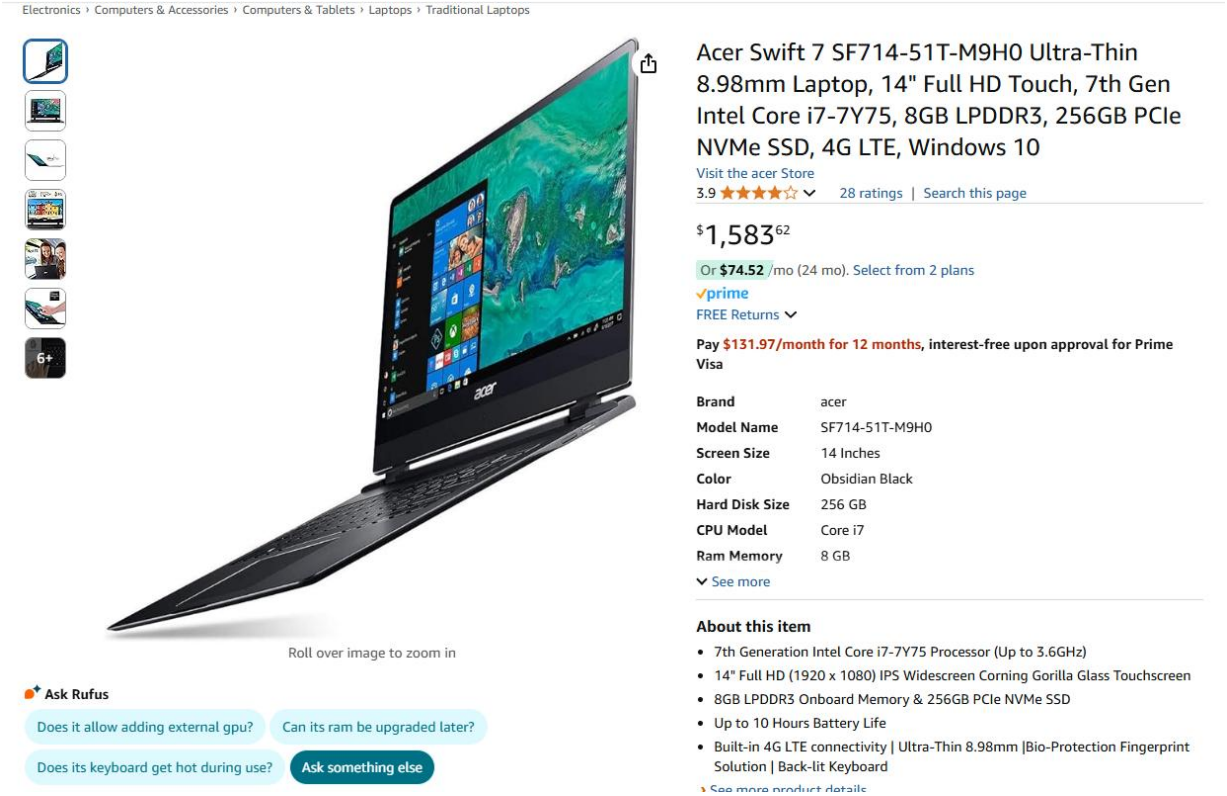
Product

Acer Swift 5 is the World's Lightest 15-inch Notebook

BERLIN, GERMANY - **Editor's Summary**

- Weighing just 990 grams, the ground-breaking Swift 5 makes a big impact with the latest 8th Gen Intel™ Core® processors, superb style and a thin-bezeled 15.6-inch display
- The Swift 5 features a full HD 1920x1080 IPS[1] touchscreen with ultra-narrow bezels, giving it an incredible 87.6% screen-to-body ratio to create an immersive viewing experience
- New Swift 3 models have slim designs and bezels in an array of options with 13.3-inch and 14-inch displays, the latest 8th Gen Intel Core processors and a configuration with built-in 4G LTE[2] connectivity on the go

(*E.g.*, https://news.acer.com/acer-swift-5-is-the-worlds-lightest-15-inch-notebook).



(*E.g.*, https://www.amazon.com/Acer-SF714-51T-M9H0-Ultra-Thin-i7-7Y75-Protective/dp/B07CHKMSGZ).

16. The Accused Instrumentalities provided or performed a method of iteratively decoding a plurality of sequences of received baseband signals in accordance with the 4G/LTE standards disclosed in the 3GPP Standard Specifications.

5 Channel coding, multiplexing and interleaving

Data and control streams from/to MAC layer are encoded /decoded to offer transport and control services over the radio transmission link. Channel coding scheme is a combination of error detection, error correcting, rate matching, interleaving and transport channel or control information mapping onto/splitting from physical channels.

5.1.3 Channel coding

The bit sequence input for a given code block to channel coding is denoted by $c_0, c_1, c_2, c_3, \ldots c_{K-1}$, where K is the number of bits to encode. After encoding the bits are denoted by $d_0^{(i)}, d_1^{(i)}, d_2^{(i)}, d_3^{(i)}, \ldots, d_{D-1}^{(i)}$, where D is the number of encoded bits per output stream and i indexes the encoder output stream. The relation between c_k and $d_k^{(i)}$ and between K and D is dependent on the channel coding scheme.

The following channel coding schemes can be applied to TrCHs:

- tail biting convolutional coding;
- turbo coding.

Usage of coding scheme and coding rate for the different types of TrCH is shown in table 5.1.3-1. Usage of coding scheme and coding rate for the different control information types is shown in table 5.1.3-2.

Usage of coding scheme and coding rate for the different types of TrCH is shown in table 5.1.3-1. Usage of coding scheme and coding rate for the different control information types is shown in table 5.1.3-2.

The values of D in connection with each coding scheme:

- tail biting convolutional coding with rate 1/3: $D = K$;
- turbo coding with rate 1/3: $D = K + 4$.

The range for the output stream index i is 0, 1 and 2 for both coding schemes.

Table 5.1.3-1: Usage of channel coding scheme and coding rate for TrCHs

TrCH	Coding scheme	Coding rate
UL-SCH	Turbo coding	1/3
DL-SCH		
PCH		
MCH		
SL-SCH		
SL-DCH		
BCH	Tail biting convolutional coding	1/3
SL-BCH		

(*See* 3GPP TS 136 212 V17.1.0 (Page:10, Section 5).

5.1.3.2 Turbo coding

5.1.3.2.1 Turbo encoder

The scheme of turbo encoder is a Parallel Concatenated Convolutional Code (PCCC) with two 8-state constituent encoders and one turbo code internal interleaver. The coding rate of turbo encoder is 1/3. The structure of turbo encoder is illustrated in figure 5.1.3-2.

The transfer function of the 8-state constituent code for the PCCC is:

$$G(D) = \left[1, \frac{g_1(D)}{g_0(D)}\right],$$

where

$$g_0(D) = 1 + D^2 + D^3,$$

5.1.3.2.3 Turbo code internal interleaver

The bits input to the turbo code internal interleaver are denoted by $c_0, c_1, \ldots, c_{K-1}$, where K is the number of input bits. The bits output from the turbo code internal interleaver are denoted by $c'_0, c'_1, \ldots, c'_{K-1}$.

The relationship between the input and output bits is as follows:

$$c'_i = c_{\Pi(i)}, \; i=0, 1\ldots, (K\text{-}1)$$

where the relationship between the output index i and the input index $\Pi(i)$ satisfies the following quadratic form:

$$\Pi(i) = \left(f_1 \cdot i + f_2 \cdot i^2\right) \bmod K$$

The parameters f_1 and f_2 depend on the block size K and are summarized in Table 5.1.3-3.

(*See* 3GPP TS 136 212 V17.1.0 (Page:10, Section 5).

17. Based on information and belief, each of the Accused Instrumentalities processed received baseband digital signals in an iterative manner. The standard discloses that Turbo coding shall be used for transport blocks. The Turbo encoder consists of two 8-state constituent encoders and an internal interleaver. This means that in LTE, transport blocks at the eNodeB (Defendant's products) are encoded using Turbo coding, which consists of two constituent encoders and an interleaver. Products based on an eNodeB perform Turbo encoding at the transmitter side before sending data to the UE (User Equipment), where the Turbo decoding process occurs on the UE side, or vice versa. However, in cases where the eNodeB receives the encoded data from the UE,

it performs Turbo decoding to retrieve the original information. The eNodeB also interacts with the UE's iterative decoding through HARQ (Hybrid Automatic Repeat Request), which is a form of iterative transmission and decoding feedback. Thus, for mapping to Defendant, the Turbo encoding process at the eNodeB can be linked with the iterative Turbo decoding process at the UE and vice versa, showing how the transmitted data is encoded iteratively at the eNodeB and then decoded iteratively at the UE.

18. The Accused Instrumentalities provided processing of systematic information data and extrinsic information data using the maximum a posteriori (MAP) probability algorithm.

5.1.3.2 Turbo coding

5.1.3.2.1 Turbo encoder

The scheme of turbo encoder is a Parallel Concatenated Convolutional Code (PCCC) with two 8-state constituent encoders and one turbo code internal interleaver. The coding rate of turbo encoder is 1/3. The structure of turbo encoder is illustrated in figure 5.1.3-2.

The transfer function of the 8-state constituent code for the PCCC is:

$$G(D) = \left[1, \frac{g_1(D)}{g_0(D)}\right],$$

where

$$g_0(D) = 1 + D^2 + D^3,$$

(*See* 3GPP TS 136 212 V17.1.0 (Page:14, Section 5.1.3.2)).

$$g_1(D) = 1 + D + D^3.$$

The initial value of the shift registers of the 8-state constituent encoders shall be all zeros when starting to encode the input bits.

The output from the turbo encoder is

$$d_k^{(0)} = x_k$$

$$d_k^{(1)} = z_k$$

$$d_k^{(2)} = z'_k$$

for $k = 0,1,2,\ldots, K-1$.

If the code block to be encoded is the 0-th code block and the number of filler bits is greater than zero, i.e., $F > 0$, then the encoder shall set $c_k = 0$, $k = 0,\ldots,(F\text{-}1)$ at its input and shall set $d_k^{(0)} = < NULL >$, $k = 0,\ldots,(F\text{-}1)$ and $d_k^{(1)} = < NULL >$, $k = 0,\ldots,(F\text{-}1)$ at its output.

The bits input to the turbo encoder are denoted by $c_0, c_1, c_2, c_3, \ldots c_{K-1}$, and the bits output from the first and second 8-state constituent encoders are denoted by $z_0, z_1, z_2, z_3, \ldots, z_{K-1}$ and $z'_0, z'_1, z'_2, z'_3, \ldots, z'_{K-1}$, respectively. The bits output from the turbo code internal interleaver are denoted by $c'_0, c'_1, \ldots c'_{K-1}$, and these bits are to be the input to the second 8-state constituent encoder.

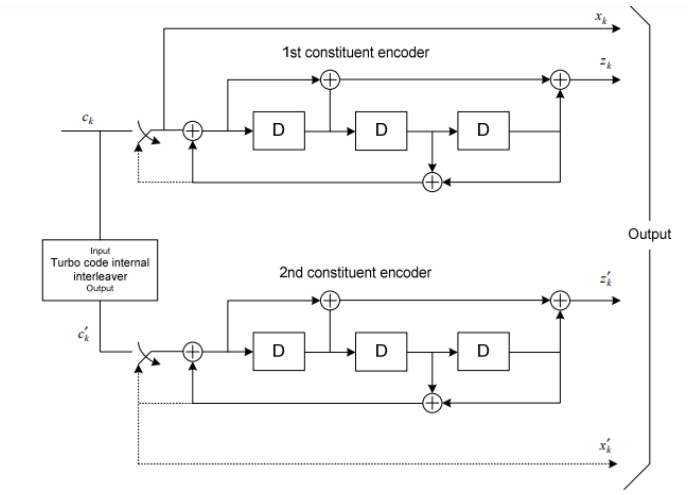


Figure 5.1.3-2: Structure of rate 1/3 turbo encoder (dotted lines apply for trellis termination only)

(*See* 3GPP TS 136 212 V17.1.0 (Page:14, Section 5.1.3.2)).

5.2.3.3 Physical Layer Implementation

The parameters of the physical layer simulation were set according to the parameters for a DCH in multipath fading conditions given in [9] for the downlink and [10] for the uplink. The TB size is 928 bits and the Turbo decoder uses the Log-MAP algorithm with 4 iterations. The rake receiver has 6 fingers at 60 possible positions.

The different channel conditions given in Tables 2, 3 and 4 were extracted from [18] (Selection procedures for the choice of radio transmission technologies of the UMTS).

(*See* 3GPP TR 126 935 V16.0.0 (Page: 15, Section 5.2.3.3).

19. Additionally, and alternatively, as discussed above, each of the Accused Instrumentalities processed received baseband digital signals in an iterative manner through its implementation of turbo encoding/decoding. Further, the soft decision generation using MAP or Log-MAP algorithm is a fundamental part of turbo encoding/decoding, which directly corresponds to the turbo encoder structure defined in 5.1.3.2.1. The MAP algorithm operates on the encoded bits generated by the 8-state constituent encoders and utilizes the interleaved parity bits for iterative decoding. While Turbo decoding is not explicitly covered in TS 36.212, the Turbo encoder structure (Section 5.1.3.2) forms the foundation for soft decision generation using MAP/Log-MAP. The claim element is mappable because the MAP-based soft decision decoding inherently relies on the encoded bit streams defined in TS 36.212

20. The Accused Instrumentalities included various 4G solutions, and products are designed to comply with LTE standards, which typically employ Turbo coding for error correction. Turbo decoding in these standards commonly utilizes the Maximum a Posteriori (MAP) probability algorithm or its logarithmic approximation (Log-MAP) to generate soft decisions

5 Channel coding, multiplexing and interleaving

Data and control streams from/to MAC layer are encoded /decoded to offer transport and control services over the radio transmission link. Channel coding scheme is a combination of error detection, error correcting, rate matching, interleaving and transport channel or control information mapping onto/splitting from physical channels.

5.1.3.2 Turbo coding

5.1.3.2.1 Turbo encoder

The scheme of turbo encoder is a Parallel Concatenated Convolutional Code (PCCC) with two 8-state constituent encoders and one turbo code internal interleaver. The coding rate of turbo encoder is 1/3. The structure of turbo encoder is illustrated in figure 5.1.3-2.

The transfer function of the 8-state constituent code for the PCCC is:

$$G(D) = \left[1, \frac{g_1(D)}{g_0(D)}\right],$$

where

$$g_0(D) = 1 + D^2 + D^3,$$

$$g_1(D) = 1 + D + D^3.$$

The initial value of the shift registers of the 8-state constituent encoders shall be all zeros when starting to encode the input bits.

The output from the turbo encoder is

$$d_k^{(0)} = x_k$$

$$d_k^{(1)} = z_k$$

$$d_k^{(2)} = z'_k$$

for $k = 0,1,2,\ldots, K-1$.

If the code block to be encoded is the 0-th code block and the number of filler bits is greater than zero, i.e., $F > 0$, then the encoder shall set $c_k, = 0$, $k = 0,\ldots,(F\text{-}1)$ at its input and shall set $d_k^{(0)} =< NULL >$, $k = 0,\ldots,(F\text{-}1)$ and $d_k^{(1)} =< NULL >$, $k = 0,\ldots,(F\text{-}1)$ at its output.

The bits input to the turbo encoder are denoted by $c_0, c_1, c_2, c_3, \ldots c_{K-1}$, and the bits output from the first and second 8-state constituent encoders are denoted by $z_0, z_1, z_2, z_3, \ldots, z_{K-1}$ and $z'_0, z'_1, z'_2, z'_3, \ldots, z'_{K-1}$, respectively. The bits output from the turbo code internal interleaver are denoted by $c'_0, c'_1, \ldots c'_{K-1}$, and these bits are to be the input to the second 8-state constituent encoder.

(*See* 3GPP TS 136 212 V17.1.0 (Page:14, Section).

5.2.3.3 Physical Layer Implementation

The parameters of the physical layer simulation were set according to the parameters for a DCH in multipath fading conditions given in [9] for the downlink and [10] for the uplink. The TB size is 928 bits and the Turbo decoder uses the Log-MAP algorithm with 4 iterations. The rake receiver has 6 fingers at 60 possible positions.

The different channel conditions given in Tables 2, 3 and 4 were extracted from [18] (Selection procedures for the choice of radio transmission technologies of the UMTS).

(*See* 3GPP TR 126 935 V16.0.0 (Page: 15, Section 5.2.3.3)).

21. The Accused Instrumentalities implement a Turbo encoder as specified in ETSI TS 36.212, which generates systematic and parity bits. While TS 36.212 does not explicitly disclose the Turbo decoder, Turbo decoding is commonly performed using the Maximum a Posteriori (MAP) probability algorithm and/or its logarithmic approximation (Log-MAP) to generate soft decisions. Given that Turbo encoding inherently requires a corresponding Turbo decoding process for proper data recovery, it is reasonable to infer that the Accused Instrumentalities utilize a MAP-based and/or Log-MAP-based decoding algorithm to generate soft decisions, which aligns with the claim element.

22. The Accused Instrumentalities included weighting and storing soft decision information into the corresponding memory module (*e.g.*, "Interleaver").

5.1.4 Rate matching

5.1.4.1 Rate matching for turbo coded transport channels

The rate matching for turbo coded transport channels is defined per coded block and consists of interleaving the three information bit streams $d_k^{(0)}$, $d_k^{(1)}$ and $d_k^{(2)}$, followed by the collection of bits and the generation of a circular buffer as depicted in Figure 5.1.4-1. The output bits for each code block are transmitted as described in clause 5.1.4.1.2.

(*See* 3GPP TS 136 212 V17.1.0 (Page:17, Section 5.1.4)).

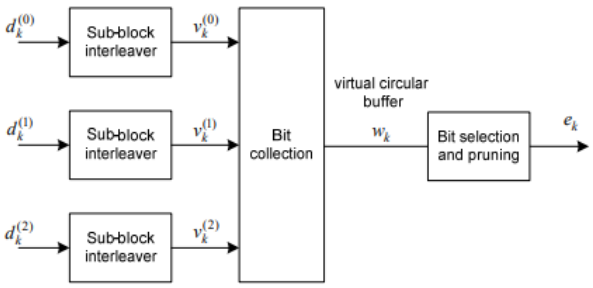


Figure 5.1.4-1. Rate matching for turbo coded transport channels

The bit stream $d_k^{(0)}$ is interleaved according to the sub-block interleaver defined in clause 5.1.4.1.1 with an output sequence defined as $v_0^{(0)}, v_1^{(0)}, v_2^{(0)}, \ldots, v_{K_\Pi-1}^{(0)}$ and where K_Π is defined in clause 5.1.4.1.1.

The bit stream $d_k^{(1)}$ is interleaved according to the sub-block interleaver defined in clause 5.1.4.1.1 with an output sequence defined as $v_0^{(1)}, v_1^{(1)}, v_2^{(1)}, \ldots, v_{K_\Pi-1}^{(1)}$.

The bit stream $d_k^{(2)}$ is interleaved according to the sub-block interleaver defined in clause 5.1.4.1.1 with an output sequence defined as $v_0^{(2)}, v_1^{(2)}, v_2^{(2)}, \ldots, v_{K_\Pi-1}^{(2)}$.

The sequence of bits e_k for transmission is generated according to clause 5.1.4.1.2.

(*See* 3GPP TS 136 212 V17.1.0 (Page:17, Section 5.1.4)).

5.1.4.1.2 Bit collection, selection and transmission

The circular buffer of length $K_w = 3K_\Pi$ for the r-th coded block is generated as follows:

$w_k = v_k^{(0)}$ for $k = 0, \ldots, K_\Pi - 1$

$w_{K_\Pi + 2k} = v_k^{(1)}$ for $k = 0, \ldots, K_\Pi - 1$

$w_{K_\Pi + 2k + 1} = v_k^{(2)}$ for $k = 0, \ldots, K_\Pi - 1$

Denote the soft buffer size for the transport block by N_{IR} bits and the soft buffer size for the r-th code block by N_{cb} bits. The size N_{cb} is obtained as follows, where C is the number of code blocks computed in clause 5.1.2:

- $N_{cb} = \min\left(\left\lfloor \frac{N_{IR}}{C} \right\rfloor, K_w\right)$ for DL-SCH and PCH transport channels
- $N_{cb} = K_w$ for UL-SCH, MCH, SL-SCH and SL-DCH transport channels

(*See* 3GPP TS 136 212 V17.1.0 (Page:19, Section 5.1.4.1.2)).

6.2.5 HARQ FEC decoder

The HARQ decoder combines the demodulated and deinterleaved data signal with previously transmitted redundancy versions. For this operation it applies a two stage rate matching scheme and performs turbo decoding of the combined soft-information.

To speed up the MSD reception in adverse transmission conditions, the HARQ decoding is performed for partially received messages, starting from the second redundancy version, *rv*1. Decoding is then attempted after reception of each of the three data parts of the MSD frame (see clause 5.1.5). The decoding attempts based on partial messages is beneficial since, in many cases, the correct MSD can be decoded already after the incremental redundancy contained in the first data part D1 of *rv*1. Figure 18 summarizes the decoder algorithm.

After MSD data bits are decoded, a descrambling operation as described in clause 5.1.2 applies.

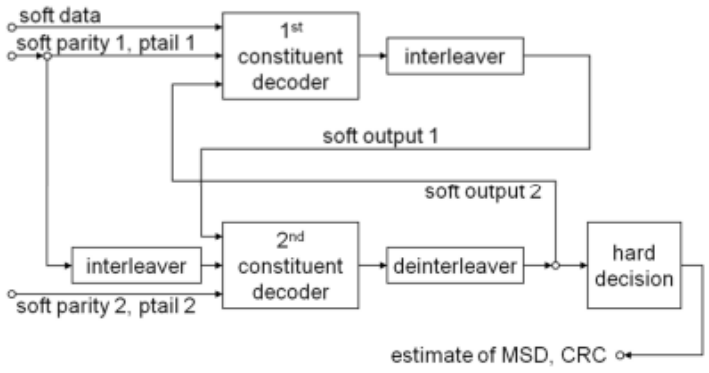


Figure 18: Turbo decoder

(*See* 3gpp TS 126 267 V17.0.0 (Page: 25, Section 6.2.5)).

23. The Accused Instrumentalities implemented a Turbo encoder as defined in TS 36.212, where systematic and parity bits are stored in interleaving buffers before transmission. Although TS 36.212 does not explicitly disclose soft decision weighting and storage, Turbo decoding—typically used to decode Turbo-encoded data—employs soft decision weighting based on Log-Likelihood Ratios (LLRs) and stores the weighted information in memory modules for iterative decoding. Given that Turbo encoding in TS 36.212 inherently requires corresponding Turbo decoding, it is reasonable to infer that the Accused Instrumentalities implemented soft decision weighting and storage in compliance with industry-standard Turbo decoding methods.

24. The Accused Instrumentalities perform performed iterative decoding a predetermined number of times, from the first to the last of multiple decoders, where the output

from the last soft decision decoder is fed back as input to the first soft decision decoder (e.g., during the Turbo coding/decoding process).

5.1.3.2 Turbo coding

5.1.3.2.1 Turbo encoder

The scheme of turbo encoder is a Parallel Concatenated Convolutional Code (PCCC) with two 8-state constituent encoders and one turbo code internal interleaver. The coding rate of turbo encoder is 1/3. The structure of turbo encoder is illustrated in figure 5.1.3-2.

The transfer function of the 8-state constituent code for the PCCC is:

$$G(D) = \left[1, \frac{g_1(D)}{g_0(D)}\right],$$

where

$$g_0(D) = 1 + D^2 + D^3,$$

$$g_1(D) = 1 + D + D^3.$$

The initial value of the shift registers of the 8-state constituent encoders shall be all zeros when starting to encode the input bits.

The output from the turbo encoder is

$$d_k^{(0)} = x_k$$

$$d_k^{(1)} = z_k$$

$$d_k^{(2)} = z'_k$$

for $k = 0,1,2,\ldots, K-1$.

If the code block to be encoded is the 0-th code block and the number of filler bits is greater than zero, i.e., $F > 0$, then the encoder shall set $c_k = 0$, $k = 0,\ldots,(F\text{-}1)$ at its input and shall set $d_k^{(0)} =< NULL >$, $k = 0,\ldots,(F\text{-}1)$ and $d_k^{(1)} =< NULL >$, $k = 0,\ldots,(F\text{-}1)$ at its output.

The bits input to the turbo encoder are denoted by $c_0, c_1, c_2, c_3, \ldots c_{K-1}$, and the bits output from the first and second 8-state constituent encoders are denoted by $z_0, z_1, z_2, z_3, \ldots, z_{K-1}$ and $z'_0, z'_1, z'_2, z'_3, \ldots, z'_{K-1}$, respectively. The bits output from the turbo code internal interleaver are denoted by $c'_0, c'_1, \ldots c'_{K-1}$, and these bits are to be the input to the second 8-state constituent encoder.

(*See* 3GPP TR 126 935 V16.0.0 (Page: 14, Section 5.1.3.2)).

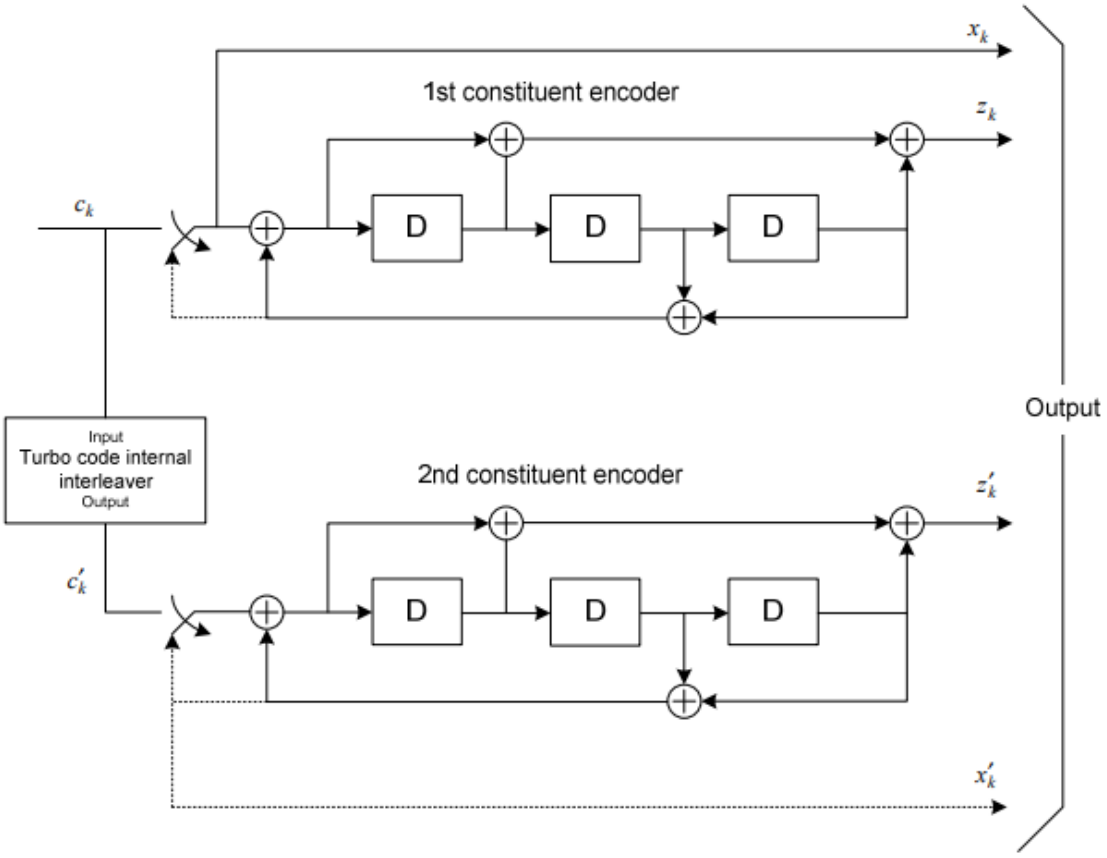


Figure 5.1.3-2: Structure of rate 1/3 turbo encoder (dotted lines apply for trellis termination only)

5.1.3.2.2 Trellis termination for turbo encoder

Trellis termination is performed by taking the tail bits from the shift register feedback after all information bits are encoded. Tail bits are padded after the encoding of information bits.

The first three tail bits shall be used to terminate the first constituent encoder (upper switch of figure 5.1.3-2 in lower position) while the second constituent encoder is disabled. The last three tail bits shall be used to terminate the second constituent encoder (lower switch of figure 5.1.3-2 in lower position) while the first constituent encoder is disabled.

The transmitted bits for trellis termination shall then be:

$$d_K^{(0)} = x_K,\ d_{K+1}^{(0)} = z_{K+1},\ d_{K+2}^{(0)} = x'_K,\ d_{K+3}^{(0)} = z'_{K+1}$$

$$d_K^{(1)} = z_K,\ d_{K+1}^{(1)} = x_{K+2},\ d_{K+2}^{(1)} = z'_K,\ d_{K+3}^{(1)} = x'_{K+2}$$

$$d_K^{(2)} = x_{K+1},\ d_{K+1}^{(2)} = z_{K+2},\ d_{K+2}^{(2)} = x'_{K+1},\ d_{K+3}^{(2)} = z'_{K+2}$$

(*See* 3GPP TR 126 935 V16.0.0 (Page: 14, Section 5.1.3.2)).

5.1.3.2.3 Turbo code internal interleaver

The bits input to the turbo code internal interleaver are denoted by $c_0, c_1, \ldots, c_{K-1}$, where K is the number of input bits. The bits output from the turbo code internal interleaver are denoted by $c'_0, c'_1, \ldots c'_{K-1}$.

The relationship between the input and output bits is as follows:

$$c'_i = c_{\Pi(i)}, \; i=0, 1\ldots, (K\text{-}1)$$

where the relationship between the output index i and the input index $\Pi(i)$ satisfies the following quadratic form:

$$\Pi(i) = \left(f_1 \cdot i + f_2 \cdot i^2\right) \bmod K$$

The parameters f_1 and f_2 depend on the block size K and are summarized in Table 5.1.3-3.

Table 5.1.3-3: Turbo code internal interleaver parameters

i	K	f_1	f_2	i	K	f_1	f_2	i	K	f_1	f_2	i	K	f_1	f_2
1	40	3	10	48	416	25	52	95	1120	67	140	142	3200	111	240
2	48	7	12	49	424	51	106	96	1152	35	72	143	3264	443	204
3	56	19	42	50	432	47	72	97	1184	19	74	144	3328	51	104
4	64	7	16	51	440	91	110	98	1216	39	76	145	3392	51	212
5	72	7	18	52	448	29	168	99	1248	19	78	146	3456	451	192
6	80	11	20	53	456	29	114	100	1280	199	240	147	3520	257	220
7	88	5	22	54	464	247	58	101	1312	21	82	148	3584	57	336
8	96	11	24	55	472	29	118	102	1344	211	252	149	3648	313	228
9	104	7	26	56	480	89	180	103	1376	21	86	150	3712	271	232
10	112	41	84	57	488	91	122	104	1408	43	88	151	3776	179	236
11	120	103	90	58	496	157	62	105	1440	149	60	152	3840	331	120
12	128	15	32	59	504	55	84	106	1472	45	92	153	3904	363	244
13	136	9	34	60	512	31	64	107	1504	49	846	154	3968	375	248

(*See* 3GPP TR 126 935 V16.0.0 (Page: 14, Section 5.1.3.2)).

6.2.5 HARQ FEC decoder

The HARQ decoder combines the demodulated and deinterleaved data signal with previously transmitted redundancy versions. For this operation it applies a two stage rate matching scheme and performs turbo decoding of the combined soft-information.

To speed up the MSD reception in adverse transmission conditions, the HARQ decoding is performed for partially received messages, starting from the second redundancy version, *rv*1. Decoding is then attempted after reception of each of the three data parts of the MSD frame (see clause 5.1.5). The decoding attempts based on partial messages is beneficial since, in many cases, the correct MSD can be decoded already after the incremental redundancy contained in the first data part D1 of *rv*1. Figure 18 summarizes the decoder algorithm.

After MSD data bits are decoded, a descrambling operation as described in clause 5.1.2 applies.

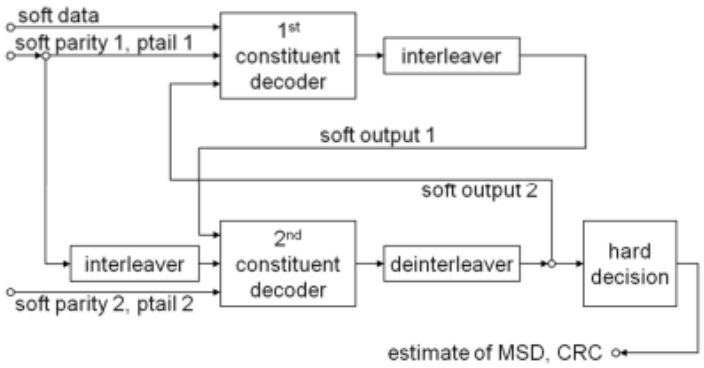


Figure 18: Turbo decoder

(*See* 3GPP TS 126 267 V17.0.0 (Page: 25, Section 6.2.5)).

25. HARQ employs a two-stage rate matching scheme and turbo decoding to combine soft information from different versions of the transmission, aligning with the concept of iterative decoding and feedback between decoders. The Accused Instrumentalities' assertion of iterative decoding with feedback between decoders in a circular circuit can be mapped to sections of TS 36.212 that describe the Turbo encoder structure (Section 5.1.3.2.1), trellis termination (Section 5.1.3.2.2), and the internal interleaver (Section 5.1.3.2.3), although decoding itself is not explicitly detailed in the standard. While TS 36.212 primarily focuses on Turbo encoding and the interleaving process, the iterative nature of encoding, involving feedback loops and interleaving, conceptually mirrors the iterative decoding process used in Turbo codes. Specifically, the iterative refinement of soft decisions and feedback to previous stages in the decoding process aligns with

the circular feedback mechanism described in the claim. Thus, while Turbo decoding is not disclosed in the standard, the iterative structure and feedback loops inherent in Turbo encoding provide a basis for mapping to the claim.

26. Plaintiff has been damaged as a result of Defendant's infringing conduct. Defendant is thus liable to Plaintiff for damages in an amount that adequately compensates Plaintiff for such Defendant's infringement of the '742 Patent, *i.e.*, in an amount that by law cannot be less than would constitute a reasonable royalty for the use of the patented technology, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

27. On information and belief, Defendant has had at least constructive notice of the '742 patent by operation of law and, to the extent required (no marking is required for method claims), marking requirements have been complied with.

IV. JURY DEMAND

Plaintiff, under Rule 38 of the Federal Rules of Civil Procedure, requests a trial by jury of any issues so triable by right.

V. PRAYER FOR RELIEF

WHEREFORE, Plaintiff respectfully requests that the Court find in its favor and against Defendant, and that the Court grant Plaintiff the following relief:

a. Judgment that one or more claims of United States Patent No. 6,813,742 have been infringed, either literally and/or under the doctrine of equivalents, by Defendant;

b. Judgment that Defendant account for and pay to Plaintiff all damages to and costs incurred by Plaintiff because of Defendant's infringing activities and other conduct complained of herein;

c. That Plaintiff be granted pre-judgment and post-judgment interest on the damages caused by Defendant's infringing activities and other conduct complained of herein; and

d. That Plaintiff be granted such other and further relief as the Court may deem just and proper under the circumstances.

February 13, 2025

DIRECTION IP LAW

/s/ Steven G. Kalberg

David R. Bennett (IL Bar No.: 6244214)
Steven G. Kalberg (IL Bar No.: 6336131)
P.O. Box 14184
Chicago, Illinois 60614-0184
Telephone: (312) 291-1667
dbennett@directionip.com
skalberg@directionip.com

Attorneys for Plaintiff TurboCode LLC