IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

ASCALE TECHNOLOGIES LLC,	§	Case No.
Plaintiff,	§	**JURY TRIAL DEMANDED**
v.	§	
TEXAS INSTRUMENTS, INC.,	§	
Defendant.	§	

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Ascale Technologies LLC ("Ascale" or "Plaintiff") for its Complaint against Defendant Texas Instruments, Inc., ("TI" or "Defendant") alleges as follows:

THE PARTIES

1. Ascale is a limited liability company, organized and existing under the laws of the State of Texas, with its principal place of business located at 104 East Houston Street, Suite 140, Marshall, Texas 75760.

2. Upon information and belief, Defendant Texas Instruments, Inc. ("TI") is a publicly traded corporation, organized and existing under the laws of the State of Delaware, with its principal place of business located at 12500 TI Boulevard, Dallas, Texas 75243.

3. On information and belief, TI is a technology company in the business of researching, developing, making, using, and selling semiconductor products, including the TI-branded products accused of infringement in this case by Ascale (the "Accused Products" defined below).

JURISDICTION

4. This is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. §§ 1, *et seq*. This Court has jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and 1338(a) and 1367.

5. This Court has personal jurisdiction over the Defendant consistent with the requirements of the Due Process Clause of the United States Constitution and the Texas Long Arm Statute. Defendant TI has its principal place of business in Dallas, Texas, where it employs more than 20,000 employees.

6. TI has, thereby, committed acts of direct infringement in the United States and in this District in violation of Ascale's intellectual property rights.

7. Venue is proper in this Judicial District pursuant to 28 U.S.C. §§ 1391(b) and 1400(b) because Defendant is subject to personal jurisdiction in this District, has committed acts of patent infringement in this District, and has a regular and established place of business in this District, including at least a commercial manufacturing facility located at 6412 U.S. Highway 75, Sherman, Texas, 75090. In addition to its existing facilities in this District, TI has, upon information and belief, commenced its construction activities with respect to a new $30 billion chip manufacturing facility also located in this District. Further, upon information and belief, Defendant has previously admitted or not contested proper venue in this District in other patent infringement actions.

PATENTS-IN-SUIT

8. On May 27, 2014, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 8,739,165 (the "'165 Patent") entitled "Shared Resource Based Thread

Scheduling With Affinity and/or Selectable Criteria." A true and correct copy of the '165 Patent is attached as Exhibit A.

9. On February 10, 2009, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 7,490,266 (the "'266 Patent") entitled "Integrated Circuit and Processing System with Improved Power Source Monitoring and Methods For Use Therewith." A true and correct copy of the '266 Patent is attached as Exhibit B.

10. On March 17, 2015, the United States Patent and Trademark Office duly and legally issued U.S. Patent No. 8,984,254 (the "'254 Patent") entitled "Techniques for Utilizing Translation Lookaside Buffer Entry Numbers to Improve Processor Performance." A true and correct copy of the '254 Patent is attached as Exhibit C.

11. Ascale is the sole and exclusive owner of all right, title, and interest in the '165 Patent, the '266 Patent, and the '254 Patent (collectively, the "Patents-in-Suit"), and holds the exclusive right to take all actions necessary to enforce its rights to the Patents-in-Suit, including the filing of this patent infringement lawsuit. Ascale also has the right to recover all damages for past, present, and future infringement of the Patents-in-Suit and to seek injunctive relief as appropriate under the law.

12. Ascale has at all times complied with the marking provisions of 35 U.S.C. § 287 with respect to the Patents-in-Suit.

FACTUAL ALLEGATIONS

13. The Patents-in-Suit generally cover systems and methods for coordinating memory operations and providing data patterns for calibration of memory systems.

14. The '165 Patent generally relates to the field of thread scheduling and, more particularly, to shared resource based thread scheduling with affinity and/or selectable criteria. The

technology described in the ’165 Patent was developed by Andrew C. Russell and William C. Moyer. By way of example, this technology is implemented today in multi-core processors that allocate tasks to appropriate cores based on workload and demand characteristics, such as task priority, core affinity, and task affinity.

15. The ’254 Patent generally relates to improving processor performance and, more specifically, to techniques for utilizing translation lookaside buffer entry numbers to improve processor performance. The technology described in the ‘254 Patent was developed by Thang M. Tran and Edmund J. Gieske. By way of example, this technology is implemented today in processors that implement translation lookaside buffers to translate between virtual and physical addresses.

16. The ’266 Patent generally relates to the field of processing systems as may be used in systems on integrated circuits and related methods, and more specifically to efficient implementation of a processor in conjunction with a battery or external power supply. The technology described in the ‘266 Patent was developed by Marcus W. May. By way of example, this technology is implemented today in processors that operate in conjunction with a power and/or battery management module, such as a battery management IC, PMU, and/or PMIC.

17. Upon information and belief, TI has had knowledge and notice of the Patents-in-Suit, and its infringement thereof, since they issued. TI was a direct competitor to Freescale prior to its acquisition by NXP (and to SigmaTel prior to its acquisition by Freescale), and upon information and belief, monitored or was otherwise aware of its patented inventions, including due to their impact on Freescale and TI’s market position, and based on its hiring of former Freescale employees. Alternatively, to the extent that TI avoided actual knowledge of the Patents-in-Suit, and its infringement thereof, it was willfully blind. Upon information and belief, to the extent it

lacked actual knowledge of infringement, TI deliberately avoided learning of infringement, despite subjectively believing that there was a high probability that it infringed NXP or Freescale's patents, and specifically the Patents-in-Suit. Upon information and belief, TI has adopted a policy or practice of not reviewing the patents of others, including those related to TI's specific industry and of NXP and Freescale in particular, thereby remaining willfully blind to the Patents-in-Suit. Upon information and belief, TI lacks written policies disseminated to employees regarding monitoring or avoidance of patent infringement by TI, and lacks mechanisms for employees to report patents which they believe TI may infringe. Upon information and belief, TI and its employees understood that there was a high likelihood that patents filed on innovations by Freescale, SigmaTel, and NXP read on the Accused Products based on their widely publicized R&D programs, and competitor status.

18. TI has infringed and is continuing to infringe one or more of the Patents-in-Suit by making, using, selling, offering to sell, and/or importing, and by actively inducing others to make, use, sell, offer to sell, and/or import, integrated circuits including a processor including, but not limited to, microcontrollers (MCUs), DSPs, Processors, Wireless Connectivity chips, Display Controllers, and PMICs (the "Accused Products"). The Accused Products include at least the products in the aforementioned categories identified on the TI website. *See e.g.*, https://www.ti.com/microcontrollers-mcus-processors/products.html#; https://www.ti.com/power-management/multi-channel-ics-pmic/products.html; https://www.ti.com/dlp-chip/automotive/products.html#1907=Controller&.

COUNT I
(Infringement of the '165 Patent)

19. Paragraphs 1 through 18 are incorporated by reference as if fully set forth herein.

20. Ascale has not licensed or otherwise authorized Defendant to make, use, offer for sale, sell, or import any products that embody the inventions of the '165 Patent.

21. Defendant has and continues to directly infringe the '165 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products including, but not limited to, multi-core processors, such as the TDA4VM Processors.

22. For example, Defendant has and continues to directly infringe at least claim 10 of the '165 Patent by making, using, offering to sell, selling, and/or importing into the United States products that comprise an apparatus, comprising: a plurality of processors; and control circuitry, coupled to the plurality of processors, said control circuitry comprising: core availability circuitry for determining if a core is available to execute a thread; core affinity circuitry for determining if the core has an affinity for the thread, wherein said determining if the core has an affinity for the thread comprises counting a number of writes by one or more other threads to a cache associated with the core since the thread was last executed by the core; monitoring circuitry for monitoring one or more characteristics of the apparatus; and select circuitry for selecting one or more of the plurality of processors to execute the thread based on the affinity for the thread and the one or more characteristics of the apparatus.

23. The Accused Products comprise a plurality of processors. For example, the TDA4VM comprises multiple cores, each of which is a processor.

1 Features

Processor cores:

- C7x floating point, vector DSP, up to 1.0GHz, 80 GFLOPS, 256 GOPS
- Deep-learning matrix multiply accelerator (MMA), up to 8 TOPS (8b) at 1.0GHz
- Vision Processing Accelerators (VPAC) with Image Signal Processor (ISP) and multiple vision assist accelerators
- Depth and Motion Processing Accelerators (DMPAC)
- Dual 64-bit Arm® Cortex®-A72 microprocessor subsystem at up to 2.0GHz
  - 1MB shared L2 cache per dual-core Cortex®-A72 cluster
  - 32KB L1 DCache and 48KB L1 ICache per Cortex®-A72 core
- Six Arm® Cortex®-R5F MCUs at up to 1.0GHz
  - 16K I-Cache, 16K D-Cache, 64K L2 TCM
  - Two Arm® Cortex®-R5F MCUs in isolated MCU subsystem
  - Four Arm® Cortex®-R5F MCUs in general compute partition
- Two C66x floating point DSP, up to 1.35GHz, 40GFLOPS, 160GOPS
- 3D GPU PowerVR® Rogue 8XE GE8430, up to 750MHz, 96GFLOPS, 6Gpix/sec
- Custom-designed interconnect fabric supporting near max processing entitlement

https://www.ti.com/lit/ds/symlink/tda4vm.pdf?ts=1727372255384&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FTDA4VM

24. The Accused Products comprise control circuitry, coupled to the plurality of processors. For example, the TDA4VM comprises a controller (e.g., an interrupt controller) coupled to the plurality of processor cores running operating environments and platforms, such as Linux, QNX (kernel architecture), Real-Time Operating Systems (RTOS), and TIOVX (OpenVX framework), that optimize workload scheduling, and support multitasking, interrupt handling, resource management, thread scheduling, and the like. For example, TIOVX further supports task priority, core affinity, and task affinity based scheduling.

Hardware accelerators	1 Deep learning accelerator, 1 Depth and Motion accelerator, 1 Vision Processing accelerator, 1 video encode/decode accelerator
Features	Vision Analytics
Operating system	Linux, QNX, RTOS

https://www.ti.com/product/TDA4VM#product-details

Develop MCU applications faster with TI-RTOS

TI-RTOS accelerates development schedules by eliminating the need to create basic system software functions from scratch. TI-RTOS scales from a real-time multitasking kernel - TI-RTOS Kernel - to a complete RTOS solution including additional middleware components, device drivers and power management. TI-RTOS and TI's ultra low-power MCUs combine to enable developers to design applications with much longer battery life. By providing essential system software components pre-tested and pre-integrated, TI-RTOS enables developers to focus on differentiating their application.

TI-RTOS builds on existing proven software components to ensure reliability and quality. It augments these with documentation, additional examples and APIs appropriate for multitasking development and integration testing to verify that all components work together. TI-RTOS applications may be developed with multiple Integrated Development Environments (IDEs) or toolchains, including Code Composer Studio™ IDE Desktop, Code Composer Studio IDE Cloud, Energia (an Arduino-compatible software environment), IAR Embedded Workbench IDE and GCC.

https://www.ti.com/tool/TI-RTOS-MCU

TIOVX allows users to create vision and compute applications using OpenVX API. These OpenVX applications can be executed on TI SoCs like TDA2x, TDA3x and TDA4x. TIOVX is fully conformant to OpenVX v1.1 specification. TIOVX also provides optimized OpenVX kernels for C66x DSP. An extension API allows users to integrate their own natively developed custom kernels and call them using OpenVX APIs. Examples showi

https://software-dl.ti.com/jacinto7/esd/processor-sdk-rtos-jacinto7/08_06_00_12/exports/docs/tiovx/docs/user_guide/index.html

25. The Accused Products comprise control circuitry comprising: core availability circuitry for determining if a core is available to execute a thread. For example, the TDA4VM comprises a controller including circuitry corresponding with functionality for determining if a core is available to execute a thread, such as a Multiprocessor Affinity Register (MPIDR), interrupt controller, power management circuitry, and/or other circuitry running a kernel architecture which detects core availability.

MPIDR_EL1, Multiprocessor Affinity Register

The MPIDR_EL1 characteristics are:

Purpose

In a multiprocessor system, provides an additional processor identification mechanism for scheduling purposes, and indicates whether the implementation includes the Multiprocessing Extensions.

This register is part of the Identification registers functional group.

https://yurichev.com/mirrors/ARMv8-A_Architecture_Reference_Manual_(Issue_A.a).pdf

c0, Multiprocessor Affinity Register

The MPIDR characteristics are:

Purpose Enables CPUs to be recognized and characterized within a twin-CPU system.

Usage constraints The MPIDR is:

- a read-only register
- accessible in Privileged mode only.

Configurations Available in all processor configurations.

Attributes See Table 4-7.

Figure 4-11 shows the MPIDR bit assignments.

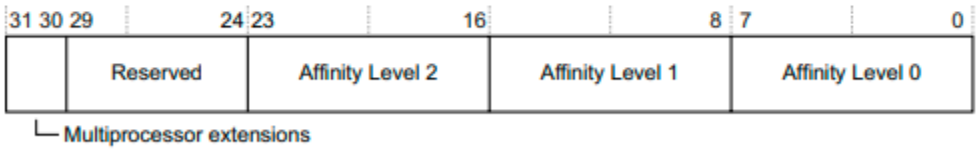


Figure 4-11 MPIDR bit assignments

Table 4-7 shows the MPIDR bit assignments.

https://yurichev.com/mirrors/ARMv8-A_Architecture_Reference_Manual_(Issue_A.a).pdf

Power management

TI-RTOS fully leverages the power management features of TI's ultra-low power microprocessors. TI-RTOS Kernel supports tickless operation, which greatly reduces the frequency of unnecessary wake-ups simply to serve the timer interrupt for the tick. When to suppress ticks is managed transparently by the TI-RTOS Kernel, freeing the user of the need to explicitly hardcode this into their application. For most ultra-low power MCUs, TI-RTOS also provides a power manager that controls peripheral clock gates and power domains and implements aggressive "standby" low-power modes that reduce power consumption to a tiny percentage of normal execution. The power manager is integrated with power-aware drivers and stacks which enable the optimal power-down state to be selected automatically when the processor enters the idle thread.

https://www.ti.com/lit/po/sprt646a/sprt646a.pdf?ts=1730961846024&ref_url=https%253A%252F%252Fwww.google.com%252F

Index	Module	Description
1	SCI	The SCI Resource Manager will incorrectly generate a warning log that an ACK flag is not present.
2	devnp-cpsw2g	The devnp-cpsw2g driver must have its core affinity set, such that the driver only runs on the first instance A72. This avoids a resource conflict that is under investigation.

https://software-dl.ti.com/jacinto7/esd/processor-sdk-qnx-jacinto7/07_00_00_05/exports/docs/release_notes_07_00_00.html

YIELD

YIELD is a hint instruction. Software with a multithreading capability can use a YIELD instruction to indicate to the PE that it is performing a task, for example a spin-lock, that could be swapped out to improve overall system performance. The PE can use this hint to suspend and resume multiple software threads if it supports the capability.

https://yurichev.com/mirrors/ARMv8-A_Architecture_Reference_Manual_(Issue_A.a).pdf

The YIELD instruction

The YIELD instruction provides a hint that the task performed by a thread is of low importance so that it could yield, see *YIELD* on page C5-773. This mechanism can be used to improve overall performance in an *Symmetric Multi-Threading* (SMT) or *Symmetric Multi-Processing* (SMP) system.

Examples of when the YIELD instruction might be used include a thread that is sitting in a spin-lock, or where the arbitration priority of the snoop but in an SMP system is modified. The YIELD instruction permits binary compatibility between SMT and SMP systems.

The YIELD instruction is a NOP (No Operation) hint instruction.

The YIELD instruction has no effect in a single-threaded system, but developers of such systems can use the instruction to flag its intended use for future migration to a multiprocessor or multithreading system. Operating systems can use YIELD in places where a yield hint is wanted, knowing that it will be treated as a NOP if there is no implementation benefit.

https://yurichev.com/mirrors/ARMv8-A_Architecture_Reference_Manual_(Issue_A.a).pdf

The Accused Products comprise control circuitry comprising: core affinity circuitry for determining if the core has an affinity for the thread, wherein said determining if the core has an affinity for the thread comprises counting a number of writes by one or more other threads to a cache associated with the core since the thread was last executed by the core. For example, the TDA4VM comprises a controller including circuitry corresponding with functionality for determining if the core has an affinity for the thread (e.g., based on an affinity score). Based on the information and belief, the arm architecture monitors the events, such as cache access, cache write-back, cache coherency, etc., counts the number of writes by one or more threads, and further interprets the potential thread affinity for the particular core. For example, upon information and belief, circuitry running the ARM architecture further monitors at least cache access, cache write-back, cache coherency, etc., counts the number of writes by one or more threads.

uint32_t	core_affinity If task runs on a SMP CPU then this value tells the affinity of task to a given core, Valid values are 0 .. max cores in the SMP CPU. when TIVX_TASK_AFFINITY_ANY is used OS decides the task affinity.
uint32_t	priority task priority for task associated with this target TIVX_TASK_PRI_HIGHEST is highest priority, TIVX_TASK_PRI_LOWEST is lowest priority

https://software-dl.ti.com/jacinto7/esd/processor-sdk-rtos-jacinto7/08_06_00_12/exports/docs/tiovx/docs/user_guide/index.html

```
71
82  #define TIVX_TASK_PRI_HIGHEST   (0u)
83
89  #define TIVX_TASK_PRI_LOWEST    (15u)
90
96  #define TIVX_TASK_AFFINITY_ANY      (0xFFFFu)
97
103 #define TIVX_MAX_TASK_NAME         (12u)
104
111 typedef void (VX_CALLBACK *tivx_task_main_f)(void *app_var);
112
113
119 typedef struct _tivx_task_t
120 {
123     void *tsk_handle;
124
128     uint8_t *stack_ptr;
129
132     uint32_t stack_size;
133
139     uint32_t core_affinity;
140
145     uint32_t priority;
146
148     tivx_task_main_f task_func;
149
151     void *app_var;
152
154     char  task_name[TIVX_MAX_TASK_NAME];
155 } tivx_task;
156
```

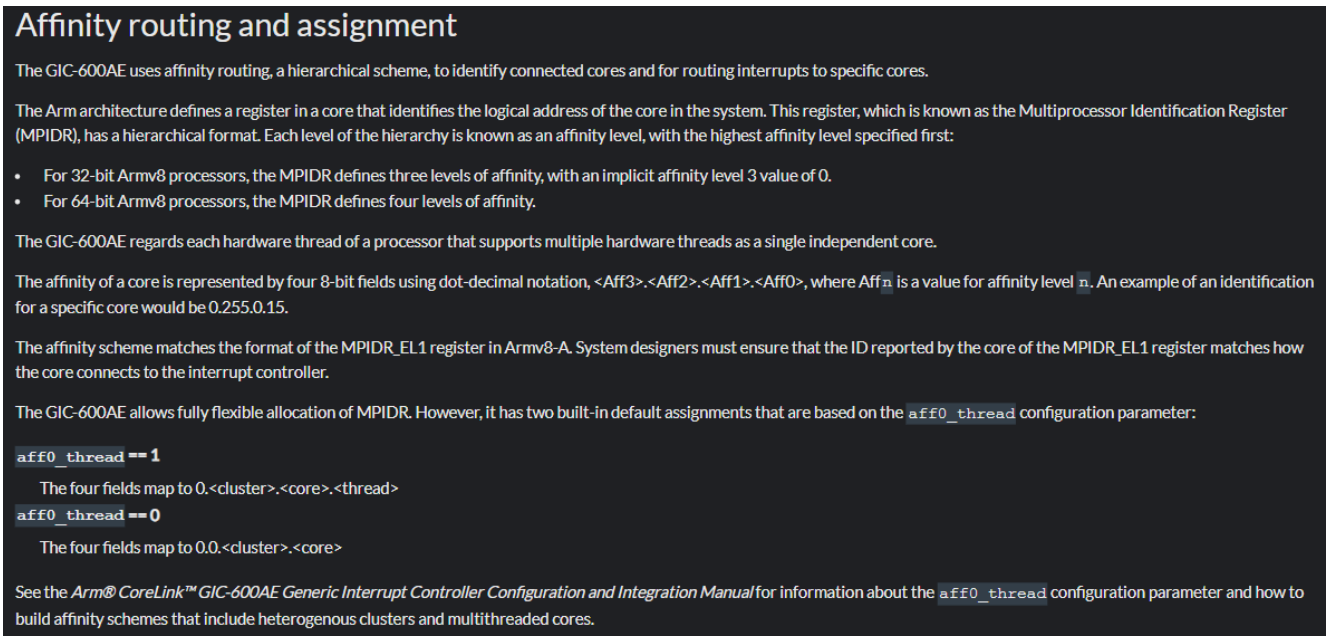
https://software-dl.ti.com/jacinto7/esd/processor-sdk-rtos-jacinto7/08_06_00_12/exports/docs/tiovx/docs/user_guide/index.html

https://software-dl.ti.com/jacinto7/esd/processor-sdk-rtos-jacinto7/08_06_00_12/exports/docs/tiovx/docs/user_guide/index.html

26. The Accused Products comprise control circuitry comprising: monitoring circuitry for monitoring one or more characteristics of the apparatus. For example, the TDA4VM comprises a controller including circuitry corresponding with functionality for monitoring one or more

characteristics, such as a power monitoring unit and/or other portions of control circuity, which measures at least task priority, power consumption, temperature, workload demand, and performance.

27. The Accused Products comprise control circuitry comprising: select circuitry for selecting one or more of the plurality of processors to execute the thread based on the affinity for the thread and the one or more characteristics of the apparatus. For example, the TDA4VM comprises a controller including circuitry corresponding with functionality for selecting a processor core on which to execute a task or workload based on an affinity score, and one or more characteristics, such as task priority, power consumption, temperature, workload demand, and/or performance.



Affinity routing and assignment

The GIC-600AE uses affinity routing, a hierarchical scheme, to identify connected cores and for routing interrupts to specific cores.

The Arm architecture defines a register in a core that identifies the logical address of the core in the system. This register, which is known as the Multiprocessor Identification Register (MPIDR), has a hierarchical format. Each level of the hierarchy is known as an affinity level, with the highest affinity level specified first:

- For 32-bit Armv8 processors, the MPIDR defines three levels of affinity, with an implicit affinity level 3 value of 0.
- For 64-bit Armv8 processors, the MPIDR defines four levels of affinity.

The GIC-600AE regards each hardware thread of a processor that supports multiple hardware threads as a single independent core.

The affinity of a core is represented by four 8-bit fields using dot-decimal notation, <Aff3>.<Aff2>.<Aff1>.<Aff0>, where Aff`n` is a value for affinity level `n`. An example of an identification for a specific core would be 0.255.0.15.

The affinity scheme matches the format of the MPIDR_EL1 register in Armv8-A. System designers must ensure that the ID reported by the core of the MPIDR_EL1 register matches how the core connects to the interrupt controller.

The GIC-600AE allows fully flexible allocation of MPIDR. However, it has two built-in default assignments that are based on the `aff0_thread` configuration parameter:

`aff0_thread` **== 1**

The four fields map to 0.<cluster>.<core>.<thread>

`aff0_thread` **== 0**

The four fields map to 0.0.<cluster>.<core>

See the *Arm® CoreLink™ GIC-600AE Generic Interrupt Controller Configuration and Integration Manual* for information about the `aff0_thread` configuration parameter and how to build affinity schemes that include heterogenous clusters and multithreaded cores.

https://developer.arm.com/documentation/101206/0003/Operation/Affinity-routing-and-assignment

28. TI has indirectly infringed and continues to indirectly infringe one or more claims of the ’165 Patent, as provided by 35 U.S.C. § 271(b), by inducing infringement by others, such as TI’s customers and end-users, in this District and elsewhere in the United States. For example,

TI's customers and end-users directly infringe, either literally or under the doctrine of equivalents, through their use of the inventions claimed in the '165 Patent. TI induces this direct infringement through its affirmative acts of manufacturing, selling, distributing, and/or otherwise making available the Accused Products, and providing instructions, documentation, and other information to customers and end-users suggesting that they use the Accused Products in an infringing manner, including technical support, SDKs, marketing, product manuals, advertisements, and online documentation. Because of TI's inducement, TI's customers and end-users use Accused Products in a way TI intends and directly infringe the '165 Patent. TI performs these affirmative acts with knowledge of the '165 Patent and with the intent, or willful blindness, that the induced acts directly infringe the '165 Patent.

29. TI has indirectly infringed and continues to indirectly infringe one or more claims of the '165 Patent, as provided by 35 U.S.C. § 271(c), by contributing to direct infringement by others, such as customers and end-users, in this District and elsewhere in the United States. TI's affirmative acts of selling and offering to sell the Accused Products in this District and elsewhere in the United States and causing the Accused Products to be manufactured, used, sold, and offered for sale contributes to others' use and manufacture of the Accused Products, such that the '165 Patent is directly infringed by others. The accused components within the Accused Products are material to the invention of the '165 Patent, are not staple articles or commodities of commerce, have no substantial non-infringing uses, and are known by TI to be especially made or adapted for use in the infringement of the '165 Patent. TI performs these affirmative acts with knowledge of the '165 Patent and with intent, or willful blindness, that they cause the direct infringement of the '165 Patent.

30. TI's infringement of the '165 Patent is willful, at least because it has and continues to knowingly and deliberately infringe the '165 Patent.

31. Ascale has suffered damages as a result of Defendant's direct and indirect infringement of the '165 Patent in an amount to be proved at trial.

32. Ascale has suffered, and will continue to suffer, irreparable harm as a result of Defendant's infringement of the '165 Patent for which there is no adequate remedy at law, unless Defendant's infringement is enjoined by this Court.

COUNT II
(Infringement of the '266 Patent)

33. Paragraphs 1 through 18 are incorporated by reference as if fully set forth herein.

34. Ascale has not licensed or otherwise authorized Defendant to make, use, offer for sale, sell, or import any products that embody the inventions of the '266 Patent.

35. Defendant has and continues to directly infringe the '266 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products including, but not limited to, processors, microcontrollers, and/or SoCs, comprising a PMU, PMIC, or other power management module, such as AM62x Sitara Processors.

36. For example, Defendant has and continues to directly infringe at least claim 1 of the '266 Patent by making, using, offering to sell, selling, and/or importing into the United States products that comprise a processing system comprising: a direct current to direct current (DC-DC) converter configured to generate a supply voltage when coupled to a battery; a memory module configured to store a plurality of operational instructions; a processing module, operatively coupled to the memory module, that is configured to execute the plurality of operational instructions, the processing module receiving power from the DC-DC converter; and a power

monitor circuit, operatively coupled to the DC-DC converter, that is distinct from and in communication with the processing module and that is configured to monitor the DC-DC converter and to power down the DC-DC converter and the processing module when a first error condition is detected in the DC-DC converter.

37. The Accused Products comprise a processing system. For example, the AM62x Sitara comprises a processor.

38. The Accused Products comprise a direct current to direct current (DC-DC) converter configured to generate a supply voltage when coupled to a battery. For example, the AM62x Sitara comprises synchronous stepdown DC-DC converters, linear regulators, general purpose I/Os, and multi-function pins configured to generate a supply voltage when coupled to a battery.

6 Detailed Description

6.1 Overview

The TPS6521905 provides three step-down converters, four LDOs, three general-purpose I/Os and three multi-Function pins. The system can be supplied by a single cell Li-Ion battery, two primary cells or a regulated supply. The device is characterized across a -40°C to +105°C temperature range, which makes the PMIC an excellent choice for various industrial applications.

https://www.ti.com/lit/ds/symlink/tps6521905.pdf?ts=1730802640926&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FTPS6521905

> The DC-DC converters are capable of 1x 3.5A and 2x 2 A. The converters require a small 470nH inductor, 4.7µF input capacitance, and a minimum 10µF output capacitance per rail depending on the switching mode configuration.

https://www.ti.com/lit/ds/symlink/tps6521905.pdf?ts=1730802640926&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FTPS6521905

39. The Accused Products comprise a memory module configured to store a plurality of operational instructions. For example, the AM62x Sitara comprises at least NVM memory,

DDR memory, cache memory, RAM, EEPROM, and/or flash memory configured to store a plurality of operational instructions.

6.6 NVM Programming

The TPS6521905 is part of Texas Instruments user-programmable PMICs. This device integrates a NVM memory that provides the ability to configure the power and digital resources. The NVM programming feature makes the TPS6521905 PMIC a flexible power solution to meet the requirements from different processors and SoCs. Programmable NVM fields include output voltages, sequencing, monitoring thresholds, GPIO control among others. OTA (Over The Air) programming, where EEPROM can be change directly without changing register settings, is not supported. Re-programming the NVM is done by first writing to the register map through the serial interface (I2C) and then saving the register settings into the NVM. The EEPROM of a device can only be programmed up to 1000 times. EEPROM values can only be changed if the input voltage (VSYS) is equal or greater than 3.3 V. The I2C pins must be pulled up to a 3.3V supply. At a high level, the programming flow can be described in three steps: determine your system requirements, update the register settings, save the new values into the NVM memory. Detailed information regarding the programming of the non-volatile memory is available in the *NVM Programming Guide* located under Technical documentation in the TPS6521905 product page on ti.com.

https://www.ti.com/lit/ds/symlink/tps6521905.pdf?ts=1730802640926&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FTPS6521905

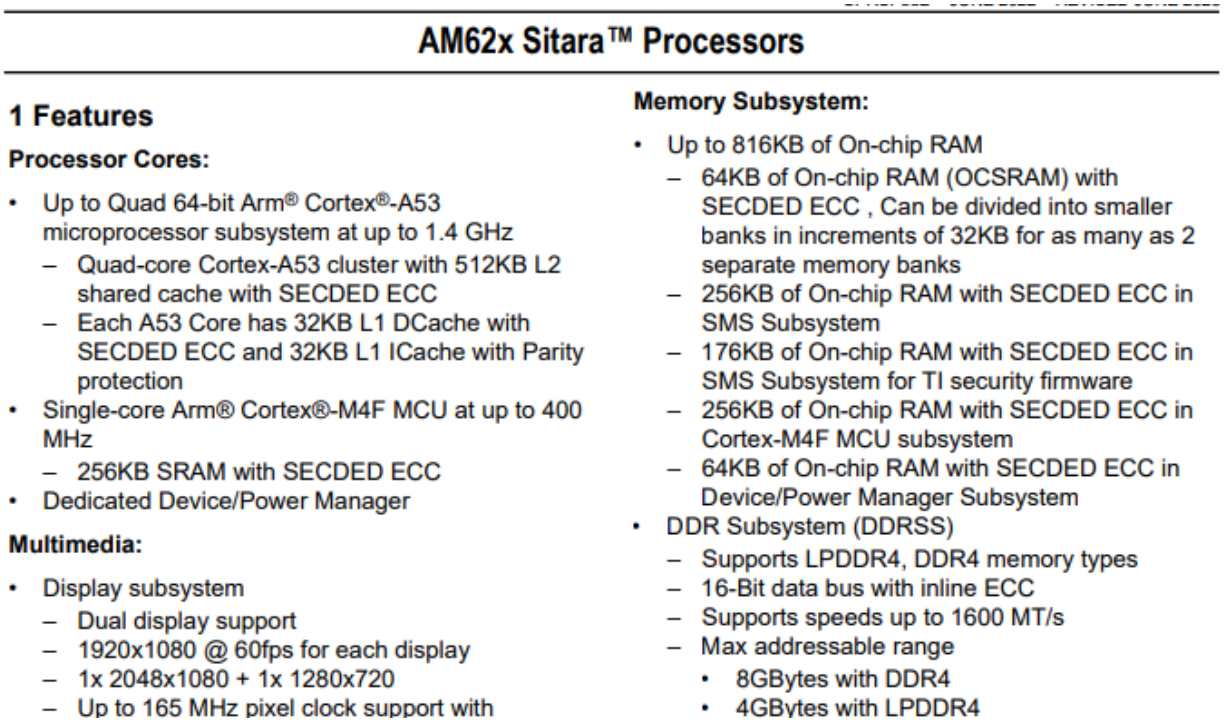
Memory Subsystem:

- Up to 816KB of On-chip RAM
  - 64KB of On-chip RAM (OCSRAM) with SECDED ECC , Can be divided into smaller banks in increments of 32KB for as many as 2 separate memory banks
  - 256KB of On-chip RAM with SECDED ECC in SMS Subsystem
  - 176KB of On-chip RAM with SECDED ECC in SMS Subsystem for TI security firmware
  - 256KB of On-chip RAM with SECDED ECC in Cortex-M4F MCU subsystem
  - 64KB of On-chip RAM with SECDED ECC in Device/Power Manager Subsystem
- DDR Subsystem (DDRSS)
  - Supports LPDDR4, DDR4 memory types
  - 16-Bit data bus with inline ECC
  - Supports speeds up to 1600 MT/s
  - Max addressable range
    - 8GBytes with DDR4
    - 4GBytes with LPDDR4

https://www.ti.com/lit/ds/symlink/am623.pdf

40. The Accused Products comprise a processing module, operatively coupled to the memory module, that is configured to execute the plurality of operational instructions, the

processing module receiving power from the DC-DC converter. For example, the AM62x Sitara comprises a processor (and cores thereof), each of which is operatively coupled to the aforementioned memory module, and interfaces with pins of a PMIC/PMU, or other power management chip through which it receives power from the DC-DC converter. For example, the VDD_Vcore pin of the processing module of the AM62x Sitara processor interfaces with at least a BUCK1 DC-DC converter.



AM62x Sitara™ Processors

1 Features

Processor Cores:

- Up to Quad 64-bit Arm® Cortex®-A53 microprocessor subsystem at up to 1.4 GHz
  - Quad-core Cortex-A53 cluster with 512KB L2 shared cache with SECDED ECC
  - Each A53 Core has 32KB L1 DCache with SECDED ECC and 32KB L1 ICache with Parity protection
- Single-core Arm® Cortex®-M4F MCU at up to 400 MHz
  - 256KB SRAM with SECDED ECC
- Dedicated Device/Power Manager

Multimedia:

- Display subsystem
  - Dual display support
  - 1920x1080 @ 60fps for each display
  - 1x 2048x1080 + 1x 1280x720
  - Up to 165 MHz pixel clock support with

Memory Subsystem:

- Up to 816KB of On-chip RAM
  - 64KB of On-chip RAM (OCSRAM) with SECDED ECC , Can be divided into smaller banks in increments of 32KB for as many as 2 separate memory banks
  - 256KB of On-chip RAM with SECDED ECC in SMS Subsystem
  - 176KB of On-chip RAM with SECDED ECC in SMS Subsystem for TI security firmware
  - 256KB of On-chip RAM with SECDED ECC in Cortex-M4F MCU subsystem
  - 64KB of On-chip RAM with SECDED ECC in Device/Power Manager Subsystem
- DDR Subsystem (DDRSS)
  - Supports LPDDR4, DDR4 memory types
  - 16-Bit data bus with inline ECC
  - Supports speeds up to 1600 MT/s
  - Max addressable range
    - 8GBytes with DDR4
    - 4GBytes with LPDDR4

https://www.ti.com/lit/ds/symlink/am623.pdf

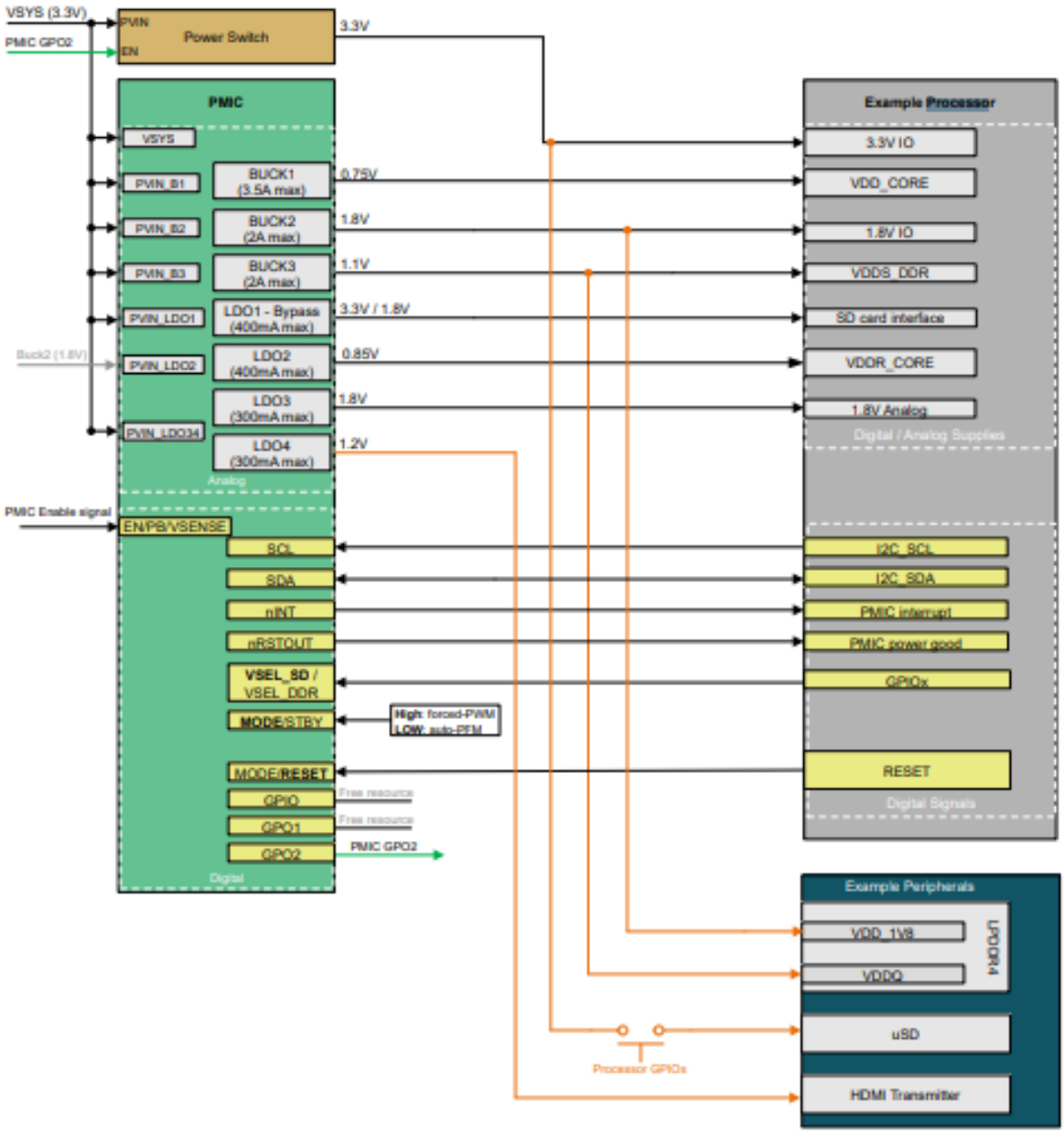


Figure 7-1. Example Power Map

https://www.ti.com/lit/ds/symlink/tps6521905.pdf?ts=1730802640926&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FTPS6521905

41. The Accused Products comprise a power monitor circuit, operatively coupled to the DC-DC converter, that is distinct from and in communication with the processing module and that is configured to monitor the DC-DC converter and to power down the DC-DC converter and the processing module when a first error condition is detected in the DC-DC converter. For example,

the AM62x Sitara comprises a PMIC, PMU or other power management module distinct from the processing module, that is operatively coupled to the DC-DC converter (e.g., a buck converter and/or LDO) and is configured to manage the DC-DC converter and to power down the DC-DC converter and the processing module when a first error condition is detected in the DC-DC converter (e.g., in an undervoltage or other error state).

> The integrated voltage supervisor monitors Buck 1–3 and LDO1–4 for undervoltage. The monitor has two sensitivity settings. A power good signal is provided to report the successful ramp of the power rails and GPIOs. The nRSTOUT pin is pulled low until the device enters ACTIVE state. When powering down from ACTIVE- or STBY-state, nRSTOUT is pulled low again. The nRSTOUT pin has an open-drain output. A fault-pin, nINT, notifies the SoC about faults.

https://www.ti.com/lit/ds/symlink/tps6521905.pdf?ts=1730802640926&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FTPS6521905

42. TI has indirectly infringed and continues to indirectly infringe one or more claims of the ’266 Patent, as provided by 35 U.S.C. § 271(b), by inducing infringement by others, such as TI’s customers and end-users, in this District and elsewhere in the United States. For example, TI’s customers and end-users directly infringe, either literally or under the doctrine of equivalents, through their use of the inventions claimed in the ’266 Patent. TI induces this direct infringement through its affirmative acts of manufacturing, selling, distributing, and/or otherwise making available the Accused Products, and providing instructions, documentation, and other information to customers and end-users suggesting that they use the Accused Products in an infringing manner, including technical support, SDKs, marketing, product manuals, advertisements, and online documentation. Because of TI’s inducement, TI’s customers and end-users use Accused Products in a way TI intends and directly infringe the ‘266 Patent. TI performs these affirmative acts with knowledge of the ’266 Patent and with the intent, or willful blindness, that the induced acts directly infringe the ’266 Patent.

43. TI has indirectly infringed and continues to indirectly infringe one or more claims of the ’266 Patent, as provided by 35 U.S.C. § 271(c), by contributing to direct infringement by others, such as customers and end-users, in this District and elsewhere in the United States. TI’s affirmative acts of selling and offering to sell the Accused Products in this District and elsewhere in the United States and causing the Accused Products to be manufactured, used, sold, and offered for sale contributes to others’ use and manufacture of the Accused Products such that the ’266 Patent is directly infringed by others. The accused components within the Accused Products are material to the invention of the ’266 Patent, are not staple articles or commodities of commerce, have no substantial non-infringing uses, and are known by TI to be especially made or adapted for use in the infringement of the ’266 Patent. TI performs these affirmative acts with knowledge of the ’266 Patent and with intent, or willful blindness, that they cause the direct infringement of the ’266 Patent.

44. TI’s infringement of the ’266 Patent is willful, at least because it has and continues to knowingly and deliberately infringe the ’266 Patent.

45. Ascale has suffered damages as a result of Defendant’s direct and indirect infringement of the ’266 Patent in an amount to be proved at trial.

46. Ascale has suffered, and will continue to suffer, irreparable harm as a result of Defendant’s infringement of the ’266 Patent for which there is no adequate remedy at law, unless Defendant’s infringement is enjoined by this Court.

COUNT III
(Infringement of the ’254 Patent)

47. Paragraphs 1 through 18 are incorporated by reference as if fully set forth herein.

48. Ascale has not licensed or otherwise authorized Defendant to make, use, offer for sale, sell, or import any products that embody the inventions of the ’254 Patent.

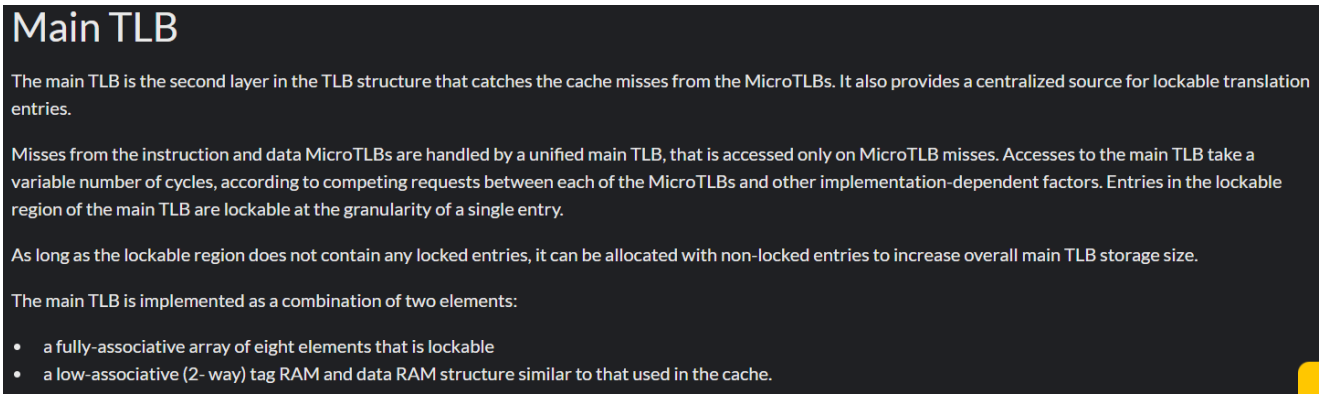
49. Defendant has and continues to directly infringe the ’254 Patent, either literally or under the doctrine of equivalents, without authority and in violation of 35 U.S.C. § 271, by making, using, offering to sell, selling, and/or importing into the United States the Accused Products including, but not limited to, ARM-based processors, such as TDA4VEN Jacinto Processors.

50. For example, Defendant has and continues to directly infringe at least claim 1 of the ’254 Patent by performing a method of operating a processor, comprising: translating, using an associated translation lookaside buffer, a first virtual address into a first physical address through a first entry number, associated with a first multi-bit translation lookaside buffer way and a first multi-bit translation lookaside buffer index, in the translation lookaside buffer; translating, using the translation lookaside buffer, a second virtual address into a second physical address through a second entry number, associated with a second multi-bit translation lookaside buffer way and a second multi-bit translation lookaside buffer index, in the translation lookaside buffer; and determining that the first and second virtual addresses point to a same physical address in memory and reference the same data by determining the first multi-bit translation lookaside buffer way is equal to the second multi-bit translation lookaside buffer way and the first multi-bit translation lookaside buffer index is equal to the second multi-bit translation lookaside buffer index.

51. The Accused Products perform a method of operating a processor. For example, the TDA4VEN Jacinto comprises an ARM-based processor.

52. The Accused Products perform a method of translating, using an associated translation lookaside buffer, a first virtual address into a first physical address through a first entry number, associated with a first multi-bit translation lookaside buffer way and a first multi-bit translation lookaside buffer index, in the translation lookaside buffer. For example, TDA4VEN

processors include ARM Cortex-A53 cores based on ARM-v8 architecture, in which a memory management unit (MMU) translates a first virtual address into a first physical address. For example, the translation lookaside buffer (TLB) in the product caches recently used translations from virtual addresses to physical addresses (i.e., translating virtual addresses to physical addresses). When the processor generates a memory access request, the first virtual address is translated by looking up a translation entry in the MicroTLB (for instruction/data access) or the Main TLB (for handling misses from the MicroTLBs). Based on information and belief, an entry number is associated with a first multi-bit translation lookaside buffer way and a first multi-bit translation lookaside buffer index, in the translation lookaside buffer.



Main TLB

The main TLB is the second layer in the TLB structure that catches the cache misses from the MicroTLBs. It also provides a centralized source for lockable translation entries.

Misses from the instruction and data MicroTLBs are handled by a unified main TLB, that is accessed only on MicroTLB misses. Accesses to the main TLB take a variable number of cycles, according to competing requests between each of the MicroTLBs and other implementation-dependent factors. Entries in the lockable region of the main TLB are lockable at the granularity of a single entry.

As long as the lockable region does not contain any locked entries, it can be allocated with non-locked entries to increase overall main TLB storage size.

The main TLB is implemented as a combination of two elements:

- a fully-associative array of eight elements that is lockable
- a low-associative (2- way) tag RAM and data RAM structure similar to that used in the cache.

https://developer.arm.com/documentation/ddi0360/f/level-1-memory-system/tlb-organization/main-tlb

3 Translating a virtual address to a physical address

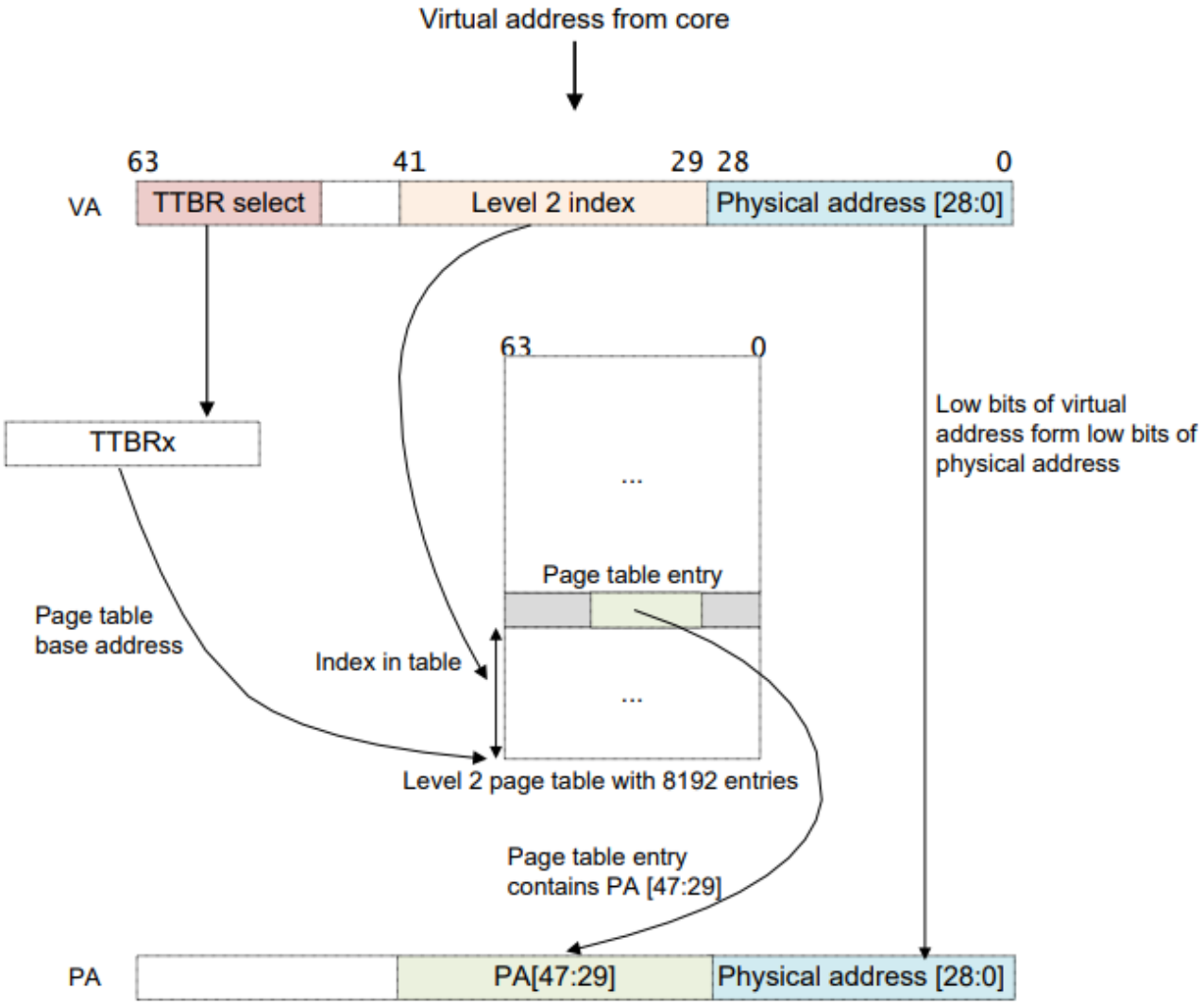
When the processor issues a virtual address for an instruction fetch, or data access, the MMU hardware translates the virtual address to the corresponding physical address. For a virtual address in an n -bit address space, the top 64-*n* bits VA[63:n] must be all 0s or 1s, otherwise the address triggers a fault.

The least significant bits are then used to give an offset within the selected section, so that the MMU combines the physical address bits from the block table entry with the least significant bits from the original address to produce the final address.

In a simple address translation involving only one level of look-up, and assumes that we are using a 64KB granule with a 42-bit virtual address space. The MMU translates a virtual address as follows:

1. If VA[63:42] = 1 then TTBR1 is used for the base address for the first translation table. When VA[63:42] = 0, TTBR0 is used for the base address for the first translation table.
2. The translation table contains 8192 ×64-bit translation table entries, and is indexed using VA[41:29]. The MMU reads the pertinent Level 2 translation table entry from the table.
3. The MMU checks the translation table entry for validity and whether the requested memory access is allowed. Assuming it is valid, the memory access is allowed.
4. In the following figure, the translation table entry refers to a 512MB page (it is a block descriptor).

https://documentation-service.arm.com/static/5efa1d23dbdee951c1ccdec5

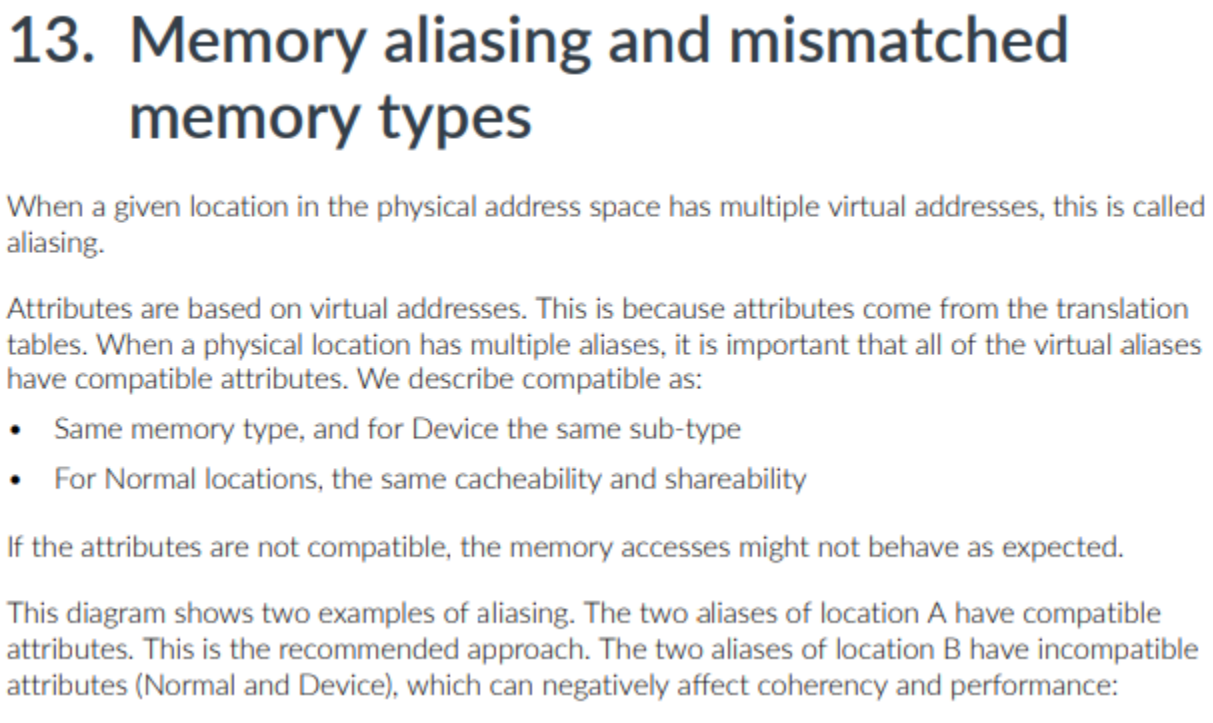


https://documentation-service.arm.com/static/5efa1d23dbdee951c1ccdec5

53. The Accused Products perform a method of translating, using the translation lookaside buffer, a second virtual address into a second physical address through a second entry number, associated with a second multi-bit translation lookaside buffer way and a second multi-bit translation lookaside buffer index, in the translation lookaside buffer. For example, as shown above, TDA4VEN processors include a translation lookaside buffer that similarly translates a second virtual address into a second physical address through a second entry number associated

with a second multi-bit translation lookaside buffer way and a second multi-bit translation lookaside buffer index, in the translation lookaside buffer.

54. The Accused Products perform a method of determining that the first and second virtual addresses point to a same physical address in memory and reference same data by determining the first multi-bit translation lookaside buffer way is equal to the second multi-bit translation lookaside buffer way and the first multi-bit translation lookaside buffer index is equal to the second multi-bit translation lookaside buffer index. For example, TDA4VEN processors support memory aliasing in which one physical address supports multiple virtual addresses. As a further example, TDA4VEN processors support instructions including IPAS2E1 (TLB invalidate by IPA) which invalidates all TLB entries associated with an intermediate physical address, which, upon information and belief, involves determining that the first and second virtual addresses point to a same physical address in memory.



13. Memory aliasing and mismatched memory types

When a given location in the physical address space has multiple virtual addresses, this is called aliasing.

Attributes are based on virtual addresses. This is because attributes come from the translation tables. When a physical location has multiple aliases, it is important that all of the virtual aliases have compatible attributes. We describe compatible as:

- Same memory type, and for Device the same sub-type
- For Normal locations, the same cacheability and shareability

If the attributes are not compatible, the memory accesses might not behave as expected.

This diagram shows two examples of aliasing. The two aliases of location A have compatible attributes. This is the recommended approach. The two aliases of location B have incompatible attributes (Normal and Device), which can negatively affect coherency and performance:

https://documentation-service.arm.com/static/63a43e333f28e5456434e18b?token=

The following table lists TLB configuration instructions:

TLB invalidate	Variant	Description
TLBI	ALLEn	TLB invalidate All, ELn.
	ALLEnIS	TLB invalidate All, ELn, Inner Shareable.
	ASIDE1	TLB invalidate by ASID, EL1.
	ASIDE1IS	TLB invalidate by ASID, EL1, Inner Shareable.
	IPAS2E1	TLB invalidate by IPA, Stage 2, EL1.

https://documentation-service.arm.com/static/5efa1d23dbdee951c1ccdec5

55. TI has indirectly infringed and continues to indirectly infringe one or more claims of the '254 Patent, as provided by 35 U.S.C. § 271(b), by inducing infringement by others, such as TI's customers and end-users, in this District and elsewhere in the United States. For example, TI's customers and end-users directly infringe, either literally or under the doctrine of equivalents, through their use of the inventions claimed in the '254 Patent. TI induces this direct infringement through its affirmative acts of manufacturing, selling, distributing, and/or otherwise making available the Accused Products, and providing instructions, documentation, and other information to customers and end-users suggesting that they use the Accused Products in an infringing manner, including technical support, SDKs, marketing, product manuals, advertisements, and online documentation. Because of TI's inducement, TI's customers and end-users use Accused Products in a way TI intends and directly infringe the '254 Patent. TI performs these affirmative acts with knowledge of the '254 Patent and with the intent, or willful blindness, that the induced acts directly infringe the '254 Patent.

56. TI has indirectly infringed and continues to indirectly infringe one or more claims of the '254 Patent, as provided by 35 U.S.C. § 271(c), by contributing to direct infringement by others, such as customers and end-users, in this District and elsewhere in the United States. TI's affirmative acts of selling and offering to sell the Accused Products in this District and elsewhere

in the United States and causing the Accused Products to be manufactured, used, sold, and offered for sale contributes to others' use and manufacture of the Accused Products, such that the '254 Patent is directly infringed by others. The accused components within the Accused Products are material to the invention of the '254 Patent, are not staple articles or commodities of commerce, have no substantial non-infringing uses, and are known by TI to be especially made or adapted for use in the infringement of the '254 Patent. TI performs these affirmative acts with knowledge of the '254 Patent and with intent, or willful blindness, that they cause the direct infringement of the '254 Patent.

57. TI's infringement of the 254 Patent is willful, at least because it has and continues to knowingly and deliberately infringe the '254 Patent.

58. Ascale has suffered damages as a result of Defendant's direct and indirect infringement of the '254 Patent in an amount to be proved at trial.

59. Ascale has suffered, and will continue to suffer, irreparable harm as a result of Defendant's infringement of the '254 Patent for which there is no adequate remedy at law, unless Defendant's infringement is enjoined by this Court.

DEMAND FOR JURY TRIAL

Plaintiff hereby demands a jury for all issues so triable.

PRAYER FOR RELIEF

WHEREFORE, Ascale prays for relief against Defendant as follows:

a. Entry of judgment declaring that Defendant has directly and/or indirectly infringed one or more claims of each of the Patents-in-Suit;

b. An order pursuant to 35 U.S.C. § 283 permanently enjoining Defendant, its officers, agents, servants, employees, attorneys, and those persons in active concert or

participation with them, from further acts of infringement of the Patents-in-Suit;

c. An order awarding damages sufficient to compensate Ascale for Defendant's infringement of the Patents-in-Suit, but in no event less than a reasonable royalty, together with interest and costs;

d. Entry of judgment declaring that this case is exceptional and awarding Ascale its costs and reasonable attorney fees under 35 U.S.C. § 285;

e. Entry of judgment awarding treble damages pursuant to 35 U.S.C. § 284 for Defendant's willful infringement of one or more of the Patents-in-Suit; and

f. Such other and further relief as the Court deems just and proper.

Dated: February 27, 2025

Respectfully submitted,

/s/ *Vincent J. Rubino, III*

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