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BY: *P*

IN THE UNITED STATES DISTRICT COURT  
FOR THE WESTERN DISTRICT OF TEXAS  
AUSTIN DIVISION

MOTOROLA, INC.

Plaintiff,

v.

MICRON TECHNOLOGY, INC.

Defendant.

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CAUSE NO. \_\_\_\_\_

A04 CA 007  
*4V*

**COMPLAINT AND DEMAND FOR JURY TRIAL**

COMES NOW the Plaintiff, and for its Complaint against Defendant, states and alleges as follows:

**THE PARTIES**

1. Plaintiff, Motorola, Inc. ("Motorola") is incorporated in the state of Delaware, having a principal place of business at 6501 William Cannon Drive West, Austin, Texas, 78735.
2. Upon information and belief, Defendant, Micron Technology, Inc., ("Defendant Micron") is incorporated in the state of Delaware and is doing business in this District at One Chisholm Trail, Suite 2200, Round Rock, Texas, 78681.

**JURISDICTION AND VENUE**

3. This is a claim of patent infringement arising under the Acts of Congress relating to patents, 35 U.S.C. §§ 271; 282-285.
4. This Court has jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).
5. Venue is proper in this Court pursuant to 28 U.S.C. §§ 1391 and 1400.

6. Personal jurisdiction is appropriate over Defendant Micron because it transacts business in this state and has committed tortious activities against Plaintiff Motorola in this state. To the extent that the tortious activities of Micron have occurred outside the State of Texas, they have resulted in injury to Motorola in this state. Among other things, this Court has personal jurisdiction over Micron pursuant to Texas's long-arm statute, codified at Tex. Civ. Prac. & Rem. Code Ann. § 17.042.

### **GENERAL ALLEGATIONS**

7. Plaintiff Motorola is a global leader in designing and manufacturing semiconductor, wireless, automotive and broadband devices. For the past 75 years, Motorola has consistently developed innovative technologies and solutions for a variety of products from car radios to cellular telephones to semiconductor chips.

8. In 1949, Plaintiff Motorola established a small research and development operation in Phoenix, Arizona to investigate the new field of transistors and solid-state technology. More than a half-century later, Motorola's semiconductor solutions are used for wireless communications, networking applications, automotive applications, and other standard products that deliver embedded processing and connectivity capabilities for millions of devices throughout the world. For example, Motorola's communications processors manage a large percentage of the world's Internet traffic. With billions of Motorola semiconductors currently in use, Motorola's embedded electronic solutions are found in most of today's advanced technology products.

9. Through its early understanding of the enormous potential of the transistor and pioneering technology developed along the way, Plaintiff Motorola has become an industry

leader in the semiconductor field. As a world leading producer of embedded processors, Motorola's semiconductor devices enable companies to develop smarter, faster, simpler, safer, and better products for people and businesses around the globe.

10. As a result of its continued investments in new technologies, Plaintiff Motorola owns a large portfolio of patents in the semiconductor and memory industry. This portfolio includes the following United States Patents (collectively the "Motorola Patents"):

- a. U.S. Patent No. 5,367,494 entitled "Randomly Accessible Memory Having Time Overlapping Memory Accesses,"
- b. U.S. Patent Nos. 5,162,672, 5,294,845 and 5,859,541 entitled "Data Processor Having An Output Terminal With Selectable Output Impedances,"
- c. U.S. Patent No. 4,791,615 entitled "Memory With Redundancy And Predecoded Signals,"
- d. U.S. Patent No. 5,455,200 entitled "Method For Making A Lead-On-Chip Semiconductor Device Having Peripheral Bond Pads,"
- e. U.S. Patent No. 5,606,275 entitled "Buffer Circuit Having Variable Output Impedance,"
- f. U.S. Patent No. 5,750,440 entitled "Apparatus And Method For Dynamically Mixing Slurry For Chemical Mechanical Polishing,"
- g. U.S. Patent No. 5,798,937 entitled "Method And Apparatus For Forming Redundant Vias Between Conductive Layers Of An Integrated Circuit," and
- h. U.S. Patent No. 5,851,927 entitled "Method Of Forming A Semiconductor Device By DUV Resist Patterning."

11. Since Plaintiff Motorola's patents cover fundamental aspects of semiconductor technology, many of these patents are quite valuable. Indeed, these patents cover a wide array of standard memory technologies in use today. Accordingly, other companies that develop and sell

semiconductor products license Motorola's patents in order to take advantage of the technology invented by Motorola.

12. Plaintiff Motorola previously notified Defendant Micron that several of Motorola's patents covered a significant number of Micron's semiconductor products and further inquired as to Micron's interest in a license under these patents.

13. Employees of Plaintiff Motorola traveled to Boise, Idaho, to meet with Defendant Micron to discuss such a license. After a half-day meeting, Micron stated that it did not have an interest in licensing Motorola's patents. Since that meeting, Motorola made additional attempts to engage Micron in further negotiations, but Micron refused to meet with Motorola.

14. Defendant Micron has thereafter continued to make and sell semiconductor products that incorporate Motorola's patented technology without Motorola's consent.

**COUNT I: INFRINGEMENT OF U.S. PATENT NO. 5,367,494**

15. On November 22, 1994, U.S. Patent No. 5,367,494 entitled "Randomly Accessible Memory Having Time Overlapping Memory Accesses," was duly issued to Plaintiff Motorola as assignee of the inventors Michael C. Shebanow, Mitchell K. Alsup, Hunter L. Scales, and George P. Hoekstra. Motorola is the owner of the entire right, title and interest in and to U.S. Patent No. 5,367,494, and has been and still is the owner thereof. U.S. Patent No. 5,367,494 is attached as Exhibit A.

16. U.S. Patent No. 5,367,494 teaches how to put multiple banks of memory on a single integrated circuit. Prior to the invention described in U.S. Patent No. 5,367,494, creating multiple-banked memory systems required several discrete memory chips. The creation of a single integrated circuit containing multiple banks of memory and the support circuitry necessary

to allow these memory banks to work in conjunction with one another was a tremendous advance in memory technology. Upon information and belief, almost all modern dynamic random access memories (DRAMs), including most, if not all, of the DRAM families manufactured in the last several years by Defendant Micron (*i.e.*, synchronous dynamic random access memory (SDRAM), dual data rate memory (DDR), second-generation dual data rate memory (DDR2), and Rambus dynamic random access memory (RDRAM)) implement the technology described in U.S. Patent No. 5,367,494.

17. Upon information and belief, Defendant Micron is liable for direct, contributory, and inducing infringement of U.S. Patent No. 5,367,494, as defined under 35 U.S.C. § 271 *et seq.*

18. Plaintiff Motorola has been damaged by Defendant Micron's foregoing infringement of U.S. Patent No. 5,367,494 and will continue to be damaged in the future unless Micron is permanently enjoined from infringing said patent.

19. Upon information and belief, Defendant Micron is aware that U.S. Patent No. 5,367,494 was duly and legally issued and is aware or should be aware that Micron's actions infringe U.S. Patent No. 5,367,494.

20. Upon information and belief, Defendant Micron's foregoing infringement of U.S. Patent No. 5,367,494 is now and has been intentional, willful, and deliberate, and will continue unless enjoined by the Court.

**COUNT II: INFRINGEMENT OF U.S. PATENT NOS. 5,162,672,  
5,294,845, AND 5,859,541**

21. On November 10, 1992, March 15, 1994, and January 12, 1999, U.S. Patent Nos. 5,162,672, 5,294,845 and 5,859,541, each entitled "Data Processor Having An Output Terminal With Selectable Output Impedances," were duly issued to Plaintiff Motorola as assignee of the

inventors Steven Craig McMahan, Kenneth Charles Scheuer, William Burl Ledbetter, Jr., Michael Gordon Gallup, and James George Gay. Motorola is the owner of the entire right, title and interest in and to U.S. Patent Nos. 5,162,672, 5,294,845 and 5,859,541, and has been and still is the owner thereof. U.S. Patent Nos. 5,162,672, 5,294,845 and 5,859,541 are attached as Exhibits B, C, and D.

22. U.S. Patent Nos. 5,162,672, 5,294,845 and 5,859,541 describe a memory device that has multiple output buffers which can be selectively activated by a user. This manner of operation allows the impedance of an output terminal to be varied, and, consequently, gives a system designer more flexibility in designing the memory subsystem of a computer system, such as the memory subsystem of a personal computer. Upon information and belief, Defendant Micron implements this technology in its DDR, DDR2, and RDRAM memory devices.

23. Upon information and belief, Defendant Micron is liable for direct, contributory, and inducing infringement of U.S. Patent Nos. 5,162,672, 5,294,845 and 5,859,541, as defined under 35 U.S.C. § 271 *et seq.*

24. Plaintiff Motorola has been damaged by Defendant Micron's foregoing infringement of U.S. Patent Nos. 5,162,672, 5,294,845 and 5,859,541 and will continue to be damaged in the future unless Micron is permanently enjoined from infringing said patents.

25. Upon information and belief, Defendant Micron is aware that U.S. Patent Nos. 5,162,672, 5,294,845 and 5,859,541 were duly and legally issued and is aware or should be aware that Micron's actions infringe U.S. Patent Nos. 5,162,672, 5,294,845 and 5,859,541.

26. Upon information and belief, Defendant Micron's foregoing infringement of U.S. Patent Nos. 5,162,672, 5,294,845 and 5,859,541 is now and has been intentional, willful, and deliberate, and will continue unless enjoined by the Court.

**COUNT III: INFRINGEMENT OF U.S. PATENT NO. 4,791,615**

27. On December 13, 1998, U.S. Patent No. 4,791,615 entitled "Memory With Redundancy And Predecoded Signals," was duly issued to Plaintiff Motorola as assignee of the inventors Perry H. Pelley, III and Bruce L. Morton. Motorola is the owner of the entire right, title and interest in and to U.S. Patent No. 4,791,615, and has been and still is the owner thereof. U.S. Patent No. 4,791,615 is attached as Exhibit E.

28. U.S. Patent No. 4,791,615 describes a clocked memory device which uses predecoded address signals to access redundant memory cells in the memory. Upon information and belief, the teachings of U.S. Patent No. 4,791,615 have found their way into a variety of modern memory devices, such as the DRAMs, designed and manufactured by Defendant Micron.

29. Upon information and belief, Defendant Micron is liable for direct, contributory, and inducing infringement of U.S. Patent No. 4,791,615, as defined under 35 U.S.C. § 271 *et seq.*

30. Plaintiff Motorola has been damaged by Defendant Micron's foregoing infringement of U.S. Patent No. 4,791,615 and will continue to be damaged in the future unless Micron is permanently enjoined from infringing said patent.

31. Upon information and belief, Defendant Micron is aware that U.S. Patent No. 4,791,615 was duly and legally issued and is aware or should be aware that Micron's actions infringe U.S. Patent No. 4,791,615.

32. Upon information and belief, Defendant Micron's foregoing infringement of U.S. Patent No. 4,791,615 is now and has been intentional, willful, and deliberate, and will continue unless enjoined by the Court.

**COUNT IV: INFRINGEMENT OF U.S. PATENT NO. 5,455,200**

33. On October 3, 1995, U.S. Patent No. 5,455,200 entitled "Method For Making A Lead-On-Chip Semiconductor Device Having Peripheral Bond Pads," was duly issued to Plaintiff Motorola as assignee of the inventors Charles G. Bigler, James J. Casto, Michael B. McShane, and David D. Afshar. Motorola is the owner of the entire right, title and interest in and to U.S. Patent No. 5,455,200, and has been and still is the owner thereof. U.S. Patent No. 5,455,200 is attached as Exhibit F.

34. Upon information and belief, Defendant Micron is liable for direct, contributory, and inducing infringement of U.S. Patent No. 5,455,200 as defined under 35 U.S.C. § 271 *et seq.*

35. Plaintiff Motorola has been damaged by Defendant Micron's foregoing infringement of U.S. Patent No. 5,455,200 and will continue to be damaged in the future unless Micron is permanently enjoined from infringing said patent.

36. Upon information and belief, Defendant Micron is aware that U.S. Patent No. 5,455,200 was duly and legally issued and is aware or should be aware that Micron's actions infringe U.S. Patent No. 5,455,200.

37. Upon information and belief, Defendant Micron's foregoing infringement of U.S. Patent No. 5,455,200 is now and has been intentional, willful, and deliberate, and will continue unless enjoined by the Court.



**COUNT V: INFRINGEMENT OF U.S. PATENT NO. 5,606,275**

38. On February 25, 1997, U.S. Patent No. 5,606,275 entitled "Buffer Circuit Having Variable Output Impedance," was duly issued to Plaintiff Motorola as assignee of the inventors Ali R. Farhang and Scott G. Nogle. Motorola is the owner of the entire right, title and interest in and to U.S. Patent No. 5,606,275, and has been and still is the owner thereof. U.S. Patent No. 5,606,275 is attached as Exhibit G.

39. Upon information and belief, Defendant Micron is liable for direct, contributory, and inducing infringement of U.S. Patent No. 5,606,275, as defined under 35 U.S.C. § 271 *et seq.*

40. Plaintiff Motorola has been damaged by Defendant Micron's foregoing infringement of U.S. Patent No. 5,606,275 and will continue to be damaged in the future unless Micron is permanently enjoined from infringing said patent.

41. Upon information and belief, Defendant Micron is aware that U.S. Patent No. 5,606,275 was duly and legally issued and is aware or should be aware that Micron's actions infringe U.S. Patent No. 5,606,275.

42. Upon information and belief, Defendant Micron's foregoing infringement of U.S. Patent No. 5,606,275 is now and has been intentional, willful, and deliberate, and will continue unless enjoined by the Court.

**COUNT VI: INFRINGEMENT OF U.S. PATENT NO. 5,750,440**

43. On May 12, 1998, U.S. Patent No. 5,750,440 entitled "Apparatus And Method For Dynamically Mixing Slurry For Chemical Mechanical Polishing," was duly issued to Plaintiff Motorola as assignee of the inventors James F. Vanell, Steven D. Ward, and James M. Mullins.

Motorola is the owner of the entire right, title and interest in and to U.S. Patent No. 5,750,440, and has been and still is the owner thereof. U.S. Patent No. 5,750,440 is attached as Exhibit H.

44. Upon information and belief, Defendant Micron is liable for direct, contributory, and inducing infringement of U.S. Patent No. 5,750,440, as defined under 35 U.S.C. § 271 *et seq.*

45. Plaintiff Motorola has been damaged by Defendant Micron's foregoing infringement of U.S. Patent No. 5,750,440 and will continue to be damaged in the future unless Micron is permanently enjoined from infringing said patent.

46. Upon information and belief, Defendant Micron is aware that U.S. Patent No. 5,750,440 was duly and legally issued and is aware or should be aware that Micron's actions infringe U.S. Patent No. 5,750,440.

47. Upon information and belief, Defendant Micron's foregoing infringement of U.S. Patent No. 5,750,440 is now and has been intentional, willful, and deliberate, and will continue unless enjoined by the Court.

**COUNT VII: INFRINGEMENT OF U.S. PATENT NO. 5,798,937**

48. On August 25, 1998, U.S. Patent No. 5,798,937 entitled "Method And Apparatus For Forming Redundant Vias Between Conductive Layers Of An Integrated Circuit," was duly issued to Plaintiff Motorola as assignee of the inventors Gabriel Bracha, Eytan Weissberger, Yehuda Volpert, and Ilan Algor. Motorola is the owner of the entire right, title and interest in and to U.S. Patent No. 5,798,937, and has been and still is the owner thereof. U.S. Patent No. 5,798,937 is attached as Exhibit I.

49. Upon information and belief, Defendant Micron is liable for direct, contributory, and inducing infringement of U.S. Patent No. 5,798,937, as defined under 35 U.S.C. § 271 *et seq.*

50. Motorola has been damaged by Defendant Micron's foregoing infringement of U.S. Patent No. 5,798,937 and will continue to be damaged in the future unless Micron is permanently enjoined from infringing said patent.

51. Upon information and belief, Defendant Micron is aware that U.S. Patent No. 5,798,937 was duly and legally issued and is aware or should be aware that Micron's actions infringe U.S. Patent No. 5,798,937.

52. Upon information and belief, Defendant Micron's foregoing infringement of U.S. Patent No. 5,798,937 is now and has been intentional, willful, and deliberate, and will continue unless enjoined by the Court.

**COUNT VIII: INFRINGEMENT OF U.S. PATENT NO. 5,851,927**

53. On December 22, 1998, U.S. Patent No. 5,851,927 entitled "Method Of Forming A Semiconductor Device By DUV Resist Patterning," was duly issued to Plaintiff Motorola as assignee of the inventors Paul Kevin Cox, Thy Ngu-Uyen Tran, Samuel Jay Wright, and Judith Sobresky. Motorola is the owner of the entire right, title and interest in and to U.S. Patent No. 5,851,927, and has been and still is the owner thereof. U.S. Patent No. 5,851,927 is attached as Exhibit J.

54. Upon information and belief, Defendant Micron is liable for direct, contributory, and inducing infringement of U.S. Patent No. 5,851,927, as defined under 35 U.S.C. § 271 *et seq.*

55. Plaintiff Motorola has been damaged by Defendant Micron's foregoing infringement of U.S. Patent No. 5,851,927 and will continue to be damaged in the future unless Micron is permanently enjoined from infringing said patent.

56. Upon information and belief, Defendant Micron is aware that U.S. Patent No. 5,851,927 was duly and legally issued and is aware or should be aware that Micron's actions infringe U.S. Patent No. 5,851,927.

57. Upon information and belief, Defendant Micron's foregoing infringement of U.S. Patent No. 5,851,927 is now and has been intentional, willful, and deliberate, and will continue unless enjoined by the Court.

### **PRAYER FOR RELIEF**

WHEREFORE, Plaintiff prays for judgment that:

- A. U.S. Patent No. 4,791,615 is valid and has been infringed by Defendant;
- B. U.S. Patent No. 5,162,672 is valid and has been infringed by Defendant;
- C. U.S. Patent No. 5,294,845 is valid and has been infringed by Defendant;
- D. U.S. Patent No. 5,367,494 is valid and has been infringed by Defendant;
- E. U.S. Patent No. 5,455,200 is valid and has been infringed by Defendant;
- F. U.S. Patent No. 5,606,275 is valid and has been infringed by Defendant;
- G. U.S. Patent No. 5,750,440 is valid and has been infringed by Defendant;
- H. U.S. Patent No. 5,798,937 is valid and has been infringed by Defendant;
- I. U.S. Patent No. 5,851,927 is valid and has been infringed by Defendant;
- J. U.S. Patent No. 5,859,541 is valid and has been infringed by Defendant;
- K. Defendant, its officers, agents, servants and employees and those persons in active concert or participation with any of them, be enjoined from further infringement of U.S. Patent No. 4,791,615, U.S. Patent No. 5,162,672, U.S. Patent No. 5,294,845, U.S. Patent No. 5,367,494,

U.S. Patent No. 5,455,200, U.S. Patent No. 5,606,275, U.S. Patent No. 5,750,440, U.S. Patent No. 5,798,937, U.S. Patent No. 5,851,927, and U.S. Patent No. 5,859,541;

L. An accounting be had for its lost profits and damages arising out of Defendant's infringement of U.S. Patent No. 4,791,615, U.S. Patent No. 5,162,672, U.S. Patent No. 5,294,845, U.S. Patent No. 5,367,494, U.S. Patent No. 5,455,200, U.S. Patent No. 5,606,275, U.S. Patent No. 5,750,440, U.S. Patent No. 5,798,937, U.S. Patent No. 5,851,927, and U.S. Patent No. 5,859,541, including treble damages for willful infringement as provided by Title 35 U.S.C. § 284, with interest;

M. Defendant be permanently enjoined from continued use or sale of Defendant's products used to infringe said patents;

N. Plaintiff be awarded its attorneys' fees, costs, and expenses in this action; and

O. Plaintiff be awarded such other and further relief as this Court may deem necessary and proper.

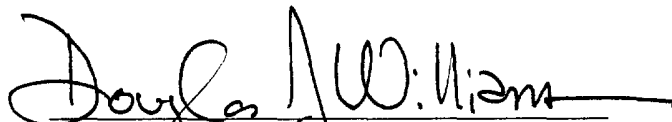
**DEMAND FOR JURY TRIAL**

Plaintiff hereby demands a trial by jury of all issues so triable.

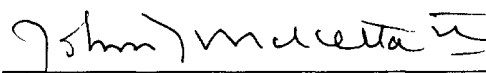
MOTOROLA, INC.,

By its attorneys,

Date: 1/8/04



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**UNITED STATES DISTRICT COURT  
WESTERN DISTRICT OF TEXAS  
AUSTIN DIVISION**

**Notice of Document/Attachment(s) Not Imaged  
but Stored with Document in Case File**

**See Original File to View/Copy Document/Attachment(s)**

Civil Case No. 1:04cv007

Motorola, Inc.

VS.

Micron Technology, Inc.

Attachments to  
Document #: 1

Description: Complaint

File Date: 1/08/04

Prepared by: sh

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