**UNITED STATES DISTRICT COURT**
**NORTHERN DISTRICT OF ALABAMA**
**NORTHEASTERN DIVISION**



| | | |
|---|---|---|
| **NORTHPEAK WIRELESS, LLC,** | ) | **Civil Action No. File** |
| | ) | |
| **Plaintiff,** | ) | |
| | ) | |
| **vs.** | ) | **No.** CV-08-J-1813-NE |
| | ) | |
| **3COM CORPORATION, ACER AMERICA CORPORATION, ASUS COMPUTER INTERNATIONAL CORPORATION, BELKIN INTERNATIONAL, INC., BUFFALO TECHNOLOGY (USA), INC., DELL, INC., D-LINK SYSTEMS, INC., EPSON AMERICA, INC., FUJITSU COMPUTER SYSTEMS CORPORATION, GATEWAY, INC., HEWLETT-PACKARD COMPANY, IOGEAR, INC., MSI COMPUTER CORP., NETGEAR, INC., ROSEWILL, INC., SANDISK CORPORATION, SEH TECHNOLOGY, INC., SMC NETWORKS, INC., SONICWALL, INC., SONY CORPORATION OF AMERICA, SONY ELECTRONICS INC., SONY COMPUTER ENTERTAINMENT AMERICA INC., TOSHIBA AMERICA, INC., TOSHIBA AMERICA INFORMATION SYSTEMS, INC., TRENDNET SYSTEMS, INC., TRENDWARE INTERNATIONAL, INC., U.S. ROBOTICS CORPORATION, VIEWSONIC CORPORATION, WATCHGUARD TECHNOLOGIES, INC., ZONET USA CORPORATION, and ZYXEL COMMUNICATIONS, INC.,** | ) | **JURY TRIAL DEMANDED** |
| | ) | |
| **Defendants.** | ) | |
| | ) | |

**COMPLAINT**

NOW COMES Plaintiff NORTHPEAK WIRELESS, LLC ("NorthPeak") and hereby makes and files this Complaint and petition for relief against each and all of the Defendants as follows:

PARTIES

1. Plaintiff NorthPeak is a Georgia Limited Liability Company having its principal place of business at 2500 Northwinds Parkway, Suite 475, Alpharetta, Georgia 30004.

2. Upon information and belief, Defendant 3COM CORPORATION ("3Com") is a Delaware corporation, having its principal place of business at 350 Campus Drive, Marlborough, Massachusetts 01752. Upon information and belief, 3Com may be served with process through its registered agent, The Corporation Company, 2000 Interstate Park Drive, Suite 204, Montgomery, Alabama 36109.

3. Upon information and belief, Defendant ACER AMERICA CORPORATION ("Acer") is a Delaware corporation, having its principal place of business at 333 West San Carlos Street, Suite 1500, San Jose, California 95110. Upon information and belief, Acer may be served with process through its registered agent, CT Corporation System, 818 West Seventh Street, Los Angeles, California 90017.

4. Upon information and belief, Defendant ASUS COMPUTER INTERNATIONAL CORPORATION ("ASUS") is a California corporation, having its principal place of business at 44370 Nobel Drive, Fremont, California 94538. Upon information and belief, ASUS may be served through its registered agent, Paul L. Gumina, US Bank Tower, 633 West 5th Street, Suite 5880, Los Angeles, California 90071.

5. Upon information and belief, Defendant BELKIN INTERNATIONAL, INC. ("Belkin") is a Delaware corporation, having its principal place of business at 501 West Walnut

Street, Compton, California 90220. Upon information and belief, Belkin may be served with process through its registered agent, National Registered Agents, Inc., 150 South Perry Street, Montgomery, Alabama 36104.

6. Upon information and belief, Defendant BUFFALO TECHNOLOGY (USA), INC. ("Buffalo") is a Delaware corporation, having its principal place of business at 1100 Metric Boulevard, Suite 750, Austin, Texas 78758. Upon information and belief, Buffalo may be served with process through its registered agent, Takayuki Nishioka, 11100 Metric Boulevard, Suite 750, Austin, Texas 78751.

7. Upon information and belief, Defendant DELL, INC. ("Dell") is a Delaware corporation, having its principal place of business at 1 Dell Way, Round Rock, Texas 78682. Upon information and belief, Dell may be served with process through its registered agent, Corporation Service Company, 701 Brazos Street, Suite 1050, Austin, Texas 78701.

8. Upon information and belief, Defendant D-LINK SYSTEMS, INC. ("D-Link") is a California corporation, having its principal place of business at 17595 Mount Herrmann Street, Fountain Valley, California 92708. Upon information and belief, D-Link may be served with process through its registered agent, Nancy Lemm, 17595 Mount Herrmann Street, Fountain Valley, California 92708.

9. Upon information and belief, Defendant EPSON AMERICA, INC. ("Epson") is a California corporation, having its principal place of business at 3840 Kilroy Airport Way, Long Beach, California 90806. Upon information and belief, Epson may be served with process through its registered agent, United States Corporation Company, 30 South Perry Street, Montgomery, Alabama 36104.

10. Upon information and belief, Defendant FUJITSU COMPUTER SYSTEMS CORPORATION ("Fujitsu") is a California corporation, having its principal place of business at 1250 East Arques Avenue, Sunnyvale, California 94085. Upon information and belief, Fujitsu may be served with process through its registered agent, CSC-Lawyers Incorporating Service, 150 South Perry Street, Montgomery, Alabama 36104.

11. Upon information and belief, Defendant GATEWAY, INC. ("Gateway") is a Delaware corporation, having its principal place of business at 7565 Irvine Center Drive, Irvine, California 92618. Upon information and belief, Gateway may be served with process through its registered agent, CT Corporation System, 319 South Coteau, Pierre, South Dakota 57501.

12. Upon information and belief, Defendant HEWLETT-PACKARD COMPANY ("HP") is a Delaware corporation, having its principal place of business at 3000 Hanover Street, Palo Alto, California 94304. Upon information and belief, HP may be served with process through its registered agent, The Corporation Company, 2000 Interstate Park Drive, Suite 204, Montgomery Alabama 36109.

13. Upon information and belief, Defendant IOGEAR, INC. ("Iogear") is a California corporation, having its principal place of business at 23 Hubble Drive, Irvine, California 92618. Upon information and belief, Iogear may be served with process through its registered agent, Sampson Shih-Shien Yang, 23 Hubble Drive, Irvine, California 92618.

14. Upon information and belief, Defendant MSI COMPUTER CORP. ("MSI") is a California corporation, having its principal place of business at 901 Canada Court, City of Industry, California 91748. Upon information and belief, MSI may be served with process through its registered agent, Connie Chang, 901 Canada Court, City of Industry, California 91748.

15. Upon information and belief, Defendant NETGEAR, INC. ("Netgear") is a Delaware corporation, having its principal place of business at 4500 Great America Parkway, Santa Clara, California 95054. Upon information and belief, Netgear may be served with process through its registered agent, CT Corporation System, 818 West Seventh Street, Los Angeles, California 90017.

16. Upon information and belief, Defendant ROSEWILL, INC. ("Rosewill") is a California corporation, having its principal place of business at 17708 Rowland Street, City of Industry, California 91748. Upon information and belief, Rosewill may be served with process through its registered agent, Robert Chang, 9997 East Rose Hills Road, Whittier, California 90601.

17. Upon information and belief, Defendant SANDISK CORPORATION ("SanDisk") is a Delaware corporation, having its principal place of business at 601 McCarthy Boulevard, Milpitas, California 95035. Upon information and belief, SanDisk may be served with process through its registered agent, The Corporation Company, 2000 Interstate Park Drive, Suite 204, Montgomery Alabama 36109.

18. Upon information and belief, Defendant SEH TECHNOLOGY, INC. ("SEH") is a Pennsylvania corporation, having its principal place of business at 37 Nutt Road, 1st Floor, Phoenixville, Pennsylvania 19460. Upon information and belief, SEH may be served at its principal place of business.

19. Upon information and belief, Defendant SMC NETWORKS, INC. ("SMC") is a Delaware corporation, having its principal place of business at 20 Mason, Irvine, California 92618. Upon information and belief, SMC may be served with process through its registered agent, The Prentice-Hall Corporation System, Inc., 2711 Centerville Road, Suite 400, Wilmington, Delaware 19808.

20. Upon information and belief, Defendant SONICWALL, INC. ("SonicWALL") is a California corporation, having its principal place of business at 1143 Borregas Avenue, Sunnyvale, California 94089. Upon information and belief, SonicWALL may be served through its registered agent, Frederick M. Gonzalez, 1143 Borregas Avenue, Sunnyvale, California 94089.

21. Upon information and belief, Defendant SONY CORPORATION OF AMERICA is a New York corporation, having its principal place of business at 550 Madison Avenue, 27th Floor, New York, New York 10022. Upon information and belief, Defendant SONY ELECTRONICS INC. is a Delaware corporation, having its principal place of business at 16530 Via Esprillo, San Diego, California 92127. Upon information and belief, Defendant SONY COMPUTER ENTERTAINMENT AMERICA INC. is a Delaware corporation, having its principle place of business at 919 East Hillsdale Boulevard, Foster City CA, 94404. Defendant Sony Corporation Of America, Sony Electronics Inc., and Sony Computer Entertainment America shall be collectively referred to herein as the "Sony Defendants."

22. Upon information and belief, both Sony Corporation of America and Sony Computer Entertainment America Inc. may be served through their registered agent, CSC-Lawyers Incorporating Service, 2730 Gateway Oaks Drive, Suite 100, Sacramento, California 95833. Upon information and belief, Sony Electronics, Inc. may be served through its registered agent, CSC-Lawyers Incorporating Service, 150 South Perry Street, Montgomery, Alabama 36104.

23. Upon information and belief, Defendant TOSHIBA AMERICA, INC. is a New York corporation, having its principal place of business at 1251 Avenue of the Americas, Suite 4110, New York, New York 10020. Upon information and belief, Defendant TOSHIBA AMERICA INFORMATION SYSTEMS, INC. is a California corporation, having its principal place of business at 9740 Irvine Boulevard, Irvine, California 92618. Defendant Toshiba America, Inc. and Defendant

Toshiba America Information Systems, Inc. shall be collectively referred to herein as the "Toshiba Defendants."

24. Upon information and belief, Toshiba America, Inc. may be served through its registered agent, CT Corporation System, 818 West Seventh Street, Los Angeles, California 90017. Toshiba America Information Systems, Inc. may be served through its registered agent, The Corporation Company, 2000 Interstate Park Drive, Suite 204, Montgomery, Alabama 36109.

25. Upon information and belief, Defendant TRENDNET SYSTEMS, INC. is a California corporation, having its principal place of business at 20675 Manhattan Place, Torrance, California 90501. Upon information and belief, Defendant TRENDWARE INTERNATIONAL, INC. is a California corporation, having its principal place of business at 20675 Manhattan Place, Torrance, California 90501. Defendant Trendnet Systems, Inc. and Defendant Trendware International, Inc. shall be collectively referred to herein as the "TRENDnet Defendants."

26. Upon information and belief, both Trendnet Systems, Inc. and Trendware International, Inc. may be served through their registered agent, Sharon Chang, 23240 Hawthorne Boulevard, Suite 215, Torrance, California 90505.

27. Upon information and belief, Defendant U.S. ROBOTICS CORPORATION ("USR") is a Delaware corporation, having its principal place of business at 935 National Parkway, Schaumburg, Illinois 60173. Upon information and belief, USR may be served with process through its registered agent, CT Corporation System, 208 South LaSalle Street, Suite 814, Chicago, Illinois 60604.

28. Upon information and belief, Defendant VIEWSONIC CORPORATION ("ViewSonic") is a Delaware corporation, having its principal place of business at 381 Brea Canyon

Road, Walnut, California 91789. ViewSonic may be served with process through its registered agent, Theodore R. Sanders, 381 Brea Canyon Road, Walnut, California 91789.

29. Upon information and belief, Defendant WATCHGUARD TECHNOLOGIES, INC. ("WatchGuard") is a Delaware corporation, having its principal place of business at 505 Fifth Avenue South, Suite 500, Seattle, Washington 98104. Upon information and belief, WatchGuard may be served with process through its registered agent, Summit Law Group, PLLC, 315 5th Avenue, Suite 1000, Seattle, Washington 98104.

30. Upon information and belief, Defendant ZONET USA CORPORATION ("Zonet") is a California corporation, having its principal place of business at 19929 Harrison Avenue, Walnut, California 91789. Upon information and belief, Zonet may be served with process through its registered agent, Jenny Yang at 19929 Harrison Avenue, Walnut, California 91789.

31. Upon information and belief, Defendant ZYXEL COMMUNICATIONS, INC. ("ZyXEL") is a California corporation, having its principal place of business at 1130 North Miller Street, Anaheim, California 91789. Upon information and belief, ZyXEL may be served with process through its registered agent, Jeremy Chou, 1130 North Miller Street, Anaheim, California 91789.

## JURISDICTION AND VENUE

32. This is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. §101 *et seq.*

33. This Court has jurisdiction over the subject matter of this action pursuant to 28 U.S.C. §§1331 and 1338(a).

34. This Court has personal jurisdiction over the Defendants. Upon information and belief, each of the Defendants has transacted business in this judicial district and/or has committed, contributed to, and/or induced acts of patent infringement in this judicial district.

35. Venue within this district is proper under 28 U.S.C. §§1391 and 1400(b).

## FACTS GIVING RISE TO THIS ACTION

### Patents-in-Suit

36. On December 11, 1990, United States Patent No. 4,977,577, entitled "Wireless Alarm System" (the "'577 Patent"), was duly and legally issued by the United States Patent and Trademark Office (the "PTO"). A copy of the '577 Patent is attached hereto as Exhibit "A."

37. On November 16, 1999, United States Patent No. 5,987,058, entitled "Wireless Alarm System" (the "'058 Patent"), was duly and legally issued by the PTO. A copy of the '058 Patent is attached hereto as Exhibit "B."

38. NorthPeak is the assignee of the '577 Patent and the '058 Patent (collectively, the "Patents").

39. The Patents are valid and enforceable.

### Defendants' Acts of Infringement

40. 3Com makes, uses, sells, offers to sell, and/or imports products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation 3Com wireless access points, routers, and adapters.

41. Acer makes, uses, sells, offers to sell, and/or imports products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation products marketed under the Acer Aspire, Extensa, Ferrari, and TravelMate brands.

42. ASUS makes, uses, sells, offers to sell, and/or imports products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation ASUS wireless routers and adapters, as well as computers sold under the ASUS Eee PC, A2 Series, A3 Series, A5 Series, A6 Series, A7 Series, B50 Series, V1 Series, V2 Series, F2 Series, F6 Series, F7 Series, F8 Series, W1 Series, W2 Series, M Series, and Lamborghini brands.

43. Belkin makes, uses, sells, offers to sell, and/or imports products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation Belkin wireless network access points, routers, and adapters.

44. Buffalo makes, uses, sells, offers to sell, and/or imports products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation Buffalo wireless access points, routers, and adapters.

45. Dell makes, uses, sells, offers to sell, and/or imports products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation devices marketed under the Dell Inspiron, Studio, XPS, Vostro, Latitude, Precision Mobile, V305, and 968 brands.

46. D-Link makes, uses, sells, offers to sell, and/or imports products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation D-Link wireless access points, routers, and adapters.

47. Epson makes, uses, sells, offers to sell, and/or imports products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation products marketed under the Epson Artisan and WorkForce brands.

48. Fujitsu makes, uses, sells, offers to sell, and/or imports products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation products marketed under the Fujitsu LifeBook and Stylistic brands.

49. Gateway makes, uses, sells, offers to sell, and/or imports products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation products marketed under the Gateway MT Series, ML Series, T Series, M Series, P Series, and C Series brands.

50. HP makes, uses, sells, offers to sell, and/or imports products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation products sold under the HP Pavilion, Deskjet, Photosmart, Officejet, and HP Compaq brands.

51. Iogear makes, uses, sells, offers to sell, and/or imports products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation Iogear wireless routers and adapters.

52. MSI makes, uses, sells, offers to sell, and/or imports products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation MSI wireless adapters, as well as computers sold under the Wind, Aesthetics, Entertainment, Gaming, Professional, and Value brands.

53. Netgear makes, uses, sells, offers to sell, and/or imports products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation Netgear wireless access points, routers, and adapters.

54. Rosewill makes, uses, sells, offers to sell, and/or imports products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation Rosewill wireless routers and adapters.

55. SanDisk makes, uses, sells, offers to sell, and/or imports products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation SanDisk wireless adapters, as well as products marketed under the Sansa Connect brand.

56. SEH makes, uses, sells, offers to sell, and/or imports products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation the SEH IC156-WLAN-HP, IC156-WLAN-EPSON, IC156-WLAN-KYO, PS54a-G, PS56, PS113, PS159, and the IC190-WLAN-CONNECT products.

57. SMC makes, uses, sells, offers to sell, and/or imports products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation SMC wireless routers, access points, and adapters.

58. SonicWALL makes, uses, sells, offers to sell, and/or imports products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation the SonicWALL 01-SSC-5815, 01-SSC-5740, 01-SSC-6551, 01-SSC-6851, and 01-SSC-6081 products.

59. The Sony Defendants make, use, sell, offer to sell, and/or import products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation products marketed under the Sony Vaio and PlayStation brands.

60. The Toshiba Defendants make, use, sell, offer to sell, and/or import products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation products marketed under the Toshiba Protégé, Satellite, Satellite Pro, Tecra, and Qosmio brands.

61. The TRENDnet Defendants make, use, sell, offer to sell, and/or import products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation TRENDnet wireless access points, routers, and adapters.

62. USR makes, uses, sells, offers to sell, and/or imports products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation USR wireless routers, access points, and adapters.

63. ViewSonic makes, uses, sells, offers to sell, and/or imports products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation the ViewSonic WPCI-100, WPG-150, WAPBR-100, WUSB100, WMG80, WMG120, WMA100, V210, V212, VR38r-01, VR38r-02, VR38r-02A, VR38r-05, VR38r-07, and the VR38r-08 products.

64. WatchGuard makes, uses, sells, offers to sell, and/or imports products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation products marketed under the WatchGuard FireBox brand.

65. Zonet makes, uses, sells, offers to sell, and/or imports products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation Zonet wireless routers and adapters.

66. ZyXEL makes, uses, sells, offers to sell, and/or imports products that incorporate and/or utilize direct sequence spread spectrum wireless technology, including without limitation ZyXEL wireless routers and adapters.

## COUNT I

### Infringement of the '577 Patent

67. Plaintiff repeats and incorporates by reference the allegations in paragraphs 1 through 66 as if set forth fully verbatim herein.

68. Upon information and belief, Defendants are infringing and have infringed and will continue to infringe one or more claims of the '577 Patent by performing, without authority, one or more of the following acts: (a) making, using, offering to sell, and/or selling within the United States the invention as claimed in one or more claims of the '577 Patent in violation of 35 U.S.C. § 271(a); (b) importing into the United States the invention of one or more claims of the '577 Patent in violation of 35 U.S.C. § 271(a); (c) contributing to the infringement of one or more claims of the '577 Patent by others in the United States in violation of 35 U.S.C. § 271(c); and/or (d) inducing others to infringe one or more claims of the '577 Patent within the United States in violation of 35 U.S.C. § 271(b).

69. As a direct and proximate result of the Defendants' infringement of the '577 Patent, Plaintiff has suffered and will continue to suffer damages.

70. Plaintiff is entitled to recover from Defendants the damage sustained by Plaintiff as a result of Defendants wrongful acts in an amount subject to proof at trial.

COUNT II

Infringement of the '058 Patent

71. Plaintiff repeats and incorporates by reference the allegations in paragraphs 1 through 70 as if set forth fully verbatim herein.

72. Upon information and belief, Defendants are infringing and have infringed and will continue to infringe one or more claims of the '058 Patent by performing, without authority, one or more of the following acts: (a) making, using, offering to sell, and/or selling within the United States the invention as claimed in one or more claims of the '058 Patent in violation of 35 U.S.C. § 271(a); (b) importing into the United States the invention of one or more claims of the '058 Patent in violation of 35 U.S.C. § 271(a); (c) contributing to the infringement of one or more claims of the

'058 Patent by others in the United States in violation of 35 U.S.C. § 271(c); and/or (d) inducing others to infringe one or more claims of the '058 Patent within the United States in violation of 35 U.S.C. § 271(b).

73. As a direct and proximate result of the Defendants' infringement of the '058 Patent, Plaintiff has suffered and will continue to suffer damages.

74. Plaintiff is entitled to recover from Defendants the damage sustained by Plaintiff as a result of Defendants wrongful acts in an amount subject to proof at trial.

## PRAYER FOR RELIEF

WHEREFORE, Plaintiff prays for the following relief against Defendants:

A. A judgment that Defendants have infringed, actively induced infringement of, and/or contributorily infringed the '577 Patent, as set forth herein;

B. A judgment that Defendants have infringed, actively induced infringement of, and/or contributorily infringed the '058 Patent, as set forth herein;

C. An award of all damages recoverable under the United States Patent Laws, in an amount to be proven at trial;

D. A judgment and order requiring Defendants to pay Plaintiff's prejudgment and post-judgment interest on the damages awarded;

E. A judgment requiring Defendants to pay the costs of this action (including all disbursements) and attorneys' fees as provided by 35 U.S.C. §285, with prejudgment interest; and

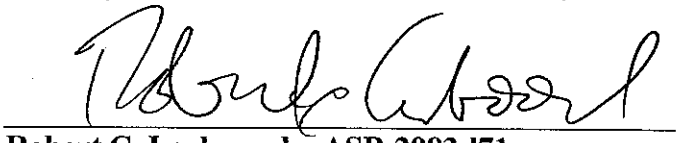
F. Such other and further relief as this Court may deem just and equitable.

## DEMAND FOR JURY TRIAL

Plaintiff hereby demands that all issues so triable be determined by a jury.

Respectfully submitted, this 1st day of October, 2008.

**WILMER & LEE, P.A.**
Attorneys for Plaintiff, NorthPeak Wireless, LLC



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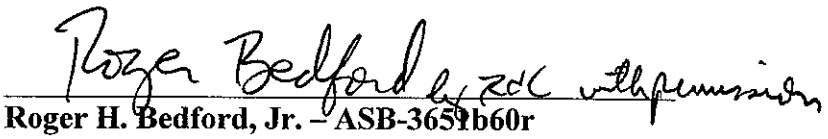
Attorneys for Plaintiff, NorthPeak Wireless, LLC



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# EXHIBIT "A"

# United States Patent [19]

**Arthur et al.**

[11] **Patent Number: 4,977,577**

[45] **Date of Patent: Dec. 11, 1990**


[54] **WIRELESS ALARM SYSTEM**


[75] Inventors: **James D. Arthur**, Costa Mesa, Calif.; **H. Britton Sanderford, Jr.**, New Orleans; **Robert E. Rouquette**, Kenner, both of La.

[73] Assignee: **Axonn Corporation**, New Orleans, La.



[21] Appl. No.: **266,461**

[22] Filed: **Nov. 2, 1988**

[51] **Int. Cl.**[5] ..... **H04K 1/00**

[52] **U.S. Cl.** ..... **375/1**

[58] **Field of Search** ..... 375/1; 380/34; 370/71



[56] **References Cited**

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| | | | |
|---|---|---|---|
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*Primary Examiner*—Salvatore Cangialosi

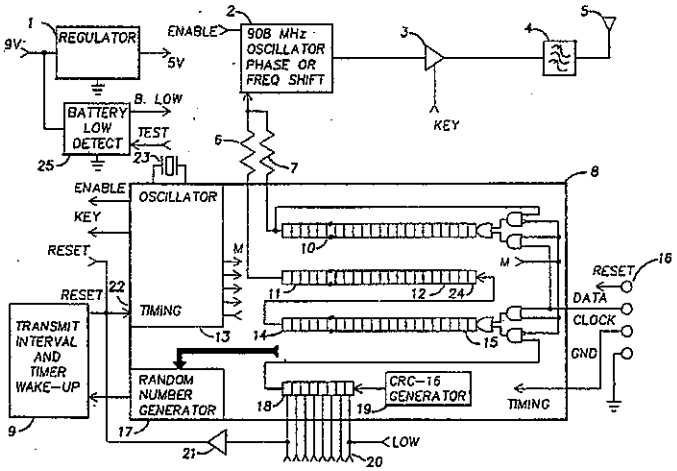
*Attorney, Agent, or Firm*—David B. Newman, Jr. & Associates



[57] **ABSTRACT**

A wireless alarm system using spread spectrum transmitters, fast frequency shift keying, spread spectrum receivers and computer with a display. The spread spectrum transmitter includes an oscillator coupled to a microprocessor with chip code generation means, preamble register, address register and data register. The spread spectrum receiver acquires synchronization of the spread spectrum signal using a microprocessor coupled to the quieting, signal strength or baseband output of the receiver, with a two step algorithm. The steps comprise achieving a coarse lock and a fine lock to the spread spectrum signal.


**14 Claims, 8 Drawing Sheets**



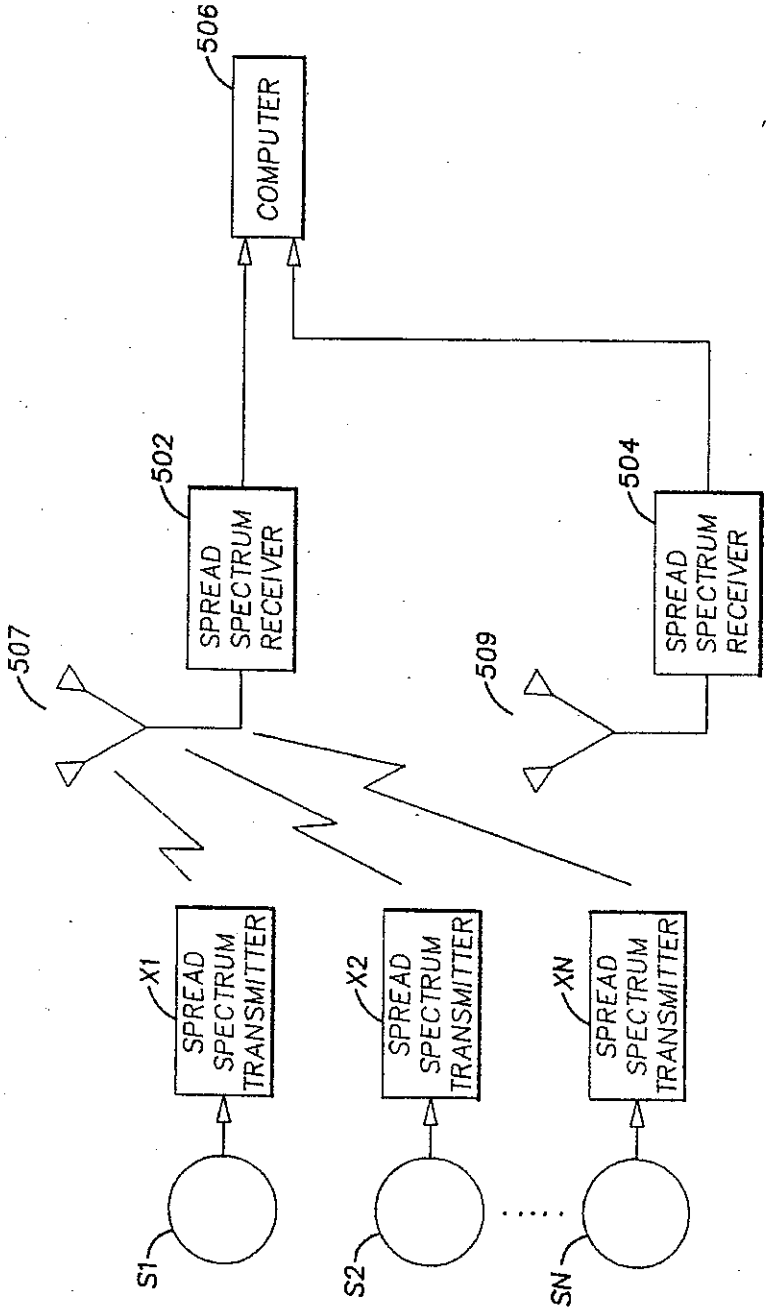

506
COMPUTER
502
SPREAD SPECTRUM RECEIVER
504
SPREAD SPECTRUM RECEIVER
507
509
X1
SPREAD SPECTRUM TRANSMITTER
X2
SPREAD SPECTRUM TRANSMITTER
XN
SPREAD SPECTRUM TRANSMITTER
S1
S2
SN

FIG. 1

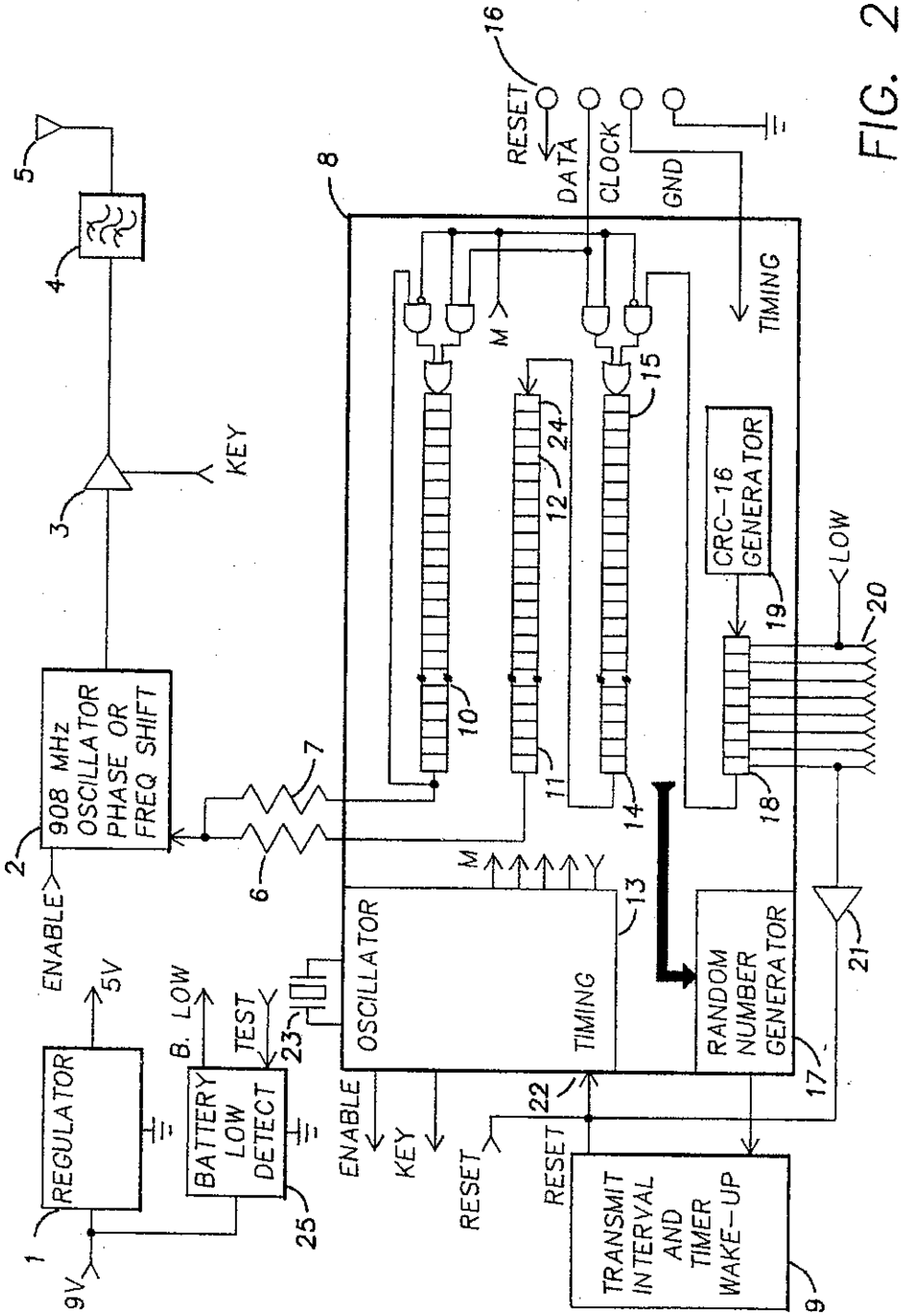

RESET
DATA
CLOCK
GND
16
8
TIMING
M
15
24
12
10
11
14
CRC-16 GENERATOR
LOW
20
19
18
5
4
3
KEY
908 MHz OSCILLATOR PHASE OR FREQ SHIFT
2
7
6
ENABLE
5V
9V
1
REGULATOR
B. LOW
TEST
23
BATTERY LOW DETECT
25
OSCILLATOR
TIMING
13
RANDOM NUMBER GENERATOR
21
17
22
ENABLE
KEY
RESET
RESET
TRANSMIT INTERVAL AND TIMER WAKE-UP
9

FIG. 2

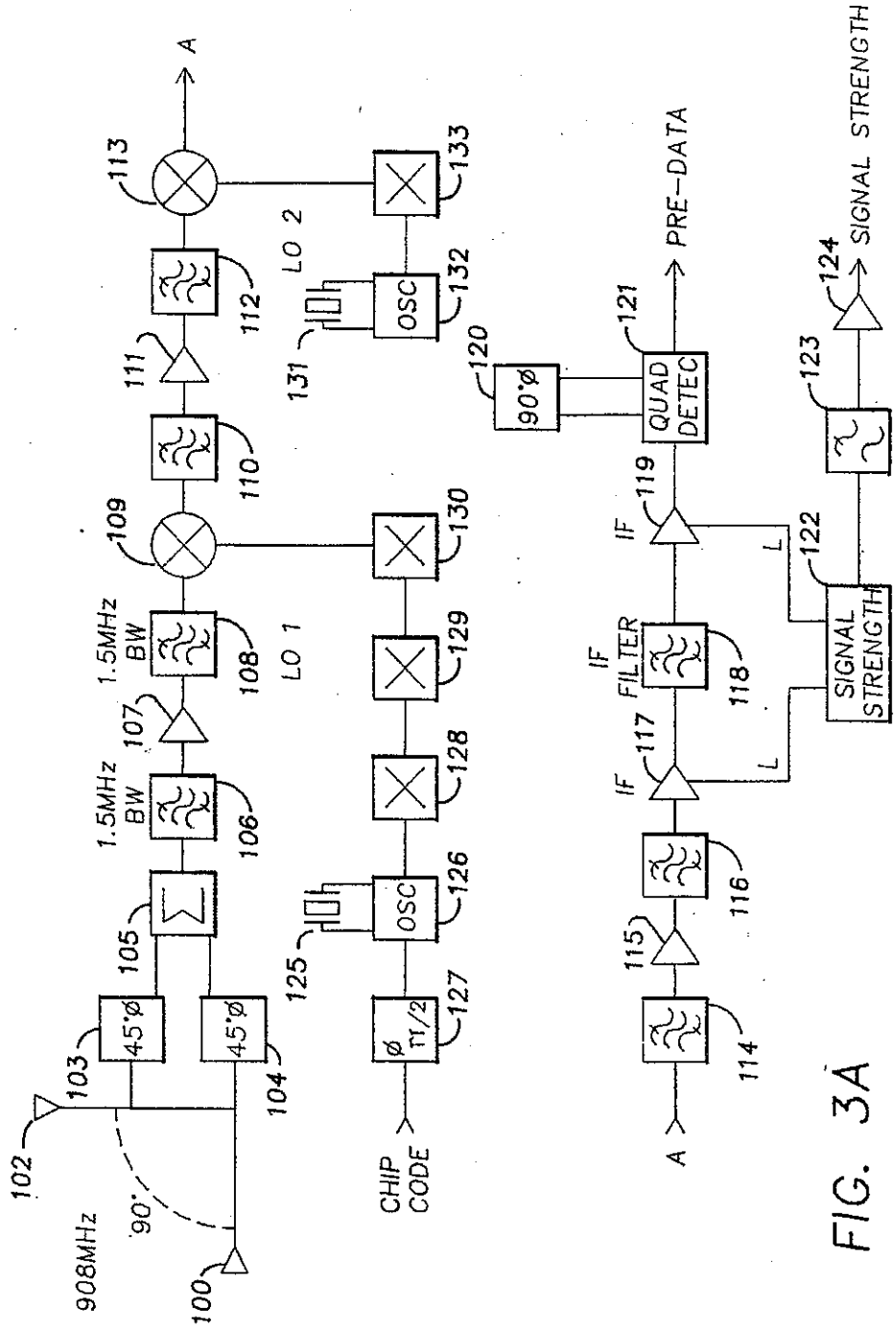

908MHz
90°
CHIP CODE
PRE-DATA
SIGNAL STRENGTH
LO 1
LO 2
1.5MHz BW
IF FILTER
QUAD DETEC
45°ø
90°ø
ø π/2
OSC
IF
L
A

FIG. 3A

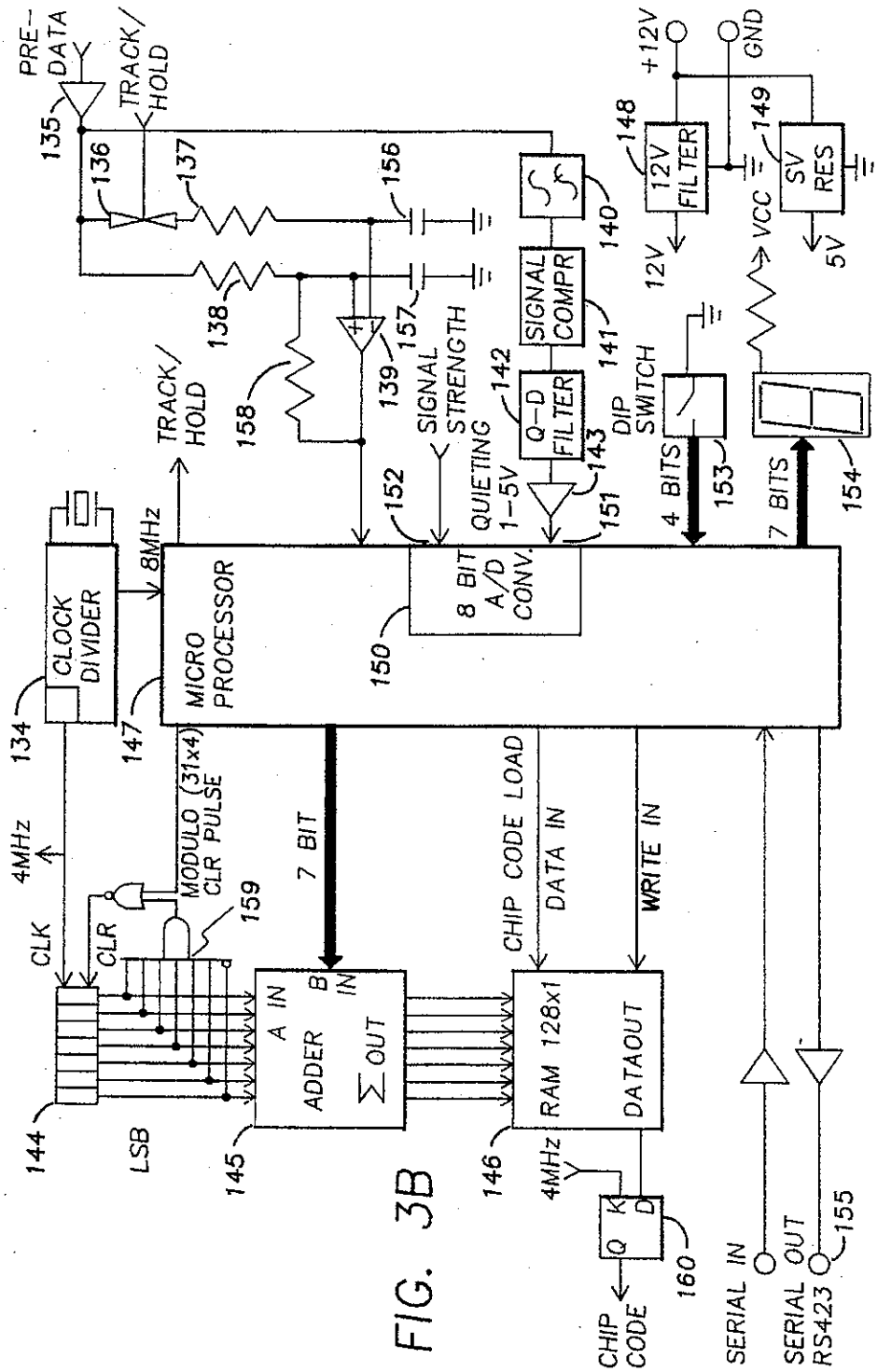

PRE-DATA
TRACK/HOLD
135
136
137
156
138
157
139
158
140
SIGNAL COMPR
141
142
Q-D FILTER
143
151
152
+12V
GND
148
12V FILTER
149
5V RES
VCC
12V
5V
DIP SWITCH
4 BITS
153
7 BITS
154
TRACK/HOLD
SIGNAL STRENGTH
QUIETING 1-5V
8MHz
CLOCK DIVIDER
MICRO PROCESSOR
8 BIT A/D CONV.
150
134
147
4MHz
CLK
CLR
MODULO (31x4) CLR PULSE
159
7 BIT
CHIP CODE LOAD
DATA IN
WRITE IN
144
LSB
A IN
B IN
ADDER
Σ OUT
145
RAM 128x1
DATAOUT
146
4MHz
K
Q
D
160
CHIP CODE
SERIAL IN
SERIAL OUT RS423
155

FIG. 3B

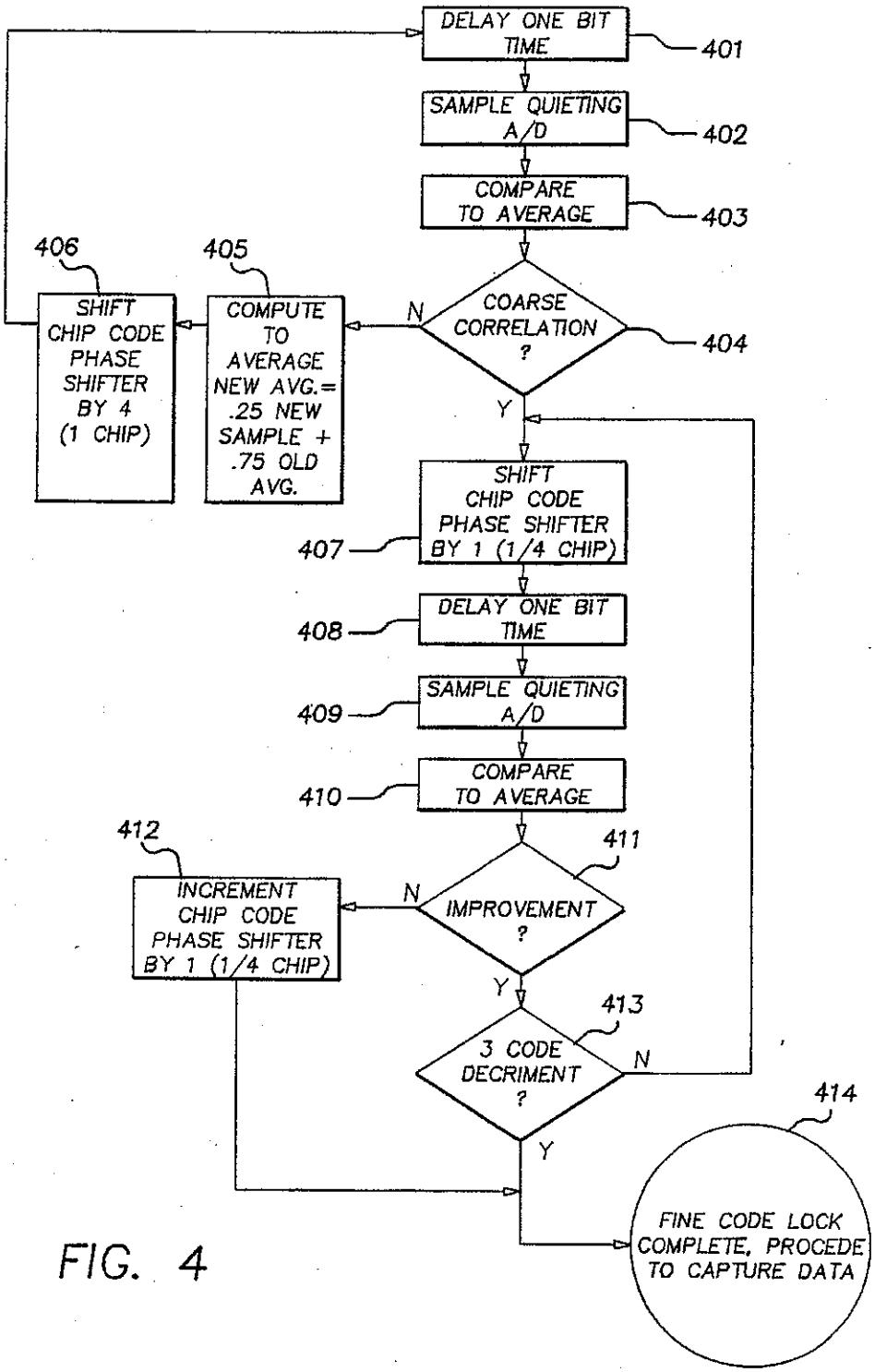

DELAY ONE BIT TIME
401
SAMPLE QUIETING A/D
402
COMPARE TO AVERAGE
403
COARSE CORRELATION ?
404
N
Y
406
SHIFT CHIP CODE PHASE SHIFTER BY 4 (1 CHIP)
405
COMPUTE TO AVERAGE NEW AVG.= .25 NEW SAMPLE + .75 OLD AVG.
407
SHIFT CHIP CODE PHASE SHIFTER BY 1 (1/4 CHIP)
408
DELAY ONE BIT TIME
409
SAMPLE QUIETING A/D
410
COMPARE TO AVERAGE
411
IMPROVEMENT ?
412
INCREMENT CHIP CODE PHASE SHIFTER BY 1 (1/4 CHIP)
413
3 CODE DECRIMENT ?
414
FINE CODE LOCK COMPLETE, PROCEDE TO CAPTURE DATA

FIG. 4

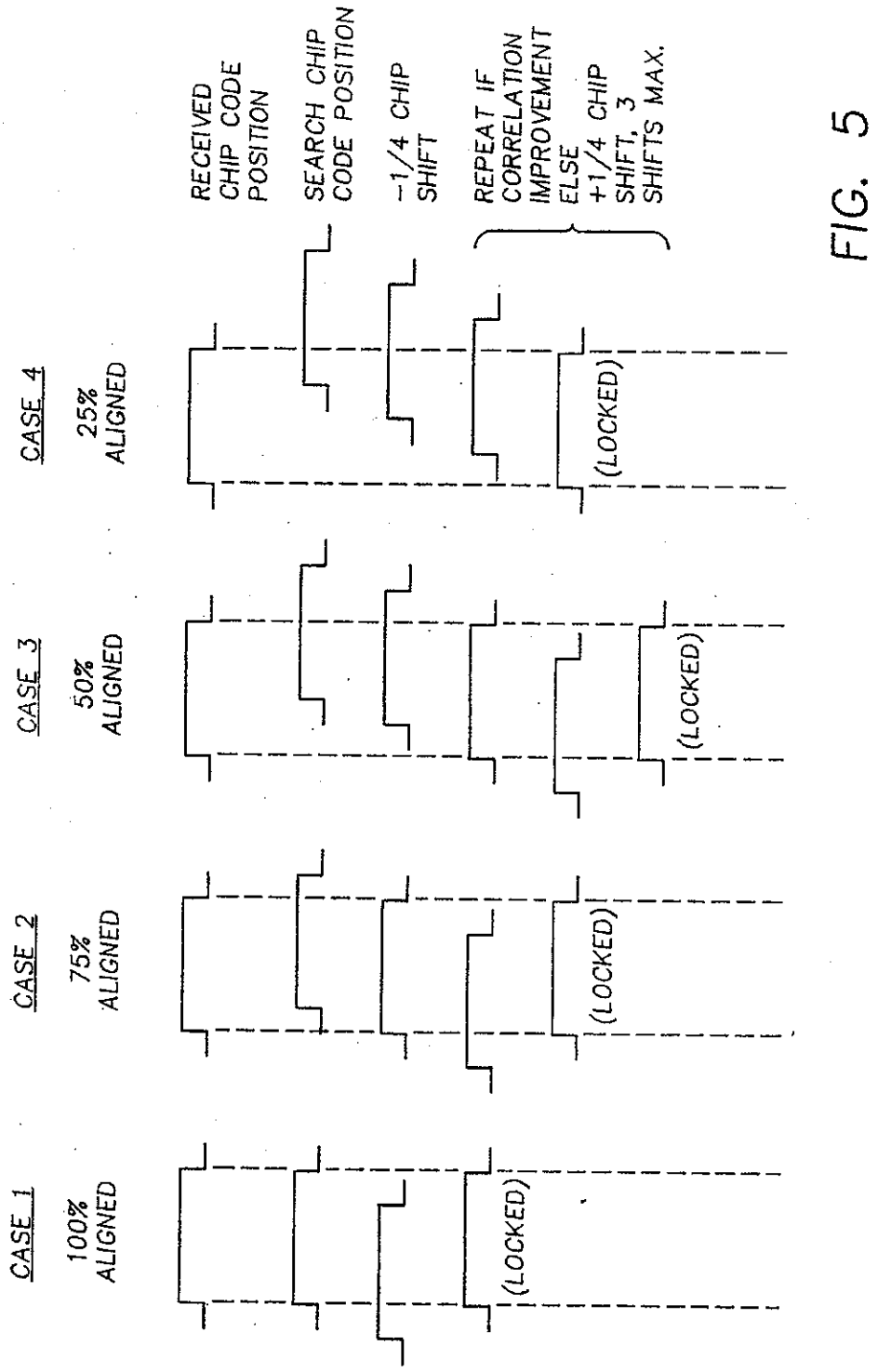

RECEIVED CHIP CODE POSITION
SEARCH CHIP CODE POSITION
-1/4 CHIP SHIFT
REPEAT IF CORRELATION IMPROVEMENT ELSE +1/4 CHIP SHIFT, 3 SHIFTS MAX.
CASE 4
25% ALIGNED
(LOCKED)
CASE 3
50% ALIGNED
(LOCKED)
CASE 2
75% ALIGNED
(LOCKED)
CASE 1
100% ALIGNED
(LOCKED)

FIG. 5

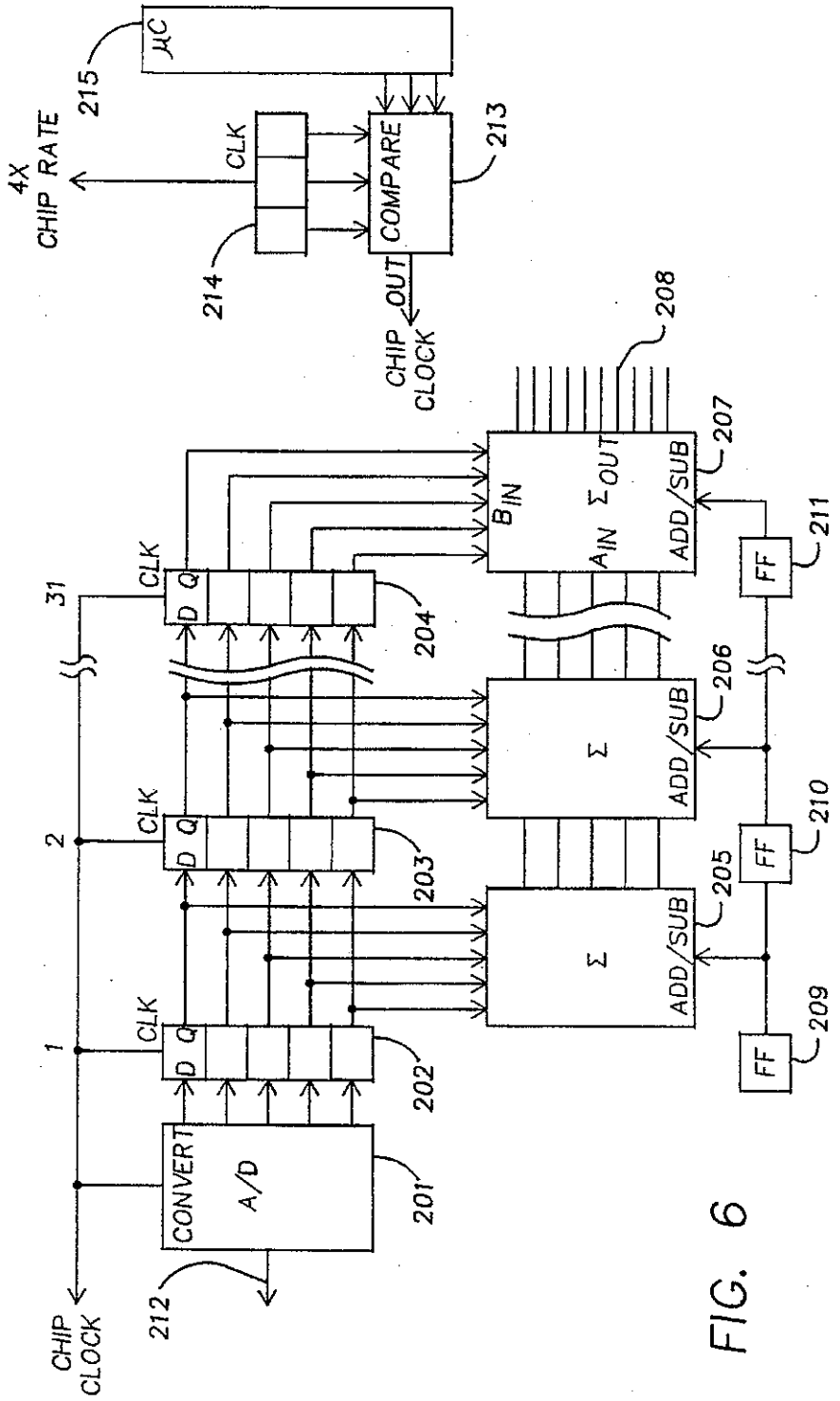
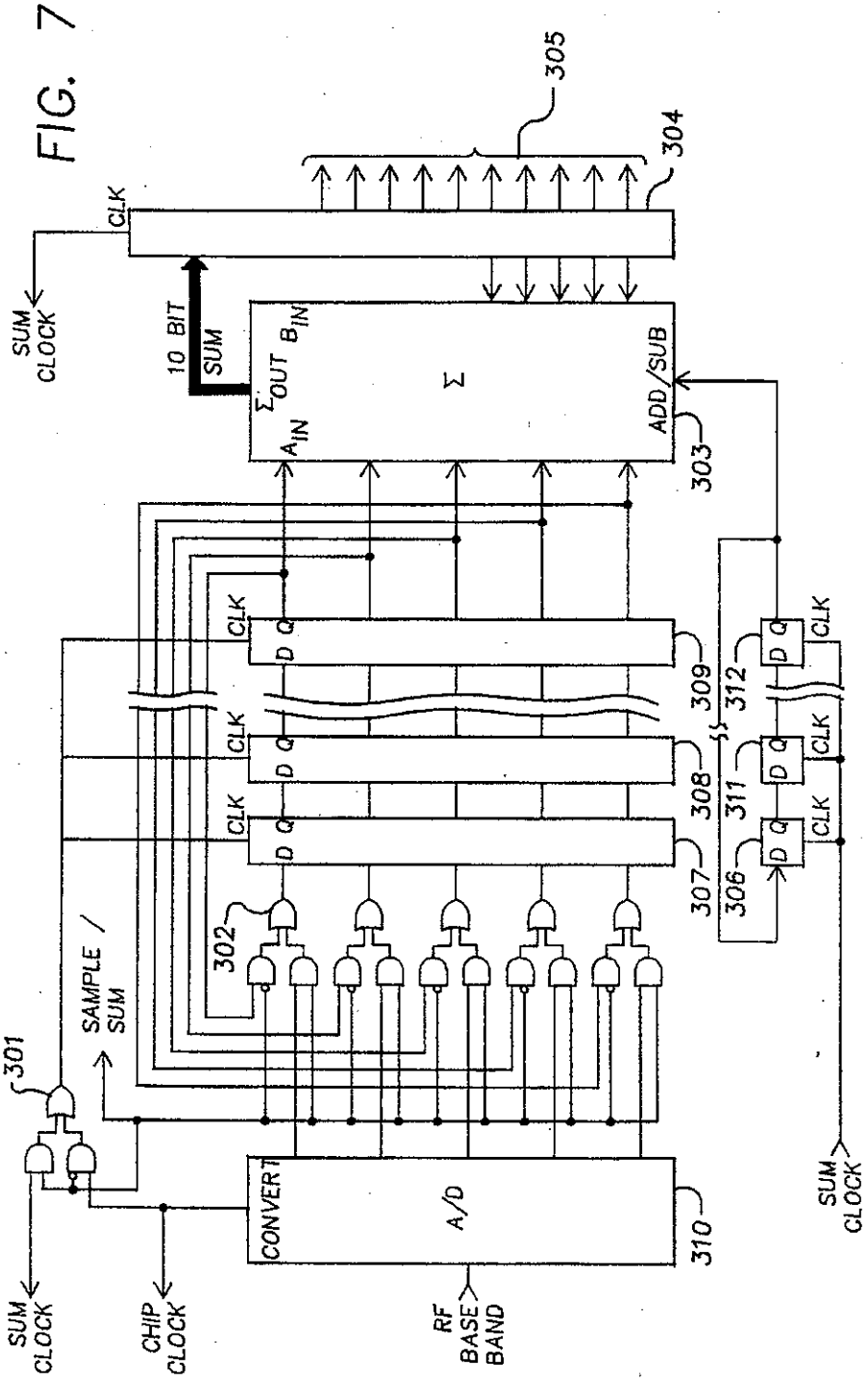

μC
215
4X CHIP RATE
CLK
COMPARE
213
214
CHIP OUT
CHIP CLOCK
208
207
ADD/SUB
$B_{IN}$
$\Sigma_{OUT}$
$A_{IN}$
211
FF
CLK
D Q
31
204
206
Σ
2
203
205
210
1
202
209
CONVERT
A/D
201
212
CHIP CLOCK

FIG. 6

FIG. 7


305
304
CLK
SUM CLOCK
10 BIT SUM
$\Sigma_{OUT}$ $B_{IN}$
$A_{IN}$
Σ
ADD/SUB
303
CLK
D Q
309
312
308
311
307
306
302
SAMPLE / SUM
301
CONVERT
A/D
310
SUM CLOCK
CHIP CLOCK
RF BASE BAND

# WIRELESS ALARM SYSTEM

## BACKGROUND OF THE INVENTION

This invention relates to a wireless warning system for use in a large office building, and more particularly a wireless fire warning and detection system which employs spread spectrum technology with high reliability for continuously monitoring the building.

## DESCRIPTION OF THE PRIOR ART

A number of systems and techniques have been employed in the prior art as a warning system for large buildings. These include having warning sensors for detecting fire, security, or other means wired directly to a main console, with indicators that a particular sensor has been activated. Systems also have been developed employing a radio link between the sensor and receiver. For example, U.S. Pat. No. 4,550,312 to Galloway et al. teaches the use of wideband sensors and transmitters. The sensors/transmitters transmit digital information to a central station by radio. These transmissions of messages are proceeded by an additional access code to identify a particular property. This increases the message overhead, however, which lowers system throughput and lowers battery life.

U.S. Pat. No. 4,661,804 to Abel discloses a receiver-decoder used with a plurality of encode or transmitter units using digitally encoded addresses. This use of multiple redundant 35 second interval short transmissions is used to achieve reliable throughput.

U.S. Pat. No. 4,734,680 to Gehman et al. teaches the use of a pseudorandom number to lower probability of repeat data collisions. The Gehman invention provides for only four bits or sixteen time slot positions over which to transmit, which are inadequate for large systems with hundreds of transmitters. The Gehman disclosure does not teach the use of a randomization interval with hundreds of possible of time slots with spread spectrum so that a destructive data collision can only occur in one chip time. Further, the Gehman patent does not teach the use of the transmitters unique address as a seed to the pseudorandom number generator, preventing two transmitters from drifting into lockstep transmitting schedule.

## OBJECTS AND SUMMARY OF THE INVENTION

An object of the present invention is to provide a wireless warning system having a high reliability for transmitting digital data via radio waves from an alarm or data transmission device to a remotely located receiver.

Another object of the invention is to provide a wireless warning system capable of data error detection and error correction using redundancy, for increasing communications reliability.

A further object of the invention is to provide a wireless warning system having a safety margin against jamming and undesirable interference.

According to the present invention, as embodied and broadly described herein, a wireless warning system is provided comprising a plurality of sensors coupled to a plurality of spread spectrum transmitters, respectively. The plurality of sensors are for detecting or warning against smoke, heat, unauthorized entry, or other sensing device to indicate some particular function in a room of a building. The system further includes at least one spread spectrum receiver having polar diversity antennas and microprocessor having a display, with the microprocessor coupled to the spread spectrum receivers.



An apparatus coupled to a modulation input of an oscillator of a spread spectrum transmitter is provided for controlling the spread spectrum transmitter, which includes chip-code-generation means, preamble means, address means, and data means. The chip-code-generation means can be embodied as a recirculating register, the preamble means can be embodied as a preamble register, the address means can be embodied as an address register, and the data means can be embodied as a data register. The recirculating register is coupled to the modulation input of the oscillator for storing the spread spectrum code. The recirculating register also outputs the spread spectrum chip code as a modulating voltage to the modulation input of the oscillator. The preamble register is coupled to the modulation input of the voltage controlled oscillator. The preamble register stores a preamble, and outputs, during a transmitting interval, the preamble as a modulating voltage to the modulation input of the voltage controlled oscillator. The preamble may include a coarse lock preamble and a fine lock preamble.

The address register is coupled to the modulation input of the voltage controlled oscillator through the preamble register. The address register stores a device address and a type code, and outputs, during a transmitting interval, the device address and the type code as a modulating voltage to the modulation input of the voltage controlled oscillator.

The data register is coupled to the data input and to the modulation input of the voltage controlled oscillator through the preamble register and the address register. The data register stores data received from the data input, and outputs, during the transmitting interval, the data as a modulating voltage to the modulation input of the voltage controlled oscillator.

The present invention further includes a error detection means coupled to the data register for putting a redundancy check code word at the end of a data sequence, for error detection.

A timing circuit is provided coupled to the enable input of the voltage oscillator for enabling the voltage controlled oscillator during the transmitting interval. The timing circuit also is coupled to the keying input of the RF power amplifier for enabling an RF power amplifier during the transmitting interval. Additionally, a pseudorandom sequence generator is coupled to the timing circuit for generating a random number for modifying the timing duration between each transmitting interval.

The present invention also includes an apparatus for generating a spread spectrum chip code for use with a receiver, including means for entering the spread spectrum chip code having n single chips. The entering means may be embodied as a hand terminal. The apparatus further includes memory means for storing chip words, each chip word having a plurality of bits. The memory means may include a random access memory (RAM) or other memory device. Also included is a processing means coupled to the entering means and to the memory means, and responsive to receiving the spread spectrum chip code for transforming a single chip of the spread spectrum chip code to a chip word and storing the chip word in memory means. The pro-

cessing means may be, for example, a microprocessor or other electronic circuit device to accomplish these functions. Additionally, counting means are included coupled to the memory means for sequencing through n addresses of the chip words stored in the memory means, and sequentially outputting the chip words to the receiver.

The present invention further includes an apparatus for synchronizing spread spectrum chip code using a two step algorithm in a process coupled to a receiver having a quieting output. The apparatus includes means for correlating a first signal from the quieting output of the receiver with multiple code iterations of the spread spectrum chip code by comparing the first signal to an adaptive average to be exceeded by a preset margin. The means for correlating includes determining whether the amplitude of the first signal exceeds the preset margin. Included are means coupled to the correlating means for computing the adaptive average, in response to the first signal not exceeding the preset margin. The computing means adds the amplitude of the first signal to the previously computed adaptive average. Means coupled to the quieting output of the receiver is provided for correlating a second signal in response to the first signal exceeding the preset margin. The second signal is correlated with a portion the time duration of multiple code iterations of the spread spectrum signal. The means for correlating the second signal compares the amplitude of the second signal to an adaptive average by a preset margin to determine whether the second signal exceeds the preset margin.

A second species of the spread spectrum chip code synchronization method and apparatus, according to the present invention, is provided. The second species includes the spread spectrum chip code synchronization apparatus coupled to a baseband output of a receiver. The apparatus includes means coupled to the baseband output of the receiver for sampling and digitizing a plurality of analog signals from the baseband output of the receiver, for generating a plurality of data signals. Each of the analog baseband signals is sampled and digitized during one chip time. Register means are provided, coupled to the sampling and digitizing means, for shifting the plurality of data signals sequentially through a plurality of shift registers. Means is provided coupled to the register means for adding in parallel each of the plurality of data signals stored in the plurality of registers according to a plurality of predetermined weights for each of the plurality of data signals. The adding means generates a correlation sum.

Comparing means coupled to the adding means compares the correlation sum to a preset margin. Means coupled to the comparing means dithers a chip clock by at least one portion of one chip time, thereby improving clock lock.

A third species of the spread spectrum chip code synchronization apparatus is provided according to the present invention. The apparatus comprises means coupled to the baseband output of the receiver for sampling and digitizing a plurality of analog signals from the baseband output of the receiver. The sampling and digitizing means also generates a plurality of data signals. Each of the analog signals is sampled and digitized during one chip time.

Register means also is provided in the third species of the spread spectrum chip code synchronization apparatus, according to the present invention, coupled to the sampling and digitizing means for shifting and recirculating the plurality of data signals sequentially through a plurality of shift registers. Means additionally is provided coupled to the register means for adding sequentially the data signals passing through one of the shift registers according to a predetermined weighting algorithm.

Additional objects and advantages of the inventions will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention.

## BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate a preferred embodiment of the invention, and together with the description, serve to explain the principles of the invention.

FIG. **1** is a block diagrammatic view of the wireless sensor and detector system according to the present invention;

FIG. **2** is a schematic diagram of a spread spectrum transmitter;

FIG. **3A** is a block diagram of a spread spectrum receiver;

FIG. **3B** is a schematic diagram of a spread spectrum chip code microprocessor of the receiver;

FIG. **4** is a flow chart of the code locking algorithm;

FIG. **5** is a timing diagram of the spread spectrum chip positions;

FIG. **6** is a schematic diagram of a parallel correlator coarse lock dither circuit for proving a fine lock; and

FIG. **7** is a schematic diagram of a parallel correlator with a serial correlation sum accumulation.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings.

### Wireless Warning Detection System

FIG. **1** illustrates the wireless warning system of the present invention. A plurality of sensors **S1, S2, . . . , SN**, are coupled to a plurality of spread spectrum transmitters **X1, X2, . . . , XN**, respectively. Also shown are the elements of a base station including a first spread spectrum receiver **502** and a second spread spectrum receiver **504**, each of which are coupled to polar diversity antennas **507, 509**, respectively. A microprocessor **506** having a microprocessor display is coupled to the first spread spectrum receiver **502** and the second spread spectrum receiver **504**. The wireless warning detection system of FIG. **1** provides a high reliability for transmitting digital data via radio waves from a sensor **S1, S2, . . . , SN**. The sensor **S1, S2, . . . , SN** may be, for example, a smoke head detector, a security sensing device, or other initiating device or modulating device. As set forth below, the high reliability of the system includes means for data error detection and error correction.

The preferred embodiment consists of many sensor devices **S1, S2, . . . , SN** which may be a smoke detector, pull station, contact alarm, waterflow detector, guard station, or security access controller. These can be expanded directly to include voice modulation, local area network data link, long-range alarm monitoring, remote power meter reading, remote process control, etc.

The initiating device provides either a contact input or reflected light smoke chamber level or data byte to the spread spectrum transmitters X1, X2, . . . , XN. The spread spectrum transmitters X1, X2, . . . , XN include means for data message encoding in serial form and data integrity validation, means for re-sending the message to achieve redundancy, means for randomizing the message transmit interval to avoid repeat collisions, means for modulating the serial message into spread spectrum form and means for transmitting the spread spectrum carrier at the desired frequency.

The spread spectrum receiver's antennas **507, 509** minimize signal fading via polar diversity. Using two receivers provides redundancy as a primary and secondary means for receiving transmissions. The two polar diversity antennas provide spatial diversity against signal fading. The spread spectrum receiver **507, 509** collects the RF energy from polar diversity antenna **507, 509** and filters out undesirable frequencies. The receivers compare and synchronize desirable frequencies to the spread spectrum code of interest thereby extracting the original serial transmission. The spread spectrum receivers **507, 509** further validate the serial transmitter message and forward this information to computer **508** for display.

The spread spectrum of the present invention, in a preferred embodiment, uses fast frequency shift keying (FFSK). The techniques disclosed below are equally applicable for frequency hopping or phase shift keyed spread spectrum methods.

## Transmitter

Referring to FIG. **2**, a preferred embodiment of the transmitter of the instant invention is shown including chip-code-generation means, preamble means, address means, data means, timing means, pseudorandom-sequence means, and error-detection means. The chip-code-generation means may be embodied as a recirculating register **10** and the preamble means may be embodied as a preamble register **11**. The chip-code-generation means may be embodied as a shift register with exclusive ORed feedback taps. The address means may be embodied as an address register **14**, the data means may be embodied as a data register **18**, and the error-detection means may be embodied as cyclical-redundancy-check (CRC) generator **19**. The timing means may be embodied as timing circuit **13**, and the pseudorandom sequence means may be embodied as the random number generator **17**.

In the exemplary arrangement shown, a microprocessor **8** includes the recirculating register **10**, preamble register **11**, address register **14**, data register **18**, CRC generator **19**, random number generator **17**, and timing circuit **13**. The timing circuit **13** is embodied as a timing algorithm in software, located in microprocessor **8**. Alternatively, these registers and circuits may be put together with discrete components or independently wired and constructed as separate elements, as is well known in the art.

As shown in FIG. **2**, an oscillator, which is shown as a voltage controlled oscillator **2** is coupled to an RF power amplifier **3**, and the RF power amplifier **3** is coupled through a bandpass filter **4** to a micropatch or equivalent antenna **5**. The voltage controlled oscillator **2** includes an enable input and a modulation input, where the voltage controlled oscillator generates a spread spectrum signal in response to a modulating voltage being applied to the modulation input. The voltage controlled oscillator **2** is enabled by applying an enable signal to the enable input. The RF power amplifier **3** has a keying input and will amplify a signal from the voltage controlled oscillator **2** only if a keying signal is applied to the keying input. The voltage controlled oscillator **2** alternatively can be frequency locked to the microprocessor's crystal to improve stability. The voltage controlled oscillator **2** also can be replaced by a capacitor and inductor tuned oscillator and a phase shift keyed modulator, or any other means for generating a signal.

The microprocessor **8** is coupled to the modulation input of the voltage controlled oscillator **2** through first resistor **R6** and second resistor **R7**. The microprocessor **8** broadly controls the voltage controlled oscillator **2** by supplying an enable signal to the enable input of the voltage controlled oscillator **2**, and a modulating voltage to the modulation input of the voltage controlled oscillator **2**. Also, the microprocessor **8** controls the RF power amplifier **3** by supplying a keying signal to the keying input of the RF power amplifier **3**.

Included in the microprocessor **8** is a recirculating register **10** coupled to the modulation input of the voltage controlled oscillator **2** through second resistor **R7**. The recirculating register **10** stores a spread spectrum chip code, and outputs, during a transmitting interval, the spread spectrum chip code as a modulating voltage to the modulation input of voltage controlled oscillator **2**.

The preamble register **11** is coupled to the modulation input of the voltage controlled oscillator **2** through first resistor **R6**. The preamble includes the coarse lock preamble and the fine lock preamble. The preamble register **11** stores a coarse lock preamble in cells **12** and a fine lock preamble in cells **24**. The preamble register **11** outputs during the transmitting interval, the coarse lock preamble and the fine lock preamble as a modulating voltage to the modulation input of the voltage controlled oscillator **2** through first resistor **R6**. First resistor **R6** and second resistor **R7** are chosen such that the desired spreading from the chip code and the data coming from the preamble register **11** is achieved.

Also shown in FIG. **2** is an address register **14** coupled to the modulation input of the voltage controlled oscillator **2** through the preamble register **11** and first resistor **R6**. The address register **14** stores a device address and a type code, and outputs during a transmitting interval, the device address and type code as a modulating voltage to the modulation input of the voltage controlled oscillator **2**.

A data register **18** is coupled to a data input **20** and to the modulation input of the voltage controlled oscillator **2** through the preamble register **14** and the address register **11**. The data register **18** stores data received from the data input, and outputs, during the transmitting interval, the data as a modulating voltage to the modulation input of the voltage controlled oscillator **2**. The data from the preamble register **11**, address register **14**, and data register **18** are outputted in sequence, and at the end of a sequence, the cyclical redundancy check generator **19** outputs a data word at the end of the code for error detection.

A timing circuit **13** is included in microprocessor **8**, and is coupled to the enable input of the voltage controlled oscillator **2** and to the keying input of the RF power amplifier **3** for enabling the voltage controlled oscillator **2** and the RF power amplifier **3**, by outputting an enable signal to the enable input and a keying signal

to the keying input of the RF power amplifier **3**, respectively, during the transmitting interval. In essence, voltage controlled oscillator **2** and RF power amplifier **3** are not active or activated during a time duration of non-transmission, and are only activate during a transmission interval. The time duration between transmission intervals is made to vary in response to the random number generator **17** generating a random number and transferring the random number to the timing circuit **13**. The random number modifies the timing duration between each transmitting interval randomly.

Also shown are the voltage supply, regulator circuit **1**, and battery low detector **25**.

The spread spectrum transmitter monitors one or more data inputs **20** and transmits periodically a supervisory data message. One or more of the data inputs **20** can be set **21** such that they cause a priority transmission at an increased rate higher than the supervisory message rate.

During installation of the transmitter, a device address (**1-4095**) **12**, "Type" code **15** (fire, security, panic, heat, pull station, etc.) stored in preamble register **11**, and a spread spectrum chip code stored in recirculating register **10** are loaded via programming connector **16**. At installation time the "Panel" computer assigns the device ID address to each room number or unique device in the system which is to be monitored. The panel computer then prints a sticky label with the device's ID, address, type code and spread spectrum chip code, both in decimal and bar code form. The label is fixed to the smoke detector or alarming device and via the programming connector **16**, or the number can be entered manually with the aid of a hand-held terminal. Alternatively a bar code reader can be connected to the programming connector **16** and the device can be read electronically from the bar code and entered into the transmitter. Microprocessor timing is controlled by crystal **23**. Transmit timing is controlled by the wake-up timer **9**, which has its own low power oscillator.

In operation, the transmitter sends a supervisory message often enough so that the receiver can detect failure of any transmitter within **200** seconds. The microprocessor **8** effectively "sleeps" between these transmissions to conserve battery life while counter **9** counts down to wake-up microprocessor **8**. In order to minimize the chance of reoccurring data collisions from multiple simultaneous transmitters, the transmit interval is modified by random number generator **17**. Very fine resolution intervals are used equal to 500 temporal transmit positions. The random number generator **17** is seeded with the transmitter's unique address **14**, resulting in different transmit schedules for each unit, thereby avoiding continuous collisions between transmitters.

Once the microprocessor **8** is reset by the wake-up circuit **9** the timing circuit **13** allows the crystal **23** to stabilize for 1–5 ms. The timing circuit **13** then enables the transmitter oscillator **2** and allows it to stabilize for 1 ms. The timing circuit **13** subsequently enables the RF amplifier **3** by sending a keying signal to the keying input. The RF energy from the RF amplifier **3** is filtered by bandpass filter **4** to reduce spurious RF emissions. The filtered signal is passed to a PCB foil micropatch 2 dBi gain antenna **5** which radiates the RF energy to an appropriate receiver. When the timing circuit **13** keys the RF power amplifier **3** it also begins to recirculate the spread spectrum **31** chip code stored in recirculating register **10** at a chip rate of 1 to 1.3 MHz. The chip code in turn causes a voltage swing 0–5 volts at the modulation input of the microprocessor. The voltage swing in conjunction with a modulation setting second resistor R7 creates a proportional current which modulates voltage controlled oscillator **2** thereby generating a spread spectrum FSK signal. This improves the signal to noise ratio at the receiver by reducing required bandwidth and minimizes the chances for intersecting interference. The data is super imposed on the chip code by the resistor **6** as a 1/31 deviation of the total modulation. Two or three adjacent chip code sequences are used to equal one bit time resulting in a baud rate of 14–21 KB/s.

In order for a receiver to demodulate a spread spectrum chip code, it must time lock onto the spread spectrum chip code. Disclosed are three methods of this timing acquisition, one is serial and two are parallel assisted. All methods require some synchronization bits in the transmitted message specifically allocated to code timing acquisition, which allow the receiver to search the code and find a correlation peak. The serial correlator searches one bit time per chip in the code sequence to achieve a $\pm\frac{1}{2}$ chip code lock. This search can be hastened by searching one code sequence time instead of one bit time thereby providing a two or three to one speed increase. The parallel correlator searches all 31 chip sequences in parallel so that an initial $\pm\frac{1}{2}$ chip synchronization ("lock") can be achieved in one bit or one chip code sequence time. "Fine" code lock ($\pm\frac{1}{4}$ chip) for either serial or parallel assisted schemes must be followed by transmitted bit times allocated to allowing the receiver to achieve a higher resolution correlation "time" lock. One-quarter chip lock accuracies perform to within 1.25 dB of optimal code alignment. The receiver's fine code lock algorithm seeks to optimize the correlation peak. Higher levels of code lock can be achieved by searching in smaller fractions of a chip. This can facilitate "time of flight" distance or location measurement applications such that 25 ns, 25 feet, of measurement resolution can be achieved.

The transmitter's microprocessor **8** stores a synchronizing preamble in preamble register **11** of 36 bits for a serial correlator, which are broken into 31 bits for coarse lock **11** and 5 bits for fine lock **12**. For the two parallel correlation methods disclosed 6 bits are used in the synchronizing preamble, 1 bit for coarse lock and 5 bits for fine lock. The actual code locking bits are transmitted as alternating ones and zeros so that the receiver's data demodulator can adaptively choose an optimal 1/0 voltage level decision point. The preamble is followed by a single data message synchronization bit **24** then 12 ID address bits **14** and 3 unit type bits **15** from address register **11**, then 8 bits of input data from data register **18** and lastly 16 bits of CRC-16 data integrity check **19**. The CRC-16 generator **19** is based on the entire proceeding message.

Once the message is transmitted, the timing circuit **13** turns off the enable signal at the enable input to voltage controlled oscillator **2** and the keying input of RF power amplifier **3**, regenerates a new random number from random number generator **17**, presets that number into the transmit interval wake-up circuit **9** and then sets the microprocessor **8** into the sleep mode. Battery voltage regulation is provided by a micropower regulator **1**. Battery voltage is pulse tested to conserve battery life **25**.

The CRC-16 generator can have its kernel seeded with an identification number unique to each facility. For example, the kernel can be set by the facility ad-

dress. Any facility having a transmission system which uses such a unique code as the kernel for the CRC-16 generator can be separated from adjacent facilities without additional transmission time or message bits.

Receiver

The spread spectrum receiver comprises several major blocks:

A. The RF section which converts the received signal to lower frequencies;

B. Chip code generator with means of chip code phase shifting for correlation lock;

C. Means to measure both signal strength and quieting to detect correlation lock over the dynamic range of the system;

D. An adaptive data demodulator tolerant to DC i.e.: long strings of 1's or 0's; and

E. microprocessor algorithms to perform the above.

FIG. 3A shows the RF portion of the receiver which converts the received signal to lower frequencies. FIG. 3B shows a chip code generator with means for shifting a chip code phase for correlation lock, and means for measuring signal strength and the quieting output of the receiver to detect correlation lock over the dynamic range of the system. In FIG. 3A, a first polar diversity antenna **100** and a second polar diversity antenna **102** are shown and are physically turned so that their spatial phase relationship is 90°. Signals received from each of the first and second polar diversity antennas **100, 102** are passed through a 45° phase shifting network **104, 103**, respectively and then to a combiner **105**. The combiner **105** combines the signals received from the first and second polar diversity antennas **100, 102**. The combined signal then passes through a first bandpass filter **106**, is amplified by amplifier **107** and passed through a second bandpass filter **108**, and is mixed with the mixer **109**. Typically, a crystal **125** controls the frequency of an oscillator **126**. The signal from oscillator **126** is frequency multiplied by first, second and third frequency multipliers **128, 129, 130**. The signal is mixed at first mixer **109** with the received signal from second bandpass filter **108**. The oscillator **126** is modulated by the spread spectrum chip code through a phase shifter **127**. The spread spectrum chip code is generated by the circuit in FIG. 3B. First mixer **109** down converts the received signal to a first intermediate frequency signal. The first intermediate frequency signal is in a first intermediate frequency range, and is passed through third bandpass filter **110**, amplified by second amplifier **111** and passed through fourth bandpass filter **112**. The output signal from bandpass filter **112** is mixed with a second mixer **113** with a second oscillator signal from second oscillator **132** to a second intermediate frequency. The frequency of the second oscillator **132** is controlled by second crystal **131** and frequency multiplied by fourth frequency multiplier **133**. The second intermediate frequency signal is then passed through fifth bandpass filter **114**, amplified by third amplifier **115**, filtered by sixth bandpass filter **116**, and amplified by fourth amplifier **117**. The second intermediate signal then passes via two routes. The first route passes through seventh bandpass filter **118**, fifth amplifier **119** and quadrature detector **121**. The quadrature detector **121** is coupled to a 90° phase shift network **120**. The output of the quadrature detector **121** is the pre-data. Taps are taken from fourth and fifth amplifiers **117, 119**. Signals from these taps pass through signal strength combiner **122**, pass through eighth bandpass filter **123** and sixth amplifier **124**. The output of sixth amplifier **124** is the signal strength.

Referring to FIG. 3B, an apparatus which is embodied as a microprocessor **147** is shown for synchronizing a spread spectrum chip code using a two step algorithm in a microprocessor coupled to the pre-data output of the receiver. The signal from the pre-data output of the receiver passes through circuitry for generating a quieting output of the receiver.

The signal from circuitry coupled to the pre-data output, for generating the quieting output, includes amplifier **135**, ninth bandpass filter **140**, signal compressor **141**, quadrature detector filter **142** to produce the quieting output from seventh amplifier **143**. The output of seventh amplifier **143** is the quieting output, and passes to the microprocessor **147** through analog to digital converter **150**. The pre-data signal also passes through a filter comprising fourth and fifth resistors **138, 137** operational amplifier **139** with sixth resistor **158**, and first and second capacitors **157, 156**. This signal is fed to the microprocessor **147**.

The microprocessor **147** further includes means coupled to the correlation means for computing the adaptive average in response to the amplitude of the first data signal not exceeding the preset margin by adding the amplitude of the first data signal to the previously computed adaptive average. The microprocessor **147** comprises means coupled to the quieting output of the receiver via amplifier **143** for correlating the amplitude of a second data signal in response to the amplitude of the first data signal exceeding the preset margin. The second data signal is from the quieting output of the receiver. The first data signal is the digitized amplitude of the first signal, and the second data signal is the digitized amplitude of the second signal. When correlating the second data signal, the microprocessor **147** compares multiple iterations of the spread spectrum chip code, by comparing the second data signal to the adaptive average by a preset margin to determine whether the amplitude of the second data signal exceeds the preset margin.

The microprocessor **147** synchronizes the spread spectrum chip code by comparing the first signal during one information bit to an adaptive average to determine whether coarse correlation has been achieved. In response to the first signal not achieving coarse correlation, the microprocessor **147** computes an adaptive average by adding a first portion of the first data signal to a second portion of the adaptive average. Additionally, the microprocessor **147** correlates a second signal in response to the amplitude of the first signal exceeding the adaptive average by a preset margin to within a portion of one chip of the spread spectrum chip code by comparing the amplitude of the second signal to the adaptive by a preset margin to determine whether the second signal exceeds the preset margin.

The microprocessor **147** also generates a spread spectrum chip code for use with the receiver, which is inputted through phase shifter **127** to oscillator **126** of FIG. 3A. The apparatus, which includes the microprocessor **147** and related circuitry, includes means for entering a spread spectrum chip code having n chips. The entering means may be embodied as hand terminal **153**. Also, the apparatus includes memory means for storing chip words, which may be embodied as random access memory **146**. The random access memory **146** is coupled to the microprocessor **147**. The random access memory **146** stores each chip word having a plurality of bits per

chip. In a preferred embodiment, there are four bits per chip word. The apparatus further includes counting means coupled to the random access memory **146** for sequencing through n addresses of the chip words in the random access memory **146** and sequentially outputting the chip words to the receiver. The counting means may be embodied as adder **145** and timing circuit **147** with AND gate **159** for determining when to roll over when counting through n chip words. Clock divider **134** is included for controlling the microprocessor **147**.

In operation, the RF energy is received by two polar diversity antennas **101** and **102** which are physically rotated 90 degrees, then phase shifted +45 degrees by the first phase shifter **103**, and −45 degrees by the second phase shifter **104** and finally summed **105**. This polar diversity method enhances faded area reception. The signal is bandwidth limited to 2.0 MHz by a first bandpass filter **106**, amplified by first amplifier **107** and bandpass filtered by second bandpass filter **108** before being presented to the first mixer **109**.

The first local oscillator generated by a crystal controlled oscillator **126** which is then phase modulated to the equivalent frequency pull of a modulation of 90° at a rate set by the chip code generator.

The chip code is initially selected by either the hand terminal **153** or by the remote serial port **155**. Four chip code sets are loaded into the RAM **146** such that a single "1"0 is represented as "1111", this allows sub chip code searches by sequencing the two low order ram address bits. The ram memory is addressed at four times the chip rate so that ¼ chip resolution code searches can be performed. The counter **144** in conjunction with the clock input **156** sets this chip code rate. The binary counter **144** causes the RAM **146** to sequentially select and modulo repeat the entire stored chip code. The AND gate **59** determines the 31st count state ×4 to create a reset pulse and causes the counter to cycle through (31×4) modulo states. In order to rapidly jump to any chip code table position the summer **145** is used to add offset **161** selected by the microprocessor's search algorithm. The flip-flop **160** synchronizes the output of the RAM **146** to the chip code clock **156** to avoid variable propagation delays due to the counters and adders.

Once the chip code has modulated the oscillator **126**, the combined signal is multiplied by **128**, **129**, and **130** to provide a signal from the first local oscillator to frequency mixer **109**. This mixing stage **109** provides several features including lowering the frequency to 160 MHz, narrowing the bandwidth to 125 kHz, and when the microprocessor locks the code sequence, the mixer **109** despreads the original transmitted data signal.

The first mixer **109** output is bandpass filtered by third bandpass filter **110**, amplified by second amplifier **111** and bandpass filtered by fourth bandpass filter **112**. The first intermediate frequency signal is mixed by second mixer **13** with a signal from the second local oscillator. The second local oscillator signal originates from second oscillator **132** and is controlled by crystal **131**. The resulting sine wave is frequency multiplied by fourth frequency multiplier **133** before being mixed at second mixer **113**. The signal resulting from the second mixer **113** is lowered in frequency to 10.7 MHz and is bandpass filtered by fifth bandpass filter **114**, amplified by third amplifier **115** and bandpass filtered by sixth bandpass filter **116**. This signal is sent to fourth amplifier **117** with feedback bias current measured along with fifth amplifier **119** by a signal strength measurement circuit **122**. The signal strength measurement is low pass filtered by first lowpass filter **123** and buffered by sixth amplifier **124** before passing to the signal strength analog multiplexer input **152**.

The signal from fourth amplifier **117** is filtered by sixth bandpass filter **118** and amplified by fifth amplifier **119**. This output of fifth amplifier **119** is then quadrature detected with the aid of phase shifting circuit **120**. The output of the quadrature detector **121** is buffered by amplifier **135**, then high pass filtered **140**. The signal is compressed to a manageable 45 dB dynamic range by compressor **141**. The compressed signal is passed through a quieting detector filter **142** and buffered by amplifier **143** before being inputted to the analog multiplexer input **151**.

The "pre-data", buffered by amplifier **135**, is also presented to an adaptive data demodulator. Varying DC levels will be present on this signal due to frequency uncertainty between the receiver and transmitters. The data 1/0 decision threshold is chosen as the average voltage of an alternating 1/0/1 . . . pattern in the synch preamble. During the preamble code lock search time, the analog switch **136** is enabled and pre charges capacitor **156** through resistor **137**. This places an average voltage on capacitor **156** between a logic "1" and a logic "0". Once code lock is achieved, and the data message synchronization bit **24** is detected, the analog switch **136** is opened leaving the capacitor **156** at a stable level for the duration of the message. The buffered pre-data level is then filtered **157** with hysteresis set by resistors **158** and **138** and compared to the voltage level on capacitor **156**. This results in reliable data bits provided on the output of voltage comparator **139**.

## Code Locking Algorithm

The code locking algorithm seeks to determine a correlation peak by comparing the received RF signal energy to a microprocessor controlled copy of the desired chip code pattern. The code locking algorithm digitizes the quieting detectors analog output once per bit time. The software maintains an adaptive average of the quieting samples to determine the level of correlation improvement. The described algorithm code locks to within ¼ chip time or within 1.25 dB of optimum. The baseband output also can be used in place of the quieting output.

The present invention includes three methods of using a microprocessor for synchronizing the timing acquisition of a spread spectrum chip code received by the receiver. The spread spectrum signal comprises a plurality of information bits. Each information bit is spread in spectrum by a plurality of chips from a spread spectrum code. The first method, as depicted in FIG. **4**, comprises the steps performed by the microprocessor of inserting **401** a delay of one information bit time before the first information bit received by the receiver, and sampling and digitizing **402** the first signal from the quieting output of the receiver to generate a first data signal. The sampling and digitizing alternatively can be taken from the baseband or signal strength output of the receiver. The first method compares **404** the amplitude of the first data signal to the adaptive average during the time of one information bit to determine whether coarse correlation has been achieved. In response to coarse correlation not being achieved, the method computes **405** the adaptive average by adding a first portion of the amplitude of the first data signal to a second portion of the previously computed adaptive average. If

the coarse correlation has been achieved, then the method shifts **407** the chip code by a third portion of one information bit time. In a preferred embodiment of the present invention, the chip time is divided into four portions, thus the shifts **407** is equivalent to delaying the chip by ¼ chip time duration.

An additional delay is inserted **408** and the method samples and digitizes **409** a second signal from the quieting output of the receiver to generate a second data signal. The amplitude of the second data signal during one information bit time is compared **410** to the adaptive average to determine whether fine correlation has been achieved. If fine correlation has been achieved, then a data capture algorithm is initiated **414**. If fine correlation has not been achieved, then the method shifts **412** the chip code phase shifter by a third portion, which is equivalent in the present preferred embodiment to a ¼ time duration of a chip. The method then proceeds to initiate the data capture algorithm.

A delay **401** is inserted before digital conversion of the quieting output **402**. This delay serves to insure reoccurring data samples equal to one information bit time. The new sample is compared to the running adaptive average **403**. If the improvement is greater than a preset margin, then coarse correlation **404** is achieved. Otherwise, if the new sample is within the noise error of the running average, the new sample is combined with the old average **405**; average=(0.25 new +0.75 old average). The chip code phase shifter **161** is incremented by a count of 4 (1 chip time). This coarse code lock algorithm is then indefinitely repeated until coarse code lock is acquired.

If coarse correlation is achieved **404**, then the algorithm seeks to "fine" code lock. The chip code phase shifter **161** is shifted **407** by one (¼ chip time). The one information bit time synchronizing delay is passed **408**. The quieting detector output is digitized **409** and compared **410** to the running quieting output average. If the new sample did not improve **411** the quieting by the preset margin then the chip code phase shifter is incremented **412** by ¼ chip to its past more optimum position. Fine lock is completed **414** and the code lock algorithm jumps to a data capture algorithm.

If the required margin of quieting improvement is achieved **411**, then the number of chip code shifts is checked **413**. Any search code position which is shifted more than three ¼ chip steps would undesirably slip one whole code cycle. Comparison **413** stops a search on the third code slip and assumes an optimum correlation is achieved then proceeds to the data acquisition algorithm **414**. If three code phase decrements have not occurred, the algorithm repeats at shift **407**.

FIG. **5** shows four cases with one-quarter chip code lock achieved in each case using the first method.

A second method and apparatus for synchronizing a spread spectrum chip code using the baseband signal output of the receiver is shown in FIG. **6**. The apparatus aspect of the invention includes means for sampling and digitizing a plurality of analog baseband signals, register means for shifting the plurality of data signals, means for adding in parallel the plurality of data signals, means for comparing the correlation sum and means for dithering a chip/sample clock by a portion of a chip time. The sampling and digitizing means may be embodied as analog to digital converter **201** The register means may be embodied as the plurality of registers **202, 203, 204**. The adding means may be embodied as adders **205, 206, 207** and the comparing means may be embodied as comparator **213**. The dithering means may be embodied as the microprocessor **215**.

As illustratively shown, the apparatus for synchronizing the spread spectrum chip code has the analog to digital converter **201** coupled to the RF baseband output of the receiver **212**. The analog to digital converter **201** samples and digitizes the plurality of analog baseband signals from the baseband output of the receiver **212** and generates a plurality of data signals. The plurality of registers **202, 203, 204** is coupled to the analog to digital converter **201** and shifts the plurality of data signals sequentially through the plurality of registers **202, 203, 204**. The plurality of adders **205, 206, 207** are coupled to the plurality of registers **202, 203, 204**, respectively, for adding in parallel each of the data signals stored in the plurality of registers **202, 203, 204** according to a plurality of predetermined weights for each of the plurality of data signals, respectively, to generate a correlation sum. The weights are controlled by flip flop circuits **209, 210, 211**, which contain the spread spectrum chip code. The adder **207** outputs a correlation sum **208** to a comparator **213** for comparing the correlation sum to a predetermined margin or threshold. The dithering circuit embodies as a microprocessor **215** is coupled to the comparator **213** and dithers the chip clock by at least a first portion of one chip time, thereby improving chip lock.

In operation, the second method of using a microprocessor for synchronizing the timing acquisition of the spread spectrum chip code received by a receiver comprises the steps of sampling and digitizing using the analog to digital converter **201**, the plurality of analog baseband signals from the baseband output of the receiver **212**, to generate a plurality of data signals. Each of the analog baseband signals is sampled and digitized during one chip time. The method shifts the plurality of baseband signals through the plurality of shift registers **202, 203, 204**. The plurality of data signals are added in parallel according to a plurality of predetermined weights, from flip flops **209, 210, 211** for each of the plurality of data signals, respectively, in the plurality of adders **205, 206, 207** to generate a correlation sum **208**. The correlation sum **208** is compared to a predetermined threshold or preset margin, and a chip clock is then dithered by at least a first portion of one chip time to improve clock lock. In a preferred embodiment, the first portion is one quarter of one chip time.

The chip clock samples once per chip time. A coarse chip lock may therefore be incorrect by ±½ of a chip. To improve the lock, the chip clock is slewed in ±¼ and/or ±⅛ chip steps controlled by an algorithm in microprocessor **215**. A clock with a rate equal to four times the chip rate is counted by counter **214**. The counters output is compared to an output of the microprocessor **215** equal to the code phase being searched. The microprocessor **215** can thereby search in fine chip code steps after a rapid parallel assisted search in 1, 31 chip code time. The total search required is equal to 6 chip code times, which can be sent in the spread spectrum transmitters code-lock preamble as disclosed.

As a further component reduction of the circuitry described above in the second species of the method and apparatus for synchronizing a spread spectrum chip code, the parallel assisted chip code lock can be serially summed instead of parallel summed. The serial sum of all 31 stages must be computed between chip samples (less than 1,000 ns). This speed can be achieved with

available high speed CMOS ASICS with clock speeds of 40 MHz or greater.

A third species of the spread spectrum chip code synchronizing method and apparatus is disclosed in the present invention, and is set forth in FIG. 7. The third species of the spread spectrum chip code synchronizing apparatus couples to the baseband output of the receiver. The apparatus includes means coupled to the baseband output of the receiver for sampling and digitizing the plurality of analog baseband signals, register means coupled to the sampling and digitizing means for shifting and recirculating the plurality of data signals, and means coupled to the register means for adding sequentially the data signals passing through the shift register means. As shown in FIG. 7, the sampling and digitizing may be embodied as analog to digital converter **310**. The register means may be embodied as registers **307, 308, 309** and the adding means may be embodied as adder **303**. As shown in FIG. 7, the analog to digital converter **310** is coupled to the baseband output of the receiver, and passes through a plurality of gates **302** to the plurality of registers **307, 308, 309,** to adder **303**. Also shown is a plurality of flip flops **306, 311, 312** having the spread spectrum chip code therein. The flip flops **306, 311, 312** input the spread spectrum chip code into the adder **303**. The adder **330** is coupled to a correlation sum accumulator **304** which outputs a correlation sum **305**.

In the preferred embodiment, the third species of the apparatus for synchronizing the spread spectrum chip code has the analog to digital converter **310** coupled to the baseband output of the receiver for sampling and digitizing a plurality of analog baseband signals and generating a plurality of data signals. Each of the analog baseband signals is sampled and digitized during one chip time. The plurality of registers **307, 308, 309** is coupled to the analog to digital converter **310** through gates **302** for shifting and recirculating the plurality of data signals sequentially through the plurality of registers **307, 308, 309** and gates **302**. The adder **303** is coupled to register **309** for adding sequentially the data signals passing through registers **309** according to predetermined weights set forth in flip flops **306, 311, 312**.

In operation, the third method of uses a microprocessor for synchronizing the timing acquisition of the spread spectrum chip code received by the receiver. The method samples and digitizes the plurality of analog baseband signals from the baseband output of the receiver using analog to digital converter **310**, to generate a plurality of data signals. Each of the analog baseband signals is sampled and digitized during one chip time. The method further includes shifting and recirculating the plurality of data signals sequentially through the plurality of registers **307, 308, 309**. The data signals are added sequentially as they pass through register **309** using adder **310** and accumulated. The correlation sum accumulator **304** then passes the correlation sum **305** to the microprocessor.

The third method is similar to the second method, except that there is only one adder **303** for the entire register chain instead of one adder per stage. The registers **307, 308, 309** are steered to recirculated by the AND/OR gates **302**. The stored chip code string can also be shifted and recirculated. After each chip clock rising stage transition, an analog data sample is converted by analog to digital converter **310** and stored in register **307**. Data in the registers are shifted to the right as in the circuit in of FIG. **6**. Immediately following the chip sample, a sequence is performed to accumulate a correlation sum. The AND/OR steering gates **301** and **302** are switched to the "sum" state. This passes a high speed summing clock of **40** MHz for **31** clock cycles to the registers **307, 305, 309** and to the stored spread spectrum chip code in **306, 311, 312**. The steering gates **302** causes data in registers **307, 305, 309** to recirculate so that after **31** clock cycles of the adding phase, the data in registers **307, 308, 309** will be in their original positions and ready to accept another spread spectrum chip code data sample and store phase. After each 40 MHz summing clock transition a new sum is generated by adder **303** and accumulated in accumulator **304**. Adder **303** is caused to either add or subtract the inputs Ain from the accumulated total. This is determined by the stored chip code string in flip-flop **312** which creates the x (+1) or x (−1) correlation weighting causing either the addition or subtraction of the Ain inputs. The outputs of accumulator **304** are transferred to the next register stage and then at the next clock rising edge, the accumulator stores that total. After 31 summing clock cycles the accumulation **304** will contain the correlation sum **305**. The multibit words stored and summed by the two alternative methods can be reduced to one bit samples and sums, resulting in a small loss of performance.

It will be apparent to those skilled in the art that various modifications can be made to the wireless detection system of the instant invention without departing from the spirit or scope of the invention, and it is intended that the present invention cover modifications and variations of the wireless detection system provided they come within the scope of the appended claims and their equivalents.

We claim:

**1.** A spread spectrum transmitter comprising:

modulation means having an enable input and a moduation input, for modulating an RF signal with spread spectrum for reducing interference and providing code division multiple access in response to a modulating voltage being applied at the modulation input and an enable signal being applied at the enable input;

an RF power amplifier coupled to said modulating means, and having a keying input;

a bandpass filter coupled to said RF power amplifier;

an antenna coupled to said bandpass filter;

a microprocessor coupled to said modulation means and said RF power amplifier for controlling said modulation means and said RF power amplifier, respectively, said microprocessor including,

chip-code-generation means coupled to the modulation input of said modulation means for storing a spread spectrum chip code, and outputting, during a transmitting interval, the spread spectrum chip code as a modulating voltage to the modulation input of said modulating means;

a preamble register coupled to the modulation input of said modulation means for storing a preamble, and outputting, during the transmitting interval, the preamble as a modulating voltage to the modulation input of said modulation means;

an address register coupled to the modulation input of said said modulation means through said preamble register for storing a device address and a type code, and outputting, during the transmitting interval, the device address and type code as

a modulating voltage to the modulation input of said modulation means;

a data register coupled to a data input and to the modulation input of said modulation means through said preamble register and said address register, for storing information data received from the data input, and outputting, during the transmitting interval, the information data as a modulating voltage to the modulation input of said modulation means;

error detection means coupled to said data register for generating error detection data from the preamble, device address and type code and the information data, wherein said error detection means is initialized with a value unique to each installation using said spread spectrum transmitter;

wherein said preamble register, said address register, said data register and said error detection means sequentially output the preamble, device address and type code, error detection data and information data to the modulation input and the spread spectrum chip code from said chip code generating means spreads the preamble, device address and type code, error detection data and information data to generate the spread spectrum of the RF signal, and wherein the preamble provides acquisition for spread spectrum synchronization for demodulating the spread spectrum of the RF signal;

a timing circuit coupled to the enable input of said modulation means and to the keying input of said RF power amplifier for enabling said modulation means and said RF power amplifier, by outputting an enable signal to the enable input of said modulation means and a keying signal to the keying input of said RF power amplifier, respectively, during the transmitting interval; and

a pseudorandom sequence generator coupled to said timing circuit for generating a random number for modifying the timing duration between each transmitting interval.

2. An apparatus coupled to a keying input of an RF power amplifier of a spread spectrum transmitter, for controlling said spread spectrum transmitter, said apparatus comprising:

a modulator having a modulation input, for modulating an RF signal with spread spectrum for reducing interference and providing code division multiple access;

chip-code-generation means coupled to the modulation input of said modulator for storing a spread spectrum chip code, and outputting the spread spectrum chip code as a modulating voltage to the modulation input of said modulator;

a preamble register coupled to the modulation input of said modulator for storing a preamble, and outputting the preamble as a modulating voltage to the modulation input of said modulator;

an address register coupled to the modulation input of said modulator for storing a device address, and outputting the device address as a modulating voltage to said modulator;

a data register coupled to a data input and to the modulation input of said modulator for storing information data received from the data input, and outputting the information data as a modulating voltage to the modulation input of said modulator; and

wherein said preamble register, said address register, and said data register sequentially output the preamble, device address, and information data to the modulation input and the spread spectrum chip code from said chip code generating means spreads the preamble, device address, and information data to generate the spread spectrum of the RF signal, an wherein the preamble provides acquisition for spread spectrum synchronization for demodulating the spread spectrum of the RF signal.

3. An apparatus coupled to a modulation input of a modulator of a spread spectrum transmitter, for controlling said spread spectrum transmitter, for communicating with a receiver, said apparatus comprising:

chip code generation means coupled to the modulation input of said modulator for storing a spread spectrum chip code, and outputting the spread spectrum chip code as a modulating voltage to said modulator;

a preamble register coupled to the modulation input of said modulator for storing a preamble, and outputting the preamble as a modulating voltage to the modulation input of said modulator;

an address register coupled to the modulation input of said modulator for storing a device address, and outputting the device address as a modulating voltage to the modulation input of said modulator;

a data register coupled to a data input and to the modulation input of said modulator for storing information data received from the information data input, and outputting the data as a modulating voltage to the modulation input of said modulator;

a cyclical redundancy check generator coupled to said data register for generating error detection data from the preamble, device address, and the information data;

a timing circuit coupled to said modulator for enabling said modulator during a transmitting interval; and

wherein said preamble register, said address register, said data register, and said cyclical redundancy check generator sequentially output the preamble, device address, and information data and error detection data to the modulation input and the spread spectrum chip code from said chip code generating means spreads the preamble, device address information data and error detection data to generate the spread spectrum of the RF signal, and wherein the preamble provides acquisition for spread spectrum synchronization of the spread spectrum of the RF signal, for demodulating the spread spectrum of the RF signal.

4. The apparatus as set forth in claim 3 further including a pseudorandom sequence generator coupled to said timing circuit for generating a random number for modifying the timing duration between each transmitting interval.

5. An apparatus coupled to modulation means having a modulation input for modulating an RF signal with spread spectrum for reducing interference and providing code division multiple access, for controlling said spread spectrum transmitter, said apparatus comprising:

chip-code-generation means coupled to the modulation input of said modulation means for storing a spread spectrum chip code, and outputting the

spread spectrum chip code as a modulating voltage to the modulation input of said modulation means;

preamble means coupled to the modulation input of said modulation means for storing a preamble, and outputting the preamble as a modulating voltage to the modulation input of said modulating means;

address means coupled to the modulation input of said modulation means through said preamble means for storing a device address, and outputting the device address as a modulating voltage to the modulation input of said modulation means;

data means coupled to a data input and to the modulation input of said modulation means through said preamble means and said address means, for storing information data received from the data input, and outputting the information data as a modulating voltage to the modulation input of said modulation means;

wherein said preamble means, said address means, and said data means sequentially output the preamble, device address, and information data to the modulation input and the spread spectrum chip code from said chip code generating means spreads the preamble, device address, and information data at the modulation input to generate the spread spectrum of an RF signal, and wherein the preamble provides acquisition for spread spectrum synchronization of the spread spectrum of the RF signal, for demodulating the spread spectrum of the RF signal.

**6.** The apparatus as set forth in claim **5** further including timing means coupled to the enable input of said oscillator for enabling said oscillator during a transmitting interval.

**7.** The apparatus as set forth in claim **5** further including pseudorandom sequence means coupled to said timing means for generating a random number for modifying the timing duration between each transmitting interval.

**8.** The apparatus as set forth in claim **5** further including error-detection means coupled to said data register for generating an error detection algorithm.

**9.** An apparatus coupled to modulation means having a modulation input for modulating an RF signal with spread spectrum for reducing interference, for controlling said spread spectrum transmitter, said apparatus comprising:

chip-code-generation means coupled to the modulation input of said modulation means for storing a spread spectrum chip code, and outputting the spread spectrum chip code as a modulating voltage to the modulation input of said modulation means;

preamble means coupled to the modulation input of said modulation means for storing a preamble, and outputting the preamble as a modulating voltage to the modulation input of said modulation means;

address means coupled to the modulation input of said modulation means for storing a device address, and outputting the device address as a modulating voltage to the modulation input of said modulation means; and

wherein said preamble means, and said address means, sequentially output the preamble, and device address, to the modulation input and the spread spectrum chip code from said chip code generating means spread the preamble, and device address at the modulation input to generate the spread spectrum of an RF signal, and wherein the preamble provides acquisition for spread spectrum snychronization of the spread spectrum of the RF signal, for demodulating the spread spectrum of the RF signal.

**10.** The apparatus as set forth in claim **9** further including timing means coupled to the enable input of said oscillator and to the keying input of said RF power amplifier for enabling said oscillator and said RF power amplifier, respectively, during a transmitting interval.

**11.** The apparatus as set forth in claim **9** further including pseudorandom sequence means coupled to said timing means for generating a random number for modifying the timing duration between each transmitting interval.

**12.** The apparatus as set forth in claim **9** further including error-detection means coupled to said data register for generating an error detection algorithm.

**13.** A method using processor means for controlling a spread spectrum transmitter having an oscillator with a modulation input and an RF power amplifier with a keying input, comprising the steps, performed by said processor means, of:

storing a spread spectrum chip code in chip code generation means coupled to the modulation input of said oscillator;

outputting, during a transmitting interval, a preamble from a preamble register to the modulation input of said oscillator;

outputting, during a transmitting interval, a device address from an address register coupled to the modulation input of said oscillator;

outputting simultaneously, during the transmitting interval, data from a data register and the spread spectrum chip code stored in said chip code generation means, to the modulation input of said oscillator, thereby generating a spread spectrum signal including the data; and

generating an enabling signal and a keying signal during the transmitting interval, from a timing circuit coupled to the enable input of said oscillator and to the keying input of said RF power amplifier, for activating said oscillator and said RF power amplifier.

**14.** A method using processor means for controlling a spread spectrum transmitter having an oscillator with a modulation input, comprising the steps, performed by said processor means, of:

outputting, during a transmitting interval, a preamble from a preamble register to the modulation input of said oscillator;

outputting, during a transmitting interval, a device address from an address register coupled to the modulation input of said oscillator; and

outputting simultaneously, during the transmitting interval, data from a data register and a spread spectrum chip code stored in chip code generation means, to the modulation input of said oscillator, thereby generating a spread spectrum signal including the data.

* * * * *

# EXHIBIT "B"

US005987058A

# United States Patent [19]

Sanderford et al.

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[54] **WIRELESS ALARM SYSTEM**

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[73] Assignee: **Axonn Corporation**, New Orleans, La.

[ * ] Notice: This patent is subject to a terminal disclaimer.

[21] Appl. No.: **08/487,523**

[22] Filed: **Jun. 7, 1995**

**Related U.S. Application Data**

[60] Continuation of application No. 07/782,345, Oct. 24, 1991, Pat. No. 5,598,427, which is a division of application No. 07/569,682, Aug. 20, 1990, Pat. No. 5,095,493, which is a division of application No. 07/266,461, Nov. 2, 1988, Pat. No. 4,977,577.

[51] **Int. Cl.**[6] ..... **H04B 1/69**

[52] **U.S. Cl.** ..... **375/208**; 375/200

[58] **Field of Search** ..... 375/200, 202, 375/208, 210, 367; 455/100, 113; 370/515

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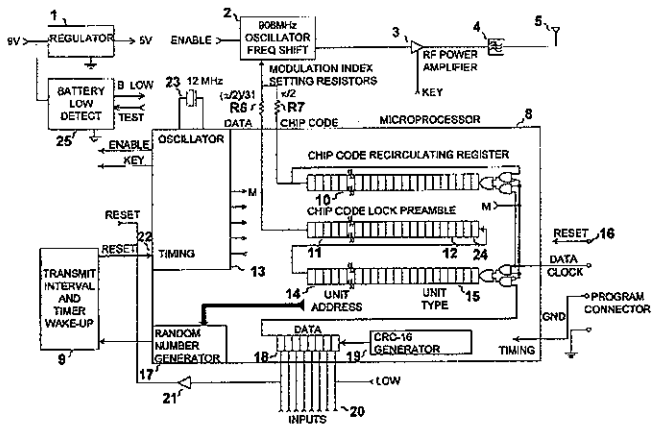
*Primary Examiner*—Young T. Tse

*Attorney, Agent, or Firm*—Oblon, Spivak, McClelland, Maier & Neustadt, P.C.

[57] **ABSTRACT**

A wireless alarm system using spread spectrum transmitters, fast frequency shift keying, spread spectrum receivers and computer with a display. The spread spectrum transmitter includes an oscillator coupled to a microprocessor with chip code generation means, preamble register, address register and data register. The spread spectrum receiver acquires synchronization of the spread spectrum signal using a microprocessor coupled to the quieting, signal strength or baseband output of the receiver, with a two step algorithm. The steps comprise achieving a coarse lock and a fine lock to the spread spectrum signal.

**95 Claims, 11 Drawing Sheets**



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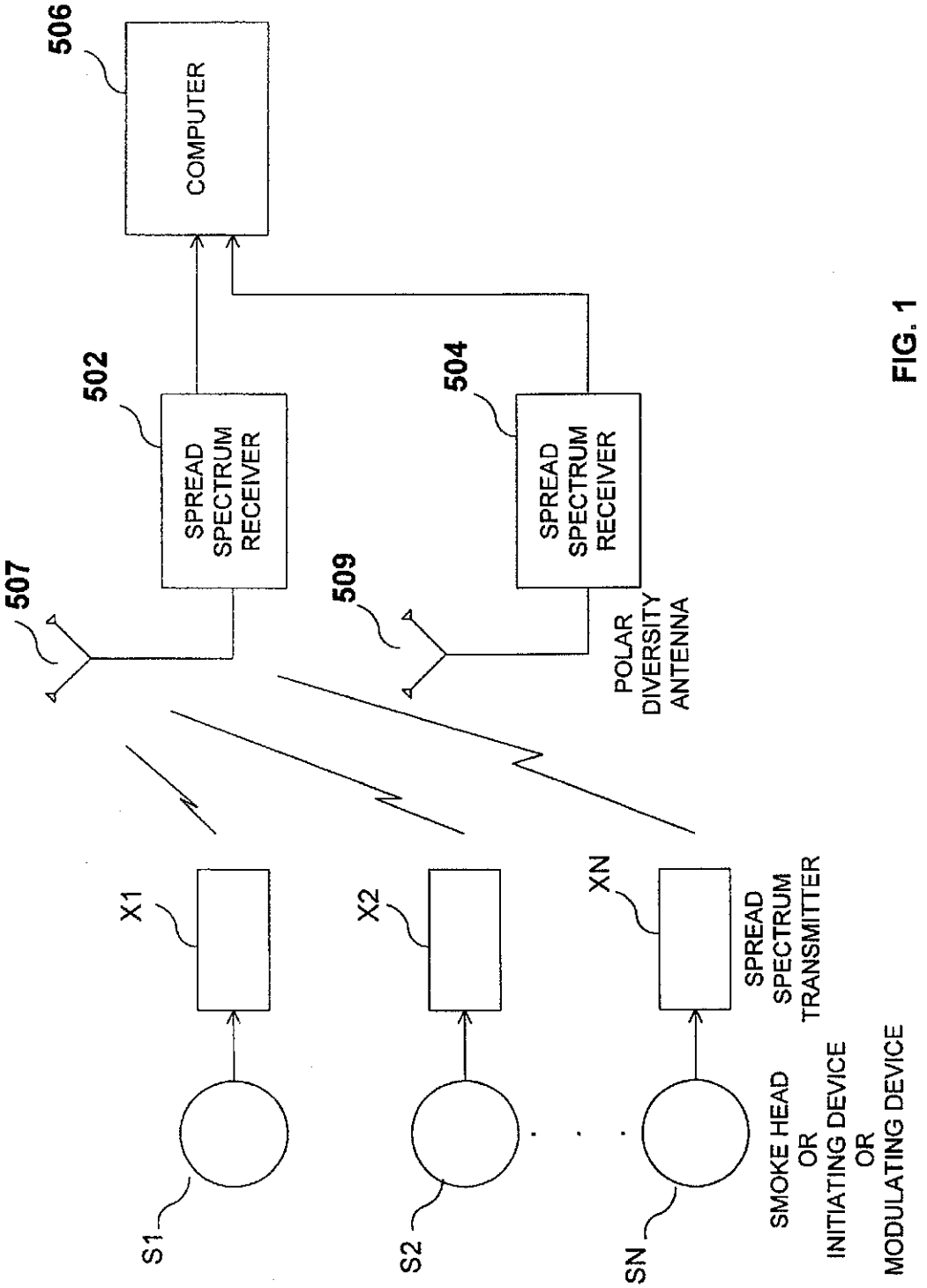
506
COMPUTER
502
SPREAD SPECTRUM RECEIVER
504
SPREAD SPECTRUM RECEIVER
507
509
POLAR DIVERSITY ANTENNA
X1
X2
XN
SPREAD SPECTRUM TRANSMITTER
S1
S2
SN
SMOKE HEAD OR INITIATING DEVICE OR MODULATING DEVICE

FIG. 1

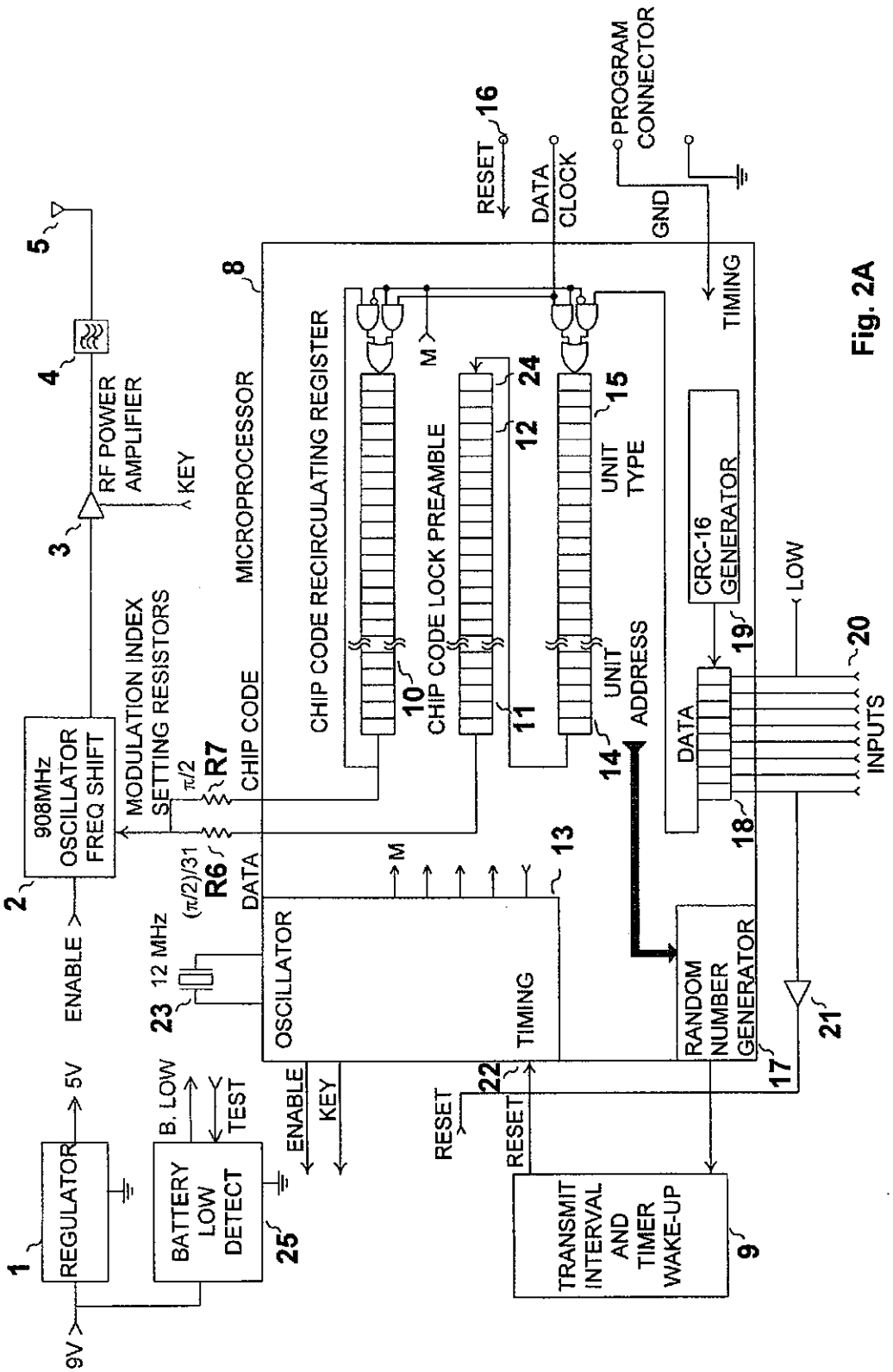
REGULATOR
5V
9V
1
BATTERY LOW DETECT
B. LOW
TEST
25
908MHz OSCILLATOR FREQ SHIFT
2
ENABLE
3
RF POWER AMPLIFIER
4
5
KEY
MODULATION INDEX SETTING RESISTORS
R7
R6
π/2
(π/2)/31
CHIP CODE
DATA
12 MHz
23
OSCILLATOR
MICROPROCESSOR
8
CHIP CODE RECIRCULATING REGISTER
10
CHIP CODE LOCK PREAMBLE
11
12
24
M
13
TIMING
22
RESET
ENABLE
KEY
TRANSMIT INTERVAL AND TIMER WAKE-UP
9
RESET
16
DATA
CLOCK
PROGRAM CONNECTOR
GND
TIMING
UNIT TYPE
15
UNIT ADDRESS
14
RANDOM NUMBER GENERATOR
17
CRC-16 GENERATOR
19
DATA
18
LOW
20
INPUTS
21

Fig. 2A

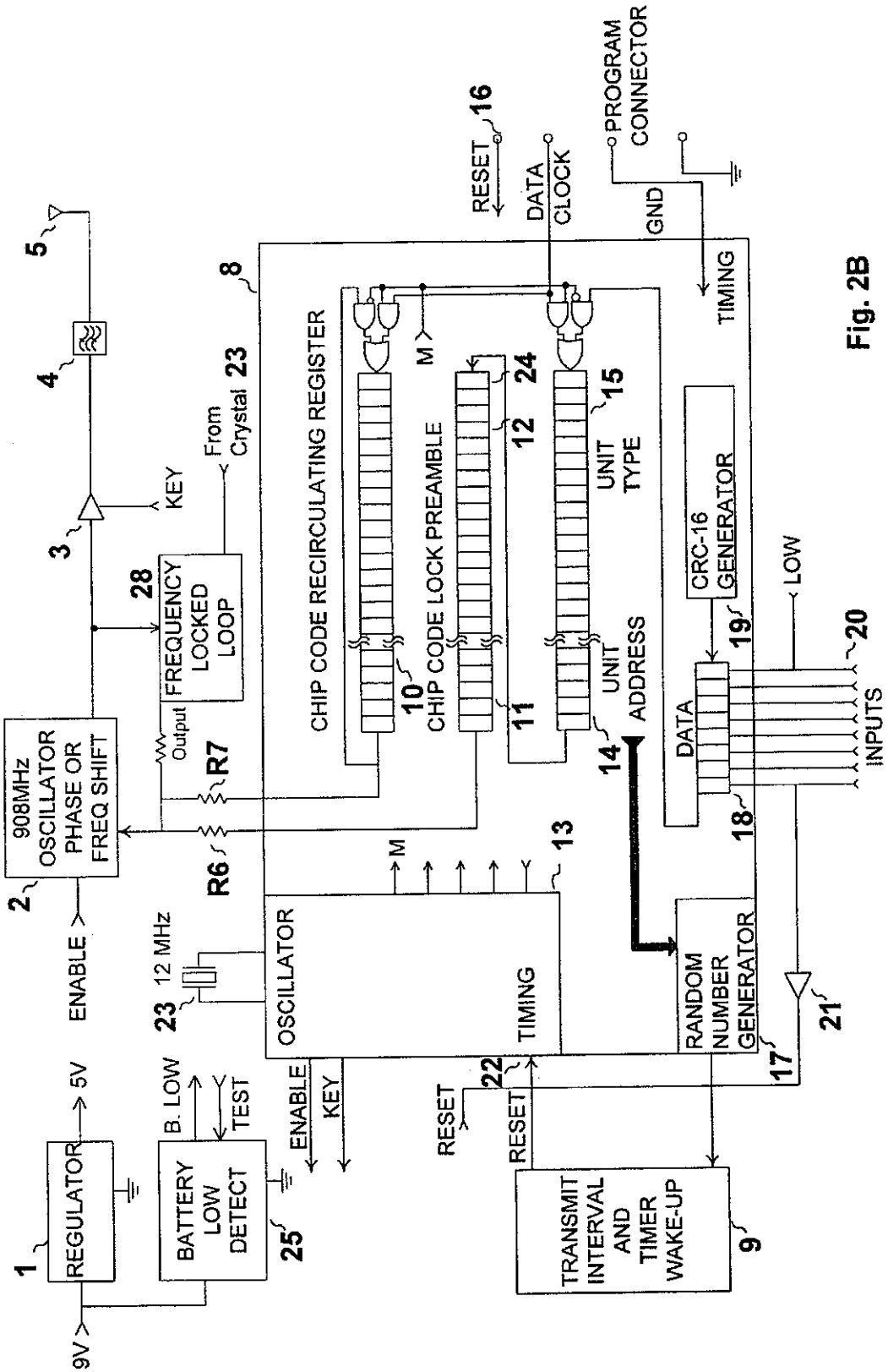
RESET 16
DATA CLOCK
PROGRAM CONNECTOR
GND
TIMING
5
4
3
8
KEY
From Crystal 23
28
FREQUENCY LOCKED LOOP
CHIP CODE RECIRCULATING REGISTER
M
24
12
15
UNIT TYPE
CRC-16 GENERATOR
LOW
19
20
CHIP CODE LOCK PREAMBLE
10
11
UNIT ADDRESS
14
DATA
INPUTS
Output
R7
908MHz OSCILLATOR PHASE OR FREQ SHIFT
R6
2
18
13
M
ENABLE
12 MHz
23
OSCILLATOR
TIMING
RANDOM NUMBER GENERATOR
21
17
5V
B. LOW
TEST
ENABLE
KEY
RESET
22
RESET
REGULATOR
BATTERY LOW DETECT
25
TRANSMIT INTERVAL AND TIMER WAKE-UP
9
1
9V

Fig. 2B

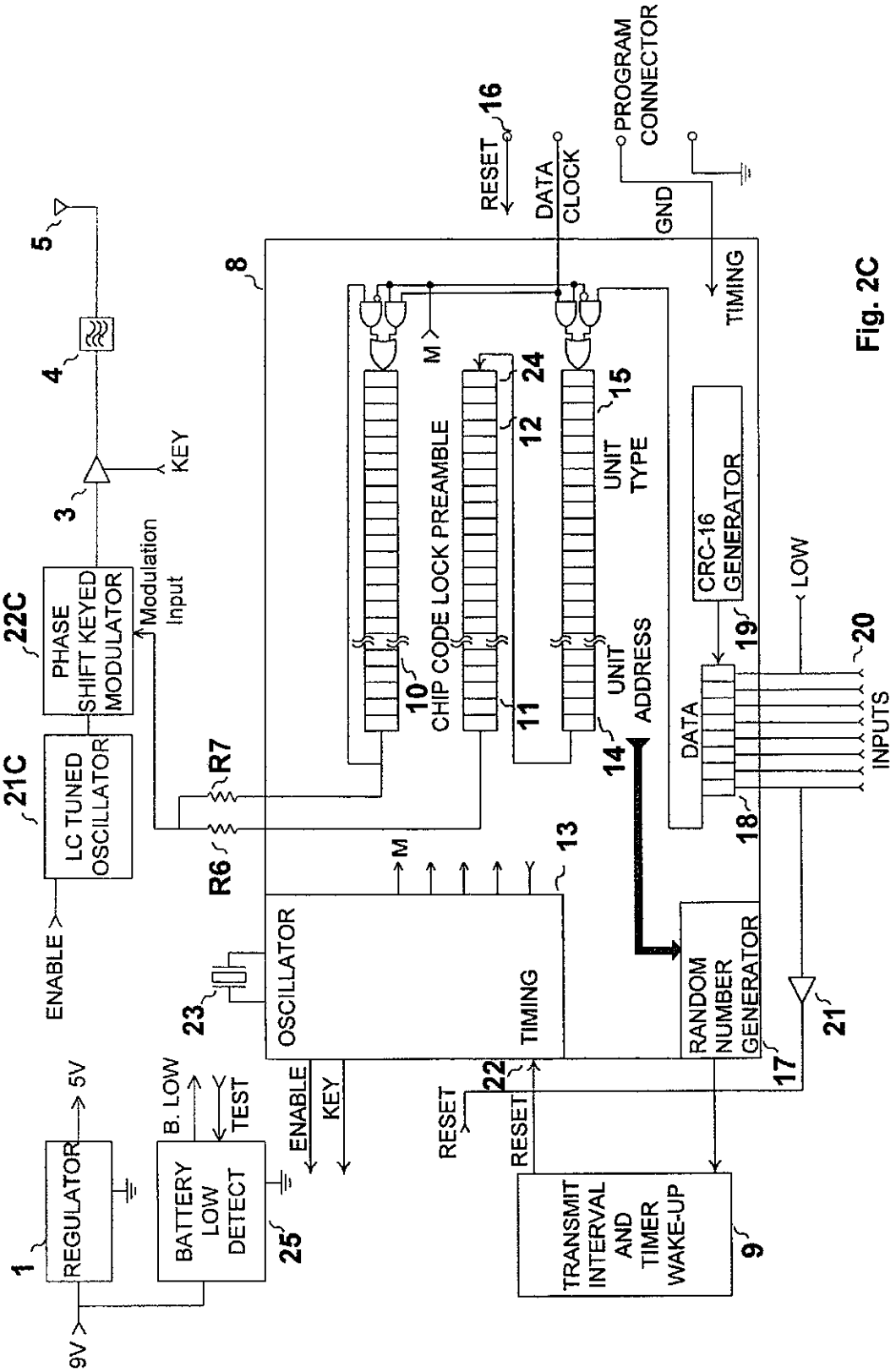
RESET
16
DATA
CLOCK
PROGRAM CONNECTOR
GND
TIMING
5
4
3
KEY
8
M
24
12
15
UNIT TYPE
CHIP CODE LOCK PREAMBLE
10
11
UNIT ADDRESS
14
CRC-16 GENERATOR
19
LOW
20
DATA
INPUTS
18
22C
PHASE SHIFT KEYED MODULATOR
Modulation Input
21C
LC TUNED OSCILLATOR
R7
R6
ENABLE
M
13
Y
23
OSCILLATOR
TIMING
RANDOM NUMBER GENERATOR
21
17
22
RESET
RESET
ENABLE
KEY
B. LOW
TEST
5V
REGULATOR
BATTERY LOW DETECT
25
1
9V
TRANSMIT INTERVAL AND TIMER WAKE-UP
9

Fig. 2C

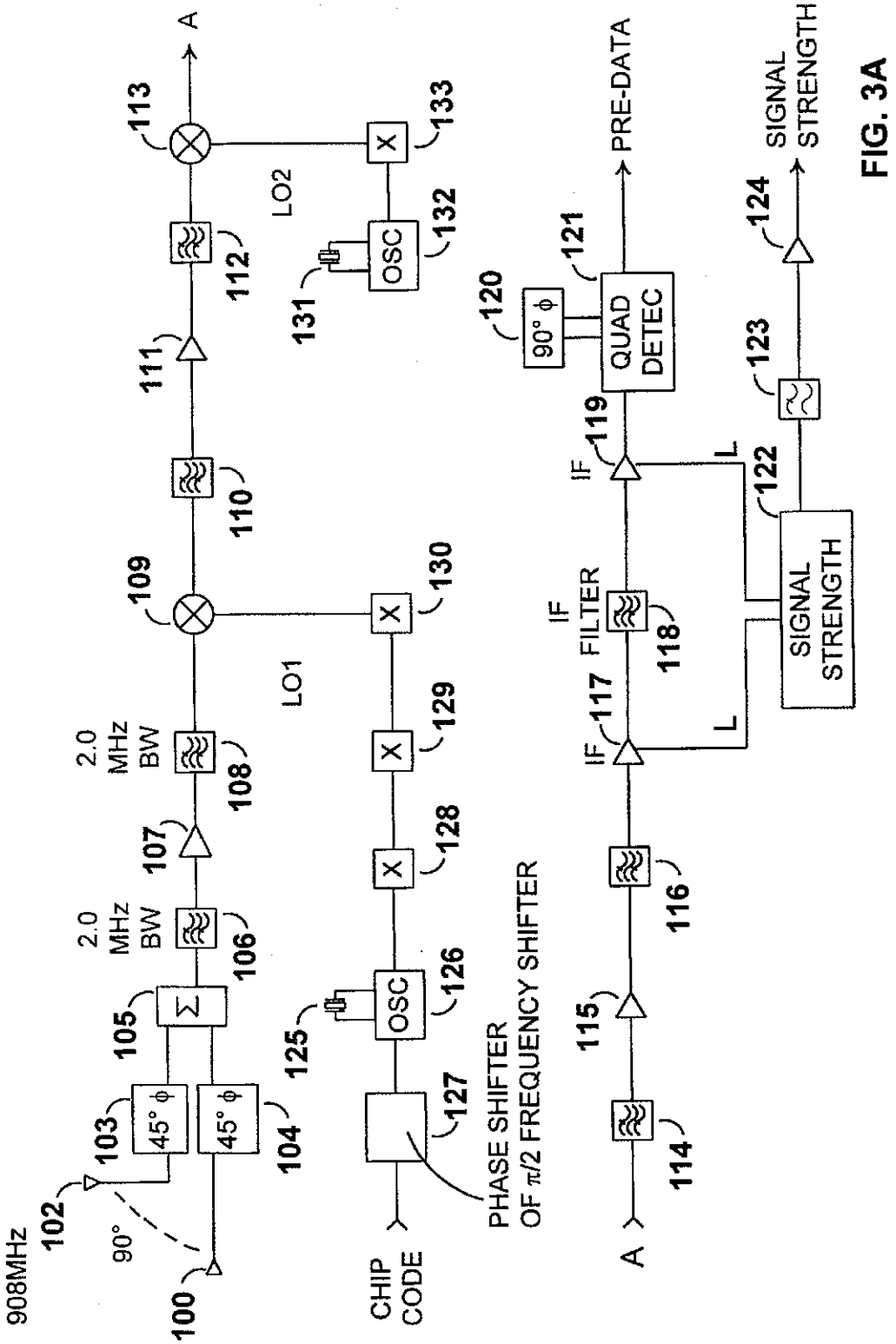
908MHz
102
90°
100
103
45° ϕ
104
45° ϕ
105
Σ
106
2.0 MHz BW
107
2.0 MHz BW
108
109
LO1
110
111
LO2
112
113
A
CHIP CODE
125
OSC
126
127
PHASE SHIFTER OF π/2 FREQUENCY SHIFTER
128
129
130
131
OSC
132
133
A
114
115
116
IF
117
IF FILTER
118
IF
119
120
90° ϕ
121
QUAD DETEC
PRE-DATA
122
SIGNAL STRENGTH
123
124
SIGNAL STRENGTH
L
L

FIG. 3A

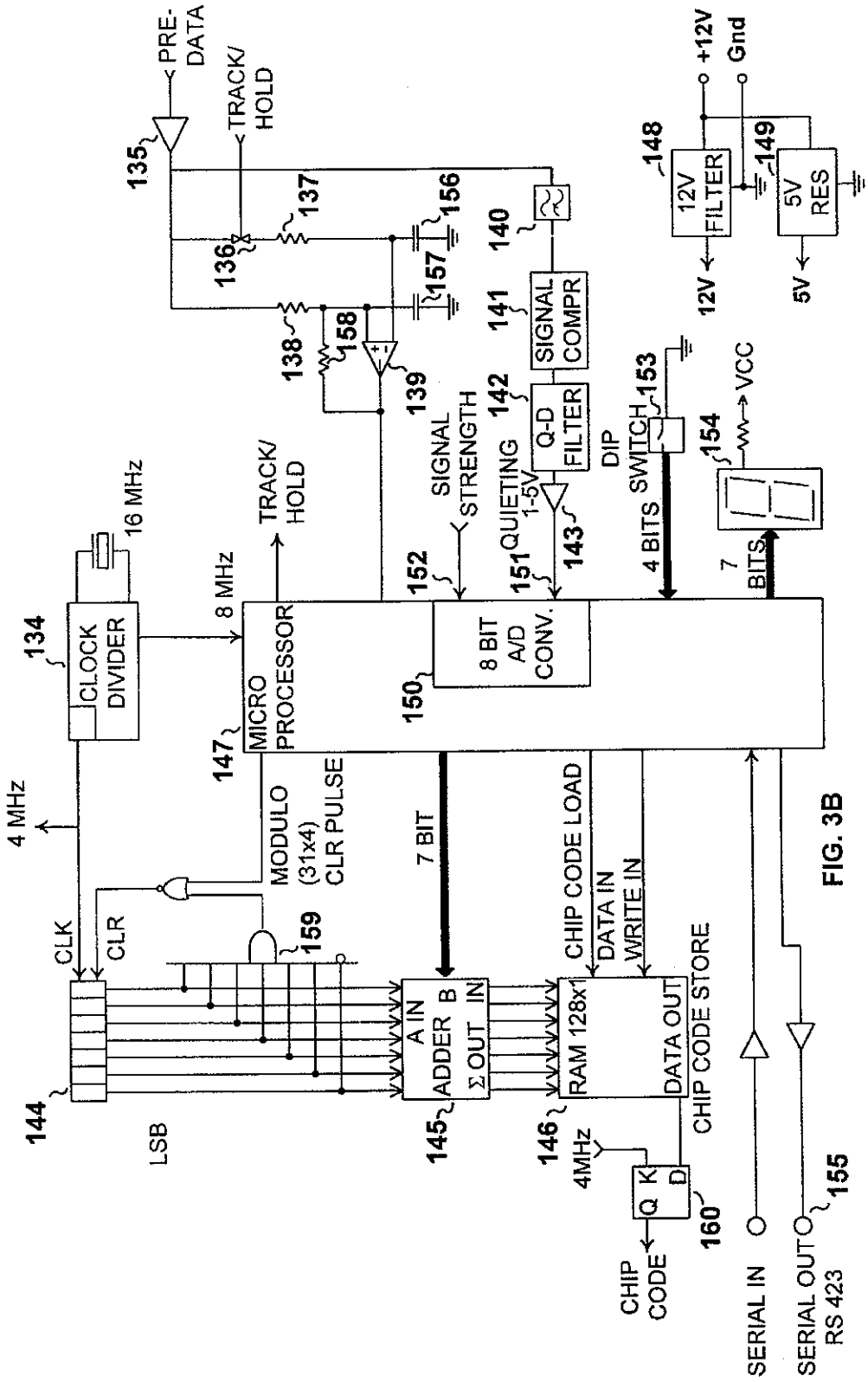
PRE-DATA
TRACK/HOLD
135
137
136
156
157
140
141
SIGNAL COMPR
138
158
139
142
Q-D FILTER
SIGNAL STRENGTH
QUIETING 1-5V
143
151
152
+12V
Gnd
148
12V FILTER
149
5V RES
12V
5V
DIP SWITCH
153
154
VCC
4 BITS
7 BITS
16 MHz
CLOCK DIVIDER
134
8 MHz
TRACK/HOLD
MICRO PROCESSOR
147
8 BIT A/D CONV.
150
4 MHz
MODULO (31x4) CLR PULSE
7 BIT
CHIP CODE LOAD
DATA IN
WRITE IN
CLK
CLR
159
144
LSB
A IN
ADDER B
Σ OUT IN
145
RAM 128x1
DATA OUT
CHIP CODE STORE
146
4MHz
Q K D
160
CHIP CODE
SERIAL IN
SERIAL OUT RS 423
155

FIG. 3B

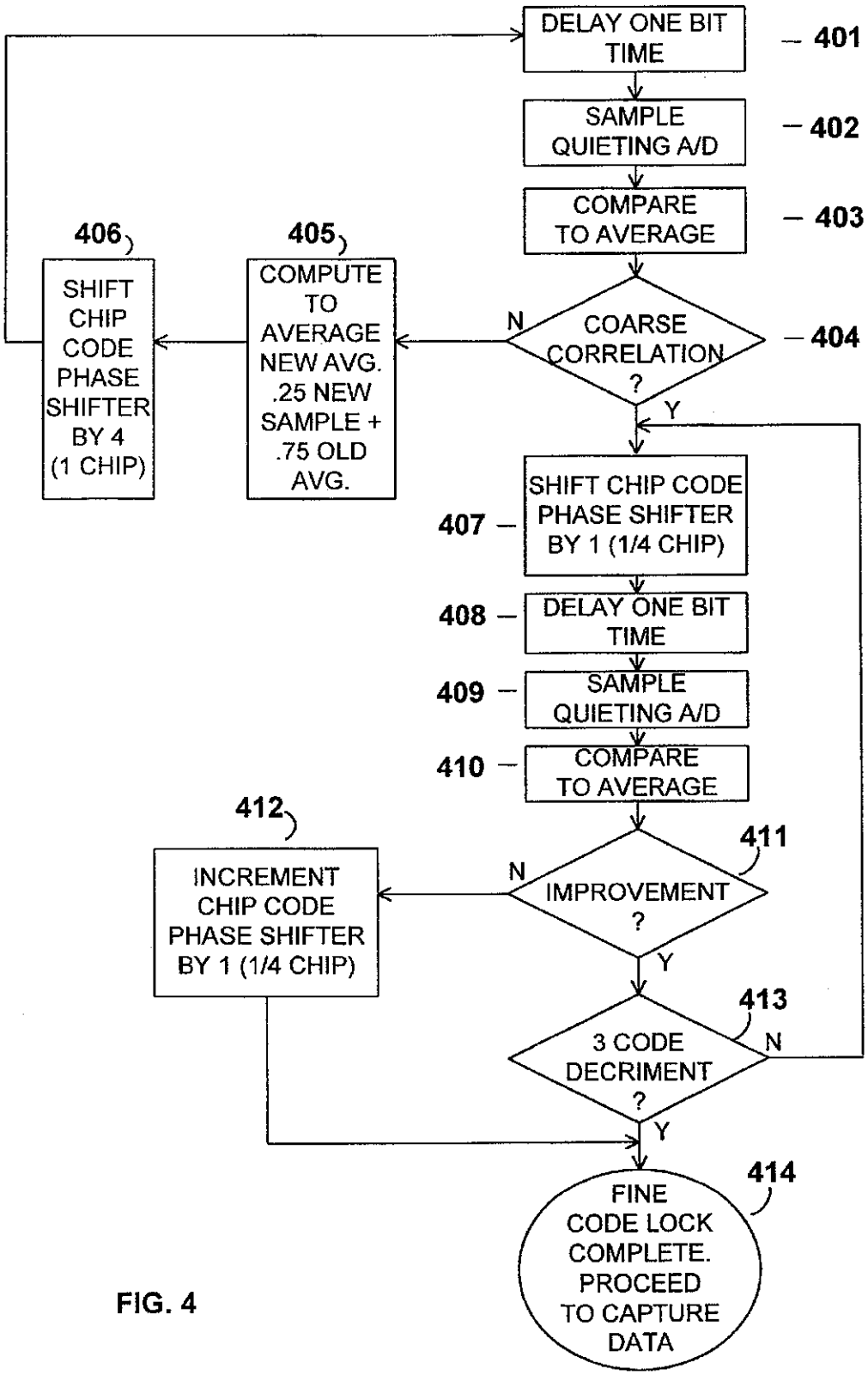
DELAY ONE BIT TIME
401
SAMPLE QUIETING A/D
402
COMPARE TO AVERAGE
403
406
405
SHIFT CHIP CODE PHASE SHIFTER BY 4 (1 CHIP)
COMPUTE TO AVERAGE NEW AVG. .25 NEW SAMPLE + .75 OLD AVG.
N
COARSE CORRELATION ?
404
Y
SHIFT CHIP CODE PHASE SHIFTER BY 1 (1/4 CHIP)
407
DELAY ONE BIT TIME
408
SAMPLE QUIETING A/D
409
COMPARE TO AVERAGE
410
412
411
INCREMENT CHIP CODE PHASE SHIFTER BY 1 (1/4 CHIP)
N
IMPROVEMENT ?
Y
413
3 CODE DECRIMENT ?
N
Y
414
FINE CODE LOCK COMPLETE. PROCEED TO CAPTURE DATA

FIG. 4

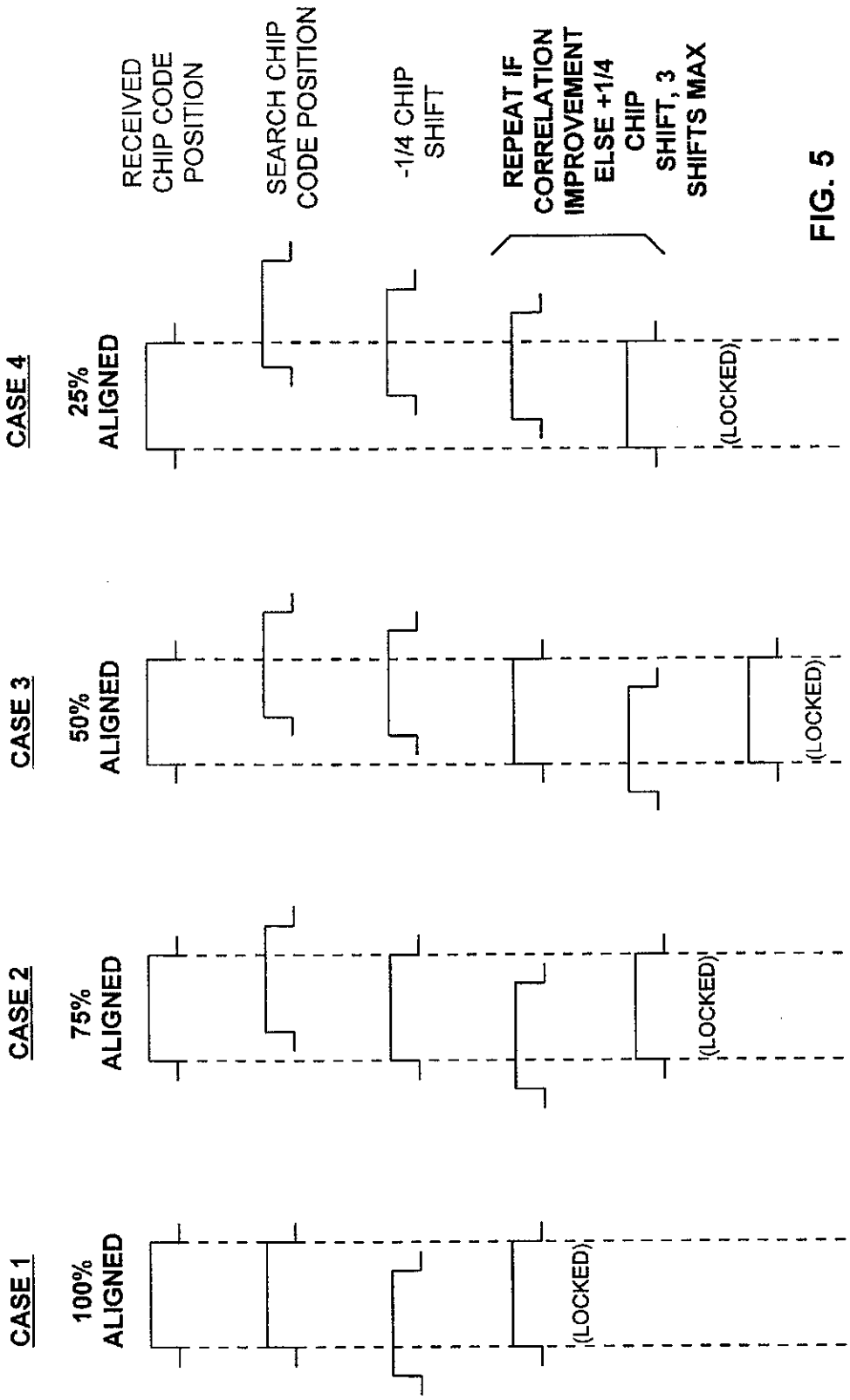
RECEIVED CHIP CODE POSITION
SEARCH CHIP CODE POSITION
-1/4 CHIP SHIFT
REPEAT IF CORRELATION IMPROVEMENT ELSE +1/4 CHIP SHIFT, 3 SHIFTS MAX
CASE 4
25% ALIGNED
(LOCKED)
CASE 3
50% ALIGNED
(LOCKED)
CASE 2
75% ALIGNED
(LOCKED)
CASE 1
100% ALIGNED
(LOCKED)

FIG. 5

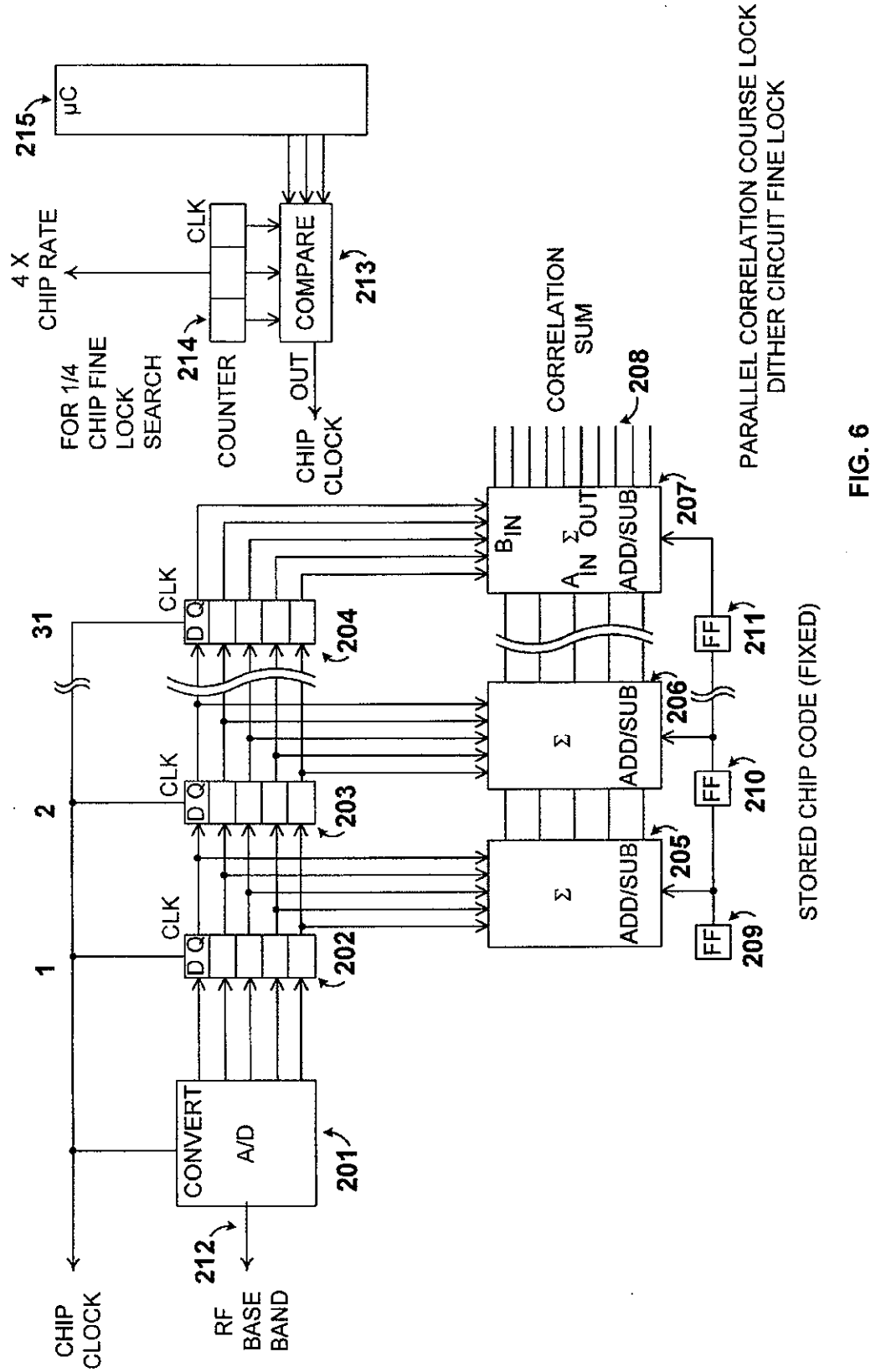
μC
215
4 X CHIP RATE
FOR 1/4 CHIP FINE LOCK SEARCH
CLK
COUNTER
214
COMPARE
213
OUT
CHIP CLOCK
CORRELATION SUM
208
PARALLEL CORRELATION COURSE LOCK DITHER CIRCUIT FINE LOCK
B IN
A IN
Σ OUT
ADD/SUB
207
FF
211
206
210
205
209
STORED CHIP CODE (FIXED)
CLK
D Q
204
203
202
31
2
1
CONVERT
A/D
201
212
RF BASE BAND
CHIP CLOCK

FIG. 6

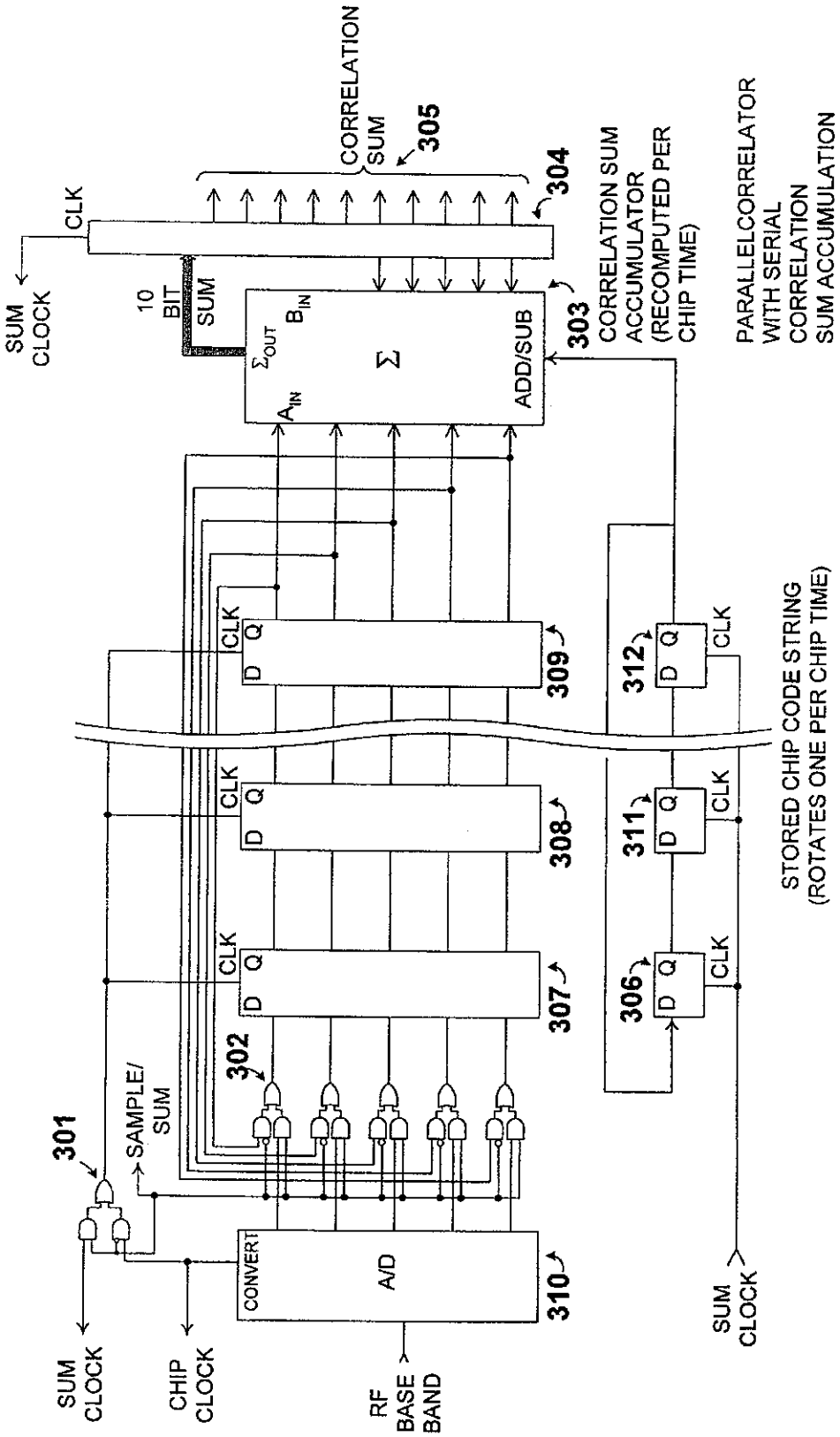
CORRELATION SUM
305
304
CLK
SUM CLOCK
10 BIT SUM
303
CORRELATION SUM ACCUMULATOR (RECOMPUTED PER CHIP TIME)
PARALLELCORRELATOR WITH SERIAL CORRELATION SUM ACCUMULATION
$B_{IN}$
$\Sigma_{OUT}$
$\Sigma$
$A_{IN}$
ADD/SUB
CLK
D Q
309
312
308
311
307
306
302
SAMPLE/ SUM
301
CONVERT
A/D
310
SUM CLOCK
CHIP CLOCK
RF BASE BAND
STORED CHIP CODE STRING (ROTATES ONE PER CHIP TIME)
SUM CLOCK

FIG. 7

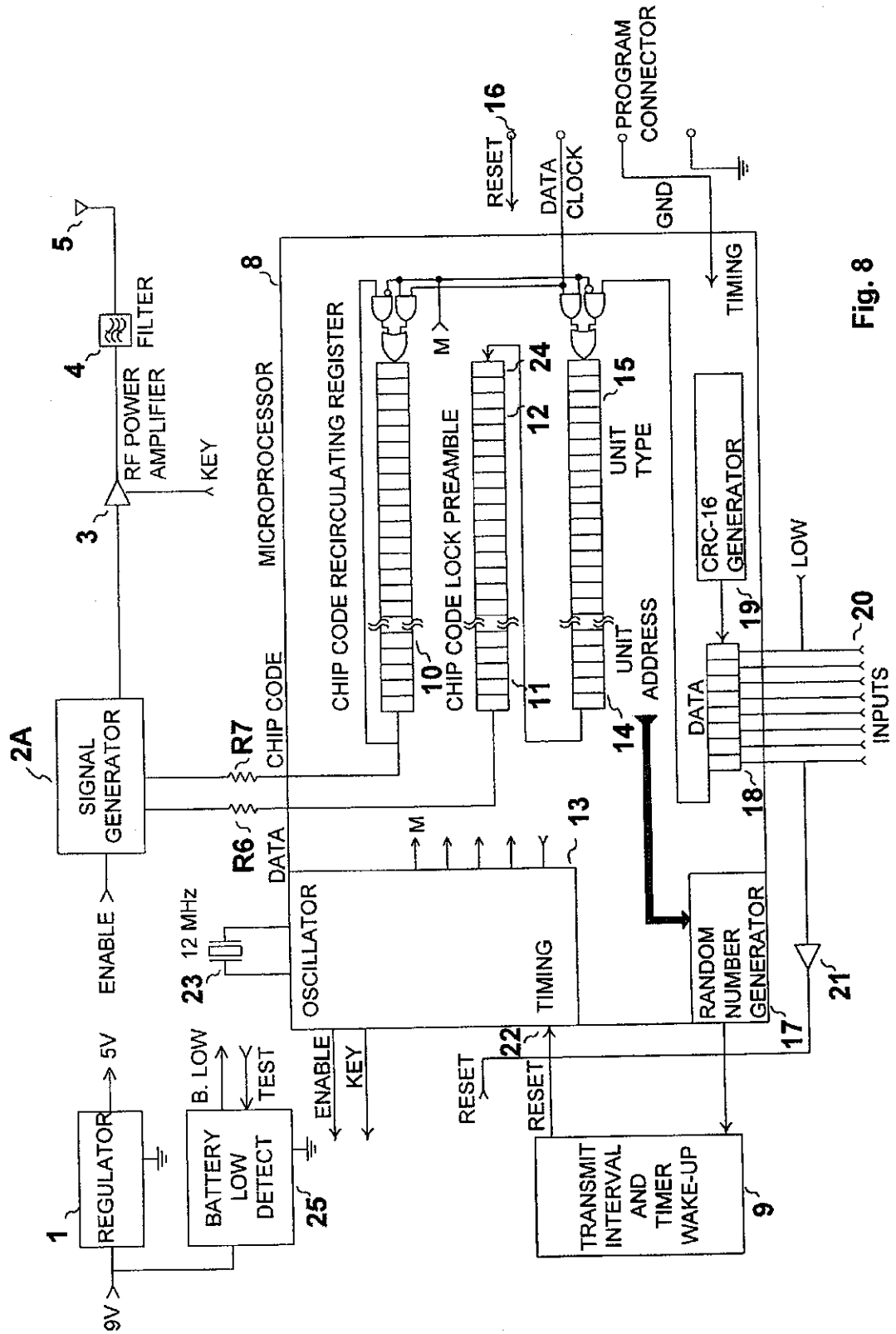
RESET
16
DATA
CLOCK
PROGRAM CONNECTOR
GND
TIMING
5
4
FILTER
RF POWER AMPLIFIER
KEY
3
8
MICROPROCESSOR
CHIP CODE RECIRCULATING REGISTER
M
24
12
15
UNIT TYPE
CRC-16 GENERATOR
LOW
10
CHIP CODE LOCK PREAMBLE
11
UNIT ADDRESS
19
20
2A
SIGNAL GENERATOR
R7
CHIP CODE
14
DATA
INPUTS
R6
DATA
13
18
M
ENABLE
23
12 MHz
OSCILLATOR
TIMING
RANDOM NUMBER GENERATOR
21
17
5V
B. LOW
TEST
ENABLE
KEY
22
RESET
RESET
1
REGULATOR
BATTERY LOW DETECT
25
TRANSMIT INTERVAL AND TIMER WAKE-UP
9
9V

Fig. 8

# WIRELESS ALARM SYSTEM

## CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation of application Ser. No. 07/782,345 (filed Oct. 24, 1991) revived, now U.S. Pat. No. 5,598,427, which is a divisional of Ser. No. 07/569,682 (filed Aug. 8, 1990), now U.S. Pat. No. 5,095,493, which is a divisional of Ser. No. 07/266,461 (filed Nov. 2, 1988), now U.S. Pat. No. 4,977,577.

## BACKGROUND OF THE INVENTION

This invention relates to a wireless warning system for use in a large office building, and more particularly a wireless fire warning and detection system which employs spread spectrum technology with high reliability for continuously monitoring the building.

## DESCRIPTION OF THE PRIOR ART

A number of systems and techniques have been employed in the prior art as a warning system for large buildings. These include having warning sensors for detecting fire, security, or other means wired directly to a main console, with indicators that a particular sensor has been activated. Systems also have been developed employing a radio link between the sensor and a receiver. For example, U.S. Pat. No. 4,550,312 to Galloway et al. teaches the use of wide-band sensors and transmitters. The sensors/transmitters transmit digital information to a central station by radio. These transmissions of messages are proceeded by an additional access code to identify a particular property. This increases the message overhead, however, which lowers system throughput and lowers battery life.

U.S. Pat. No. 4,661,804 to Abel discloses a receiver-decoder used with a plurality of encode or transmitter units using digitally encoded addresses. This use of multiple redundant 35 second interval short transmissions is used to achieve reliable throughput.

U.S. Pat. No. 4,734,680 to Gehman et al. teaches the use of a pseudorandom number to lower probability of repeat data collisions. The Gehman invention provides for only four bits or sixteen time slot positions over which to transmit, which are inadequate for large systems with hundreds of transmitters. The Gehman disclosure does not teach the use of a randomization interval with hundreds of possible of time slots with spread spectrum so that a destructive data collision can only occur in one chip time. Further, the Gehman patent does not teach the use of the transmitters unique address as a seed to the pseudorandom number generator, preventing two transmitters from drifting into lockstep transmitting schedule.

## OBJECTS AND SUMMARY OF THE INVENTION

An object of the present invention is to provide a wireless warning system having a high reliability for transmitting digital data via radio waves from an alarm or data transmission device to a remotely located receiver.

Another object of the invention is to provide a wireless warning system capable of data error detection and error correction using redundancy, for increasing communications reliability.

A further object of the invention is to provide a wireless warning system having a safety margin against jamming and undesirable interference.



According to the present invention, as embodied and broadly described herein, a wireless warning system is provided comprising a plurality of sensors coupled to a plurality of spread spectrum transmitters, respectively. The plurality of sensors are for detecting or warning against smoke, heat, unauthorized entry, or other sensing device to indicate some particular function in a room of a building. The system further includes at least one spread spectrum receiver having polar diversity antennas and microprocessor having a display, with the microprocessor coupled to the spread spectrum receivers.

An apparatus coupled to a modulation input of an oscillator of a spread spectrum transmitter is provided for controlling the spread spectrum transmitter, which includes chip-code-generation means, preamble means, address means, and data means. The chip-code-generation means can be embodied as a recirculating register, the preamble means can be embodied as a preamble register, the address means can be embodied as an address register, and the data means can be embodied as a data register. The recirculating register is coupled to the modulation input of the oscillator for storing the spread-spectrum code. The recirculating register also outputs the spread spectrum chip code as a modulating voltage to the modulation input of the oscillator. The preamble register is coupled to the modulation input of the voltage controlled oscillator. The preamble register stores a preamble, and outputs, during a transmitting interval, the preamble as a modulating voltage to the modulation input of the voltage controlled oscillator. The preamble may include a coarse lock preamble and a fine lock preamble.

The address register is coupled to the modulation input of the voltage controlled oscillator through the preamble register. The address register stores a device address and a type code, and outputs, during a transmitting interval, the device address and the type code as a modulating voltage to the modulation input of the voltage controlled oscillator.

The data register is coupled to the data input and to the modulation input of the voltage controlled oscillator through the preamble register and the address register. The data register stores data received from the data input, and outputs, during the transmitting interval, the data as a modulating voltage to the modulation input of the voltage controlled oscillator.

The present invention further includes a error detection means coupled to the data register for putting a redundancy check code word at the end of a data sequence, for error detection.

A timing circuit is provided coupled to the enable input of the voltage oscillator for enabling the voltage controlled oscillator during the transmitting interval. The timing circuit also is coupled to the keying input of the RF power amplifier for enabling an RF power amplifier during the transmitting interval. Additionally, a pseudorandom sequence generator is coupled to the timing circuit or generating a random number for modifying the timing duration between each transmitting interval.

The present invention also includes an apparatus for generating spread spectrum chip code for use with a receiver, including means for entering the spread spectrum chip code having n single chips. The entering means may be embodied as a hand terminal. The apparatus further includes memory means for storing chip words, each chip word having a plurality of bits. The memory means may include a random access memory (RAM) or other memory device. Also included is a processing means coupled to the entering

means and to the memory means, and responsive to receiving the spread spectrum chip code for transforming a single chip of the spread spectrum chip code to a chip word and storing the chip word in memory means. The processing means may be, for example, a microprocessor or other electronic circuit device to accomplish these functions. Additionally, counting means are included coupled to the memory means for sequencing through n addresses of the chip words stored in the memory means, and sequentially outputting the chip words to the receiver.

The present invention further includes an apparatus for synchronizing spread spectrum chip code using a two step algorithm in a process coupled to a receiver having a quieting output. The apparatus includes means for correlating a first signal from the quieting output of the receiver with multiple code iterations of the spread spectrum chip code by comparing the first signal to an adaptive average to be exceeded by a preset margin. The means for correlating includes determining whether the amplitude of the first signal exceeds the preset margin. Included are means coupled to the correlating means for computing the adaptive average, in response to the first signal not exceeding the preset margin. The computing means adds the amplitude of the first signal to the previously computed adaptive average. Means coupled to the quieting output of the receiver is provided for correlating a second signal in response to the first signal exceeding the preset margin. The second signal is orrelated with a portion the time duration of multiple code iterations of the spread spectrum signal. The means for correlating the second signal compares the amplitude of the second signal to an adaptive average by a preset margin to determine whether the second signal exceeds the preset margin.

A second species of the spread spectrum chip code synchronization method and apparatus, according to the present invention, is provided. The second species includes the spread spectrum chip code synchronization apparatus coupled to a baseband output of a receiver. The apparatus includes means coupled to the baseband output of the receiver for sampling and digitizing a plurality of analog signals from the baseband output of the receiver, for generating a plurality of data signals. Each of the analog baseband signals is sampled and digitized during one chip time. Register means are provided, coupled to the sampling and digitizing means, for shifting the plurality of data signals sequentially through a plurality of shift registers. Means is provided coupled to the register means for adding in parallel each of the plurality of data signals stored in the plurality of registers according to a plurality of predetermined weights for each of the plurality of data signals. The adding means generates a correlation sum.

Comparing means coupled to the adding means compares the correlation sum to a preset margin. Means coupled to the comparing means dithers a chip clock by at least one portion of one chip time, thereby improving clock lock.

A third species of the spread spectrum chip code synchronization apparatus is provided according to the present invention. The apparatus comprises means coupled to the baseband output of the receiver for sampling and digitizing a plurality of analog signals from the baseband output of the receiver. The sampling and digitizing means also generates a plurality of data signals. Each of the analog signals is sampled and digitized during one chip time.

Register means also is provided in the third species of the spread spectrum chip code synchronization apparatus, according to the present invention, coupled to the sampling and digitizing means for shifting and recirculating the plurality of data signals sequentially through a plurality of shift registers. Means additionally is provided coupled to the register means for adding sequentially the data signals passing through one of the shift registers according to a predetermined weighting algorithm.

Additional objects and advantages of the inventions will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention.

## BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate a preferred embodiment of the invention, and together with the description, serve to explain the principles of the invention.

FIG. **1** is a block diagrammatic view of the wireless sensor and detector system according to the present invention;

FIG. **2A** is a schematic diagram of a spread spectrum transmitter;

FIG. **2B** is a schematic diagram of a spread spectrum transmitter including a frequency locked loop;

FIG. **2C** is a schematic diagram of a spread spectrum transmitter including an LC tuned oscillator and phase shift keyed modulator.

FIG. **3A** is a block diagram of a spread spectrum receiver;

FIG. **3B** is a schematic diagram of a spread spectrum chip code microprocessor of the receiver;

FIG. **4** is a flow chart of the code locking algorithm;

FIG. **5** is a timing diagram of the spread spectrum chip positions;

FIG. **6** is a schematic diagram of a parallel correlator coarse lock dither circuit for proving a fine lock; and

FIG. **7** is a schematic diagram of a parallel correlator with a serial correlation sum accumulation.

FIG. **8** is a schematic diagram of an alternate configuration of a spread spectrum diagram transmitter.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings.

### Wireless Warning Detection System

FIG. **1** illustrates the wireless warning system of the present invention. A plurality of sensors **S1, S2, . . . , SN**, are coupled to a plurality of spread spectrum transmitters **X1, X2, . . . , XN**, respectively. Also shown are the elements of a base station including a first spread spectrum receiver **502** and a second spread spectrum receiver **504**, each of which are coupled to polar diversity antennas **507, 509**, respectively. A microprocessor **506** having a microprocessor display is coupled to the first spread spectrum receiver **502** and the second spread spectrum receiver **504**. The wireless warning detection system of FIG. **1** provides a high reliability for transmitting digital data via radio waves from a sensor **S1, S2, . . . , SN**. The sensor **S1, S2, . . . , SN** may be, for example, a smoke head detector, a security sensing device, or other initiating device or modulating device. As set forth below, the high reliability of the system includes means for data error detection and error correction.

The preferred embodiment consists of many sensor devices **S1, S2, . . . , SN** which may be a smoke detector, pull

station, contact alarm, waterflow detector, guard station, or security access controller. These can be expanded directly to include voice modulation, local area network data link, long-range alarm monitoring, remote power meter reading, remote process control, etc.

The initiating device provides either a contact input or reflected light smoke chamber level or data byte to the spread spectrum transmitters X1, X2, . . . , XN. The spread spectrum transmitters X1, X2, . . , XN include means for data message encoding in serial form and data integrity validation, means for re-sending the message to achieve redundancy, means for randomizing the message transmit interval to avoid repeat collisions, means for modulating the serial message into spread spectrum form and means for transmitting the spread spectrum carrier at the desired frequency.

The spread spectrum receiver's antennas **507, 509** minimize signal fading via polar diversity. Using two receivers provides redundancy as a primary and secondary means for receiving transmissions. The two polar diversity antennas provide spatial diversity against signal fading. The spread spectrum receivers **502, 504** collect the RF energy from polar diversity antenna **507, 509** and filters out undesirable frequencies. The receivers compare and synchronize desirable frequencies to the spread spectrum code of interest thereby extracting the original serial transmission. The spread spectrum receivers **502, 504** further validate the serial transmitter message and forward this information to computer **506** for display.

The spread spectrum of the present invention, in a preferred embodiment, uses fast frequency shift keying (FFSK). The techniques disclosed below are equally applicable for frequency hopping or phase shift keyed spread spectrum methods.

Transmitter

Referring to FIG. **2A**, a preferred embodiment of the transmitter of the instant invention is shown including chip-code-generation means, preamble means, address means, data means, timing means, pseudorandom-sequence means, and error-detection means. The chip-code-generation means may be embodied as a recirculating register **10** and the preamble means may be embodied as a preamble register **11**. The chip-code-generation means may be embodied as a shift register with exclusive ORed feedback taps. The address means may be embodied as an address register **14**, the data means may be embodied as a data register **18**, and the error-detection means may be embodied as cyclical-redundancy-check (CRC) generator **19**. The timing means may be embodied as timing circuit **13**, and the pseudorandom sequence means may be embodied as the random number generator **17**.

In the exemplary arrangement shown, a microprocessor **8** includes the recirculating register **10**, preamble register **11**, address register **14**, data register **18**, CRC generator **19**, random number generator **17**, and timing circuit **13**. The timing circuit **13** is embodied as a timing algorithm in software, located in microprocessor **8**. Alternatively, these registers and circuits may be put together with discrete components or independently wired and constructed as separate elements, as is well known in the art.

As shown in FIG. **2A**, an oscillator, which is shown as a voltage controlled oscillator **2** is coupled to an RF power amplifier **3**, and the RF power amplifier **3** is coupled through a bandpass filter **4** to a micropatch or equivalent antenna **5**. The voltage controlled oscillator **2** includes an enable input and a modulation input, where the voltage controlled oscillator generates a spread spectrum signal in response to a modulating voltage being applied to the modulation input. The voltage controlled oscillator **2** is enabled by applying an enable signal to the enable input. The RF power amplifier **3** has a keying input and will amplify a signal from the voltage controlled oscillator **2** only if a keying signal is applied to the keying input. The voltage controlled oscillator **2** alternatively can be frequency locked to the microprocessor's crystal to improve stability. As shown in FIG. **8**, the voltage controlled oscillator **2** also can be replaced by a capacitor and inductor tuned oscillator and a phase shift keyed modulator, or any other means for generating a signal **2A**.

The microprocessor **8** is coupled to the modulation input of the voltage controlled oscillator **2** through first resistor **R6** and second resistor **R7**. The microprocessor **8** broadly controls the voltage controlled oscillator **2** by supplying an enable signal to the enable input of the voltage controlled oscillator **2**, and a modulating voltage to the modulation input of the voltage controlled oscillator **2**. Also, the microprocessor **8** controls the RF power amplifier **3** by supplying a keying signal to the keying input of the RP power amplifier **3**.

Included in the microprocessor **8** is a recirculating register **10** coupled to the modulation input of the voltage controlled oscillator **2** through second resistor **R7**. The recirculating register **10** stores a spread spectrum chip code, and outputs, during a transmitting interval, the spread spectrum chip code as a modulating voltage to the modulation input of voltage controlled oscillator **2**, thereby enabling the voltage controlled oscillator **2** to produce a spread spectrum frequency shift keying (FSK) modulated signal as shown in FIG. **2A**. The configuration thus described is equally applicable to produce a phase shift keying (PSK) spread spectrum modulated signal as explained above by substituting a phase shift keying-modulator and tuned oscillator as shown in FIG. **8**.

The preamble register **11** is coupled to the modulation input of the voltage controlled oscillator **2** through first resistor **R6**. The preamble includes the coarse lock preamble and the fine lock preamble. The preamble register **11** stores a coarse lock preamble in cells **12** and a fine lock preamble in cells **24**. The preamble register **11** outputs during the transmitting interval, the coarse lock preamble and the fine lock preamble as a modulating voltage to the modulation input of the voltage controlled oscillator **2** through first resistor **R6**. First resistor **R6** and second resistor **R7** are chosen such that the desired spreading from the chip code and the data coming from the preamble register **11** is achieved.

Also shown in FIG. **2A** is an address register **14** coupled to the modulation input of the voltage controlled oscillator **2** through the preamble register **11** and first resistor **R6**. The address register **14** stores a device address and a type code, and outputs during a transmitting interval, the device address and type code as a modulating voltage to the modulation input of the voltage controlled oscillator **2**.

A data register **18** is coupled to a data input **20** and to the modulation input of the voltage controlled oscillator **2** through the preamble register **14** and the address register **11**. The data register **18** stores data received from the data input, and outputs, during the transmitting interval, the data as a modulating voltage to the modulation input of the voltage controlled oscillator **2**. The data from the preamble register **11**, address register **14**, and data register **18** are outputted in sequence, and at the end of a sequence, the cyclical redundancy check generator **19** outputs a data word at the end of the code for error detection.

A timing circuit **13** is included in microprocessor **8**, and is coupled to the enable input of the voltage controlled oscillator **2** and to the keying input of the RF power amplifier **3** for enabling the voltage controlled oscillator **2** and the RF power amplifier **3**, by outputting an enable signal to the enable input of the voltage controlled oscillator **2** and a keying signal to the keying input of the RF power amplifier **3**, respectively, during.the transmitting interval. In essence, voltage controlled oscillator **2** and RF power amplifier **3** are not active or activated during a time duration of non-transmission, and are only activate during a transmission interval. The time duration between transmission intervals is made to vary in response to the random number generator **17** generating a random number and transferring the random number to the timing circuit **13**. The random number modifies the timing duration between each transmitting interval randomly.

Also shown are the voltage supply, regulator circuit **1**, and battery low detector **25**.

The spread spectrum transmitter monitors one or more data inputs **20** and transmits periodically a supervisory data message. One or more of the data inputs **20** can be set **21** such that they cause a priority transmission at an increased rate higher than the supervisory message rate.

During installation of the transmitter, a device address (1-4095) **12**, "Type" code **15** (fire, security, panic, heat, pull station, etc.) stored in preamble register **11**, and a spread spectrum chip code stored in recirculating register **10** are loaded via programming connector **16**. At installation time the "Panel" computer assigns the device ID address to each room number or unique device in the system which is to be monitored. The panel computer then prints a sticky label with the device's ID, address, type code and spread spectrum chip code, both in decimal and bar code form. The label is fixed to the smoke detector or alarming device and via the programming connector **16**, or the number can be entered manually with the aid of a hand-held terminal. Alternatively a bar code reader can be connected to the programming connector **16** and the device can be read electronically from the bar code and entered into the transmitter. Microprocessor timing is controlled by crystal **23**. Transmit timing is controlled by the wake-up timer **9**, which has its own low power oscillator.

In operation, the transmitter sends a supervisory message often enough so that the receiver can detect failure of any transmitter within 200 seconds. The microprocessor **8** effectively "sleeps" between these transmissions to conserve battery life while counter **9** counts down to wake-up microprocessor **8**. In order to minimize the chance of reoccurring data collisions from multiple simultaneous transmitters, the transmit interval is modified by random number generator **17**. Very fine resolution intervals are used equal to 500 temporal transmit positions. The random number generator **17** is seeded with the transmitter's unique address **14**, resulting in different transmit schedules for each unit, thereby avoiding continuous collisions between transmitters.

Once the microprocessor **8** is reset by the wake-up circuit **9** the timing circuit **13** allows the crystal **23** to stabilize for 1–5 ms. The timing circuit **13** then enables the transmitter oscillator **2** and allows it to stabilize for 1 ms. The timing circuit **13** subsequently enables the RP amplifier **3** by sending a keying signal to the keying input. The RF energy from the RF amplifier **3** is filtered by bandpass filter **4** to reduce spurious RF emissions. The filtered signal is passed to a PCB foil micropatch 2 dBi gain antenna **5** which radiates the RF energy to an appropriate receiver. When the timing circuit **13** keys the RF power amplifier **3** it also begins to recirculate the spread spectrum **31** chip code stored in recirculating register **10** at a chip rate of 1 to 1.3 MHz. The chip code in turn causes a voltage swing 0–5 volts at the modulation input of the oscillator **2**. The voltage swing in conjunction with a modulation setting second resistor R7 creates a proportional current which modulates voltage controlled oscillator **2** thereby generating a spread spectrum FSK signal. This improves the signal to noise ratio at the receiver by reducing required bandwidth and minimizes the chances for intersecting interference. The data is super imposed on the chip code by the resistor **R6** as a $\frac{1}{31}$ deviation of the total modulation. Two or three adjacent chip code sequences are used to equal one bit time resulting in a baud rate of 14–21 KB/s.

In order for a receiver to demodulate a spread spectrum chip code, it must time lock onto the spread spectrum chip code. Disclosed are three methods of this timing acquisition, one is serial and two are parallel assisted. All methods require some synchronization bits in the transmitted message specifically allocated to code timing acquisition, which allow the receiver to search the code and find a correlation peak. The serial correlator searches one bit time per chip in the code sequence to achieve a ±½ chip code lock. This search can be hastened by searching one code sequence time instead of one bit time thereby providing a two or three to one speed increase. The parallel correlator searches all **31** chip sequences in parallel so that an initial ±½ chip synchronization ("lock") can be achieved in one bit or one chip code sequence time. "Fine" code lock (±¼ chip) for either serial or parallel assisted schemes must be followed by transmitted bit times allocated to allowing the receiver to achieve a higher resolution correlation "time" lock. One quarter chip lock accuracies perform to within 1.25 dB of optimal code alignment. The receiver's fine code lock algorithm seeks to optimize the correlation peak. Higher levels of code lock can be achieved by searching in smaller fractions of a chip. This can facilitate "time of flight" distance or location measurement applications such that 25 ns, 25 feet, of measurement resolution can be achieved.

The transmitter's microprocessor **8** stores a synchronizing preamble in preamble register **11** of 36 bits for a serial correlator, which are broken into 31 bits for coarse lock **11** and 5 bits for fine lock **12**. For the two parallel correlation methods disclosed 6 bits are used in the synchronizing preamble, 1 bit for coarse lock and 5 bits for fine lock. The actual code locking bits are transmitted as alternating ones and zeros so that the receiver's data demodulator can adaptively choose an optimal 1/0 voltage level decision point. The preamble is followed by a single data message synchronization bit **24** then 12 ID address bits **14** and 3 unit type bits **15** from address register **11**, then 8 bits of input data from data register **18** and lastly 16 bits of CRC-16 data integrity check **19**. The CRC-16 generator **19** is based on the entire proceeding message.

Once the message is transmitted, the timing circuit **13** turns off the enable signal at the enable input to voltage controlled oscillator **2** and the keying input of RF power amplifier **3**, regenerates a new random number from random number generator **17**, presets that number into the transmit interval wake-up circuit **9** and then sets the microprocessor **8** into the sleep mode. Battery voltage regulation is provided by a micropower regulator **1**. Battery voltage is pulse tested to conserve battery life **25**.

The CRC-16 generator can have its kernel seeded with an identification number unique to each facility. For example,

the kernel can be set by the facility address. Any facility having a transmission system which uses such a unique code as the kernel for the CRC-16 generator can be separated from adjacent facilities without additional transmission time or message bits.

FIGS. 2B and 2C illustrate components similar to FIG. 2A but include the addition of a frequency locked Loop **28** for frequency locking in FIG. 2B, and LC tuned oscillator **21C** (or equivalent) and a phase shift keyed modulator **22C** for creating and modulating a signal in FIG. 2C.

Receiver

The spread spectrum receiver comprises several major blocks:

A. The RF section which converts the received signal to lower frequencies;

B. Chip code generator with means of chip code phase shifting for correlation lock;

C. Means to measure both signal strength and quieting to detect correlation lock over the dynamic range of the system;

D. An adaptive data demodulator tolerant to DC i.e.: long strings of 1's or 0's; and

E. microprocessor algorithms to perform the above.

FIG. 3A shows the RF portion of the receiver which converts the received signal to lower frequencies. FIG. 3B shows a chip code generator with means for shifting a chip code phase for correlation lock, and means for measuring signal strength and the quieting output of the receiver to detect correlation lock over the dynamic range of the system. In FIG. 3A, a first polar diversity antenna **100** and a second polar diversity antenna **102** are shown and are physically turned so that their spatial phase relationship is 90°. Signals received from each of the first and second polar diversity antennas **100, 102** are passed through a 45° phase shifting network **104, 103**, respectively and then to a combiner **105**. The combiner **105** combines the signals received from the first and second polar diversity antennas **100, 102**. The combined signal then passes through a first bandpass filter **106**, is amplified by amplifier **107** and passed through a second bandpass filter **108**, and is mixed with the mixer **109**. Typically, a crystal **125** controls the frequency of an oscillator **126**. The signal from oscillator **126** is frequency multiplied by first, second and third frequency multipliers **128, 129, 130**. The signal is mixed at first mixer **109** with the received signal from second bandpass filter **108**. The oscillator **126** is modulated by the spread spectrum chip code through a phase shifter or n/2 frequency shifter **127**. The spread spectrum chip code is generated by the.circuit in FIG. 3B. First mixer **109** down converts the received signal to a first intermediate frequency signal. The first intermediate frequency signal is in a first intermediate frequency range, and is passed through third bandpass filter **110**, amplified by second amplifier **111** and passed through fourth bandpass filter **112**. The output signal from bandpass filter **112** is mixed with a second mixer **113** with a second oscillator signal from second oscillator **132** to a second intermediate frequency. The frequency of the second oscillator **132** is controlled by second crystal **131** and frequency multiplied by fourth frequency multiplier **133**. The second intermediate frequency signal is then passed through fifth bandpass filter **114**, amplified by third amplifier **115**, filtered by sixth bandpass filter **116**, and amplified by fourth amplifier **117**. The second intermediate signal then passes via two routes. The first route passes through seventh bandpass filter **118**, fifth amplifier **119** and quadrature detector **121**. The quadrature detector **121** is coupled to a 90° phase shift network **120**. The output of the quadrature detector **121** is the pre-data. Taps are taken from fourth and fifth amplifiers **117, 119**. Signals from these taps pass through signal strength combiner **122**, pass through eighth bandpass filter **123** and sixth amplifier **124**. The output of sixth amplifier **124** is the signal strength.

Referring to FIG. 3B, an apparatus which is embodied as a microprocessor **147** is shown for synchronizing a spread spectrum chip code using a two step algorithm in a microprocessor coupled to the pre-data output of the receiver. The signal from the pre-data output of the receiver passes through circuitry for generating a quieting output of the receiver.

The signal from circuitry coupled to the pre-data output, for generating the quieting output, includes amplifier **135**, ninth bandpass filter **140**, signal compressor **141**, quadrature detector filter **142** to produce the quieting output from seventh amplifier **143**. The output of seventh amplifier **143** is the quieting output, and passes to the microprocessor **147** through analog to digital converter **150**. The pre-data signal also passes through a filter comprising fourth and fifth resistors **138, 137** operational amplifier **139** with sixth resistor **158**, and first and second capacitors **157, 156**. This signal is fed to the microprocessor **147**.

The microprocessor **147** further includes means coupled to the correlation means for computing the adaptive average in response to the amplitude of the first data signal not exceeding the preset margin by adding the amplitude of the first data signal to the previously computed adaptive average. The microprocessor **147** comprises means coupled to the quieting output of the receiver via amplifier **143** for correlating the amplitude of a second data signal in response to the amplitude of the first data signal exceeding the preset margin. The second data signal is from the quieting output of the receiver. The first data signal is the digitized amplitude of the first signal, and the second data signal is the digitized amplitude of the second signal. When correlating the second data signal the microprocessor **147** compares multiple iterations of the spread spectrum chip code, by comparing the second data signal to the adaptive average by a preset margin to determine whether the amplitude of the second data signal exceeds the preset margin.

The microprocessor **147** synchronizes the spread spectrum chin code by comparing the first signal during one information bit to an adaptive average to determine whether coarse correlation has been achieved. In response to the first signal not achieving coarse correlation, the microprocessor **147** computes an adaptive average by adding a first portion of the first data signal to a second portion of the adaptive average. Additionally, the microprocessor **147** correlates a second signal in response to the amplitude of the first signal exceeding the adaptive average by a preset margin to within a portion of one chip of the spread spectrum chip code by comparing the amplitude of the second signal to the adaptive by a preset margin to determine whether the second signal exceeds the preset margin.

The microprocessor **147** also generates a spread spectrum chip code for use with the receiver, which is inputted through phase shifter or n/2 frequency shifter **127** to oscillator **126** of FIG. 3A. The apparatus, which includes the microprocessor **147** and related circuitry, includes means for entering a spread spectrum chip code having n chips. The entering means may be embodied as hand terminal **153**. Also, the apparatus includes memory means for storing chip words, which may be embodied as random access memory

146. The random access memory 146 is coupled to the microprocessor 147. The random access memory 146 stores each chip word having a plurality of bits per chip. In a preferred embodiment, there are four bits per chip word. The apparatus further includes counting means coupled to the random access memory 146 for sequencing through n addresses of the chip words in the random access memory 146 and sequentially outputting the chip words to the receiver. The counting means may be embodied as adder 145 and timing circuit 144 with AND gate 159 for determining when to roll over when counting through n chip words. Clock divider 134 is included for controlling the microprocessor 147.

In operation, the RF energy is received by two polar diversity antennas 101 and 102 which are physically rotated 90 degrees, then phase shifted +45 degrees by the first phase shifter 103, and −45 degrees by the second phase shifter 104 and finally summed 105. This polar diversity method enhances faded area reception. The signal is bandwidth limited to 2.0 MHz by a first bandpass filter 106, amplified by first amplifier 107 and bandpass filtered by second bandpass filter 108 before being presented to the first mixer 109.

The first local oscillator generated by a crystal controlled oscillator 126 which is then phase modulated to the equivalent frequency pull of a modulation of 90° at a rate set by the chip code generator.

The chip code is initially selected by either the hand terminal 153 or by the remote serial port 155. Four chip code sets are loaded into the RAM 146 such that a single "1" is represented as "1111", this allows sub chip code searches by sequencing the two low order ram address bits. The ram memory is addressed at four times the chip rate so that ¼ chip resolution code searches can be performed. The counter 144 in conjunction with the clock input 156 sets this chip code rate. The binary counter 144 causes the RAM 146 to sequentially select and modulo repeat the entire stored chip code. The AND gate 59 determines the 31st count state ×4 to create a reset pulse and causes the counter to cycle through (31×4) modulo states. In order to rapidly jump to any chip code table position the summer 145 is used to add offset 161 selected by the microprocessor's search algorithm. The flip-flop 160 synchronizes the output of the RAM 146 to the chip code clock 156 to avoid variable propagation delays due to the counters and adders.

Once the chip code has modulated the oscillator 126, the combined signal is multiplied by 128, 129, and 130 to provide a signal from the first local oscillator to frequency mixer 109. This mixing stage 109 provides several features including lowering the frequency to 160 MHz, narrowing the bandwidth to 125 kHz, and when the microprocessor locks the code sequence, the mixer 109 despreads the original transmitted data signal.

The first mixer 109 output is bandpass filtered by third bandpass filter 110, amplified by second amplifier 111 and bandpass filtered by fourth bandpass filter 112. The first intermediate frequency signal is mixed by second mixer 13 with a signal from the second local oscillator. The second local oscillator signal originates from second oscillator 132 and is controlled by crystal 131. The resulting sine wave is frequency multiplied by fourth frequency multiplier 133 before being mixed at second mixer 113. The signal resulting from the second mixer 113 is lowered in frequency to 10.7 MHz and is bandpass filtered by fifth bandpass filter 114, amplified by third amplifier 115 and bandpass filtered by sixth bandpass filter 116. This signal is sent to fourth amplifier 117 with feedback bias current measured along with fifth amplifier 119 by a signal strength measurement circuit 122. The signal strength measurement is low pass filtered by first lowpass filter 123 and buffered by sixth amplifier 124 before passing to the signal strength analog multiplexer input 152.

The signal from fourth amplifier 117 is filtered by sixth bandpass filter 118 and amplified by fifth amplifier 119. This output of fifth amplifier 119 is then quadrature detected with the aid of phase shifting circuit 120. The output of the quadrature detector 121 is buffered by amplifier 135, then high pass filtered 140. The signal is compressed to a manageable 45 dB dynamic range by compressor 141. The compressed signal is passed through a quieting detector filter 142 and buffered by amplifier 143 before being inputted to the analog multiplexer input 151.

The "pre-data", buffered by amplifier 135, is also presented to an adaptive data demodulator. Varying DC levels will be present on this signal due to frequency uncertainty between the receiver and transmitters. The data 1/0 decision threshold is chosen as the average voltage of an alternating 1/0/1 . . . pattern in the synch preamble. During the preamble code lock search time, the analog switch 136 is enabled and pre charges capacitor 156 through resistor 137. This places an average voltage on capacitor 156 between a logic "1" and a logic "0". Once code lock is achieved, and the data message synchronization bit 24 is detected, the analog switch 136 is opened leaving the capacitor 156 at a stable level for the duration of the message. The buffered pre-data level is then filtered 157 with hysteresis set by resistors 158 and 138 and compared to the voltage level on capacitor 156. This results in reliable data bits provided on the output of voltage comparator 139.

### Code Locking Algorithm

The code locking algorithm seeks to determine a correlation peak by comparing the received RF signal energy to a microprocessor controlled copy of the desired chip code pattern. The code locking algorithm digitizes the quieting detectors analog output once per bit time. The software maintains an adaptive average of the quieting samples to determine the level of correlation improvement. The described algorithm code locks to within ¼ chip time or within 1.25 dB of optimum. The baseband output also can be used in place of the quieting output.

The present invention includes three methods of using a microprocessor for synchronizing the timing acquisition of a spread spectrum chip code received by the receiver. The spread spectrum signal comprises a plurality of information bits. Each information bit is spread in spectrum by a plurality of chips from a spread spectrum code. The first method, as depicted in FIG. 4, comprises the steps performed by the microprocessor of inserting 401 a delay of one information bit time before the first information bit received by the receiver, and sampling and digitizing 402 the first signal from the quieting output of the receiver to generate a first data signal. The sampling and digitizing alternatively can be taken from the baseband or signal strength output of the receiver. The first method compares 404 the amplitude of the first data signal to the adaptive average during the time of one information bit to determine whether coarse correlation has been achieved. In response to coarse correlation not being achieved, the method computes 405 the adaptive average by adding a first portion of the amplitude of the first data signal to a second portion of the previously computed adaptive average. If the coarse correlation has been

achieved, then the method shifts **407** the chip code by a third portion of one information bit time. In a preferred embodiment of the present invention, the chip time is divided into four portions, thus the shifts **407** is equivalent to delaying the chip by ¼ chip time duration.

An additional delay is inserted **408** and the method samples and digitizes **409** a second signal from the quieting output of the receiver to generate a second data signal. The amplitude of the second data signal during one information bit time is compared **410** to the adaptive average to determine whether fine correlation has been achieved. If fine correlation has been achieved, then a data capture algorithm is initiated **414**. If fine correlation has not been achieved, then the method shifts **412** the chip code phase shifter by a third portion, which is equivalent in the present preferred embodiment to a ¼ time duration of a chip. The method then proceeds to initiate the data capture algorithm.

A delay **401** is inserted before digital conversion of the quieting output **402**. This delay serves to insure re-occurring data samples equal to one information bit time. The new sample is compared to the running adaptive average **403**. If the improvement is greater than a preset margin, then coarse correlation **404** is achieved. Otherwise, if the new sample is within the noise error of the running average, the new sample is combined with the old average **405**; average=(0.25 new+0.75 old average). The chip code phase shifter **161** is incremented by a count of 4 (1 chip time). This coarse code lock algorithm is then indefinitely repeated until coarse code lock is acquired.

If coarse correlation is achieved **404**, then the algorithm seeks to "fine" code lock. The chip code phase shifter **407** is shifted by one (¼ chip time). The one information bit time synchronizing delay is passed **408**. The quieting detector output is digitized **409** and compared **410** to the running quieting output average. If the new sample did not improve **411** the quieting by the preset margin then the chip code phase shifter is incremented **412** by ¼ chip to its past more optimum position. Fine lock is completed **414** and the code lock algorithm jumps to a data capture algorithm.

If the required margin of quieting improvement is achieved **411**, then the number of chip code shifts is checked **413**. Any search code position which is shifted more than three ¼ chip steps would undesirably slip one whole code cycle. Comparison **413** stops a search on the third-code slip and assumes an optimum correlation is achieved then proceeds to the data acquisition algorithm **414**. If three code phase decrements have not occurred, the algorithm repeats at shift **407**.

FIG. **5** shows four cases with one-quarter chip code lock achieved in each case using the first method.

A second method and apparatus for synchronizing a spread spectrum chip code using the baseband signal output of the receiver is shown in FIG. **6**. The apparatus aspect of the invention includes means for sampling and digitizing a plurality of analog baseband signals, register means for shifting the plurality of data signals, means for adding in parallel the plurality of data signals, means for comparing the correlation sum and means for dithering a chip/sample clock by a portion of a chip time. The sampling and digitizing means may be embodied as analog to digital converter **201**. The register means may be embodied as the plurality of registers **202, 203, 204**. The adding means may be embodied as adders **205, 206, 207** and the comparing means may be embodied as comparator **213**. The dithering means may be embodied as the microprocessor **215**.

As illustratively shown, the apparatus for synchronizing the spread spectrum chip code has the analog to digital converter **201** coupled to the RF baseband output of the receiver **212**. The analog to digital converter **201** samples and digitizes the plurality of analog baseband signals from the baseband output of the receiver **212** and generates a plurality of data signals. The plurality of registers **202, 203, 204** is coupled to the analog to digital converter **201** and shifts the plurality of data signals sequentially through the plurality of registers **202, 203, 204**. The plurality of adders **205, 206, 207** are coupled to the plurality of registers **202, 203, 204**, respectively, for adding in parallel each of the data signals stored in the plurality of registers **202, 203, 204** according to a plurality of predetermined weights for each of the plurality of data signals, respectively, to generate a correlation sum. The weights are controlled by flip flop circuits **209, 210, 211**, which contain the spread spectrum chip code. The adder **207** outputs a correlation sum **208** to a comparator **213** for comparing the correlation sum to a predetermined margin or threshold. The dithering circuit embodies as a microprocessor **215** is coupled to the comparator **213** and dithers the chip clock by at least a first portion of one chip time, thereby improving chip lock.

In operation, the second method of using a microprocessor for synchronizing the timing acquisition of the spread spectrum chip code raceived by a receiver comprises the steps of sampling and digitizing using the analog to digital converter **201**, the plurality of analog baseband signals from the baseband output of the receiver **212**, to generate a plurality of data signals. Each of the analog baseband signals is sampled and digitized during one chip time. The method shifts the plurality of baseband signals through the plurality of shift registers **202, 203, 204**. The plurality of data signals are added in parallel according to a plurality of predetermined weights, from flip flops **209, 210, 211** for each of the plurality of data signals, respectively, in the plurality of adders **205, 206, 207** to generate a correlation sum **208**. The correlation sum **208** is compared to a predetermined threshold or preset margin, and a chip clock is then dithered by at least a first portion of one chip time to improve clock lock. In a preferred embodiment, the first portion is one quarter of one chip time.

The chip clock samples once per chip time. A coarse chip lock may therefore be incorrect by ±½ of a chip. To improve the lock, the chip clock is slewed in ±¼ and/or ±⅛ chip steps controlled by an algorithm in microprocessor **215**. A clock with a rate equal to four times the chip rate is counted by counter **214**. The counters output is compared to an output of the microprocessor **215** equal to the code phase being searched. The microprocessor **215** can thereby search in fine chip code steps after a rapid parallel assisted search in 1, 31 chip code time. The total search required is equal to 6 chip code times, which can be sent in the spread spectrum transmitters code-lock preamble as disclosed.

As a further component reduction of the circuitry described above in the second species of the method and apparatus for synchronizing a spread spectrum chip code, the parallel assisted chip code lock can be serially summed instead of parallel summed. The serial sum of all 31 stages must be computed between chip samples (less than 1,000 ns). This speed can be achieved with available high speed CMOS ASICS with clock speeds of 40 MHz or greater.

A third species of the spread spectrum chip code synchronizing method and apparatus is disclosed in the present invention, and is set forth in FIG. **7**. The third species of the spread spectrum chip code synchronizing apparatus couples to the baseband output of the receiver. The apparatus includes means coupled to the baseband output of the receiver for sampling and digitizing the plurality of analog

baseband signals, register means coupled to the sampling and digitizing means for shifting and recirculating the plurality of data signals, and means coupled to the register means for adding sequentially the data signals passing through the shift register means. As shown in FIG. **7**, the sampling and digitizing may be embodied as analog to digital converter **310**. The register means may be embodied as registers **307, 308, 309** and the adding means may be embodied as adder **303**. As shown in FIG. **7**, the analog to digital converter **310** is coupled to the baseband output of the receiver, and passes through a plurality of gates **302** to the plurality of registers **307, 308, 309**, to adder **303**. Also shown is a plurality of flip flops **306, 311, 312** having the spread spectrum chip code therein. The flip flops **306, 311, 312** input the spread spectrum chip code into the adder **303**. The adder **330** is coupled to a correlation sum accumulator **304** which outputs a correlation sum **305**.

In the preferred embodiment, the third species of the apparatus for synchronizing the spread spectrum chip code has the analog to digital converter **310** coupled to the baseband output of the receiver for sampling and digitizing a plurality of analog baseband signals and generating a plurality of data signals. Each of the analog baseband signals is sampled and digitized during one chip time. The plurality of registers **307, 308, 309** is coupled to the analog to digital converter **310** through gates **302** for shifting and racirculating the plurality of data signals sequentially through the plurality of registers **307, 308, 309** and gates **302**. The adder **303** is coupled to register **309** for adding sequentially the data signals passing through registers **309** according to predetermined weights set forth in flip flops **306, 311, 312**.

In operation, the third method of uses a microprocessor for synchronizing the timing acquisition of the spread spectrum chip code received by the receiver. The method samples and digitizes the plurality of analog baseband signals from the baseband output of the receiver using analog to digital converter **310**, to generate a plurality of data signals. Each of the analog baseband signals is sampled and digitized during one chip time. The method further includes shifting and recirculating the plurality of data signals sequentially through the plurality of registers **307, 308, 309**. The data signals are added sequentially as they pass through register **309** using adder **303** and accumulated. The correlation sum accumulator **304** then passes the correlation sum **305** to the microprocessor.

The third method is similar to the second method, except that there is only one adder **303** for the entire register chain instead of one adder per stage. The registers **307, 308, 309** are steered to recirculated by the AND/OR gates **302**. The stored chip code string can also be shifted and recirculated. After each chip clock rising stage transition, an analog data sample is converted by analog to digital converter **310** and stored in register **307**. Data in the registers are shifted to the right as in the circuit in of FIG. **6**. Immediately following the chip sample, a sequence is performed to accumulate a correlation sum. The AND/OR steering gates **301** and **302** are switched to the "sum" state. This passes a high speed summing clock of 40 MHz for 31 clock cycles to the registers **307, 308, 309** and to the stored spread spectrum chip code in **306, 311, 312**. The steering gates **302** causes data in registers **307, 308, 309** to recirculate so that after 31 clock cycles of the adding phase, the data in registers **307, 308, 309** will be in their original positions and ready to accept another spread spectrum chip code data sample and store phase. After each 40 MHz summing clock transition a new sum is generated by adder **303** and accumulated in accumulator **304**. Adder **303** is caused to either add or subtract the inputs Ain from the accumulated total. This is determined by the stored chip code string in flip-flop **312** which creates the $\times(+1)$ or $\times(-1)$ correlation weighting causing either the addition or subtraction of the Ain inputs. The outputs of accumulator **304** are transferred to the next register stage and then at the next clock rising edge, the accumulator stores that total. After 31 summing clock cycles the accumulation **304** will contain the correlation sum **305**. The multibit words stored and summed by the two alternative methods can be reduced to one bit samples and sums, resulting in a small loss of performance.

It will be apparent to those skilled in the art that various modifications can be made to the wireless detection system of the instant invention without departing from the spirit or scope of the invention, and it is intended that the present invention cover modifications and variations of the wireless detection system provided they come within the scope of the appended claims and their equivalents.

What is claimed as new and desired to be secured by Letters Patent of the United States is:

**1**. In a method for controlling a spread spectrum transmitter having an oscillator provided with a modulation input, the improvement comprising the steps of:

maintaining the transmitter in a low current state between transmissions of spread spectrum signals;

generating one or more chip code sequence repetitions during a transmitting interval when the transmitter is not maintained in the low current state;

inputting said one or more chip code sequence repetitions as a modulating voltage to the modulation input of the oscillator thereby causing a frequency deviation in a transmitted signal to be output from the transmitter; and

applying additionally a device address and data to the modulation input of the oscillator after inputting the one or more chip code sequence repetitions for a predetermined time period so as to allow an associated receiver to achieve initial spread spectrum timing synchronization.

**2**. The method of claim **1**, further comprising the step of:

applying a limited number of address and data bits to the modulation input of the oscillator so that the associated receiver, having a synchronization device therein, is able to receive the transmitted signal and decode the data in said transmitted signal after completion of a coarse search and without said synchronization device performing continuous chip code synchronization on said transmitted signal.

**3**. The method of claim **1**, further comprising:

applying the one or more chip code sequence repetitions as the modulating voltage to said modulation input of said oscillator at a chip rate of approximately 1.0 MHZ to 1.3 MHZ so as to produce a frequency shift keying (FSK) spread spectrum modulated signal.

**4**. The method of claim **3**, wherein the oscillator is modulated with fast frequency shift key (FFSK) modulation.

**5**. The method of claim **1**, wherein said applying step comprises:

applying the one or more chip code sequence repetitions to the modulation input of a phase shift keying (PSK) modulator that is included in said oscillator at a chip rate of approximately 1.0 MHZ to 1.3 MHZ to produce a PSK spread spectrum modulated signal as said transmitted signal.

**6**. The method of claim **1**, wherein at least one of the data applied to the modulation input causes a priority transmission at an increased rate of message transmission.