**IN THE UNITED STATES DISTRICT COURT**
**FOR THE NORTHERN DISTRICT OF ILLINOIS**
**EASTERN DIVISION**

OLE K. NILSSEN and GEO FOUNDATION, LTD.,

Plaintiffs,

v.

HARMONY LIGHTING, INC.

Defendants.

Civil Action No. 05C 2911

JURY TRIAL DEMANDED

FILED
MAY 16 2005
MICHAEL W. DOBBINS
CLERK, U.S. DISTRICT COURT

LAL

JUDGE ASPEN
MAGISTRATE JUDGE
GERALDINE SOAT BROWN

**COMPLAINT**

Plaintiffs, Ole K. Nilssen ("Nilssen") and Geo Foundation, Ltd. ("Geo Foundation"), by their undersigned attorneys, complain of Defendant Harmony Lighting, Inc. ("Harmony"), and allege as follows:

**A. Jurisdiction and Venue**

1. Jurisdiction arises under 28 U.S.C. §§ 1331 and 1338(a).

2. Venue is proper in this Court pursuant to 28 U.S.C. §§ 1391 and 1400(b).

**B. The Parties**

3. Plaintiff Ole K. Nilssen maintains residences in Florida and Illinois. Nilssen maintains an office in Illinois and conducts all of his business in Illinois.

4. Plaintiff Geo Foundation is a not-for-profit corporation incorporated in the Cayman Islands, British West Indies.

5. Defendant Harmony is a Massachusetts corporation with an office at 35 Pond Park Road, Unit 4, Hingham, Massachusetts 02043. Harmony sells infringing self-

ballasted compact fluorescent screw-in lamps ("SBCFL") in this district through established distribution channels.

**C. The Patents in Suit**

6. United States Patent No. 4,857,806 ("the '806 patent"), entitled "Self-Ballasted Screw-In Fluorescent Lamp," was duly and legally issued by the United States Patent and Trademark Office on August 15, 1989. A copy of the '806 patent is attached as Exhibit 1.

7. United States Patent No. 5,233,270 ("the '270 patent"), entitled "Self-Ballasted Screw-In Fluorescent Lamp," was duly and legally issued by the United States Patent and Trademark Office on August 3, 1993. A copy of the '270 patent is attached as Exhibit 2.

8. United States Patent No. 5,341,067 ("the '067 patent"), entitled "Electronic Ballast With Trapeziodal Voltage Waveform," was duly and legally issued by the United States Patent and Trademark Office on August 23, 1994. A copy of the '067 patent is attached as Exhibit 3.

9. United States Patent No. 5,343,123 ("the '123 patent"), entitled "Series-Resonant Inverter Ballast," was duly and legally issued by the United States Patent and Trademark Office on August 30, 1994. A copy of the '123 patent is attached as Exhibit 4.

10. United States Patent No. 5,510,680 ("the '680 patent"), entitled "Electronic Ballast With Special Voltage Waveforms," was duly and legally issued by the United States Patent and Trademark Office on April 23, 1996. A copy of the '680 patent is attached as Exhibit 5.

11. United States Patent No. 5,510,681 ("the '681 patent"), entitled "Operating Circuit For Gas Discharge Lamps," was duly and legally issued by the United States

Patent and Trademark Office on April 23, 1996. A copy of the '681 patent is attached as Exhibit 6.

12. United States Patent No. 6,172,464 B1 ("the '464 patent"), entitled "Compact Screw-In Fluorescent Lamp," was duly and legally issued by the United States Patent and Trademark Office on January 9, 2001. A copy of the '464 patent is attached as Exhibit 7.

13. Plaintiff Nilssen is the inventor and owner of the '806 patent, the '270 patent, the '067 patent, the '123 patent, the '680 patent, the '681 patent, and the '464 patent (collectively "the patents-in-suit").

14. Plaintiff Geo Foundation is an exclusive licensee of the patents-in-suit with the exclusive right to license others.

15. Geo Foundation has authorized Nilssen to negotiate patent license agreements on its behalf as a prospective licensor of the patents-in-suit, and Nilssen has negotiated on behalf of Geo Foundation.

**D. Background**

16. Harmony has been, and is currently, in the business of selling infringing products throughout the United States, including locations within the Northern District of Illinois through established distribution channels.

17. Hamrony's acts of selling and offering for sale infringing products through established distribution channels that terminate within the Northern District of Illinois demonstrates continual and systematic contacts by Harmony within the Northern District of Illinois.

18. In addition, Harmony's acts of selling and offering for sale infringing products within the Northern District of Illinois establishes minimum contacts as such contacts

were made for purposes of availing the Harmony of the privilege of doing business within the Northern District of Illinois.

19. Harmony's acts of selling and offering for sale infringing products within the Northern District of Illinois give rise to and are related to Plaintiffs' cause of action for patent infringement.

20. Exercising jurisdiction over Harmony in the Northern District of Illinois is consistent with traditional notions of fair play and substantial justice.

**Count I – Patent Infringement**

21. Plaintiffs re-allege paragraphs 1-20 as if fully incorporated herein.

22. Harmony's offers for sale and sales of SBCFLs infringe one or more claims of each patent-in-suit.

23. On information and belief, Harmony's has had knowledge of one or more of the patents-in-suit since sometime after their respective issuance dates and has knowingly and without justification infringed upon these patents through its sales and offers for sale of infringing SBCFLs.

24. Plaintiffs have the right to bring suit with respect to each of the patents-in-suit.

25. Harmony has in the past and continues to offer for sale and sell, infringing SBCFLs that embody the inventions claimed in the patents-in-suit and will continue to do so unless enjoined by this Court.

26. On information and belief, Harmony has in the past willfully infringed, and continues to willfully infringe, the patents-in-suit through its sale and offer for sale of infringing SBCFLs.

27. On information and belief, in the United States, purchasers of infringing SBCFLs sold by Harmony have used in the past and continue to use the infringing products in combination with other components, including power sources, thereby infringing the patents-in-suit.

28. On information and belief, each infringing SBCFLs sold by Harmony was designed to be used in connection with a power source.

29. On information and belief, Harmony knew of each of the patents-in-suit at all relevant times before selling infringing SBCFLs to said purchasers.

30. Harmony has in the past offered for sale and sold, and continues to offer for sale and selling infringing SBCFLs that constitute a material component of the patents-in-suit and which have no substantial use other than as an infringement of the patents-in-suit.

31. On information and belief, Harmony knew and intended that purchasers of infringing SBCFLs would use the infringing products in combination with other components, including power sources, so as to infringe the patents-in-suit.

32. On information and belief, Harmony has actively induced purchasers of infringing SBCFLs to use the infringing products in combination with other components, including power sources, so as to infringe each of the patents-in-suit.

WHEREFORE, Plaintiffs pray that judgment be entered against Harmony:

(a) awarding damages and prejudgment interest to plaintiff under 35 U.S.C. §284;

(b) enjoining Harmony from selling the infringing SBCFLs that embody the patented inventions;

(c) enjoining Harmony from contributorily infringing and inducing the infringement of the patented inventions with respect to infringing products;

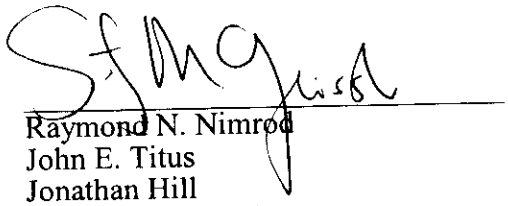
(d) increasing Plaintiffs' actual damages under 35 U.S.C. §284;

(e) awarding Plaintiffs reasonable attorney fees under 35 U.S.C. §285; and

(f) awarding such other relief as the Court deems proper.

Dated: May 16, 2005

Respectfully submitted,



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1

# United States Patent [19]

**Nilssen**

[11] **Patent Number: 4,857,806**

[45] **Date of Patent: Aug. 15, 1989**


[54] **SELF-BALLASTED SCREW-IN FLUORESCENT LAMP**


[76] Inventor: Ole K. Nilssen, Caesar Dr., Rte. 5, Barrington, Ill. 60010



[21] Appl. No.: 20,478

[22] Filed: Mar. 2, 1987

**Related U.S. Application Data**

[60] Continuation-in-part of Ser. No. 262,542, May 5, 1981, Pat. No. 4,677,345, which is a division of Ser. No. 178,107, Aug. 14, 1980, abandoned.

[51] Int. Cl.[4] ..... H01J 7/44

[52] U.S. Cl. ..... 315/72; 315/56; 315/58; 315/244; 315/DIG. 5

[58] Field of Search ..... 315/200 R, 232, 227 R, 315/242, 241 R, 243, DIG. 5, DIG. 7, 53, 209, 219, 220, 276, 278, 279, 72, 56–58; 331/113 A



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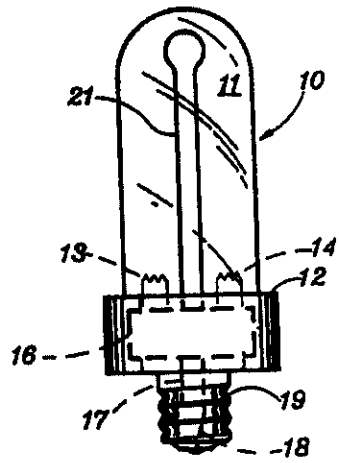
*Primary Examiner*—James J. Groody
*Assistant Examiner*—Mark R. Powell



[57] **ABSTRACT**

A fluorescent lamp is mounted on an ordinary Edison-type screw-base; which screw-base contains a frequency-converting electronic ballast. The combined lamp-ballast-assembly is adapted to be used in an ordinary screw-in lamp socket powered from ordinary 120 Volt/60 Hz power line voltage. The frequency-converting ballast within the screw-base converts the 120 Volt/60 Hz power line voltage to a high-frequency (20–30 kHz) substantially sinusoidal current, which is then used for powering the compact fluorescent lamp.


**21 Claims, 1 Drawing Sheet**



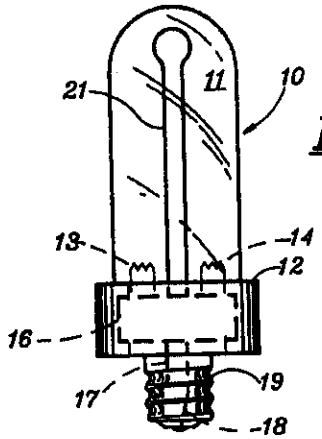



Fig. 1

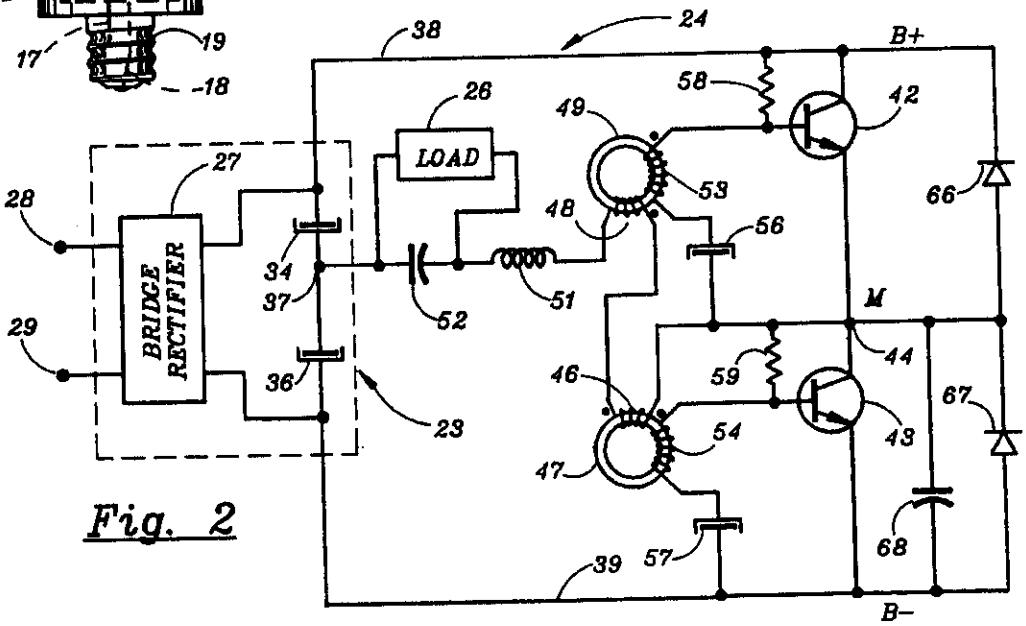



Fig. 2

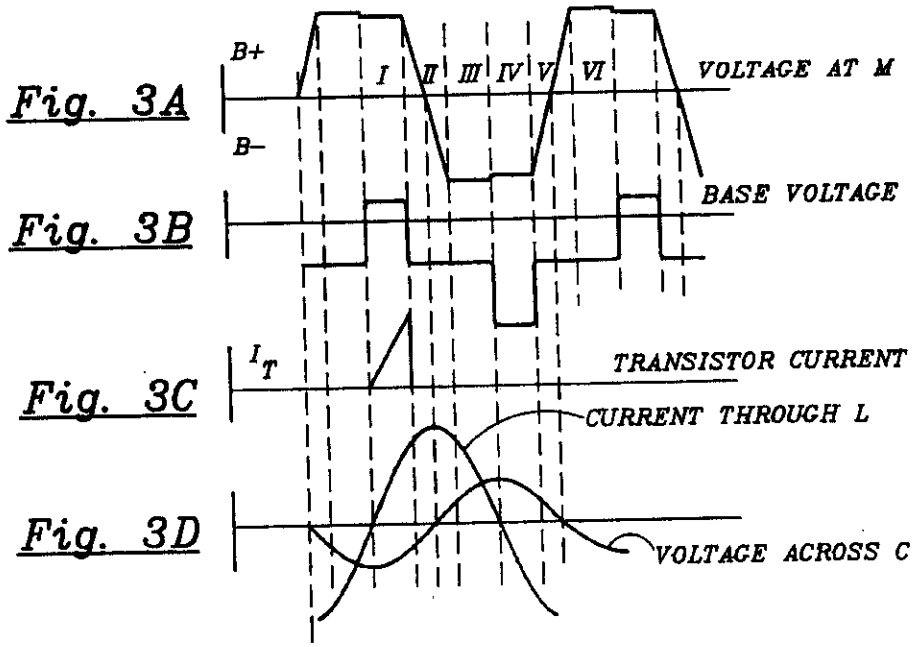



Fig. 3A

Fig. 3B

Fig. 3C

Fig. 3D

# SELF-BALLASTED SCREW-IN FLUORESCENT LAMP

## BACKGROUND OF THE INVENTION

## RELATED APPLICATION

The present application is a Continuation-in-Part of Ser. No. 262,542 filed May 5, 1981 now pat. no. 4,677,345; which is a division of Ser. No. 178,107 filed Aug. 14, 1980, now abandoned.

## FIELD OF INVENTION

The present invention relates to compact light-weight self-ballasted fluorescent lamps operable to be screwed directly into and properly powered by an ordinary Edison-type lamp socket connected with 120Volt/60Hz power line voltage.

## SUMMARY OF THE INVENTION

## OBJECT OF THE INVENTION

An object of the present invention is that of providing a compact self-ballasted screw-in fluorescent lamp assembly operable to be used in an ordinary Edison-type lamp socket.

This as well as other objects, features and advantages of the present invention will become apparent from the following description and claims.

## BRIEF DESCRIPTION

In its preferred embodiment, the present invention comprises a compact folded fluorescent lamp mounted on a base-structure adapted to be screwed into and held by an orindary Edison-type lamp socket. The base-structure comprises frequency-converting power supply means operative to be powered fromm the 120Volt/60Hz power line voltage received from the lamp socket and to provide an output to the fluorescent lamp in the form of a relatively high-frequency substantially sinusoidal current. The frequency-converting power supply supply comprises rectifier means operative to convert the 120Volt/60Hz power line voltage into a DC voltage; which DC voltage, in turn, is fed to a half-bride inverter operative to provide a high-frequency substantially squarewave voltage across a series-resonant combination of an inductor and a capacitor. The fluorescent lamp, which is of the instant-start type, is connected in parallel with the capacitor and is therefore —by way of so-called Q-multiplication —provided with adequate starting voltage and, after ignition, with a substantially constant-magnitude current.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 schematically illustrates the compact screw-in selfballasted fluorescent lamp assembly.

FIG. 2 is a schematic diagram of the frequency-converting power supply and ballasting circuit comprised within the base of the fluorescent lamp assembly.

FIG. 3 illustrates the waveforms of various voltages and current associated with the power supply and ballasting circuit of FIG. 2.

## DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 illustrates a screw-in gas discharge lamp unit 10 comprising a folded fluorescent lamp 11 secured to an integral base 12. The lamp comprises two cathodes 13, 14 which are supplied with the requisite high operating voltage from a frequency-converting power supply and ballasting circuit 16; which, because of its compact size, conveniently fits within base 12.



Circuit 16 is connected by leads 17, 18 to a screw-type plug 19 adapted for screw-in insertion into a standard Edisontype incandescent lamp socket at which ordinary 120Volt/60Hz power line voltage is available.

In FIG. 2, a power supply 23 is connected with the 120Volt/60Hz power line voltage and provides a center-tapped DC output voltage for supplying a high-efficiency half-bridge inverter circuit 24. The inverter circuit is operable to provide a high-frequency (20–30 kHz) high-magnitude current-limited voltage to a load 26, which actually represents fluorescent lamp 11 of FIG. 1.

Power supply 23 comprises bride rectifier 27 which connects with 120Volt/60Hz power line terminals 28, 29 and provides full-wave rectified power line voltage to two series-connected filter capacitors 34, 36; which filter capacitors are: i) connected together at a center-tap 37, and ii) connected between a positive B+bus 38 and a negative B- bus 39.

Inverter circuit 24 is a half-bride inverter comprising transistors 42, 43 connected in series between the B+bus and the B- bus. The collector of transistor 42 is connected to the B+bus 38, the emitter of transistor 42 and the collector of transistor 43 are connected to a midpoint line 44 ("M"), and the emitter of transistor 43 is connected to the B- bus 39.

Midpoint line 44 is connected to center-tap 37 through a primary winding 46 of a toroidal saturable core transformer 47, a primary winding 48 on an identical transformer 49, an inductor 51 and a series-connected capacitor 52. Inductor 51 and capacitor 52 are energized upon alternate transistor conduction in manner to be described later. Load 26 is connected in parallel with capacitor 52.

Drive current to the base terminals of transistors 42 and 43 is provided by secondary windings 53, 54 of transformers 49, 47, respectively. Winding 53 is also connected to midpoint line 44 through a bias capacitor 56, while winding 54 is connected to the B- bus 39 through an identical bias capacitor 57. The base terminals of transitors 42 and 43 are also connected to lines 38 and 44 through bias resistors 58 and 59, respectively. Shunt diodes 66 and 67 are connected across the collector-emitter terminals of transistors 42 and 43, respectively. Finally, a capacitor 68 is connected across the collector-emitter terminals of transistor 43 to restrain the rate of voltage rise across those terminals.

The operation of the circuit of FIG. 2 can best be understood with additional reference to FIG. 3, which illustrates significant portions of the waveforms of the voltage of midpoint M (FIG. 3A), the base-emitter voltage on transistor 42 (FIG. 3B), the current through transistor 42 (FIG. 3C), and the capacitor C voltage and the inductor 51 current (FIG. 3D).

Starting at a point where transistor 42 first starts to conduct, current flows from the B+bus 38 through windings 46 and 48 and inductor 51 to charge capacitor 52 and returns to the B+ bus through capacitor 34 (refer to the time period designated I in FIG. 3). When the saturable transformer 49 saturates at the end of period I, drive current to the base of transistor 42 will terminate, causing voltage on the base of the transistor to drop to the negative voltage stored on bias capacitor 56 in a manner to be described, causing this transistor to

become non-conductive. As shown in FIG. 3c, current-flow in transistor 43 terminates at the end of period I.

However, since the current flowing through inductor 51 cannot change instantaneously, this current will now continue to flow from the B- bus 39 through capacitor 68, eventually causing the voltage at midpoint line 44 to drop to the voltage level on the B- bus (period II in FIG. 3). Thus, capacitor 68 restrains the rate of voltage change across the collector and emitter terminals of transistor 42.

The current through inductor 51 reaches it maximum value when the voltage at midpoint line 44 is zero. During period III, the current will continue to flow through inductor 51 but will be supplied from the B- bus through shunt diode 67. It will be appreciated that during the latter half of period II and all of period III, positive current is being drawn from a negative voltage; which, in reality, means that energy is being returned to the power supply through a path of relatively low impedance.

When the inductor current reaches zero at the start of period IV, the current through the primary winding 46 of the saturable inductor 47 will cause a current to flow out of its secondary winding 54 to cause transistor 43 to become conductive, thereby causeing a reversal in the direction of current through inductor 51 and capacitor 52. When transformer 47 saturates at the end of period IV, the drive current to the base of transistor 43 terminates and the current through inductor 51 will be supplied through capacitor 68, causing the voltage at midpoint 44 to rise (Period V). When the voltage at the midpoint line M reaches the voltage on the B+bus, the current will then flow through shunt diode 66 (period VI). The cycle is then repeated.

As seen in FIG. 3, saturable transformers 47, 49 provide transistor drive current only after the current through inductor 51 has diminished to zero. Further, the the transistor drive current is terminated before the current through inductor 51 has reached its maximum amplitude. This coordination of base drive current and inductor current is achieved because of the series-connection between the inductor 51 and the primary windings 46, 48 of saturable transformers 47, 49, respectively.

The series-connected combination of inductor 51 and capacitor 52 is energized upon the alternate conduction of transistors 42 and 43. With a large value of capacitance of capacitor 52, very little voltage will be developed across its terminals. As the value of this capacitance is decreased, however, the voltage across the capacitor will increae. As the value of capacitor 52 is reduced to achieve resonance with inductor 51, the voltage on the capacitor will rise and become infinite in a loss-free circuit operating under ideal conditions.

It has been found desirable to regulate the transistor inversion frequency, determined mainly by the saturation time of saturable transformers 47, 49, to be equel to or higher than the natural resonance frequency of the inductor and capacitor combination in order to provide a high voltage output to external load 26.

Due to so-called Q-multiplication, a high-magnitude voltage develops across capacitor 52 as the transistor inversion frequency approaches the natural resonance frequency of the series-combination of inducator 51 and capacitor 52.

When invertor circuit 24 is used in the self-ballasted fluorescent lamp of FIG. 1, it has been found that the inversion frequency may be about equal to the natural resonance frequency of the series L-C tank circuit consisting of inductor 51 and capacitor 52. However, if the capacitance value of capacitor 52 is reduced below the point of resonance, unacceptably high transistor currents will result and transistor burn-out will occur.

The sizing of capacitor 52 is determined by the particular application of inverter circuit 24; but, as long as the combined load presented to the output of inverter transistors 42, 43, has an effective inductance value sufficient to provide adequate energy storage for self-sustained transistor inverter action, the current-feedback provided by saturable transformers 47, 49 will effect alternate transistor conduction without the need for additional voltage-feedback.

Because the voltages across transistors 42, 43 are relatively low (due to the absolute voltage-clamping effect of capacitors 34, 36), the half-bridge inverter 24 is very reliable. The absence of switching transients minimizes the possibility of transistor burn-out.

Inverter circuit 24 comprises means for supplying reverse bias to the conducting transistor upon saturation of its associated saturable transformer. For this purpose, capacitors 56 and 57 are charged to negative voltages as a result of reset currents flowing into secondary windings 53, 54 from the bases of transistors 42, 43, respectively. This reverse current rapidly turns off a conducting transistor to increase its switching speed and to achieve high invertor switching efficiency.

When a transistor base-emitter junction is reversely biased, it exhibits the characteristics of a Zener diode, having a reverse breakdown voltage on the order of 8 to 14 Volt for transistors typically used in high-voltage inverters.

Since load 56 comprises a fluorescent lamp, the maximum magnitude of the voltage across capacitor 52 will be limited by the lamp's ignition and operating characteristics, thereby effectively preventing voltages across inductor 51 and capacitor 52 from ever reaching destructive levels.

## ADDITIONAL EXPLANATIONS AND COMMENTS

(a) With commonly available components, inverter circuit 24 can be made to operate efficiently at any frequency between a few kHz to perhaps as high as 50 kHz. However, for various well-known reasons (i.e., eliminating audible noise, minimizing physical size, and maximizing efficiency), the frequency actually chosen for the lamp unit of FIG. 1 was in the range of 20 to 30 kHz.

(b) The fluorescent lighting unit of FIG. 1 could be made in such manner as to permit fluorescent lamp 11 to be disconnectable from its base 12 and ballasting means 16. However, if powered with normal line voltage without its lamp load connected, frequency-converting power supply and ballasting circuit 16 is apt to self-destruct.

To avoid such self-destruction, arrangements can readily be made whereby the very act of removing the load automatically establishes a situation that prevents the possible destruction of the power supply and ballasting means. For instance, with the tank capacitor (52) being permanently connected with the lamp load (11) —thereby automatically being removed whenever the lamp is removed —the inverter circuit is protected from self-destruction.

(c) At frequencies above a few kHz, the load represented by a fluorescent lamp —once it is ignited —is

substantially resistive. Thus, with the voltage across lamp 11 being of a substantially sinusoidal waveform (as indicated in FIG. 3d), the current through the lamp will also be substantially sinusoidal in waveshape.

(d) In the fluorescent lamp unit of FIG. 1, fluorescent lamp 11 is connected with power supply and ballasting circuit 16 in the exact same manner as is load 26 connected with the circuit of FIG. 2. That is, it is connected in parallel with the tank capacitor (52) of the L-C series-resonant circuit. As is conventional in instant-start fluorescent lamps —such as lamp 11 of FIG. 1 —the two terminals from each cathode are shorted together, thereby to constitute a situation where each cathode effectively is represented by only a single terminal. However, it is not necessary that the two terminals from each cathode be shorted together; in which case —for instant-start operation —connection from a lamp's power supply and ballasting means need only be made with one of the terminals of each cathode.

(d) It is thought that the present invention and many of its attendant advantages will be understood from the foregoing description and that many changes may be made in the form and construction of its components parts, the form described being merely a preferred embodiment of the invention.

I claim:

1. An arrangement comprising:

gas discharge lamp means having lamp terminals;

frequency-converting power supply and ballasting means having input terminals and output terminals, the output terminals being: (i) connected with the lamp terminals, and (ii) operative, whenever either an AC voltage or a DC voltage of magnitude about equal to that of an ordinary power line voltage is applied to the input terminals, to provide operating voltage to the lamp terminals, the frequency of the operating voltage being different from that of the ordinary power line voltage; and

base means operative to rigidly and non-detachably hold together the lamp means and the frequency-converting power supply and ballasting means, thereby to form an integral lamp unit, the base means having: (i) a screw base operative to be screwed into and held by an ordinary Edison-type lamp socket, the lamp socket having socket electrodes, and (ii) electrode means connected with the input terminals and operative, after the base means having been screwed into the Edison-type lamp socket, to make contact with the socket electrodes.

2. An arrangement comprising:

gas discharge lamp means having lamp terminals, which, for optimally effective lamp operation, must be supplied with an operating voltage of frequency different from that of the power line voltage normally present on an ordinary electric utility power line;

frequency-converting power supply and ballasting means having input terminals and output terminals, the output terminals being connected with the lamp terminals and being operative, whenever either an AC voltage or a DC voltage of magnitude about equal to that of ordinary power line voltage is applied to the input terminals, to provide the operating voltage thereto; and

base means operative to ridigly and non-detachably hold together the lamp means and the frequency-converting power supply and ballasting means, thereby to form an integral lamp unit, the base means having: (i) a screw base operative to be screwed into and held by an ordinary Edison-type lamp socket, the lamp socket having socket electrodes, and (ii) electrode means connected with the input terminals and operative, after the base means having been screwed into the Edison-type lamp socket, to make contact with the socket electrodes.

3. An arrangement comprising:

gas discharge lamp means having lamp terminals;

rectifier means having AC input terminals and DC output terminals, a DC voltage being supplied at the DC output terminals in response to the provision at the AC input terminals of either an AC voltage or a DC voltage of magnitude about equal to that of the power line voltage normally present on an ordinary electric utility power line;

inverter means connected with the DC output terminals and operative to provide a high-frequency output voltage at a set of high-frequency output terminals, the frequency of the high-frequency output voltage being substantially higher than that of the power line voltage present on an ordinary electric utility power line;

L-C tank circuit means connected with the high-frequency output terminals and operative to resonantly interact with the high-frequency output voltage provided thereat, the L-C tank circuit having a tank inductor and a tank capacitor, the gas discharge lamp means being effectively connected in parallel with the tank capacitor; and

base means operative to hold together the gas discharge lamp means, the recitifier means, the inverter means and the L-C tank circuit means, thereby to form an integral lamp unit having no detachable parts, the base means having: (i) a screw base operative to be screwed into and to be held by an ordinary Edison-type lamp socket, the lamp socket having socket electrodes at which is sometimes provided the power line voltage present on an ordinary electric utility power line, the (ii) electrode means connected with the AC input terminals and operative, after the base means having been screwed into the Edison-type lamp socket, to make contact with the socket electrodes;

whereby the lamp unit can be screwed into and be held by an ordinary Edison-type lamp socket, thereby to be properly powered from the power line voltage sometimes provided at the socket electrodes thereof.

4. The arrangement of claim 3 wherein: (i) the L-C tank circuit comprises a series-combination of an inductor and a capacitor, and (ii) this series-combination is series-resonant at or near the frequency of the high-frequency output voltage.

5. An arrangement comprising:

power supply means having input terminals and output terminals, an AC output voltage being provided at the output terminals whenever the input terminals are provided with either an AC or DC voltage of magnitude about equal to the power line voltage normally present at an ordinary electric utility power line;

a series-combination of an inductor and a capacitor connected across the output terminals and constituted such as to exhibit series-resonant action at or near the fundamental frequency of the AC output voltage;

gas discharge lamp means having a set of lamp terminals connected in parallel circuit with the capacitor, thereby to constitute a load as well as an overload protection means for the series-resonant series-combination; and

base means operative to non-detachably hold together the power supply means, the series-combination, and the gas discharge lamp means, thereby to form an integral lamp unit, the base means having: (i) a screw base operative to be screwed into and to be held by an ordinary Edison-type lamp socket, the lamp socket having socket electrodes at which is sometimes provided the power line voltage from an ordinary electric utility power line, and (ii) electrode means connected with the input terminals and operative, after the base means having been screwed into the Edison-type lamp socket, to make contact with the socket electrodes;

such that the lamp unit can be screwed into and be held by an ordinary Edison-type lamp socket, thereby to be properly powered from the power line voltage sometimes provided at the socket electrodes thereof.

6. The arrangement of claim 5 wherein the power supply means comprises:

rectifier means connected with the input terminals and operative, whenever the power line voltage is supplied thereto, to provide a DC voltage at a center-tapped DC output;

half-bride inverter means connected between the centertapped DC output and the output terminals, the half-bridge inverter means being operative to convert the DC voltage to the AC output voltage.

7. The arrangement of claim 5 wherein the AC output voltage is characterized as having a fundamental frequency that is different from that of the power line voltage.

8. The arrangement of claim 1 wherein the frequency-converting power supply and ballasting means comprises: (i) recitifer means connected with the input terminals and operative to provide a DC voltage at a set of DC terminals, and (ii) inverter means connected with the DC terminals and operative to provide to the output terminals a current of substantially sinusoidal waveshape.

9. The arrangement of claim 1 wherein the frequency-converting power supply and ballasting means comprises: (i) rectifier means connected with the input terminals and operative to provide a DC voltage at a set of DC terminals, and (ii) inverter means connected with the DC terminals and operative to provide to the output terminals a voltage of substantially sinusoidal waveshape.

10. The arrangement of claim 1 wherein the frequency-converting power supply and ballasting means comprises: (i) rectifier means connected with the input terminals and operative to provide a DC voltage at a set of DC terminals, and (ii) inverter means connected with the DC terminals and operative to provide to the output terminals a voltage suitable for starting and operating the gas discharge lamp, the inverter means having a pair of transistors series-connected across the DC terminals.

11. The arrangement of claim 1 wherein the frequency-converting power supply and ballasting means comprises: (i) rectifier means connected with the input terminals and operative to provide a DC voltage at a set of DC terminals, and (ii) inverter means connected with the DC terminals and operative to provide to the output terminals a voltage suitable for starting and operating the gas discharge lamp, the inverter means having transistor means operative to oscillate by way of positive feedback administered by way of saturable inductor means.

12. The arrangement of claim 5 wherein an AC load voltage is present across the capacitor, which AC load voltage is of substantially sinusoidal waveshape.

13. The arrangement of claim 5 wherein the AC output voltage may reasonably be characterized as being a squarewave voltage.

14. The arrangement of claim 6 wherein the half-bridge inverter means is made to oscillate by way of positive feedback administered by way of a saturable inductor means.

15. A screw-in lamp unit comprising:

gas discharge lamp means having lamp terminals;

frequency-converting ballasting means having input terminals and output terminals; the output terminals being: (i) connected with the lamp terminals; and (ii) operative, whenever an AC voltage or, alternatively, a DC voltage of magnitude about equal to that of the power line voltage normally present at an ordinary electric utility power line is applied to the input terminals, to provide operating voltage to the lamp terminals; the frequency of the operating voltage being different from that of the power line voltage; the waveshape of the operating voltage being substantially sinusoidal; and

screw base means operative to hold together the lamp means and the frequency-converting ballasting means, thereby to form the screw-in lamp unit; the screw base means having: (i) a screw base operative to be screwed into and held by an ordinary Edison-type lamp socket, the lamp socket having socket electrodes; and (ii) electrode means connected with the input terminals and operative, after the screw base means having been screwed into the Edison-type lamp socket, to make contact with the socket electrodes;

whereby the screw-in lamp unit is operative to be properly powered from: (i) the power line voltage present on an ordinary electric utility power line; and (ii) alternatively, from a DC voltage of magnitude about equal to that of this power line voltage.

16. The screw-in lamp unit of claim 15 wherein:

the frequency of the operating voltage is substantially higher than that of the power line voltage; and

the frequency-converting power supply includes: (i) inverter means connected in circuit with the input terminals and operative to provide a high-frequency inverter voltage at a set of inverter terminals; and (ii) tuned L-C circuit resonant at or near the fundamental frequency of the high-frequency inverter voltage, the tuned L-C circuit being connected between the inverter terminals and the output terminals.

17. A combination comprising:

gas discharge lamp means having lamp terminals;

rectifier means having power input terminals and DC output terminals; an output DC voltage being supplied at the DC output terminals in response to the provision at the power input terminals of an input AC voltage or, alternatively, an input DC voltage of magnitude about equal to that of the power line voltage normally present on an ordinary electric utility power line;

inverter means connected with the DC output terminals and operative to provide a high-frequency output current from a set of high-frequency output terminals; the inverter means including a transistor operative to conduct current in response to a control voltage provided at a control input; the frequency of the high-frequency output current being substantially higher than that of the power line voltage present on an ordinary electric utility power line; and

L-C circuit means connected in circuit between the high-frequency output terminals and the lamp terminals; the L-c circuit means being operative to cause a sinusoidal high-frequency voltage to be present across the lamp terminals; the high-frequency voltage having a cycle period;

the combination being so arranged as to cause the transistor to conduct current for a brief span of time once during each cycle period of the high-frequency voltage; the duration of the brief span of time being about equal to or shorter than one quarter of the cycle period.

18. The combination of claim 17 wherein: (i) the L-C circuit means includes a tank-capacitor and a tank-inductor effectively series-connected across the high-frequency output terminals; (ii) the tank-inductor and tank-capacitor being operative to resonantly interact at the frequency of the highfrequency output current; and (iii) the lamp terminals are effectively connected in parallel with the tank-capacitor.

19. The combination of claim 17 arranged to be integrated with a screw-in lamp base having base terminals, thereby to form a screw-in lamp unit; the base terminals being connected with the power input terminals.

20. A combination comprising:

gas discharge lamp means having lamp terminals;

rectifier means having power input terminals and DC output terminals; an output DC voltage being supplied at the DC output terminals in response to the provision at the power input terminals of an input AC voltage or, alternatively, an input DC voltage of magnitude about equal to that of the power line voltage normally present on an ordinary electric utility power line;

inverter means connected with the DC output terminals and operative to provide a high-frequency output current from a set of high-frequency output terminals; the inverter means including a transistor operative to conduct current in response to a control voltage provided at a control input; the frequency of the high-frequency output current being substantially higher than that of the power line voltage present on an ordinary electric utility power line; and

L-C means connected in circuit between the high-frequency output terminals and the lamp terminals; the L-C means having a tank-inductor and a tank-capacitor; the L-C means being operative to cause a first substantially sinusoidal high-frequency voltage to be present across the tank-capacitor; the lamp terminals being effectively connected in parallel with the tank-capacitor, thereby to cause a second substantially sinusoidal high-frequency voltage to be provided across the lamp terminals; the first and the second high-frequency voltage being approximately of the same frequency, phase and period;

the combination being so arranged as to cause the transistor to conduct current for a brief span of time once during each period; the duration of the brief span of time being shorter than half that of the period.

21. The combination of claim 20 wherein the tank-inductor and the tank-capacitor are: (i) effectively series-connected across the high-frequency output terminals; and (ii) operative to resonantly interact at the frequency of the high-frequency output current.

* * * * *

# 2

US005233270A

# United States Patent [19]

Nilssen

[11] Patent Number: 5,233,270

[45] Date of Patent: * Aug. 3, 1993

[54] SELF-BALLASTED SCREW-IN FLUORESCENT LAMP

[76] Inventor: Ole K. Nilssen, Caesar Dr., Barrington, Ill. 60010

[*] Notice: The portion of the term of this patent subsequent to Sep. 10, 2008 has been disclaimed.

[21] Appl. No.: 955,229

[22] Filed: Oct. 1, 1992

Related U.S. Application Data

[63] Continuation of Ser. No. 607,271, Oct. 31, 1990, abandoned, which is a continuation-in-part of Ser. No. 787,692, Oct. 15, 1985, abandoned, which is a continuation of Ser. No. 644,155, Aug. 27, 1984, abandoned, which is a continuation of Ser. No. 555,426, Nov. 23, 1983, abandoned, which is a continuation of Ser. No. 178,107, Aug. 14, 1980, abandoned.

[51] Int. Cl.[5] ..... H05B 41/29

[52] U.S. Cl. ..... 315/58; 315/326; 315/DIG. 5

[58] Field of Search ..... 315/32, 51, 53, 56, 315/58, 326, DIG. 2, DIG. 5; 313/634, 635, 317, 318, 493

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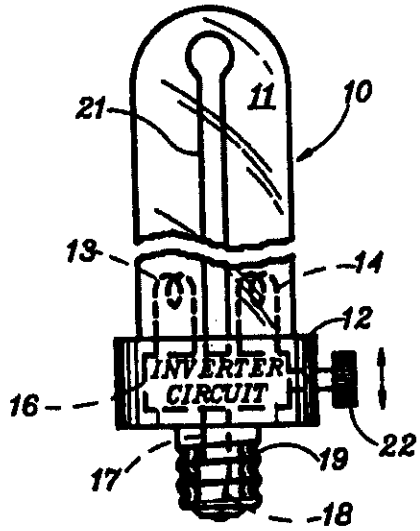
*Primary Examiner*—David Mis

[57] ABSTRACT

A compact screw-in fluorescent lamp is mounted on an ordinary Edison-type screw-base. An inverter-type ballast is integrally included with the base, thereby making the fluorescent lamp capable of being screwed into an ordinary lamp socket and to be powered therefrom by ordinary power line voltage. The fluorescent lamp is folded and has a narrowed section of glass. The inverter-type ballast, which includes a half-bridge self-oscillating inverter, is powered via a voltage doubler and powers the fluorescent lamp via an tuned L-C circuit. Light output can be adjusted by way of an adjustment means functional to adjust the inverter frequency, thereby correspondingly to adjust the magnitude of the lamp current.

18 Claims, 2 Drawing Sheets



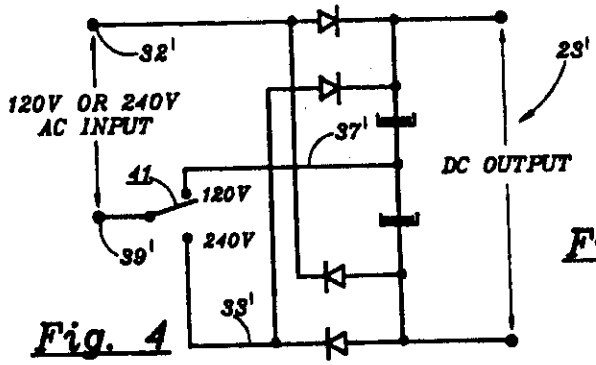



Fig. 4

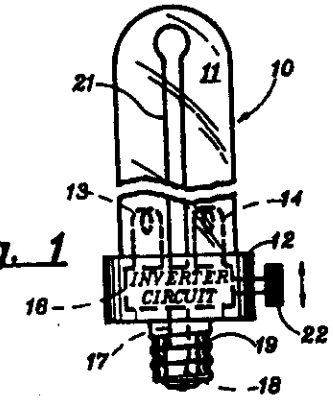



Fig. 1

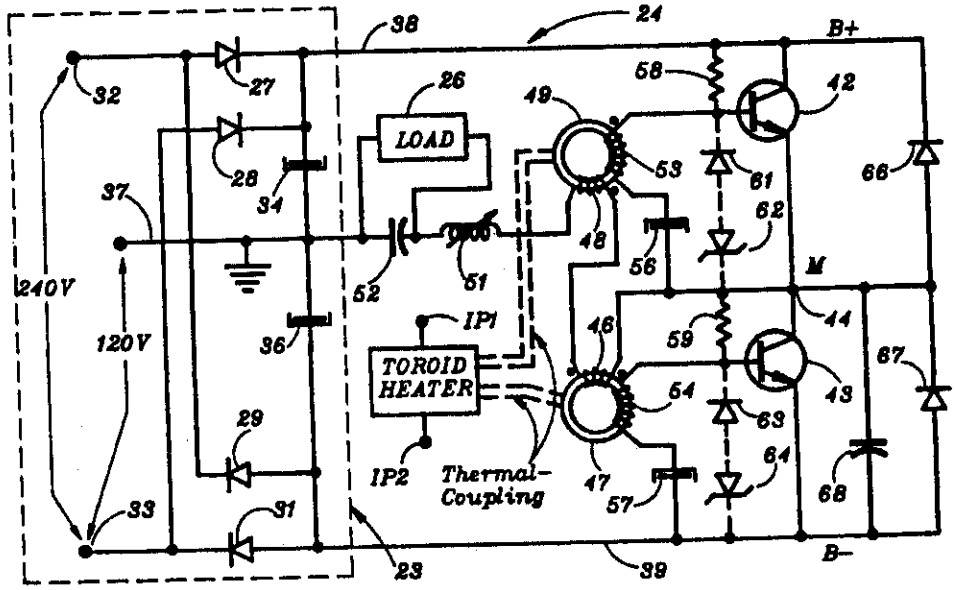



Fig. 2

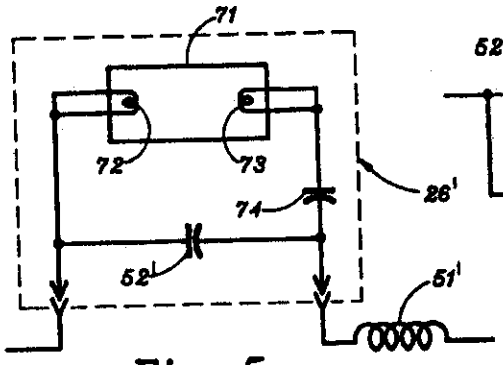



Fig. 5

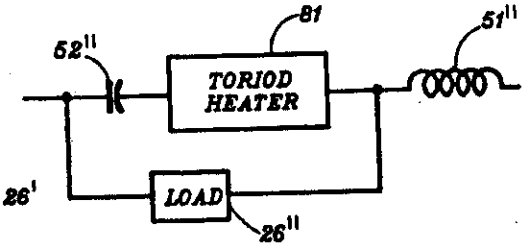



Fig. 6

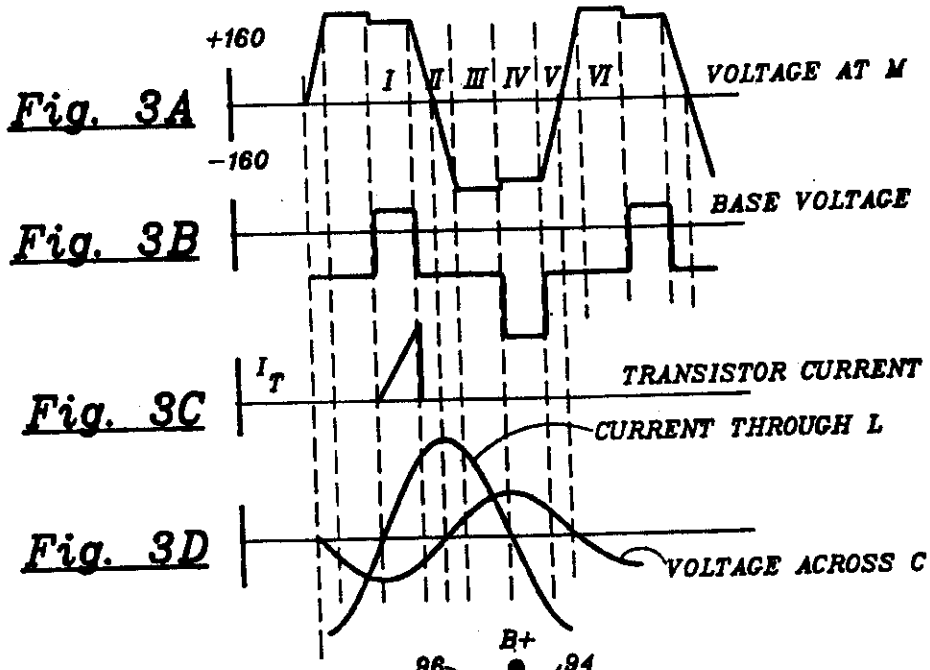



Fig. 3A

Fig. 3B

Fig. 3C

Fig. 3D

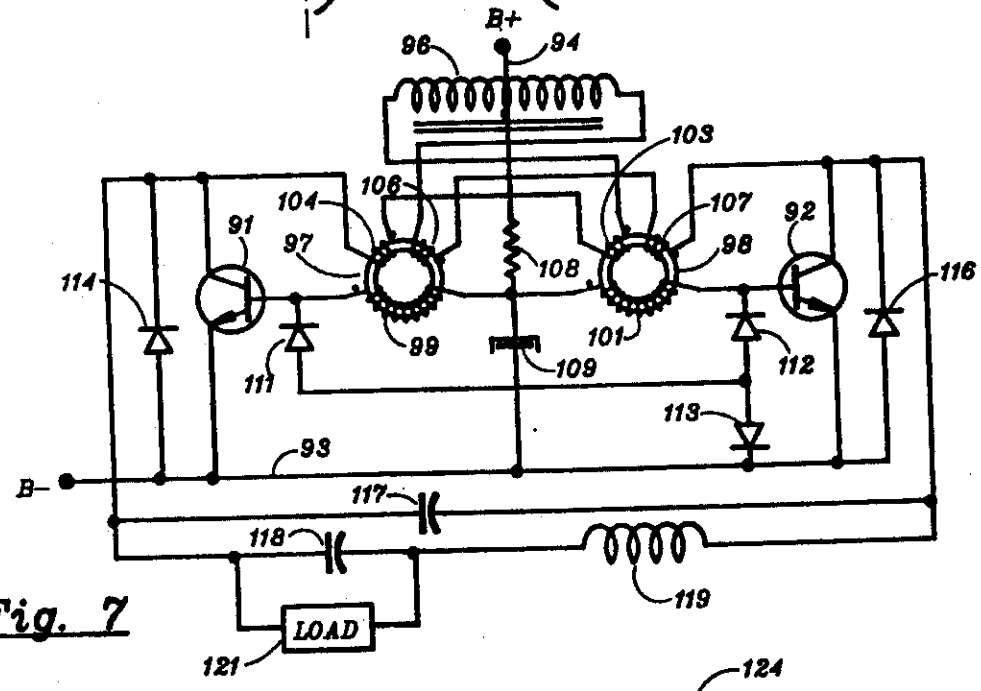



Fig. 7

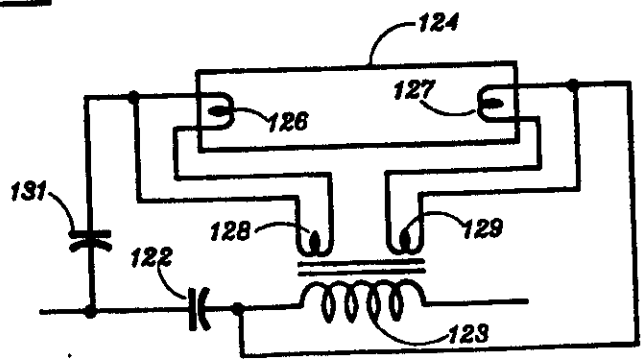



Fig. 8

# SELF-BALLASTED SCREW-IN FLUORESCENT LAMP

## BACKGROUND OF THE INVENTION

1. Related Applications

The present application is a continuation of Ser. No. 07/607,271 filed Oct. 31, 1990 now abandoned which is Continuation-in-Part of Ser. No. 06/787,692 filed Oct. 15, 1985 now abandoned; which is a continuation of Ser. No. 06/644,155 filed Aug. 27, 1984, now abandoned; which was a continuation of Ser. No. 06/555,426 filed Nov. 23, 1983, now abandoned; which was a continuation of Ser. No. 06/178,107 filed Aug. 14, 1980, now abandoned.

2. Field of Invention

This invention relates to self-ballasted screw-in gas discharge lamps as well as to power supplies particularly useful for ballasting gas discharge lamps.

3. Description of Prior Art

For a description of pertinent prior art, reference is made to U.S. Pat. No. 4,677,345 to Nilssen; which patent issued from a Division of application Serial No. 06/178,107 filed Aug. 14, 1980; which application is the original progenitor of instant application.

Otherwise, reference is made to the following U.S. Patents: U.S. Pat. No. 3,263,122 to Genuit; U.S. Pat. No. 3,320,510 to Locklair; U.S. Pat. No. 3,996,493 to Davenport et el.; U.S. Pat. No. 4,100,476 to Ghiringhelli; U.S. Pat. No. 4,262,327 to Kovacik et al.; U.S. Pat. No. 4,370,600 to Zansky; U.S. Pat. No. 4,634,932 to Nilssen; and U.S. Pat. No. 4,857,806 to Nilssen.

## SUMMARY OF THE INVENTION

### Objects of the Invention

An object of the present invention is that of providing a self-ballasted screw-in gas discharge lamp.

Another object is that of providing a compact folded fluorescent lamp.

Yet another object is that of providing means for adjusting the light output of gas discharge lamps.

These as well as other objects, features and advantages of the present invention will become apparent from the following description and claims.

## BRIEF DESCRIPTION

The present invention is directed to providing improved gas discharge lighting means and inverter circuits for powering and controlling gas discharge lamps. The inverter circuits according to the present invention are highly efficient, can be compactly constructed and are ideally suited for energizing gas discharge lamps, particularly compact folded "instant-start" "self-ballasted" fluorescent lamps.

According to one feature of the present invention, a series-connected combination of an inductor and a capacitor is provided in circuit with the inverter transistors to be energized upon periodic transistor conduction. Transistor drive current is preferably provided through the use of at least one saturable inductor to control the transistor inversion frequency to be equal to or greater than the nature resonant frequency of the inductor and capacitor combination. The high voltages efficiently developed by loading the inverter with the inductor and capacitor are ideally suited for energizing external loads such as gas discharge lamps. In such an application, the use of an adjustable inductor permits



control of the inverter output as a means of adjusting the level of lamp illumination.

According to another feature of the present invention, reliable and highly efficient half-bridge inverters include a saturable inductor in a current feedback circuit to drive the transistors for alternate conduction. The inverters also include a load having an inductance sufficient to effect periodic energy storage for self-sustained transistor inversion. Importantly, improved reliability is achieved because of the relatively low and transient-free voltages across the transistors in these half-bridge inverters.

Further, according to another feature of the present invention, novel and economical power supplies particularly useful with the disclosed inverter circuits convert conventional AC input voltages to DC for supplying to the inverters.

Yet further, according to still another feature of the invention, a rapid-start fluorescent lamp is powered by way of a series-resonant LC circuit; while heating power for the lamp's cathodes is provided via loosely-coupled auxiliary windings on the tank inductor of the LC circuit. Alternatively, cathode heating power is provided from tightly-coupled windings on the tank inductor; in which case output current-limiting is provided via a non-linear resistance means, such as an incandescent filament in a light bulb, connected in series with the output of each winding.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a front elevation of a folded fluorescent lamp unit adapted for screw-in insertion into a standard Edison incandescent socket;

FIG. 2 is a schematic diagram illustrating the essential features of a push-pull inverter circuit particularly suitable for energizing the lamp unit of FIG. 1;

FIGS. 3A–3D is a set of waveform diagrams of certain significant voltages and currents occurring in the circuit of FIG. 2;

FIG. 4 is a schematic diagram of a DC power supply connectable to both 120 and 240 volt AC inputs;

FIG. 5 is a schematic diagram which illustrates the connection of a non-self-ballasted gas discharge lamp unit to the FIG. 2 inverter circuit;

FIG. 6 is a schematic diagram which illustrates the use of a toroid heater for regulation of the inverter output;

FIG. 7 is an alternate form of push-pull inverter circuit according to the present invention;

FIG. 8 is a schematic diagram showing the connection of a gas discharge lamp of the "rapid-start" type to an inductor-capacitor-loaded inverter according to the present invention

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 illustrates a screw-in gas discharge lamp unit 10 comprising a folded fluorescent lamp 11 suitably secured to an integral base 12. The lamp comprises two cathodes 13, 14 which are supplied with the requisite high operating voltage from a frequency-converting power supply and ballasting circuit 16; which, because of its compact size, conveniently fits within the base 12.

The inverter circuit 16 is connected by leads 17, 18 to a screw-type plug 19 adapted for screw-in insertion into a standard Edison-type incandescent lamp socket at which ordinary 120 Volt/60 Hz power line voltage is available. A ground plane comprising a wire or metallic

strip 21 is disposed adjacent a portion of the fluorescent lamp 11 as a starting aid. Finally, a manually rotatable external knob 22 is connected to a shaft for mechanical adjustment of the air gap of a ferrite core inductor to vary the inductance value thereof in order to effect adjustment of the inverter voltage output connected to electrodes 13, 14 for controlled variation of the lamp illumination intensity.

With reference to FIG. 2, a power supply 23, connected to a conventional AC input, provides a DC output for supplying a high-efficiency inverter circuit 24. The inverter is operable to provide a high voltage to an external load 26, which may comprise a gas discharge device such as the fluorescent lamp 11 of FIG. 1.

The power supply 23 comprises bridge rectifier having four diodes 27, 28, 29 and 31 connectable to a 240 volt AC supply at terminals 32, 33. Capacitors 34, 36 are connected between a ground line 37 (in turn directly connected to the inverter 24) and to a B+ line 38 and a B− line 39, respectively. The power supply 23 also comprises a voltage doubler and rectifier optionally connectable to a 120 volt AC input taken between the ground line 37 and terminal 33 Or 32. The voltage doubler and rectifier means provides a direct electrical connection by way of line 37 between one of the 120 volt AC power input lines and the inverter 24, as shown in FIG. 2. The bridge rectifier and the voltage doubler and rectifier provide substantially the same DC output voltage to the inverter 24 whether the AC input is 120 or 240 volts. Typical voltages are +160 volts on the B+ line 38 and −160 volts on the B− line 39.

With additional reference to FIG. 4, which shows an alternate power supply 23', the AC input, whether 120 or 240 volts, is provided at terminals 32' and 39'. Terminal 39' is in turn connected through a single-pole double-throw selector switch 41 to terminal 37' (for 120 volt operation) or terminal 33' (for 240 volt operation). In all other respects, power supplies 23 and 23' are identical.

The inverter circuit 24 of FIG. 2 is a half-bridge inverter comprising transistors 42, 43 connected in series across the DC voltage output of the power supply 23 on B+ and B− lines 38 and 39, respectively. The collector of transistor 42 is connected to the B+ line 38, the emitter of transistor 42 and the collector of transistor 43 are connected to a midpoint line 44 (designated "M") and the emitter of transistor 43 is connected to the B− line 39. The midpoint line 44 is in turn connected to the ground line 37 through primary winding 46 of a toroidal saturable core transformer 47, a primary winding 48 on an identical transformer 49, an inductor 51 and a series-connected capacitor 52. The inductor 51 and capacitor 52 are energized upon alternate transistor conduction in a manner to be described later.

An external load 26 is preferably taken off capacitor 52, as shown in FIG. 2. The inductor 51, preferably a known ferrite core inductor, has an inductance variable by mechanical adjustment of the air gap in order to effect variation in the level of the inductor and capacitor voltage and hence the power available to the load, as will be described. When the load is a gas discharge lamp such as lamp 11 in FIG. 1, variation in this inductance upon rotation of knob 22 accomplishes a lamp dimming effect.

Drive current to the base terminals of transistors 42 and 43 is provided by secondary windings 53, 54 of transformers 49, 47, respectively. Winding 53 is also connected to midpoint lead 44 through a bias capacitor 56, while winding 54 is connected to the B− lead 39 through an identical bias capacitor 57. The base terminals of transistors 42 and 43 are also connected to lines 38 and 44 through bias resistors 58 and 59, respectively. For a purpose to be described later, the base of transistor 42 can be optionally connected to a diode 61 and a series Zener diode 64 in turn connected to the midpoint line 44; similarly, a diode 63 and series Zener diode 64 in turn connected to the B− line 39 can be connected to the base of transistor 43. Shunt diodes 66 and 67 are connected across the collector-emitter terminals of transistors 42 and 43, respectively. Finally, a capacitor 68 is connected across the collector-emitter terminals of transistor 43 to restrain the rate of voltage rise across those terminals, as will be seen presently.

The operation of the circuit of FIG. 2 can best be understood with additional reference to FIG. 3, which illustrates significant portions of the waveforms of the voltage at midpoint M (FIG. 3A), the base-emitter voltage on transistor 42 (FIG. 3B), the current through transistor 42 (FIG. 3C), and the capacitor 52 voltage and the inductor 51 current (FIG. 3D).

Assuming that transistor 42 is first to be triggered into conduction, current flows from the B+ line 38 through windings 46 and 38 and the inductor 51 to charge capacitor 52 and returns through capacitor 34 (refer to the time period designated I in FIG. 3). When the saturable inductor 49 saturates at the end of period I, drive current to the base of transistor 42 will terminate, causing voltage on the base of the transistor to drop to the negative voltage stored on the bias capacitor 56 in a manner to be described, causing this transistor to become nonconductive. A shown in FIG. 3c, current-flow in transistor 43 terminates at the end of period I.

Because the current through inductor 51 cannot change instantaneously, current will flow from the B− bus 39 through capacitor 68, causing the voltage at midpoint line 44 to drop to −160 volts (period II in FIG. 3). The capacitor 68 restrains the rate of voltage change across the collector and emitter terminals of transistor 42. The current through the inductor 51 reaches its maximum value when the voltage at the midpoint line 44 is zero. During period III, the current will continue to flow through inductor 51 but will be supplied from the B-bus through the shunt diode 67. It will be appreciated that during the latter half of period II and all of period III, positive current is being drawn from a negative voltage; which, in reality, means that energy is being returned to the power supply through a path of relatively low impedance.

When the inductor current reaches zero at the start of period IV, the current through the primary winding 46 of the saturable inductor 47 will cause a current to flow out of its secondary winding 54 to cause transistor 43 to become conductive, thereby causing a reversal in the direction of current through inductor 51 and capacitor 52. When transformer 47 saturates at the end of period IV, the drive current to the base of transistor 43 terminates and the current through inductor 51 will be supplied through capacitor 68, causing the voltage at midpoint line 44 to rise (period V). When the voltage at the midpoint line M reaches 160 volts, the current will then flow through shunt diode 66 (period VI). The cycle is then repeated.

As seen in FIG. 3, saturable transformers 47, 49 provide transistor drive current only after the current through inductor 51 has diminished to zero. Further, the transistor drive current is terminated before the

current through inductor 51 has reached its maximum amplitude. This coordination of base drive current and inductor current is achieved because of the series-connection between the inductor 51 and the primary windings 46, 48 of saturable transformers 47, 49, respectively.

The series-connected combination of the inductor 51 and the capacitor 52 is energized upon the alternate conduction of transistors 42 and 43. With a large value of capacitance of capacitor 52, very little voltage will be developed across its terminals. As the value of this capacitance is decreased, however, the voltage across this capacitor will increase. As the value of the capacitor 52 is reduced to achieve resonance with the inductor 51, the voltage on the capacitor will rise and become infinite in a loss-free circuit operating under ideal conditions.

It has been found desirable to regulate the transistor inversion frequency, determined mainly by the saturation time of the saturable inductors 47, 49, to be equal to or higher than the natural resonance frequency of the inductor and capacitor combination in order to provide a high voltage output to external load 26. A high voltage across capacitor 52 is efficiently developed as the transistor inversion frequency approaches the natural resonant frequency of the inductor 51 and capacitor 52 combination. Stated another way, the conduction period of each transistor is desirably shorter in duration than one quarter of the full period corresponding to the natural resonant frequency of the inductor and capacitor combination. When the inverter 24 is used with a self-ballasted gas discharge lamp unit, it has been found that the inversion frequency can be at least equal to the natural resonant frequency of the tank circuit. If the capacitance value of capacitor 52 is reduced still further beyond the resonance point, unacceptably high transistor currents will be experienced during transistor switching and transistor burn-out will occur.

It will be appreciated that the sizing of capacitor 52 is determined by the application of the inverter circuit 24. Variation in the values of the capacitor 52 and the inductor 51 will determine the voltages developed in the inductor-capacitor tank circuit. The external load 26 may be connected in circuit with the inductor 51 (by a winding on the inductor, for example) and the capacitor may be omitted entirely. If the combined circuit loading of the inductor 51 and the external load 26 has an effective inductance of value sufficient to effect periodic energy storage for self-sustained transistor inversion, the current feedback provided by the saturable inductors 47,49 will effect alternate transistor conduction without the need for additional voltage feedback. When the capacitor 52 is omitted, the power supply 23 provides a direct electrical connection between one of the AC power input lines and the inverter load circuit.

Because the voltages across transistors 42, 43 are relatively low (due to the effect of capacitors 34, 36), the half-bridge inverter 24 is very reliable. The absence of switching transients minimizes the possibility of transistor burn-out.

The inverter circuit 24 comprises means for supplying reverse bias to the conducting transistor upon saturation of its associated saturable inductor. For this purpose, the capacitors 56 and 57 are charged to negative voltages as a result of reset current flowing into secondary windings 53, 54 from the bases of transistors 42, 43, respectively. This reverse current rapidly turns off a conducting transistor to increase its switching speed and to achieve inverter circuit efficiency in a manner described more fully in my co-pending U.S. patent application Ser. No. 103,624 filed Dec. 14, 1979 and entitled "Bias Control for High Efficiency Inverter Circuit" (now U.S. Pat. No. 4,307,353). The more negative the voltage on the bias capacitors 56 and 57, the more rapidly charges are swept out of the bases of their associated transistors upon transistor turn-off.

When a transistor base-emitter junction is reversely biased, it exhibits the characteristics of a Zener diode having a reverse breakdown voltage on the order of 8 to 14 Volt for transistors typically used in high-voltage inverters. As an alternative, to provide a negative voltage smaller in magnitude on the base lead of typical transistor 42 during reset operation, the optional diode 61 and Zener diode 62 combination can be used. For large values of the bias capacitor 56, the base voltage will be substantially constant.

If the load 26 comprises a gas discharge lamp, the voltage across the capacitor 52 will be reduced once the lamp is ignited to prevent voltages on the inductor 51 and the capacitor 52 from reaching destructive levels. Such a lamp provides an initial time delay during which a high voltage, suitable for instant starting, is available.

FIG. 5 illustrates the use of an alternate load 26' adapted for plug-in connection to an inverter circuit such as shown in FIG. 2. The load 26' consists of a gas discharge lamp 71 having electrodes 72, 73 and connected in series with a capacitor 74. The combination of lamp 71 and capacitor 74 is connected in parallel with a capacitor 52' which serves the same purpose as capacitor 52 in the FIG. 2 circuit. However, when the load 26' is unplugged from the circuit, the inverter stops oscillating and the development of high voltages in the inverter is prevented. The fact that no high voltages are generated by the circuit if the lamp is disconnected while the circuit is oscillating is important for safety reasons.

FIG. 6 illustrates a capacitor 52'' connected in series with an inductor 51'' through a heater 81 suitable for heating the toroidal inductors 47, 49 in accordance with the level of output. The load 26'' is connected across the series combination of the capacitor 52'' and the toroid heater. The heater 81 is preferably designed to controllably heat the toroidal saturable inductors in order to decrease their saturation flux limit and hence their saturation time. The result is to decrease the periodic transistor conduction time and thereby increase the transistor inversion frequency. When a frequency-dependent impedance means, that is, an inductor or a capacitor, is connected in circuit with the AC voltage output of the inverter, change in the transistor inversion frequency will modify the impedance of the frequency-dependent impedance means and correspondingly modify the inverter output. Thus as the level of the output increases, the toroid heater 81 is correspondingly energized to effect feedback regulation of the output. Further, transistors 42, 43 of the type used in high voltage inverters dissipate heat during periodic transistor conduction. As an alternative, the toroid heater 81 can use this heat for feedback regulation of the output or control of the temperature of transistors 42, 43.

The frequency dependent impedance means may also be used in a circuit to energize a gas discharge lamp at adjustable illumination levels. Adjustment in the inversion frequency of transistors 42, 43 results in control of the magnitude of the AC current supplied to the lamp. This is preferably accomplished where saturable induc-

tors 47, 49 have adjustable flux densities for control of their saturation time.

FIG. 7 schematically illustrates an alternate form of inverter circuit, shown without the AC to DC power supply connections for simplification. In this Figure, the transistors are connected in parallel rather than in series but the operation is essentially the same as previously described.

In particular, this circuit comprises a pair of alternately conducting transistors 91, 92. The emitter terminals of the transistors are connected to a B− line 93. A B+ lead 94 is connected to the center-tap of a transformer 96. In order to provide drive current to the transistors 91, 92 for control of their conduction frequency, saturable inductors 97, 98 have secondary windings 99, 101, respectively, each secondary winding having one end connected to the base of its associated transistor; the other ends are connected to a common terminal 102. One end of transformer 96 is connected to the collector of transistor 91 through a winding 103 on inductor 98 in turn connected in series with a winding 104 on inductor 97. Likewise, the other end of transformer 96 is connected to the collector of transistor 92 through a winding 106 on inductor 97 in series with another winding 107 on inductor 98.

The B+ terminal is connected to terminal 102 through a bias resistor 108. A bias capacitor 109 connects terminal 102 to the B− lead 93. This resistor and capacitor serve the same function as resistors 58, 59 and capacitors 56, 57 in the FIG. 2 circuit.

The bases of transistors 91, 92 are connected by diodes 111, 112, respectively, to a common Zener diode 113 in turn connected to the B− lead 93. The common Zener diode 113 serves the same function as individual Zener diodes 62, 64 in FIG. 2.

Shunt diodes 114, 116 are connected across the collector-emitter terminals of transistors 91, 92, respectively. A capacitor 117 connecting the collectors of transistors 91, 92 restrains the rate of voltage rise on the collectors in a manner similar to the collector-emitter capacitor 68 in FIG. 2.

Inductive-capacitive loading of the FIG. 7 inverter is accomplished by a capacitor 118 connected in series with with an inductor 119, the combination being connected across the collectors of the transistors 91, 92. A load 121 is connected across the capacitor 118.

FIG. 8 illustrates how an inverter loaded with a series capacitor 122 and inductor 123 can be used to energize a "rapid-start" fluorescent lamp 124 (the details of the inverter circuit being omitted for simplication). The lamp 124 has a pair of cathodes 126, 127 connected across the capacitor 122 for supply of operating voltage in a manner identical to that previously described. In addition, the inductor 123 comprises a pair of magnetically-coupled auxiliary windings 128, 129 for electrically heating the cathodes 126, 127, respectively. A small capacitor 131 is connected in series with lamp 124.

Additional Explanations and Comments

(a) With reference to FIGS. 2 and 5, adjustment of the amount of power supplied to load 26', and thereby the amount of light provided by lamp 71, may be accomplished by applying a voltage of adjustable magnitude to input terminals IP1 and IP2 of the Toroid Heater; which is thermally coupled with the toroidal ferrite cores of saturable transformers 47, 49.

(b) With commonly available components, inverter circuit 4 of FIG. 2 can be made to operate efficiently at any frequency between a few kHz to perhaps as high as 50 kHz. However, for various well-known reasons (i.e., eliminating audible noise, minimizing physical size, and maximizing efficiency), the frequency actually chosen is in the range of 20 to 40 kHz.

(c) The fluorescent lighting unit of FIG. 1 could be made in such manner as to permit fluorescent lamp 11 to be disconnectable from its base 12 and ballasting means 16. However, if powered with normal line voltage without its lamp load connected, frequency-converting power supply and ballasting circuit 16 is apt to self-destruct.

To avoid such self-destruction, arrangements can readily be made whereby the very act of removing the load automatically establishes a situation that prevents the possible destruction of the power supply and ballasting means. For instance, with the tank capacitor (52) being permanently connected with the lamp load (11)—thereby automatically being removed whenever the lamp is removed—the inverter circuit is protected from self-destruction.

(d) At frequencies above a few kHz, the load represented by a fluorescent lamp—once it is ignited—is substantially resistive. Thus, with the voltage across lamp 11 being of a substantially sinusoidal waveform (as indicated in FIG. 3*d*), the current through the lamp will also be substantially sinusoidal in waveshape.

(e) In the fluorescent lamp unit of FIG. 1, fluorescent lamp 11 is connected with power supply and ballasting circuit 16 in the exact same manner as is load 26 connected with the circuit of FIG. 2. That is, it is connected in parallel with the tank capacitor (52) of the L-C series-resonant circuit. As is conventional in instant-start fluorescent lamps—such as lamp 11 of FIG. 1—the two terminals from each cathode are shorted together, thereby to constitute a situation where each cathode effectively is represented by only a single terminal. However, it is not necessary that the two terminals from each cathode be shorted together; in which case—for instant-start operation—connection from a lamp's power supply and ballasting means need only be made with one of the terminals of each cathode.

(i) It is thought that the present invention and many of its attendant advantages will be understood from the foregoing description and that many changes may be made in the form and construction of its components parts, the form described being merely a preferred embodiment of the invention.

I claim:

1. An arrangement comprising:

base means adapted to be inserted into and held by a lamp socket; the lamp socket having a pair of socket terminals whereat is provided a power line voltage; the base means having a pair of base electrodes connected with the socket terminals;

a gas discharge lamp having a first and a second lamp input terminal; the gas discharge lamp having a first and a second thermionic cathode connected, respectively, with the first and the second lamp input terminal; and

a circuit assembly connected between the base electrodes and the lamp input terminals; the circuit assembly being operative to provide a lamp current to the lamp terminals; the lamp current having a substantially sinusoidal waveshape and being of frequency substantially higher than that of the power line voltage; the circuit assembly being characterized by including:

(a) a rectifier circuit connected with the base electrodes and operative to provide a DC supply voltage across a pair of DC terminals;

(b) an inverter circuit connected with the DC terminals and operative to provide an alternating inverter voltage at a pair of inverter output terminals; the waveshape of the alternating inverter voltage being non-sinusoidal and having a period; each complete period of the alternating inverter voltage consisting of four distinct parts: (i) a first part during which its instantaneous magnitude increases at a substantially constant rate; (ii) a second part during which its instantaneous magnitude remains substantially constant at a relatively high level; (iii) a third part during which its instantaneous magnitude decreases at a substantially constant rate; and (iv) a fourth part during which its instantaneous magnitude remains substantially constant at a relatively low level; the inverter circuit being characterized by including a periodically conducting transistor conducting only during the second part of each complete period of the alternating inverter voltage; and

(c) waveshaping circuitry connected between the inverter output terminals and the lamp input terminals;

the base means, the gas discharge lamp, and the circuit assembly constituting a single mechanically integral entity functional to be inserted into and held by a lamp socket.

2. An arrangement comprising:

base means adapted to be inserted into and held by a lamp socket; the lamp socket having a pair of socket terminals whereat is provided an ordinary AC power line voltage; the base means having a pair of base electrodes connected with the socket terminals;

a gas discharge lamp having a first and a second lamp input terminal; the gas discharge lamp having a first and a second thermionic cathode having, respectively, a first and a second pair of cathode terminals; there being, inside of the gas discharge lamp, an electrically conductive path extending between each of the cathode terminals of each thermionic cathode; at least one each of the first and second pair of cathode terminals being connected, respectively, with the first and the second lamp input terminal; and

a circuit assembly connected between the base electrodes and the lamp input terminals; the circuit assembly being operative to provide a lamp current to the lamp terminals; the lamp current having a substantially sinusoidal waveshape and being of frequency substantially higher than that of the power line voltage; the circuit assembly being characterized by including:

(a) a rectifier circuit connected with the base electrodes and operative to provide a DC supply voltage across a pair of DC terminals; the absolute magnitude of the DC supply voltage being substantially higher than the absolute peak magnitude of the AC power line voltage;

(b) an inverter circuit connected with the DC terminals and operative to provide an alternating inverter voltage at a pair of inverter output terminals; the waveshape of the alternating inverter voltage being non-sinusoidal and having a period; and

(c) waveshaping circuitry connected between the inverter output terminals and the lamp input terminals;

the base means, the gas discharge lamp, and the circuit assembly constituting a single mechanically integral entity functional to be inserted into and held by a lamp socket.

3. An arrangement comprising:

base means adapted to be inserted into and held by a lamp socket; the lamp socket having a pair of socket terminals whereat is provided a power line voltage; the base means having a pair of base electrodes connected with the socket terminals;

a gas discharge lamp having a first and a second lamp input terminal; the gas discharge lamp having a first and a second thermionic cathode having, respectively, a first and a second pair of cathode terminals; there being, inside of the gas discharge lamp, an electrically conductive path extending between each of the cathode terminals of each thermionic cathode; at least one each of the first and second pair of cathode terminals being connected, respectively, with the first and the second lamp input terminal; and

a circuit assembly connected between the base electrodes and the lamp input terminals; the circuit assembly being operative to provide a high-frequency lamp voltage to the lamp terminals; the high-frequency lamp voltage being of frequency substantially higher than that of the power line voltage; the circuit assembly being characterized by: (i) being operative to provide the high-frequency lamp voltage to the lamp terminals even if each of said conductive paths were to become damaged such as to prevent current form flowing between the cathode terminals of each thermionic cathode; and (ii) by including:

(a) a rectifier circuit connected with the base electrodes and operative to provide a DC supply voltage across a pair of DC terminals;

(b) an inverter circuit connected with the DC terminals and operative to provide an alternating inverter voltage at a pair of inverter output terminals; and

(c) waveshaping circuitry connected between the inverter output terminals and the lamp input terminals;

the base means, the gas discharge lamp, and the circuit assembly constituting a single mechanically integral entry functional to be inserted into and held by a lamp socket.

4. An arrangement comprising:

base means adapted to be inserted into and held by a lamp socket; the lamp socket having a pair of socket terminals whereat is provided a power line voltage; the base means having a pair of base electrodes connected with the socket terminals;

a gas discharge lamp having a first and a second lamp input terminal; the gas discharge lamp having a first and a second thermionic cathode connected, respectively, with the first and the second lamp input terminal; and

a circuit assembly connected between the base electrodes and the lamp input terminals; the circuit assembly being operative to provide a high-frequency lamp voltage to the lamp terminals; the

high-frequency lamp voltage being of frequency substantially higher than that of the power line voltage; the circuit assembly being characterized by including:

(a) a rectifier circuit connected with the base electrodes and operative to provide a DC supply voltage across a pair of DC terminals;

(b) an inverter circuit connected with the DC terminals and operative to provide an alternating inverter voltage at a pair of inverter output terminals; the inverter circuit being characterized by including a periodically conducting transistor; the transistor being characterized by having a pair of control terminals between which exists an alternating control voltage having peak-to-peak magnitude substantially larger than twice the magnitude of the forward voltage drop of an ordinary semiconductor junction diode; and

(c) waveshaping circuitry connected between the inverter output terminals and the lamp input terminals;

the base means, the gas discharge lamp, and the circuit assembly constituting a single mechanically integral entity functional to be inserted into and held by a lamp socket.

5. An arrangement comprising:

base means adapted to be inserted into and held by a lamp socket; the lamp socket having a pair of socket terminals whereat is provided a power line voltage; the base means having a pair of base electrodes connected with the socket terminals;

a gas discharge lamp having lamp terminals; and

a circuit assembly connected between the base electrodes and the lamp terminals; the circuit assembly being operative to provide an AC lamp voltage to the lamp terminals; the AC lamp voltage being of frequency substantially higher than that of the power line voltage; the circuit assembly being characterized by including:

(a) a rectifier circuit connected with the base electrodes and operative to provide a DC supply voltage across a pair of Dc terminals; the absolute magnitude of the DC supply voltage being substantially higher than the peak absolute magnitude of the power line voltage;

(b) an inverter circuit connected with the DC terminals and operative to provide an alternating inverter voltage at a pair of inverter output terminals; and

(c) current-limiting and waveshaping circuitry connected between the inverter output terminals and the lamp terminals;

the base means, the gas discharge lamp, and the circuit assembly constituting a single mechanically integral entity functional to be inserted into and held by a lamp socket.

6. The arrangement of claim 5 wherein the inverter circuit is further characterized by including a periodically conducting transistor having a pair of control terminals between which exists an alternating control voltage having peak-to-peak magnitude larger than twice the magnitude of the forward voltage drop of an ordinary semiconductor diode junction.

7. The arrangement of claim 5 wherein the alternating inverter voltage has a peak-to-peak magnitude substantially equal to the absolute magnitude of the DC supply voltage.

8. The arrangement of claim 5 wherein one of the inverter output terminals is periodically and alternatingly connected with both the DC terminals.

9. The arrangement of claim 5 wherein the potential of one of the inverter output terminals is periodically and alternatingly substantially equal to: (i) the potential of one of the Dc terminals, and (ii) the potential of the other one of the DC terminals.

10. An arrangement comprising:

base means adapted to be inserted into and held by a lamp socket; the lamp socket having a pair of socket terminals whereat is provided a power line voltage; the base means having a pair of base electrodes connected with the socket terminals;

a gas discharge lamp having lamp terminals; and

a circuitry assembly connected between the base electrodes and the lamp terminals; the circuit assembly being operative to provide an AC lamp voltage to the lamp terminals; the AC lamp voltage being of frequency substantially higher than that of the power line voltage; the circuit assembly being characterized by including:

(a) a rectifier circuit connected with the base electrodes and operative to provide a DC supply voltage across a pair of DC terminals;

(b) an inverter circuit connected with the DC terminals and operative to provide an alternating inverter voltage at a pair of inverter output terminals; the peak-to-peak magnitude of the alternating inverter voltage being substantially equal to the magnitude of the DC supply voltage; and

(c) current-limiting and waveshaping circuitry connected between the inverter output terminals and the lamp terminals.

11. The arrangement of claim 10, wherein the absolute peak-to-peak magnitude of the alternating inverter voltage is substantially higher than the absolute peak magnitude of the power line voltage.

12. The arrangement of claim 10 wherein: (a) the inverter circuit is further characterized by including a periodically conducting transistor; (b) the alternating inverter voltage consists of four distinct parts: (i) a first part during which its instantaneous magnitude increases at a substantially constant rate, (ii) a second part during which its instantaneous magnitude remains substantially constant at a relatively high level, (iii) a third part during which its instantaneous magnitude decreases at a substantially constant rate, and (iv) a fourth part during which its instantaneous magnitude remains substantially constant at a relatively low level; and (c) the transistor is prevented from conducting current during most of the first and third periods.

13. The arrangement of claim 12 wherein the duration of the first part equals or exceeds about one tenth of the duration of the second part.

14. The arrangement of claim 10 wherein the inverter circuit includes: (i) a transistor having a pair of transistor output terminals across which the alternating inverter voltage exists and between which a transistor output current periodically flows; and (ii) circuitry functional to prevent the transistor output current from flowing except during periods when the absolute magnitude of any voltage present across the transistor output terminals is lower than half the absolute magnitude of the DC supply voltage.

15. An arrangement comprising:

base means adapted to be inserted into and held by a lamp socket; the lamp socket having a pair of

socket terminals whereat is provided a power line voltage; the base means having a pair of base electrodes connected with the socket terminals;

a gas discharge lamp having a first and a second pair o cathode terminals; and

an electronic ballasting circuit connected between the base electrodes and the cathode terminals; the ballasting circuit being characterized by:

providing a lamp operating voltage of relatively high magnitude between the pairs of cathode terminals and a cathode heating voltage of relatively low magnitude across each pair of cathode terminals; the lamp operating voltage and cathode heating voltage each alternating at a frequency substantially higher than that of the power line voltage; the magnitude of the cathode heating voltage being substantially higher prior to lamp ignition than after lamp ignition.

16. The arrangement of claim 15 wherein the magnitude of the cathode heating voltage is approximately proportional to the magnitude of the lamp operating voltage.

17. The arrangement of claim 15 wherein the electronic ballasting circuit is further characterized by including a periodically conducting transistor across which exists an alternating inverter voltage consisting of four distinct parts: (i) a first part during which its instantaneous magnitude increases at a substantially constant rate, (ii) a second part during which its instantaneous magnitude remains substantially constant at a relatively high level, (iii) a third part during which its instantaneous magnitude decreases at a substantially constant rate, and (iv) a fourth part during which its instantaneous magnitude remains substantially constant at a relatively low level; the transistor being prevented from conducting current during most of the first and third periods.

18. The arrangement of claim 15 wherein the electronic ballasting circuit is further characterized by including: (a) a periodically conducting transistor across which exists an alternating inverter voltage consisting of four distinct parts: (i) a first part during which its instantaneous magnitude increases at a substantially constant rate, (ii) a second part during which its instantaneous magnitude remains substantially constant at a relatively high level, (iii) a third part during which its instantaneous magnitude deceases at a substantially constant rate, and (iv) a fourth part during which its instantaneous magnitude remains substantially constant at a relatively low level; and (b) circuit functional to prevent the transistor conducting current during most of the first and third periods.

* * * * *

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US005341067A

# United States Patent [19]

Nilssen

[11] Patent Number: 5,341,067

[45] Date of Patent: * Aug. 23, 1994

[54] ELECTRONIC BALLAST WITH TRAPEZOIDAL VOLTAGE WAVEFORM

[76] Inventor: Ole K. Nilssen, Caesar Dr., Barrington, Ill. 60010

[*] Notice: The portion of the term of this patent subsequent to Sep. 10, 2008 has been disclaimed.

[21] Appl. No.: 46,171

[22] Filed: Apr. 27, 1993

Related U.S. Application Data

[63] Continuation of Ser. No. 955,229, Oct. 1, 1992, Pat. No. 5,233,270, which is a continuation of Ser. No. 607,271, Oct. 31, 1990, abandoned, which is a continuation-in-part of Ser. No. 787,692, Oct. 15, 1985, abandoned, which is a continuation of Ser. No. 644,155, Aug. 27, 1984, abandoned, which is a continuation of Ser. No. 555,426, Nov. 23, 1983, abandoned, which is a continuation of Ser. No. 178,107, Aug. 14, 1980, abandoned.

[51] Int. Cl.[5] ..... H05B 41/29; H05B 41/36

[52] U.S. Cl. ..... 315/209 R; 315/58; 315/226; 315/307; 315/DIG. 5

[58] Field of Search ..... 315/32, 57, 53, 56, 315/58, 326, DIG. 2, DIG. 5, 209 R, 224, 226, 297, 307, DIG. 4

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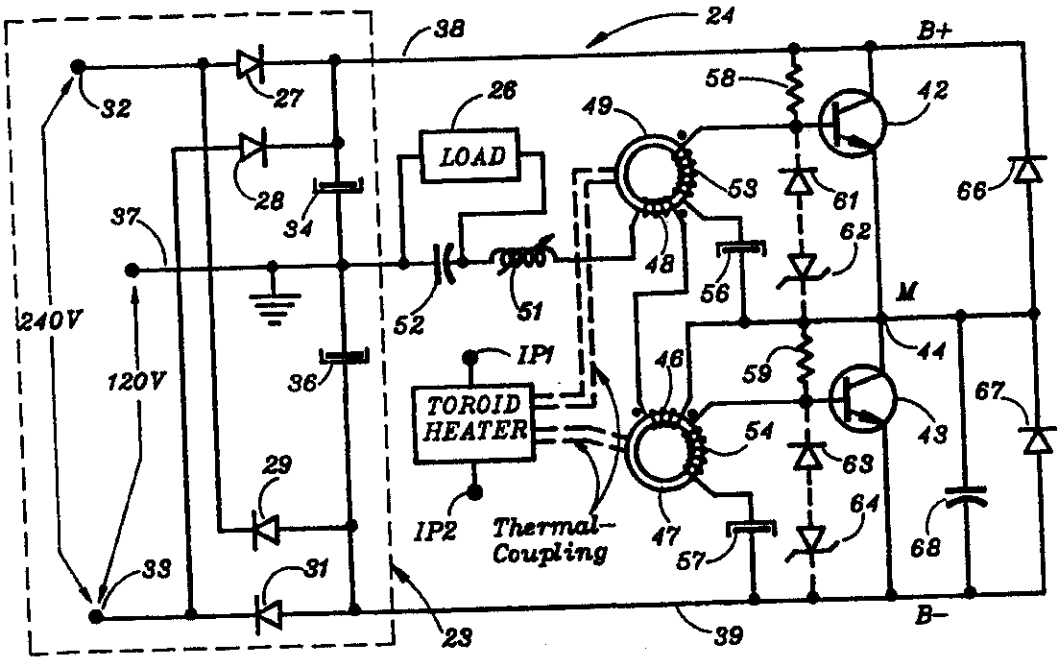
*Primary Examiner*—David Mis

[57] ABSTRACT

An electronic ballast is connected with the AC power line voltage of an ordinary electric utility power line and powers a fluorescent lamp with a substantially sinusoidal current of frequency substantially higher than that or the AC power line voltage. Within the electronic ballast is a half-bridge inverter, whose output voltage exhibits a substantially trapezoidal waveshape. The inverter is powered from a substantially constant DC voltage whose absolute magnitude if substantially higher than the absolute peak magnitude of the AC power line voltage.

59 Claims, 3 Drawing Sheets



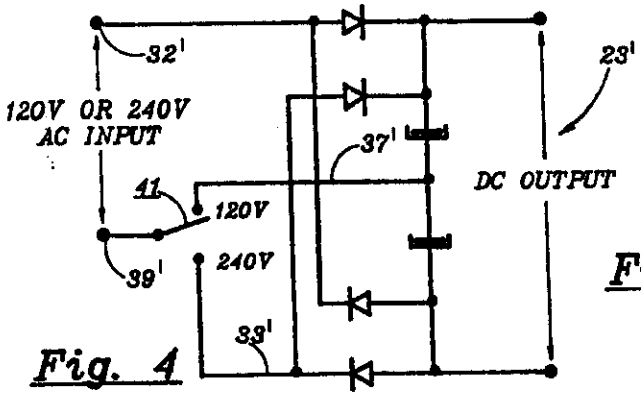



Fig. 4

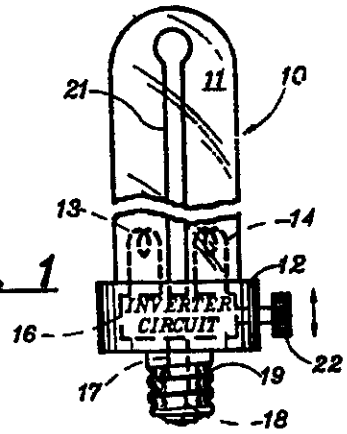



Fig. 1

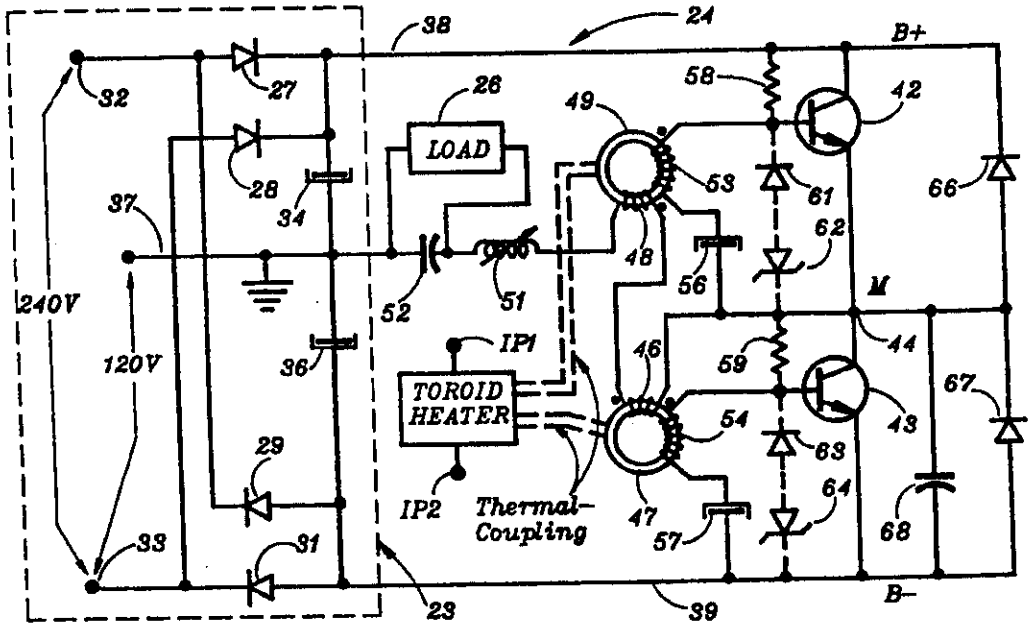



Fig. 2

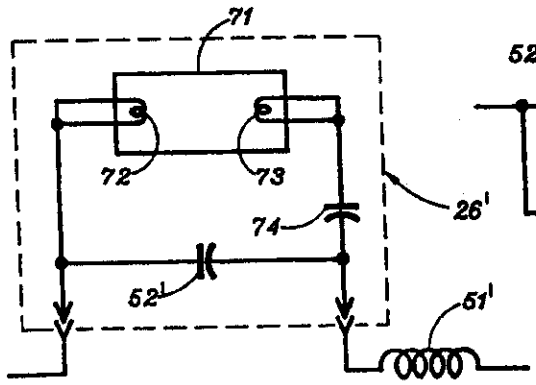



Fig. 5

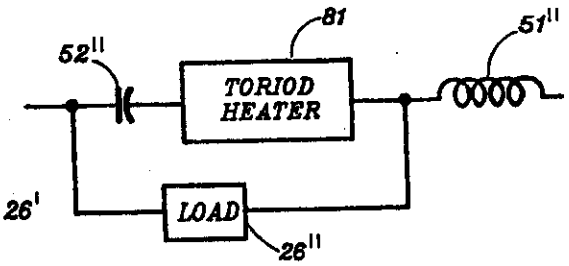



Fig. 6

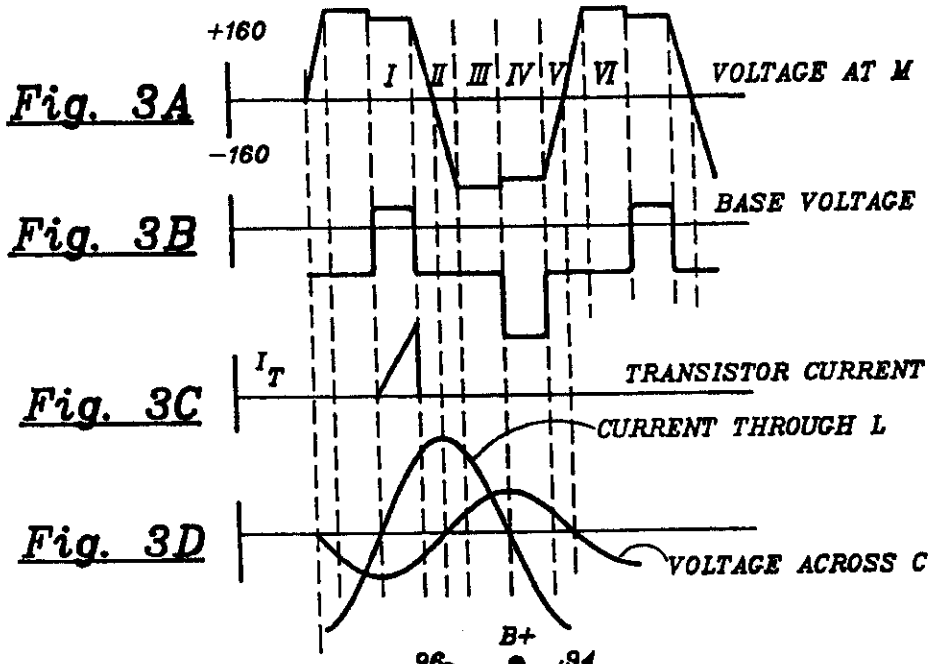



Fig. 3A

Fig. 3B

Fig. 3C

Fig. 3D

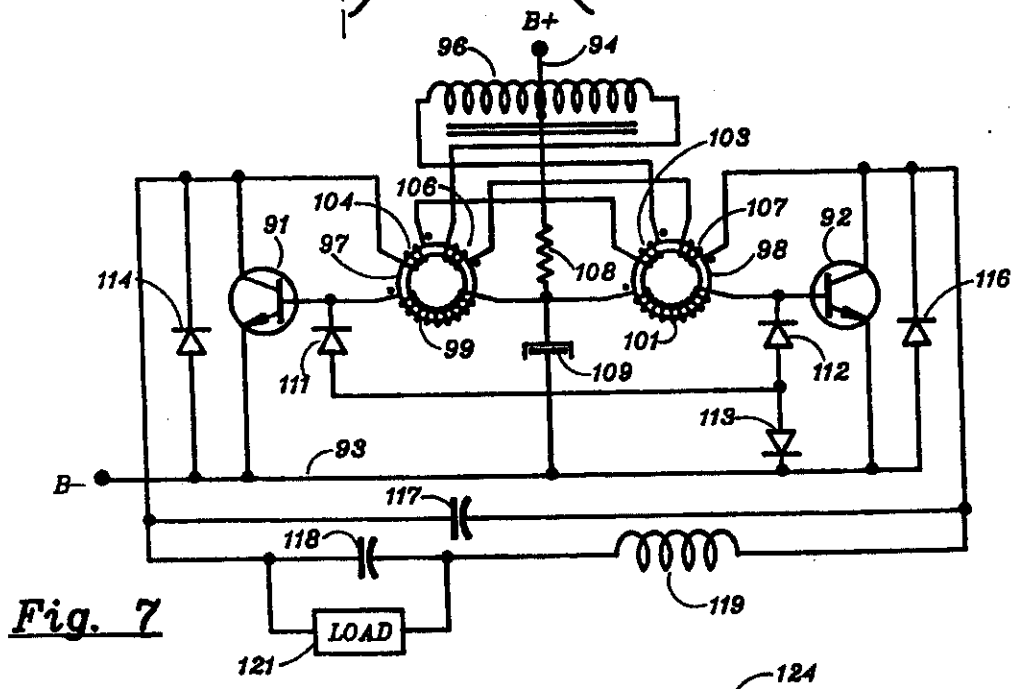



Fig. 7

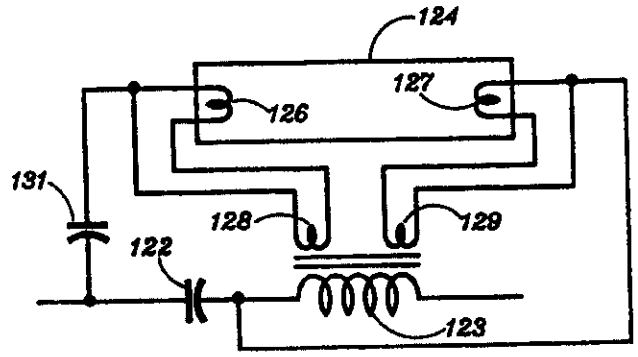
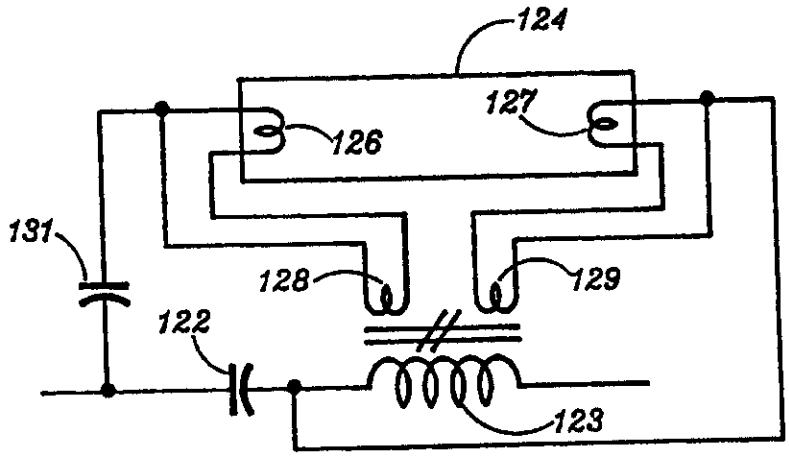



Fig. 8


124
127
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131
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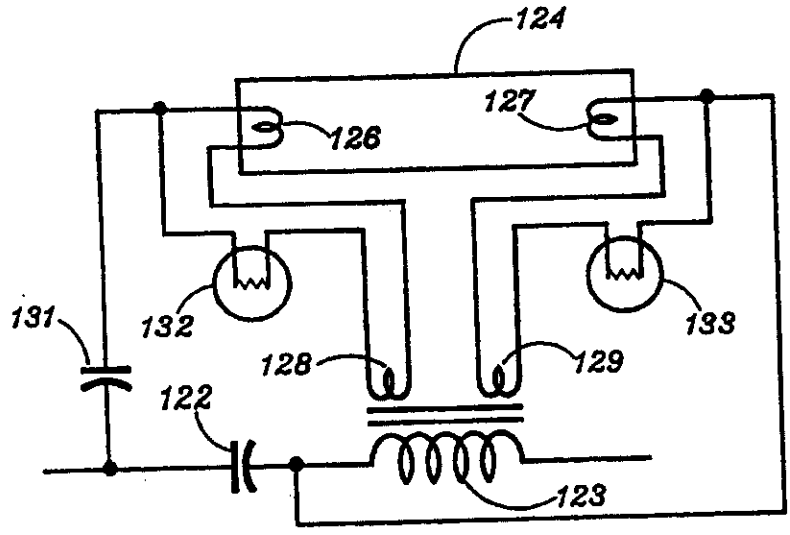
123

Fig. 9


124
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123

Fig. 10

# ELECTRONIC BALLAST WITH TRAPEZOIDAL VOLTAGE WAVEFORM

## RELATED APPLICATIONS

The present application is a continuation of Ser. No. 07/955,229 filed Oct. 01, 1992, now U.S. Pat. No. 5,233,270; which is a continuation of Ser. No. 07/607,271 filed Oct. 31, 1990, now abandoned; which is a continuation-in-part of Ser. No. 06/787,692 filed Oct. 15, 1985, now abandoned; which is a continuation of Ser. No. 06/644,155 filed Aug. 27, 1984, now abandoned; which is a continuation of Ser. No. 06/555,426 filed Nov. 23, 1983, now abandoned; which is a continuation of Ser. No. 06/178,107 filed Aug. 14, 1980, now abandoned.

## BACKGROUND OF THE INVENTION

1. Field of Invention

This invention relates to power supplies suitable for ballasting gas discharge lamps.

2. Description of Prior Art

For a description of pertinent prior art, reference is made to U.S. Pat. No. 4,677,345 to Nilssen; which patent issued from a division of application Ser. No. 06/178,107 filed Aug. 14, 1980; which application is the original progenitor of instant application.

Otherwise, reference is made to the following U.S. Pat. No. 3,263,122 to Genuit; U.S. Pat. No. 3,320,510 to Locklair; U.S. Pat. No. 3,996,493 to Davenport et el.; U.S. Pat. No. 4,100,476 to Ghiringhelli; U.S. Pat. No. 4,262,327 to Kovacik et al.; U.S. Pat. No. 4,370,600 to Zansky; as well as U.S. Pat. Nos. 4,634,932, 4,857,806, 5,047,690, 5,164,637, 5,166,578, 5,185,560, and 5,191,262 to Nilssen.

## SUMMARY OF THE INVENTION

### Objects of the Invention

An object of the present invention is that of providing a self-ballasted screw-in gas discharge lamp.

Another object is that of providing a compact folded fluorescent lamp.

Yet another object is that of providing means for adjusting the light output of gas discharge lamps.

These as well as other objects, features and advantages of the present invention will become apparent from the following description and claims.

### Brief Description

The present invention is directed to providing improved gas discharge lighting means and inverter circuits for powering and controlling gas discharge lamps. The inverter circuits according to the present invention are highly efficient, can be compactly constructed and are ideally suited for energizing gas discharge lamps, particularly compact folded "instant-start" "self-ballasted" fluorescent lamps.

According to one feature of the present invention, a series-connected combination of an inductor and a capacitor is provided in circuit with the inverter transistors to be energized upon periodic transistor conduction. Transistor drive current is preferably provided through the use of at least one saturable inductor to control the transistor inversion frequency to be equal to or greater than the nature resonant frequency of the inductor and capacitor combination. The high voltages efficiently developed by loading the inverter with the inductor and capacitor are ideally suited for energizing external loads such as gas discharge lamps. In such an application, the use of an adjustable inductor permits control of the inverter output as a means of adjusting the level of lamp illumination.



According to another feature of the present invention, reliable and highly efficient half-bridge inverters include a saturable inductor in a current feedback circuit to drive the transistors for alternate conduction. The inverters also include a load having an inductance sufficient to effect periodic energy storage for self-sustained transistor inversion. Importantly, improved reliability is achieved because of the relatively low and transient-free voltages across the transistors in these half-bridge inverters.

Further, according to another feature of the present invention, novel and economical power supplies particularly useful with the disclosed inverter circuits convert conventional AC input voltages to DC for supplying to the inverters.

Yet further, according to still another feature of the invention, a rapid-start fluorescent lamp is powered by way of a series-resonant LC circuit; while heating power for the lamp's cathodes is provided via loosely-coupled auxiliary windings on the tank inductor of the LC circuit. Alternatively, cathode heating power is provided from tightly-coupled windings on the tank inductor; in which case output current-limiting is provided via a non-linear resistance means, such as an incandescent filament in a light bulb, connected in series with the output of each winding.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a front elevation of a folded fluorescent lamp unit adapted for screw-in insertion into a standard Edison incandescent socket;

FIG. 2 is a schematic diagram illustrating the essential features of a push-pull inverter circuit particularly suitable for energizing the lamp unit of FIG. 1;

FIG. 3A-3D is a set of waveform diagrams of certain significant voltages and currents occurring in the circuit of FIG. 2;

FIG. 4 is a schematic diagram of a DC power supply connectable to both 120 and 240 volt AC inputs;

FIG. 5 is a schematic diagram which illustrates the connection of a non-self-ballasted gas discharge lamp unit to the FIG. 2 inverter circuit;

FIG. 6 is a schematic diagram which illustrates the use of a toroid heater for regulation of the inverter output;

FIG. 7 is an alternate form of push-pull inverter circuit accordind to the present invention;

FIG. 8 is a schematic diagram showing the connection of a gas discharge lamp of the "rapid-start" type to an inductor-capacitor-loaded inverter according to the present invention;

FIG. 9 is a modification of FIG. 8, showing loosely-coupled auxiliary windings on the tank inductor; and

FIG. 10 is another modification of FIG. 8, showing non-linear current-limiting means connected with the output of tightly-coupled auxiliary windings on the tank inductor.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 illustrates a screw-in gas discharge lamp unit 10 comprising a folded fluorescent lamp 11 suitably secured to an integral base 12. The lamp comprises two

cathodes 13, 14 which are supplied with the requisite high operating voltage from a frequency-converting power supply and ballasting circuit 16; which, because of its compact size, conveniently fits within the base 12.

The inverter circuit 16 is connected by leads 17, 18 to a screw-type plug 19 adapted for screw-in insertion into a standard Edison-type incandescent lamp socket at which ordinary 120 Volt/60 Hz power line voltage is available. A ground plane comprising a wire or metallic strip 21 is disposed adjacent a portion of the fluorescent lamp 11 as a starting aid. Finally, a manually rotatable external knob 22 is connected to a shaft for mechanical adjustment of the air gap of a ferrite core inductor to vary the inductance value thereof in order to effect adjustment of the inverter voltage output connected to electrodes 13, 14 for controlled variation of the lamp illumination intensity.

With reference to FIG. 2, a power supply 23, connected to a conventional AC input, provides a DC output for supplying a high-efficiency inverter circuit 24. The inverter is operable to provide a high voltage to an external load 26, which may comprise a gas discharge device such as the fluorescent lamp 11 of FIG. 1.

The power supply 23 comprises bridge rectifier having four diodes 27, 28, 29 and 31 connectable to a 248 volt AC supply at terminals 32, 33. Capacitors 34, 36 are connected between a ground line 37 (in turn directly connected to the inverter 24) and to a B+ line 38 and a B− line 39, respectively. The power supply 23 also comprises a voltage doubler and rectifier optionally connectable to a 120 volt AC input taken between the ground line 37 and terminal 33 or 32. The voltage doubler and rectifier means provides a direct electrical connection by way of line 37 netween one of the 120 volt AC power input lines and the inverter 24, as shown in FIG. 2. The bridge rectifier and the voltage doubler and rectifier provide substantially the same DC output voltage to the inverter 24 whether the AC input is 120 or 240 volts. Typical voltages are +160 volts on the B+ line 38 and −160 volts on the B− line 39.

With additional reference to FIG. 4, which shows an alternate power supply 23', the AC input, whether 120 or 240 volts, is provided at terminals 32' and 39. Terminal 39 is in turn connected through a single-pole double-throw selector switch 41 to terminal 37' (for 120 volt operation) or terminal 33' (for 240 volt operation). In all other respects, power supplies 23 and 23' are identical.

The inverter circuit 24 of FIG. 2 is a half-bridge inverter comprising transistors 42, 43 connected in series across the DC voltage output of the power supply 23 on B+ and B− lines 38 and 39, respectively. The collector of trasistor 42 is connected to the B+ line 38, the emitter of transistor 42 and the collector of transistor 43 are connected to a midpoint line 44 (designated "M") and the emitter of transistor 43 is connected to the B− line 39. The midpoint line 44 is in turn connected to the ground line 37 through primary winding 46 of a toroidal saturable core transformer 47, a primary winding 48 on an identical transformer 49, an inductor 51 and a series-connected capacitor 52. The inductor 51 and capacitor 52 are energized upon alternate transistor conduction in a manner to be described later.

An external load 26 is preferably taken off capacitor 52, as shown in FIG. 2. The inductor 51, preferably a known ferrite core inductor, has an inductance variable by mechanical adjustment of the air gap in order to effect variation in the level of the inductor and capacitor voltage and hence the power available to the load, as will be described. When the load is a gas discharge lamp such as lamp 11 in FIG. 1, variation in this inductance upon rotation of knob 22 accomplishes a lamp dimming effect.

Drive current to the base terminals of transistors 42 and 43 is provided by secondary windings 53, 54 of transformers 49, 47, respectively. Winding 53 is also connected to midpoint lead 44 through a bias capacitor 56, while winding 54 is connected to the B− lead 39 through an identical bias capacitor 57. The base terminals of transistors 42 and 43 are also connected to lines 38 and 44 through bias resistors 58 and 59, respectively. For a purpose to be described later, the base of transistor 42 can be optionally connected to a diode 61 and a series Zener diode 64 in turn connected to the midpoint line 44; similarly, a diode 63 and series Zener diode 64 in turn connected to the B− line 39 can be connected to the base of transistor 43. Shunt diodes 66 and 67 are connected across the collector-emitter terminals of transistors 42 and 43, respectively. Finally, a capacitor 68 is connected across the collector-emitter terminals of transistor 43 to restrain the rate of voltage rise across those terminals, as will be seen presently.

The operation of the circuit of FIG. 2 can best be understood with additional reference to FIG. 3, which illustrates significant portions of the waveforms of the voltage at midpoint M (FIG. 3A), the base-emitter voltage on transistor 42 (FIG. 3B), the current through transistor 42 (FIG. 3C), and the capacitor 52 voltage and the inductor 51 current (FIG. 3D).

Assuming that transistor 42 is first to be triggered into conduction, current flows from the B+ line 38 through windings 46 and 38 and the inductor 51 to charge capacitor 52 and returns through capacitor 34 (refer to the time period designated I in FIG. 3). When the saturable inductor 49 saturates at the end of period I, drive current to the base of transistor 42 will terminate, causing voltage on the base of the transistor to drop to the negative voltage stored on the bias capacitor 56 in a manner to be described, causing this transistor to become nonconductive. As shown in FIG. 3c, current-flow in transistor 43 terminates at the end of period I.

Because the current through inductor 51 cannot change instantaneously, current will flow from the B− bus 39 through capacitor 68, causing the voltage at midpoint line 44 to drop to −160 volts (period II in FIG. 3). The capacitor 68 restrains the rate of voltage change across the collector and emitter terminals of transistor 42. The current through the inductor 51 reaches its maximum value when the voltage at the midpoint line 44 is zero. During period III, the current will continue to flow through inductor 51 but will be supplied from the B− bus through the shunt diode 67. It will be appreciated that during the latter half of period II and all of period III, positive current is being drawn from a negative voltage; which, in reality, means that energy is being returned to the power supply through a path of relatively low impedance.

When the inductor current reaches zero at the start of period IV, the current through the primary winding 46 of the saturable inductor 47 will cause a current to flow out of its secondary winding 54 to cause transistor 43 to become conductive, thereby causing a reversal in the direction of current through inductor 51 and capacitor 52. When transformer 47 saturates at the end of period IV, the drive current to the base of transistor 43 terminates and the current through inductor 51 will be supplied through capacitor 68, causing the voltage at mid-

point line 44 to rise (period V). When the voltage at the midpoint line M reaches 160 volts, the current will then flow through shunt diode 66 (period VI). The cycle is then repeated.

As seen in FIG. 3, saturable transformers 47, 49 provide transistor drive current only after the current through inductor 51 has diminished to zero. Further, the transistor drive current is terminated before the current through inductor 51 has reached its maximum amplitude. This coordination of base drive current and inductor current is achieved because of the series-connection between the inductor 51 and the primary windings 46, 48 of saturable transformers 47, 49, respectively.

The series-connected combination of the inductor 51 and the capacitor 52 is energized upon the alternate conduction of transistors 42 and 43. With a large value of capacitance of capacitor 52, very little voltage will be developed across its terminals. As the value of this capacitance is decreased, however, the voltage across this capacitor will increase. As the value of the capacitor 52 is reduced to achieve resonance with the inductor 51, the voltage on the capacitor will rise and become infinite in a loss-free circuit operating under ideal conditions.

It has been found desirable to regulate the transistor inversion frequency, determined mainly by the saturation time of the saturable inductors 47, 49, to be equel to or higher than the natural resonance frequency of the inductor and capacitor combination in order to provide a high voltage output to external load 26. A high voltage across capacitor 52 is efficiently developed as the transistor inversion frequency approaches the natural resonant frequency of the inductor 51 and capacitor 52 combination. Stated another way, the conduction period of each transistor is desirably shorter in duration than one quarter of the full period corresponding to the natural resonant frequency of the inductor and capacitor combination. When the inverter 24 is used with a self-ballasted gas discharge lamp unit, it has been found that the inversion frequency can be at least equal to the natural resonant frequency of the tank circuit. If the capacitance value of capacitor 52 is reduced still further beyond the resonance point, unacceptably high transistor currents will be experienced during transistor switching and transistor burn-out will occur.

It will be appreciated that the sizing of capacitor 52 is determined by the application of the inverter circuit 24. Variation in the values of the capacitor 52 and the inductor 51 will determine the voltages developed in the inductor-capacitor tank circuit. The external load 26 may be connected in circuit with the inductor 51 (by a winding on the inductor, for example) and the capacitor may be omitted entirely. If the combined circuit loading of the inductor 51 and the external load 26 has an effective inductance of value sufficient to effect periodic energy storage for self-sustained transistor inversion, the current feedback provided by the saturable inductors 47,49 will effect alternate transistor conduction without the need for additional voltage feedback. When the capacitor 52 is omitted, the power supply 23 provides a direct electrical connection between one of the AC power input lines and the inverter load circuit.

Because the voltages across transistors 42, 43 are relatively low (due to the effect of capacitors 34, 36), the half-bridge inverter 24 is very reliable. The absence of switching transients minimizes the possibility of transistor burn-out.

The inverter circuit 24 comprises means for supplying reverse bias to the conducting transistor upon saturation of its associated saturable inductor. For this purpose, the capacitors 56 and 57 are charged to negative voltages as a result of reset current flowing into secondary windings 53, 54 from the bases of transistors 42, 43, respectively. This reverse current rapidly turns off a conducting transistor to increase its switching speed and to achieve inverter circuit efficiency in a manner described more fully in my co-pending U.S. patent application Ser. No. 103,624 filed Dec. 14, 1979 and entitled "Bias Control for High Efficiency Inverter Circuit" (now U.S. Pat. No. 4,307,353). The more negative the voltage on the bias capacitors 56 and 57, the more rapidly charges are swept out of the bases of their associated transistors upon transistor turn-off.

When a transistor base-emitter junction is reversely biased, it exhibits the characteristics of a Zener diode having a reverse breakdown voltage on the order of 8 to 14 Volt for transistors typically used in high-voltage inverters. As an alternative, to provide a negative voltage smaller in magnitude on the base lead of typical transistor 42 during reset operation, the optional diode 61 and Zener diode 62 combination can be used. For large values of the bias capacitor 56, the base voltage will be substantially constant.

If the load 26 comprises a gas discharge lamp, the voltage across the capacitor 52 will be reduced once the lamp is ignited to prevent voltages on the inductor 51 and the capacitor 52 from reaching destructive levels. Such a lamp provides an initial time delay during which a high voltage, suitable for instant starting, is available.

FIG. 5 illustrates the use of an alternate load 26' adapted for plug-in connection to an inverter circuit such as shown in FIG. 2. The load 26' consists of a gas discharge lamp 71 having electrodes 72, 73 and connected in series with a capacitor 74. The combination of lamp 71 and capacitor 74 is connected in parallel with a capacitor 52' which serves the same purpose as capacitor 52 in the FIG. 2 circuit. However, when the load 26' is unplugged from the circuit, the inverter stops oscillating and the development of high voltages in the inverter is prevented. The fact that no high voltages are generated by the circuit if the lamp is disconnected while the circuit is oscillating is important for safety reasons.

FIG. 6 illustrates a capacitor 52" connected in series with an inductor 51" through a heater 81 suitable for heating the toroidal inductors 47, 49 in accordance with the level of output. The load 26" is connected across the series combination of the capacitor 52" and the toroid heater. The heater 81 is preferably designed to controllably heat the toroidal saturable inductors in order to decrease their saturation flux limit and hence their saturation time. The result is to decrease the periodic transistor conduction time and thereby increase the transistor inversion frequency. When a frequency-dependent impedance means, that is, an inductor or a capacitor, is connected in circuit with the AC voltage output of the inverter, change in the transistor inversion frequency will modify the impedance of the frequency-dependent impdance means and correspondingly modify the inverter output. Thus as the level of the output increases, the toroid heater 81 is correspondingly energized to effect feedback regulation of the output. Further, transistors 42, 43 of the type used in high voltage inverters dissipate heat during periodic transistor conduction. As an alternative, the toroid heater 81 can use this heat for

feedback regulation of the output or control of the temperature of transistors 42, 43.

The frequency dependent impedance means may also be used in a circuit to energize a gas discharge lamp at adjustable illumination levels. Adjustment in the inversion frequency of transistors 42, 43 results in control of the magnitude of the AC current supplied to the lamp. This is preferably accomplished where saturable inductors 47, 49 have adjustable flux densities for control of their saturation time.

FIG. 7 schematically illustrates an alternate form of inverter circuit, shown without the AC to DC power supply connections for simplification. In this Figure, the transistors are connected in parallel rather than in series but the operation is essentially the same as previously described.

In particular, this circuit comprises a pair of alternately conducting transistors 91, 92. The emitter terminals of the transistors are connected to a B− line 93. A B+ lead 94 is connected to the center-tap of a transformer 96. In order to provide drive current to the transistors 91, 92 for control of their conduction frequency, saturable inductors 97, 98 have secondary windings 99, 101, respectively, each secondary winding having one end connected to the base of its associated transistor; the other ends are connected to a common terminal 102. One end of transformer 96 is connected to the collector of transistor 91 through a winding 103 on inductor 98 in turn connected in series with a winding 104 on inductor 97. Likewise, the other end of transformer 96 is connected to the collector of transistor 92 through a winding 106 on inductor 97 in series with another winding 107 on inductor 98.

The B+ terminal is connected to terminal 102 through a bias resistor 108. A bias capacitor 109 connects terminal 102 to the B− lead 93. This resistor and capacitor serve the same function as resistors 58, 59 and capacitors 56, 57 in the FIG. 2 circuit.

The bases of transistors 91, 92 are connected by diodes 111, 112, respectively, to a common Zener diode 113 in turn connected to the B− lead 93. The common Zener diode 113 serves the same function as individual Zener diodes 62, 64 in FIG. 2.

Shunt diodes 114, 116 are connected across the collector-emitter terminals of transistors 91, 92, respectively. A capacitor 117 connecting the collectors of transistors 91, 92 restrains the rate of voltage rise on the collectors in a manner similar to the collector-emitter capacitor 68 in FIG. 2.

Inductive-capacitive loading of the FIG. 7 inverter is accomplished by a capacitor 118 connected in series with with an inductor 119, the combination being connected across the collectors of the transistors 91, 92. A load 121 is connected across the capacitor 118.

FIG. 8 illustrates how an inverter loaded with a series capacitor 122 and inductor 123 can be used to energize a "rapid-start" fluorescent lamp 124 (the details of the inverter circuit being omitted for simplication). The lamp 124 has a pair of cathodes 126, 127 connected across the capacitor 122 for supply of operating voltage in a manner identical to that previously described. In addition, the inductor 123 comprises a pair of magnetically-coupled auxiliary windings 128, 129 for electrically heating the cathodes 126, 127, respectively. A small capacitor 131 is connected in series with lamp 124.

FIG. 9 illustrates the very same circuit arrangement as that of FIG. 8 except that the auxiliary windings 128, 129 are only loosely coupled to the inductor 123, thereby providing for a manifest limitation on the amount of current that can be drawn from each auxiliary winding in case it were to be accidentally short-circuited.

FIG. 18 also illustrates the very same circuit arrangement as that of FIG. 8 except that the cathodes 126, 127 are connected with their respective auxiliary windings 128, 129 by way of non-linear current-limiting means 132 and 133, respectively.

In FIG. 10, the non-linear current-limiting means 132, 133 are shown as being two (small) incandescent lamps. However, other types of non-linear resistance means could be used as well.

Both the FIG. 9 circuit and the FIG. 10 circuit serve the same basic purpose; which is that of preventing damage to the ballast circuit (such as that if FIG. 2) in case the leads used for connecting to one of the lamp cathodes 126, 127 were to be accidentally shorted. This damage prevention is accomplished by providing for manifest limitation of the maximum amount of current that can be drawn from each one of the auxiliary windings 128, 129. In the circuit of FIG. 9, this manifest limitation is accomplished by having the auxiliary windings 128, 129 couple sufficiently loosely to the main inductor 123—such as by providing a magnetic shunt between inductor 123 and the auxiliary windings—thereby correspondingly limiting the degree of impact resulting from an accidental short circuit. Such a short circuit would result in a net reduction in the effective inductance value of the tank inductor 123; which net reduction in inductance may in turn cause a precipitous increase in the magnitude of the reactive current drawn from the inverter by the series-connected inductor 123 and capacitor 122, thereby causing damage to the inverter.

## ADDITIONAL EXPLANATIONS AND COMMENTS

(a) With reference to FIGS. 2 and 5, adjustment of the amount of power supplied to load 26', and thereby the amount of light provided by lamp 71, may be accomplished by applying a voltage of adjustable magnitude to input terminals IP1 and IP2 of the Toroid Heater; which is thermally coupled with the toroidal ferrite cores of saturable transformers 47, 49.

(b) With commonly available components, inverter circuit 24 of FIG. 2 can be made to operate efficiently at any frequency between a few kHz to perhaps as high as 50 kHz. However, for various well-known reasons (i.e., eliminating audible noise, minimizing physical size, and maximizing efficiency), the frequency actually chosen is in the range of 20 to 48 kHz.

(c) The fluorescent lighting unit of FIG. 1 could be made in such manner as to permit fluorescent lamp 11 to be disconnectable from its base 12 and ballasting means 16. However, if powered with normal line voltage without its lamp load connected, frequency-converting power supply and ballasting circuit 16 is apt to self-destruct.

To avoid such self-destruction, arrangements can readily be made whereby the very act of removing the load automatically establishes a situation that prevents the possible destruction of the power supply and ballasting means. For instance, with the tank capacitor (52) being permanently connected with the lamp load (11)—thereby automatically being removed whenever the lamp is removed—the inverter circuit is protected from self-destruction.

(d) At frequencies above a few kHz, the load represented by a fluorescent lamp—once it is ignited—is substantially resistive. Thus, with the voltage across lamp **11** being of a substantially sinusoidal waveform (as indicated in FIG. 3*d*), the current through the lamp will also be substantially sinusoidal in waveshape.

(e) In the fluorescent lamp unit of FIG. **1**, fluorescent lamp **11** is connected with power supply and ballasting circuit **16** in the exact same manner as is load **26** connected with the circuit of FIG. **2**. That is, it is connected in parallel with the tank capacitor (52) of the L-C series-resonant circuit. As is conventional in instant-start fluorescent lamps—such as lamp **11** of FIG. **1**—the two terminals from each cathode are shorted together, thereby to constitute a situation where each cathode effectively is represented by only a single terminal. However, it is not necessary that the two terminals from each cathode be shorted together; in which case—for instant-start operation—connection from a lamp's power supply and ballasting means need only be made with one of the terminals of each cathode.

(f) With respect to the circuit arrangement of FIG. **9**, in situations where the tank inductor **123** includes a ferrite magnetic core having an air gap, one particularly cost-effective way of accomplishing the indicated loose coupling between the tank inductor **123** and the auxiliary windings **128, 129** is that of arranging for the auxiliary windings to be placed in the air gap in such a manner that they each couple only with part of the magnetic flux crossing the air gap.

(g) It is thought that the present invention and many of its attendant advantages will be understood from the foregoing description and that many changes may be made in the form and construction of its components parts, the form described being merely a preferred embodiment of the invention.

I claim:

**1.** An arrangement comprising:

a source operative to provide an AC power line voltage at a pair of AC terminals;

a gas discharge lamp having a pair of lamp terminals; and

a circuit assembly connected between the AC terminals and the lamp terminals; the circuit assembly being operative to provide a lamp current to the lamp terminals; the lamp current having a substantially sinusoidal waveshape and being of frequency substantially higher than that of the AC power line voltage; the circuit assembly being characterized by including:

(a) rectifying and filtering circuitry connected with the AC terminals and operative to provide a substantially constant DC supply voltage across a pair of DC terminals; the absolute magnitude of the DC supply voltage being significantly higher than the absolute peak magnitude of the AC power line voltage;

(b) inverter circuitry connected with the DC terminals and operative to provide a periodic inverter voltage at a pair of inverter terminals; and

(c) current-limiting circuitry connected between the inverter terminals and the lamp terminals.

**2.** The arrangement of claim **1** wherein there exists an electrically conductive path between one of the DC terminals and one of the AC terminals.

**3.** An arrangement comprising:

a source operative to provide an AC power line voltage at a pair of AC terminals;

a gas discharge lamp having lamp terminals; and

a circuit assembly connected between the AC terminals and the lamp terminals; the circuit assembly being operative to provide a lamp current to the lamp terminals; the lamp current having a substantially sinusoidal waveshape and being of frequency substantially higher than that of the AC power line voltage; the circuit assembly being characterized by including:

(a) rectifying and filtering circuitry connected with the AC terminals and operative to provide a substantially constant DC supply voltage across a pair of DC terminals;

(b) inverter circuitry connected with the DC terminals and operative to provide a periodic inverter voltage between a reference terminal and an inverter output terminal; the periodic inverter voltage having a fundamental period as well as an instantaneous magnitude; each complete fundamental period consisting of four distinct sub-periods: (i) a first sub-period during which the instantaneous magnitude increases at a first rate; (ii) a second sub-period during which the instantaneous magnitude remains substantially constant at a relatively high level; (iii) a third sub-period during which the instantaneous magnitude decreases at a second rate, the second rate being substantially equal to the first rate; and (iv) a fourth sub-period during which the instantaneous magnitude remains substantially constant at a relatively low level; the inverter circuitry being characterized by including a periodically conducting transistor conducting current during a significant part of the second sub-period but only during a small part of the first sub-period; and

(c) current-limiting circuitry connected between the inverter output terminal and the lamp terminals.

**4.** An arrangement comprising:

a source operative to provide an AC power line voltage at a pair of AC terminals;

a gas discharge lamp having lamp terminals; and

a circuit assembly interposed between the AC terminals and the lamp terminals; the circuit assembly supplying to the lamp terminals a lamp current of frequency substantially higher than that of the AC power line voltage; the circuit assembly being further characterized by including:

(a) rectifier circuitry connected with the AC terminals and operative to provide a substantially constant DC supply voltage across a pair of DC terminals;

(b) inverter circuitry connected with the DC terminals and operative to provide a periodic inverter voltage at a pair of inverter terminals; the periodic inverter voltage has a periodically varying instantaneous magnitude as well as a complete fundamental period consisting of (i) a first sub-period during which the instantaneous magnitude changes at a positive rate-of-change, (ii) a second sub-period during which the instantaneous magnitude remains substantially constant at a relatively high level, (iii) a third sub-period during which the instantaneous magnitude changes at a negative rate-of-change, and (iv) a fourth sub-period during which the instantaneous magnitude remains substantially constant

at a relatively low level; the duration of the second sub-period is substantially equal to that of the fourth sub-period; the duration of the first sub-period is substantially equal to that of the third sub-period; the duration of the first sub-period is substantially shorter than that of the second sub-period; the inverter circuitry is further characterized by including a transistor having a pair of transistor output terminals (e.g., a collector terminal and an emitter terminal) across which exists a transistor voltage and between which periodically flows a transistor current, but only at times when the absolute magnitude of the transistor voltage is lower than half that of the DC supply voltage; and

(c) current-limiting circuitry connected between the inverter terminals and the lamp terminals.

5. An arrangement comprising:

a source operative to provide an AC power line voltage between a pair of AC terminals;

a gas discharge lamp having a pair of lamp terminals; and

an assemblage of interconnected electronic components connected in circuit between the AC terminals and the lamp terminals; the assemblage being operative to cause a lamp current to be supplied to the lamp terminals; the lamp current being of frequency substantially higher than that of the AC power line voltage; the assemblage being further characterized by including:

(a) rectifying and filtering circuitry connected with the AC terminals and operative to provide a substantially constant DC supply voltage across a pair of DC terminals; and

(b) inverting and ballasting circuitry connected between the DC terminals and the lamp terminals; the inverting and ballasting circuitry being characterized by providing across a pair of circuit terminals a periodic inverter voltage having a fundamental period as well as an instantaneous magnitude; each fundamental period consisting of four distinct sub-periods: (i) a sub-period A during which the instantaneous magnitude increases at a substantially constant rate; (ii) a sub-period B during which the instantaneous magnitude remains substantially constant at a relatively high level; (iii) a sub-period C during which the instantaneous magnitude decreases at a substantially constant rate; and (iv) a sub-period D during which the instantaneous magnitude remains substantially constant at a relatively low level; the inverting and ballasting circuitry also being characterized by including a periodically conducting transistor; the transistor conducting current during at least a part of sub-period B, but not during at least a part of sub-period C.

6. The arrangement of claim 5 wherein the DC supply voltage has a substantially constant absolute magnitude that is distinctly higher than the peak absolute magnitude of the AC power line voltage.

7. The arrangement of claim 6 wherein the DC supply voltage attains its substantially constant absolute magnitude within a brief period after the AC power line voltage is initially caused to be provided across the pair of AC terminals.

8. The arrangement of claim 7 wherein the duration of the brief period is shorter than the duration of ten complete cycles of the AC power line voltage.

9. The arrangement of claim 8 wherein the duration of the brief period is no longer than the duration of a single complete period of the AC power line voltage.

10. The arrangement of claim 6 wherein, internally of said assemblage, there exists an electrically conductive path between one of the DC terminals and one of the AC terminals.

11. The arrangement of claim 5 wherein said transistor does not conduct current during most of the complete duration of sub-period C.

12. An arrangement comprising:

a source operative to provide an AC power line voltage at a pair of AC terminals;

a gas discharge lamp having a pair of lamp terminals; and

an assemblage of interconnected electronic components connected in circuit between the AC terminals and the lamp terminals; the assemblage being operative to cause a lamp current to be supplied to the lamp terminals; the lamp current being of frequency substantially higher than that of the AC power line voltage; the assemblage being further characterized by including:

(a) rectifying and filtering circuitry connected with the AC terminals and operative to provide a substantially constant DC supply voltage across a pair of DC terminals; the substantially constant DC supply voltage having a steady-state absolute magnitude; the steady-state absolute magnitude being significantly higher than the absolute peak magnitude of the AC power line voltage; the DC supply voltage attaining its steady-state absolute magnitude within a brief period after the AC power line voltage is initially provided at the AC terminals; the duration of the brief period being no longer than the duration of ten complete cycles of the AC power line voltage; and

(b) inverting and ballasting circuitry connected between the DC terminals and the lamp terminals; the inverting and ballasting circuitry being operative to supply said lamp current to the lamp terminals.

13. The arrangement of claim 12 wherein, within the assemblage, there exists an electrically conductive path between one of the DC terminals and one of the AC terminals.

14. The arrangement of claim 12 wherein the brief period is no longer than about 50 milli-seconds.

15. An arrangement comprising:

a source operative to provide an AC power line voltage at a pair of AC terminals;

a gas discharge lamp having a pair of lamp terminals; and

an assemblage of interconnected electronic components connected in circuit between the AC terminals and the lamp terminals; the assemblage being operative to cause a lamp current to be supplied to the lamp terminals; the lamp current being of frequency substantially higher than that of the AC power line voltage; the assemblage being further characterized by including:

(a) rectifying and filtering circuitry connected with the AC terminals and operative to provide a DC supply voltage across a pair of DC terminals; and

(b) inverting and ballasting circuitry connected between the DC terminals and the lamp terminals; the inverting and ballasting circuitry being operative to supply said lamp current to the lamp

terminals; the inverting and ballasting circuitry being further characterized by including a periodically conducting transistor; the transistor being characterized by having a pair of control terminals (e.g., a base terminal and an emitter terminal) between which exists a control voltage varying periodically between a minimum voltage level and a maximum voltage level; the absolute magnitude of the difference between the maximum voltage level and the minimum voltage level being substantially higher than twice the absolute magnitude of the forward voltage drop of an ordinary semiconductor junction diode; the periodic control voltage being of the same frequency as that of the lamp current; the forward voltage drop of an ordinary semiconductor junction diode being about 0.7 Volt.

16. The arrangement of claim 15 wherein the absolute magnitude of the difference between the maximum voltage level and the minimum voltage level is higher than 2.0 Volt.

17. The arrangement of claim 15 wherein the average absolute magnitude of the DC supply voltage is distinctly larger than the peak absolute magnitude of the AC power line voltage.

18. The arrangement of claim 16 wherein, by way of the assemblage, there exists an electrically conductive path between one of the DC terminals and one of the AC terminals.

19. An arrangement comprising:

a source operative to provide an AC power line voltage between a pair of AC terminals;

a gas discharge lamp having a pair of lamp terminals; and

an assemblage of interconnected electronic components connected in circuit between the AC terminals and the lamp terminals; the assemblage being operative to cause a lamp current to be supplied to the lamp terminals; the lamp current being of frequency substantially higher than that of the AC power line voltage; the assemblage being further characterized by including:

(a) rectifying and filtering circuitry connected with the AC terminals and operative to provide a substantially constant DC supply voltage across a pair of DC terminals; and

(b) inverting and ballasting circuitry connected between the DC terminals and the lamp terminals; the inverting and ballasting circuitry being characterized by providing across a pair of circuit terminals a periodic inverter voltage having a fundamental period as well as an instantaneous magnitude; each fundamental period consisting of four distinct sub-periods: (i) sub-period A during which the instantaneous magnitude increases in a substantially continuous manner; (ii) sub-period B during which the instantaneous magnitude remains substantially constant at a relatively high level; (iii) sub-period C during which the instantaneous magnitude decreases in a substantially continuous manner; and (iv) sub-period D during which the instantaneous magnitude remains substantially constant at a relatively low level; the inverting and ballasting circuitry being further characterized by including a periodically conducting first transistor; the first transistor conducting current during at least a substantial part of sub-period B, but not conducting current during at least a substantial part of sub-period C.

20. The arrangement of claim 19 wherein the inverting and ballasting circuitry is still further characterized by including a periodically conducting second transistor; the second transistor conducting current during at least a substantial part of sub-period D, but not conducting current during at least a substantial part of sub-period A.

21. The arrangement of claim 20 wherein the second transistor is not conducting current during most of the complete duration of sub-period A.

22. The arrangement of claim 20 wherein: (i) the first transistor and the second transistor are series-connected across the DC terminals; and (ii) the absolute value of the peak-to-peak magnitude of the first periodic inverter voltage is higher than that of the peak magnitude of the AC power line voltage.

23. The arrangement of claim 19 wherein the first transistor has a first pair of control input terminals (e.g., a base terminal and an emitter terminal) between which exists a control voltage varying periodically between a minimum voltage level and a maximum voltage level; the absolute magnitude of the difference between the maximum voltage level and the minimum voltage level being substantially higher than twice the absolute magnitude of the forward voltage drop of an ordinary semiconductor junction diode; the control voltage being of the same frequency as that of the lamp current; the forward voltage drop of an ordinary semiconductor junction diode being about 0.7 Volt.

24. An arrangement comprising:

a source operative to provide an AC power line voltage between a pair of AC terminals;

a gas discharge lamp having a pair of lamp terminals; and

a power conditioning circuit having: (i) power input terminals connected with the AC terminals, and (ii) power output terminals connectable with the lamp terminals; the power conditioning circuit being functional, as long as the lamp terminals are indeed connected with the power output terminals, to properly power the gas discharge lamp; the power conditioning circuit being further characterized by:

(a) having a first pair of terminals between which exists a first voltage whose magnitude varies in a periodic pattern; the periodic pattern having a fundamental period consisting of four sub-periods: (i) sub-period A during which the magnitude of the first voltage increases at a first rate; (ii) sub-period B during which the magnitude of the first voltage remains substantially constant at a relatively high level; (iii) sub-period C during which the magnitude of the first voltage decreases at a second rate; and (iv) sub-period D during which the magnitude of the first voltage remains substantially constant at a relatively low level, where sub-period D preceeds a next sub-period A; and

(b) having a periodically conducting transistor; the transistor conducting current during at least part of each sub-period D, but not during at least a part of each sub-period A.

25. The arrangement of claim 24 wherein the power conditioning circuit is additionally characterized by:

(c) having a second pair of terminals between which exists a DC voltage whose absolute magnitude is distinctly higher than the peak absolute magnitude

of the AC power line voltage; there being, within the power conditioning circuit, an electrically conductive path between one of the second pair of terminals and one of the power input terminals.

26. The arrangement of claim 24 wherein the power conditioning circuit is additionally characterized in that the transistor has a pair of control terminals between which exists a control voltage varying periodically between a minimum voltage level and a maximum voltage level; the absolute magnitude of the difference between the maximum voltage level and the minimum voltage level being clearly higher than two Volts.

27. The arrangement of claim 24 wherein the power conditioning circuit is additionally characterized by providing between its power output terminals an alternating voltage having a substantially sinusoidal waveform.

28. The arrangement of claim 24 wherein the power conditioning circuit is additionally characterized by providing between its power output terminals an alternating voltage having: (i) a first fundamental frequency whenever the gas discharge lamp is indeed being properly powered, and (ii) a second fundamental frequency whenever the gas discharge lamp is not connected with the power output terminals; the first fundamental frequency being clearly lower than the second fundamental frequency.

29. The arrangement of claim 24 wherein the power conditioning circuit is additionally characterized by supplying to the gas discharge lamp an alternating current having a substantially sinusoidal waveform.

30. An arrangement comprising:

a source operative to provide an AC power line voltage between a pair of AC terminals;

a gas discharge lamp having a pair of lamp terminals; and

a power conditioning circuit having: (i) power input terminals connected with the AC terminals, and (ii) power output terminals connectable with the lamp terminals; the power conditioning circuit being functional, as long as the lamp terminals are indeed connected with the power output terminals, to properly power the gas discharge lamp; the power conditioning circuit being further characterized by including a first and a second transistor series-connected across a pair of DC terminals; each transistor having a pair of transistor output terminals across which exists a transistor output voltage; the transistor output voltage varying periodically between a minimum voltage level and a maximum voltage level; the absolute magnitude of the difference between the maximum voltage level and the minimum voltage level being substantially equal to the absolute magnitude of a substantially constant DC voltage existing across the DC terminals; the absolute magnitude of the DC voltage being distinctly higher than the absolute peak magnitude of the AC power line voltage.

31. The arrangement of claim 30 wherein, within the power conditioning circuit, there exists an electrically conductive path between one of the DC terminals and one of the power input terminals.

32. An arrangement comprising:

a source operative to provide an AC power line voltage between a pair of AC terminals;

a gas discharge lamp having a pair of lamp terminals; and

a power conditioning circuit having: (i) power input terminals connected with the AC terminals, and (ii) power output terminals connectable with the lamp terminals; the power conditioning being functional, as long as the lamp terminals are indeed connected with the power output terminals, to properly power the gas discharge lamp; the power conditioning circuit being further characterized by:

(a) including a transistor having a pair of transistor output terminals across which exists a transistor output voltage whose magnitude varies in accordance with a periodic waveform; the periodic waveform having a fundamental period consisting of four sub-periods: (i) sub-period A during which the magnitude of the transistor output voltage increases at a first rate, sub-period A having a first duration, (ii) sub-period B during which the magnitude of the transistor output voltage remains substantially constant at a relatively high level, sub-period B having a second duration, (iii) sub-period C during which the magnitude of the transistor output voltage decreases at a second rate, sub-period C having a third duration, and (iv) sub-period D during which the magnitude of the transistor output voltage remains substantially constant at a relatively low level, sub-period D having a fourth duration; sub-period D preceeding a next sub-period A; and

(b) having a pair of DC terminals between which exists a DC voltage whose absolute magnitude is substantially constant and distinctly higher than the peak absolute magnitude of the AC power line voltage.

33. The arrangement of claim 32 wherein, within the power conditioning circuit, there exists an electrically conductive path between one of the pair of DC terminals and one of the power input terminals.

34. The arrangement of claim 32 wherein the second duration is distinctly shorter than half the duration of the complete fundamental period.

35. The arrangement of claim 32 wherein the second duration is distinctly longer than one quarter of the duration of the complete fundamental period.

36. The arrangement of claim 32 wherein the transistor has a pair of control terminals between which exists a control voltage having a magnitude alternating periodically between being above and being below a certain level; the transistor being characterized in that it is operative to conduct current only as long as the magnitude is above the certain level; the magnitude being above the certain level only during a certain part of the fourth duration; the certain part being clearly shorter in duration than the fourth duration.

37. The arrangement of claim 36 wherein the control signal includes an alternating voltage component having peak-to-peak magnitude in excess of 2.0 Volts.

38. The arrangement of claim 32 wherein the power conditioning circuit is additionally characterized in that: (i) a transistor current flows between the transistor output terminals; (ii) the transistor current flows during at least a part of sub-period D; and (iii) the transistor current ceases to flow clearly before the end of the immediately following sub-period A.

39. The arrangement of claim 32 wherein the power conditioning circuit is additionally characterized in that: (i) a forward transistor current flows between the transistor output terminals during each sub-period D,

but only for a certain total duration; and (ii) the magnitude of the forward transistor current increases during most of said certain total duration.

40. The arrangement of claim 32 wherein the power conditioning circuit is additionally characterized in that a forward transistor current flows between the transistor output terminals during each fundamental period, but only during a certain part of the total duration of such fundamental period; the certain part being distinctly shorter than half the duration of the complete fundamental period.

41. The arrangement of claim 40 where said certain part is distinctly shorter than 90 percent of half the duration of the complete fundamental period.

42. The arrangement of claim 32 wherein the power conditioning circuit is additionally characterized in that: (i) the sum of the fourth and first durations is designated a complete half-cycle-duration; and (ii) a forward transistor current flows between the transistor output terminals only during a certain fraction of each complete half-cycle-duration, which certain fraction is distinctly shorter than 90 percent of the complete half-cycle-duration.

43. The arrangement of claim 42 wherein the magnitude of the forward transistor current increases throughout all of the certain fraction of each complete half-cycle-duration.

44. The arrangement of claim 32 wherein the power conditioning circuit is additionally characterized in that: (i) the sum of the fourth and first durations is designated a complete half-cycle-duration; (ii) a transistor current flows between the transistor output terminals only during a certain part of each complete half-cycle-duration; and (iii) the magnitude of the transistor current increases during most of said certain part.

45. The arrangement of claim 44 wherein the magnitude of the transistor current increases throughout said certain part.

46. An arrangement comprising:

a source operative to provide an AC power line voltage between a pair of AC terminals;

a gas discharge lamp having a pair of lamp terminals; and

a power conditioning circuit having: (i) power input terminals connected with the AC terminals, and (ii) power output terminals connectable with the lamp terminals; the power conditioning circuit being functional, as long as the lamp terminals are indeed connected with the power output terminals, to properly power the gas discharge lamp; the power conditioning circuit being further characterized by:

(a) including a transistor having a pair of transistor output terminals across which exists a transistor output voltage whose magnitude varies in accordance with a periodic waveform; the periodic waveform having a fundamental period consisting of four sub-periods:

(i) sub-period A during which the magnitude of the transistor output voltage increases at a first rate; sub-period A having a first duration;

(ii) sub-period B during which the magnitude of the transistor output voltage remains substantially constant at a relatively high level; sub-period B having a second duration;

(iii) sub-period C during which the magnitude of the transistor output voltage decreases at a second rate; sub-period C having a third duration; and

(iv) sub-period D during which the magnitude of the transistor output voltage remains substantially constant at a relatively low level; sub-period D having a fourth duration; sub- period D preceeding a next sub-period A; and

(b) with the sum of the fourth duration and the first duration being designated as a total half-cycle-duration, having a forward transistor current flowing between the transistor output terminals only during a certain fraction of each total half-cycle-duration; the certain fraction being distinctly shorter than 90 percent of the complete half-cycle-duration.

47. An arrangement comprising:

a source operative to provide an AC power line voltage between a pair of AC terminals;

a gas discharge lamp having a pair of lamp terminals; and

a power conditioning circuit having: (i) power input terminals connected with the AC terminals, and (ii) power output terminals connectable with the lamp terminals; the power conditioning circuit being functional, as long as the lamp terminals are indeed connected with the power output terminals, to properly power the gas discharge lamp; the power conditioning circuit being further characterized by:

(a) including a transistor having a pair of transistor output terminals across which exists a transistor output voltage whose magnitude varies in accordance with a periodic waveform; the periodic waveform having a fundamental period consisting of four sub-periods:

(i) sub-period A during which the magnitude of the transistor output voltage increases at a first rate; sub-period A having a first duration;

(ii) sub-period B during which the magnitude of the transistor output voltage remains substantially constant at a relatively high level; sub-period B having a second duration;

(iii) sub-period C during which the magnitude of the transistor output voltage decreases at a second rate; sub-period C having a third duration; and

(iv) sub-period D during which the magnitude of the transistor output voltage remains substantially constant at a relatively low level; sub-period D having a fourth duration; sub-period D preceeding a next sub-period A; and

(b) with the sum of the fourth duration and the first duration being designated as a complete half-cycle-duration, having a transistor current flowing between the transistor output terminals only during a certain part of each complete half-cycle-duration; the magnitude of the transistor current increasing during most of said certain part.

48. An arrangement comprising:

a source operative to provide an AC power line voltage between a pair of AC terminals;

a gas discharge lamp having a pair of lamp terminals; and

a power conditioning circuit having: (i) power input terminals connected with the AC terminals, and (ii) power output terminals connectable with the lamp terminals; the power conditioning circuit being functional, as long as the lamp terminals are indeed connected with the power output terminals, to

properly power the gas discharge lamp; the power conditioning circuit being further characterized by:

(a) including a transistor having a pair of transistor output terminals across which exists a transistor output voltage whose magnitude varies in accordance with a periodic waveform; the periodic waveform having a fundamental period consisting of four sub-periods:

(i) sub-period A during which the magnitude of the transistor output voltage increases at a first rate; sub-period A having a first duration;

(ii) sub-period B during which the magnitude of the transistor output voltage remains substantially constant at a relatively high level; sub-period B having a second duration;

(iii) sub-period C during which the magnitude of the transistor output voltage decreases at a second rate; sub-period C having a third duration; and

(iv) sub-period D during which the magnitude of the transistor output voltage remains substantially constant at a relatively low level; sub-period D having a fourth duration; sub-period D preceeding a next sub-period A; and

(b) having a forward transistor current flowing between the transistor output terminals, but substantially only during a certain fraction of sub-period D.

49. The arrangement of claim 48 wherein said certain fraction is distinctly lower than 90 percent of the duration of a complete half-cycle of the periodic waveform; which duration is defined as being equal to the sum of the fourth duration and the first duration.

50. An arrangement comprising:

a source operative to provide an AC power line voltage between a pair of AC terminals;

a gas discharge lamp having a pair of lamp terminals; and

a power conditioning circuit having: (i) power input terminals connected with the AC terminals, and (ii) power output terminals connectable with the lamp terminals; the power conditioning being functional, as long as the lamp terminals are indeed connected with the power output terminals, to properly power the gas discharge lamp; the power conditioning circuit being further characterized by:

(a) including a transistor having a pair of transistor output terminals across which exists a transistor output voltage whose magnitude varies in accordance with a periodic waveform; the periodic waveform having a fundamental period consisting of four sub-periods:

(i) sub-period A during which the magnitude of the transistor output voltage increases at a first rate; sub-period A having a first duration;

(ii) sub-period B during which the magnitude of the transistor output voltage remains substantially constant at a relatively high level; sub-period B having a second duration;

(iii) sub-period C during which the magnitude of the transistor output voltage decreases at a second rate; sub-period C having a third duration; and

(iv) sub-period D during which the magnitude of the transistor output voltage remains substantially constant at a relatively low level; sub-period D having a fourth duration; sub-period D preceeding a next sub-period A; and

(b) having a transistor current periodically flowing between the transistor output terminals; the transistor current, during times when indeed flowing, having a magnitude that changes in a unidirectional manner, thereby having either always a positive slope or always a negative slope.

51. A combination comprising:

a source providing a supply voltage at a pair of socket terminals in an ordinary Edison-type lamp socket; and

an assembly characterized by including:

(a) a fluorescent lamp having a pair of lamp terminals;

(b) a base having a pair of base terminals and being adapted to be screwed into said Edison-type lamp socket, thereby for the base terminals to make electrical connection with the socket terminals; the base being further characterized by: (i) including a threaded portion, and (ii) by having a maximum diameter not larger than about 2.5 times the maximum diameter of the threaded portion;

(c) inverter circuit connected between the base terminals and the lamp terminals; the inverter circuit being disposed within the base and operative, by drawing power from the base terminals, to provide an alternating current to the lamp terminals; the frequency of the alternating current being substantially higher than the frequency of the supply voltage.

52. A combination comprising:

a source providing a supply voltage at a pair of socket terminals in an ordinary Edison-type lamp socket; and

an assembly characterized by including:

(a) a fluorescent lamp having a pair of lamp terminals;

(b) a base having a pair of base terminals and being adapted to be screwed into said Edison-type lamp socket, thereby for the base terminals to make electrical connection with the socket terminals;

(c) inverter circuit connected in circuit between the base terminals and the lamp terminals; the inverter circuit being disposed within the base and operative, by drawing power from the base terminals, to provide an alternating current to the lamp terminals; the frequency of the alternating current being substantially higher than the frequency of the supply voltage; the waveform of the alternating current being substantially sinusoidal.

53. An arrangement comprising:

a source providing a supply voltage at a pair of supply terminals;

a gas discharge lamp having a pair of lamp terminals; and

an assembly of electronic components connected in circuit between the supply terminals and the lamp terminals; the assembly being operative, by drawing power from the supply terminals, to provide a periodically alternating current to the lamp terminals; the frequency of the alternating current being substantially higher than the frequency of the supply voltage; the assembly being further characterized by including a transistor through which flow periodic current pulses and across which exist periodic voltage pulses; each current pulse being char-

acterized, starting at a certain point in time, by decreasing over a first span of time from a certain initial magnitude to a near-zero magnitude, remaining at said near-zero magnitude for a duration equal to at least half the period of the alternating current; each voltage pulse being characterized, starting at said certain point in time, by increasing over a second span of time from a near-zero magnitude to a certain maximum magnitude, remaining at the certain maximum magnitude for a distinct period of time; the first span of time being distinctly shorter than the second span of time.

54. The arrangement of claim 53 wherein the second span of time is at least twice as long as the first span of time.

55. The arrangement of claim 53 wherein the magnitude of the voltage across the transistor never exceeds the certain maximum magnitude.

56. The arrangement of claim 53 wherein the distinct period of time is at least as long as the second span of time.

57. A combination comprising:

a source providing an AC supply voltage at a pair of socket terminals in an ordinary Edison-type lamp socket; and

an assembly characterized by including:

(a) a fluorescent lamp having lamp terminals;

(b) a base having base terminals and being adapted to be screwed into said Edison-type lamp socket, thereby for the base terminals to make electrical connection with the socket terminals;

(c) inverter circuit connected between the base terminals and the lamp terminals; the inverter circuit being disposed within the base and operative, by drawing power from the base terminals, to provide an alternating current to the lamp terminals; the frequency of the alternating current being substantially higher than the frequency of the supply voltage; the inverter circuit being further characterized by having a pair of DC terminals across which exists a DC voltage of absolute magnitude distinctly higher than the peak absolute magnitude of the AC supply voltage.

58. The arrangement of claim 57 wherein the inverter circuit is further characterized by including two transistors series-connected across the DC terminals.

59. A combination comprising:

a source providing a supply voltage at a set of socket terminals in an ordinary Edison-type lamp socket; and

an assembly characterized by including:

(a) a fluorescent lamp having lamp terminals;

(b) a base having base terminals and being adapted to be screwed into said Edison-type lamp socket, thereby for the base terminals to make electrical connection with the socket terminals; and

(c) an assembly of electronic components connected in circuit between the base terminals and the lamp terminals; the assembly being disposed within the base and operative, by drawing power from the base terminals, to provide an alternating current to the lamp terminals, thereby to cause the fluorescent lamp to ignite even though connected with only two of the lamp's terminals; the frequency of the alternating current being substantially higher than the frequency of the supply voltage.

* * * * *

# 4

US005343123A

# United States Patent [19]

Nilssen

[11] Patent Number: 5,343,123

[45] Date of Patent: Aug. 30, 1994

[54] SERIES-RESONANT INVERTER BALLAST

[76] Inventor: Ole K. Nilssen, Caesar Dr., Barrington, Ill. 60010

[21] Appl. No.: 933,891

[22] Filed: Aug. 24, 1992

Related U.S. Application Data

[60] Continuation of Ser. No. 798,869, Nov. 25, 1991, abandoned, which is a continuation of Ser. No. 357,797, May 30, 1989, abandoned, which is a continuation-in-part of Ser. No. 20,478, Mar. 2, 1987, Pat. No. 4,857,806, which is a continuation-in-part of Ser. No. 262,542, May 5, 1981, Pat. No. 4,895,943, which is a division of Ser. No. 178,107, Aug. 14, 1980, Pat. No. 4,902,516, which is a continuation-in-part of Ser. No. 973,741, Dec. 28, 1978, which is a continuation-in-part of Ser. No. 890,586, Mar. 20, 1978, Pat. No. 4,184,128.

[51] Int. Cl.[5] ..... H05B 37/02

[52] U.S. Cl. ..... 315/219; 315/57; 315/62; 315/212; 361/674; 362/221; 362/216

[58] Field of Search ..... 361/377; 362/221, 216; 315/57, 62, DIG. 7, 219, 212; 331/113 A

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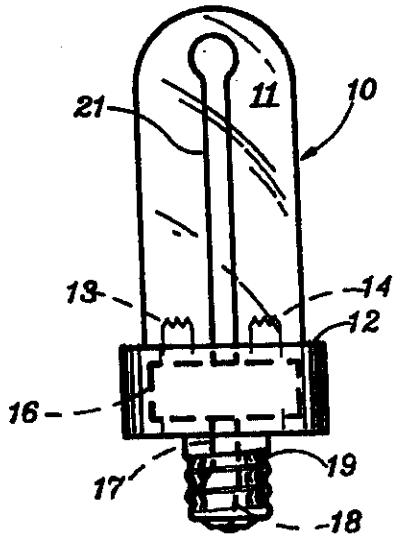
*Primary Examiner*—Robert J. Pascal
*Assistant Examiner*—Reginald A. Ratliff

[57] ABSTRACT

A half-bridge inverter is powered from an ordinary electric utility power line by way of a full wave rectifier-filter means. The high frequency voltage output of the inverter is loaded with a series-combination of a tank inductor and a tank capacitor, with a fluorescent lamp being connected in parallel with the tank capacitor. The ON-time of each of the inverter's two transistors is shorter than half the period of the high frequency voltage; thereby preventing the two transistors from conducting simultaneously; thereby, in turn, protecting the inverter from self-destruction in case of lamp failure.

18 Claims, 1 Drawing Sheet



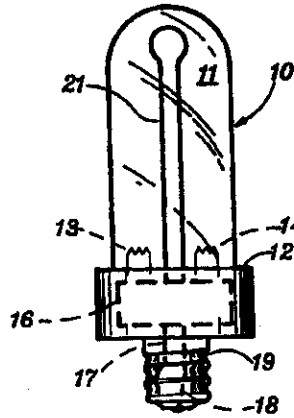



Fig. 1

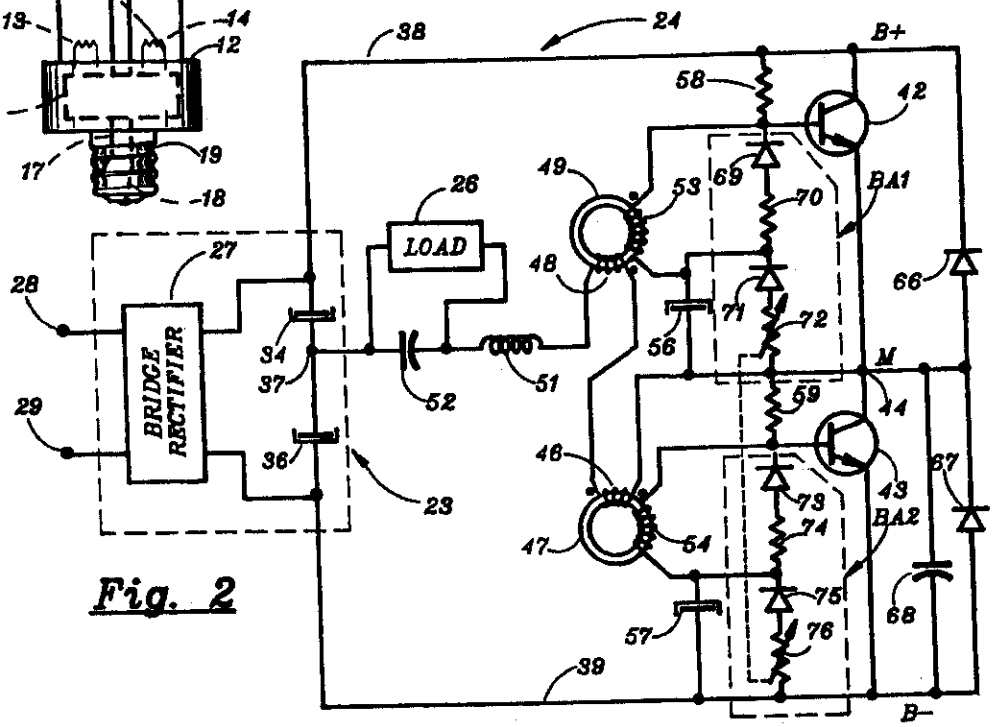



Fig. 2

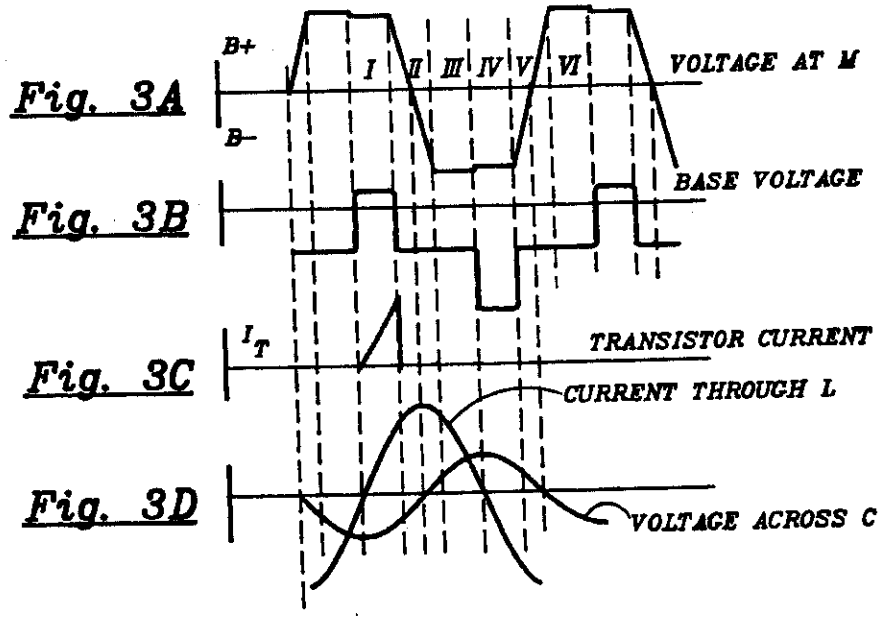



Fig. 3A

Fig. 3B

Fig. 3C

Fig. 3D

# SERIES-RESONANT INVERTER BALLAST

Instant application is a continuation of Ser. No. 07/798,869 filed Nov. 25, 1991, now abandoned; which is a continuation of Ser. No. 07/357,797 now abandoned filed May 30, 1989; which is a continuation-in-part of Ser. No. 07/020,478 filed Mar. 2, 1987, now U.S. Pat. No. 4,857,806; which is a continuation-in-part of Ser. No. 06/262,542 filed May 5, 1981, now U.S. Pat. No. 4,895,943 which is a division of Ser. No. 06/178,107 filed Aug. 14, 1980, now U.S. Pat. No. 4,902,516.

Instant application is also a continuation-in-part of Ser. No. 07/717,860 filed Jun. 19, 1991, now U.S. Pat. No. 5,166,578.

Instant application is also a continuation-in-part of Ser. No. 07/743,216 filed Aug. 9, 1991, now U.S. Pat. No. 5,164,637.

Instant application is also a continuation-in-part of Ser. No. 07/887,427 filed May 21, 1992, now U.S. Pat. No. 5,214,356.

Instant application is also a continuation-in-part of Ser. No. 07/995,229 filed Oct. 1, 1992, now U.S. Pat. No. 5,233,270.

## FIELD OF INVENTION

Instant invention relates to inverter-type fluorescent lamp ballasting means operable to be powered from an ordinary electric utility power line.

## SUMMARY OF THE INVENTION

### Objects of the Invention

An object of the present invention is that of providing a reliable cost-effective fluorescent lamp ballasting means.

This as well as other objects, features and advantages of the present invention will become apparent from the following description and claims.

## BRIEF DESCRIPTION

In its preferred embodiment, instant invention comprises a half-bridge inverter powered from an ordinary electric utility power line by way of a full wave rectifier-filter means. The high frequency squarewave voltage output of the inverter is loaded with a series-combination of a tank inductor and a tank capacitor, with a fluorescent lamp being connected in parallel with the tank capacitor. The ON-time (or forward conduction period) of each of the inverter's two transistors is shorter than half the period of the high frequency voltage; thereby manifestly preventing the two transistors from conducting simultaneously; thereby, in turn, protecting the inverter from self-destruction in case of lamp failure.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 schematically illustrates a compact, screw-in, self-ballasted fluorescent lamb assembly constructed on basis of the preferred embodiment of the invention.

FIG. 2 is a schematic diagram of the preferred embodiment of the invention.

FIGS. 3(*a–d*) illustrates the waveforms of various voltages and currents associated with the ballasting circuit of FIG. 2.



## DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 illustrates a screw-in gas discharge lamp unit 10 comprising a folded fluorescent lamp 11 secured to an integral base 12. The lamp comprises two cathodes 13, 14 which are supplied with the requisite high operating voltage from a frequency-converting power supply and ballasting circuit 16; which, because of its compact size, conveniently fits within base 12.

Circuit 16 is connected by leads 17, 18 to a screw-type plug 19 adapted for screw-in insertion into a standard Edison-type incandescent lamp socket at which ordinary 120 Volt/60 Hz power line voltage is available.

In FIG. 2, a power supply 23 is connected with the 120 Volt/60 Hz power line voltage and provides a center-tapped DC output voltage for supplying a high-efficiency half-bridge inverter circuit 24. The inverter circuit is operable to provide a high-frequency (20–30 kHz) high-magnitude current-limited voltage to a load 26, which actually represents fluorescent lamp 11 of FIG. 1.

Power supply 23 comprises bridge rectifier 27 which connects with 120 Volt/60 Hz power line terminals 28, 29 and provides full-wave rectified power line voltage to two series-connected filter capacitors 34, 36; which filter capacitors are: i) connected together at a center-tap 37, and ii) connected between a positive B+ bus 38 and a negative B- bus 39.

Inverter circuit 24 is a half-bridge inverter comprising transistors 42, 43 connected in series between the B+ bus and the B— bus. The collector of transistor 42 is connected to B+ DUS 38, the emitter of transistor 42 and the collector of transistor 43 are connected to a midpoint line 44 ("M"), and the emitter of transistor 43 is connected to the B— bus 39.

Midpoint line 44 is connected to center-tap 37 through a primary winding 46 of a toroidal saturable core transformer 47, a primary winding 48 on an identical transformer 49, a tank inductor 51 (L) and a series-connected tank capacitor 52 (C) Inductor 51 and capacitor 52 are energized upon alternate transistor conduction in manner to be described later. Load 26 is connected in parallel with capacitor 52.

Drive current to the base terminals of transistors 42 43 is provided by secondary windings 53, 54 of transformers 47, respectively. Winding 53 is also connected to midpoint line 44 through a bias capacitor 56, while winding 54 is connected to the B— bus 39 through an identical bias capacitor 57. The base terminals of transistors 42 and 43 are also connected to lines 38 and 44 through bias resistors 58 and 59, respectively. Shunt diodes 66 and 67 are connected across the collector-emitter terminals of transistors 42 and 43, respectively. A capacitor 68 is connected across the collector-emitter terminals of transistor 43 to restrain the rate of voltage rise across those terminals.

A first optional biasing arrangement BA1 comprises a diode 69 connected with its cathode to the base of transistor 42 and with its anode to the cathode of a diode 71 by way of a resistor 70; the anode of diode 71 is connected with the emitter of transistor 42 by way of a resistor 72; the cathode of diode 71 is connected with the un-dotted side of secondary winding 53 of transformer 49. A second optional biasing arrangement BA2 comprises a diode 73 connected with its cathode to the base of transistor 43 and with its anode to the cathode of

a diode 75 by way of a resistor 74; the anode of diode 75 is connected with the emitter of transistor 43 by way of a resistor 76; the cathode of diode 76 is connected with the un-dotted side of secondary winding 54 of transformer 47.

The operation of the circuit of FIG. 2 can best be understood with additional reference to FIG. 3, which illustrates significant portions of the waveforms of the voltage at midpoint M (FIG. 3A), the base-emitter voltage on transistor 42 (FIG. 3B), the current through transistor 42 (FIG. 3C), and the capacitor 52 voltage and the inductor 51 current (FIG. 3D).

Starting at a point where transistor 42 first starts to conduct, current flows from the B+ bus 38 through windings 46 and 48 and inductor 51 to charge capacitor 52 and returns to the B+ bus through capacitor 34 (refer to the time period designated I in FIG. 3). When the saturable transformer 49 saturates at the end of period I, drive current to the base of transistor 42 will terminate, causing voltage on the base of the transistor to drop to the negative voltage stored on bias capacitor 56 in a manner to be described, causing this transistor to become non-conductive. As shown in FIG. 3c, current-flow in transistor 43 terminates at the end of period I.

However, since the current flowing through inductor 51 cannot change instantaneously, this current will now continue to flow from the B— bus 39 through capacitor 68, eventually causing the voltage at midpoint line 44 to drop to the voltage level on the B— bus (period II in FIG. 3). Thus, capacitor restrains the rate of voltage change across the collector and emitter terminals of transistor 42.

The current through inductor 51 reaches its maximum value when the voltage at midpoint line 44 is zero. During period III the current will continue to flow through inductor 51 but will be supplied from the B— bus through shunt diode 67. It will appreciated that during the latter half of period II and all of period III, positive current is being drawn from a negative voltage; which, in reality, means that energy is being returned to the power supply through a path of relatively low impedance.

When the inductor current reaches zero at the start of period IV, the current through the primary winding 46 of the saturable inductor 47 will cause a current to flow out of secondary winding 54 to cause transistor 43 to become conductive, thereby causing a reversal in the direction of current through inductor 51 and capacitor 52. When transformer 47 saturates at the end of period IV, the drive current to the base of transistor 43 terminates and the current through inductor 51 will supplied through capacitor 68, causing the voltage at midpoint 44 to rise (Period V). When the voltage at the midpoint line M reaches the voltage on the B+ bus, the current will then flow through shunt diode 66 (period VI). The cycle is then repeated.

As seen in FIG. 3, saturable transformers 47, 49 provide transistor drive current only after the current through inductor 51 has diminished to zero. Further, the the transistor drive current is terminated before the current through inductor has reached its maximum amplitude. This coordination of base drive current and inductor current is achieved because of the series-connection between the inductor 51 and the primary windings 46, 48 of saturable transformers 47, 49, respectively.

The series-connected combination of inductor 51 and capacitor 52 is energized upon the alternate conduction of transistors 42 and 43. With a large value of capacitance of capacitor 52, very little voltage will be developed across its terminals. As the value of this capacitance is decreased, however, the voltage across this capacitor will increase. As the value of capacitor 52 is reduced to achieve resonance with inductor 51, the voltage on the capacitor will rise and become infinite in a loss-free circuit operating under ideal conditions.

It has been found desirable to regulate the transistor inversion frequency, determined mainly by the saturation time of saturable transformers 47, 49, to be equal to or higher than the natural resonance frequency of the inductor ana capacitor combination in order to provide a high voltage output to external load 26.

Due to so-called Q-multiplication, a high-magnitude voltage develops across capacitor 52 as the transistor inversion frequency approaches the natural resonance frequency of one series-combination of inductor 51 and capacitor 52.

When inverter circuit 24 is used in the self-ballasted fluorescent lamp of FIG. 1, it has been found that the inversion frequency may be about equal to the natural resonance frequency of the series L-C tank circuit consisting of inductor 51 and capacitor 52. However, if the capacitance value of capacitor 52 is reduced below the point of resonance, unacceptably high transistor currents will result and transistor burn-out will occur.

The sizing of capacitor 52 is determined by the particular application of inverter circuit 24; but, as long as the combined load presented to the output of inverter transistors 42, 43, has an effective inductance value sufficient to provide adequate energy storage for self-sustained transistor inverter action, the current-feedback provided by saturable transformers 47, 49 will effect alternate transistor conduction without the need for additional voltage-feedback.

Because the voltages across transistors 42, 43 are relatively low (due to the absolute voltage-clamping effect to capacitors 34, 36), the half-bridge inverter 24 is very reliable. The absence of switching transients minimizes the possibility of transistor burn-out.

Inverter circuit 24 comprises means for supplying reverse bias to the conducting transistor upon saturation of its associated saturable transformer. For this purpose, capacitors 56 and 57 are charged to negative voltages as a result of reset currents flowing into secondary windings 53, 54 from the bases of transistors 42, 43, respectively. This reverse current rapidly turns off a conducting transistor to increase its switching speed and to achieve high inverter switching efficiency.

When a transistor base-emitter junction is reversely biased, it exhibits the characteristics of a Zener diode, having a reverse breakdown voltage on the order of 8 to 14 Volt for transistors typically used in high-voltage inverters.

Since load 26 comprises a fluorescent lamp, the maximum magnitude of the voltage across capacitor 52 will be limited by the lamp's ignition and operating characteristics, thereby effectively preventing voltages across inductor 51 and capacitor 52 from ever reaching destructive levels.

The above-presented explanation of the operation of the FIG. 2 inverter circuit was based on the two biasing arrangements (BA1 and BA2) being non-connected.

With these biasing arrangements actually connected as indicated, the inverter's operation will become independent of the exact magnitudes of the transistors' base-emitter Zenering voltages. Instead, the magnitude of

the negative bias voltage established on each of capacitors 56 and 57 can now be chosen by choice of resistance value of resistor 72 and/or resistor 76: the lower the resistance value, the lower the magnitude of the associated negative bias voltage; and, in turn, the longer the transistors' ON-time, the lower the inverter's self-oscillating frequency, and the higher the magnitudes of the inverter's output current and power.

By providing for means whereby the resistance values of resistors 72 and 76 can be manually adjusted (in tandem and/or individually), the power provided to the fluorescent lamp may be correspondingly adjusted: the lower the resistance values, the more power provided to the lamp.

Moreover, due to the negative feedback effect inherently provided by resistors 72 and 74, the inverter may be made to operate safely even with the fluorescent lamp being non-connected.

This negative feedback effect is due to the fact that, as the magnitude of the current flowing through the L-C circuit increases, the magnitudes of the drive currents provided to the transistors' bases increase, and the magnitudes of the currents drawn out of capacitors 56 and 57 increase correspondingly; which, in turn, increases the magnitudes of the negative bias voltages present on these capacitors to the point where the magnitudes of the currents flowing through resistors 72 and 76 equal those of the increased base currents. However, the increased negative bias voltages will inherently shorten the transistors' ON-times; which, in turn, will increase the inverter frequency, thereby reducing the inverter's output current; etc. In other words, the indicated biasing arrangements provide for an automatic self-limiting of the magnitude of the inverter's output current.

Additional Explanations and Comments

a) With commonly available components, inverter circuit 24 can be made to operate efficiently at any frequency between a few kHz to perhaps as high as 50 kHz. However, for various well-known reasons (i.e., eliminating audible noise, minimizing physical size, and maximizing efficiency), the frequency actually chosen for the lamp unit of FIG. 1 was in the range of 20 to 30 kHz.

b) The fluorescent lighting unit of FIG. 1 could be made in such manner as to permit fluorescent lamp 11 to be disconnectable from its base 12 and ballasting means 16. However, if powered with normal line voltage without its lamp load connected, frequency-converting power supply and ballasting circuit 16 is apt to self-destruct.

To avoid such self-destruction, arrangements can readily be made whereby the very act of removing the load automatically establishes a situation that prevents the possible destruction of the power supply and ballasting means. For instance, with the tank capacitor (52) being permanently connected with the lamp load (11)—thereby automatically being removed whenever the lamp is removed—the inverter circuit is protected from self-destruction.

c) At frequencies above a few kHz, the loam represented by a fluorescent lamp—once it is ignited—is substantially resistive. Thus, with the voltage across lamp 11 being of a substantially sinusoidal waveform (as indicated in FIG. 3*d*), the current through the lamp will also be substantially sinusoidal in waveshape.

d) In the fluorescent lamp unit of FIG. 1, fluorescent lamp 11 is connected with power supply and ballasting circuit 16 in the exact same manner as is load 26 connected with the circuit of FIG. 2. That is, it is connected in parallel with the tank capacitor (52) of the L-C series-resonant circuit. As is conventional in instant-start fluorescent lamps—such as lamp 11 of FIG. 1—the two terminals from each cathode are shorted together, thereby to constitute a situation where each cathode effectively is represented by only a single terminal. However, it is not necessary that the two terminals from each cathode be shorted together; in which case—for instant-start operation —connection from a lamp's power supply and ballasting means need only be made with one of the terminals of each cathode.

e) It is noted that the transistor's ON-time is shorter than half the period of the inverter's high frequency squarewave voltage output; which voltage output is illustrated by FIG. 3A.

The fact that each of the transistors' ON-times is shorter than half the period of the inverter's high frequency output voltage (or output current) is important: it inherently provides for a situation where the two transistors are manifestly prevented from conducting at the same time, thereby providing protection against circuit failure due to excess-magnitude transistor currents.

f) By adjusting the resistance values of resistors 72 and/or 76, the ON-times of the associated transistors are adjusted accordingly. For instance, by increasing the resistance value of resistor 76, the ON-time associated with transistor 43 is shortened; and, as a result, the magnitude of the current provided to the load 26 is reduced.

g) It is thought that the present invention and many of its attendant advantages will be understood from the foregoing description and that many changes may be made in the form and construction of its components parts, the form described being merely a preferred embodiment of the invention.

I claim:

1. A lamp assembly operable to be inserted into and held by an ordinary Edison-type lamp socket; the lamp socket having socket electrodes at which is provided an AC power line voltage; the lamp assembly comprising:

a gas discharge lamp having lamp terminals;

base means operable to be inserted into and held by the Edison-type lamp socket; the base means having base electrodes operable to make electrical contact with the socket electrodes; the base means also including a combination of:

(a) rectifier means connected with the base electrodes and operative, whenever the base means is indeed inserted into the Edison-type lamp socket, to provide a DC voltage at a set of DC terminals;

(b) inverter means connected with the DC terminals and operative to provide an inverter voltage from a pair of inverter terminals; the inverter voltage having a fundamental period consisting of four time segments: (i) a first time segment during which the magnitude of the inverter voltage remains at a first substantially constant level, (ii) a second time segment during which the magnitude of the inverter voltage increases in a substantially gradual manner, (iii) a third time segment during which the magnitude of the inverter voltage remains at a third substantially constant level, and (iv) a fourth time segment during which the magnitude of the inverter volt-

age decreases in a substantially gradual manner; the inverter means including: (i) a first transistor characterized by conducting current during the first time segment but not during more than half of the second time segment, nor during any other time, and (ii) a second transistor characterized by conducting current during the third time segment but not during more than half of the fourth time segment, nor during any other time; the duration of the first time segment being: (i) approximately equal to that of the third time segment, and (ii) distinctly shorter than half the duration of the fundamental period;

(c) current-limiting means connected between the inverter terminals and a pair of output terminals; and

(d) connect means operative to connect the output terminals with the lamp terminals.

2. The lamp assembly of claim 1 wherein the first transistor is characterized by having a pair of control terminals across which is applied a control voltage having a peak-to-peak magnitude substantially larger than twice the forward voltage drop of an ordinary semiconductor junction.

3. The lamp assembly of claim 1 wherein the inverter voltage has a peak-to-peak magnitude equal to the magnitude of the DC voltage.

4. The lamp assembly of claim 1 wherein the two transistors are series-connected across the DC terminals.

5. A lamp assembly operable to be inserted into and held by an ordinary Edison-type lamp socket; the lamp socket having socket electrodes at which is provided an AC power line voltage; the lamp assembly comprising;

a gas discharge lamp having lamp terminals; and

base means operable to be inserted into and held by the Edison-type lamp socket; the base means having base electrodes operable to make electrical contact with the socket electrodes; the base means also including a combination of:

(a) rectifier means connected with the base electrodes and operative, whenever the base means is indeed inserted into the Edison-type lamp socket, to provide a DC voltage at a set of DC terminals;

(b) inverter means connected with the DC terminals and operative to provide an inverter voltage from a pair of inverter terminals; the inverter voltage having a fundamental period consisting of four time segments: (i) a first time segment during which the magnitude of the inverter voltage remains at a first substantially constant level, (ii) a second time segment during which the magnitude of the inverter voltage increases in a substantially gradual manner, (iii) a third time segment during which the magnitude of the inverter voltage remains at a third substantially constant level, and (iv) a fourth time segment during which the magnitude of the inverter voltage decreases in a substantially gradual manner; the inverter means including a first transistor characterized by conducting current in its forward direction during the first time segment; the duration of the first time segment being: (i) approximately equal to that of the third time segment, and (ii) distinctly shorter than half the duration of the fundamental period; the first transistor being operative to prevent the flow of current in its forward direction during at least a significant part of each of the second and fourth time segments;

(c) current-limiting means connected between the inverter terminals and a pair of output terminals; and

(d) connect means operative to connect the output terminals with the lamp terminals.

6. A lamp assembly adapted to be inserted into and held by an ordinary Edison-type lamp socket; the lamp socket having socket electrodes at which is provided an ordinary AC power line voltage; the lamp assembly comprising:

a gas discharge lamp having two lamp terminals; and

base means operable to be inserted into the Edison-type lamp socket; the base means having base electrodes operable to make electrical contact with the socket electrodes; the base means including frequency-converting ballast means connected in circuit between the base electrodes and the lamp terminals; the ballast means being operative to provide an AC voltage to the lamp terminals; the ballast means being characterized by including a periodically conducting first transistor having: (i) a pair of control input terminals receiving a control signal, and (ii) a pair of output terminals across which exists a periodically varying transistor voltage; the periodically varying transistor voltage being characterized by having a fundamental period consisting of four time segments: (i) a first time segment during which the magnitude of the transistor voltage remains at a first substantially constant level, (ii) a second time segment during which the magnitude of the transistor voltage increases in a substantially gradual manner, (iii) a third time segment during which the magnitude of the transistor voltage remains at a third substantially constant level, and (iv) a fourth time segment during which the magnitude of the transistor voltage decreases in a substantially gradual manner; the transistor conducting current in its forward direction during at least part of the first time segment but not during most of the second time segment.

7. The lamp assembly of claim 6 wherein the control signal has a peak-to-peak magnitude distinctly larger than twice the forward voltage drop of an ordinary semiconductor diode junction.

8. The lamp assembly of claim 6 wherein the duration of the first time segment is distinctly shorter than half the duration of the fundamental period.

9. The lamp assembly of claim 6 wherein to current flows through the first transistor during any part of the fourth period.

10. The lamp assembly of claim 6 further characterized by including: (i) a pair of terminals across which exists a DC voltage; and (ii) a second transistor series-connected with the first transistor to form a series-combination, which series-combination being connected across the DC terminals.

11. A lamp assembly adapted to be inserted into an held by an ordinary Edison-type lamp socket; the lamp socket having socket electrodes at which is provided an ordinary AC power line voltage; the lamp assembly comprising:

a gas discharge lamp having lamp terminals; and

base means operable to be inserted into and held by the Edison-type lamp socket; the base means including base electrodes operable to make electrical

contact with the socket electrodes; the base means also including a sub-assembly connected in circuit between the base electrodes and the lamp terminals; the sub-assembly being functional, as long as the base electrodes do indeed make electrical contact with the socket electrodes, to provide a lamp AC voltage to the lamp terminals; the frequency of the lamp AC voltage being distinctly higher than that of the AC power line voltage; the sub-assembly being further characterized by including: (i) a pair of DC terminals across which exists a DC voltage; and (ii) two periodically conducting transistors series-connected across the DC terminals.

12. The lamp assembly of claim 11 wherein the base means is further characterized in that the absolute magnitude of the DC voltage is distincly higher than the peak absolute magnitude of the AC power line voltage.

13. The lamp assembly of claim 11 wherein the gas discharge lamp includes plural parallel-disposed cylindrically-shaped lamp-segments protruding out from the base means and is further characterized by not having any non-translucent object mounted in between the cylindrically-shaped sections.

14. The lamp assembly of claim 11 wherein: (i) the base means includes a cylindrically-shaped screw-type plug; and (ii) the gas discharge lamp includes at least one cylindrically-shaped lamp-segment having its cylindrical axis disposed parallel to the cylindrical axis of the cylindrically-shaped screw-type plug.

15. The lamp assembly of claim 11 wherein the base means includes a housing structure onto one side of which is mounted the gas discharge lamp and onto the opposite side of which is mounted a cylindrically-shaped screw-type plug screwed into the lamp socket; the screw-type plug having (i) a cylindrical axis, and (ii) a maximum screw-base diameter; the cylindrical axis constituting an axis of symmetry for the base means; which base means further characterized by having a maximum diameter no larger than about 2.5 times the maximum screw-base diameter.

16. A lamp assembly operable to be inserted into and held by an ordinary Edison-type lamp socket; the lamp socket having socket electrodes at which is provided an AC power line voltage; the lamp assembly comprising:

a gas discharge lamp having lamp terminals; and

base means operable to be inserted into and held by the Edison-type lamp socket; the base means having base electrodes operable to make electrical contact with the socket electrodes; the base means also including a combination of:

(a) rectifier means connected with the base electrodes and operative, whenever the base means is indeed inserted into the Edison-type lamp socket, to provide a DC voltage between a pair of DC terminals;

(b) inverter means connected with the DC terminals and operative to provide an AC inverter voltage from a pair of inverter terminals; the AC inverter voltage having a fundamental cycle period; the AC inverter voltage being further characterized by being of frequency distinctly higher than that of the AC power line voltage; the inverter means including a first transistor characterized by conducting current in its forward direction for but a brief period once during each fundamental cycle period; the duration of the brief period being distinctly shorter than half the duration of the fundamental cycle period.

17. The lamp assembly of claim 16 further characterized in that the inverter means includes a second transistor series-connected with the first transistor to form a series-combination, which series-combination is connected across the DC terminals.

18. The lamp assembly of claim 16 further characterized in that the absolute magnitude of the DC voltage is distinctly higher than the peak absolute magnitude of the AC power line voltage.

* * * * *

US005510680A

# United States Patent [19]

Nilssen

[11] Patent Number: 5,510,680

[45] Date of Patent: Apr. 23, 1996

[54] ELECTRONIC BALLAST WITH SPECIAL VOLTAGE WAVEFORMS

[76] Inventor: Ole K. Nilssen, 408 Caesar Dr., Barrington, Ill. 60010

[21] Appl. No.: 993,628

[22] Filed: Dec. 21, 1992

Related U.S. Application Data

[63] Continuation of Ser. No. 751,587, Aug. 22, 1991, which is a continuation of Ser. No. 546,267, Jun. 29, 1990, which is a continuation-in-part of Ser. No. 787,962, Oct. 16, 1985, Pat. No. 4,700,625, which is a continuation of Ser. No. 644,155, Aug. 27, 1984, abandoned, which is a continuation of Ser. No. 555,426, Nov. 23, 1983, abandoned, which is a continuation of Ser. No. 178,107, Aug. 14, 1980, abandoned, said Ser. No. 751,587, is a continuation-in-part of Ser. No. 717,860, Jun. 19, 1991, Pat. No. 5,166,578, which is a continuation of Ser. No. 636,246, Dec. 31, 1990, abandoned, which is a continuation of Ser. No. 787,692, Oct. 15, 1985, abandoned, which is a continuation of Ser. No. 644,155, which is a continuation of Ser. No. 555,426, which is a continuation of Ser. No. 178,107, said Ser. No. 555,426, Nov. 23, 1983, is a continuation-in-part of Ser. No. 330,599, Dec. 14, 1981, Pat. No. 4,441,087, which is a continuation of Ser. No. 973,741, Dec. 28, 1978, abandoned, which is a continuation-in-part of Ser. No. 890,586, Mar. 20, 1978, Pat. No. 4,184,128, said Ser. No. 178,107, Aug. 14, 1980, is a continuation-in-part of Ser. No. 23,849, Mar. 26, 1979, Pat. No. 4,279,011.

[51] Int. Cl.[6] ..... H05B 37/02

[52] U.S. Cl. ..... 315/209 R; 315/219; 315/223; 315/239

[58] Field of Search ..... 315/209 R, 247, 315/219, 223, 239, DIG. 7

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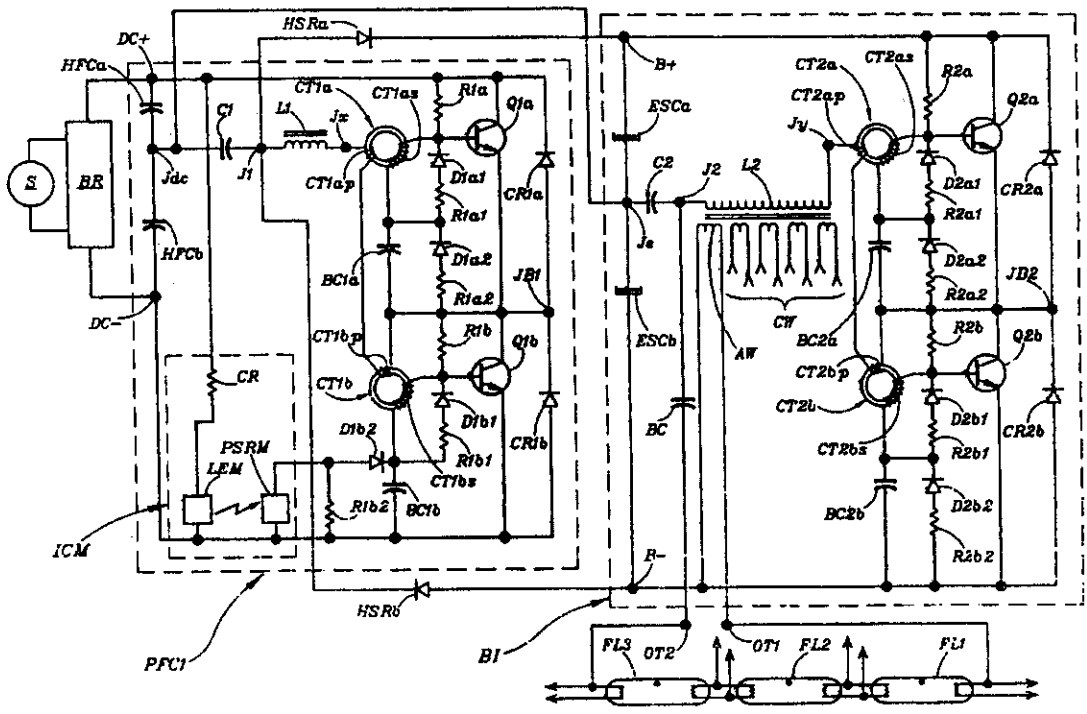
*Primary Examiner*—Frank Gonzalez
*Assistant Examiner*—Reginald A. Ratliff

[57] ABSTRACT

An inverter-type electronic ballast for a gas discharge lamp is powered by a DC supply voltage provided from a rectifier-filter combination connected with an ordinary electric utility power line. The absolute magnitude of the DC supply voltage is higher than the peak absolute magnitude of the power line voltage. The ballast includes an inverter circuit operative to provide an inverter output voltage of special trapezoidal-like waveshape; which output voltage is applied to a series-resonant combination of an inductor and a capacitor. The gas discharge lamp is connected in parallel with the capacitor. The inverter is driven by a voltage of special waveshape and controllable frequency. By controlling the frequency, the magnitude of the current supplied to the gas discharge lamp can be adjusted, thereby correspondingly adjusting the amount of light produced by the lamp.

32 Claims, 3 Drawing Sheets



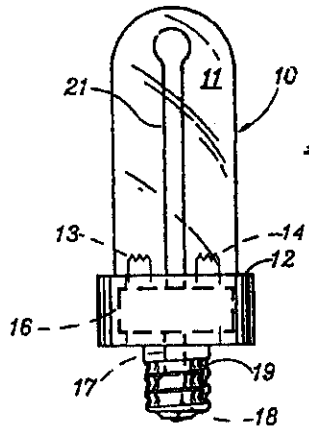



Fig. 1

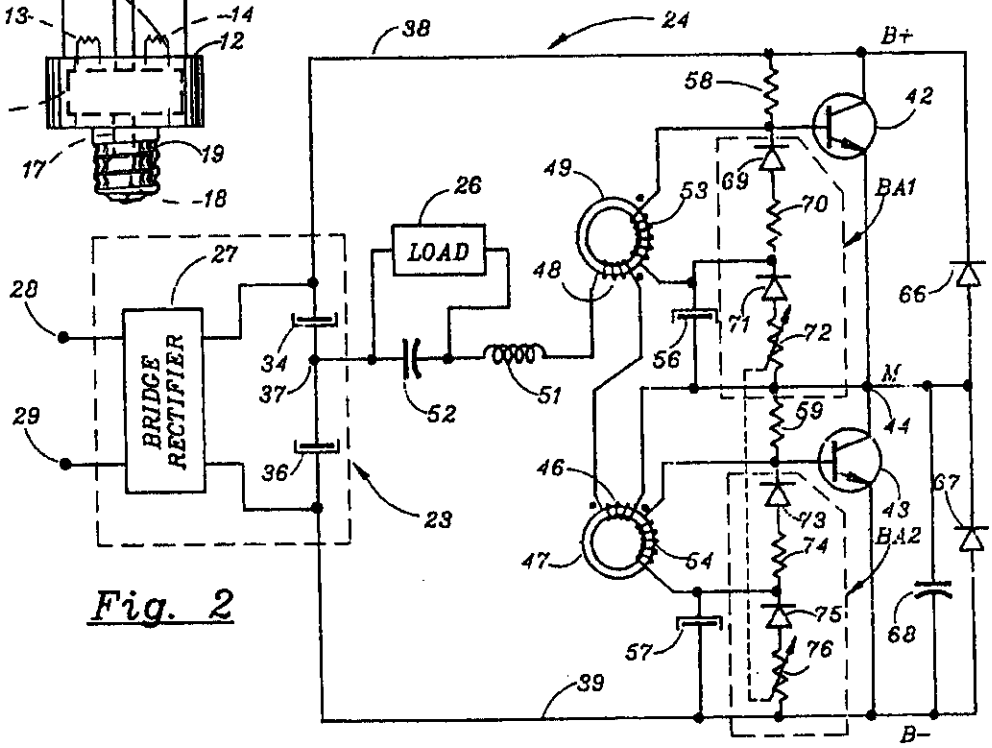



Fig. 2

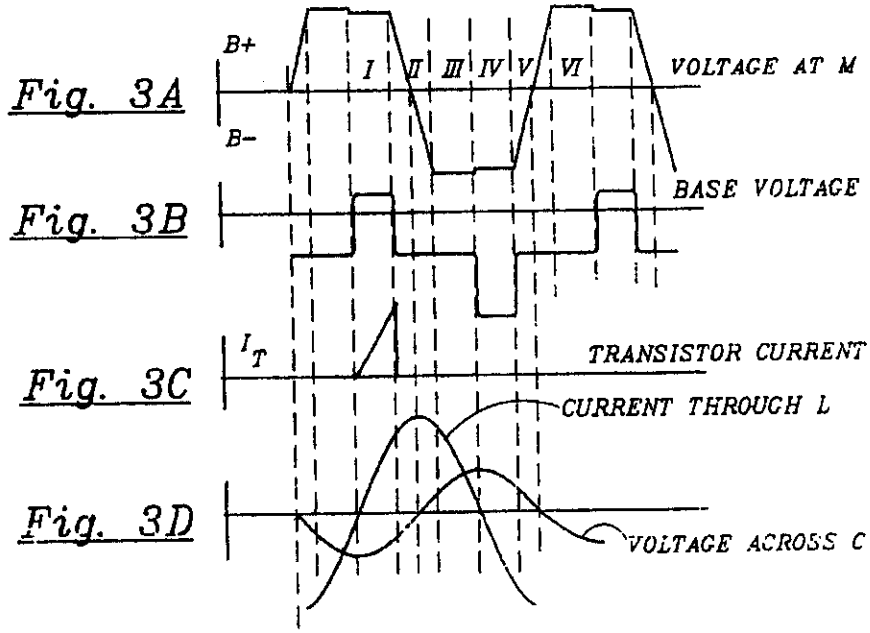



Fig. 3A

Fig. 3B

Fig. 3C

Fig. 3D

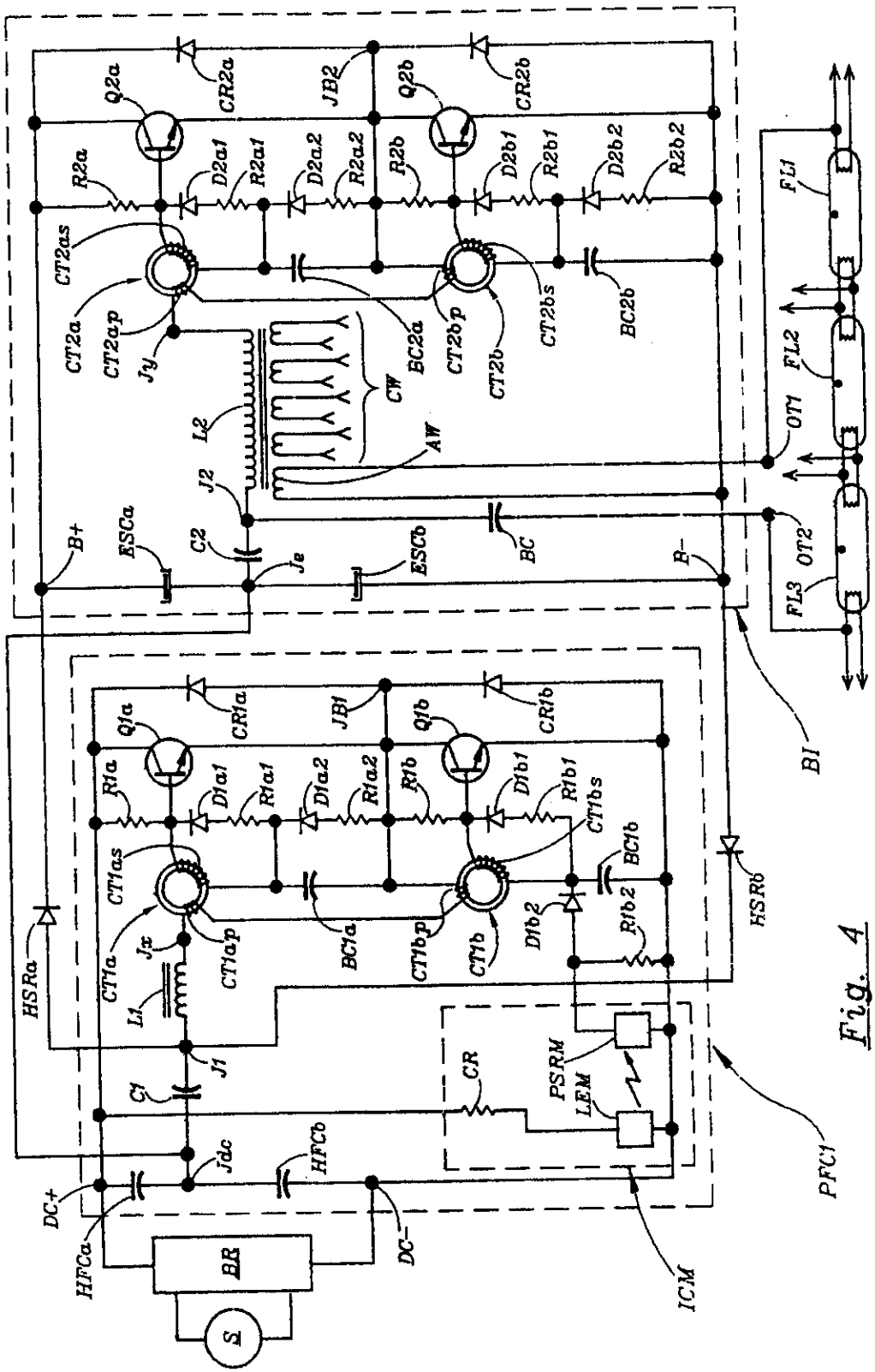

Q2a
CR2a
JB2
Q2b
CR2b
R2a
D2a1
R2a1
D2a2
R2a2
R2b
D2b1
R2b1
D2b2
R2b2
FL1
CT2as
CT2a
CT2ap
Jy
BC2a
CT2bp
CT2b
CT2bs
BC2b
CW
AW
L2
J2
FL2
OT1
B+
ESCa
C2
Je
ESCb
BC
B-
OT2
FL3
Q1a
CR1a
JB1
Q1b
CR1b
R1a
D1a1
R1a1
D1a2
R1a2
R1b
D1b1
R1b1
CT1bs
BC1b
CT1as
CT1a
Jx
CT1ap
BC1a
CT1bp
CT1b
D1b2
R1b2
HSRb
HSRa
L1
J1
C1
CR
PSRM
LEM
Jdc
HFCb
DC+
HFCa
BR
S
DC-
ICM
PFC1
BI

Fig. 4

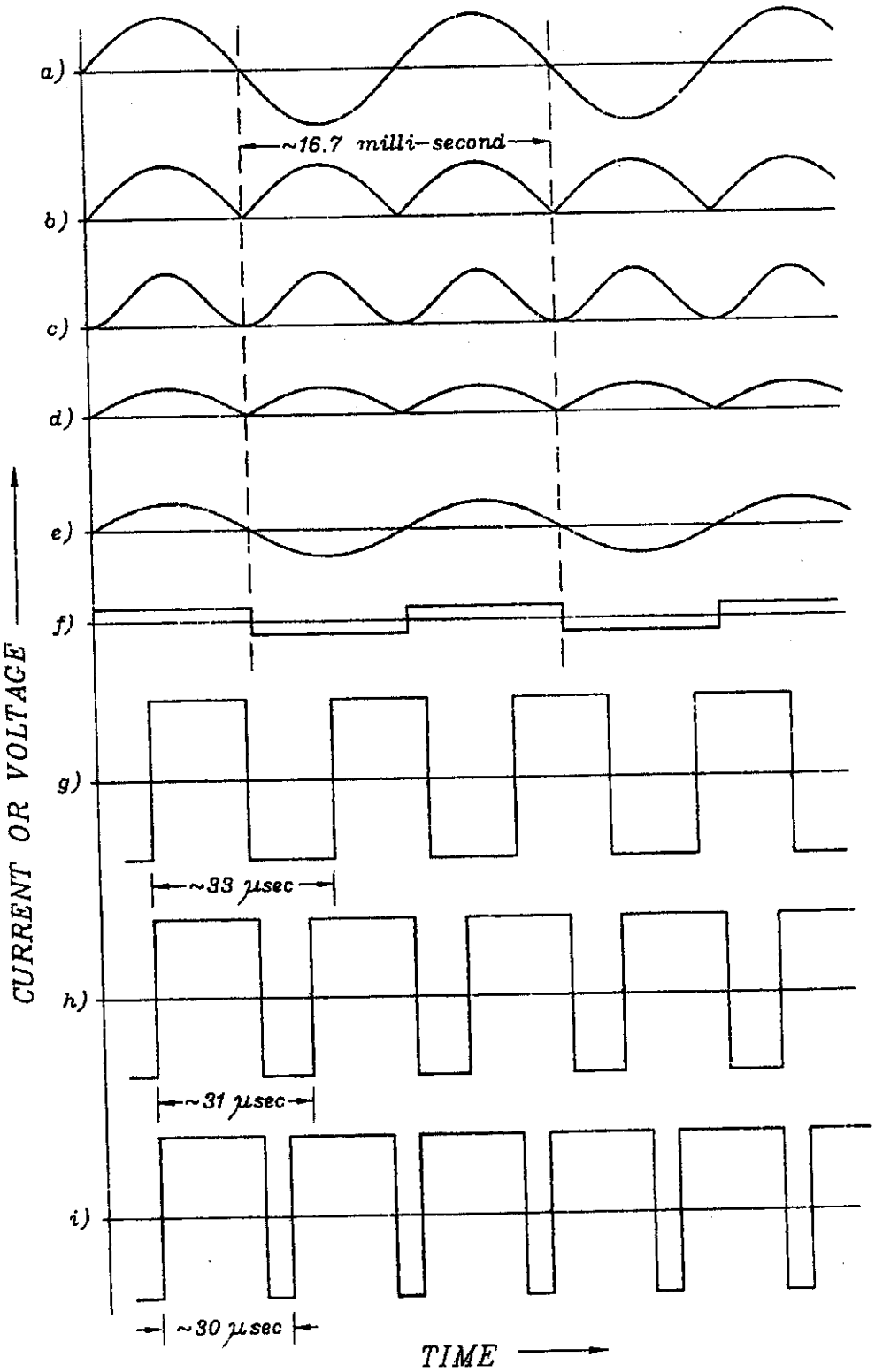

a)
~16.7 milli-second
b)
c)
d)
e)
f)
g)
~33 μsec
h)
~31 μsec
i)
~30 μsec
CURRENT OR VOLTAGE
TIME

Fig. 5

# ELECTRONIC BALLAST WITH SPECIAL VOLTAGE WAVEFORMS

## RELATED APPLICATIONS

The present application is a continuation of Ser. No. 07/751,587 filed Aug. 22, 1991; which is a continuation of Ser. No. 07/546,267 filed Jun. 29, 1990; which is a continuation-in-part of Ser. No. 06/787,962 filed Oct. 16, 1985, now U.S. Pat No. 4,700,625 which is a continuation of Ser. No. 06/644,155 filed Aug. 27, 1984, now abandoned; which is a continuation of Ser. No. 06/555,426 filed Nov. 23, 1983, now abandoned; which was a continuation of Ser. No. 06/178,107 filed Aug. 14, 1980, now abandoned;

Application Ser. No. 07/751,587 is also a continuation-in-part of Ser. No. 07/717,860 filed Jun. 19, 1991 now U.S. Pat. No. 5,166,578 which is a continuation of Ser. No. 07/636,246 filed Dec. 31, 1990, now abandoned which is a continuation of Ser. No. 06/787,692 filed Oct. 15, 1985, now abandoned; which is a continuation of Ser. No. 06/644,155 filed Aug. 27, 1984, now abandoned; which is a continuation of Ser. No. 06/555,426 filed Nov. 23, 1983, now abandoned; which is a continuation of Ser. No. 06/178,107 filed Aug. 14, 1980, now abandoned.

Application Ser. No. 06/555,426 is also a continuation-in-part of Ser. No. 06/330,599 filed Dec. 14, 1981, now U.S. Pat. No. 4,441,087; which is a continuation of Ser. No. 973,741 filed Dec. 28, 1978, now abandoned; which is a continuation-in-part of Ser. No. 890,586 filed Mar. 20, 1978, now U.S. Pat. No. 4,184,128.

Application Ser. No. 06/178,107 is also a continuation-in-part of Ser. No. 23,849 filed Mar. 26, 1979, now U.S. Pat. No. 4,279,011.

## BACKGROUND OF THE INVENTION

### Field of Invention

This invention relates to electronic ballast circuits for gas discharge lamps.

## SUMMARY OF THE INVENTION

An object of the present invention is that of providing a reliable cost-effective fluorescent lamp ballasting means.

This as well as other objects, features and advantages of the present invention will become apparent from the following description and claims.

## BRIEF DESCRIPTION

In a preferred embodiment, instant invention comprises a first half-bridge inverter that is powered from an unfiltered full-wave-rectified ordinary 60 Hz electric utility power line voltage. This first inverter provides at a first inverter output (across which is series-connected a first tuned L-C circuit) a first squarewave voltage of fundamental frequency between about 30 and 33 kHz; which first squarewave voltage is magnitude-modulated at 120 Hz.

The first tuned L-C circuit, which is series-resonant at about 30 kHz, is parallel-loaded by a full-wave high-frequency rectifier whose DC output is applied to a substantially constant-magnitude DC voltage existing across a pair of energy-storing capacitors.

At a constant 30 kHz inverter frequency, the waveshape of the current drawn from the power line is substantially that of a squarewave in phase with the power line voltage, thereby giving rise to a power factor of about 90%. However, by frequency-modulating the first inverter at 120 Hz, the waveshape of the line current is made to be substantially that of a sinewave in phase with the power line voltage, thereby giving rise to a power factor close to 100% and a total harmonic distortion of negligible magnitude.



A second half-bridge inverter is powered from the substantially constant-magnitude DC voltage and provides at a second inverter output (across which is series-connected a second tuned L-C circuit) a second squarewave voltage of fundamental frequency between about 30 and 33 kHz.

The second tuned L-C circuit, which is also series-resonant at about 30 kHz, is parallel-loaded by three series-connected fluorescent lamps. The magnitude of the current supplied to these three lamps is adjustable by adjusting the frequency of the second inverter between about 30 and 33 kHz.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 schematically illustrates a compact, screw-in, self-ballasted fluorescent lamp assembly; which lamp assembly may advantageously comprise the type of ballasting means represented by the present invention.

FIG. 2 is a schematic diagram of a half-bridge inverter and ballasting circuit of the basic type used in the preferred embodiment of the present invention.

FIGS. 3(*a–d*) illustrate the waveforms of various voltages and currents associated with the ballasting circuit of FIG. 2.

FIG. 4 illustrated the preferred embodiment of the present invention.

FIGS. 5(*a–i*) illustrate various voltage and current waveforms associated with the operation of the preferred embodiment of the present invention.

## DESCRIPTION OF THE INVENTION

FIG. 1 illustrates a screw-in gas discharge lamp unit **10** comprising a folded fluorescent lamp **11** suitably secured to an integral base **12**. The lamp comprises two cathodes **13, 14** which are supplied with the requisite high operating voltage from a frequency-converting power supply and ballasting circuit **16**; which, because of its compact size, conveniently fits within the base **12**.

Circuit **16** is connected by leads **17, 18** to a screw-type plug **19** adapted for screw-in insertion into a standard Edison-type incandescent lamp socket at which a typical 60 Hz.

In FIG. 2, a power supply **23** is connected with the 120 Volt/60 Hz power line voltage and provides a center-tapped DC output voltage for supplying a high-efficiency half-bridge inverter circuit **24**. The inverter circuit is operable to provide a high-frequency (e.g., 30 kHz) high-magnitude current-limited voltage to an external load **26**, which actually represents fluorescent lamp **11** of FIG. 1.

Power supply **23** comprises bridge rectifier **27** which connects with 120 Volt/60 Hz power line terminals **28,29** and provides full-wave rectified power line voltage to two series-connected filter capacitors **34, 36**; which filter capacitors are: (i) connected together at a center-tap **37**, and (ii) connected between positive B+ bus **38** and negative B– bus **39**.

Inverter circuit **24** is a half-bridge inverter comprising transistors **42, 43** connected in series across the DC voltage output of the power supply **23** on B+ and B– lines **38** and **39**, respectively. The collector of transistor **42** is connected to

the B+ line 38, the emitter of transistor 42 and the collector of transistor 43 are connected to a midpoint line 44 (designated "M") and the emitter of transistor 43 is connected to the B– line 39.

Midpoint line 44 is connected to center-tap 37 through primary winding 46 of a toroidal saturable core transformer 47, a primary winding 48 on an identical transformer 49, an inductor 51 and a series-connected capacitor 52. The inductor 51 and capacitor 52 are energized upon alternate transistor conduction in a manner to be described later. Load 26 is connected in parallel with capacitor 52.

Drive current to the base terminals of transistors 42 and 43 is provided by secondary windings 53, 54 of transformers 49, 47, respectively. Winding 53 is also connected to midpoint lead 44 through a bias capacitor 56, while winding 54 is connected to the B– lead 39 through an identical bias capacitor 57. The base terminals of transistors 42 and 43 are also connected to lines 38 and 44 through bias resistors 58 and 59, respectively. Shunt diodes 66 and 67 are connected across the collector-emitter terminals pf transistors 42 and 43, respectively. A capacitor 68 is connected across the collector-emitter terminals of transistor 43 to restrain the rate of voltage rise across those terminals.

A first optional biasing arrangement BA1 comprises a diode 69 connected with its cathode to the base of transistor 42 and with its anode to the cathode of a diode 71 by way of a resistor 70; the anode of diode 71 is connected with the emitter of transistor 42 by way of a resistor 72; the cathode of diode 71 is connected with the un-dotted side of secondary winding 53 of transformer 49. A second optional biasing arrangement BA2 comprises a diode 73 connected with its cathode to the base of transistor 43 and with its anode to the cathode of a diode 75 by way of a resistor 74; the anode of diode 76 is connected with the emitter of transistor 42 by way of a resistor 72; the cathode of diode 71 is connected with the un-dotted side of secondary winding 54 of transformer 47.

## Details of Operation of the FIG. 2 Circuit

The operation of the circuit of FIG. 2 can best be understood with additional reference to FIG. 3, which illustrates significant portions of the waveforms of the voltage at midpoint M (FIG. 3A), the base-emitter voltage on transistor 42 (FIG. 3B), the current through transistor 42 (FIG. 3C), and the capacitor 52 voltage and the inductor 51 current (FIG. 3D).

Starting at a paint where transistor 42 first starts to conduct, current flows from the B+ line 38 through windings 46 and 48 and inductor 51 to charge capacitor 52 and returns to the B+ line through capacitor 34 (refer to the time period designated I in FIG. 3). When the saturable inductor 49 saturates at the end of period I, drive current to the base of transistor 42 will terminate, causing voltage on the base of the transistor to drop to the negative voltage stored on the bias capacitor 56 in a manner to be described, causing this transistor to become non-conductive. As shown in FIG. 3c, current-flow in transistor 43 terminates at the end of period I.

However, since the current flowing through inductor 51 cannot change instantaneously, this current will now continue to flow from the B– bus 39 through capacitor 68, eventually causing the voltage at midpoint line 44 to drop to the voltage level of the B– bus (period II in FIG. 3). Thus, capacitor 68 restrains the rate of voltage change across the collector and emitter terminals of transistor 42.



The current through the inductor 51 reaches its maximum value when the voltage at the midpoint line 44 is zero. During period III, the current will continue to flow through inductor 51 but will be supplied from the B– bus through the shunt diode 67. It will be appreciated that during the latter half of period II and all of period III, positive current is being drawn from a negative voltage; which, in reality, means that energy is being returned to the power supply through a path of relatively low impedance.

When the inductor current reaches zero at the start of period IV, the current through the primary winding 46 of the saturable inductor 47 will cause a current to flow out of its secondary winding 54 to cause transistor 43 to become conductive, thereby causing a reversal in the direction of current through inductor 51 and capacitor 52. When transformer 47 saturates at the end of period IV, the drive current to the base of transistor 43 terminates and the current through inductor 51 will be supplied through capacitor 68, causing the voltage at midpoint line 44 to rise (period V). When the voltage at the midpoint line M reaches the voltage on the B+ bus, the current will then flow through shunt diode 66 (period VI). The cycle is then repeated.

As seen in FIG. 3, the saturable inductors 47, 49 provide transistor drive current only after the current through inductor 51 has diminished to zero. Further, the transistor drive current is terminated before the current through inductor 51 has reached its maximum amplitude. This coordination of base drive current and inductor current is achieved because of the series-connection between the inductor 51 and the primary windings 46, 48 of saturable transformers 47, 49, respectively.

The series-connected combination of the inductor 51 and the capacitor 52 is energized upon the alternate conduction of transistors 42 and 43. With a large value of capacitance of capacitor 52, very little voltage will be developed across its terminals. As the value of this capacitance is decreased, however, the voltage across this capacitor will increase. As the value of the capacitor 52 is reduced to achieve resonance with the inductor 51, the voltage on the capacitor will rise and become infinite in a loss-free circuit operating under ideal conditions.

It has been found desirable to regulate the transistor inversion frequency, determined mainly by the saturation time of the saturable inductors 47, 49, to be equal to or higher than the natural resonance frequency of the inductor and capacitor combination in order to provide a high voltage output to external load 26.

Due to so-called Q-multiplication, a high-magnitude voltage develops across capacitor 52 as the transistor inversion frequency approaches the natural resonance-frequency of the series-combination of inductor 51 and capacitor 52.

When inverter circuit 24 is used in the self-ballasted fluorescent lamp of FIG. 1, it has been found that the inversion frequency may be about equal to the natural resonance frequency of the series L-C tank circuit consisting of inductor 51 and capacitor 52. However, if the capacitance value of capacitor 52 is reduced below the point of resonance, unacceptably high transistor currents will result and transistor burn-out will occur.

The sizing of capacitor 52 is determined by the particular application of inverter circuit 24; but as long as the combined load (i.e., as represented to the output of inverter transistors 42, 43) has an effective inductance value sufficient to provide adequate energy storage for self-sustained transistor inverter action, the current-feedback provided by saturable transformers 47, 49 will effect alternate transistor conduction without the need for additional voltage feedback.

Because the voltages across transistors **42**, **43** are of relatively low magnitude (due to the absolute voltage-clamping effect of capacitors **34**, **36**), the half-bridge inverter **24** is very reliable. The absence of switching transients minimizes the possibility of transistor burn-out.

Inverter circuit **24** comprises means for supplying reverse bias to a conducting transistor upon saturation of its associated saturable transformer. For this purpose, capacitors **56**, **57** are charged to negative voltages as a result of reset currents flowing into secondary windings **53**, **54** from the bases of transistors **42**, **43**, respectively. This reverse current rapidly turns off a conducting transistor to increase its switching speed and to achieve high inverter switching efficiency.

When a transistor base-emitter junction is reversely biased, it exhibits the characteristics of a Zener diode, having a reverse breakdown (i.e., Zenering) voltage on the order of 8 to 14 Volt for transistors typically used in high-voltage inverters.

Since liad **56** comprises a fluorescent lamp, the maximum magnitude of the voltage across capacitor **52** will be limited by the lamp's ignition and operating characteristics, thereby effectively preventing voltages across inductor **51** and capacitor **52** from ever reaching destructive levels.

The above-presented explanation of the operation of the FIG. 2 inverter circuit was based on the two biasing arrangements (BA1 and BA2) being non-connected.

With these biasing arrangements actually connected as indicated, the inverter's operation will become independent of the exact magnitude of the transistors' base-emitter Zenering voltages. Instead, the magnitude of the negative bias voltage established on each of capacitors **56** and **57** can now be chosen by choice of resistance value of resistor **72** and/or resistor **76**: the lower the resistance value, the lower the magnitude of the associated negative bias voltage; and, in turn, the longer the transistors' ON-time, the lower the inverter's self-oscillating frequency, and the higher the magnitudes of the inverter's output current and power.

By providing for means whereby the resistance values of resistors **72** and **76** can be manually adjusted (in tandem and/or individually), the power provided to the fluorescent lamp may be correspondingly adjusted: the lower the resistance values, the more power provided to the lamp.

Moreover, due to the negative feedback effect inherently provided by resistors **72** and **74**, the inverter may be made to operate safely even with the fluorescent lamp being non-connected.

This negative feedback effect is due to the fact that, as the magnitude of the current flowing through the L-C circuit increases, the magnitudes of the drive currents provided to the transistors' bases increase, and the magnitudes of the currents drawn out of capacitors **56** and **57** increase correspondingly; which, in turn, increase the magnitudes of the negative bias voltages present on these capacitors to the point where the magnitudes of the currents flowing through resistors **72** and **76** equal those of the increased base currents. However, the increased negative bias voltage will inherently shorten the transistors' ON-times; which, in turn, will increase the inverter frequency, thereby reducing the inverter's output current; etc. In other words, the indicated biasing arrangements provide for an automatic self-limiting of the magnitude of the inverter's output current.

### Additional Comments re the FIG. 2 Circuit

(a) With commonly available components, inverter circuit **24** can be made to operate efficiently at any frequency between a few kHz to perhaps as high as 50 kHz. However, for various well-known reasons (i.e., eliminating audible noise, minimizing physical size, and maximizing efficiency), the frequency actually chosen for the lamp unit of FIG. **1** was in the range of 20 to 30 kHz.

(b) The fluorescent lighting unit of FIG. **1** could be made in such manner as to permit fluorescent lamp **11** to be disconnectable from its base **12** and ballasting means **16**. However, if powered with normal line voltage without its lamp load connected, frequency-converting power supply and ballasting circuit **16** is apt to self-destruct.

To avoid self-destruction, arrangements can readily be made whereby the very act of removing the load automatically establishes a situation that prevents the possible destruction of the power supply and the ballasting means. For instance, with the tank capacitor (**52**) being permanently connected with the lamp load (**11**)—thereby automatically being removed whenever the lamp is removed—the inverter circuit is protected from self-destruction.

(c) At frequencies above a few kHz, the load represented by a fluorescent lamp—once it is ignited—is substantially resistive. Thus, with the voltage across lamp **11** being on a substantially sinusoidal waveform (as indicated in FIG. **3***d*), the current through the lamp will also be substantially sinusoidal in waveshape.

(d) In the fluorescent lamp unit of FIG. **1**, fluorescent lamp **11** is connected with power supply and ballasting circuit **16** in the exact same manner as is load **26** connected with the circuit of FIG. **2**. That is, it is connected in parallel with the tank capacitor (**52**) of the L-C series-resonant circuit. As is conventional in instant-start fluorescent lamps—such as lamp **11** of FIG. **1**—the two terminals from each cathode are shorted together, thereby to constitute a situation where each cathode effectively is represented by only a single terminal. However, it is not necessary that the two terminals from each cathode be shorted together; in which case—for instant-start operation—connection of a lamp's power supply and ballasting means need only be made with one of the terminals of each cathode.

(e) It is noted that the transistor's ON-time is shorter than half the period of the inverter's high frequency squarewave voltage output; which voltage output is illustrated by FIG. **3A**.

The fact that each of the transistors' ON-times is shorter than half the period of the inverter's high frequency output voltage (or output current) is important: it inherently provides for a situation where the two transistors are manifestly prevented from conducting at the same time, thereby providing protection against circuit failure due to excess-magnitude transistor currents.

(f) By adjusting the resistance values of resistors **72** and/or **72**, the ON-times of the associated transistors are adjusted accordingly. For instance, by increasing the resistance value of resistor **76**, the ON-time associated with transistor **43** is shortened; and, as a result, the magnitude of the current provided to the load **26** is reduced.

### Details of Construction of the Preferred Embodiment

In FIG. **4**, a source S represents an ordinary electric utility power line providing 120 Volt/60 Hz power line voltage to the input of bridge rectifier BR, whose DC output is applied between a DC– bus and a DC+ bus.

A high-frequency filter capacitor HFCa is connected between a junction Jdc and the DC+ bus; a high-frequency

filter capacitor HFCb is connected between the DC– bus and junction Jdc.

A tank capacitor C1 is connected between junction Jdc and a junction J1; a tank inductor L1 is connected between junction J1 and a junction Jx.

A transistor Q1*a* is connected with its collector to the DC+ bus and with its emitter to a junction bus JB1; a transistor Q1*b* is cojnected with its collector to junction bus JB1 and with its emitter to the DC– bus. A commutating rectifier CR1*a* is connected with its cathode to the DC+ bus and with its anode to junction bus JB1; a commutating rectifier CR1*b* is connected with its cathode to junction bus JB1 and with its anode to the DC– bus.

Primary windings CT1*ap* and CT1*bp* of saturable current transformers CT1*a* and CT1*b*, respectively, are series-connected between junctions Jx and junction bus JB1.

Secondary winding CT1*as* of transformer CT1*a* is connected between the base of transistor Q1*a* and the cathode of a diode D1*a*2, whose anode is connected with junction bus JB1 via a resistor R1*a*2. A diode D1*a*1 is connected with its cathode to the base of transistor Q1*a* and with its anode to the cathode of diode D1*a*2 via a resistor R1*a*1. A resistor R1*a* is connected between the DC+ bus and the base of transistor Q1*a*. A bias capacitor BC1*a* is connected between the cathode of diode D1*a*2 and junction bus JB1.

Secondary winding CT1*bs* of transformer CT1*b* is connected between the base of transistor Q1*b* and the cathode of a diode D1*b*2, whose anode is connected with the DC– bus via a resistor R1*b*2. A diode D1*b*1 is connected with its cathode to the base of transistor Q1*b* and with its anode to the cathode of diode D1*b*2 via a resistor R1*b*1. A resistor R1*b* is connected between junction bus JB1 and the base of transistor Q1*b*. A bias capacitor BC1*b* is connected between the cathode of diode D1*b*2 and the DC– bus.

A high-speed rectifier HSRa is connected with its anode to junction J1 and with its cathode to a B+ bus; a high-speed rectifier HSRb is connected with its cathode to junction J1 and with its anode to a B– bus.

An energy-storing capacitor ESCa is connected between a junction Je and the B+ bus, junction Je being connected with junction Jdc; an energy-storing capacitor ESCb is connected between junction Je and the B– bus.

A tank capacitor C2 is connected between junction Je and a junction J2; a tank inductor is connected between junction J2 and a junction Jy.

A transistor Q2*a* is connected with its collector to the B+ bus and with its emitter to a junction bus JB2; a transistor Q2*b* is connected with its collector to junction bus JB2 and with its emitter to the B– bus. A commutating rectifier CR2*a* is connected with its cathode to the B+ bus and with its anode to junction bus JB2; a commutating rectifier CR2*b* is connected with its cathode to junction bus JB2 and with its anode to the B– bus.

Primary windings CT2*ap* and CT2*bp* of saturable current transformers CT2*a* and CT2*b*, respectively, are series-connected between junction Jy and junction bus JB2.

Secondary winding CT2*as* of transformer CT2*a* is connected between the base of transistor Q2*a* and the cathode of a diode D2*a*2, whose anode is connected with junction bus JB2 via a resistor R2*a*2. A diode D2*a*1 is connected with its cathode to the base of transistor Q2*a* and with its anode to the cathode of diode D2*a*2 via a resistor R2*a*1. A resistor R2*a* is connected between the B+ bus and the base of transistor Q2*a*. A bias capacitor BC2*a* is connected between the cathode of diode D2*a*2 and junction bus JB2.

Secondary winding CT2*bs* of transformer CT2*b* is connected between the base of transistor Q2*b* and the cathode of a diode D2*b*2, whose anode is connected with the B– bus via a resistor R2*b*2. A diode D2*b*1 is connected with its cathode to the base of transistor Q2*b* and with its anode to the cathode of diode D2*b*2 via a resistor R2*b*1. A resistor R2*b* is connected between junction bus JB2 and the base of transistor Q2*b*. A bias capacitor BC2*b* is connected between the cathode of diode D2*b*2 and the B– bus.

An auxiliary winding AW is wound as a loosely coupled secondary winding on tank inductor L2 and connected between the B– bus and an output terminal OT1. A DC blocking capacitor BC is connected between junction J2 and an output terminal OT2.

Also wound on tank inductor L2 are four cathode windings CW; which four cathode windings are connected with corresponding pairs of cathode terminals of three series-connected fluorescent lamps FL1, FL2 and FL3; which three fluorescent lamps are series-connected across output terminals OT1 and OT2.

An inverter control means ICM is connected between the DC– bus and the DC+ bus, as well as with the anode of diode D1*b*2; which inverter control means consists of: (i) a photo-sensitive resistive means PSRM connected between the anode of diode D1*b*2 and the DC– bus; and (ii) a light-emitting means LEM, such as a light-emitting diode (or LED), connected in series with a control resistor CR between the DC– bus and the DC+ bus. Light-emitting means LEM is so positioned and arranged that its light output impinges on a light-receptive part of photo-sensitive resistive means PSRM.

The half-bridge inverter with Q1*a* and Q1*b* as its switching transistors is identified as power-factor-correcting inverter PFCI; and the half-bridge inverter with Q2*a* and Q2*b* as its switching transistors is identified as ballast inverter BI.

## Details of Operation of the Preferred Embodiment

The operation the preferred embodiment of instant invention may best be understood when read with reference to FIG. 5; which illustrates various current and voltage waveforms associated with the operation of the circuit arrangement of FIG. 4.

With reference to the waveforms of FIG. 5 and the circuit arrangement of FIG. 4, as long as the magnitude of the DC voltage existing between the B– bus and the B+ bus remains substantially constant, waveform: (a) represents that of the 120 Volt/60 Hz power line voltage supplied from source S; (b) represents the corresponding DC voltage present between the DC– bus and the DC+ bus; (c) represents the net current provided via high-speed rectifiers HSRa and HSRb to energy-storing capacitors ESCa and ESCb; (d) represents the current drawn from the DC output of bridge rectifier BR; and (e) represents the waveform of the current drawn from source S. Waveform (f) represents the current that would be drawn from source S in case the light from light-emitting means LEM were to be kept at a constant intensity, such as would occur if a filter capacitor were to be connected thereacross.

The two half-bridge inverters (PFCI and BI) both operate in the same basic manner as does the half-bridge inverter of FIG. 2.

In case of the PFCI inverter, the load constitutes the substantially constant-magnitude DC voltage present across energy-storing capacitors ESCa and ESCb; in case of the BI

inverter, the principal load constitutes the three series-connected fluorescent lamps FL1, FL2 and FL3.

In the overall operation of the circuit of FIG. 4, the PFCI inverter continually charges the two energy-storing capacitors (ESCa/ESCb), while the BI inverter continually discharges these same energy-storing capacitors. Thus, the magnitude of the DC voltage across these energy-storing capacitors will stabilize at a point where the average rate of capacitor-charging equals the average rate of capacitor-discharging.

While the average rate of capacitor-charging is essentially fixed for a given magnitude of the voltage supplied by the source (S), the average rate of capacitor-discharging increases with increasing magnitude of the DC voltage present across the energy-storing capacitors (i.e., between the B– bus and the B+ bus).

Absent any control by inverter control means ICM, a basic characteristic of the series-driven parallel-loaded PFCI inverter powering a constant-voltage-magnitude load, such as indeed represented by capacitors ESCa/ESCb, is that the instantaneous magnitude of the current provided to this load will be roughly proportional to the instantaneous magnitude of the DC voltage powering the inverter. Thus, absent control, the magnitude of the charging current supplied to capacitors ESCa/ESCb will vary in proportion with the magnitude of the DC voltage present between the DC– bus and the DC+ bus.

However, another basic characteristic of the PFCI inverter is that, with a constant-magnitude DC voltage present between the DC– bus and the DC+ bus, the magnitude of the charging current supplied to capacitors ESCa/ESCb is roughly proportional to the conductance of photo-sensitive resistive means PSRM; which, in turn, is roughly proportional to the amount of light emitted from light-emitting means LEM; which, in turn, is roughly proportional to the magnitude of the current flowing through light-emitting means LEM; which, in turn, is roughly proportional to the magnitude of the DC voltage present between the DC– bus and the DC+ bus.

Thus, with the amount of light emitted by light-emitting means LEM being roughly proportional to the instantaneous magnitude of the DC voltage present between the DC– bus and the DC+ bus, the instantaneous magnitude of the charging current supplied to capacitor ESCa/ESCb will be roughly proportional to the square of the instantaneous magnitude of that DC voltage.

As an overall consequence, the instantaneous magnitude of the cur rent drawn by the PFCI inverter will be roughly proportional to the instantaneous magnitude of the DC voltage present between the DC– bus and the DC+ bus; which is to say that the instantaneous magnitude of the current drawn from the power line (i.e., source S) will be proportional to the instantaneous magnitude of the voltage provided from the power line; which, in turn, provides for the power drawn from the power line by the circuit arrangement of FIG. 4 to exhibit a power factor close to unity (i.e., 100%). Moreover, the waveform of the current drawn from the power line will exhibit an exceptionally low degree of harmonic distortion.

In effecting its control action, inverter control means ICM causes both symmetry-modulation and frequency-modulation of the inverter output voltage provided between junction Jdc and junction Jx. As illustrated by FIG. 5(*g*), this inverter output voltage is a nearly symmetrical squarewave of a certain frequency (about 30 kHz) whenever the instantaneous magnitude of the DC voltage between the DC– bus and the DC+ bus is at its maximum (about 170 Volt). However, with the instantaneous magnitude of this DC voltage being about half its maximum, the inverter output voltage—as illustrated by FIG. 5(*h*)—is a clearly asymmetrical squarewave. Moreover, its frequency is now higher (about 32 kHz). As indicated by FIG. 5(*i*), at a still lower magnitude of the DC voltage between the DC– bus and the DC+ bus, the inverter output voltage is still more asymmetrical and of still higher frequency.

Thus, the PFCI inverter effects its control action by a combination of symmetry-modulation and frequency-modulation.

Increasing frequency—other things being equal—provides for reduced-magnitude charging current to energy-storing capacitors ESCa/ESCb. This is so for the reason that the natural series-resonance-frequency of the L2-C2 tuned circuit is below the inverter's actual frequency

Increasing asymmetry—other things being equal—also provides for reduced-magnitude charging current to energy-storing capacitors ESCa/ESCb. This is so for the reason that the magnitude of the fundamental frequency component of the inverter's output voltage decreases roughly in proportion to the degree of asymmetry.

As the degree of conductance of photo-sensitive resistive means PSRM increases, the magnitude of the negative bias voltage present across bias capacitor BC1*b* decreases; which results in a longer ON-time for transistor Q1*b*.

As for the BI inverter, the operation is substantially as described in connection with the circuit of FIG. 2, except for the particular feature associated with auxiliary winding AW.

The phasing of the AW winding is such that the fundamental frequency component of the high-frequency voltage provided at output terminal OT1 is substantially out-of-phase with the high-frequency voltage provided at output terminal OT2. That way, the magnitude of the net voltage provided across the three series-connected lamps is larger than it would be if the lamps had been connected directly across tank capacitor C2.

In case of ordinary F40 or F34 T-12 Rapid-Start fluorescent lamps, each lamp requires an operating voltage of RMS magnitude equal to about 100 Volt; which implies a total RMS magnitude of about 300 Volt across the three series-connected lamps.

To reduce potentially dangerous electric shock effects, as might result from capacitive coupling directly from the glass envelope of the fluorescent tube to the hand of a person installing and/or removing the fluorescent lamps from their sockets, it is important that the magnitude of the lamp's arc voltage be not much higher than about 200 Volt RMS (at about 30 kHz) with respect to ground. If it were to exceed this 200 Volt RMS magnitude, a person might receive a potentially hazardous electric shock effect merely from grabbing the fluorescent tube at a point where the potential of the ionized gas inside the glass envelope were higher than 200 Volt RMS with respect to ground.

In the particular arrangement of FIG. 4, the maximum magnitude of the 30 kHz potential of the ionized gas within the fluorescent glass tube is indeed maintained below approximately 200 Volt RMS with respect to ground, in spite of the fact that the three lamps require an operating voltage of 300 Volt RMS magnitude. This result has been achieved by way of the AW winding, whose output voltage—during lamp operation—is about 100 Volt RMS with respect to the B– bus; which, with respect to the 30 kHz inverter voltage, is indeed at ground potential.

On the other hand, the magnitude of the voltage contributed by the AW winding should be as low as reasonably

possible for the reason that its waveform is of such nature as to cause degradation of the lamp current crest factor; which degradation is due to the fact that—contrary to the case with the voltage across the tank capacitor (C2)—the waveshape of the voltage present across the tank inductor (L2) includes the full magnitude of the squarewave voltage provided at the inverter's output (i.e., the voltage provided between junctions Je and Jy).

With the DC voltage provided between the B– bus and the B+ bus being of substantially constant magnitude, the lamp current crest factor would be about 1.5 if the lamps were to have been connected directly across the tank capacitor. However, had the lamps instead been connected directly across the tank inductor, the lamp current crest factor would have been far in excess of 1.7; which is normally considered the maximum permissible level for lamp current crest factor. On the other hand, with only one third of the lamp voltage derived from the tank inductor voltage, and with the remaining two thirds being derived from the tank capacitor voltage, the net resulting lamp current crest factor is kept just below 1.7—as is indeed the case in the arrangement of FIG. 4.

## Additional Comments

(aa) The reason that the AW winding is loosely coupled with tank inductor L2 is related to minimizing detrimental effects on lamp current crest factor due to powering the lamps in part by the tank inductor voltage. By effectively providing the tank inductor voltage to the fluorescent lamp via a series inductance, the detrimental effects on lamp current crest factor are indeed reduced. However, the same result can be obtained by placing an inductor in series with the fluorescent lamps.

(ab) Light-emitting means LEM is likely not to be totally linear in terms of light output as function of the magnitude of the driving DC current. Likewise, photo-sensitive resistive means is likely not to be totally linear with respect to its effective conductance versus amount of light received. In addition, the symmetry-modulation and frequency-modulation resulting from changes in the conductance of the photo-sensitive resistive means are not likely to be totally linear.

However, it is not necessary that these various relationships be totally linear. Instead, the largest part of the sought-after effect—namely power factor correction and reduction of power line harmonics—will result even if the various relationships be quite non-linear.

Of course, by carefully selecting and matching the non-linearities of the different effects, as well as by introducing various linearizing means, nearly any desired degree of final power factor correction can be achieved.

(ac) The time constant associated with bias capacitor BC1*b* and its associated charge leakage means—namely resistor R1*b*2 and photo-sensitive resistive means PSRM—must be long with respect to a complete cycle of the 30 kHz inverter frequency. However, this time constant should be short compared with a complete cycle of the 120 Hz ripple voltage on the DC voltage present between the DC– bus and the DC+ bus.

(ad) The waveshape of the high-frequency current flowing from tank capacitor C1 of FIG. 4 is substantially sinusoidal— with the positive halves flowing though rectifier HSRa and the negative halves flowing through rectifier HSRb.

(ae) The absolute instantaneous magnitude of the high-frequency current flowing from junction J1 and through rectifiers HSRa and HSRb is—except for any imperfections in the HSRa/HSRb rectifiers—equal to that of the net DC current flowing into energy-storing capacitors ESCa and ESCb.

(af) The waveshape of the current flowing through the three series-connected fluorescent lamps is also nearly sinusoidal; except that a modest degree of distortion is introduced by the harmonics of the component of high-frequency voltage provided by auxiliary winding AW. However, as long as the magnitude of this component is kept relatively small compared with the magnitude of the voltage provided from the tank capacitor—say, no higher than about 50% thereof—the distortion of the lamp current is insufficient to cause significant deterioration of the lamp current crest factor.

(ag) Each of transistors Q1*a* and Q1*b* (as combined with their respective commutating rectifiers CR1*a* and CR1*b*) acts as a rapidly operating ON-OFF switch—current flowing through one or the other transistor, but never through both transistors at the same time. The forward conduction time of transistor Q1*b* decreases as the absolute magnitude of the negative bias voltage on bias capacitor BC1*b* increases. Thus, with the instantaneous magnitude of the DC voltage present between the DC– bus and the DC+ bus being substantially equal to that of the AC power line voltage provided from source S, the absolute magnitude of this bias voltage varies synchronously with that of the AC power line voltage; thereby, in turn, causing the effective ON-time of transistor Q1*b* to vary synchronously with the absolute magnitude of the AC power line voltage as well.

(ah) It is important that the natural resonance frequencies of the L1-C1 and the L2-C2 series-tuned circuits of FIG. 4 are lower than (or at least not higher than) the operating (or switching) frequencies of the PFCI and the BI inverters, respectively.

(ai) It is believed that the present invention and its several attendant advantages and features will be understood from the preceeding description. However, without departing from the spirit of the invention, many changes may be made in its form and in the selection, construction and interrelationships of is constituent parts, the form herein presented merely representing the presently preferred embodiment.

I claim:

1. An arrangement comprising:

rectifier device connected with a source of power line voltage and operative to provide a DC voltage at a set of DC terminals;

a power conditioner connected with the DC terminals and operative to provide a high-frequency output voltage at a high-frequency output; the high-frequency output voltage having a fundamental frequency substantially higher than that of the power line voltage; the power conditioner including an inverter circuit connected between the DC terminals and the high-frequency output; the inverter circuit being characterized by (i) including a pair of alternatingly switching transistors series-connected between the DC terminals, and (ii) producing an alternating inverter voltage of non-symmetrical waveshape across a pair of inverter terminals; the non-symmetrical waveshape having a complete cycle period including: (i) a positive part during which the magnitude of the inverter voltage remains at an approximately constant positive level; (ii) a negative part during which the magnitude of the inverter voltage remains at an approximately constant negative level; (iii) a negative-going part during which the magnitude of the inverter voltage changes rapidly from the posi-

tive level to the negative level; and (iv) a positive-going part during which the inverter voltage changes rapidly from the negative level to the positive level; the duration of the positive part being, at least at certain times, distinctly different from the duration of the negative part; the alternating inverter voltage having, irrespective of the duration of the negative part as a fraction of the duration of the positive part, an average magnitude equal to zero when averaged over the complete cycle period; and

a gas discharge lamp assembly operative to connect with the high-frequency output and to be powered by the high-frequency output voltage provided thereat.

2. The arrangement of claim 1 wherein the inverter circuit includes a control sub-circuit operative, in response to a control signal, to control the ratio between the duration of the positive part and the duration of the negative part.

3. The arrangement of claim 1 wherein the inverter circuit includes a control sub-circuit operative, in response to a control signal, to control the fundamental frequency of the alternating inverter voltage.

4. The arrangement of claim 1 wherein the inverter circuit includes a control sub-circuit operative, in response to a control signal, to control the fundamental frequency of the alternating inverter voltage as well as the ratio between the duration of the positive part and the duration of the negative part.

5. The arrangement of claim 1 wherein the inverter circuit is characterized by including an L-C tuned circuit having a natural resonance frequency at or near the fundamental frequency of the alternating inverter voltage.

6. An arrangement comprising:

rectifier means connected with a source of power line voltage and operative to provide a DC voltage at a set of DC terminals;

power conditioner means connected with the DC terminals and operative to provide a high-frequency output voltage at a high-frequency output; the high-frequency output voltage having a fundamental frequency substantially higher than that of the power line voltage; the power conditioner means including an inverter means connected in circuit between the DC terminals and the high-frequency output; the inverter means including a first and a second transistor having, respectively, a first pair and a second pair of control input terminals; the first transistor being periodically rendered conductive in response to periodic voltage pulses provided at its control terminals; each individual voltage pulse having a pulse duration; the inverter means being characterized by producing an alternating inverter voltage a pair of inverter terminals; the alternating inverter voltage having a cycle period including: (i) a first part during which the magnitude of the inverter voltage is of positive polarity; and (ii) a second part during which the magnitude of the inverter voltage is of negative polarity; the duration of the second part being distinctly longer than said pulse duration; and

gas discharge lamp means operative to connect with the high-frequency output and to be powered by the high-frequency output voltage provided thereat.

7. The arrangement of claim 6 wherein the duration of the second part is at least ten percent longer than said pulse duration.

8. The arrangement of claim 6 wherein the second transistor is: (i) periodically rendered conductive in response to periodic voltage pulses provided at its control terminals; and (ii) prevented from being rendered conductive during times when the first transistor is conductive.

9. An assembly comprising:

a rectifier sub-assembly having a pair of AC input terminals operable to be connected with the AC power line voltage of an ordinary electric utility power line and, when indeed so connected, to provide a DC voltage at a set of DC output terminals;

an inverter sub-assembly having a set of DC input terminals connected with the DC output terminals and operative to provide a high-frequency output voltage between a pair of high-frequency output terminals; the high-frequency output voltage having a fundamental frequency substantially higher than that of the AC power line voltage; the inverter sub-assembly being characterized by producing, across a pair of inverter terminals, a periodically alternating inverter voltage having a basic period consisting of: (i) a first segment during which its magnitude remains approximately constant at a positive potential; (ii) a second segment during which its magnitude decreases in a substantially continuous manner; (iii) a third segment during which its magnitude remains approximately constant at a negative potential; and (iv) a fourth segment during which its magnitude increases in a substantially continuous manner;

a gas discharge lamp connected in circuit with the high-frequency output terminals; the gas discharge lamp having a pair of thermionic cathodes, each having a pair of cathode terminals; and

a screw-base having a pair of base terminals; the screw-base, the rectifier sub-assembly, the inverter sub-assembly, and the gas discharge lamp being combined so as to constitute a lamp assembly operable to be screwed into and held by an ordinary electric lamp socket, thereby to cause said AC power line voltage to be applied to the base terminals.

10. The assembly of claim 9 wherein:

(a) the screw-base is characterized by having a standard screw-base width, which is about one inch; and

(b) the assembly is characterized by having: (i) a maximum height not exceeding eight times the standard screw-base width; and (ii) a maximum width not exceeding three times the standard screw-base width.

11. The assembly of claim 9 further characterized by having a capacitor effectively connected in parallel with the gas discharge lamp, thereby to form a lamp-capacitor parallel-combination.

12. The assembly of claim 11 still further characterized by having an inductor effectively connected in series with the lamp-capacitor parallel-combination; the inductor and the capacitor being operative to resonantly interact at the frequency of the high-frequency output voltage.

13. The assembly of claim 9 wherein the gas discharge lamp: (i) has a pair of thermionic cathodes; and (ii) is started without having been provided with preheating power to the thermionic cathodes.

14. The assembly of claim 9 wherein the gas discharge lamp: (i) has a thermionic cathode with a pair of cathode terminals; and (ii) is operated without being supplied with a cathode heating voltage across its cathode terminals.

15. The assembly of claim 9 wherein the inverter sub-assembly is further characterized by including a transistor having a pair of transistor terminals through which flows a periodic transistor current and across which exists a periodic transistor voltage; the transistor current flowing only during periods when the absolute magnitude of the transistor voltage is substantially lower than that of the DC voltage.

16. The assembly of claim 9 wherein the inverter sub-assembly is further characterized by including a transistor having a pair of transistor terminals through which periodically flows a transistor current and across which exists a periodic transistor voltage; the transistor current being prevented from flowing except during periods when the absolute magnitude of the transistor voltage is substantially lower than that of the DC voltage.

17. The assembly of claim 9 wherein: (i) the rectifier sub-assembly is further characterized by having two capacitors series-connected between the DC output terminals; and (ii) the inverter sub-assembly is further characterized by having two transistors series-connected between the DC input terminals.

18. The assembly of claim 9 wherein the periodically alternating inverter output voltage is characterized by having a trapezoidal waveform.

19. The assembly of claim 9 wherein the duration of the first segment is distincly shorter than half the duration of the basic period.

20. The assembly of claim 9 additionally characterized by comprising a cylindrical housing means: (i) onto one side of which is mounted the gas discharge lamp; (ii) onto the other side of which is mounted the screw-base; and (iii) within which is mounted said inverter sub-assembly.

21. An assembly comprising:

a rectifier & filter sub-assembly mounted within a housing means and having a pair of AC input terminals operable, by way of a screw-base integrally mounted onto the housing means and adapted to be screwed into an Edison-type incandescent lamp socket, to be connected with the AC power line voltage of an ordinary electric utility power line and, when indeed so connected, to provide a DC voltage at a set of DC output terminals;

an inverter sub-assembly also mounted, at least in part, within the housing means; the inverter sub-assembly having a set of DC input terminals connected with the DC output terminals and being operative to provide a high-frequency output voltage between a pair of high-frequency output terminals; the high-frequency output voltage having a fundamental frequency substantially higher than that of the AC power line voltage; the inverter sub-assembly being further characterized by producing, across a pair of inverter terminals, a periodically alternating inverter voltage having a basic period consisting of: (i) a first segment during which its magnitude remains essentially constant at a positive potential; (ii) a second segment during which its magnitude decreases in a substantially continuous manner; (iii) a third segment during which its magnitude remains essentially constant at a negative potential; and (iv) a fourth segment during which its magnitude increases in a substantially continuous manner; and

a gas discharge lamp mounted onto the housing means; the gas discharge lamp being connected in circuit with the high-frequency output terminals; the gas discharge lamp being further characterized by having a pair of thermionic cathodes, each having a pair of cathode terminals.

22. An assembly comprising:

a rectifier & filter sub-assembly mounted at least partly within a cylindrical housing means and having a pair of AC input terminals operable, by way of a screw-base integrally mounted onto the cylindrical housing means and adapted to be screwed into an Edison-type incandescent lamp socket, to be connected with the AC power line voltage of an ordinary electric utility power line and, when indeed so connected, to provide a DC voltage at a set of DC output terminals;

an inverter sub-assembly also mounted at least partly within the cylindrical housing means; the inverter sub-assembly having a set of DC input terminals connected with the DC output terminals and operative to provide a high-frequency output voltage between a pair of high-frequency output terminals; the high-frequency output voltage having a fundamental frequency substantially higher than that of the AC power line voltage; the inverter sub-assembly being further characterized by producing, across a pair of inverter terminals, a periodically alternating inverter voltage having a basic period consisting of: (i) a first segment during which its magnitude remains roughly constant at a positive potential; (ii) a second segment during which its magnitude decreases in a substantially continuous and gradual manner; (iii) a third segment during which its magnitude remains roughly constant at a negative potential; and (iv) a fourth segment during which its magnitude increases in a substantially continuous and gradual manner; and

a gas discharge lamp mounted onto the cylindrical housing means; the gas discharge lamp being connected in circuit with the high-frequency output terminals; the gas discharge lamp being further characterized by having a pair of thermionic cathodes, each having a pair of cathode terminals.

23. An assembly comprising:

a first sub-assembly connected with the AC power line voltage of an ordinary electric utility power line and operative to provide a DC voltage at a pair of DC output terminals;

a second sub-assembly having a first DC input terminal and a second DC input terminal, both connected with the DC output terminals; the second sub-assembly including a first transistor connected between the first DC input terminal and a center terminal, and a second transistor connected between the center terminal and the second DC input terminal; the second sub-assembly being further characterized in that it provides a periodically alternating output voltage across a pair of AC output terminals, one of which AC output terminals being the center terminal; the periodically alternating output voltage having a waveshape with a complete cycle period consisting of: (i) a positive part during which its instantaneous magnitude remains at an essentially constant positive level; (ii) a negative part during which its instantaneous magnitude remains at an essentially constant negative level; (iii) a negative-going part during which its instantaneous magnitude changes rapidly from the positive level to the negative level; and (iv) a positive-going part during which its instantaneous magnitude changes rapidly from the negative level to the positive level; the duration of the positive part being, at least under some conditions, significantly different from the duration of the negative part; and

a third sub-assembly connected with the AC output terminals and including a light-emitting gas discharge lamp.

24. The assembly of claim 23 additionally characterized by: (i) including a housing structure; (ii) having a screw-base integrally mounted on the housing structure and protruding therefrom, the screw-base being of such nature as to permit it to be screwed into and held by an Edison-type incandescent lamp socket; (iii) having at least a part of the

first sub-assembly included within the housing structure; (iv) having the light-emitting gas discharge lamp mounted on the housing structure and protruding therefrom in a direction substantially opposite of the direction along which the screw-base protrudes; the gas discharge lamp being further characterized by having a pair of thermionic cathodes, each having a pair of cathode terminals.

25. The assembly of claim 23 additionally characterized by: (i) including a housing structure; (ii) having a screw-base integrally mounted on the housing structure and protruding therefrom, the screw-base being of such nature as to permit it to be screwed into and held by an Edison-type incandescent lamp socket; (iii) having at least a part of the second sub-assembly included within the housing structure; (iv) having the light-emitting gas discharge lamp mounted on the housing means and protruding therefrom in a direction substantially opposite of the direction along which the screw-base protrudes.

26. An assembly comprising:

a rectifier sub-assembly having a pair of AC input terminals operable to be connected with the AC power line voltage of an ordinary electric utility power line and, when indeed so connected, to provide a DC voltage at a set of DC output terminals;

an inverter sub-assembly having a set of DC input terminals connected with the DC output terminals and operative to provide a high-frequency output voltage between a pair of high-frequency output terminals; the high-frequency output voltage having a fundamental frequency substantially higher than that of the AC power line voltage; the inverter sub-assembly including a transistor having a pair of transistor terminals between which flows a periodic transistor current and across which exists a periodic transistor voltage; the transistor current flowing only when the absolute magnitude of the transistor voltage is substantially lower than that of the DC voltage; the inverter sub-assembly being also characterized by producing, across a pair of inverter terminals, a periodically alternating inverter voltage having a basic period consisting of: (i) a first segment during which its magnitude remains approximately constant at a positive potential; (ii) a second segment during which its magnitude decreases in a substantially continuous manner; (iii) a third segment during which its magnitude remains approximately constant at a negative potential; and (iv) a fourth segment during which its magnitude increases in a substantially continuous manner; and

a gas discharge lamp connected in circuit with the high-frequency output terminals.

27. The arrangement of claim 26 wherein the periodic transistor current flows only during periods when the absolute magnitude of the transistor voltage is lower than half that of the DC voltage.

28. An assembly comprising:

a rectifier sub-assembly having a pair of AC input terminals operable to be connected with the AC power line voltage of an ordinary electric utility power line and, when indeed so connected, to provide a DC voltage at a set of DC output terminals;

an inverter sub-assembly having a set of DC input terminals connected with the DC output terminals and operative to provide a high-frequency output voltage between a pair of high-frequency output terminals; the high-frequency output voltage having a fundamental frequency substantially higher than that of the AC power line voltage; the inverter sub-assembly including a transistor having a pair of transistor terminals between which flows a periodic transistor current and across which exists a periodic transistor voltage; the inverter sub-assembly including circuitry operative to prevent transistor current from flowing except when the absolute magnitude of the transistor voltage is substantially lower than that of the DC voltage; the inverter sub-assembly being also characterized by producing, across a pair of inverter terminals, a periodically alternating inverter voltage having a basic period consisting of: (i) a first segment during which its magnitude remains approximately constant at a positive potential; (ii) a second segment during which its magnitude decreases in a substantially continuous manner; (iii) a third segment during which its magnitude remains approximately constant at a negative potential; and (iv) a fourth segment during which its magnitude increases in a substantially continuous manner; and

a gas discharge lamp connected in circuit with the high-frequency output terminals.

29. The arrangement of claim 28 wherein the periodic transistor current is prevented from flowing except when the absolute magnitude of the transistor voltage is lower than half that of the DC voltage.

30. The assembly of claim 28 additionally characterized by: (i) comprising a screw-base; (ii) having the screw-base, the rectifier sub-assembly, and the inverter sub-assembly combined so as to constitute a lamp assembly operable to be screwed into and held by an ordinary electric lamp socket; and (iii) having a periodically conducting transistor with a pair of control terminals across which exists an alternating control voltage having a peak-to-peak magnitude substantially higher than twice the forward voltage drop of an ordinary semiconductor junction.

31. The assembly of claim 28 additionally characterized by: (i) comprising a screw-base; (ii) having the screw-base, the rectifier sub-assembly, and the inverter sub-assembly combined so as to constitute a lamp assembly operable to be screwed into and held by an ordinary electric lamp socket; (iii) having a periodically conducting transistor with a transistor terminal; and (iv) exhibiting an electrically conductive path between the transistor terminal and one of the AC input terminals.

32. The assembly of claim 29 additionally characterized by: (i) comprising a screw-base having a base terminal connected with one of the AC input terminals and operative to connected with a terminal in an ordinary Edison-type lamp socket; (ii) having the screw-base, the rectifier sub-assembly, and the inverter sub-assembly combined so as to constitute a lamp assembly operable to be screwed into and held by an ordinary electric lamp socket; (iii) having a periodically conducting transistor with a transistor terminal; and (iv) exhibiting an electrically conductive path between the transistor terminal and at least one the AC input terminals.

* * * * *

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US005510680A

# United States Patent [19]

Nilssen

[11] Patent Number: 5,510,680

[45] Date of Patent: Apr. 23, 1996

[54] **ELECTRONIC BALLAST WITH SPECIAL VOLTAGE WAVEFORMS**

[76] Inventor: **Ole K. Nilssen**, 408 Caesar Dr., Barrington, Ill. 60010

[21] Appl. No.: **993,628**

[22] Filed: **Dec. 21, 1992**

**Related U.S. Application Data**

[63] Continuation of Ser. No. 751,587, Aug. 22, 1991, which is a continuation of Ser. No. 546,267, Jun. 29, 1990, which is a continuation-in-part of Ser. No. 787,962, Oct. 16, 1985, Pat. No. 4,700,625, which is a continuation of Ser. No. 644,155, Aug. 27, 1984, abandoned, which is a continuation of Ser. No. 555,426, Nov. 23, 1983, abandoned, which is a continuation of Ser. No. 178,107, Aug. 14, 1980, abandoned, said Ser. No. 751,587, is a continuation-in-part of Ser. No. 717,860, Jun. 19, 1991, Pat. No. 5,166,578, which is a continuation of Ser. No. 636,246, Dec. 31, 1990, abandoned, which is a continuation of Ser. No. 787,692, Oct. 15, 1985, abandoned, which is a continuation of Ser. No. 644,155, which is a continuation of Ser. No. 555,426, which is a continuation of Ser. No. 178,107, said Ser. No. 555,426, Nov. 23, 1983, is a continuation-in-part of Ser. No. 330,599, Dec. 14, 1981, Pat. No. 4,441,087, which is a continuation of Ser. No. 973,741, Dec. 28, 1978, abandoned, which is a continuation-in-part of Ser. No. 890,586, Mar. 20, 1978, Pat. No. 4,184,128, said Ser. No. 178,107, Aug. 14, 1980, is a continuation-in-part of Ser. No. 23,849, Mar. 26, 1979, Pat. No. 4,279,011.

[51] **Int. Cl.**[6] ..... **H05B 37/02**

[52] **U.S. Cl.** ..... **315/209 R**; 315/219; 315/223; 315/239

[58] **Field of Search** ..... 315/209 R, 247, 315/219, 223, 239, DIG. 7

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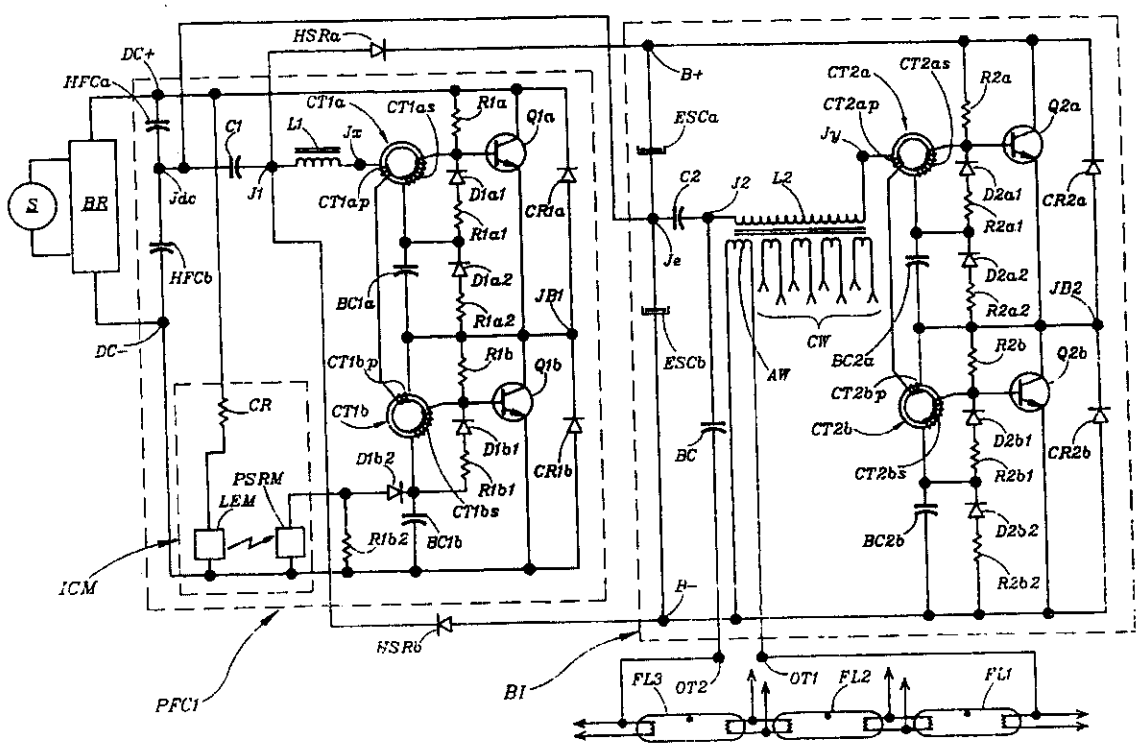
*Primary Examiner*—Frank Gonzalez
*Assistant Examiner*—Reginald A. Ratliff

[57] **ABSTRACT**

An inverter-type electronic ballast for a gas discharge lamp is powered by a DC supply voltage provided from a rectifier-filter combination connected with an ordinary electric utility power line. The absolute magnitude of the DC supply voltage is higher than the peak absolute magnitude of the power line voltage. The ballast includes an inverter circuit operative to provide an inverter output voltage of special trapezoidal-like waveshape; which output voltage is applied to a series-resonant combination of an inductor and a capacitor. The gas discharge lamp is connected in parallel with the capacitor. The inverter is driven by a voltage of special waveshape and controllable frequency. By controlling the frequency, the magnitude of the current supplied to the gas discharge lamp can be adjusted, thereby correspondingly adjusting the amount of light produced by the lamp.

**32 Claims, 3 Drawing Sheets**



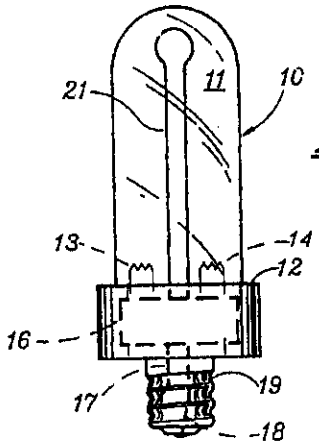



Fig. 1

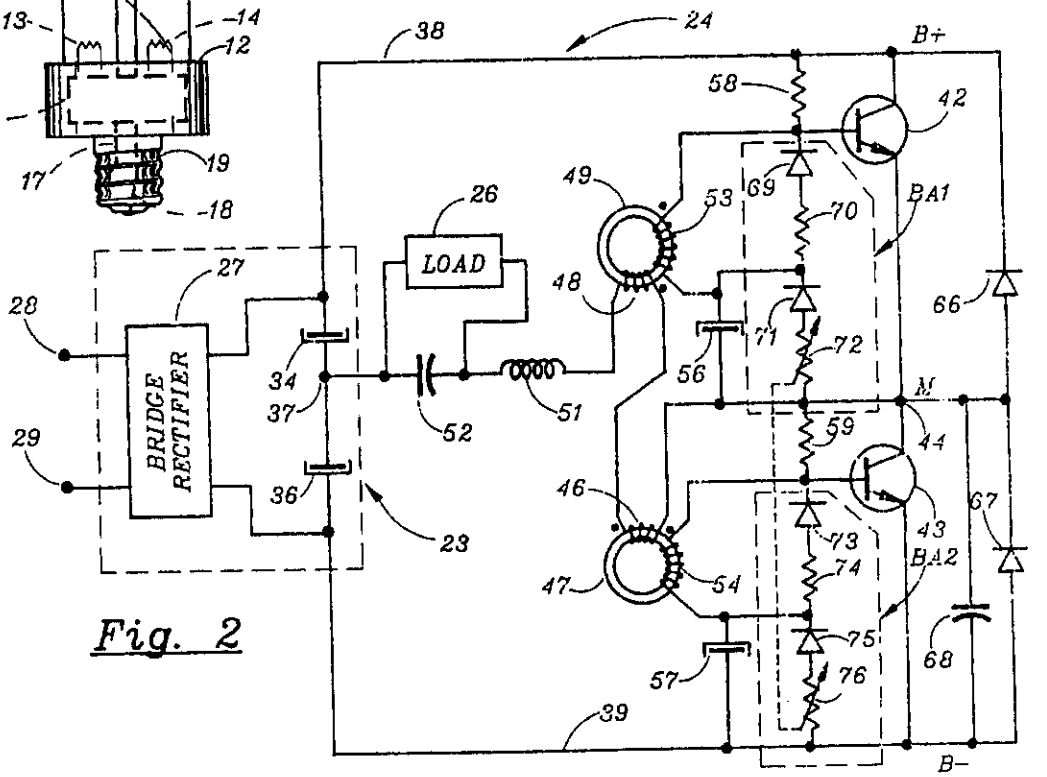



Fig. 2

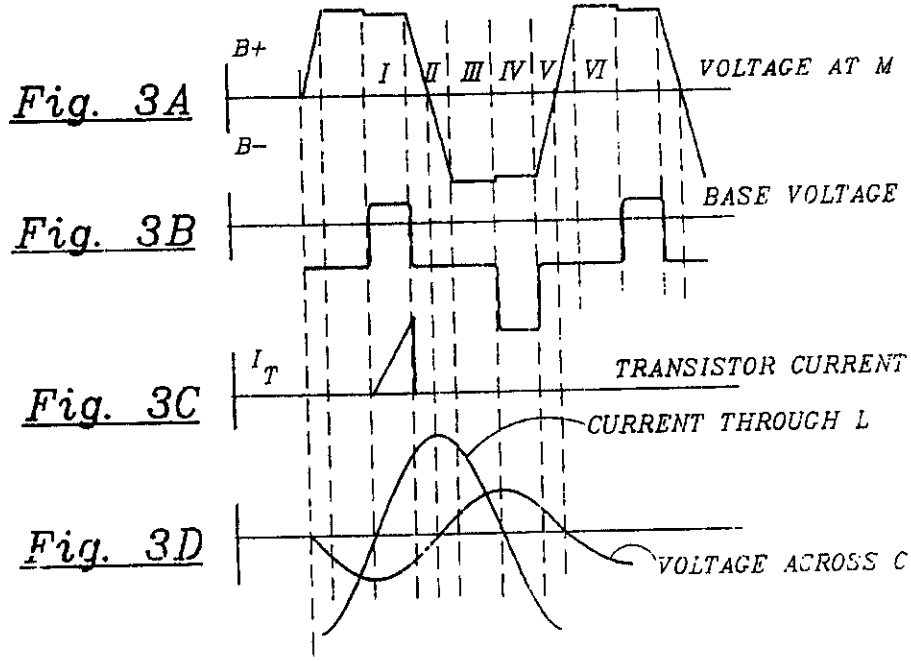



Fig. 3A

Fig. 3B

Fig. 3C

Fig. 3D

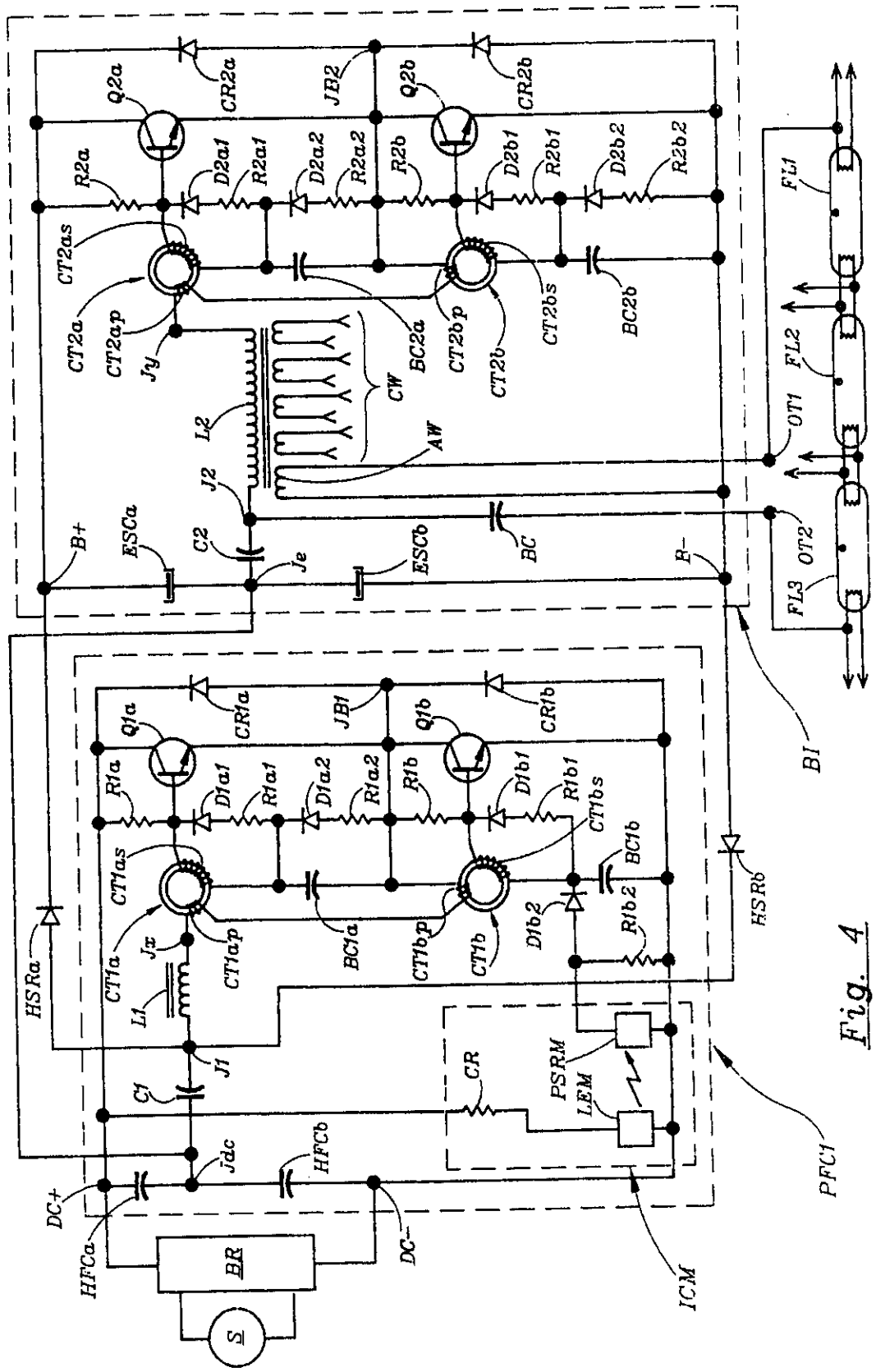

Q2a
CR2a
JB2
Q2b
CR2b
R2a
D2a1
R2a1
D2a2
R2a2
R2b
D2b1
R2b1
D2b2
R2b2
FL1
CT2as
CT2a
CT2ap
Jy
CW
BC2a
CT2bp
CT2b
CT2bs
BC2b
FL2
L2
AW
OT1
J2
C2
Je
ESCa
ESCb
BC
B+
B-
OT2
FL3
BI
Q1a
CR1a
JB1
Q1b
CR1b
R1a
D1a1
R1a1
D1a2
R1a2
R1b
D1b1
R1b1
CT1bs
CT1as
BC1b
HSRb
HSRa
CT1a
Jx
CT1ap
BC1a
CT1bp
CT1b
D1b2
R1b2
L1
J1
C1
CR
PSRM
LEM
PFC1
Jdc
HFCb
DC+
HFCa
BR
S
DC-
ICM

Fig. 4

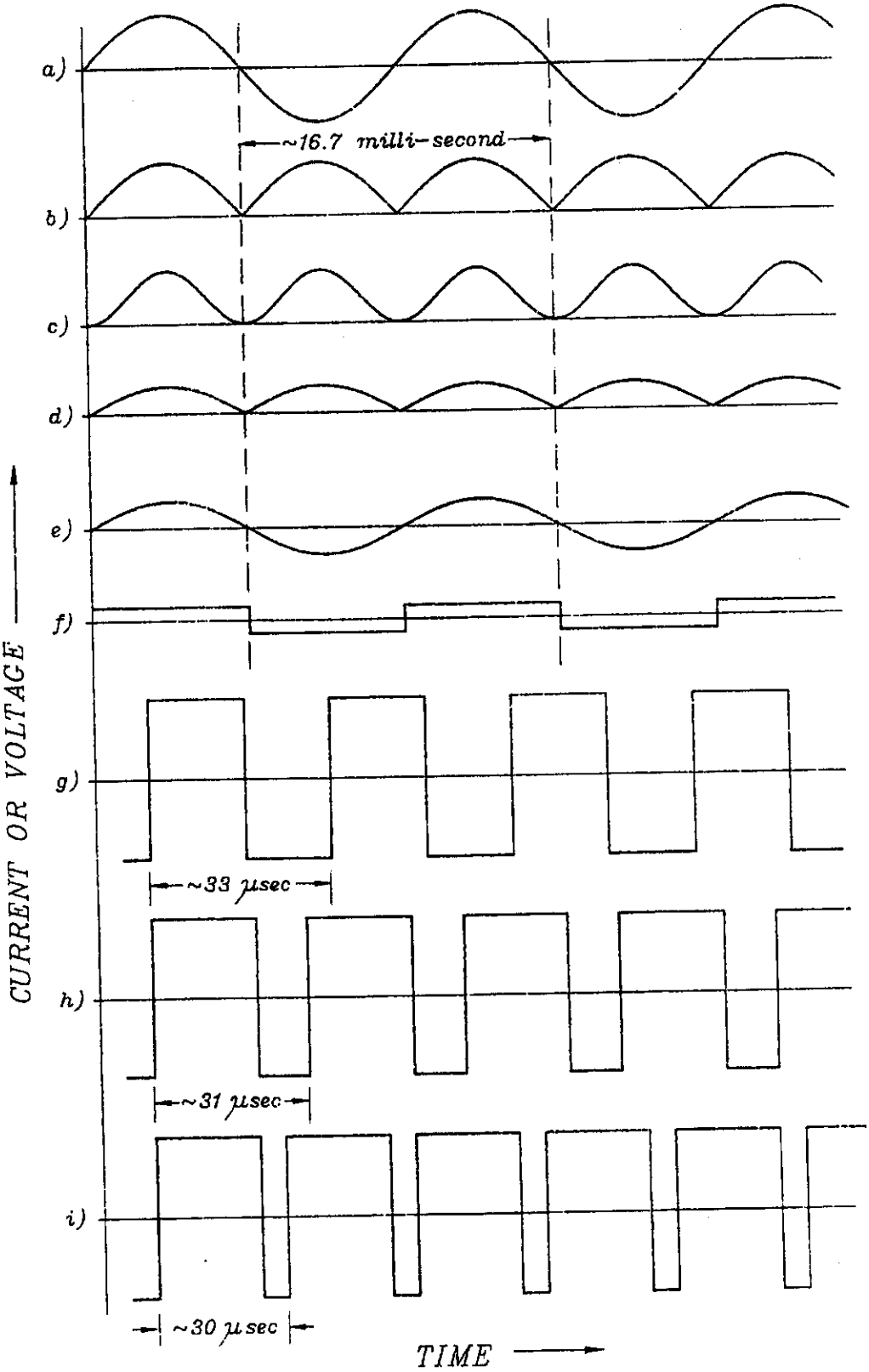

a)
~16.7 milli-second
b)
c)
d)
e)
f)
g)
~33 μsec
h)
~31 μsec
i)
~30 μsec
CURRENT OR VOLTAGE
TIME

Fig. 5

# ELECTRONIC BALLAST WITH SPECIAL VOLTAGE WAVEFORMS

## RELATED APPLICATIONS

The present application is a continuation of Ser. No. 07/751,587 filed Aug. 22, 1991; which is a continuation of Ser. No. 07/546,267 filed Jun. 29, 1990; which is a continuation-in-part of Ser. No. 06/787,962 filed Oct. 16, 1985, now U.S. Pat No. 4,700,625 which is a continuation of Ser. No. 06/644,155 filed Aug. 27, 1984, now abandoned; which is a continuation of Ser. No. 06/555,426 filed Nov. 23, 1983, now abandoned; which was a continuation of Ser. No. 06/178,107 filed Aug. 14, 1980, now abandoned;

Application Ser. No. 07/751,587 is also a continuation-in-part of Ser. No. 07/717,860 filed Jun. 19, 1991 now U.S. Pat. No. 5,166,578 which is a continuation of Ser. No. 07/636,246 filed Dec. 31, 1990, now abandoned which is a continuation of Ser. No. 06/787,692 filed Oct. 15, 1985, now abandoned; which is a continuation of Ser. No. 06/644,155 filed Aug. 27, 1984, now abandoned; which is a continuation of Ser. No. 06/555,426 filed Nov. 23, 1983, now abandoned; which is a continuation of Ser. No. 06/178,107 filed Aug. 14, 1980, now abandoned.

Application Ser. No. 06/555,426 is also a continuation-in-part of Ser. No. 06/330,599 filed Dec. 14, 1981, now U.S. Pat. No. 4,441,087; which is a continuation of Ser. No. 973,741 filed Dec. 28, 1978, now abandoned; which is a continuation-in-part of Ser. No. 890,586 filed Mar. 20, 1978, now U.S. Pat. No. 4,184,128.

Application Ser. No. 06/178,107 is also a continuation-in-part of Ser. No. 23,849 filed Mar. 26, 1979, now U.S. Pat. No. 4,279,011.

## BACKGROUND OF THE INVENTION

### Field of Invention

This invention relates to electronic ballast circuits for gas discharge lamps.

## SUMMARY OF THE INVENTION

An object of the present invention is that of providing a reliable cost-effective fluorescent lamp ballasting means.

This as well as other objects, features and advantages of the present invention will become apparent from the following description and claims.

## BRIEF DESCRIPTION

In a preferred embodiment, instant invention comprises a first half-bridge inverter that is powered from an unfiltered full-wave-rectified ordinary 60 Hz electric utility power line voltage. This first inverter provides at a first inverter output (across which is series-connected a first tuned L-C circuit) a first squarewave voltage of fundamental frequency between about 30 and 33 kHz; which first squarewave voltage is magnitude-modulated at 120 Hz.

The first tuned L-C circuit, which is series-resonant at about 30 kHz, is parallel-loaded by a full-wave high-frequency rectifier whose DC output is applied to a substantially constant-magnitude DC voltage existing across a pair of energy-storing capacitors.

At a constant 30 kHz inverter frequency, the waveshape of the current drawn from the power line is substantially that of a squarewave in phase with the power line voltage, thereby giving rise to a power factor of about 90%. However, by frequency-modulating the first inverter at 120 Hz, the waveshape of the line current is made to be substantially that of a sinewave in phase with the power line voltage, thereby giving rise to a power factor close to 100% and a total harmonic distortion of negligible magnitude.



A second half-bridge inverter is powered from the substantially constant-magnitude DC voltage and provides at a second inverter output (across which is series-connected a second tuned L-C circuit) a second squarewave voltage of fundamental frequency between about 30 and 33 kHz.

The second tuned L-C circuit, which is also series-resonant at about 30 kHz, is parallel-loaded by three series-connected fluorescent lamps. The magnitude of the current supplied to these three lamps is adjustable by adjusting the frequency of the second inverter between about 30 and 33 kHz.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 schematically illustrates a compact, screw-in, self-ballasted fluorescent lamp assembly; which lamp assembly may advantageously comprise the type of ballasting means represented by the present invention.

FIG. 2 is a schematic diagram of a half-bridge inverter and ballasting circuit of the basic type used in the preferred embodiment of the present invention.

FIGS. 3(*a–d*) illustrate the waveforms of various voltages and currents associated with the ballasting circuit of FIG. 2.

FIG. 4 illustrated the preferred embodiment of the present invention.

FIGS. 5(*a–i*) illustrate various voltage and current waveforms associated with the operation of the preferred embodiment of the present invention.

## DESCRIPTION OF THE INVENTION

FIG. 1 illustrates a screw-in gas discharge lamp unit **10** comprising a folded fluorescent lamp **11** suitably secured to an integral base **12**. The lamp comprises two cathodes **13, 14** which are supplied with the requisite high operating voltage from a frequency-converting power supply and ballasting circuit **16**; which, because of its compact size, conveniently fits within the base **12**.

Circuit **16** is connected by leads **17, 18** to a screw-type plug **19** adapted for screw-in insertion into a standard Edison-type incandescent lamp socket at which a typical 60 Hz.

In FIG. 2, a power supply **23** is connected with the 120 Volt/60 Hz power line voltage and provides a center-tapped DC output voltage for supplying a high-efficiency half-bridge inverter circuit **24**. The inverter circuit is operable to provide a high-frequency (e.g., 30 kHz) high-magnitude current-limited voltage to an external load **26**, which actually represents fluorescent lamp **11** of FIG. 1.

Power supply **23** comprises bridge rectifier **27** which connects with 120 Volt/60 Hz power line terminals **28,29** and provides full-wave rectified power line voltage to two series-connected filter capacitors **34, 36**; which filter capacitors are: (i) connected together at a center-tap **37**, and (ii) connected between positive B+ bus **38** and negative B– bus **39**.

Inverter circuit **24** is a half-bridge inverter comprising transistors **42, 43** connected in series across the DC voltage output of the power supply **23** on B+ and B– lines **38** and **39**, respectively. The collector of transistor **42** is connected to

the B+ line **38**, the emitter of transistor **42** and the collector of transistor **43** are connected to a midpoint line **44** (designated "M") and the emitter of transistor **43** is connected to the B– line **39**.

Midpoint line **44** is connected to center-tap **37** through primary winding **46** of a toroidal saturable core transformer **47**, a primary winding **48** on an identical transformer **49**, an inductor **51** and a series-connected capacitor **52**. The inductor **51** and capacitor **52** are energized upon alternate transistor conduction in a manner to be described later. Load **26** is connected in parallel with capacitor **52**.

Drive current to the base terminals of transistors **42** and **43** is provided by secondary windings **53**, **54** of transformers **49**, **47**, respectively. Winding **53** is also connected to midpoint lead **44** through a bias capacitor **56**, while winding **54** is connected to the B– lead **39** through an identical bias capacitor **57**. The base terminals of transistors **42** and **43** are also connected to lines **38** and **44** through bias resistors **58** and **59**, respectively. Shunt diodes **66** and **67** are connected across the collector-emitter terminals pf transistors **42** and **43**, respectively. A capacitor **68** is connected across the collector-emitter terminals of transistor **43** to restrain the rate of voltage rise across those terminals.

A first optional biasing arrangement BA1 comprises a diode **69** connected with its cathode to the base of transistor **42** and with its anode to the cathode of a diode **71** by way of a resistor **70**; the anode of diode **71** is connected with the emitter of transistor **42** by way of a resistor **72**; the cathode of diode **71** is connected with the un-dotted side of secondary winding **53** of transformer **49**. A second optional biasing arrangement BA2 comprises a diode **73** connected with its cathode to the base of transistor **43** and with its anode to the cathode of a diode **75** by way of a resistor **74**; the anode of diode **76** is connected with the emitter of transistor **42** by way of a resistor **72**; the cathode of diode **71** is connected with the un-dotted side of secondary winding **54** of transformer **47**.

## Details of Operation of the FIG. 2 Circuit

The operation of the circuit of FIG. **2** can best be understood with additional reference to FIG. **3**, which illustrates significant portions of the waveforms of the voltage at midpoint M (FIG. **3A**), the base-emitter voltage on transistor **42** (FIG. **3B**), the current through transistor **42** (FIG. **3C**), and the capacitor **52** voltage and the inductor **51** current (FIG. **3D**).

Starting at a paint where transistor **42** first starts to conduct, current flows from the B+ line **38** through windings **46** and **48** and inductor **51** to charge capacitor **52** and returns to the B+ line through capacitor **34** (refer to the time period designated I in FIG. **3**). When the saturable inductor **49** saturates at the end of period I, drive current to the base of transistor **42** will terminate, causing voltage on the base of the transistor to drop to the negative voltage stored on the bias capacitor **56** in a manner to be described, causing this transistor to become non-conductive. As shown in FIG. **3***c*, current-flow in transistor **43** terminates at the end of period I.

However, since the current flowing through inductor **51** cannot change instantaneously, this current will now continue to flow from the B– bus **39** through capacitor **68**, eventually causing the voltage at midpoint line **44** to drop to the voltage level of the B– bus (period II in FIG. **3**). Thus, capacitor **68** restrains the rate of voltage change across the collector and emitter terminals of transistor **42**.

The current through the inductor **51** reaches its maximum value when the voltage at the midpoint line **44** is zero. During period III, the current will continue to flow through inductor **51** but will be supplied from the B– bus through the shunt diode **67**. It will be appreciated that during the latter half of period II and all of period III, positive current is being drawn from a negative voltage; which, in reality, means that energy is being returned to the power supply through a path of relatively low impedance.

When the inductor current reaches zero at the start of period IV, the current through the primary winding **46** of the saturable inductor **47** will cause a current to flow out of its secondary winding **54** to cause transistor **43** to become conductive, thereby causing a reversal in the direction of current through inductor **51** and capacitor **52**. When transformer **47** saturates at the end of period IV, the drive current to the base of transistor **43** terminates and the current through inductor **51** will be supplied through capacitor **68**, causing the voltage at midpoint line **44** to rise (period V). When the voltage at the midpoint line M reaches the voltage on the B+ bus, the current will then flow through shunt diode **66** (period VI). The cycle is then repeated.

As seen in FIG. **3**, the saturable inductors **47**, **49** provide transistor drive current only after the current through inductor **51** has diminished to zero. Further, the transistor drive current is terminated before the current through inductor **51** has reached its maximum amplitude. This coordination of base drive current and inductor current is achieved because of the series-connection between the inductor **51** and the primary windings **46**, **48** of saturable transformers **47**, **49**, respectively.

The series-connected combination of the inductor **51** and the capacitor **52** is energized upon the alternate conduction of transistors **42** and **43**. With a large value of capacitance of capacitor **52**, very little voltage will be developed across its terminals. As the value of this capacitance is decreased, however, the voltage across this capacitor will increase. As the value of the capacitor **52** is reduced to achieve resonance with the inductor **51**, the voltage on the capacitor will rise and become infinite in a loss-free circuit operating under ideal conditions.

It has been found desirable to regulate the transistor inversion frequency, determined mainly by the saturation time of the saturable inductors **47**, **49**, to be equal to or higher than the natural resonance frequency of the inductor and capacitor combination in order to provide a high voltage output to external load **26**.

Due to so-called Q-multiplication, a high-magnitude voltage develops across capacitor **52** as the transistor inversion frequency approaches the natural resonance-frequency of the series-combination of inductor **51** and capacitor **52**.

When inverter circuit **24** is used in the self-ballasted fluorescent lamp of FIG. **1**, it has been found that the inversion frequency may be about equal to the natural resonance frequency of the series L-C tank circuit consisting of inductor **51** and capacitor **52**. However, if the capacitance value of capacitor **52** is reduced below the point of resonance, unacceptably high transistor currents will result and transistor burn-out will occur.

The sizing of capacitor **52** is determined by the particular application of inverter circuit **24**; but as long as the combined load (i.e., as represented to the output of inverter transistors **42**, **43**) has an effective inductance value sufficient to provide adequate energy storage for self-sustained transistor inverter action, the current-feedback provided by saturable transformers **47**, **49** will effect alternate transistor conduction without the need for additional voltage feedback.

Because the voltages across transistors **42**, **43** are of relatively low magnitude (due to the absolute voltage-clamping effect of capacitors **34**, **36**), the half-bridge inverter **24** is very reliable. The absence of switching transients minimizes the possibility of transistor burn-out.

Inverter circuit **24** comprises means for supplying reverse bias to a conducting transistor upon saturation of its associated saturable transformer. For this purpose, capacitors **56**, **57** are charged to negative voltages as a result of reset currents flowing into secondary windings **53**, **54** from the bases of transistors **42**, **43**, respectively. This reverse current rapidly turns off a conducting transistor to increase its switching speed and to achieve high inverter switching efficiency.

When a transistor base-emitter junction is reversely biased, it exhibits the characteristics of a Zener diode, having a reverse breakdown (i.e., Zenering) voltage on the order of 8 to 14 Volt for transistors typically used in high-voltage inverters.

Since liad **56** comprises a fluorescent lamp, the maximum magnitude of the voltage across capacitor **52** will be limited by the lamp's ignition and operating characteristics, thereby effectively preventing voltages across inductor **51** and capacitor **52** from ever reaching destructive levels.

The above-presented explanation of the operation of the FIG. **2** inverter circuit was based on the two biasing arrangements (BA1 and BA2) being non-connected.

With these biasing arrangements actually connected as indicated, the inverter's operation will become independent of the exact magnitude of the transistors' base-emitter Zenering voltages. Instead, the magnitude of the negative bias voltage established on each of capacitors **56** and **57** can now be chosen by choice of resistance value of resistor **72** and/or resistor **76**: the lower the resistance value, the lower the magnitude of the associated negative bias voltage; and, in turn, the longer the transistors' ON-time, the lower the inverter's self-oscillating frequency, and the higher the magnitudes of the inverter's output current and power.

By providing for means whereby the resistance values of resistors **72** and **76** can be manually adjusted (in tandem and/or individually), the power provided to the fluorescent lamp may be correspondingly adjusted: the lower the resistance values, the more power provided to the lamp.

Moreover, due to the negative feedback effect inherently provided by resistors **72** and **74**, the inverter may be made to operate safely even with the fluorescent lamp being non-connected.

This negative feedback effect is due to the fact that, as the magnitude of the current flowing through the L-C circuit increases, the magnitudes of the drive currents provided to the transistors' bases increase, and the magnitudes of the currents drawn out of capacitors **56** and **57** increase correspondingly; which, in turn, increase the magnitudes of the negative bias voltages present on these capacitors to the point where the magnitudes of the currents flowing through resistors **72** and **76** equal those of the increased base currents. However, the increased negative bias voltage will inherently shorten the transistors' ON-times; which, in turn, will increase the inverter frequency, thereby reducing the inverter's output current; etc. In other words, the indicated biasing arrangements provide for an automatic self-limiting of the magnitude of the inverter's output current.

Additional Comments re the FIG. **2** Circuit

(a) With commonly available components, inverter circuit **24** can be made to operate efficiently at any frequency between a few kHz to perhaps as high as 50 kHz. However, for various well-known reasons (i.e., eliminating audible noise, minimizing physical size, and maximizing efficiency), the frequency actually chosen for the lamp unit of FIG. **1** was in the range of 20 to 30 kHz.

(b) The fluorescent lighting unit of FIG. **1** could be made in such manner as to permit fluorescent lamp **11** to be disconnectable from its base **12** and ballasting means **16**. However, if powered with normal line voltage without its lamp load connected, frequency-converting power supply and ballasting circuit **16** is apt to self-destruct.

To avoid self-destruction, arrangements can readily be made whereby the very act of removing the load automatically establishes a situation that prevents the possible destruction of the power supply and the ballasting means. For instance, with the tank capacitor (**52**) being permanently connected with the lamp load (**11**)—thereby automatically being removed whenever the lamp is removed—the inverter circuit is protected from self-destruction.

(c) At frequencies above a few kHz, the load represented by a fluorescent lamp—once it is ignited—is substantially resistive. Thus, with the voltage across lamp **11** being oa a substantially sinusoidal waveform (as indicated in FIG. **3***d*), the current through the lamp will also be substantially sinusoidal in waveshape.

(d) In the fluorescent lamp unit of FIG. **1**, fluorescent lamp **11** is connected with power supply and ballasting circuit **16** in the exact same manner as is load **26** connected with the circuit of FIG. **2**. That is, it is connected in parallel with the tank capacitor (**52**) of the L-C series-resonant circuit. As is conventional in instant-start fluorescent lamps—such as lamp **11** of FIG. **1**—the two terminals from each cathode are shorted together, thereby to constitute a situation where each cathode effectively is represented by only a single terminal. However, it is not necessary that the two terminals from each cathode be shorted together; in which case—for instant-start operation—connection of a lamp's power supply and ballasting means need only be made with one of the terminals of each cathode.

(e) It is noted that the transistor's ON-time is shorter than half the period of the inverter's high frequency squarewave voltage output; which voltage output is illustrated by FIG. **3A**.

The fact that each of the transistors' ON-times is shorter than half the period of the inverter's high frequency output voltage (or output current) is important: it inherently provides for a situation where the two transistors are manifestly prevented from conducting at the same time, thereby providing protection against circuit failure due to excess-magnitude transistor currents.

(f) By adjusting the resistance values of resistors **72** and/or **72**, the ON-times of the associated transistors are adjusted accordingly. For instance, by increasing the resistance value of resistor **76**, the ON-time associated with transistor **43** is shortened; and, as a result, the magnitude of the current provided to the load **26** is reduced.

Details of Construction of the Preferred Embodiment

In FIG. **4**, a source S represents an ordinary electric utility power line providing 120 Volt/60 Hz power line voltage to the input of bridge rectifier BR, whose DC output is applied between a DC– bus and a DC+ bus.

A high-frequency filter capacitor HFCa is connected between a junction Jdc and the DC+ bus; a high-frequency

filter capacitor HFCb is connected between the DC– bus and junction Jdc.

A tank capacitor C1 is connected between junction Jdc and a junction J1; a tank inductor L1 is connected between junction J1 and a junction Jx.

A transistor Q1*a* is connected with its collector to the DC+ bus and with its emitter to a junction bus JB1; a transistor Q1*b* is cojnected with its collector to junction bus JB1 and with its emitter to the DC– bus. A commutating rectifier CR1*a* is connected with its cathode to the DC+ bus and with its anode to junction bus JB1; a commutating rectifier CR1*b* is connected with its cathode to junction bus JB1 and with its anode to the DC– bus.

Primary windings CT1*ap* and CT1*bp* of saturable current transformers CT1*a* and CT1*b*, respectively, are series-connected between junctions Jx and junction bus JB1.

Secondary winding CT1*as* of transformer CT1*a* is connected between the base of transistor Q1*a* and the cathode of a diode D1*a*2, whose anode is connected with junction bus JB1 via a resistor R1*a*2. A diode D1*a*1 is connected with its cathode to the base of transistor Q1*a* and with its anode to the cathode of diode D1*a*2 via a resistor R1*a*1. A resistor R1*a* is connected between the DC+ bus and the base of transistor Q1*a*. A bias capacitor BC1*a* is connected between the cathode of diode D1*a*2 and junction bus JB1.

Secondary winding CT1*bs* of transformer CT1*b* is connected between the base of transistor Q1*b* and the cathode of a diode D1*b*2, whose anode is connected with the DC– bus via a resistor R1*b*2. A diode D1*b*1 is connected with its cathode to the base of transistor Q1*b* and with its anode to the cathode of diode D1*b*2 via a resistor R1*b*1. A resistor R1*b* is connected between junction bus JB1 and the base of transistor Q1*b*. A bias capacitor BC1*b* is connected between the cathode of diode D1*b*2 and the DC– bus.

A high-speed rectifier HSRa is connected with its anode to junction J1 and with its cathode to a B+ bus; a high-speed rectifier HSRb is connected with its cathode to junction J1 and with its anode to a B– bus.

An energy-storing capacitor ESCa is connected between a junction Je and the B+ bus, junction Je being connected with junction Jdc; an energy-storing capacitor ESCb is connected between junction Je and the B– bus.

A tank capacitor C2 is connected between junction Je and a junction J2; a tank inductor is connected between junction J2 and a junction Jy.

A transistor Q2*a* is connected with its collector to the B+ bus and with its emitter to a junction bus JB2; a transistor Q2*b* is connected with its collector to junction bus JB2 and with its emitter to the B– bus. A commutating rectifier CR2*a* is connected with its cathode to the B+ bus and with its anode to junction bus JB2; a commutating rectifier CR2*b* is connected with its cathode to junction bus JB2 and with its anode to the B– bus.

Primary windings CT2*ap* and CT2*bp* of saturable current transformers CT2*a* and CT2*b*, respectively, are series-connected between junction Jy and junction bus JB2.

Secondary winding CT2*as* of transformer CT2*a* is connected between the base of transistor Q2*a* and the cathode of a diode D2*a*2, whose anode is connected with junction bus JB2 via a resistor R2*a*2. A diode D2*a*1 is connected with its cathode to the base of transistor Q2*a* and with its anode to the cathode of diode D2*a*2 via a resistor R2*a*1. A resistor R2*a* is connected between the B+ bus and the base of transistor Q2*a*. A bias capacitor BC2*a* is connected between the cathode of diode D2*a*2 and junction bus JB2.

Secondary winding CT2*bs* of transformer CT2*b* is connected between the base of transistor Q2*b* and the cathode of a diode D2*b*2, whose anode is connected with the B– bus via a resistor R2*b*2. A diode D2*b*1 is connected with its cathode to the base of transistor Q2*b* and with its anode to the cathode of diode D2*b*2 via a resistor R2*b*1. A resistor R2*b* is connected between junction bus JB2 and the base of transistor Q2*b*. A bias capacitor BC2*b* is connected between the cathode of diode D2*b*2 and the B– bus.

An auxiliary winding AW is wound as a loosely coupled secondary winding on tank inductor L2 and connected between the B– bus and an output terminal OT1. A DC blocking capacitor BC is connected between junction J2 and an output terminal OT2.

Also wound on tank inductor L2 are four cathode windings CW; which four cathode windings are connected with corresponding pairs of cathode terminals of three series-connected fluorescent lamps FL1, FL2 and FL3; which three fluorescent lamps are series-connected across output terminals OT1 and OT2.

An inverter control means ICM is connected between the DC– bus and the DC+ bus, as well as with the anode of diode D1*b*2; which inverter control means consists of: (i) a photo-sensitive resistive means PSRM connected between the anode of diode D1*b*2 and the DC– bus; and (ii) a light-emitting means LEM, such as a light-emitting diode (or LED), connected in series with a control resistor CR between the DC– bus and the DC+ bus. Light-emitting means LEM is so positioned and arranged that its light output impinges on a light-receptive part of photo-sensitive resistive means PSRM.

The half-bridge inverter with Q1*a* and Q1*b* as its switching transistors is identified as power-factor-correcting inverter PFCI; and the half-bridge inverter with Q2*a* and Q2*b* as its switching transistors is identified as ballast inverter BI.

## Details of Operation of the Preferred Embodiment

The operation the preferred embodiment of instant invention may best be understood when read with reference to FIG. 5; which illustrates various current and voltage waveforms associated with the operation of the circuit arrangement of FIG. 4.

With reference to the waveforms of FIG. 5 and the circuit arrangement of FIG. 4, as long as the magnitude of the DC voltage existing between the B– bus and the B+ bus remains substantially constant, waveform: (a) represents that of the 120 Volt/60 Hz power line voltage supplied from source S; (b) represents the corresponding DC voltage present between the DC– bus and the DC+ bus; (c) represents the net current provided via high-speed rectifiers HSRa and HSRb to energy-storing capacitors ESCa and ESCb; (d) represents the current drawn from the DC output of bridge rectifier BR; and (e) represents the waveform of the current drawn from source S. Waveform (f) represents the current that would be drawn from source S in case the light from light-emitting means LEM were to be kept at a constant intensity, such as would occur if a filter capacitor were to be connected thereacross.

The two half-bridge inverters (PFCI and BI) both operate in the same basic manner as does the half-bridge inverter of FIG. 2.

In case of the PFCI inverter, the load constitutes the substantially constant-magnitude DC voltage present across energy-storing capacitors ESCa and ESCb; in case of the BI

inverter, the principal load constitutes the three series-connected fluorescent lamps FL1, FL2 and FL3.

In the overall operation of the circuit of FIG. 4, the PFCI inverter continually charges the two energy-storing capacitors (ESCa/ESCb), while the BI inverter continually discharges these same energy-storing capacitors. Thus, the magnitude of the DC voltage across these energy-storing capacitors will stabilize at a point where the average rate of capacitor-charging equals the average rate of capacitor-discharging.

While the average rate of capacitor-charging is essentially fixed for a given magnitude of the voltage supplied by the source (S), the average rate of capacitor-discharging increases with increasing magnitude of the DC voltage present across the energy-storing capacitors (i.e., between the B– bus and the B+ bus).

Absent any control by inverter control means ICM, a basic characteristic of the series-driven parallel-loaded PFCI inverter powering a constant-voltage-magnitude load, such as indeed represented by capacitors ESCa/ESCb, is that the instantaneous magnitude of the current provided to this load will be roughly proportional to the instantaneous magnitude of the DC voltage powering the inverter. Thus, absent control, the magnitude of the charging current supplied to capacitors ESCa/ESCb will vary in proportion with the magnitude of the DC voltage present between the DC– bus and the DC+ bus.

However, another basic characteristic of the PFCI inverter is that, with a constant-magnitude DC voltage present between the DC– bus and the DC+ bus, the magnitude of the charging current supplied to capacitors ESCa/ESCb is roughly proportional to the conductance of photo-sensitive resistive means PSRM; which, in turn, is roughly proportional to the amount of light emitted from light-emitting means LEM; which, in turn, is roughly proportional to the magnitude of the current flowing through light-emitting means LEM; which, in turn, is roughly proportional to the magnitude of the DC voltage present between the DC– bus and the DC+ bus.

Thus, with the amount of light emitted by light-emitting means LEM being roughly proportional to the instantaneous magnitude of the DC voltage present between the DC– bus and the DC+ bus, the instantaneous magnitude of the charging current supplied to capacitor ESCa/ESCb will be roughly proportional to the square of the instantaneous magnitude of that DC voltage.

As an overall consequence, the instantaneous magnitude of the cur rent drawn by the PFCI inverter will be roughly proportional to the instantaneous magnitude of the DC voltage present between the DC– bus and the DC+ bus; which is to say that the instantaneous magnitude of the current drawn from the power line (i.e., source S) will be proportional to the instantaneous magnitude of the voltage provided from the power line; which, in turn, provides for the power drawn from the power line by the circuit arrangement of FIG. 4 to exhibit a power factor close to unity (i.e., 100%). Moreover, the waveform of the current drawn from the power line will exhibit an exceptionally low degree of harmonic distortion.

In effecting its control action, inverter control means ICM causes both symmetry-modulation and frequency-modulation of the inverter output voltage provided between junction Jdc and junction Jx. As illustrated by FIG. 5(*g*), this inverter output voltage is a nearly symmetrical squarewave of a certain frequency (about 30 kHz) whenever the instantaneous magnitude of the DC voltage between the DC– bus and the DC+ bus is at its maximum (about 170 Volt). However, with the instantaneous magnitude of this DC voltage being about half its maximum, the inverter output voltage—as illustrated by FIG. 5(*h*)—is a clearly asymmetrical squarewave. Moreover, its frequency is now higher (about 32 kHz). As indicated by FIG. 5(*i*), at a still lower magnitude of the DC voltage between the DC– bus and the DC+ bus, the inverter output voltage is still more asymmetrical and of still higher frequency.

Thus, the PFCI inverter effects its control action by a combination of symmetry-modulation and frequency-modulation.

Increasing frequency—other things being equal—provides for reduced-magnitude charging current to energy-storing capacitors ESCa/ESCb. This is so for the reason that the natural series-resonance-frequency of the L2-C2 tuned circuit is below the inverter's actual frequency

Increasing asymmetry—other things being equal—also provides for reduced-magnitude charging current to energy-storing capacitors ESCa/ESCb. This is so for the reason that the magnitude of the fundamental frequency component of the inverter's output voltage decreases roughly in proportion to the degree of asymmetry.

As the degree of conductance of photo-sensitive resistive means PSRM increases, the magnitude of the negative bias voltage present across bias capacitor BC1*b* decreases; which results in a longer ON-time for transistor Q1*b*.

As for the BI inverter, the operation is substantially as described in connection with the circuit of FIG. 2, except for the particular feature associated with auxiliary winding AW.

The phasing of the AW winding is such that the fundamental frequency component of the high-frequency voltage provided at output terminal OT1 is substantially out-of-phase with the high-frequency voltage provided at output terminal OT2. That way, the magnitude of the net voltage provided across the three series-connected lamps is larger than it would be if the lamps had been connected directly across tank capacitor C2.

In case of ordinary F40 or F34 T-12 Rapid-Start fluorescent lamps, each lamp requires an operating voltage of RMS magnitude equal to about 100 Volt; which implies a total RMS magnitude of about 300 Volt across the three series-connected lamps.

To reduce potentially dangerous electric shock effects, as might result from capacitive coupling directly from the glass envelope of the fluorescent tube to the hand of a person installing and/or removing the fluorescent lamps from their sockets, it is important that the magnitude of the lamp's arc voltage be not much higher than about 200 Volt RMS (at about 30 kHz) with respect to ground. If it were to exceed this 200 Volt RMS magnitude, a person might receive a potentially hazardous electric shock effect merely from grabbing the fluorescent tube at a point where the potential of the ionized gas inside the glass envelope were higher than 200 Volt RMS with respect to ground.

In the particular arrangement of FIG. 4, the maximum magnitude of the 30 kHz potential of the ionized gas within the fluorescent glass tube is indeed maintained below approximately 200 Volt RMS with respect to ground, in spite of the fact that the three lamps require an operating voltage of 300 Volt RMS magnitude. This result has been achieved by way of the AW winding, whose output voltage—during lamp operation—is about 100 Volt RMS with respect to the B– bus; which, with respect to the 30 kHz inverter voltage, is indeed at ground potential.

On the other hand, the magnitude of the voltage contributed by the AW winding should be as low as reasonably

possible for the reason that its waveform is of such nature as to cause degradation of the lamp current crest factor; which degradation is due to the fact that—contrary to the case with the voltage across the tank capacitor (C2)—the waveshape of the voltage present across the tank inductor (L2) includes the full magnitude of the squarewave voltage provided at the inverter's output (i.e., the voltage provided between junctions Je and Jy).

With the DC voltage provided between the B– bus and the B+ bus being of substantially constant magnitude, the lamp current crest factor would be about 1.5 if the lamps were to have been connected directly across the tank capacitor. However, had the lamps instead been connected directly across the tank inductor, the lamp current crest factor would have been far in excess of 1.7; which is normally considered the maximum permissible level for lamp current crest factor. On the other hand, with only one third of the lamp voltage derived from the tank inductor voltage, and with the remaining two thirds being derived from the tank capacitor voltage, the net resulting lamp current crest factor is kept just below 1.7—as is indeed the case in the arrangement of FIG. 4.

Additional Comments

(aa) The reason that the AW winding is loosely coupled with tank inductor L2 is related to minimizing detrimental effects on lamp current crest factor due to powering the lamps in part by the tank inductor voltage. By effectively providing the tank inductor voltage to the fluorescent lamp via a series inductance, the detrimental effects on lamp current crest factor are indeed reduced. However, the same result can be obtained by placing an inductor in series with the fluorescent lamps.

(ab) Light-emitting means LEM is likely not to be totally linear in terms of light output as function of the magnitude of the driving DC current. Likewise, photo-sensitive resistive means is likely not to be totally linear with respect to its effective conductance versus amount of light received. In addition, the symmetry-modulation and frequency-modulation resulting from changes in the conductance of the photo-sensitive resistive means are not likely to be totally linear.

However, it is not necessary that these various relationships be totally linear. Instead, the largest part of the sought-after effect—namely power factor correction and reduction of power line harmonics—will result even if the various relationships be quite non-linear.

Of course, by carefully selecting and matching the non-linearities of the different effects, as well as by introducing various linearizing means, nearly any desired degree of final power factor correction can be achieved.

(ac) The time constant associated with bias capacitor BC1*b* and its associated charge leakage means—namely resistor R1*b*2 and photo-sensitive resistive means PSRM—must be long with respect to a complete cycle of the 30 kHz inverter frequency. However, this time constant should be short compared with a complete cycle of the 120 Hz ripple voltage on the DC voltage present between the DC– bus and the DC+ bus.

(ad) The waveshape of the high-frequency current flowing from tank capacitor C1 of FIG. 4 is substantially sinusoidal— with the positive halves flowing though rectifier HSRa and the negative halves flowing through rectifier HSRb.

(ae) The absolute instantaneous magnitude of the high-frequency current flowing from junction J1 and through rectifiers HSRa and HSRb is—except for any imperfections in the HSRa/HSRb rectifiers—equal to that of the net DC current flowing into energy-storing capacitors ESCa and ESCb.

(af) The waveshape of the current flowing through the three series-connected fluorescent lamps is also nearly sinusoidal; except that a modest degree of distortion is introduced by the harmonics of the component of high-frequency voltage provided by auxiliary winding AW. However, as long as the magnitude of this component is kept relatively small compared with the magnitude of the voltage provided from the tank capacitor—say, no higher than about 50% thereof—the distortion of the lamp current is insufficient to cause significant deterioration of the lamp current crest factor.

(ag) Each of transistors Q1*a* and Q1*b* (as combined with their respective commutating rectifiers CR1*a* and CR1*b*) acts as a rapidly operating ON-OFF switch—current flowing through one or the other transistor, but never through both transistors at the same time. The forward conduction time of transistor Q1*b* decreases as the absolute magnitude of the negative bias voltage on bias capacitor BC1*b* increases. Thus, with the instantaneous magnitude of the DC voltage present between the DC– bus and the DC+ bus being substantially equal to that of the AC power line voltage provided from source S, the absolute magnitude of this bias voltage varies synchronously with that of the AC power line voltage; thereby, in turn, causing the effective ON-time of transistor Q1*b* to vary synchronously with the absolute magnitude of the AC power line voltage as well.

(ah) It is important that the natural resonance frequencies of the L1-C1 and the L2-C2 series-tuned circuits of FIG. 4 are lower than (or at least not higher than) the operating (or switching) frequencies of the PFCI and the BI inverters, respectively.

(ai) It is believed that the present invention and its several attendant advantages and features will be understood from the preceeding description. However, without departing from the spirit of the invention, many changes may be made in its form and in the selection, construction and interrelationships of is constituent parts, the form herein presented merely representing the presently preferred embodiment.

I claim:

1. An arrangement comprising:

rectifier device connected with a source of power line voltage and operative to provide a DC voltage at a set of DC terminals;

a power conditioner connected with the DC terminals and operative to provide a high-frequency output voltage at a high-frequency output; the high-frequency output voltage having a fundamental frequency substantially higher than that of the power line voltage; the power conditioner including an inverter circuit connected between the DC terminals and the high-frequency output; the inverter circuit being characterized by (i) including a pair of alternatingly switching transistors series-connected between the DC terminals, and (ii) producing an alternating inverter voltage of non-symmetrical waveshape across a pair of inverter terminals; the non-symmetrical waveshape having a complete cycle period including: (i) a positive part during which the magnitude of the inverter voltage remains at an approximately constant positive level; (ii) a negative part during which the magnitude of the inverter voltage remains at an approximately constant negative level; (iii) a negative-going part during which the magnitude of the inverter voltage changes rapidly from the posi-

tive level to the negative level; and (iv) a positive-going part during which the inverter voltage changes rapidly from the negative level to the positive level; the duration of the positive part being, at least at certain times, distinctly different from the duration of the negative part; the alternating inverter voltage having, irrespective of the duration of the negative part as a fraction of the duration of the positive part, an average magnitude equal to zero when averaged over the complete cycle period; and

a gas discharge lamp assembly operative to connect with the high-frequency output and to be powered by the high-frequency output voltage provided thereat.

2. The arrangement of claim 1 wherein the inverter circuit includes a control sub-circuit operative, in response to a control signal, to control the ratio between the duration of the positive part and the duration of the negative part.

3. The arrangement of claim 1 wherein the inverter circuit includes a control sub-circuit operative, in response to a control signal, to control the fundamental frequency of the alternating inverter voltage.

4. The arrangement of claim 1 wherein the inverter circuit includes a control sub-circuit operative, in response to a control signal, to control the fundamental frequency of the alternating inverter voltage as well as the ratio between the duration of the positive part and the duration of the negative part.

5. The arrangement of claim 1 wherein the inverter circuit is characterized by including an L-C tuned circuit having a natural resonance frequency at or near the fundamental frequency of the alternating inverter voltage.

6. An arrangement comprising:

rectifier means connected with a source of power line voltage and operative to provide a DC voltage at a set of DC terminals;

power conditioner means connected with the DC terminals and operative to provide a high-frequency output voltage at a high-frequency output; the high-frequency output voltage having a fundamental frequency substantially higher than that of the power line voltage; the power conditioner means including an inverter means connected in circuit between the DC terminals and the high-frequency output; the inverter means including a first and a second transistor having, respectively, a first pair and a second pair of control input terminals; the first transistor being periodically rendered conductive in response to periodic voltage pulses provided at its control terminals; each individual voltage pulse having a pulse duration; the inverter means being characterized by producing an alternating inverter voltage a pair of inverter terminals; the alternating inverter voltage having a cycle period including: (i) a first part during which the magnitude of the inverter voltage is of positive polarity; and (ii) a second part during which the magnitude of the inverter voltage is of negative polarity; the duration of the second part being distinctly longer than said pulse duration; and

gas discharge lamp means operative to connect with the high-frequency output and to be powered by the high-frequency output voltage provided thereat.

7. The arrangement of claim 6 wherein the duration of the second part is at least ten percent longer than said pulse duration.

8. The arrangement of claim 6 wherein the second transistor is: (i) periodically rendered conductive in response to periodic voltage pulses provided at its control terminals; and (ii) prevented from being rendered conductive during times when the first transistor is conductive.

9. An assembly comprising:

a rectifier sub-assembly having a pair of AC input terminals operable to be connected with the AC power line voltage of an ordinary electric utility power line and, when indeed so connected, to provide a DC voltage at a set of DC output terminals;

an inverter sub-assembly having a set of DC input terminals connected with the DC output terminals and operative to provide a high-frequency output voltage between a pair of high-frequency output terminals; the high-frequency output voltage having a fundamental frequency substantially higher than that of the AC power line voltage; the inverter sub-assembly being characterized by producing, across a pair of inverter terminals, a periodically alternating inverter voltage having a basic period consisting of: (i) a first segment during which its magnitude remains approximately constant at a positive potential; (ii) a second segment during which its magnitude decreases in a substantially continuous manner; (iii) a third segment during which its magnitude remains approximately constant at a negative potential; and (iv) a fourth segment during which its magnitude increases in a substantially continuous manner;

a gas discharge lamp connected in circuit with the high-frequency output terminals; the gas discharge lamp having a pair of thermionic cathodes, each having a pair of cathode terminals; and

a screw-base having a pair of base terminals; the screw-base, the rectifier sub-assembly, the inverter sub-assembly, and the gas discharge lamp being combined so as to constitute a lamp assembly operable to be screwed into and held by an ordinary electric lamp socket, thereby to cause said AC power line voltage to be applied to the base terminals.

10. The assembly of claim 9 wherein:

(a) the screw-base is characterized by having a standard screw-base width, which is about one inch; and

(b) the assembly is characterized by having: (i) a maximum height not exceeding eight times the standard screw-base width; and (ii) a maximum width not exceeding three times the standard screw-base width.

11. The assembly of claim 9 further characterized by having a capacitor effectively connected in parallel with the gas discharge lamp, thereby to form a lamp-capacitor parallel-combination.

12. The assembly of claim 11 still further characterized by having an inductor effectively connected in series with the lamp-capacitor parallel-combination; the inductor and the capacitor being operative to resonantly interact at the frequency of the high-frequency output voltage.

13. The assembly of claim 9 wherein the gas discharge lamp: (i) has a pair of thermionic cathodes; and (ii) is started without having been provided with preheating power to the thermionic cathodes.

14. The assembly of claim 9 wherein the gas discharge lamp: (i) has a thermionic cathode with a pair of cathode terminals; and (ii) is operated without being supplied with a cathode heating voltage across its cathode terminals.

15. The assembly of claim 9 wherein the inverter sub-assembly is further characterized by including a transistor having a pair of transistor terminals through which flows a periodic transistor current and across which exists a periodic transistor voltage; the transistor current flowing only during periods when the absolute magnitude of the transistor voltage is substantially lower than that of the DC voltage.

16. The assembly of claim 9 wherein the inverter sub-assembly is further characterized by including a transistor having a pair of transistor terminals through which periodically flows a transistor current and across which exists a periodic transistor voltage; the transistor current being prevented from flowing except during periods when the absolute magnitude of the transistor voltage is substantially lower than that of the DC voltage.

17. The assembly of claim 9 wherein: (i) the rectifier sub-assembly is further characterized by having two capacitors series-connected between the DC output terminals; and (ii) the inverter sub-assembly is further characterized by having two transistors series-connected between the DC input terminals.

18. The assembly of claim 9 wherein the periodically alternating inverter output voltage is characterized by having a trapezoidal waveform.

19. The assembly of claim 9 wherein the duration of the first segment is distinctly shorter than half the duration of the basic period.

20. The assembly of claim 9 additionally characterized by comprising a cylindrical housing means: (i) onto one side of which is mounted the gas discharge lamp; (ii) onto the other side of which is mounted the screw-base; and (iii) within which is mounted said inverter sub-assembly.

21. An assembly comprising:

a rectifier & filter sub-assembly mounted within a housing means and having a pair of AC input terminals operable, by way of a screw-base integrally mounted onto the housing means and adapted to be screwed into an Edison-type incandescent lamp socket, to be connected with the AC power line voltage of an ordinary electric utility power line and, when indeed so connected, to provide a DC voltage at a set of DC output terminals;

an inverter sub-assembly also mounted, at least in part, within the housing means; the inverter sub-assembly having a set of DC input terminals connected with the DC output terminals and being operative to provide a high-frequency output voltage between a pair of high-frequency output terminals; the high-frequency output voltage having a fundamental frequency substantially higher than that of the AC power line voltage; the inverter sub-assembly being further characterized by producing, across a pair of inverter terminals, a periodically alternating inverter voltage having a basic period consisting of: (i) a first segment during which its magnitude remains essentially constant at a positive potential; (ii) a second segment during which its magnitude decreases in a substantially continuous manner; (iii) a third segment during which its magnitude remains essentially constant at a negative potential; and (iv) a fourth segment during which its magnitude increases in a substantially continuous manner; and

a gas discharge lamp mounted onto the housing means; the gas discharge lamp being connected in circuit with the high-frequency output terminals; the gas discharge lamp being further characterized by having a pair of thermionic cathodes, each having a pair of cathode terminals.

22. An assembly comprising:

a rectifier & filter sub-assembly mounted at least partly within a cylindrical housing means and having a pair of AC input terminals operable, by way of a screw-base integrally mounted onto the cylindrical housing means and adapted to be screwed into an Edison-type incandescent lamp socket, to be connected with the AC power line voltage of an ordinary electric utility power line and, when indeed so connected, to provide a DC voltage at a set of DC output terminals;

an inverter sub-assembly also mounted at least partly within the cylindrical housing means; the inverter sub-assembly having a set of DC input terminals connected with the DC output terminals and operative to provide a high-frequency output voltage between a pair of high-frequency output terminals; the high-frequency output voltage having a fundamental frequency substantially higher than that of the AC power line voltage; the inverter sub-assembly being further characterized by producing, across a pair of inverter terminals, a periodically alternating inverter voltage having a basic period consisting of: (i) a first segment during which its magnitude remains roughly constant at a positive potential; (ii) a second segment during which its magnitude decreases in a substantially continuous and gradual manner; (iii) a third segment during which its magnitude remains roughly constant at a negative potential; and (iv) a fourth segment during which its magnitude increases in a substantially continuous and gradual manner; and

a gas discharge lamp mounted onto the cylindrical housing means; the gas discharge lamp being connected in circuit with the high-frequency output terminals; the gas discharge lamp being further characterized by having a pair of thermionic cathodes, each having a pair of cathode terminals.

23. An assembly comprising:

a first sub-assembly connected with the AC power line voltage of an ordinary electric utility power line and operative to provide a DC voltage at a pair of DC output terminals;

a second sub-assembly having a first DC input terminal and a second DC input terminal, both connected with the DC output terminals; the second sub-assembly including a first transistor connected between the first DC input terminal and a center terminal, and a second transistor connected between the center terminal and the second DC input terminal; the second sub-assembly being further characterized in that it provides a periodically alternating output voltage across a pair of AC output terminals, one of which AC output terminals being the center terminal; the periodically alternating output voltage having a waveshape with a complete cycle period consisting of: (i) a positive part during which its instantaneous magnitude remains at an essentially constant positive level; (ii) a negative part during which its instantaneous magnitude remains at an essentially constant negative level; (iii) a negative-going part during which its instantaneous magnitude changes rapidly from the positive level to the negative level; and (iv) a positive-going part during which its instantaneous magnitude changes rapidly from the negative level to the positive level; the duration of the positive part being, at least under some conditions, significantly different from the duration of the negative part; and

a third sub-assembly connected with the AC output terminals and including a light-emitting gas discharge lamp.

24. The assembly of claim 23 additionally characterized by: (i) including a housing structure; (ii) having a screw-base integrally mounted on the housing structure and protruding therefrom, the screw-base being of such nature as to permit it to be screwed into and held by an Edison-type incandescent lamp socket; (iii) having at least a part of the

first sub-assembly included within the housing structure; (iv) having the light-emitting gas discharge lamp mounted on the housing structure and protruding therefrom in a direction substantially opposite of the direction along which the screw-base protrudes; the gas discharge lamp being further characterized by having a pair of thermionic cathodes, each having a pair of cathode terminals.

**25**. The assembly of claim **23** additionally characterized by: (i) including a housing structure; (ii) having a screw-base integrally mounted on the housing structure and protruding therefrom, the screw-base being of such nature as to permit it to be screwed into and held by an Edison-type incandescent lamp socket; (iii) having at least a part of the second sub-assembly included within the housing structure; (iv) having the light-emitting gas discharge lamp mounted on the housing means and protruding therefrom in a direction substantially opposite of the direction along which the screw-base protrudes.

**26**. An assembly comprising:

a rectifier sub-assembly having a pair of AC input terminals operable to be connected with the AC power line voltage of an ordinary electric utility power line and, when indeed so connected, to provide a DC voltage at a set of DC output terminals;

an inverter sub-assembly having a set of DC input terminals connected with the DC output terminals and operative to provide a high-frequency output voltage between a pair of high-frequency output terminals; the high-frequency output voltage having a fundamental frequency substantially higher than that of the AC power line voltage; the inverter sub-assembly including a transistor having a pair of transistor terminals between which flows a periodic transistor current and across which exists a periodic transistor voltage; the transistor current flowing only when the absolute magnitude of the transistor voltage is substantially lower than that of the DC voltage; the inverter sub-assembly being also characterized by producing, across a pair of inverter terminals, a periodically alternating inverter voltage having a basic period consisting of: (i) a first segment during which its magnitude remains approximately constant at a positive potential; (ii) a second segment during which its magnitude decreases in a substantially continuous manner; (iii) a third segment during which its magnitude remains approximately constant at a negative potential; and (iv) a fourth segment during which its magnitude increases in a substantially continuous manner; and

a gas discharge lamp connected in circuit with the high-frequency output terminals.

**27**. The arrangement of claim **26** wherein the periodic transistor current flows only during periods when the absolute magnitude of the transistor voltage is lower than half that of the DC voltage.

**28**. An assembly comprising:

a rectifier sub-assembly having a pair of AC input terminals operable to be connected with the AC power line voltage of an ordinary electric utility power line and, when indeed so connected, to provide a DC voltage at a set of DC output terminals;

an inverter sub-assembly having a set of DC input terminals connected with the DC output terminals and operative to provide a high-frequency output voltage between a pair of high-frequency output terminals; the high-frequency output voltage having a fundamental frequency substantially higher than that of the AC power line voltage; the inverter sub-assembly including a transistor having a pair of transistor terminals between which flows a periodic transistor current and across which exists a periodic transistor voltage; the inverter sub-assembly including circuitry operative to prevent transistor current from flowing except when the absolute magnitude of the transistor voltage is substantially lower than that of the DC voltage; the inverter sub-assembly being also characterized by producing, across a pair of inverter terminals, a periodically alternating inverter voltage having a basic period consisting of: (i) a first segment during which its magnitude remains approximately constant at a positive potential; (ii) a second segment during which its magnitude decreases in a substantially continuous manner; (iii) a third segment during which its magnitude remains approximately constant at a negative potential; and (iv) a fourth segment during which its magnitude increases in a substantially continuous manner; and

a gas discharge lamp connected in circuit with the high-frequency output terminals.

**29**. The arrangement of claim **28** wherein the periodic transistor current is prevented from flowing except when the absolute magnitude of the transistor voltage is lower than half that of the DC voltage.

**30**. The assembly of claim **28** additionally characterized by: (i) comprising a screw-base; (ii) having the screw-base, the rectifier sub-assembly, and the inverter sub-assembly combined so as to constitute a lamp assembly operable to be screwed into and held by an ordinary electric lamp socket; and (iii) having a periodically conducting transistor with a pair of control terminals across which exists an alternating control voltage having a peak-to-peak magnitude substantially higher than twice the forward voltage drop of an ordinary semiconductor junction.

**31**. The assembly of claim **28** additionally characterized by: (i) comprising a screw-base; (ii) having the screw-base, the rectifier sub-assembly, and the inverter sub-assembly combined so as to constitute a lamp assembly operable to be screwed into and held by an ordinary electric lamp socket; (iii) having a periodically conducting transistor with a transistor terminal; and (iv) exhibiting an electrically conductive path between the transistor terminal and one of the AC input terminals.

**32**. The assembly of claim **29** additionally characterized by: (i) comprising a screw-base having a base terminal connected with one of the AC input terminals and operative to connected with a terminal in an ordinary Edison-type lamp socket; (ii) having the screw-base, the rectifier sub-assembly, and the inverter sub-assembly combined so as to constitute a lamp assembly operable to be screwed into and held by an ordinary electric lamp socket; (iii) having a periodically conducting transistor with a transistor terminal; and (iv) exhibiting an electrically conductive path between the transistor terminal and at least one the AC input terminals.

* * * * *

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US005510681A

# United States Patent [19]

Nilssen

[11] Patent Number: 5,510,681

[45] Date of Patent: Apr. 23, 1996

[54] **OPERATING CIRCUIT FOR GAS DISCHARGE LAMPS**

[76] Inventor: Ole K. Nilssen, 408 Caesar Dr., Barrington, Ill. 60010

[21] Appl. No.: 227,999

[22] Filed: Apr. 15, 1994

**Related U.S. Application Data**

[63] Continuation of Ser. No. 770,414, Oct. 3, 1991, which is a continuation-in-part of Ser. No. 663,566, Mar. 4, 1991, Pat. No. 5,185,560, and Ser. No. 768,105, Sep. 30, 1991, abandoned, said Ser. No. 768,105, Sep. 30, 1991, abandoned, is a continuation of Ser. No. 787,692, Oct. 15, 1985, abandoned, which is a continuation of Ser. No. 644,155, Aug. 27, 1984, which is a continuation of Ser. No. 555,426, Nov. 23, 1983, which is a continuation of Ser. No. 178,107, Aug. 14, 1980, abandoned, which is a continuation-in-part of Ser. No. 973,741, Dec. 28, 1978, abandoned, which is a continuation-in-part of Ser. No. 890,586, Mar. 20, 1978, Pat. No. 4,184,128.

[51] Int. Cl.[6] ..... H05B 37/02

[52] U.S. Cl. ..... 315/219; 315/223; 315/289; 315/DIG. 5; 315/DIG. 7

[58] Field of Search ..... 315/171, 173, 315/175, 176, DIG. 5, DIG. 7, 207, 208, 200 R, 289, 223, 308, 219

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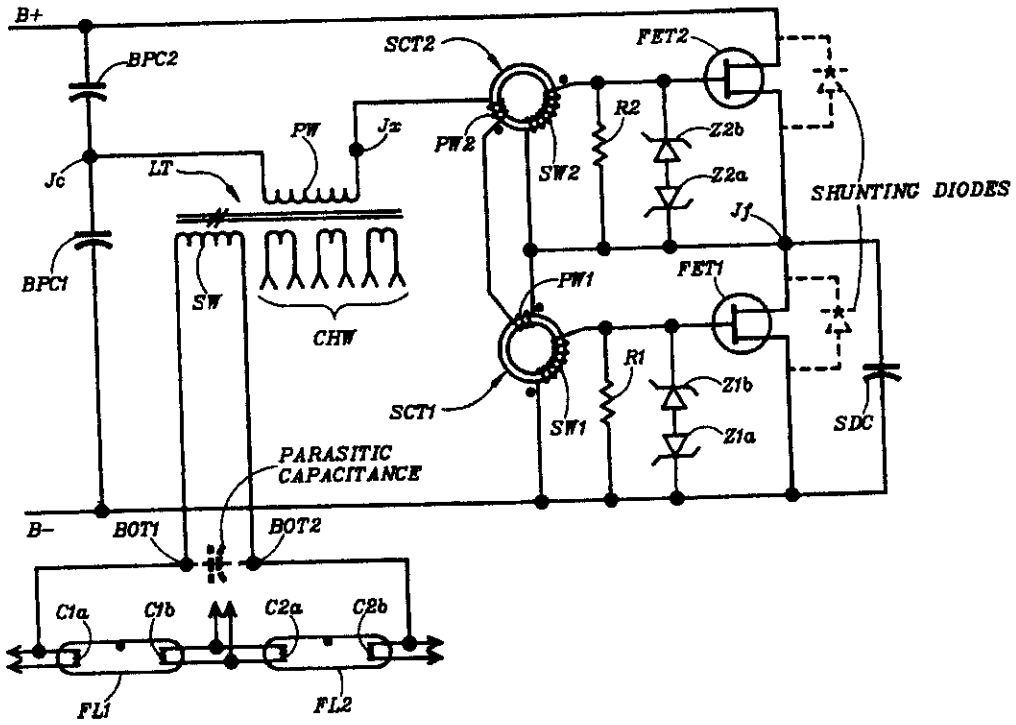
*Primary Examiner*—Frank Gonzalez
*Assistant Examiner*—Reginald A. Ratliff

[57] **ABSTRACT**

A half-bridge inverter is powered from a constant-magnitude DC supply voltage and provides at the inverter's output a first AC output voltage that is describable as a modified squarewave voltage. This first AC voltage is applied across a series-combination of an inductor and a capacitor, the junction between which is clamped to the DC supply voltage. As a result, a second AC voltage gets established across the capacitor; which second AC voltage is also describable as being a modified squarewave voltage. However, the phasing of the second AC voltage is delayed by approximately 90 degrees with respect to the first AC voltage; which results in the voltage across the inductor being of approximately sinusoidal waveform. A fluorescent lamp is connected in series with a ballast capacitor; and the lamp-capacitor series combination is connected across the inductor, thereby resulting in a nearly sinusoidal current being provided to the fluorescent lamp. Lamp starting aid is provided by a voltage-doubling circuit supplying a high-magnitude current-limited DC voltage across the ballast capacitor for ignition purposes.

**17 Claims, 8 Drawing Sheets**



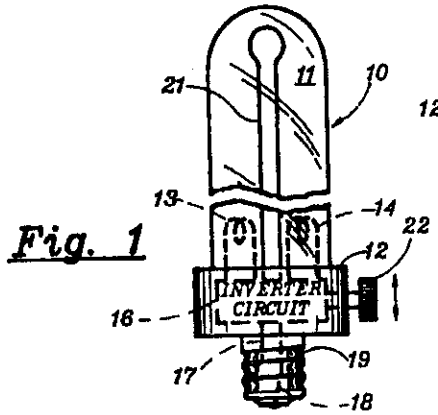



Fig. 1

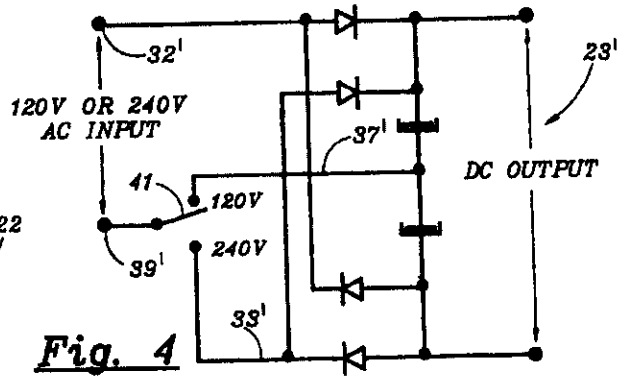



Fig. 4

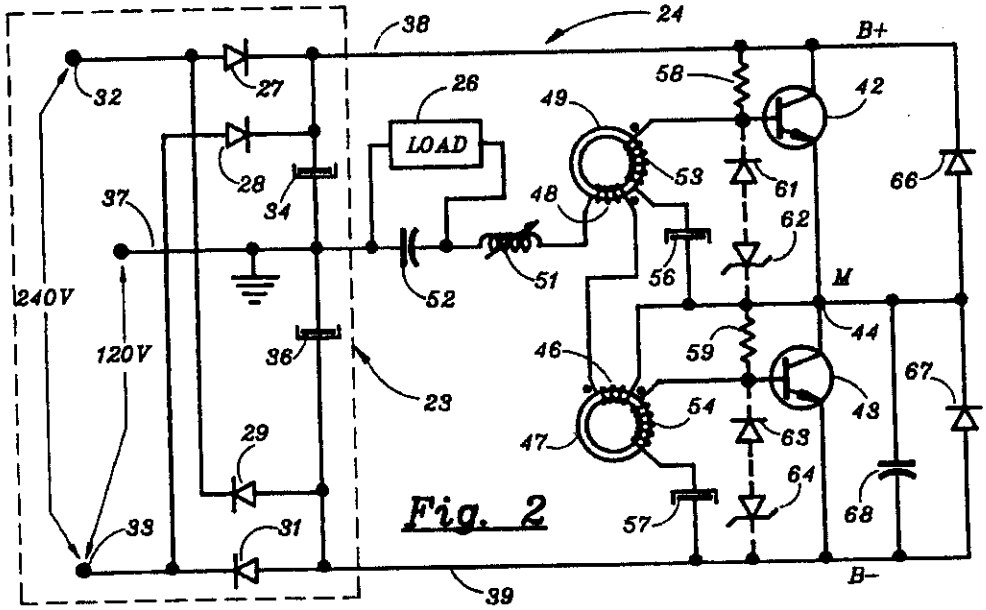



Fig. 2

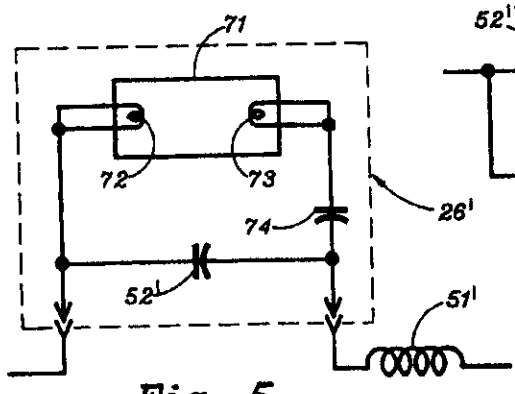



Fig. 5

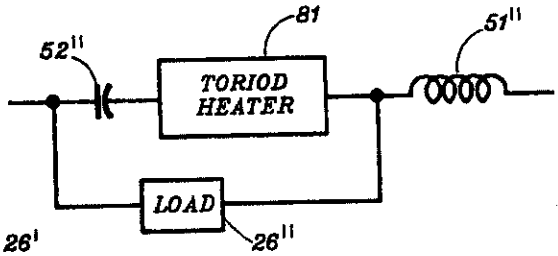



Fig. 6

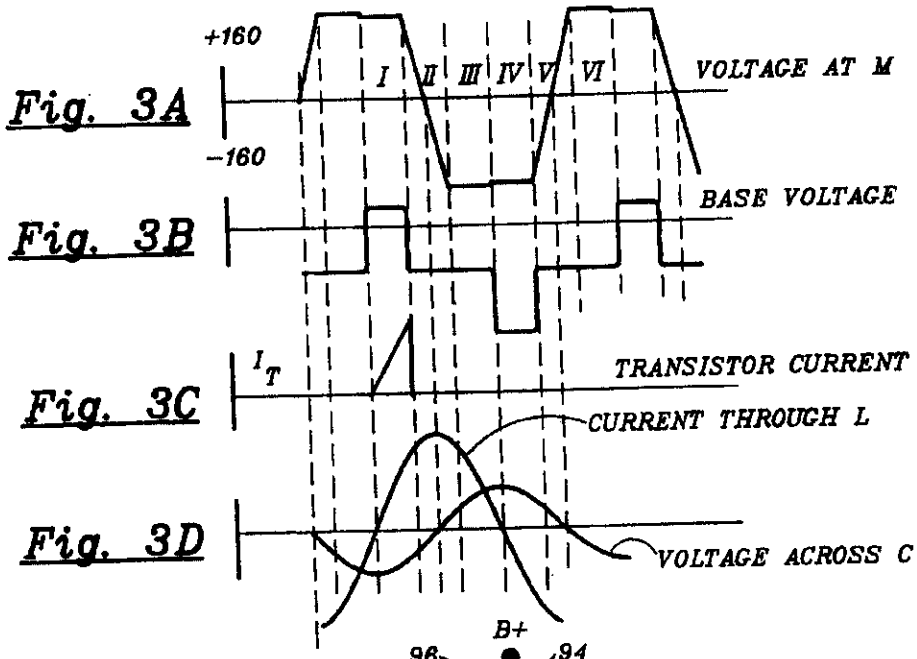



Fig. 3A

Fig. 3B

Fig. 3C

Fig. 3D

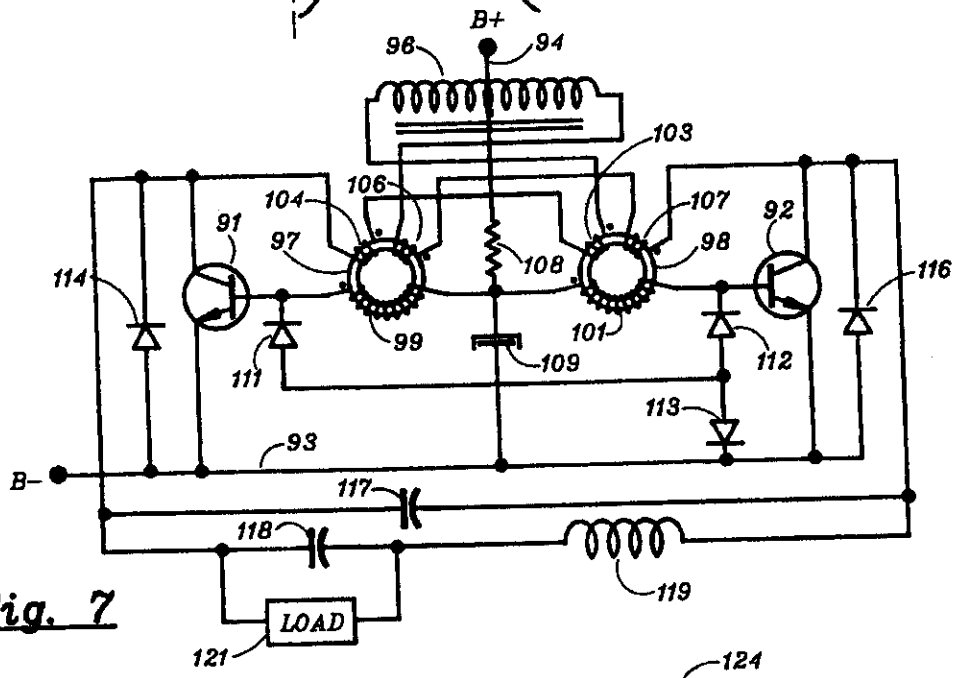



Fig. 7

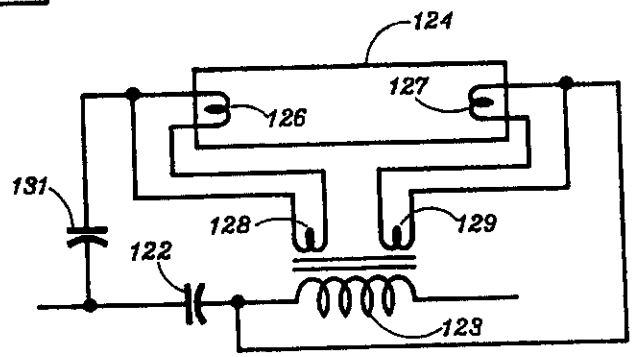



Fig. 8

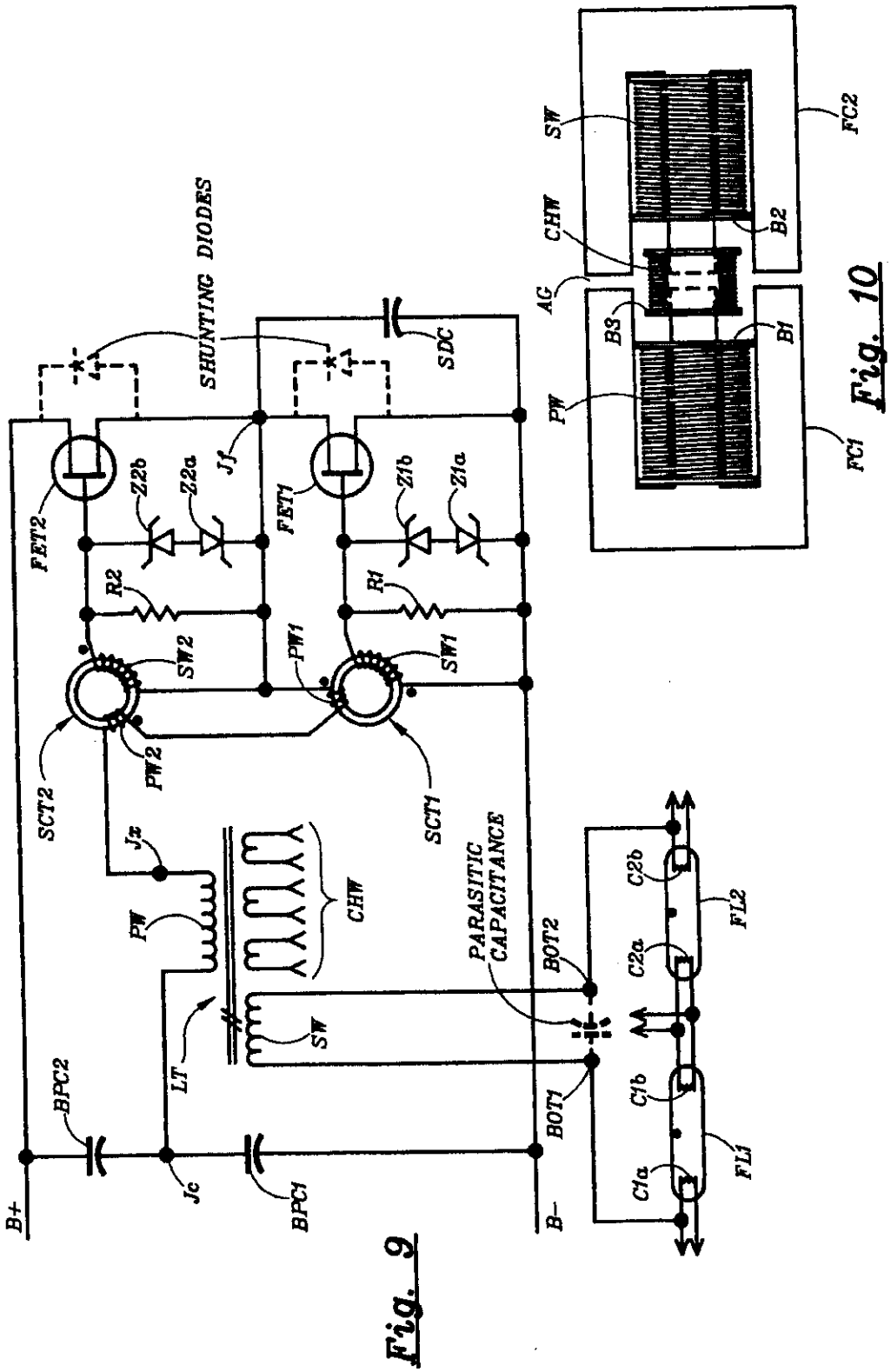

SHUNTING DIODES
SDC
FET2
FET1
Z2b
Z2a
Z1b
Z1a
Jf
R2
R1
SW2
SW1
PW1
PW2
SCT2
SCT1
Jx
PW
CHW
SW
LT
Jc
BPC2
BPC1
B+
B-
PARASITIC CAPACITANCE
BOT2
BOT1
C2b
C2a
C1b
C1a
FL2
FL1

Fig. 9


SW
CHW
AG
PW
B3
B2
B1
FC2
FC1

Fig. 10

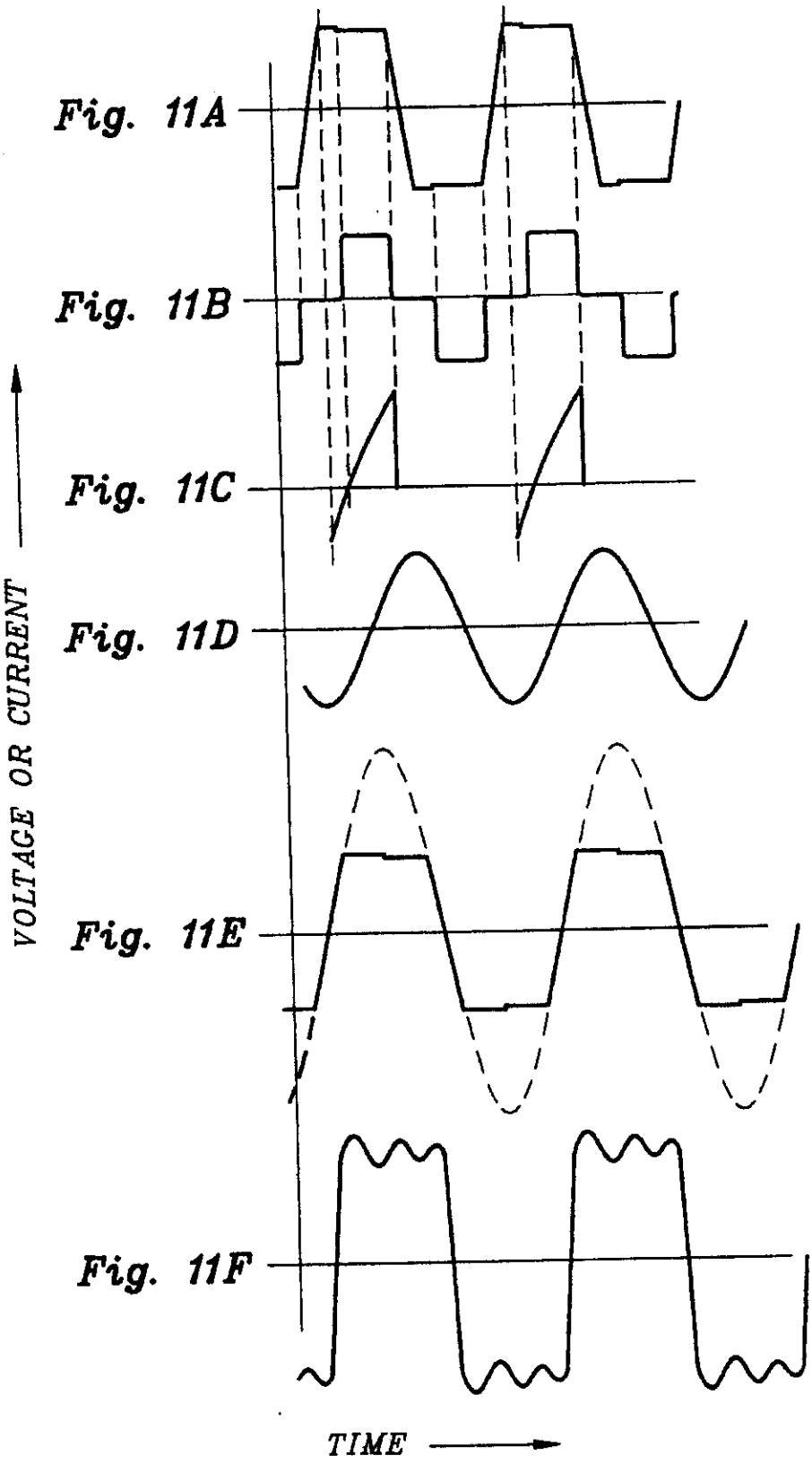


Fig. 11A
Fig. 11B
Fig. 11C
Fig. 11D
Fig. 11E
Fig. 11F
VOLTAGE OR CURRENT
TIME

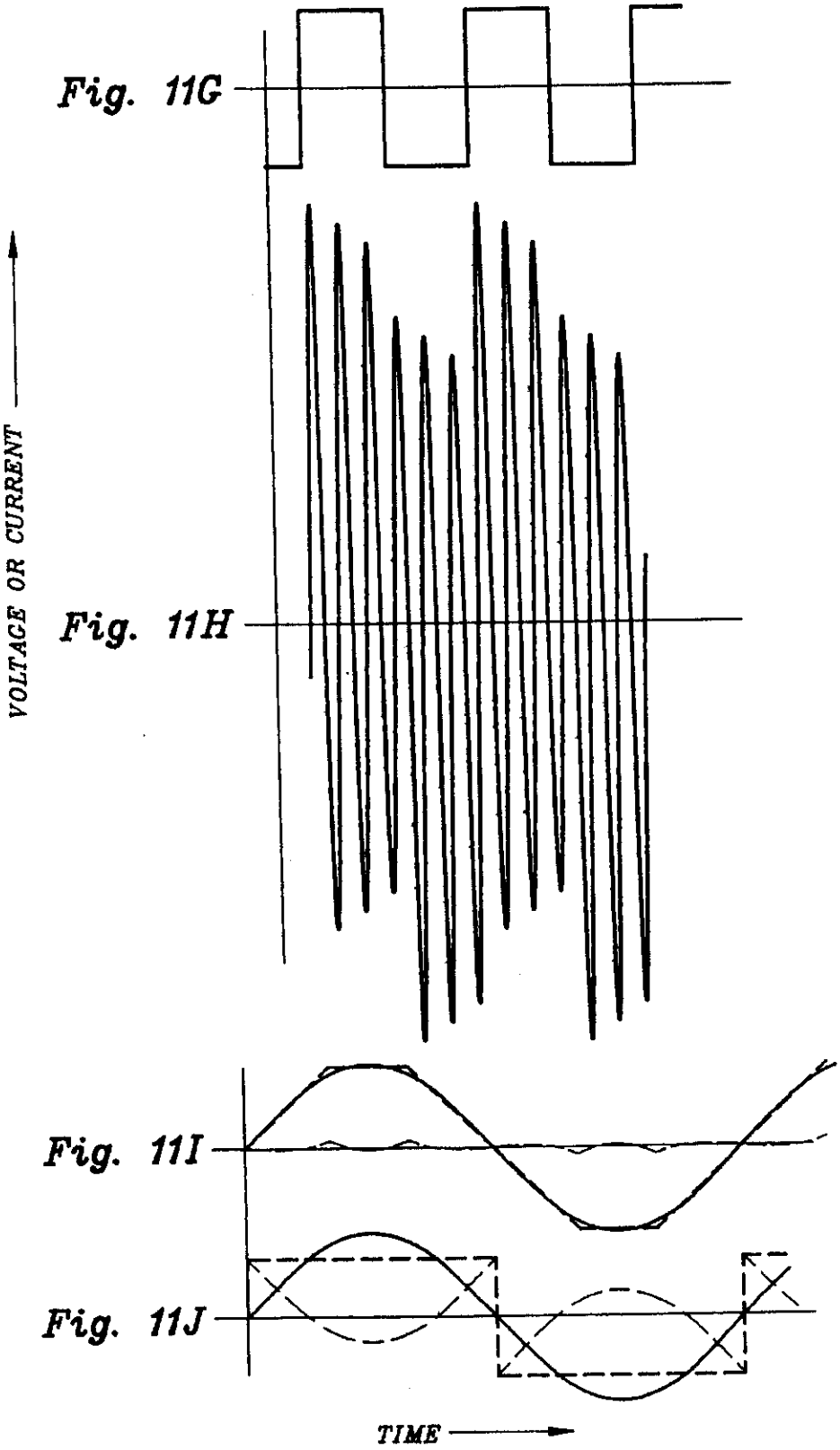


Fig. 11G
Fig. 11H
VOLTAGE OR CURRENT
Fig. 11I
Fig. 11J
TIME

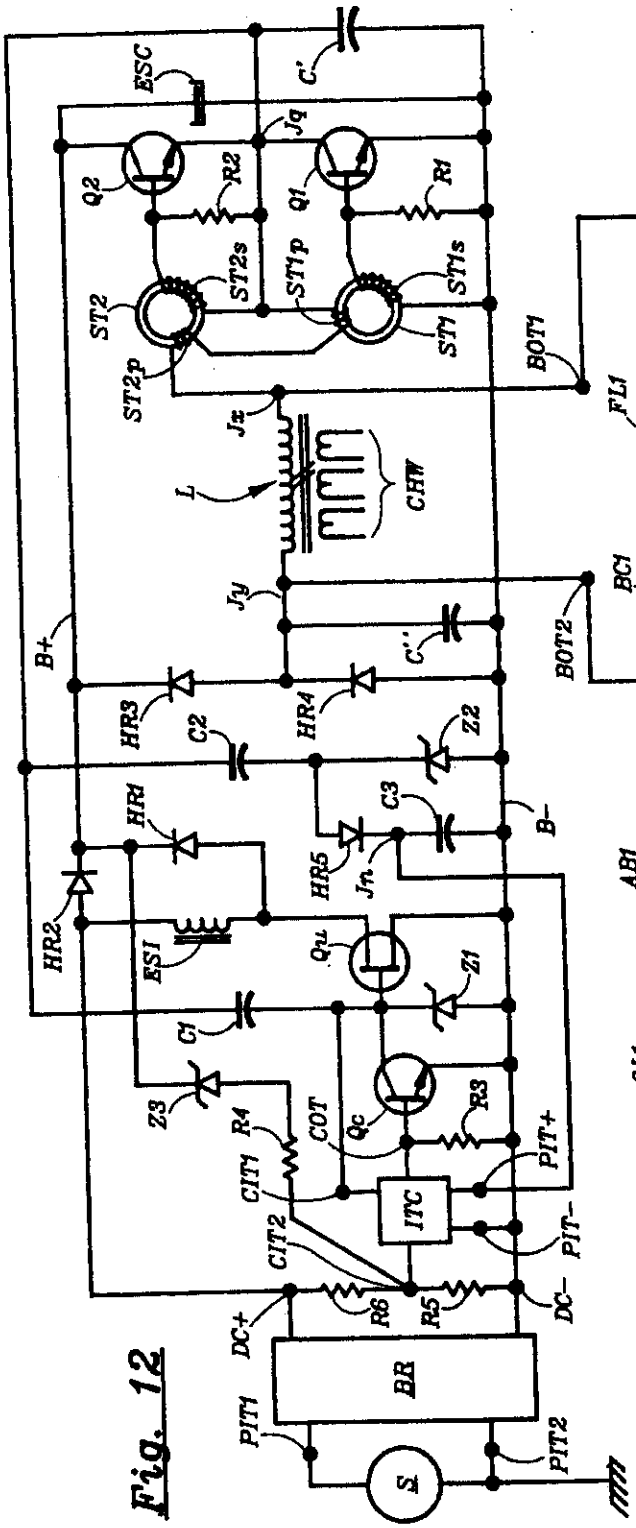

ESC
C'
Jq
Q2
R2
Q1
R1
ST2s
ST1p
ST1s
ST2
ST1
ST2p
BOT1
FL1
FL2
Jx
L
CHW
Jy
BC1
BC2
B+
C''
BOT2
HR3
HR4
C2
Z2
HR1
C3
B-
HR5
Jn
HR2
ES1
Qu
Z1
C1
Z3
R4
COT
Qc
R3
PIT+
CIT1
ITC
CIT2
PIT-
R6
R5
DC-
DC+
BR
PIT1
PIT2
S

Fig. 12

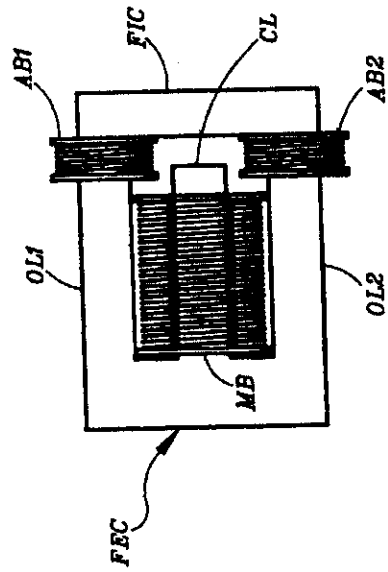

FIC
CL
AB1
AB2
OL1
OL2
MB
FEC

Fig. 13

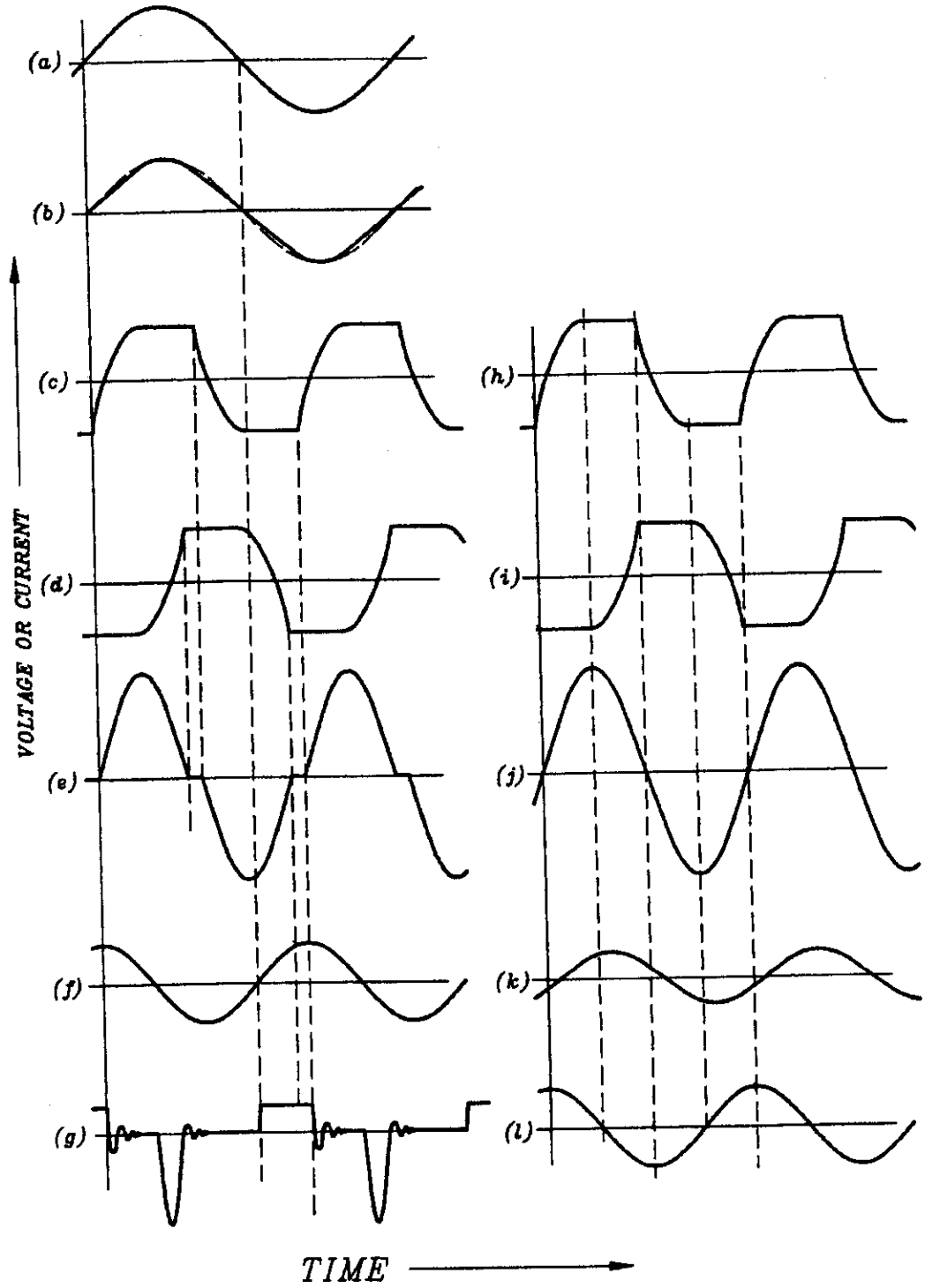



Fig. 14

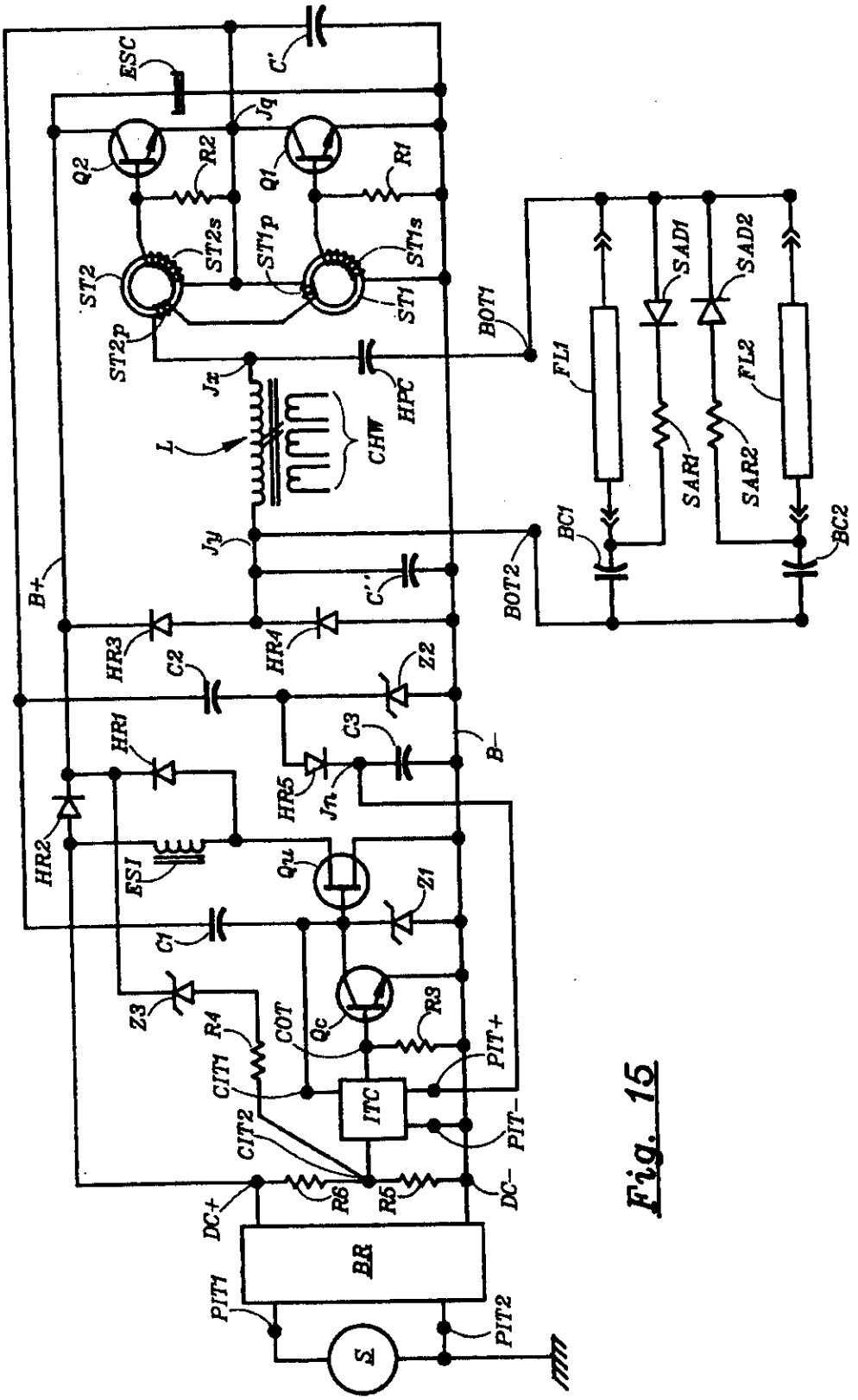

ESC
C'
Jq
Q2
R2
Q1
R1
ST2s
ST1p
ST1s
ST2
ST1
ST2p
BOT1
Jx
HPC
L
CHW
FL1
SAD1
SAD2
FL2
SAR1
SAR2
BC1
BC2
Jy
C''
BOT2
B+
HR3
HR4
C2
Z2
HR1
C3
B-
HR5
Jn
HR2
ESJ
Qu
Z1
C1
Z3
R4
COT
Qc
R3
PIT+
CIT1
ITC
CIT2
PIT-
R6
R5
DC-
DC+
BR
PIT1
PIT2
S

Fig. 15

# OPERATING CIRCUIT FOR GAS DISCHARGE LAMPS

This application is a continuation of Ser. No. 07/770,414 filed Oct. 3, 1991, which is a Continuation-in-Part of Ser. No. 07/663,566 filed Mar. 4, 1991, now U.S. Pat. No. 5,185,560, as well as of Ser. No. 07/768,105 filed Sep. 30, 1991, now abandoned; which Ser. No. 07/768,105 is a Continuation of Ser. No. 06/787,692 filed Oct. 15, 1985, now abandoned; which is a Continuation of Ser. No. 06/644,155 filed Aug. 27, 1984; which is a Continuation of Ser. No. 06/555,426 filed Nov. 23, 1983; which is a Continuation of Ser. No. 06/178,107 filed Aug. 14, 1980, now abandoned; which is a Continuation-in-Part of Ser. No. 05/973,741 filed Dec. 28, 1978, now abandoned; which is a Continuation-in-Part of Ser. No. 05/890,586 filed Mar. 20, 1978, now U.S. Pat. No. 4,184,128.

## BACKGROUND OF THE INVENTION

1. Field of Invention

This invention relates to ballasting means for gas discharge lamps.

2. Description of Prior Art

For a description of pertinent prior art, reference is made to U.S. Pat. No. 4,677,345 to Nilssen; which patent issued from a Division of application Ser. No. 06/178,107 filed Aug. 14, 1980; part of the disclosure of which application is the basis for instant application.

Otherwise, reference is made to the following U.S. Pat. Nos. 3,263,122 to Genuit; 3,320,510 to Locklair; 3,996,493 to Davenport et el.; 4,100,476 to Ghiringhelli; 4,262,327 to Kovacik et al.; 4,370,600 to Zansky; 4,634,932 to Nilssen; and 4,857,806 to Nilssen.

## SUMMARY OF THE INVENTION

### Objects of the Invention

A main object of the present invention is that of providing a cost-effective ballasting means for gas discharge lamps.

This as well as other objects, features and advantages of the present invention will become apparent from the following description and claims.

### Brief Description of the Invention

A half-bridge inverter is powered from a DC rail by a constant-magnitude DC supply voltage and provides at the inverter's output terminals a first AC output voltage that is describable as a modified squarewave voltage. This first AC voltage, whose waveshape is shaped away from that of an ordinary squarewave voltage by using a slow-down capacitor of substantial capacitance connected directly across the inverter's output terminals, is applied across a series-combination of an inductor and a capacitor; which inductor and capacitor are connected together at a junction; which, in turn, is connected with the DC rail by way of a pair of clamping rectifiers; which means that the voltage developing across the capacitor will be clamped by the DC supply voltage. As a result, a second AC voltage gets established across the capacitor; which second AC voltage is also describable as being a modified squarewave voltage. However, the phasing of the second AC voltage is delayed by approximately 90 degrees with respect to the first AC voltage; which results in the voltage across the inductor being of approximately sinusoidal waveform. A fluorescent lamp is connected in series with a ballast capacitor; and the lamp-capacitor series combination is connected across the inductor, thereby resulting in a nearly sinusoidal current being provided to the fluorescent lamp. Lamp starting aid is provided by way of a current-limited auxiliary DC voltage applied across the lamp.



The DC supply voltage is attained and regulated by way of an up-converter principally consisting of an energy-storing inductor connected between a field-effect transistor (i.e., a FET) and the DC output terminals of a bridge rectifier powered from ordinary 120 Volt/60 Hz power line voltage. The FET is caused to enter its ON state (thereby causing the energy-storing inductor to be charged-up) by having its gate-source input capacitance being provided with a certain amount of charge (i.e., sufficient to cause the FET to switch into its ON-state) each time one of the transistors in the self-oscillating half-bridge inverter is switched OFF. After a delay of about 10 micro-seconds after having been switched ON, an automatic timing circuit causes a short circuit to be placed across the gate-source input capacitance for a time just long enough to drain away the gate-source charge, thereby causing the FET to switch OFF; thereby, in turn, causing the energy stored in the energy-storing inductor to be discharged into an energy-storing capacitor connected across the DC rail. To minimize the harmonics associated with the wavefrom of the current drawn from the power line, the delay is decreased with increasing instantaneous magnitude of the power line voltage. Also, to provide for effective regulation of the magnitude of the DC supply voltage, the delay is decreased as the magnitude of the DC supply voltage exceeds a predetermined level.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a front elevation of a folded fluorescent lamp unit adapted for screw-in insertion into a standard Edison incandescent socket;

FIG. 2 is a schematic diagram illustrating the essential features of a push-pull inverter circuit particularly suitable for energizing the lamp unit of FIG. 1;

FIGS. 3A–3D is a set of waveform diagrams of certain significant voltages and currents occurring in the circuit of FIG. 2;

FIG. 4 is a schematic diagram of a DC power supply connectable to both 120 and 240 volt AC inputs;

FIG. 5 is a schematic diagram which illustrates the connection of a non-self-ballasted gas discharge lamp unit to the FIG. 2 inverter circuit;

FIG. 6 is a schematic diagram which illustrates the use of a toroid heater for regulation of the inverter output;

FIG. 7 is an alternate form of push-pull inverter circuit according to one aspect of the present invention;

FIG. 8 is a schematic diagram showing the connection of a gas discharge lamp of the "rapid-start" type to an inductor-capacitor-loaded inverter according to the present invention;

FIG. 9 is a schematic diagram illustrating an inverter ballast circuit arrangement wherein a pair of series-connected fluorescent lamps is powered, by way of a reactance transformer, from an inverter output voltage having a trapezoidal (i.e. truncated sinewave) waveform like that of FIG. 3A.

FIG. 10 is a schematic illustration of the reactance transformer used in the circuit arrangement of FIG. 9.

FIGS. 11A–11J show various voltage and current waveforms associated with the circuit arrangement of FIG. 9.

FIG. 12 is a schematic diagram illustrating the main preferred embodiment of the present invention.

FIG. 13 is a schematic illustration of a combination tank inductor and cathode heater transformer used in the preferred embodiment of FIG. 12.

FIGS. 14A–14I shows various voltage and current waveforms associated with the circuit arrangement of FIG. 12.

FIG. 15 is a schematic diagram of a modified main preferred embodiment; whci is identical to that of FIG. 12 except for an added lamp starting aid arrangement.

## DESCRIPTION OF VARIOUS PREFERRED EMBODIMENTS

FIG. 1 illustrates a screw-in gas discharge lamp unit 10 comprising a folded fluorescent lamp 11 suitably secured to an integral base 12. The lamp comprises two cathodes 13, 14 which are supplied with the requisite high operating voltage from a frequency-converting power supply and ballasting circuit 16; which, because of its compact size, conveniently fits within the base 12.

The inverter circuit 16 is connected by leads 17, 18 to a screw-type plug 19 adapted for screw-in insertion into a standard Edison-type incandescent lamp socket at which ordinary 120 Volt/60 Hz power line voltage is available. A ground plane comprising a wire or metallic strip 21 is disposed adjacent a portion of the fluorescent lamp 11 as a starting aid. Finally, a manually rotatable external knob 22 is connected to a shaft for mechanical adjustment of the air gap of a ferrite core inductor to vary the inductance value thereof in order to effect adjustment of the inverter voltage output connected to electrodes 13, 14 for controlled variation of the lamp illumination intensity.

With reference to FIG. 2, a power supply 23, connected to a conventional AC input, provides a DC output for supplying a high-efficiency inverter circuit 24. The inverter is operable to provide a high voltage to an external load 26, which may comprise a gas discharge device such as the fluorescent lamp 11 of FIG. 1.

The power supply 23 comprises bridge rectifier having four diodes 27, 28, 29 and 31 connectable to a 240 volt AC supply at terminals 32, 33. Capacitors 34, 36 are connected between a ground line 37 (in turn directly connected to the inverter 24) and to a B+ line 38 and a B– line 39, respectively. The power supply 23 also comprises a voltage doubler and rectifier optionally connectable to a 120 volt AC input taken between the ground line 37 and terminal 33 or 32. The voltage doubler and rectifier means provides a direct electrical connection by way of line 37 between one of the 120 volt AC power input lines and the inverter 24, as shown in FIG. 2. The bridge rectifier and the voltage doubler and rectifier provide substantially the same DC output voltage to the inverter 24 whether the AC input is 120 or 240 volts. Typical voltages are +160 volts on the B+ line 38 and –160 volts on the B– line 39.

With additional reference to FIG. 4, which shows an alternate power supply 23', the AC input, whether 120 or 240 volts, is provided at terminals 32' and 39. Terminal 39 is in turn connected through a single-pole double-throw selector switch 41 to terminal 37' (for 120 volt operation) or terminal 33' (for 240 volt operation). In all other respects, power supplies 23 and 23' are identical.

The inverter circuit 24 of FIG. 2 is a half-bridge inverter comprising transistors 42, 43 connected in series across the DC voltage output of the power supply 23 on B+ and B– lines 38 and 39, respectively. The collector of transistor 42 is connected to the B+ line 38, the emitter of transistor 42 and the collector of transistor 43 are connected to a midpoint line 44 (designated "M") and the emitter of transistor 43 is connected to the B– line 39. The midpoint line 44 is in turn connected to the ground line 37 through primary winding 46 of a toroidal saturable core transformer 47, a primary winding 48 on an identical transformer 49, an inductor 51 and a series-connected capacitor 52. The inductor 51 and capacitor 52 are energized upon alternate transistor conduction in a manner to be described later.

An external load 26 is preferably taken off capacitor 52, as shown in FIG. 2. The inductor 51, preferably a known ferrite core inductor, has an inductance variable by mechanical adjustment of the air gap in order to effect variation in the level of the inductor and capacitor voltage and hence the power available to the load, as will be described. When the load is a gas discharge lamp such as lamp 11 in FIG. 1, variation in this inductance upon rotation of knob 22 accomplishes a lamp dimming effect.

Drive current to the base terminals of transistors 42 and 43 is provided by secondary windings 53, 54 of transformers 49, 47, respectively. Winding 53 is also connected to midpoint lead 44 through a bias capacitor 56, while winding 54 is connected to the B– lead 39 through an identical bias capacitor 57. The base terminals of transistors 42 and 43 are also connected to lines 38 and 44 through bias resistors 58 and 59, respectively. For a purpose to be described later, the base of transistor 42 can be optionally connected to a diode 61 and a series Zener diode 64 in turn connected to the midpoint line 44; similarly, a diode 63 and series Zener diode 64 in turn connected to the B– line 39 can be connected to the base of transistor 43. Shunt diodes 66 and 67 are connected across the collector-emitter terminals of transistors 42 and 43, respectively. Finally, a capacitor 68 is connected across the collector-emitter terminals of transistor 43 to restrain the rate of voltage rise across those terminals, as will be seen presently.

The operation of the circuit of FIG. 2 can best be understood with additional reference to FIG. 3, which illustrates significant portions of the waveforms of the voltage at midpoint M (FIG. 3A), the base-emitter voltage on transistor 42 (FIG. 3B), the current through transistor 42 (FIG. 3C), and the capacitor 52 voltage and the inductor 51 current (FIG. 3D).

Assuming that transistor 42 is first to be triggered into conduction, current flows from the B+ line 38 through windings 46 and 38 and the inductor 51 to charge capacitor 52 and returns through capacitor 34 (refer to the time period designated I in FIG. 3). When the saturable inductor 49 saturates at the end of period I, drive current to the base of transistor 42 will terminate, causing voltage on the base of the transistor to drop to the negative voltage stored on the bias capacitor 56 in a manner to be described, causing this transistor to become non-conductive. As shown in FIG. 3c, current-flow in transistor 43 terminates at the end of period I.

Because the current through inductor 51 cannot change instantaneously, current will flow from the B– bus 39 through capacitor 68, causing the voltage at midpoint line 44 to drop to –160 volts (period II in FIG. 3). The capacitor 68 restrains the rate of voltage change across the collector and emitter terminals of transistor 42. The current through the inductor 51 reaches its maximum value when the voltage at the midpoint line 44 is zero. During period III, the current will continue to flow through inductor 51 but will be

supplied from the B– bus through the shunt diode **67**. It will be appreciated that during the latter half of period II and all of period III, positive current is being drawn from a negative voltage; which, in reality, means that energy is being returned to the power supply through a path of relatively low impedance.

When the inductor current reaches zero at the start of period IV, the current through the primary winding **46** of the saturable inductor **47** will cause a current to flow out of its secondary winding **54** to cause transistor **43** to become conductive, thereby causing a reversal in the direction of current through inductor **51** and capacitor **52**. When transformer **47** saturates at the end of period IV, the drive current to the base of transistor **43** terminates and the current through inductor **51** will be supplied through capacitor **68**, causing the voltage at midpoint line **44** to rise (period V). 'When the voltage at the midpoint line M reaches 160 volts, the current will then flow through shunt diode **66** (period VI). The cycle is then repeated.

As seen in FIG. **3**, saturable transformers **47**, **49** provide transistor drive current only after the current through inductor **51** has diminished to zero. Further, the transistor drive current is terminated before the current through inductor **51** has reached its maximum amplitude. This coordination of base drive current and inductor current is achieved because of the series-connection between the inductor **51** and the primary windings **46**, **48** of saturable transformers **47**, **49**, respectively.

The series-connected combination of the inductor **51** and the capacitor **52** is energized upon the alternate conduction of transistors **42** and **43**. With a large value of capacitance of capacitor **52**, very little voltage will be developed across its terminals. As the value of this capacitance is decreased, however, the voltage across this capacitor will increase. As the value of the capacitor **52** is reduced to achieve resonance with the inductor **51**, the voltage on the capacitor will rise and become infinite in a loss-free circuit operating under ideal conditions.

It has been found desirable to regulate the transistor inversion frequency, determined mainly by the saturation time of the saturable inductors **47**, **49**, to be equel to or higher than the natural resonance frequency of the inductor and capacitor combination in order to provide a high voltage output to external load **26**. A high voltage across capacitor **52** is efficiently developed as the transistor inversion frequency approaches the natural resonant frequency of the inductor **51** and capacitor **52** combination. Stated another way, the conduction period of each transistor is desirably shorter in duration than one quarter of the full period corresponding to the natural resonant frequency of the inductor and capacitor combination. When the inverter **24** is used with a self-ballasted gas discharge lamp unit, it has been found that the inversion frequency can be at least equal to the natural resonant frequency of the tank circuit. If the capacitance value of capacitor **52** is reduced still further beyond the resonance point, unacceptably high transistor currents will be experienced during transistor switching and transistor burn-out will occur.

It will be appreciated that the sizing of capacitor **52** is determined by the application of the inverter circuit **24**. Variation in the values of the capacitor **52** and the inductor **51** will determine the voltages developed in the inductor-capacitor tank circuit. The external load **26** may be connected in circuit with the inductor **51** (by a winding on the inductor, for example) and the capacitor may be omitted entirely. If the combined circuit loading of the inductor **51** and the external load **26** has an effective inductance of value sufficient to effect periodic energy storage for self-sustained transistor inversion, the current feedback provided by the saturable inductors **47**,**49** will effect alternate transistor conduction without the need for additional voltage feedback. When the capacitor **52** is omitted, the power supply **23** provides a direct electrical connection between one of the AC power input lines and the inverter load circuit.

Because the voltages across transistors **42**, **43** are relatively low (due to the effect of capacitors **34**, **36**), the half-bridge inverter **24** is very reliable. The absence of switching transients minimizes the possibility of transistor burn-out.

The inverter circuit **24** comprises means for supplying reverse bias to the conducting transistor upon saturation of its associated saturable inductor. For this purpose, the capacitors **56** and **57** are charged to negative voltages as a result of reset current flowing into secondary windings **53**, **54** from the bases of transistors **42**, **43**, respectively. This reverse current rapidly turns off a conducting transistor to increase its switching speed and to achieve inverter circuit efficiency in a manner described more fully in my co-pending U.S. patent application Ser. No. 103,624 filed Dec. 14, 1979 and entitled "Bias Control for High Efficiency Inverter Circuit" (now U.S. Pat. No. 4,307,353). The more negative the voltage on the bias capacitors **56** and **57**, the more rapidly charges are swept out of the bases of their associated transistors upon transistor turn-off.

When a transistor base-emitter junction is reversely biased, it exhibits the characteristics of a Zener diode having a reverse breakdown voltage on the order of 8 to 14 Volt for transistors typically used in high-voltage inverters. As an alternative, to provide a negative voltage smaller in magnitude on the base lead of typical transistor **42** during reset operation, the optional diode **61** and Zener diode **62** combination can be used. For large values of the bias capacitor **56**, the base voltage will be substantially constant.

If the load **26** comprises a gas discharge lamp, the voltage across the capacitor **52** will be reduced once the lamp is ignited to prevent voltages on the inductor **51** and the capacitor **52** from reaching destructive levels. Such a lamp provides an initial time delay during which a high voltage, suitable for instant starting, is available.

FIG. **5** illustrates the use of an alternate load **26'** adapted for plug-in connection to an inverter circuit such as shown in FIG. **2**. The load **26'** consists of a gas discharge lamp **71** having electrodes **72**, **73** and connected in series with a capacitor **74**. The combination of lamp **71** and capacitor **74** is connected in parallel with a capacitor **52'** which serves the same purpose as capacitor **52** in the FIG. **2** circuit. However, when the load **26'** is unplugged from the circuit, the inverter stops oscillating and the development of high voltages in the inverter is prevented. The fact that no high voltages are generated by the circuit if the lamp is disconnected while the circuit is oscillating is important for safety reasons.

FIG. **6** illustrates a capacitor **52"** connected in series with an inductor **51"** through a heater **81** suitable for heating the toroidal inductors **47**, **49** in accordance with the level of output. The load **26"** is connected across the series combination of the capacitor **52"** and the toroid heater. The heater **81** is preferably designed to controllably heat the toroidal saturable inductors in order to decrease their saturation flux limit and hence their saturation time. The result is to decrease the periodic transistor conduction time and thereby increase the transistor inversion frequency. When a frequency-dependent impedance means, that is, an inductor or

a capacitor, is connected in circuit with the AC voltage output of the inverter, change in the transistor inversion frequency will modify the impedance of the frequency-dependent impdance means and correspondingly modify the inverter output. Thus as the level of the output increases, the toroid heater **81** is correspondingly energized to effect feedback regulation of the output. Further, transistors **42, 43** of the type used in high voltage inverters dissipate heat during periodic transistor conduction. As an alternative, the toroid heater **81** can use this heat for feedback regulation of the output or control of the temperature of transistors **42, 43.**

The frequency dependent impedance means may also be used in a circuit to energize a gas discharge lamp at adjustable illumination levels. Adjustment in the inversion frequency of transistors **42, 43** results in control of the magnitude of the AC current supplied to the lamp. This is preferably accomplished where saturable inductors **47, 49** have adjustable flux densities for control of their saturation time.

FIG. **7** schematically illustrates an alternate form of inverter circuit, shown without the AC to DC power supply connections for simplification. In this Figure, the transistors are connected in parallel rather than in series but the operation is essentially the same as previously described.

In particular, this circuit comprises a pair of alternately conducting transistors **91, 92.** The emitter terminals of the transistors are connected to a B– line **93.** A B+ lead **94** is connected to the center-tap of a transformer **96.** In order to provide drive current to the transistors **91, 92** for control of their conduction frequency, saturable inductors **97, 98** have secondary windings **99, 101,** respectively, each secondary winding having one end connected to the base of its associated transistor; the other ends are connected to a common terminal **102.** One end of transformer **96** is connected to the collector of transistor **91** through a winding **103** on inductor **98** in turn connected in series with a winding **104** on inductor **97.** Likewise, the other end of transformer **96** is connected to the collector of transistor **92** through a winding **106** on inductor **97** in series with another winding **107** on inductor **98.**

The B+ terminal is connected to terminal **102** through a bias resistor **108.** A bias capacitor **109** connects terminal **102** to the B– lead **93.** This resistor and capacitor serve the same function as resistors **58, 59** and capacitors **56, 57** in the FIG. **2** circuit.

The bases of transistors **91, 92** are connected by diodes **111, 112,** respectively, to a common Zener diode **113** in turn connected to the B– lead **93.** The common Zener diode **113** serves the same function as individual Zener diodes **62, 64** in FIG. **2.**

Shunt diodes **114, 116** are connected across the collector-emitter terminals of transistors **91, 92,** respectively.

A capacitor **117** connecting the collectors of transistors **91, 92** restrains the rate of voltage rise on the collectors in a manner similar to the collector-emitter capacitor **68** in FIG. **2.**

Inductive-capacitive loading of the FIG. **7** inverter is accomplished by a capacitor **118** connected in series with with an inductor **119,** the combination being connected across the collectors of the transistors **91, 92.** A load **121** is connected across the capacitor **118.**

FIG. **8** illustrates how an inverter loaded with a series capacitor **122** and inductor **123** can be used to energize a "rapid-start" fluorescent lamp **124** (the details of the inverter circuit being omitted for simplication). The lamp **124** has a pair of cathodes **126, 127** connected across the capacitor **122** for supply of operating voltage in a manner identical to that previously described. In addition, the inductor **123** comprises a pair of magnetically-coupled auxiliary windings **128, 129** for electrically heating the cathodes **126, 127,** respectively. A small capacitor **131** is connected in series with lamp **124.**

FIG. **9** shows an embodiment of the present invention that is expressly aimed at an alternative way of taking advantage of the fact that the inverter output voltage of the inverter circuit arrangement of FIG. **2** has the particular trapezoidal waveshape illustrated by FIG. **3A.**

In FIG. **9,** a DC supply voltage of about 320 Volt is assumed to be provided between a B– bus and a B+ bus.

A first high-frequency bypass capacitor **BPC1** is connected between the B– bus and a junction Jc; and a second high-frequency bypass capacitor **BPC2** is connected between junction Jc and the B+ bus. The source of a first field effect transistor **FET1** is connected with the B– bus, while the drain of this same transistor is connected with a junction Jf. The source of a second field effect transistor **FET2** is connected with junction Jf, while the drain of this same transistor is connected with the B+ bus. As shown in dashed outline, each field effect transistor has a commutating diode built-in between its drain and source. A slow-down capacitor SDC is connected between junction Jf and the B– bus

The primary winding **PW** of a leakage transformer LT is connected between junction Jc and a junction Jx; the primary winding **PW1** of a first saturable current transformer **SCT1** is series-connected with the primary winding **PW2** of a second saturable current transformer **SCT2** between junctions Jf and Jx.

A secondary winding **SW1** of transformer **SCT1** is connected between the source and gate terminals of **FET1;** and a secondary winding **SW2** of transformer **SCT2** is connected between the source and gate terminals of **FET2.** A resistor **R1** is connected across secondary winding **SW1;** and a resistor **R2** is connected across secondary winding **SW2.** A Zener diode **Z1*a*** is connected with its cathode to the source of FET1 and with its anode to the anode of a Zener diode **Z1*b*,** whose cathode is connected with the gate **FET1.** A Zener diode **Z2*a*** is connected with its cathode to the source of FET2 and with its anode to the anode of a Zener diode **Z2*b*,** whose cathode is connected with the gate of **FET2.**

A secondary winding SW of leakage transformer LT is connected between ballast output terminals **BOT1** and **BOT2.**

A first fluorescent lamp **FL1** is series-connected with a second fluorescent lamp **FL2** to form a series-combination; which series-combination is connected between ballasts output terminals **BOT1** and **BOT2.** Lamp **FL1** has a first cathode **C1*a*** and a second cathode **C1*b*;** while lamp **FL2** has a first cathode **C2*a*** and a second cathode **C2*b*.** Each cathode has two cathode terminals. Each of the terminals of cathode **C1*b*** is connected with one of the terminals of cathode **C2*a*.** Each cathode's terminals are connected with the terminals of one of three separate cathode heater windings CHW.

The leakage transformer of FIG. **9** is illustrated in further detail in FIG. **10.** In particular and by way of example, leakage transformer LT includes a first and a second ferrite core element **PC1** and **PC2,** each of which is an extra long so-called E-core; which E-cores abut each other across an air gap AG. Primary winding PW is wound on a first bobbin **B1;** and secondary winding SW is wound on a second bobbin **B2.** Cathode heating windings CHW are wound on a small third bobbin **B3;** which bobbin **B3** is adjustably positioned between bobbins **B1** and **B2.**

The operation of the circuit arrangement of FIG. 9 may best be understood by referring to the voltage and current waveforms of FIGS. 11A to 11F

FIG. 11A shows the waveform of the voltage provided at the output of the half-bridge inverter of FIG. 9 during a situation where lamps FL1 and FL2 are being fully powered. In particular, FIG. 11A shows the waveform of the voltage provided at junction Jf as measured with reference to junction Jc. (The voltage at Jx is substantially equal to the voltage at Jf).

This waveform is substantially equal to that of FIG. 3A.

FIG. 11B shows the corresponding waveform of the gate-to-source voltage (i.e. the control voltage) of FET2.

FIG. 11C shows the corresponding drain current flowing through FET2; which is the current drawn by the upper half of the half-bridge inverter from the DC supply voltage (i.e., from the B+ bus ).

FIG. 11D shows the corresponding current flowing through fluorescent lamps FL1 and FL2.

FIG. 11E shows the waveform of the voltage provided at the output of the half-bridge inverter of FIG. 9 for a situation where ballast output terminals BOT1/BOT2 are unloaded except for stray (or parasitic) capacitance associated with the wiring extending between ballast output terminals BOT1/BOT2 and lamp cathodes C1*a* and C2*b*.

The waveform of FIG. 11E is substantially equal to that of FIG. 11A except for an increase in the duration of each cycle period.

FIG. 11F shows the corresponding open circuit output voltage present across ballast output terminals BOT1 and BOT2.

FIG. 11G shows the waveform of the voltage provided at the output of the half-bridge inverter of FIG. 9 for a situation where: (i) slowdown capacitor SDC has been removed; and (ii) ballast output terminals BOT1/BOT2 are unloaded except for stray (or parasitic) capacitance associated with the wiring extending between ballast output terminals BOT1/BOT2 and lamp cathodes C1*a* and C2*b*.

It is noted that the waveform of FIG. 11G is substantially a true squarewave as opposed to the trapezoidal (or truncated sinusoidal) waveforms of FIGS. 11A and 11E.

FIG. 11H shows the waveform of the corresponding voltage present across ballast output terminals BOT1 and BOT2.

FIG. 11I shows the trapezoidal waveform most nearly equal to a given sinusoidal waveform (which trapezoidal waveform can be seen to be closely similar to that of FIG. 1A). That is, the particular trapezoidal waveform shown represents a best fit—as far as a trapezoidal waveform is concerned—to a sinusoidal waveform. This best fit is arrived-at by superimposing a trapezoidal waveform on the given sinusoidal waveform and by varying the shape and/or magnitude of the trapezoidal waveform until a shape and a magnitude are found that provides for the minimum RMS magnitude of the difference in the two waveforms; which minimum difference is shown by the lightly dashed waveform.

FIG. 11J shows the corresponding situation for a squarewave, indicating a much larger RMS magnitude for the resulting minimum difference; which is to say that a squarewave voltage is a much poorer approximation to a sinewave voltage than is a properly chosen trapezoidal voltage.

The basic inverter part of FIG. 9 operates much like the inverter part of FIG. 2, except that the switching transistors are field effect transistors instead of bi-polar transistors.

The loading of the inverter, however, is different. In the circuit of FIG. 9, the inverter's output voltage is applied to the primary winding of a leakage transformer (LT); and the output is drawn from a primary winding of this leakage transformer. In this connection, it is important to notice that a leakage transformer is a transformer wherein there is substantial leakage of magnetic flux between the primary winding and the secondary winding; which is to say that a substantial part of the flux generated by the transformer's primary winding does not link with the transformer's secondary winding.

The flux leakage aspect of transformer LT is illustrated by the structure of FIG. 10. Magnetic flux generated by (and emanating from) primary winding PW passes readily through the high-permeability ferrite of ferrite core FC1. However, as long as secondary winding SW is connected with a load at its output (and/or if there is an air gap, as indeed there is), the flux emanating from the primary winding has to overcome magnetic impedance to flow through the secondary winding; which implies the development of a magnetic potential difference between the legs of the long E-cores—especially between the legs of ferrite core FC1. In turn, this magnetic potential difference causes some of the magnetic flux generated by the primary winding to flow directly between the legs of the E-cores (i.e. directly across the air gap between the legs of the E-cores), thereby not linking with (i.e. flowing through) the secondary winding. Thus, the longer the legs of the E-cores and/or the larger the air gap, the less of the flux generated by the primary winding links with the secondary winding—and conversely. As a result, the magnitude of the current available from the secondary winding is limited by an equivalent internal inductance.

Due to the substantial air gap (AG), the primary winding of leakage transformer LT is capable of storing a substantial amount of inductive energy (just as is the case with inductor S1 of FIG. 2). Stated differently but equivalently, leakage transformer LT has an equivalent input-shunt inductance (existing across the input terminals of its primary or input winding) capable of storing a substantial amount of energy. It also has an equivalent output-series inductance (effectively existing in series with the output terminals of its secondary or output winding) operative to limit the magnitude of the current available from its output. It is important to recognize that the input-shunt inductance is an entity quite separate and apart from the output-series inductance.

Just as in the circuit of FIG. 2, when one of the transistors is switched OFF, the current flowing through primary winding PW can not instantaneously stop flowing. Instead, it must continue to flow until the energy stored in the input-shunt inductance is dissipated and/or discharged. In particular and by way of example, at the moment FET2 is switched OFF, current flows through primary winding PW, entering at the terminal connected with junction Jx and exiting at the terminal connected with junction Jc. Just after the point in time where FET2 is switched OFF, this current will continue to flow, but—since it can not any longer flow through transistor FET2—it must now flow through slow-down capacitor SDC. Thus, the current drawn out of capacitor SDC will cause this capacitor to change its voltage: gradually causing it to decrease from a magnitude of about +160 Volt (which is the magnitude of the DC supply voltage present at the B+ bus as referenced-to junction Jc) to about −160 Volt (which is the magnitude of the DC supply voltage present at the B− bus as referended-to junction Jc). Of course, as soon as it reaches about −160 Volt, it gets clamped by the commutating (or shunting, or clamping) diode built-

into FET1; which built-in diode corresponds to shunting diode 67 of the FIG. 2 circuit.

The resulting waveform of the inverter's output voltage will be as illustrated by FIGS. 11A and 11E. The slope of the inverter output voltage as it alternatingly changes between −160 Volt and +160 Volt is determined by two principal factors: (i) the value of the input-shunt inductance of primary winding PW; and (ii) the magnitude of slow-down capacitor SDC. The lower the capacitance of the slow-down capacitor, the steeper the slope. The lower the inductance of the input-shunt inductance, the steeper the slope. Without any slow-down capacitor, the slope will be very steep: limited entirely by the basic switching speed of the inverter's transistors; which, for field effect transistors is particularly high (i.e. fast).

In particular, in the circuit of FIG. 9, the relatively modest up- and down- slopes of the inverter's output voltage (see waveforms of FIGS. 11A and 11E)—which are determined by the capacitance of the slow-down capacitor—are chosen to be far lower than the very steep slopes that result when the slow-down capacitor is removed; which latter situation is illustrated by FIG. 11G. In fact, the slopes of the inverter's output voltage are chosen in such manner as to result in this output voltage having a particularly low content of harmonic components, thereby minimizing potential problems associated with unwanted resonances of the output-series inductance with parasitic capacitances apt to be connected with ballast output terminals BOT1/BOT2 by way of more-or-less ordinary wiring harness means used for connecting between these output terminals and the associated fluorescent lamps (FL1 and FL2).

With the preferred capacitance value of slow-down capacitor SDC, the inverter output voltage waveform will be as shown in FIGS. 11E, and the output voltage provided from secondary winding SW—under a condition of no load other than that resulting from a parasitic resonance involving a worst-value of parasitic output capacitance—will be as shown in FIG. 11F.

On the other hand, without having any slow-down capacitor, the inverter output voltage waveform will be as shown in FIG. 11G, and the output voltage provided from secondary winding SW—under a condition of no load other than that resulting from a parasitic resonance involving a worst-value of parasitic output capacitance—will be as shown in FIG. 11 H. Under this condition, the power drawn by the inverter from its DC supply is more than 50 Watt; which power drain result from power dissipations within the inverter circuit and—if permitted to occur for more than a very short period—will cause the inverter to self-destruct.

On the other hand, the power drawn by the inverter under the same identical condition except for having modified the shape of the inverter's output voltage to be like that of FIG. 11E (instead of being like that of FIG. 11 G) is only about 3 Watt; which amount of power drain is small enough not to pose any problem with respect to inverter self-destruction, nor even with respect to excessive power usage during extended periods where the inverter ballast is connected with its power source but without actually powering its fluorescent lamp load.

One difference between the circuit of FIG. 2 and that of FIG. 9 involves that fact that the FIG. 9 circuit uses field effect transistors. Never-the-less, the control of each transistor is effected by way of saturable current feedback transformers. However, instead of delivering its output current to a base-emitter junction, each current transformer now delivers its output current to a pair of series-connected opposed-polarity Zener diodes (as parallel-connected with a damping resistor and the gate-source input capacitance). The resulting difference in each transistor's control voltage is seen by comparing the waveform of FIG. 3B with that of FIG. 11B. In either case, however, the transistor is not switched into its ON-state until after the absolute magnitude of the voltage across its switched terminals (i.e. the source-drain terminals for a FET) has substantially diminished to zero.

In further contrast with the arrangement of FIG. 2, the inverter circuit of FIG. 9 is not loaded by way of a series-tuned L-C circuit. Instead, it is in fact loaded with a parallel-tuned L-C circuit; which parallel-tuned L-C circuit consists of the slow-down capacitor SDC as parallel-connected with the input-shunt inductance of primary winding PW. Yet, in complete contrast with other inverters loaded with parallel-tuned L-C circuits, the inverter of FIG. 9 is powered from a voltage source providing a substantially fixed-magnitude (i.e. non-varying) DC voltage.

Also in complete contrast with other inverters loaded with parallel-tuned L-C circuits, the inverter circuit of FIG. 9 provides for clamping (or clipping or truncating) of the naturally sinusoidal resonance voltage that would otherwise (i.e. in the absence of clamping) develop across the parallel-tuned L-C circuit; which naturally sinusoidal resonance voltage is illustrated by the dashed waveform of FIG. 11E.

In the FIG. 9 circuit, the indicated voltage clamping (or clipping or truncating) is accomplished by way of the commutating (or shunting) diodes built into each of the field effect switching transistors. In the FIG. 2 circuit, this clamping is accomplished by shunting diodes 66 and 67.

As previously indicated, to minimize the spurious and potentially damaging resonances which might occur due to an unknown parasitic capacitance becoming connected with ballast output terminals BOT1 and BOT2, it is important to minimize the harmonic content of the inverter's output voltage (which harmonic content—for a symmetrical inverter waveform—consists of all the odd harmonics in proportionally diminishing magnitudes). To attain such harmonic minimization, it is important that the inverter's output voltage be made to match or fit as nearly as possible the waveform of a sinusoidal voltage; which "best fit" occurs when the duration of the up/down-slopes equals about 25% of the total cycle period; which, as can readily be seen by direct visual inspection, corresponds closely to the waveforms actually depicted by FIGS. 3A, 11A and 11E.

However, substantial beneficial effects actually results even if the total duration of the up/down slopes were to be less than 25% of the total duration of the inverter output voltage period. In fact, substantial beneficial effects are attained with up-down slopes constituting as little as 10% of the total cycle period.

## Details of Construction of the Main Preferred Embodiment

In FIG. 12, which represents the main preferred embodiment of the invention, a source S of 120 Volt/60 Hz voltage is applied to power input terminals PIT1 and PIT2 of a full-wave bridge rectifier BR, the unidirectional voltage output of which is provided between DC output terminals DC− and DC+. The DC-terminal is connected with a B− bus.

A field-effect transistor Qu is connected with its source terminal to the B− bus and with its drain terminal to the anode of a high-speed rectifier HR1, whose cathode is connected with a B+ bus. Another high-speed rectifier HR2

is connected with its anode to the DC+ terminal and with its cathode to the B+ bus. An energy-storing inductor ESI is connected between the DC+ terminal and the drain terminal of transistor Qu; and an energy-storing capacitor ESC is connected between the B– bus and the B+ bus.

Between the B+ bus and the B– bus are also connected a series-combination of two transistors Q1 and Q2; the emitter of transistor Q1 being connected with the B– bus; the collector of transistor Q2 being connected with the B+ bus; and the collector of transistor Q1 and the emitter of transistor Q2 are both connected with a junction Jq.

A saturable current transformer ST1 has a secondary winding ST1s connected between the base and the emitter of transistor Q1; and a saturable current transformer ST2 has a secondary winding ST2s connected between the base and the emitter of transistor Q2. A resistor R1 is also connected between the base and the emitter of transistor Q1; and a resistor R2 is connected between the base and the emitter of transistor Q2.

Saturable transformer ST1 has a primary winding ST1*p*, and saturable transformer ST2 has a primary winding ST2*p*; which two primary windings are series-connected between junction Jq and a junction Jx.

A first tank capacitor C' is connected between junction Jq and the B– bus. A tank inductor L is connected between junction Jx and a junction Jy; and a second tank capacitor C" is connected between junction Jy and the B– bus.

Junction Jy is connected with the anode of a high-speed rectifier HR3, whose cathode is connected with the B+ bus. A high-speed rectifier HR4 is connected with its cathode to the anode of rectifier HR3 and with its anode to the B– bus.

Junction Jx is connected with ballast output terminals BOT1; and junction Jy is connected with ballast output terminal BOT2.

A first fluorescent lamp FL1 is disconnectably connected in series with a first ballast capacitor BC1 to form a first series-combination; which first series-combination is connected between ballast output terminals BOT1 and BOT2. Similarly, a second fluorescent lamp FL2 is disconnectably connected in series with a second ballast capacitor BC2 to form a second series-combination; which second series-combination is also connected between ballast output terminals BOT1 and BOT2.

A capacitor C1 is connected between junction Jq and the gate terminal of transistor Qu; and a Zener diode Z1 is connected with its cathode to the gate terminal of transistor Qu and with its anode to the B– bus.

A capacitor C2 is connected between junction Jq and the cathode of a Zener diode Z2, whose anode is connected with the B– bus. A high-speed rectifier HR5 is connected with its anode to the cathode of Xener diode Z2 and with its cathode to a junction Jn. A capacitor C3 is connected between junction Jn and the B– bus.

A control transistor Qc is connected with its collector to the gate terminal of field effect transistor Qu and with its emitter to the B– bus. A resistor R3 is connected between the base of transistor Qc and the B– bus. An interval timer circuit ITC (such as an RC-type timer based on a so-called programmable unijunction transistor or PUT) has: (i) a positive DC power input terminal PIT+ connected with junction Jn; (ii) a negative DC power input terminal PIT– connected with the B– bus; (iii) a first control input terminal CIT1 connected with the gate terminal of transistor Qu; (iv) a second control input terminal CIT2; and (v) a control output terminal COT connected with the base of transistor Qc.

A Zener diode Z3 is connected with its cathode to the B+ bus; a resistor R4 is connected between signal input terminal SIT and the anode of Zener diode Z3; a resistor R5 is connected between second control input terminal CIT2 and the B– bus; and a resistor R6 is connected between the DC+ terminal and second control input terminal CIT2.

A set of cathode heater windings CHW are wound on tank inductor L; which cathode heater windings are connected with the thermionic cathodes of fluorescent lamps FL1 and FL2.

FIG. 13 provides certain details of tank inductor L and its associated cathode heater windings CHW.

Tank inductor L is wound on a main bobbin MB, which is positioned on the center leg CL of a ferrite E-core FEC, which is combined with an matching ferrite I-core FIC. Two of the cathode heater windings (the two which each powers a single thermionic cathode) are wound on a first auxiliary bobbin AB1, which is placed on one of the outer legs OL1 of ferrite E-core FC; and the remaining cathode heater winding (the one that powers two thermionic cathodes) is wound on a second auxiliary bobbin AB2, which is placed on the other outer leg OL2 of the ferrite E-core.

## Explanation of Waveforms of FIG. 14

With reference to the circuit diagram of FIG. 12, the various waveforms of FIG. 14 may be explained as follows.

Waveform (a) represents the 120 Volt/60 Hz power line voltage present across power input terminals PIT1/PIT2.

Waveform (b) represents the current flowing from the power line and into power input terminals PIT1/PIT2.

Waveform (c) represents the alternating voltage present at junction Jq, which is substantially the same as that present at junction Jx, prior to lamp ignition.

Waveform (d) represents the alternating voltage present at junction Jy prior to lamp ignition.

Waveform (e) represents the voltage present between junctions Jx and Jy, which is the same as the voltage present between ballast output terminals BOT1 and BOT2, prior to lamp ignition.

Waveform (f) represent the current flowing through tank inductor L.

Waveform (g) represent the waveform of the voltage present at the base of transistor Q1.

Waveform (h) represents the alternating voltage present at junction Jq, which is substantially the same as that present at junction Jx, after lamp ignition.

Waveform (i) represents the alternating voltage present at junction Jy after lamp ignition.

Waveform (j) represents the voltage present between junction Jx and Jy, which is the same voltage as is present between ballast output terminals BOT1 and BOT2, after lamp ignition.

Waveform (k) represents the current flowing through one of the fluorescent lamps in response to the voltage represented by waveform (j).

Waveform (l) represent the current flowing through tank inductor L after lamp ignition.

## Details of Operation of the Main Preferred Embodiment

The unfiltered full-wave-rectified power line voltage present between the DC– terminal and the DC+ terminal has an instantaneous absolute magnitude that is substantially

equal to that of the 120 Volt/60 Hz power line voltage impressed between power input terminals PIT1 and PIT2. Thus, within a few milliseconds of application of this power line voltage, energy-storing capacitor ESC will be charged-up to the peak magnitude (i.e., about 160 Volt) of the power line voltage.

Self-sustaining inverter operation is then initiated by providing a brief current pulse to the base of transistor Q1. (While this can be done manually, in an actual ballast the triggering will be done automatically by way of a simple trigger means consisting of a resistor, a capacitor and a Diac.)

Once triggered, the inverter (which consists of principal components ESC, Q1, Q2, ST1, ST2, L, C', C", HR3 and HR4) will enter into a mode of stable self-oscillation as a result of the positive current feedback provided via saturable transformers ST1 and ST2; and will provide a 33 kHz (actually: a frequency in the range between 30 and 40 kHz) alternating voltage at junction Jq; the waveform of which alternating voltage will be as illustrated by waveforms (c) and (h) of FIG. 14.

The inverter's output voltage is coupled to the gate of field-effect transistor Qu by way of capacitor C1, thereby causing a positive gate voltage to develop thereat each time the inverter's output voltage increases in magnitude. More specifically, as the instantaneous magnitude of the voltage at junction Jq starts to rise (i.e., starts going toward a positive potential), a pulse of positive current flows through capacitor C1 and into the gate of Qu, thereby causing the voltage at the gate to increase rapidly to the point where Zener diode Z1 starts to conduct in its Zenering mode. That is, by action of Zener diode Z1, the voltage on the gate is prevented from attaining a positive voltage higher than about 15 Volt. Once having increased to 15 Volt positive, however, the gate voltage will remain substantially at that level until either: (i) a reverse current is provided through capacitor C1, or (ii) control transistor Qc is switched ON. Such a reverse current will indeed be provided as soon as the instantaneous magnitude of the voltage at junction Jq starts to fall (i.e., starts going toward a negative potential); which will occur about 15 micro-seconds after it started to rise. (It is noted, however, that the gate voltage is prevented from going more than about 0.7 Volt negative due to the plain rectifier action of Zener diode Z1. )

In other words, a 33 kHz substantially squarewave-shaped alternating voltage is provided at the gate of transistor Qu, thereby—at a 33 kHz rate—causing this transistor to switch ON and OFF with an ON-duty-cycle that is limited to a maximum of 50%. Thus, during each positive-voltage segment of the squarewave-like gate voltage, energy-storing inductor ESI gets connected across terminals DC– and DC+, thereby to be charged-up from the voltage present therebetween. Then, during each zero-voltage (or negative-voltage) segment of the squarewave-like gate voltage, the energy having been stored-up in inductor ESI during the previous half-cycle gets deposited on energy-storing capacitor ESC via rectifier HR1.

If transistor Qu were to be switched ON and OFF at a constant frequency (i.e., 33 kHz ) and at a constant duty-cycle (e.g., 50%), the magnitude of the current drawn from the DC+ terminal would increase more than proportionally with the magnitude of the DC voltage provided thereat; which would result in the instantaneous magnitude of the current drawn from the power line not being proportional to the instantaneous magnitude of the power line voltage; which, in turn, would result in a lower-than-desired power factor as well well as a higher-than-desired amount of harmonics.

Without any input provided to its second control input terminal CIT2, the interval timer circuit (ITC) operates in such manner as to cause control transistor Qc automatically to switch ON about 12 micro-seconds each time after the field effect transistor Qu has been switched ON. Thus, absent a control voltage at second control input terminal CIT2, field effect transistor Qu is switched ON for a duration of about 12 micro-seconds once every 30 micro-seconds (i.e., at a rate of 33 kHz).

However, this duration of 12 micro-seconds is caused to decrease as a monotonic function of the magnitude of the voltage provided at second control input terminal CIT2; and, since the magnitude of the voltage provided at this second control input terminal CIT2 is made to increase with increasing magnitude of the DC+ voltage (as provided via resistor R6), the duration of the ON-time of the field effect transistor Qu will decrease with increasing magnitude of the DC+ voltage. As an overall result, the waveshape of the current drawn from the power line will be improved, thereby providing for a power factor of about 99% and a total harmonic distortion of well under 10%.

A key aspect of the main preferred embodiment relates to the shape of the waveform of the alternating voltage provided at the inverter's output (e.i., at junction Jq); which waveform is shown by waveforms (c) and (h) in FIG. 14 and may be described as a first quarter segment consisting of the initial 90 degrees of a sinusoidally rising voltage, followed by a second quarter segment consisting of a substantially constant-magnitude positive voltage, followed by a third quarter segment consisting of the initial 90 degrees of a sinusoidally falling voltage, followed by a fourth quarter segment consisting of a substantially constant-magnitude negative voltage.

This particular wave shape is attained in part by making the tank inductor have a natural resonance frequency with tank capacitor C' that is substantially equal to the inverter's fundamental operating frequency.

However, the shape of the waveform of the alternating voltage provided at junction Jy is equally important to the proper functioning of the preferred embodiment; which waveshape is illustrated by waveforms (d) and (i) of FIG. 14, and may be described in a manner similar to that of the waveform of the alternating voltage provided at junction Jq.

The particular waveshape of the alternating voltage present at junction Jy is attained in part by making the tank inductor have a natural resonance frequency with tank capacitor C" that is substantially equal to that of the inverter's fundamental operating frequency. Thus, the capacitance of tank capacitor C' should be about equal to that of tank capacitor C".

Moreover, the ON-time of each of the inverter's two switching transistors (Q1 and Q2) should be equal to one quarter of the duration of a complete period of the natural resonance frequency of the tank inductor and either one of the two tank capacitors (C' and C").

The voltage existing between junctions Jq (or Jx) and junction Jy will be perfectly sinusoidal when all the conditions spelled-out above are in effect. However, prior to lamp ignition, the waveform is sinusoidal except for brief intervals between each half-cycle; during which intervals the magnitude is zero. Yet, after lamp ignition, the waveform is indeed sinusoidal.

The reason for the difference in the waveforms before and after lamp ignition relates mainly to the effect of loading the

L-C'/C" tuned circuit; which loading causes the natural resonance period to change slightly from the unloaded condition.

As can be seen from waveform (k) of FIG. 14, the crest factor of the resulting lamp current is about 1.4, which is considered excellent.

It should be noted that, under the condition of perfect timing and tuning—as represented by waveform (j) of FIG. 14—only one of the tank capacitors is acting as tank capacitor at any one time. In fact, they alternate with quarter cycle intervals.

The peak magnitude of the ballast output voltage—i.e., the voltage provided between junctions Jx and Jy—is exactly equal to the magnitude of the DC supply voltage provided between the B– bus and the B+ bus. A typical preferred magnitude for the DC supply voltage is about 350 Volt; which magnitude can—by way of simple control of the up-converter function (as provided by field-effect transistor Qu in combination with its associated timing circuit)—briefly be increased to about 450 Volt to facilitate the lamp ignition process.

The magnitude of the DC supply voltage is regulated by way of interval timer circuit ITC to be about 350 Volt. This regulation is accomplished with the help of Zener diode Z3, which has a Zenering voltage slightly below 350 Volt. Thus, as soon as the magnitude of the DC supply voltage tends to increase beyond 350 Volt, current starts flowing through resistor R4, thereby: (i) starting to increase the magnitude of the voltage applied to the second control input terminal CIT2, (ii) in turn, starting to shorten the duration of the ON-time of field effect transistor Qu, and (iii) in further turn, to reduce the amount of energy pumped up to the B+ bus per operating cycle of the up-converter.

The 33 kHz voltage provided between the ballast output terminals BOT1 and BOT2 is balanced with respect to ground; which means that electric shock hazard problems are automatically mitigated. In fact, in case of ordinary F40/T-12 fluorescent lamps, with reference to the so-called U.L. "pin test", safety from electric shock hazard is provided for without resorting to the usual isolation transformer or ground-fault interrupt means.

## Details of the Modified Main Preferred Embodiment

The circuit arrangement of FIG. 15 is identical to that of FIG. 12 except that: (i) a high-pass capacitor HPC is connected between junction Jx and ballast output terminal BOT1; (ii) a first series-combination of a first starting aid diode SAD1 and a first starting aid resistor SAR1 is connected across the terminals operative to receive and hold fluorescent lamp FL1; and (iii) a second series-combination of a second starting aid diode SAD2 and a second starting aid resistor SAR2 is connected across the terminals operative to receive and hold fluorescent lamp FL2.

The main purpose of capacitor HPC is that of blocking the flow of unidirectional and low frequency (i.e., 60 Hz) current from any of the lamp sockets (i.e., from any the terminals operative to receive and hold the fluorescent lamps) to ground. The purpose of this blockage is that of preventing electric shock hazard to a person servicing the lighting fixture in which the lamps are used. The high-frequency voltage developing across capacitor HPC is of negligible magitude in comparison with the magnitude of the high-frequency voltage provided between ballast output terminals BOT1 and BOT2.

To avoid such self-destruction, arrangements can readily be made whereby the very act of removing the load automatically establishes a situation that prevents the possible destruction of the power supply and ballasting means. For instance, with the tank capacitor (52) being permanently connected with the lamp load (11)—thereby automatically being removed whenever the lamp is removed—the inverter circuit is protected from self-destruction.

(d) At frequencies above a few kHz, the load represented by a fluorescent lamp—once it is ignited—is substantially resistive. Thus, with the voltage across lamp 11 being of a substantially sinusoidal waveform (as indicated in FIG. 3*d*), the current through the lamp will also be substantially sinusoidal in waveshape.

(e) In the fluorescent lamp unit of FIG. 1, fluorescent lamp 11 is connected with power supply and ballasting circuit 16 in the exact same manner as is load 26 connected with the circuit of FIG. 2. That is, it is connected in parallel with the tank capacitor (52) of the L-C series-resonant circuit. As is conventional in instant-start fluorescent lamps—such as lamp 11 of FIG. 1—the two terminals from each cathode are shorted together, thereby to constitute a situation where each cathode effectively is represented by only a single terminal. However, it is not necessary that the two terminals from each cathode be shorted together; in which case—for instant-start operation—connection from a lamp's power supply and ballasting means need only be made with one of the terminals of each cathode.

(f) In FIG. 9, a Parasitic Capacitance is shown as being connected across terminals BOT1 and BOT2. The value of this parasitic capacitance may vary over a wide range, depending on unpredictable details of the particular usage situation at hand. Values for the parasitic capacitance will expectedly vary between 100 and 1000 pico-Farad—depending on the nature of the wiring harness used for connecting between the output of secondary winding SW and the plural terminals of lamps FL1/FL2.

(g) The worst case of parasitic oscillation associated with the circuit arrangement of FIG. 9 is apt to occur when the value of the parasitic capacitance (i.e., the capacitance of the ballast-to-lamp wiring harness) is such as to cause series-resonance with the output-series inductance of secondary winding

The purpose of each of the two series-combinations—which consist of elements SAD1 & SAR1 and SAD2 & SAR2—is that of facilitating lamp ignition. The magnitude of each of starting aid resistors SAR1 and SAR2 is chosen such as to provide for a certain degree of build-up of DC voltage on each of the associated ballast capacitors; which DC voltage will aid in lamp ignition; yet, being strictly limited in terms of the maximum amount of DC current caused to flow through the lamp during normal operation, will have no negative impact on basic lamp life and function.

The advantage of the indicated DC starting aid circuit is that it permits proper lamp starting with far lower magnitude of high-frequency outout voltage than otherwise required. For instance, due to certain peculiarities with some F34/T-12 fluorescent lamps, without the herein described DC starting aid method, a lamp starting voltage of about 350 Volt RMS is required. With instant DC starting aid method, a starting voltqage of 250 Volt RMS is quite sufficient.

Of course, reduced starting voltage requirements give rise to improved ballast efficiency, lighter component specifications, reduced size and weight, etc.

## Additional Explanations and Comments

(a) With reference to FIGS. 2 and 5, adjustment of the amount of power supplied to load 26', and thereby the

amount of light provided by lamp 71, may be accomplished by applying a voltage of adjustable magnitude to input terminals IP1 and IP2 of the Toroid Heater; which is thermally coupled with the toroidal ferrite cores of saturable transformers 47, 49.

(b) With commonly available components, inverter circuit 24 of FIG. 2 can be made to operate efficiently at any frequency between a few kHz to perhaps as high as 50 kHz. However, for various well-known reasons (i.e., eliminating audible noise, minimizing physical size, and maximizing efficiency), the frequency actually chosen is in the range of 20 to 40 kHz.

(c) The fluorescent lighting unit of FIG. 1 could be made in such manner as to permit fluorescent lamp 11 to be disconnectable from its base 12 and ballasting means 16. However, if powered with normal line voltage without its lamp load connected, frequency-converting power supply and ballasting circuit 16 is apt to self-destruct. SW at the third harmonic component of the inverter's output voltage. The next worst case of parasitic oscillation is apt to occur when the value of the parasitic capacitance is such as to series-resonate with the output-series inductance at the fifth harmonic component of the inverter's output voltage. With the typical value of 5.4 milli-Henry for the output-series inductance, it takes a total of about 600 pico-Farad to resonate at the third harmonic component of the inverter's 30 kHz output voltage; and it takes about 220 pico-Farad to resonate at the fifth harmonic component of the inverter's output voltage. These capacitance values are indeed of such magnitudes that they may be encountered in an actual usage situation of an electronic ballast. Moreover, at higher inverter frequencies, the magnitudes of the critical capacitance values become even lower.

(h) FIG. 10 shows cathode heater windings CHW placed on a bobbin separate from that of primary winding PW as well as separate from that of secondary winding SW. However, in many situations, it would be better to place the cathode heater windings directly onto the primary winding bobbin B1. In other situations it would be better to place the cathode heater windings directly onto the secondary winding bobbin B2.

If the cathode heater windings are wound on bobbin B1 (i.e. in tight coupling with the primary winding), the magnitude of the cathode heating voltage will remain constant regardless of whether or not the lamp is ignited; which effect is conducive to maximixing lamp life. On the other hand, if the cathode heater windings are wound on bobbin B2 (i.e. in tight coupling with the secondary winding), the magnitude of the cathode heating voltage will be high prior to lamp ignition and low after lamp ignition; which effect is conducive to high luminous efficacy.

By placing the cathode heater windings in a location between primary winding PW and secondary winding SW, it is possible to attain an optimization effect: a maximization of luminous efficacy combined with only a modest sacrifice in lamp life. That is, by adjusting the position of bobbin B3, a corresponding adjustment of the ratio of pre-ignition to post-ignition cathode heater voltage magnitude may be accomplished.

(i) For easier lamp starting, a starting aid capacitor may be used in shunt across one of the fluorescent lamps FL1/FL2.

Also, a starting aid electrode (or ground plane) may advantageously be placed adjacent the fluorescent lamps; which starting aid electrode should be electrically connected with the secondary winding, such as via a capacitor of low capacitance value.

(j) To control (reduce) the degree of magnetic coupling between primary winding PW and secondary winding SW, a magnetic shunt may be positioned across the legs of the E-cores—in a position between bobbins B1 and B3.

(k) Considering the waveforms of FIGS. 1A, 11A and 11E each to include 360 degrees for each full and complete cycle: (i) each half-cycle would include 180 degrees; (ii) each total up-slope would include almost or about 60 degrees degrees; (iii) each total down-slope would include almost or about 60 degrees; and (iv) each horizontal segment would include about 120 degrees or more. Yet, as previously indicated, substantial utility may be attained even if each complete up-slope and down-slope were to include as little 18 degrees.

(l) In the FIG. 9 circuit, the inverter's operating frequency is not ordinarily (or necessarily) equal to the natural resonance frequency of the parallel-tuned L-C circuit that consists of slow-down capacitor SDC and the input-shunt inductance of primary winding PW. Rather, the inverter's actual operating frequency is ordinarily lower than would be this natural resonance frequency.

(m) With reference to FIG. 11I, in a trapezoidal waveform that constitutes a best fit for a sinusoidal waveform, the peak magnitude is lower than that of the sinusoidal waveform, and the up-slope and down-slope are each steeper that the corresponding slopes of the sinusoidal waveform.

(n) The FIG. 9 inverter arrangement has to be triggered into self-oscillation. A suitable automatic triggering means would include a resistor, a capacitor, and a so-called Diac. However, manual triggering may be accomplished by merely momentarily connecting a discharged capacitor (of relatively small capacitance value) between the gate of transistor FET1 and the B+ bus.

(o) Most switching-type field effect transistors have built-in commutating (or shunting) diodes, as indicated in FIG. 9. However, if such were not to be the case, such diodes should be added externally, as indicated in the FIG. 2 circuit.

(p) In ordinary inverter circuits, the inverter output voltage is effectively a squarewave voltage with very steep up-slopes and down-slopes. In inverters using field effect transistors, the time required for the inverter's squarewave output voltage to change between its extreme negative potential to its extreme positive potential is usually on the order of 100 nano-seconds or less. In inverters using bi-polar transistors, this time is usually on the order of 500 nano-seconds or less. In the inverter of the FIG. 9 circuit, however, this time has been extended—by way of the large-capacitance-value slow-down capacitor SDC—to be on the order of several micro-seconds, thereby achieving a substantial reduction of the magnitudes of the harmonic components of the inverter's (now trapezoidal) output voltage.

(q) In an actual prototype of the FIG. 9 ballast circuit—which prototype was designed to properly power two 48 inch 40 Watt T-12 fluorescent lamps—the following approximate parameters and operating results prevailed:

1. operating frequency: about 30 kHz;
2. slow-down capacitor: 0.02 micro-Farad;
3. shunt-input inductance: 1.4 milli-Henry;
4. up-slope duration: about 4 micro-seconds;
5. down-slope duration: about 4 micro-seconds;
6. series-output inductance: 5.4 milli-Henry;
7. parasitic capacitance across BOT1/BOT2 terminals; 800 pico-Farad;
8. power consumption when unloaded: about 4 Watt;
9. power consumption when loaded with two F40/T12 fluorescent lamps: about 70 Watt;

10. power consumption when unloaded but with slow-down capacitor removed: about 80 Watt.

It is be noted that the natural resonance frequency of the L-C circuit consisting of a slow-down capacitor of 0.02 micro-Farad as parallel-combined with a shunt-input inductance of about 1.4 milli-Henry is about 30 kHz. This means that—as far as the fundamental component of the 30 kHz inverter output voltage is concerned—the parallel-tuned L-C circuit represents a very high impedance, thereby constituting no substantive loading on the inverter's output.

(r) Of course, the FIG. **9** ballast circuit can be made in the form of a push-pull circuit such as illustrated by FIG. **7**; in which case center-tapped transformer **96** would be modified in the sense of being made as a leakage transformer in full correspondence with leakage transformer LT of FIG. **9**. Also, of course, inductor **119**, capacitor **118**, and load **121** would be removed. Instead, the load would be placed at the output of the secondary winding of the modified center-tapped transformer **96**; which would be made such as to have appropriate values of input-shunt inductance and output-series inductance. Capacitor **117** would constitute the slow-down capacitor.

(s) The auxiliary DC supply voltage required for proper operation of interval timer circuit ITC is obtained by way of capacitor C2 from the inverter's squarewave output voltage. The magnitude of this auxiliary DC supply voltage (about 10 Volt) is determined by the Zenering voltage of Zener diode Z2. Filtering filtering of this DC voltage is accomplished via capacitor C3.

(t) To meet usual requirements with respect to EMI suppression, suitable filter means is included with bridge rectifier BR.

(u) Further details with respect to the operation of a half-bridge inverter is provided in U.S. Pat. No. 4,184,128 to Nilssen, particularly via FIG. **8** thereof.

(v) Power source S in FIG. **1** is shown as having one of its terminals connected with earth ground. In fact, it is standard practice that one of the power line conductors of an ordinary electric utility power line be electrically connected with earth ground.

(w) The B– bus of the ballast circuit of FIG. **2** is connected with one of the DC output terminals of bridge rectifier BR; which means that, at least intermittently, the B– bus is electrically connected with earth ground.

(x) The term "crest factor" pertains to a waveform and identifies the ratio between the peak magnitude of that waveform to the RMS magnitude of that waveform. Thus, in case of a sinusoidal waveform, the crest factor is about 1.4 in that the peak magnitude is 1.4 times as large as the RMS magnitude.

(y) In the arrangement of FIG. **12**, if additional output voltage magnitude were to be desired, an auxiliary secondary winding may be added to tank inductor L. However, except if lamps were not going to be parallel-connected, this auxiliary winding should be tightly cou-led with the tank inductor winding.

However, in case just a single fluorescent lamp (or two or more series-connected lamps) were to be used, this auxiliary secondary winding could advantageously be loosely coupled with the tank inductor winding, in which case its internal inductance could be used as the ballasting reactance.

(z) In an actual prototype of the FIG. **12** ballast circuit—which prototype was designed to properly power two 40 Watt T-12 fluorescent lamps—the following approximate parameters and operating results prevailed:

1. operating frequency: 35 kHz;
2. first tank capacitor C': 0.022 micro-Farad;
3. second tank capacitor C": 0.022 micro-Farad;
4. tank inductor L: 0.9 milli-Henry;
5. total up-slope duration: 7.0 micro-seconds;
6. total down-slope duration: 7.0 micro-seconds;
7. inverter transistor ON-time: 7.0 micro-seconds;
8. each ballast capacitor BC1/BC2: 0.0056 micro-Farad;
9. power consumption when unloaded: less than 5.0 Watt;
10. lamp current crest factor: 1.3;
11. magnitude of DC supply voltage: 400 Volt;
12. each fluorescent lamp: F40/T-12;
13. total power when fully loaded: 75 Watt.

(aa) With reference to FIG. **13**, by balancing the cathode heater windings between the two outer legs of the ferrite E-core, short circuit protection is attained. If the cathode heater winding(s) on one of the legs were to be short-circuited, the magnetic flux in the core will simply automatically flow through the other leg and—although providing more cathode heating power to the cathodes connected to the windings on this other leg—will not give rise to any critical damage.

(ab) With reference to FIG. **10**, it is noted that dimming of light output can be achieved by providing for an adjustable magnetic shunting means positioned between primary winding PW and secondary winding SW; which magnetic shunting means should provide for a shunting path for magnetic flux between the two outer legs and the center leg of the E-cores.

(ac) Careful analysis of the waveforms of FIG. **14** will reveal that—for a given magnitude of the DC supply voltage—the peak-to-peak magnitude of the AC voltage provided across ballast output terminals BOT1 and BOT2 will be ever so slightly lower before lamp ignition as compared with after lamp ignition. This effect is due to the slightly imperfect phasing between waveforms (c) and (d) versus that between waveforms (h) and (i); which imperfect phasing is evidenced by the brief zero-magnitude segments of waveform (e).

However, due to the normal effect of lamp loading, the magnitude of the DC supply voltage is apt to be somewhat higher prior to lamp ignition as compared with after lamp ignition; which latter effect will more than cancel the effect of phasing imperfection.

(ad) Although it is indicated that tank capacitor C' be of the same capacitance as that of tank capacitor C", such is by no means necessary. In fact, in some situations it is distinctly an advantage for one tank capacitor to have a larger capacitance than that of the other tank capacitor.

(ae) In FIG. **13**, an alternative location for the cathode heater windings is on ferrite I-core FIC—with one set of windings on each side of the center leg of ferrite E-core FEC.

(af) The basic concept underlying the DC starting aid circuit represented by elements SAD1 and SAR1 of FIG. **15** is that of providing a starting aid current of low frequency (or DC) in a situation where the main lamp operating power will be provided by way of a high-frequency current. That way, since the magnitude of useful starting aid current is very small compared with the magnitude of the lamp's normal operating current, the Volt-Ampere rating of the power supply means used for providing starting aid current can be very small compared with the Volt-Ampere rating of the power supply means having used to supply the main lamp operating current.

The basic value associated with supplying starting aid current via a source separate from that supplying the main

lamp operating current, is that of a substantial reduction in the Volt-Ampere requirements of the source supplying the main lamp operating current. In particular, if the lamp were to be started (i.e., ignited) by the source providing the main lamp operating current, the Volt-Ampere rating of that source would have to be the product of the lamp starting voltage and the lamp operating current. However, by way of subject starting aid means, the magnitude of the open circuit voltage actually required to be supplied by the source delivering the main lamp operating current can be reduced by a factor of about two, thereby reducing the Volt-Ampere rating of that source by that same factor.

(ag) With reference to FIG. 15, when fluorescent lamp FL1 is not connected with its socket terminals (as indicated by the two pairs of double arrows), the peak magnitude of the voltage provided between these socket terminals is equal to twice the peak magnitude of the high-frequency voltage provided at ballast output terminals BOT1 and BOT2. Similarly, with the lamp in its socket but prior to lamp ignition, and assuming resistor SAR1 to be of sufficiently low resistance value (e.g., about 22 kOhm) the peak magnitude of the voltage present across the lamp terminals is equal to twice the peak magnitude of the high frequency voltage; which explains why the series-combination of diode SAD1 and resistor SAR1 connected across the lamp terminals constitutes such an effective starting aid means in situations where the main lamp operating current is sullied by way of a capacitor, such as ballast capacitor BC1.

(ah) In the circuit arrangement of FIG. 15, the lamps are seen to be connected directly across inductor L. However, in most cases either a higher-magnitude voltage or a lower-magnitude voltage than that developing across inductor L will be required for optimum operation of the lamps. Whenever a higher-magnitude voltage is required, the preferred arrangement is to tightly couple two additional windings with inductor L. One of these windings should then be used in auto-transformer fashion to add to the magnitude of the output voltage provided at ballast output terminals BOT1; and the other of these windings should similarly be used to add to the magnitude of the output voltage provided at ballast output terminals BOT2. Whenever a lower-magnitude voltage is required, ballast output terminals should be connected with two symmetrically-arranged taps on inductor L.

(ai) By direct inspection of FIG. 14, it can be seen that the RMS magnitude of waveform (j), which represents the AC voltage present between ballast output terminals BOT1/BOT2 under full load, is larger than that of waveform (d), which represents the AC voltage present between output terminals BOT1/BOT2 under no load.

Thus, the RMS magnitude of the AC output voltage provided between ballast output terminals BOT1 and BOT2 is larger after the lamps have ignited compared with prior to lamp ignition.

(aj) It is thought that the present invention and many of its attendant advantages will be understood from the foregoing description and that many changes may be made in the form and construction of its components parts, the form described being merely a preferred embodiment of the invention.

I claim:

1. An arrangement comprising:

a source functional to provide an AC voltage between a first and a second source terminal; there being substantially no galvanic connection between the first source terminal and earth ground; there being substantial galvanic connection between the second source terminal and earth ground; the term galvanic connection being defined as a connection by way of which a unidirectional current can flow;

a capacitor having a first and a second capacitor terminal; the first capacitor terminal being connected with the second source terminal; and

gas discharge lamp having a first and a second lamp terminal disconnectably connected with the first source terminal and the second capacitor terminal, respectively;

whereby neither the first source terminal nor the second capacitor terminal exhibits galvanic connection with earth ground.

2. The arrangement of claim 1 wherein the frequency of the AC voltage is larger by at least two orders of magnitude compared with the frequency of the power line voltage normally present at an ordinary electric utility power line.

3. The arrangement of claim 1 wherein: (i) the source is connected in circuit with an ordinary electric utility power line; and (ii) current of frequency about equal to that of the voltage present on the power line is substantially prevented from flowing between earth ground and the first source terminal as well as between earth ground and the second capacitor terminals.

4. The arrangement of claim 1 wherein, prior to lamp ignition: (i) an ignition voltage exists between the lamp terminals; and (ii) the ignition voltage includes a substantial component of DC voltage.

5. An arrangement comprising:

a circuit assembly operative to provide a DC voltage at a pair of DC terminals;

an inverter connected with the DC terminals and operative to provide an AC voltage between a pair of AC terminals;

gas discharge lamp having a pair of lamp terminals; and

a sub-circuit connected between the AC terminals and the lamp terminals; the sub-circuit being operative to cause a lamp current to flow through the lamp;

the arrangement being operative to cause the RMS magnitude of the AC voltage to be higher after lamp ignition compared with before lamp ignition.

6. An arrangement comprising:

a power source providing a power line voltage at a pair of power line terminals;

a first sub-circuit connected with the power line terminals and operative to provide a DC voltage at a pair of DC terminals;

a second sub-circuit connected with the DC terminals and operative to provide an AC voltage between a pair of AC terminals; the second sub-circuit being characterized by having two transistors series-connected between the DC terminals; the AC voltage being characterized by being non-sinusoidal and by having a peak-to-peak magnitude distinctly higher than the peak magnitude of the power line voltage; the AC voltage being further characterized by having a fundamental period: (i) during a first part of which its instantaneous magnitude remains substantially constant at a first given level; and (ii) during a second part of which its instantaneous magnitude remains substantially constant at a second given level, the second part having a total duration substantially equal to that of the first part as well as substantially equal to at least one fourth the total duration of the whole fundamental period;

gas discharge lamp having lamp terminals; and

a third sub-circuit connected between the AC terminals and the lamp terminals; the third sub-circuit being

operative, in response to the AC voltage, to cause a lamp current to flow through the lamp.

7. The arrangement of claim 6 wherein the lamp current has a waveform that is substantially sinusoidal.

8. The arrangement of claim 6 further characterized in that the absolute magnitude of the DC voltage is distinctly higher than the peak absolute magnitde of the power line voltage.

9. The arrangement of claim 6 wherein each transistor has a pair of control terminals across which exists a transistor control voltage; the transistor control voltage being characterized by: (i) being of the same fundamental frequency as that of the AC voltage; (ii) having a peak-to-peak magnitude distinctly higher than twice the magnitude of the forward voltage drop of an ordinary junction diode; and (iii) alternating between a first substantially constant level and a second sunstantially constant level, spending a certain amount of time at each substantially constant level, which certain amount of time is equal to at least one fourth of the duration of the whole period of the AC voltage.

10. An arrangement comprising:

a power source providing a power line voltage at a pair of power line terminals;

a first sub-circuit connected with the power line terminals and operative to provide a DC voltage at a pair of DC terminals;

a second sub-circuit connected with the DC terminals and operative to provide an AC voltage between a pair of AC terminals; the AC voltage being characterized by having a fundamental period: (i) during a first part of which its instantaneous magnitude remains substantially constant at a first given level; and (ii) during a second part of which its instantaneous magnitude remains substantially constant at a second given level, the second part having a total duration substantially equal to that of the first part as well as substantially equal to at least one fourth the total duration of the whole fundamental period;

gas discharge lamp having lamp terminals;

a third sub-circuit connected between the AC terminals and the lamp terminals; the third sub-circuit being operative, in response to the AC voltage, to cause a lamp current to flow through the lamp; and

physical structure: (i) operative to combine the three sub-circuits and the gas discharge lamp in such manner as to constitute a single integral physical entity; and (ii) including a base adapted to be screwed into and held by a lamp socket of a type usually used for an ordinary household incandescent light bulb.

11. An arrangement comprising:

a power source providing a power line voltage at a pair of power line terminals;

a first sub-circuit connected with the power line terminals and operative to provide a DC voltage at a pair of DC terminals;

a second sub-circuit connected with the DC terminals and operative to provide an AC voltage between a pair of AC terminals; the AC voltage being characterized by having a fundamental period: (i) during a first part of which its instantaneous magnitude remains substantially constant at a first given level; and (ii) during a second part of which its instantaneous magnitude remains substantially constant at a second given level, the second part having a total duration substantially equal to that of the first part as well as distinctly longer than one fourth the total duration of the whole fundamental period;

gas discharge lamp having lamp terminals;

a third sub-circuit connected between the AC terminals and the lamp terminals; the third sub-circuit being operative, in response to the AC voltage, to cause a lamp current to flow through the lamp; and

physical structure combining the three subcircuits and the gas discharge lamp in such manner as to result in a single substantially rigid physical structure characterized by having a protruding threaded portion adapted to be screwed into and held by an Edison-type lamp socket.

12. An arrangement comprising:

a first sub-circuit adapted to connect with the power line voltage of an ordinary electric utility power line and, when indeed so connected, operative to provide a DC voltage at a pair of DC terminals;

a second sub-circuit connected with the DC terminals and operative to provide an AC voltage between a pair of AC terminals; the AC voltage being characterized by having a fundamental period: (i) during a first part of which its instantaneous magnitude remains substantially constant at a first given level; and (ii) during a second part of which its instantaneous magnitude remains substantially constant at a second given level, the second part having a total duration substantially equal to that of the first part as well as distinctly longer than one fourth the total duration of the whole fundamental period;

gas discharge lamp having lamp terminals;

a third sub-circuit connected between the AC terminals and the lamp terminals; the third sub-circuit being operative, in response to the AC voltage, to cause a lamp current to flow through the lamp; and

physical structure combining the three subcircuits and the gas discharge lamp in such manner as to result in a single substantially rigid physical structure characterized by having a protruding threaded portion adapted to be screwed into and held by an Edison-type lamp socket.

13. The arrangement of claim 12 further characterized by: (i) the gas discharge lamp having a longitudinal axis, a maximum longitudinal dimension, and a cross-section with a maximum crosssectional dimension; and (ii) in a situation wherein the longitudinal axis is disposed vertically, the three sub-circuits all being disposed below the gas discharge lamp.

14. The arrangement of claim 13 yet further characterized it that: (i) the threaded portion has a maximum transverse dimension; and (ii) the maximum cross-sectional dimension is no larger than three times the maximum transverse dimension of the threaded portion.

15. The arrangement of claim 12 further characterized by: (i) the threaded portion having a maximum transverse dimension; (ii) the gas discharge lamp having but a single chamber of ionizable gas; which chamber being of tubular shape; which tubularly shaped chamber being curved, thereby to give rise to a gas discharge path that is curved; and (iii) having a pair of thermionic cathodes spaced apart

by a distance no larger than three times the maximum transverse dimension of the threaded portion.

16. The arrangement of claim 13 yet further characterized in that the length of the maximum longitudinal dimension is equal to at least twice the length of thee maximum cross-sectional dimension.

17. The arrangement of claim 12 wherein the second part is further characterized by having a total duration that is distinctly shorter than half the total duration of the whole fundamental period.

* * * * *

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(12) **United States Patent**
**Nilssen**

(10) **Patent No.: US 6,172,464 B1**
(45) **Date of Patent: Jan. 9, 2001**

(54) **COMPACT SCREW-IN FLUORESCENT LAMP**

(76) Inventor: **Ole K. Nilssen**, Caesar Dr., Barrington, IL (US) 60010

( * ) Notice: Under 35 U.S.C. 154(b), the term of this patent shall be extended for 0 days.

(21) Appl. No.: **08/394,251**

(22) Filed: **Feb. 24, 1995**

**Related U.S. Application Data**

(63) Continuation-in-part of application No. 07/579,569, filed on Sep. 10, 1990, now abandoned, which is a continuation-in-part of application No. 06/787,692, filed on Oct. 15, 1985, now abandoned, which is a continuation of application No. 06/644,155, filed on Aug. 27, 1984, now abandoned, which is a continuation of application No. 06/555,426, filed on Nov. 23, 1983, now abandoned, which is a continuation of application No. 06/178,107, filed on Aug. 14, 1980, now abandoned.

(51) Int. Cl.[7] ..... H01J 13/46; H01J 17/34; H01J 19/78

(52) U.S. Cl. ..... 315/56; 315/71; 315/DIG. 7; 315/DIG. 4; 315/DIG. 5; 315/219; 315/224; 315/205

(58) Field of Search ..... 315/56, 71, 36, 315/DIG. 4, DIG. 5, DIG. 7, 307, 291, 219, 209 R, 224, 205

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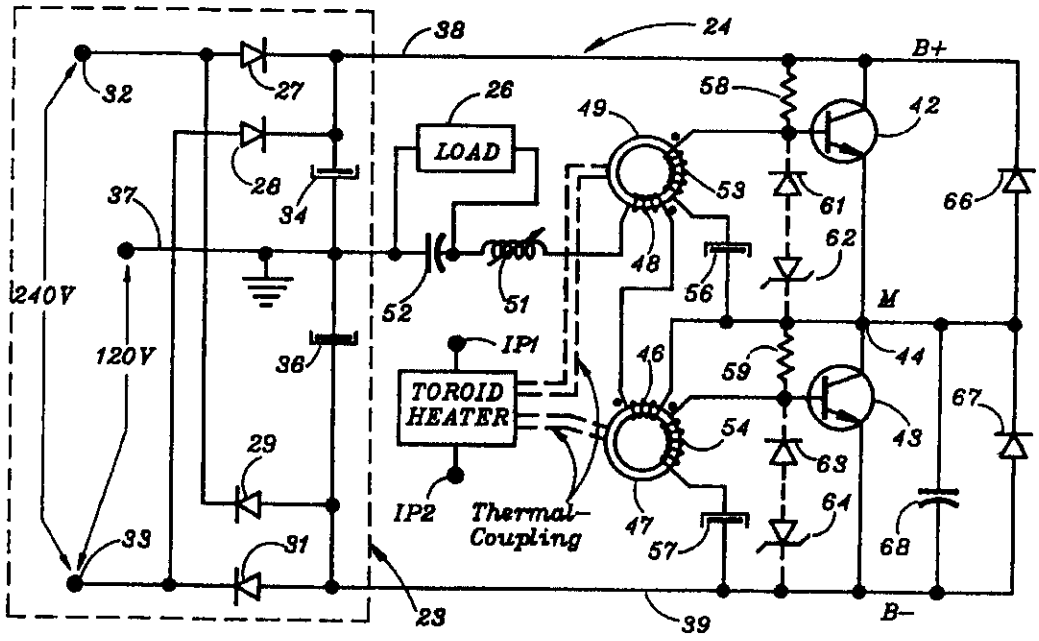
*Primary Examiner*—Michael B Shingleton

(57) **ABSTRACT**

In a high-frequency electronic ballast, a fluorescent lamp is connected with and powered by way of a series-resonant LC circuit. A resistive load is connected with the LC circuit, thereby to constitute a load therefor before ignition of the fluorescent lamp or in case the fluorescent lamp were to fail to ignite.

**6 Claims, 3 Drawing Sheets**



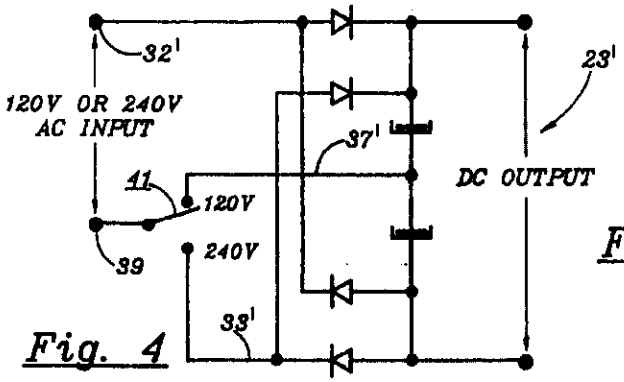



Fig. 4

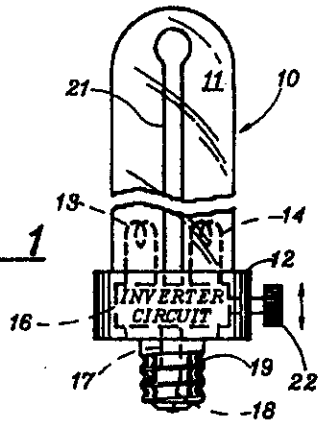



Fig. 1

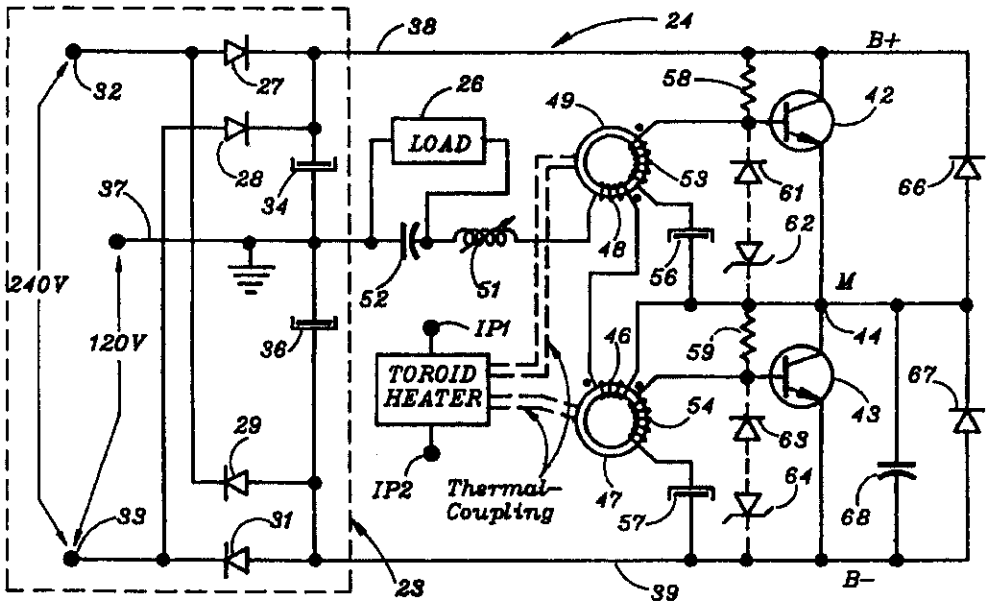



Fig. 2

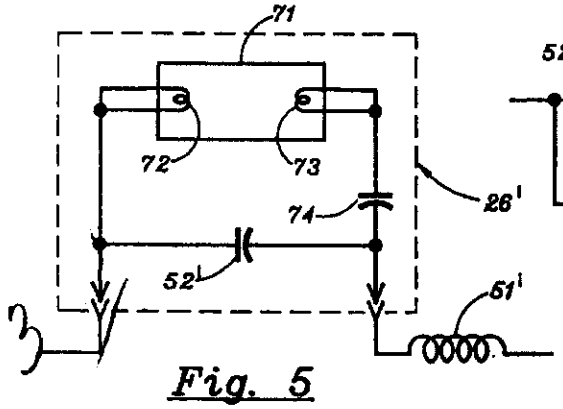



Fig. 5

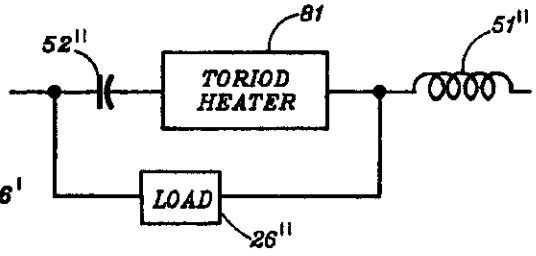



Fig. 6

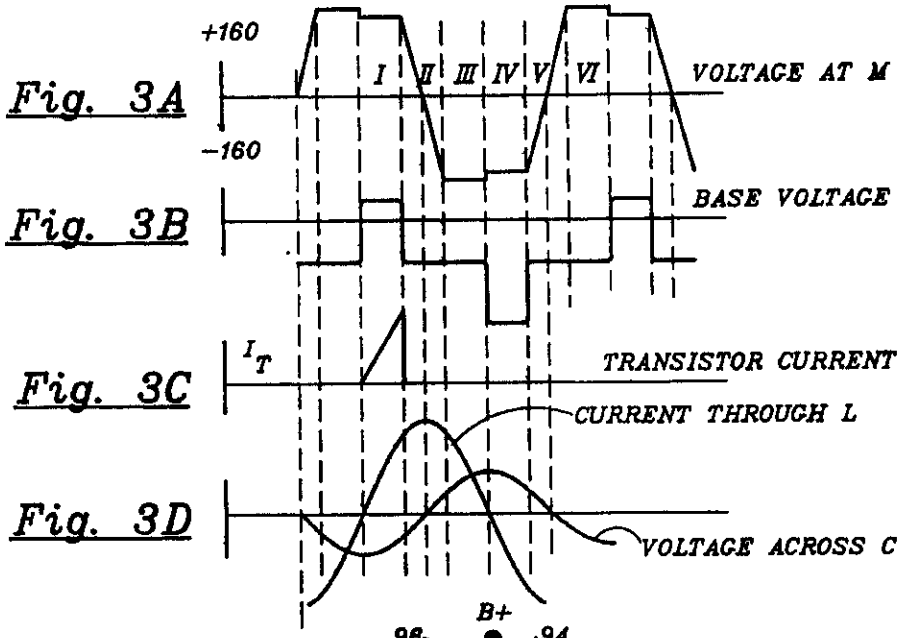



Fig. 3A

Fig. 3B

Fig. 3C

Fig. 3D

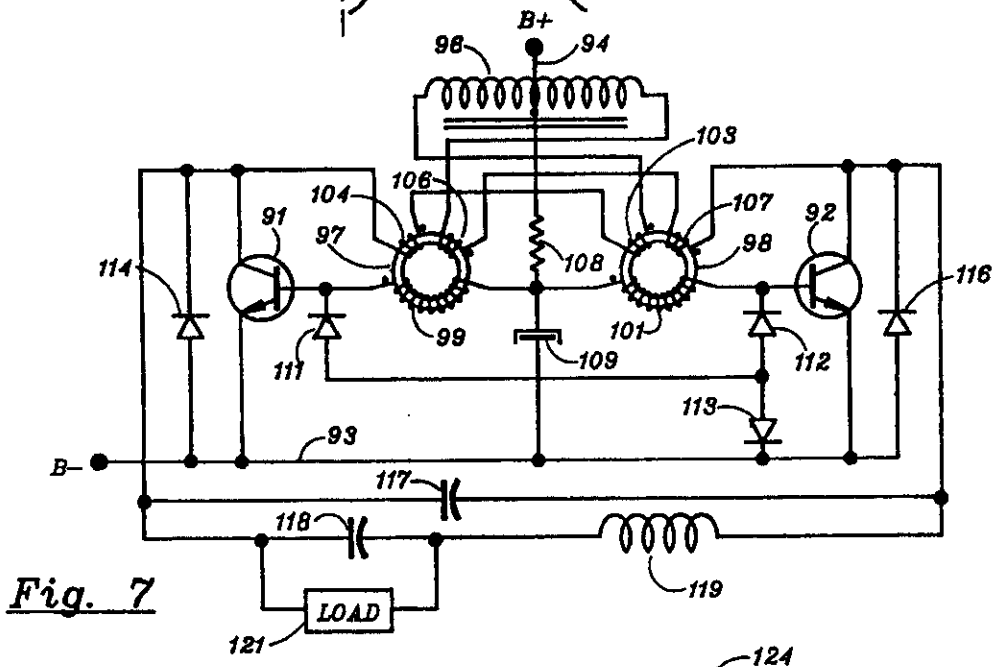



Fig. 7

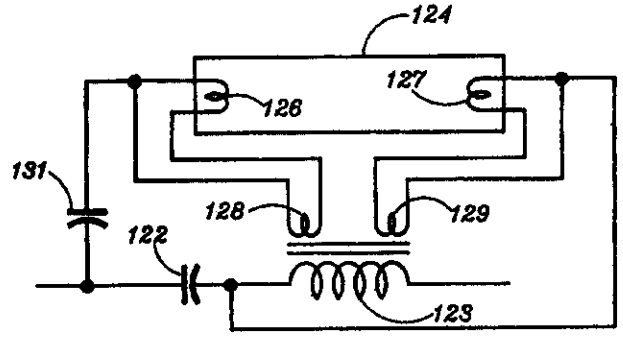



Fig. 8

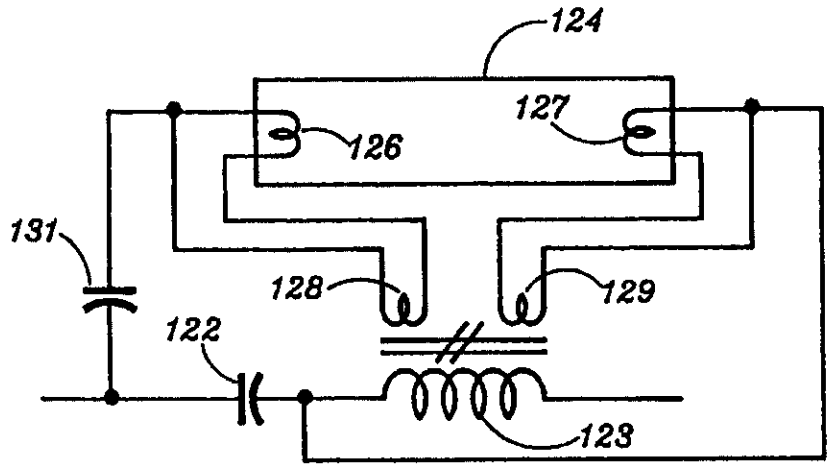

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Fig. 9

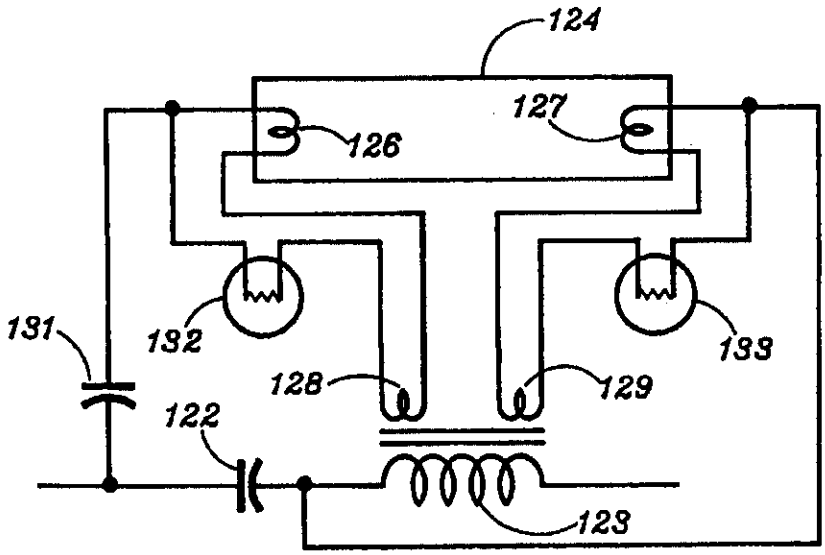
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Fig. 10

# COMPACT SCREW-IN FLUORESCENT LAMP

## RELATED APPLICATIONS

The present application is a Continuation-in-Part of Ser. No. 07/579,569 filed Sep. 10, 1990; which is a Continuation-in-Part of Ser. No. 06/787,692 filed Oct. 15, 1985; which is a Continuation of Ser. No. 06/644,155 filed Aug. 27, 1984, now abandoned; which was a Continuation of Ser. No. 06/555,426 filed Nov. 23, 1983, now abandoned; which was a Continuation of Ser. No. 06/178,107 filed Aug. 14, 1980, now abandoned.

## BACKGROUND OF THE INVENTION

1. Field of Invention

This invention relates to electronic ballasts for rapid-start fluorescent lamps, particularly where the lamps are powered via a series-resonant LC circuit.

2. Description of Prior Art

For a description of pertinent prior art, reference is made to U.S. Pat. No. 4,677,345 to Nilssen; which patent issued from a Division of application Ser. No. 06/178,107 filed Aug. 14, 1980; which application is the original progenitor of instant application.

Otherwise, reference is made to the following U.S. Pat. No. 3,263,122 to Genuit; U.S. Pat. No. 3,320,510 to Locklair; U.S. Pat. No. 3,996,493 to Davenport et el.; U.S. Pat. No. 4,100,476 to Ghiringhelli; U.S. Pat. No. 4,262,327 to Kovacik et al.; U.S. Pat. No. 4,370,600 to Zansky; U.S. Pat. No. 4,634,932 to Nilssen; and U.S. Pat. No. 4,857,806 to Nilssen.

## SUMMARY OF THE INVENTION

Objects of the Invention

Objects of the present invention are those of providing for cost-effective electronic ballasts as well as compact screw-in fluorescent lamps.

This as well as other objects, features and advantages of the present invention will become apparent from the following description and claims.

Brief Description

The present invention is directed to providing improved inverter circuits for powering and controlling gas discharge lamps. The inverter circuits according to the present invention are highly efficient, can be compactly constructed and are ideally suited for energizing gas discharge lamps, particularly "instant-start" and "self-ballasted" fluorescent lamps.

According to one form of the present invention, a series-connected combination of an inductor and a capacitor is provided in circuit with the inverter transistors to be energized upon periodic transistor conduction. Transistor drive current is preferably provided through the use of at least one saturable inductor to control the transistor inversion frequency to be equal to or greater than the nature resonant frequency of the inductor and capacitor combination. The high voltages efficiently developed by loading the inverter with the inductor and capacitor are ideally suited for energizing external loads such as gas discharge lamps. In such an application, the use of an adjustable inductor permits control of the inverter output as a means of adjusting the level of lamp illumination.

According to another important form of the present invention, reliable and highly efficient half-bridge inverters include a saturable inductor in a current feedback circuit to drive the transistors for alternate conduction. The inverters



also include a load having an inductance sufficient to effect periodic energy storage for self-sustained transistor inversion. Importantly, improved reliability is achieved because of the relatively low and transient-free voltages across the transistors in these half-bridge inverters.

Further, according to another feature of the present invention, novel and economical power supplies particularly useful with the disclosed inverter circuits convert conventional AC input voltages to DC for supplying to the inverters.

Yet further, according to still another feature of the invention, a rapid-start fluorescent lamp is powered by way of a series-resonant LC circuit; while heating power for the lamp's cathodes is provided via loosely-coupled auxiliary windings on the tank inductor of the LC circuit. Alternatively, cathode heating power is provided from tightly-coupled windings on the tank inductor; in which case output current-limiting is provided via a non-linear resistance means, such as an incandescent filament in a light bulb, connected in series with the output of each winding.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a front elevation of a folded fluorescent lamp unit adapted for screw-in insertion into a standard Edison incandescent socket;

FIG. 2 is a schematic diagram illustrating the essential features of a push-pull inverter circuit particularly suitable for energizing the lamp unit of FIG. 1;

FIGS. 3A–3D is a set of waveform diagrams of certain significant voltages and currents occurring in the circuit of FIG. 2;

FIG. 4 is a schematic diagram of a DC power supply connectable to both 120 and 240 volt AC inputs;

FIG. 5 is a schematic diagram which illustrates the connection of a non-self-ballasted gas discharge lamp unit to the FIG. 2 inverter circuit;

FIG. 6 is a schematic diagram which illustrates the use of a toroid heater for regulation of the inverter output;

FIG. 7 is an alternate form of push-pull inverter circuit accordind to the present invention;

FIG. 8 is a schematic diagram showing the connection of a gas discharge lamp of the "rapid-start" type to an inductor-capacitor-loaded inverter according to the present invention;

FIG. 9 is a modification of FIG. 8, showing loosely-coupled auxiliary windings on the tank inductor; and

FIG. 10 is another modification of FIG. 8, showing nonlinear current-limiting means connected with the output of tightly-coupled auxiliary windings on the tank inductor.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 illustrates a screw-in gas discharge lamp unit **10** comprising a folded fluorescent lamp **11** suitably secured to an integral base **12**. The lamp comprises two cathodes **13, 14** which are supplied with the requisite high operating voltage from a frequency-converting power supply and ballasting circuit **16**; which, because of its compact size, conveniently fits within the base **12**.

The inverter circuit **16** is connected by leads **17, 18** to a screw-type plug **19** adapted for screw-in insertion into a standard Edison-type incandescent lamp socket at which ordinary 120 Volt/60 Hz power line voltage is available. A ground plane comprising a wire or metallic strip **21** is disposed adjacent a portion of the fluorescent lamp **11** as a

starting aid. Finally, a manually rotatable external knob **22** is connected to a shaft for mechanical adjustment of the air gap of a ferrite core inductor to vary the inductance value thereof in order to effect adjustment of the inverter voltage output connected to electrodes **13, 14** for controlled variation of the lamp illumination intensity.

With reference to FIG. **2**, a power supply **23**, connected to a conventional AC input, provides a DC output for supplying a high-efficiency inverter circuit **24**. The inverter is operable to provide a high voltage to an external load **26**, which may comprise a gas discharge device such as the fluorescent lamp **11** of FIG. **1**.

The power supply **23** comprises bridge rectifier having four diodes **27, 28, 29** and **31** connectable to a 240 volt AC supply at terminals **32, 33**. Capacitors **34, 36** are connected between a ground line **37** (in turn directly connected to the inverter **24**) and to a B+ line **38** and a B− line **39**, respectively. The power supply **23** also comprises a voltage doubler and rectifier optionally connectable to a 120 volt AC input taken between the ground line **37** and terminal **33** or **32**. The voltage doubler and rectifier means provides a direct electrical connection by way of line **37** netween one of the 120 volt AC power input lines and the inverter **24**, as shown in FIG. **2**. The bridge rectifier and the voltage doubler and rectifier provide substantially the same DC output voltage to the inverter **24** whether the AC input is 120 or 240 volts. Typical voltages are +160 volts on the B+ line **38** and −160 volts on the B− line **39**.

With additional reference to FIG. **4**, which shows an alternate power supply **23'**, the AC input, whether 120 or 240 volts, is provided at terminals **32'** and **39**. Terminal **39** is in turn connected through a single-pole double-throw selector switch **41** to terminal **37'** (for 120 volt operation) or terminal **33'** (for 240 volt operation). In all other respects, power supplies **23** and **23'** are identical.

The inverter circuit **24** of FIG. **2** is a half-bridge inverter comprising transistors **42, 43** connected in series across the DC voltage output of the power supply **23** on B+ and B− lines **38** and **39**, respectively. The collector of trasistor **42** is connected to the B+ line **38**, the emitter of transistor **42** and the collector of transistor **43** are connected to a midpoint line **44** (designated "M") and the emitter of transistor **43** is connected to the B− line **39**. The midpoint line **44** is in turn connected to the ground line **37** through primary winding **46** of a toroidal saturable core transformer **47**, a primary winding **48** on an identical transformer **49**, an inductor **51** and a series-connected capacitor **52**. The inductor **51** and capacitor **52** are energized upon alternate transistor conduction in a manner to be described later.

An external load **26** is preferably taken off capacitor **52**, as shown in FIG. **2**. The inductor **51**, preferably a known ferrite core inductor, has an inductance variable by mechanical adjustment of the air gap in order to effect variation in the level of the inductor and capacitor voltage and hence the power available to the load, as will be described. When the load is a gas discharge lamp such as lamp **11** in FIG. **1**, variation in this inductance upon rotation of knob **22** accomplishes a lamp dimming effect.

Drive current to the base terminals of transistors **42** and **43** is provided by secondary windings **53, 54** of transformers **49, 47**, respectively. Winding **53** is also connected to midpoint lead **44** through a bias capacitor **56**, while winding **54** is connected to the B− lead **39** through an identical bias capacitor **57**. The base terminals of transistors **42** and **43** are also connected to lines **38** and **44** through bias resistors **58** and **59**, respectively. For a purpose to be described later, the base of transistor **42** can be optionally connected to a diode **61** and a series Zener diode **64** in turn connected to the midpoint line **44**; similarly, a diode **63** and series Zener diode **64** in turn connected to the B− line **39** can be connected to the base of transistor **43**. Shunt diodes **66** and **67** are connected across the collector-emitter terminals of transistors **42** and **43**, respectively. Finally, a capacitor **68** is connected across the collector-emitter terminals of transistor **43** to restrain the rate of voltage rise across those terminals, as will be seen presently.

The operation of the circuit of FIG. **2** can best be understood with additional reference to FIG. **3**, which illustrates significant portions of the waveforms of the voltage at midpoint M (FIG. 3A), the base-emitter voltage on transistor **42** (FIG. 3B), the current through transistor **42** (FIG. 3C), and the capacitor **52** voltage and the inductor **51** current (FIG. 3D).

Assuming that transistor **42** is first to be triggered into conduction, current flows from the B+ line **38** through windings **46** and **38** and the inductor **51** to charge capacitor **52** and returns through capacitor **34** (refer to the time period designated I in FIG. 3). When the saturable inductor **49** saturates at the end of period I, drive current to the base of transistor **42** will terminate, causing voltage on the base of the transistor to drop to the negative voltage stored on the bias capacitor **56** in a manner to be described, causing this transistor to become non-conductive. As shown in FIG. 3c, current-flow in transistor **43** terminates at the end of period I.

Because the current through inductor **51** cannot change instantaneously, current will flow from the B− bus **39** through capacitor **68**, causing the voltage at midpoint line **44** to drop to −160 volts (period II in FIG. 3). The capacitor **68** restrains the rate of voltage change across the collector and emitter terminals of transistor **42**. The current through the inductor **51** reaches its maximum value when the voltage at the midpoint line **44** is zero. During period III, the current will continue to flow through inductor **51** but will be supplied from the B− bus through the shunt diode **67**. It will be appreciated that during the latter half of period II and all of period III, positive current is being drawn from a negative voltage; which, in reality, means that energy is being returned to the power supply through a path of relatively low impedance.

When the inductor current reaches zero at the start of period IV, the current through the primary winding **46** of the saturable inductor **47** will cause a current to flow out of its secondary winding **54** to cause transistor **43** to become conductive, thereby causing a reversal in the direction of current through inductor **51** and capacitor **52**. When transformer **47** saturates at the end of period IV, the drive current to the base of transistor **43** terminates and the current through inductor **51** will be supplied through capacitor **68**, causing the voltage at midpoint line **44** to rise (period V). When the voltage at the midpoint line M reaches 160 volts, the current will then flow through shunt diode **66** (period VI). The cycle is then repeated.

As seen in FIG. **3**, saturable transformers **47, 49** provide transistor drive current only after the current through inductor **51** has diminished to zero. Further, the transistor drive current is terminated before the current through inductor **51** has reached its maximum amplitude. This coordination of base drive current and inductor current is achieved because of the series-connection between the inductor **51** and the primary windings **46, 48** of saturable transformers **47, 49**, respectively.

The series-connected combination of the inductor **51** and the capacitor **52** is energized upon the alternate conduction of transistors **42** and **43**. With a large value of capacitance of capacitor **52**, very little voltage will be developed across its terminals. As the value of this capacitance is decreased, however, the voltage across this capacitor will increase. As the value of the capacitor **52** is reduced to achieve resonance with the inductor **51**, the voltage on the capacitor will rise and become infinite in a loss-free circuit operating under ideal conditions.

It has been found desirable to regulate the transistor inversion frequency, determined mainly by the saturation time of the saturable inductors **47, 49**, to be equel to or higher than the natural resonance frequency of the inductor and capacitor combination in order to provide a high voltage output to external load **26**. A high voltage across capacitor **52** is efficiently developed as the transistor inversion frequency approaches the natural resonant frequency of the inductor **51** and capacitor **52** combination. Stated another way, the conduction period of each transistor is desirably shorter in duration than one quarter of the full period corresponding to the natural resonant frequency of the inductor and capacitor combination. When the inverter **24** is used with a self-ballasted gas discharge lamp unit, it has been found that the inversion frequency can be at least equal to the natural resonant frequency of the tank circuit. If the capacitance value of capacitor **52** is reduced still further beyond the resonance point, unacceptably high transistor currents will be experienced during transistor switching and transistor burn-out will occur.

It will be appreciated that the sizing of capacitor **52** is determined by the application of the inverter circuit **24**. Variation in the values of the capacitor **52** and the inductor **51** will determine the voltages developed in the inductor-capacitor tank circuit. The external load **26** may be connected in circuit with the inductor **51** (by a winding on the inductor, for example) and the capacitor may be omitted entirely. If the combined circuit loading of the inductor **51** and the external load **26** has an effective inductance of value sufficient to effect periodic energy storage for self-sustained transistor inversion, the current feedback provided by the saturable inductors **47,49** will effect alternate transistor conduction without the need for additional voltage feedback. When the capacitor **52** is omitted, the power supply **23** provides a direct electrical connection between one of the AC power input lines and the inverter load circuit.

Because the voltages across transistors **42, 43** are relatively low (due to the effect of capacitors **34, 36**), the half-bridge inverter **24** is very reliable. The absence of switching transients minimizes the possibility of transistor burn-out.

The inverter circuit **24** comprises means for supplying reverse bias to the conducting transistor upon saturation of its associated saturable inductor. For this purpose, the capacitors **56** and **57** are charged to negative voltages as a result of reset current flowing into secondary windings **53, 54** from the bases of transistors **42, 43**, respectively. This reverse current rapidly turns off a conducting transistor to increase its switching speed and to achieve inverter circuit efficiency in a manner described more fully in my co-pending U.S. patent application Ser. No. 103,624 filed Dec. 14, 1979 and entitled "Bias Control for High Efficiency Inverter Circuit" (now U.S. Pat. No. 4,307,353). The more negative the voltage on the bias capacitors **56** and **57**, the more rapidly charges are swept out of the bases of their associated transistors upon transistor turn-off.

When a transistor base-emitter junction is reversely biased, it exhibits the characteristics of a Zener diode having a reverse breakdown voltage on the order of 8 to 14 Volt for transistors typically used in high-voltage inverters. As an alternative, to provide a negative voltage smaller in magnitude on the base lead of typical transistor **42** during reset operation, the optional diode **61** and Zener diode **62** combination can be used. For large values of the bias capacitor **56**, the base voltage will be substantially constant.

If the load **26** comprises a gas discharge lamp, the voltage across the capacitor **52** will be reduced once the lamp is ignited to prevent voltages on the inductor **51** and the capacitor **52** from reaching destructive levels. Such a lamp provides an initial time delay during which a high voltage, suitable for instant starting, is available.

FIG. **5** illustrates the use of an alternate load **26'** adapted for plug-in connection to an inverter circuit such as shown in FIG. **2**. The load **26'** consists of a gas discharge lamp **71** having electrodes **72, 73** and connected in series with a capacitor **74**. The combination of lamp **71** and capacitor **74** is connected in parallel with a capacitor **52'** which serves the same purpose as capacitor **52** in the FIG. **2** circuit. However, when the load **26'** is unplugged from the circuit, the inverter stops oscillating and the development of high voltages in the inverter is prevented. The fact that no high voltages are generated by the circuit if the lamp is disconnected while the circuit is oscillating is important for safety reasons.

FIG. **6** illustrates a capacitor **52"** connected in series with an inductor **51"** through a heater **81** suitable for heating the toroidal inductors **47, 49** in accordance with the level of output. The load **26"** is connected across the series combination of the capacitor **52"** and the toroid heater. The heater **81** is preferably designed to controllably heat the toroidal saturable inductors in order to decrease their saturation flux limit and hence their saturation time. The result is to decrease the periodic transistor conduction time and thereby increase the transistor inversion frequency. When a frequency-dependent impedance means, that is, an inductor or a capacitor, is connected in circuit with the AC voltage output of the inverter, change in the transistor inversion frequency will modify the impedance of the frequency-dependent impdance means and correspondingly modify the inverter output. Thus as the level of the output increases, the toroid heater **81** is correspondingly energized to effect feedback regulation of the output. Further, transistors **42, 43** of the type used in high voltage inverters dissipate heat during periodic transistor conduction. As an alternative, the toroid heater **81** can use this heat for feedback regulation of the output or control of the temperature of transistors **42, 43**.

The frequency dependent impedance means may also be used in a circuit to energize a gas discharge lamp at adjustable illumination levels. Adjustment in the inversion frequency of transistors **42, 43** results in control of the magnitude of the AC current supplied to the lamp. This is preferably accomplished where saturable inductors **47, 49** have adjustable flux densities for control of their saturation time.

FIG. **7** schematically illustrates an alternate form of inverter circuit, shown without the AC to DC power supply connections for simplification. In this Figure, the transistors are connected in parallel rather than in series but the operation is essentially the same as previously described.

In particular, this circuit comprises a pair of alternately conducting transistors **91, 92**. The emitter terminals of the transistors are connected to a B– line **93**. A B+ lead **94** is connected to the center-tap of a transformer **96**. In order to provide drive current to the transistors **91, 92** for control of their conduction frequency, saturable inductors **97, 98** have

secondary windings **99, 101**, respectively, each secondary winding having one end connected to the base of its associated transistor; the other ends are connected to a common terminal **102**. One end of transformer **96** is connected to the collector of transistor **91** through a winding **103** on inductor **98** in turn connected in series with a winding **104** on inductor **97**. Likewise, the other end of transformer **96** is connected to the collector of transistor **92** through a winding **106** on inductor **97** in series with another winding **107** on inductor **98**.

The B+ terminal is connected to terminal **102** through a bias resistor **108**. A bias capacitor **109** connects terminal **102** to the B− lead **93**. This resistor and capacitor serve the same function as resistors **58, 59** and capacitors **56, 57** in the FIG. **2** circuit.

The bases of transistors **91, 92** are connected by diodes **111, 112**, respectively, to a common Zener diode **113** in turn connected to the B− lead **93**. The common Zener diode **113** serves the same function as individual Zener diodes **62, 64** in FIG. **2**.

Shunt diodes **114, 116** are connected across the collector-emitter terminals of transistors **91, 92**, respectively. A capacitor **117** connecting the collectors of transistors **91, 92** restrains the rate of voltage rise on the collectors in a manner similar to the collector-emitter capacitor **68** in FIG. **2**.

Inductive-capacitive loading of the FIG. **7** inverter is accomplished by a capacitor **118** connected in series with with an inductor **119**, the combination being connected across the collectors of the transistors **91, 92**. A load **121** is connected across the capacitor **118**.

FIG. **8** illustrates how an inverter loaded with a series capacitor **122** and inductor **123** can be used to energize a "rapid-start" fluorescent lamp **124** (the details of the inverter circuit being omitted for simplication). The lamp **124** has a pair of cathodes **126, 127** connected across the capacitor **122** for supply of operating voltage in a manner identical to that previously described. In addition, the inductor **123** comprises a pair of magnetically-coupled auxiliary windings **128, 129** for electrically heating the cathodes **126, 127**, respectively. A small capacitor **131** is connected in series with lamp **124**.

FIG. **9** illustrates the very same circuit arrangement as that of FIG. **8** except that the auxiliary windings **128, 129** are only loosely coupled to the inductor **123**, thereby providing for a manifest limitation on the amount of current that can be drawn from each auxiliary winding in case it were to be accidentally short-circuited.

FIG. **10** also illustrates the very same circuit arrangement as that of FIG. **8** except that the cathodes **126, 127** are connected with their respective auxiliary windings **128, 129** by way of nonlinear current-limiting means **132** and **133**, respectively.

In FIG. **10**, the non-linear current-limiting means **132, 133** are shown as being two (small) incandescent lamps. However, other types of non-linear resistance means could be used as well.

Both the FIG. **9** circuit and the FIG. **10** circuit serve the same basic purpose; which is that of preventing damage to the ballast circuit (such as that if FIG. **2**) in case the leads used for connecting to one of the lamp cathodes **126, 127** were to be accidentally shorted. This damage prevention is accomplished by providing for manifest limitation of the maximum amount of current that can be drawn from each one of the auxiliary windings **128, 129**. In the circuit of FIG. **9**, this manifest limitation is accomplished by having the auxiliary windings **128, 129** couple sufficiently loosely to the main inductor **123**—such as by providing a magnetic shunt between inductor **123** and the auxiliary windings—thereby correspondingly limiting the degree of impact resulting from an accidental short circuit. Such a short circuit would result in a net reduction in the effective inductance value of the tank inductor **123**; which net reduction in inductance may in turn cause a precipitous increase in the magnitude of the reactive current drawn from the inverter by the series-connected inductor **123** and capacitor **122**, thereby causing damage to the inverter.

Additional Explanations and Comments

(a) With reference to FIGS. **2** and **5**, adjustment of the amount of power supplied to load **26'**, and thereby the amount of light provided by lamp **71**, may be accomplished by applying a voltage of adjustable magnitude to input terminals IP1 and IP2 of the Toroid Heater; which is thermally coupled with the toroidal ferrite cores of saturable transformers **47, 49**.

(b) With commonly available components, inverter circuit **24** of FIG. **2** can be made to operate efficiently at any frequency between a few kHz to perhaps as high as 50 kHz. However, for various well-known reasons (i.e., eliminating audible noise, minimizing physical size, and maximizing efficiency), the frequency actually chosen is in the range of 20 to 40 kHz.

(c) The fluorescent lighting unit of FIG. **1** could be made in such manner as to permit fluorescent lamp **11** to be disconnectable from its base **12** and ballasting means **16**. However, if powered with normal line voltage without its lamp load connected, frequency-converting power supply and ballasting circuit **16** is apt to self-destruct.

To avoid such self-destruction, arrangements can readily be made whereby the very act of removing the load automatically establishes a situation that prevents the possible destruction of the power supply and ballasting means. For instance, with the tank capacitor (**52**) being permanently connected with the lamp load (**11**)—thereby automatically being removed whenever the lamp is removed—the inverter circuit is protected from self-destruction.

(d) At frequencies above a few kHz, the load represented by a fluorescent lamp—once it is ignited—is substantially resistive. Thus, with the voltage across lamp **11** being of a substantially sinusoidal waveform (as indicated in FIG. **3***d*), the current through the lamp will also be substantially sinusoidal in waveshape.

(e) In the fluorescent lamp unit of FIG. **1**, fluorescent lamp **11** is connected with power supply and ballasting circuit **16** in the exact same manner as is load **26** connected with the circuit of FIG. **2**. That is, it is connected in parallel with the tank capacitor (**52**) of the L-C series-resonant circuit. As is conventional in instant-start fluorescent lamps—such as lamp **11** of FIG. **1**—the two terminals from each cathode are shorted together, thereby to constitute a situation where each cathode effectively is represented by only a single terminal. However, it is not necessary that the two terminals from each cathode be shorted together; in which case—for instant-start operation—connection from a lamp's power supply and ballasting means need only be made with one of the terminals of each cathode.

(f) with respect to the circuit arrangement of FIG. **9**, in situations where the tank inductor **123** includes a ferrite magnetic core having an air gap, one particularly cost-effective way of accomplishing the indicated loose coupling between the tank inductor **123** and the auxiliary windings **128, 129** is that of arranging for the auxiliary windings to be placed in the air gap in such a manner that they each couple only with part of the magnetic flux crossing the air gap.

(g) in FIG. 1, the compact screw-in fluorescent lamp has a longitudinal central axis penetrating through the center of the bottom of base 19 (i.e., at the point where lead 18 is connected), passing up centrally between the two legs of lamp 11, and emerging at the center of the very top of lamp 11.

(h) In FIG. 1, as a skilled artisan would perceive by direct inspection, the visible parts are drawn to scale. Thus, for instance:

(i) the height and width (i.e., diameter) of screw-base 19 are in proper proportion to those of an actual screw-base on an ordinary household incandescent lamp;

(ii) the diameter of the individual straight legs of the folded fluorescent lamp 11 are shown in proportion to the diameter of the screw-base;

(iii) the diameter of the bent portion connecting the top parts of the two straight lamp legs is shown in proper proportion to the diameter of the lamp legs; and

(iv) the distance between the two straight lamp legs is shown in proper proportion to the diameter of those lamp legs.

Of course, for a screw-in fluorescent lamp to have maximum utility, it is imperative that it has dimensions sufficiently compact to permit it to be conveniently used in most places where an incandescent lamp would ordinarily be used. Thus, it is important that its maximum diameter not be any larger than those of an ordinary household incandescent lamp (whose maximum diameter is typically about twice that of its screw-base). The screw-in fluorescent lamp depicted in FIG. 1 clearly satisfies those requirements.

What is claimed is:

1. An arrangement comprising:

a screw-base inserted into and held by a lamp socket adapted to accept and hold an ordinary household incandescent light bulb; the screw-base having base terminals and being otherwise characterized by having a central screw-base axis around which the outer boundary of the screw-base forms an approximately cylindrical surface; the lamp socket having socket terminals at which is provided AC power line voltage such as that normally provided from an ordinary electric utility power line;

a fluorescent lamp having lamp terminals; the fluorescent lamp being characterized by including at least two straight cylindrical light-emitting glass-enclosed sections disposed parallel to each other as well as to a central lamp axis; a lamp terminal being disposed at one end of each of the two straight cylindrical light-emitting glass-enclosed sections; the other ends of the two straight cylindrical light-emitting glass-enclosed sections being connected together via a transversely disposed light-emitting glass-enclosed section; said transversely disposed section being of a maximum dimension substantially no longer than just sufficient to reach between said other ends;

electronic sub-assembly having power input terminals connected with the base terminals and power output terminals connected with the lamp terminals; the sub-assembly being operative, whenever supplied with AC power line voltage at its power input terminals, to supply an alternating lamp current to the lamp terminals; the alternating lamp current being of frequency distinctly higher than that of the AC power line voltage; the sub-assembly being additionally characterized by not including a transformer having a primary winding connected across the power input terminals; the electronic sub-assembly being further characterized by including two terminals across which exists a DC voltage having a substantially constant absolute magnitude that is distinctly higher than the peak absolute magnitude of the AC power line voltage; and

structure means operative to hold together the screw-base, the fluorescent lamp, and the electronic sub-assembly, thereby to form an integral screw-in lamp structure characterized by having an overall longitudinal axis parallel with the central screw-base axis as well as with the central lamp axis.

2. An arrangement comprising:

a screw-base inserted into and held by a lamp socket adapted to accept and hold an ordinary household incandescent light bulb; the screw-base having base terminals and being otherwise characterized by having a central screw-base axis around which the outer boundary of the screw-base forms an approximately cylindrical surface; the lamp socket having socket terminals at which is provided AC power line voltage such as that normally provided from an ordinary electric utility power line;

a fluorescent lamp having lamp terminals; the fluorescent lamp being characterized by including at least two straight cylindrical light-emitting glass-enclosed sections disposed parallel to each other as well as to a central lamp axis; a lamp terminal being disposed at one end of each of the two straight cylindrical light-emitting glass-enclosed sections; the other ends of the two straight cylindrical light-emitting glass-enclosed sections being connected together via a transversely disposed light-emitting glass-enclosed section; said transversely disposed section being of a maximum dimension substantially no longer than just sufficient to reach between said other ends;

electronic sub-assembly having power input terminals connected with the base terminals and power output terminals connected with the lamp terminals; the sub-assembly being operative, whenever supplied with AC power line voltage at its power input terminals, to supply an alternating lamp current to the lamp terminals; the alternating lamp current being of frequency distinctly higher than that of the AC power line voltage; the sub-assembly being additionally characterized by not including a transformer having a primary winding connected across the power input terminals; the electronic sub-assembly being further characterized by including a pair of terminals across which exists a DC voltage and between which are series-connected two transistors; the transistors being characterized by alternatingly conducting current; at least one of the transistors conducting current in the form of periodic unidirectional current pulses; the periodic unidirectional current pulses occurring at a frequency equal to that of the alternating lamp current; each individual unidirectional current pulse having a duration distinctly shorter than half of a complete period of the alternating lamp current; and

structure means operative to hold together the screw-base, the fluorescent lamp, and the electronic sub-assembly, thereby to form an integral screw-in lamp structure characterized by having an overall longitudinal axis parallel with the central screw-base axis as well as with the central lamp axis.

3. A structure characterized by having a central axis about which the following elements are assembled:

a screw-base operative to screw into a lamp socket of a type usually used for receiving and holding an ordinary household incandescent light bulb; the screw-base being otherwise characterized by having base terminals and by being disposed symmetrically about the central axis;

a fluorescent lamp having lamp terminals and plural cylindrical lamp segments disposed apart from, but parallel to, each other as well as to the central axis; each of the plural cylindrical lamp segments having a total length; the fluorescent lamp being further characterized in that a flat plane disposed perpendicular to the central axis and intersecting one of the cylindrical lamp segments anywhere along its total length creates a cross-sectional pattern that (i) is symmetrical with respect to a flat plane disposed parallel to the central axis, and (ii) includes nothing but cross-sections of substantially identical cylindrical lamp segments;

an electronic sub-assembly having input terminals and output terminals; the input terminals being connected with the base terminals; the output terminals being connected with the lamp terminals; the electronic sub-assembly being operative to supply an alternating voltage at its output terminals provided it be supplied with an AC power line voltage at its input terminals; the frequency of the alternating voltage being distinctly higher than that of the AC power line voltage; the electronic subassembly being additionally characterized by including a transistor through which flows unidirectional current pulses at a periodic rate equal to that of the alternating voltage; each current pulse having a duration distinctly shorter than half of the complete cycle of the alternating voltage; and

housing means mounted rigidly on the screw-base and operative to house the electronic sub-assembly as well as to hold and support the fluorescent lamp, thereby to form a fluorescent lamp entity adapted to be screwed into and powered from a lamp socket at which ordinary AC power line voltage is provided.

4. A structure characterized by having a central axis about which the following elements are assembled:

a screw-base operative to screw into a lamp socket of a type usually used for receiving and holding an ordinary household incandescent light bulb; the screw-base being otherwise characterized by having base terminals and by being disposed symmetrically about the central axis;

a fluorescent lamp having lamp terminals and plural cylindrical lamp segments disposed apart from, but parallel to, each other as well as to the central axis; each of the plural cylindrical lamp segments having a total length; the fluorescent lamp being further characterized in that a flat plane disposed perpendicular to the central axis and intersecting one of the cylindrical lamp segments anywhere along its total length creates a cross-sectional pattern that (i) is symmetrical with respect to a flat plane disposed parallel to the central axis, and (ii) includes nothing but cross-sections of substantially identical cylindrical lamp segments;

an electronic sub-assembly having input terminals and output terminals; the input terminals being connected with the base terminals; the output terminals being connected with the lamp terminals; the electronic sub-assembly being operative to supply an alternating voltage at its output terminals provided it be supplied with an AC power line voltage at its input terminals; the frequency of the alternating voltage being distinctly higher than that of the AC power line voltage; the electronic subassembly being additionally characterized by including a pair of terminals across which exists a DC voltage having a substantially constant absolute magnitude that is distinctly larger than the absolute peak magnitude of the AC power line voltage; and

housing means mounted rigidly on the screw-base and operative to house the electronic sub-assembly as well as to hold and support the fluorescent lamp, thereby to form a fluorescent lamp entity adapted to be screwed into and powered from a lamp socket at which ordinary AC power line voltage is provided.

5. A structure characterized by having a central axis about which the following elements are assembled:

a screw-base operative to screw into a lamp socket of a type usually used for receiving and holding an ordinary household incandescent light bulb; the screw-base being otherwise characterized by having base terminals and by being disposed symmetrically about the central axis;

a fluorescent lamp having lamp terminals and plural cylindrical lamp segments disposed apart from, but parallel to, each other as well as to the central axis; each of the plural cylindrical lamp segments having a total length; the fluorescent lamp being further characterized in that a flat plane disposed perpendicular to the central axis and intersecting one of the cylindrical lamp segments anywhere along its total length creates a cross-sectional pattern that (i) is symmetrical with respect to a flat plane disposed parallel to the central axis, and (ii) includes nothing but cross-sections of substantially identical cylindrical lamp segments;

an electronic sub-assembly having input terminals and output terminals; the input terminals being connected with the base terminals; the output terminals being connected with the lamp terminals; the electronic sub-assembly being operative to supply an alternating voltage at its output terminals provided it be supplied with an AC power line voltage at its input terminals; the frequency of the alternating voltage being distinctly higher than that of the AC power line voltage; the electronic subassembly being additionally characterized by including a pair of terminals across which (i) exists a DC voltage, and (ii) are series-connected two filter capacitors; and

housing means mounted rigidly on the screw-base and operative to house the electronic sub-assembly as well as to hold and support the fluorescent lamp, thereby to form a fluorescent lamp entity adapted to be screwed into and powered from a lamp socket at which ordinary AC power line voltage is provided.

6. A structure characterized by having a central axis about which the following elements are assembled:

a screw-base operative to screw into a lamp socket of a type usually used for receiving and holding an ordinary household incandescent light bulb; the screw-base being otherwise characterized by having base terminals and by being disposed symmetrically about the central axis;

a fluorescent lamp having lamp terminals and plural cylindrical lamp segments disposed apart from, but parallel to, each other as well as to the central axis; each of the plural cylindrical lamp segments having a total length; the fluorescent lamp being further characterized

in that a flat plane disposed perpendicular to the central axis and intersecting one of the cylindrical lamp segments anywhere along its total length creates a cross-sectional pattern that (i) is symmetrical with respect to a flat plane disposed parallel to the central axis, and (ii) includes nothing but cross-sections of substantially identical cylindrical lamp segments;

an electronic sub-assembly having input terminals and output terminals; the input terminals being connected with the base terminals; the output terminals being connected with the lamp terminals; the electronic sub-assembly being operative to supply an alternating voltage at its output terminals provided it be supplied with an AC power line voltage at its input terminals; the frequency of the alternating voltage being distinctly higher than that of the AC power line voltage; the electronic subassembly being additionally characterized by including a voltage-doubling rectifier assembly connected with the base terminals as well as with a pair of DC terminals across which exists a DC voltage of substantially constant magnitude; which substantially constant magnitude is distinctly higher than the peak absoltr magnitude of the AC power line voltage; and

housing means mounted rigidly on the screw-base and operative to house the electronic sub-assembly as well as to hold and support the fluorescent lamp, thereby to form a fluorescent lamp entity adapted to be screwed into and powered from a lamp socket at which ordinary AC power line voltage is provided.

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