ROBERT J. YORIO (SBN 93178)
JASON T. ANDERSON (SBN 212938)
CARR & FERRELL LLP
2225 East Bayshore Road, Suite 200
PALO ALTO CA 94303
Telephone: (650) 812-3400
Facsimile: (650) 812-3444

Attorneys for Plaintiff
ACTICON TECHNOLOGIES LLC

UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

ACTICON TECHNOLOGIES LLC Plaintiff, v. SHINING TECHNOLOGY, INC.; DYNA MICRO, INC. d/b/a ADDONICS TECHNOLOGIES; ICHIKAWA MITSURU CORPORATION; WISE ADVANCED, CO. LTD.; and FORTUNA POWER SYSTEMS LTD. Defendants.	CASE NO. **COMPLAINT FOR PATENT INFRINGEMENT** JURY TRIAL DEMANDED

I. INTRODUCTION

1. Plaintiff ACTICON TECHNOLOGIES LLC (hereinafter "ACTICON") is the owner of U.S. Patent Nos. 4,972,470 ("the '470 patent"), 4,686,506 ("the '506 patent") and 4,603,320 ("the '320 patent"), which describe various forms of electronic connectors used to connect computers to external devices such as portable hard disk drives, CD-ROM drives, and video terminals. Defendants SHINING TECHNOLOGY, INC., DYNA MICRO, INC. d/b/a

ADDONICS TECHNOLOGIES, ICHIKAWA MITSURU CORPORATION, WISE ADVANCED CO., LTD and FORTUNA POWER SYSTEMS, LTD (collectively, "DEFENDANTS") are manufacturers and/or distributors which make, import, offer for sale, sell and/or distribute various electronic connectors which embody the '320 patent, the '506 patent, and/or the '470 patent. DEFENDANTS are, therefore, infringing the '320 patent, the '506 patent, and/or the '470 patent. ACTICON demands a jury trial and complains against DEFENDANTS as follows:

II. JURISDICTION

2. This is a patent infringement action arising under the United States Patent Act (35 U.S.C. § 271 *et seq.*). This Court has subject matter jurisdiction pursuant to 28 U.S.C. sections 1331 and 1338(a).

3. Plaintiff is informed and believes, and on that basis alleges, that DEFENDANTS are subject to personal jurisdiction in this District, because DEFENDANTS have caused tortious injury in this District by acts both inside and outside the District, and regularly solicit business in this District or derive substantial revenue for sales of goods, including infringing goods in this District, or otherwise have engaged in a persistent course of conduct in this District.

III. VENUE

4. Venue is proper in this District pursuant to 28 U.S.C. § 1391 because the allegedly infringing activities of DEFENDANTS took place in this judicial district.

IV. INTRA-DISTRICT ASSIGNMENT

5. For the purposes of Civil L.R. 3-2(c) and (d), this action arises in the Oakland Division, in that a substantial part of the events and omissions which gave rise to the claims occurred in the County of Alameda.

V. PARTIES

6. Plaintiff ACTICON is a limited liability corporation which has its principal place of business in Suffern, NY.

7. Defendant SHINING TECHNOLOGY, INC. ("Shining") is a California corporation, which has its principal place of business in Cypress, California. Plaintiff is informed and believes, and on that basis alleges, that Shining designs, manufactures, markets, sells and/or imports electronic connectors that specifically target the laptop, portable and desktop computing market.

8. Defendant DYNA MICRO, INC., doing business as ADDONICS TECHNOLOGIES, INC. is a California corporation, which has its principal place of business in Fremont, California. Plaintiff is informed and believes, and on that basis alleges, that DYNA MICRO, INC. designs, manufactures, markets, sells and/or imports electronic connectors that specifically target the laptop, portable and desktop computing market.

9. ACTICON is informed and believes, and on that basis alleges, that Defendant ICHIKAWA MITSURU CORPORATION ("IMC") is a Japanese corporation, which has its principal place of business in Tokyo, Japan. ACTICON is informed and believes, and on that basis alleges, that IMC designs, manufactures, markets, sells and/or imports electronic connectors that specifically target the laptop, portable and desktop computing market.

10. ACTICON is informed and believes, and on that basis alleges, that Defendant WISE ADVANCED, CO. LTD. ("WISE") is a Taiwanese corporation. ACTICON is informed and believes, and on that basis alleges, that WISE designs, manufactures, markets, sells and/or imports electronic connectors that specifically target the laptop, portable and desktop computing market.

11. ACTICON is informed and believes, and on that basis alleges, that Defendant FORTUNA POWER SYSTEMS LTD. ("FORTUNA") is a United Kingdom corporation, which has its principal place of business in Hampshire, England. ACTICON is informed and believes, and on that basis alleges, that FORTUNA designs, manufactures, markets, sells and/or imports electronic connectors that specifically target the laptop, portable and desktop computing market.

VI. GENERAL ALLEGATIONS

12. ACTICON is the sole and exclusive owner of United States Patent No. 4,603,320, issued on July 29, 1986, entitled "Connector Interface". A copy of the '320 patent is attached hereto as Exhibit 'A'

13. ACTICON is the sole and exclusive owner of United States Patent No. 4,686,506, issued on August 11, 1987, entitled "Multiple Connector Interface". A copy of the '506 patent is attached hereto as Exhibit 'B'.

14. ACTICON is the sole and exclusive owner of United States Patent No 4,972,470, issued on November 20, 1990 entitled "Programmable Connector." A copy of the '470 patent is attached hereto as Exhibit 'C'.

15. The'320, '506, and '470 patented inventions describe various electronic connectors that convert signals between a computer and certain external devices in order to obtain a desired connecting configuration and/or function.

16. ACTICON is informed and believes, and on that basis alleges, that DEFENDANTS make, use, import, offer for sale and/or sell certain products in the United States which infringe upon the '320 Patent, the '506 Patent, and/or the '470 Patent, including but not limited to the following products: (1) ScardSI PCMCIA Storage; (2) CitiDISK/CitiROM; (3) SparCSI Parallel Port Storage; (4) CitiVIEW – PCMCIA/CitiVIEW Scan Converter; and (5)

USB Converter (collectively, "the Accused Products"). Each of these products employ a electronic connector that connects a computer and one or more external devices, whereby such electronic connector converts signals between the computer and external devices in order to obtain a desired connecting configuration and/or function.

COUNT I

(Patent Infringement – U.S. Patent No. 4,603,320)

17. ACTICON repeats and realleges each of the allegations set forth in paragraphs 1 through 16 as though fully set forth herein.

18. ACTICON is informed and believes, and on that basis alleges, that DEFENDANTS make, use, import, offer for sale and/or sell the Accused Products, and possibly other products that infringe the '320 patent, and will continue to do so unless enjoined by this Court.

19. DEFENDANTS' conduct in making, using, importing, offering for sale and/or selling the Accused Products, and possibly other infringing products, constitutes an infringement of ACTICON'S rights under the '320 patent.

20. ACTICON is informed and believes, and on that basis alleges, that DEFENDANTS are actively inducing themselves and others to infringe, and/or committing acts of contributory infringement of one or more claims of the '320 patent, through their activities related to making, using, importing, offering for sale and/or selling the Accused Products, all in violation of 35 U.S.C. § 271.

21. ACTICON has been damaged by the DEFENDANTS' infringing conduct, in an amount not presently ascertainable. Moreover, such conduct is likely to cause substantial harm to ACTICON, unless this Court enjoins the infringing conduct.

22. ACTICON is informed and believes, and on that basis alleges, that DEFENDANTS' infringement of the '320 patent has been, and continues to be, willful and deliberate.

WHEREFORE, ACTICON seeks relief as set out in the Prayer.

COUNT II

(Patent Infringement – U.S. Patent No. 4,686,506)

23. ACTICON repeats and realleges each of the allegations set forth in paragraphs 1 through 16 as though fully set forth herein.

24. ACTICON is informed and believes, and on that basis alleges, that DEFENDANTS make, use, import, offer for sale and/or sell the Accused Products, and possibly other products that infringe the '506 patent, and will continue to do so unless enjoined by this Court.

25. DEFENDANTS' conduct in making, using, importing, offering for sale and/or selling the Accused Products, and possibly other infringing products, constitutes an infringement of ACTICON'S rights under the '506 patent.

26. ACTICON is informed and believes, and on that basis alleges, that DEFENDANTS are actively inducing themselves and others to infringe, and/or committing acts of contributory infringement of one or more claims of the '506 patent, through their activities related to making, using, importing, offering for sale and/or selling the Accused Products, all in violation of 35 U.S.C. § 271.

27. ACTICON has been damaged by the DEFENDANTS' infringing conduct, in an amount not presently ascertainable. Moreover, such conduct is likely to cause substantial harm to ACTICON, unless this Court enjoins the infringing conduct.

28. ACTICON is informed and believes, and on that basis alleges, that DEFENDANTS' infringement of the '506 patent has been, and continues to be, willful and deliberate.

WHEREFORE, ACTICON seeks relief as set out in the Prayer.

COUNT III

(Patent Infringement – U.S. Patent No. 4,972,470)

29. ACTICON repeats and realleges each of the allegations set forth in paragraphs 1 through 16 as though fully set forth herein.

30. ACTICON is informed and believes, and on that basis alleges, that DEFENDANTS make, use, import, offer for sale and/or sell the Accused Products, and possibly other products that infringe the '470 patent, and will continue to do so unless enjoined by this Court.

31. DEFENDANTS' conduct in making, using, importing, offering for sale and/or selling the Accused Products and possibly other infringing products constitutes an infringement of ACTICON'S rights under the '470 patent.

32. ACTICON is informed and believes, and on that basis alleges, that DEFENDANTS are actively inducing themselves and others to infringe, and/or committing acts of contributory infringement of one or more claims of the '470 patent, through their activities related to making, using, importing, offering for sale and/or selling the Accused Products, all in violation of 35 U.S.C. § 271.

33. ACTICON has been damaged by the DEFENDANTS' infringing conduct, in an amount not presently ascertainable. Moreover, such conduct is likely to cause substantial harm to ACTICON, unless this Court enjoins the infringing conduct.

34. ACTICON is informed and believes, and on that basis alleges, that DEFENDANTS' infringement of the '470 patent has been, and continues to be, willful and deliberate.

WHEREFORE, ACTICON seeks relief as set out in the Prayer.

PRAYER FOR RELIEF

WHEREFORE, ACTICON prays for judgment against DEFENDANTS on all Counts as follows:

1. For judgment that DEFENDANTS have infringed the '320 patent, the '470 patent and the '506 patent;

2. For judgment that DEFENDANTS have induced infringement of the '320 patent, the '470 patent and the '506 patent;

3. For judgment that DEFENDANTS have contributorily infringed the '320 patent, the '470 patent and the '506 patent;

4. For judgment that DEFENDANTS' infringement of the '320 patent, the '470 patent and the '506 patent is, and has been, willful and deliberate;

5. On all Counts, for a preliminary and permanent injunction enjoining DEFENDANTS, its subsidiaries, officers, agents, servants, employees, licensees, and all other persons in active concert or participation with DEFENDANTS, from further infringement, inducement of infringement, or contributor infringement of the '320 patent, the '470 patent and the '506 patent;

6. On all Counts, for an award of damages pursuant to 35 U.S.C. § 284 adequate to compensate ACTICON for DEFENDANTS' infringement of the '320 patent, the '470 patent, and the '506 patent, but not less than a reasonable royalty, with interest, including pre-judgment

interest, and a trebling of such damages in view of the willful and deliberate nature of the infringement.

7. For costs, including expenses and reasonable attorney's fees pursuant to 35 U.S.C. §§ 284 and 285; and

8. For further and/or alternative relief as deemed just and proper.

DATE: January 23, 2002

CARR & FERRELL LLP

By: _____
ROBERT J. YORIO

Attorneys for Plaintiff ACTICON TECHNOLOGIES LLC

DEMAND FOR JURY TRIAL

ACTICON TECHNOLOGIES LLC hereby demands a jury trial of all issues in the above-captioned action which are triable to a jury.

DATE: January 23, 2002

CARR & FERRELL LLP

By: Robert J. Yorio
ROBERT J. YORIO

Attorneys for Plaintiff ACTICON TECHNOLOGIES LLC

United States Patent [19]

Farago

[11] Patent Number: 4,603,320

[45] Date of Patent: Jul. 29, 1986

[54] CONNECTOR INTERFACE

[75] Inventor: Steven Farago, Mount Kisco, N.Y.

[73] Assignees: Anico Research, Ltd. Inc., Mount Kisco; Rapitech Systems Inc., New York, both of N.Y.

[21] Appl. No.: 484,823

[22] Filed: Apr. 13, 1983

[51] Int. Cl.[4] H03K 13/24

[52] U.S. Cl. ..... 340/347 DD; 339/176 MP; 361/394

[58] Field of Search ..... 340/347 DD, 339/17 R, 339/17 C, 17 F, 14 R, 17 M, 17 LC, 17 N, 176 R, 176 M, 176 MP; 361/392-395, 412, 415; 364/705-771; 179/20 P

[56] References Cited

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3,885,167	5/1975	Berglund	340/347 DD
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4,361,955	12/1982	Lancaster	339/17 F
4,458,967	7/1984	King et al.	339/14 R
4,487,464	12/1984	Kirschenbaum	339/19

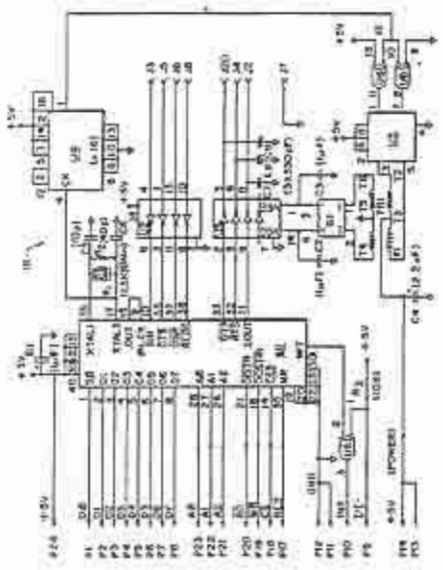
Primary Examiner—Vit W. Miska

Attorney, Agent, or Firm—Israel Nissenbaum

[57] ABSTRACT

A connector interface for enabling communications between first and second data handling systems wherein the data in the first system is arranged in a first type of format and the data in the second system is arranged in a second type of format, includes a connector housing with first and second sets of electrical contact elements exposed at different portions of the housing. Circuitry contained entirely within the housing operates to convert data transmitted to the first set of contact elements from the first data handling system into corresponding data in the second type of format for transmission to the second data handling system through the second set of contact elements, and to convert data transmitted to the second set of contact elements from the second data handling system into corresponding data in the first format for transmission to the first data handling system. One set of electrical contact elements may, for example, be arranged to extend out from the connector housing in two parallel rows to allow the elements to be directly connected to corresponding terminals arranged in a dual in line configuration on an outside printed circuit board. The connector arrangement greatly simplifies the design and construction of data processing systems requiring specific interfaces between certain parts of the systems, such as between data terminal equipment and data communication equipment employing serial binary data interchange.

23 Claims, 7 Drawing Figures



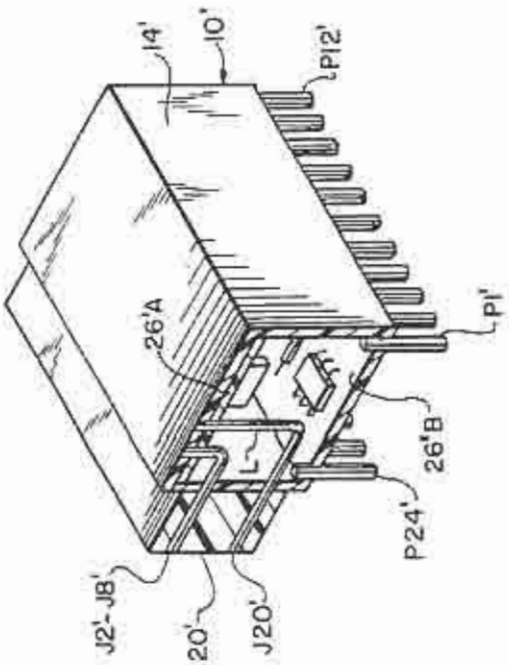


EXHIBIT A

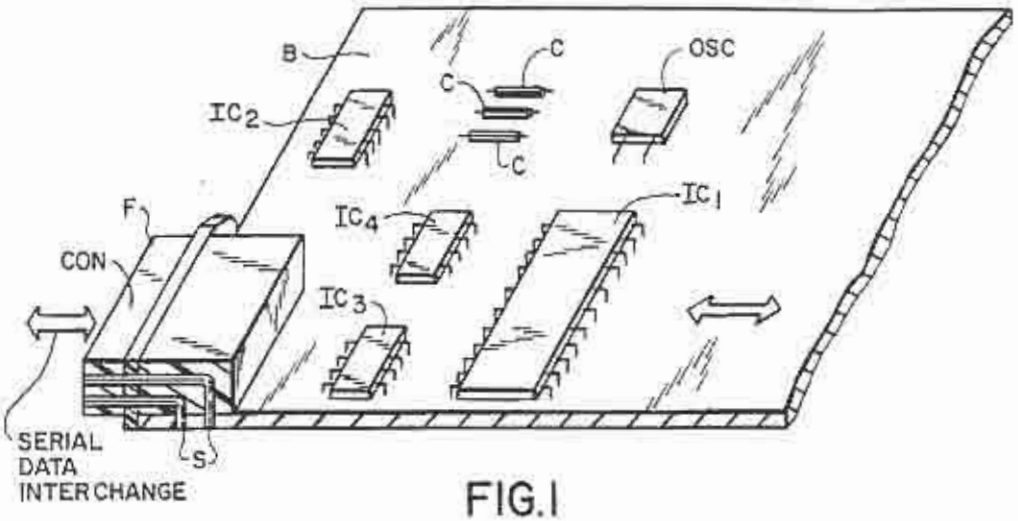
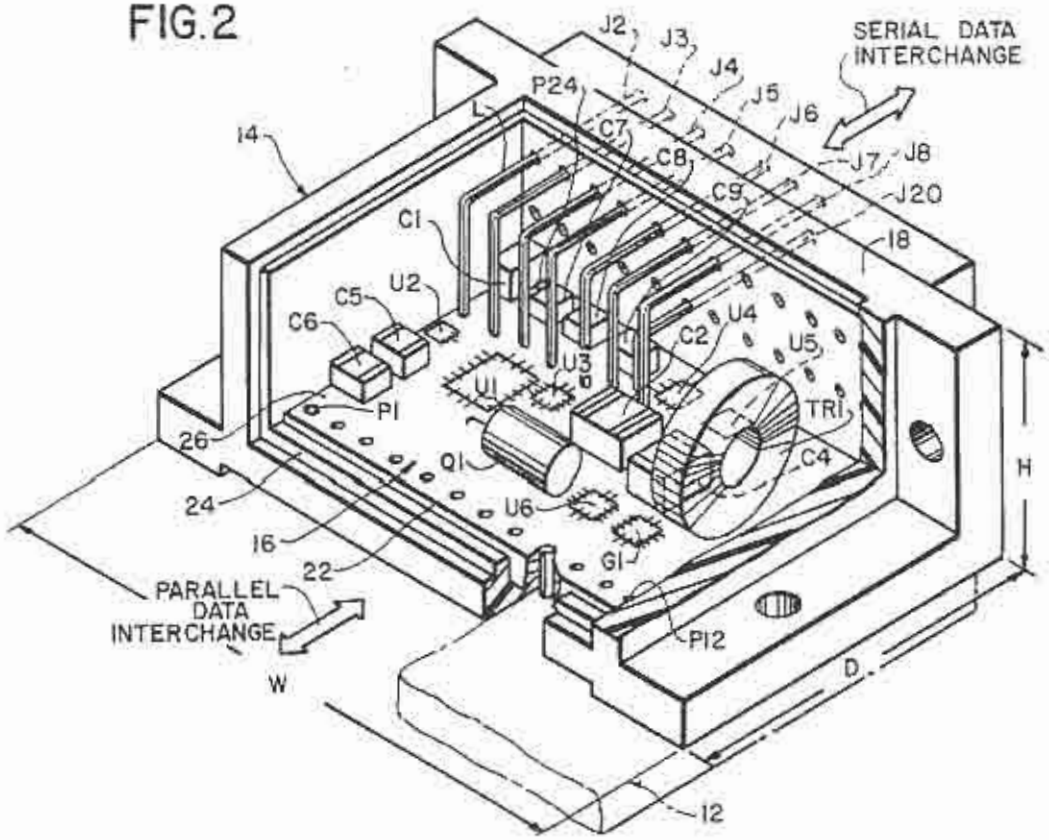
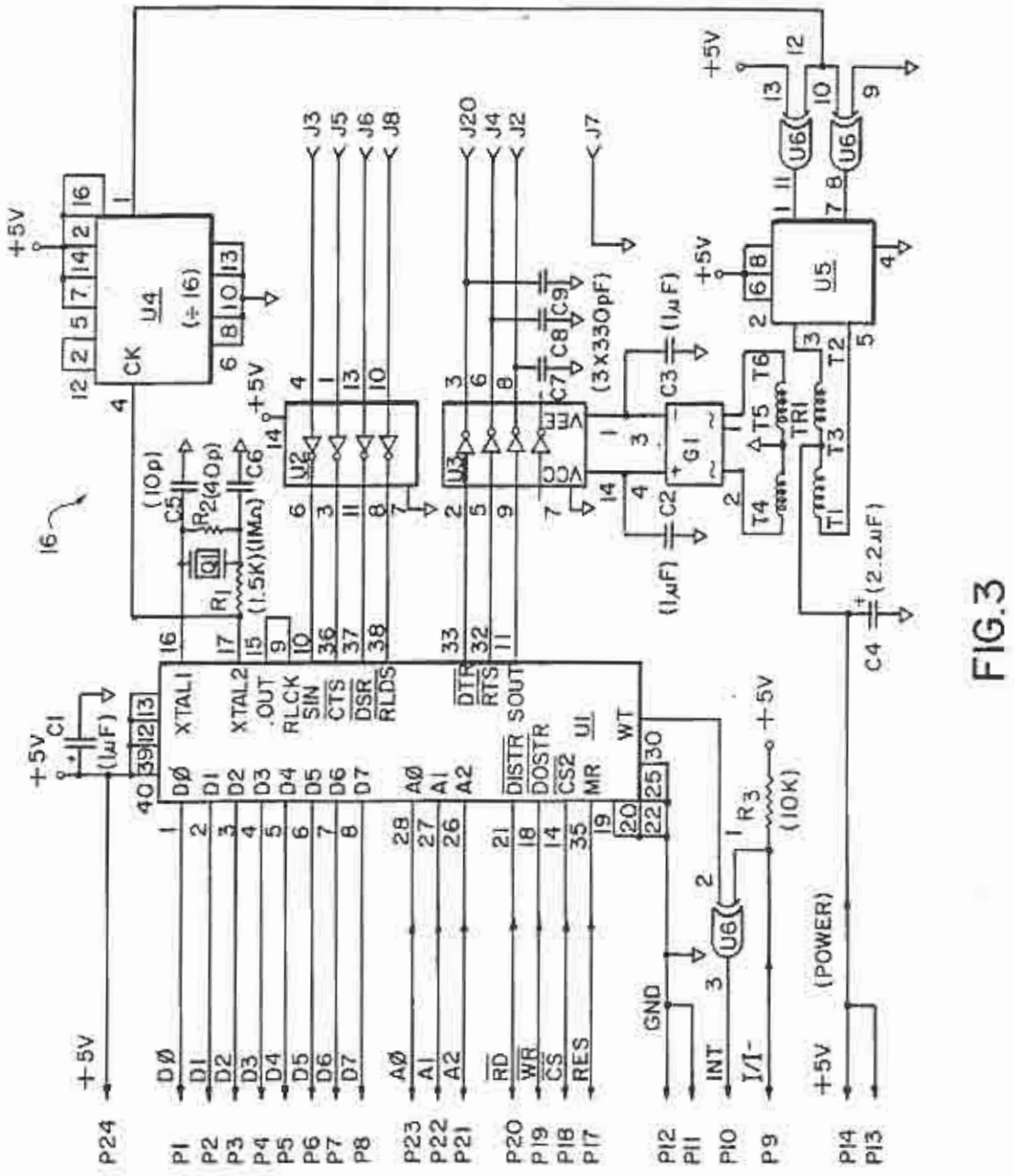


FIG.1
PRIOR ART

FIG.2




+5V
U4
(÷ 16)
CK
16
(10p)
C5
R2(40p)
C6
Q1
R1
(1.5K)(1MΩ)
U2
U3
J3
J5
J6
J8
J20
J4
J2
J7
C7
C8
C9
(3X330pF)
C3
(1μF)
C2
(1μF)
G1
T5
T6
T4
T1
TRI
T3
T2
U5
U6
C4
(2.2μF)
C1
(1μF)
XTAL1
XTAL2
OUT
RLCK
SIN
CTS
DSR
RLDS
DTR
RTS
SOUT
UI
WT
DISTR
DOSTR
CS2
MR
D0
D1
D2
D3
D4
D5
D6
D7
A0
A1
A2
RD
WR
CS
RES
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(10K)
GND
INT
I/I-
(POWER)
P24
P1
P2
P3
P4
P5
P6
P7
P8
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P12
P11
P10
P9
P14
P13

FIG.3

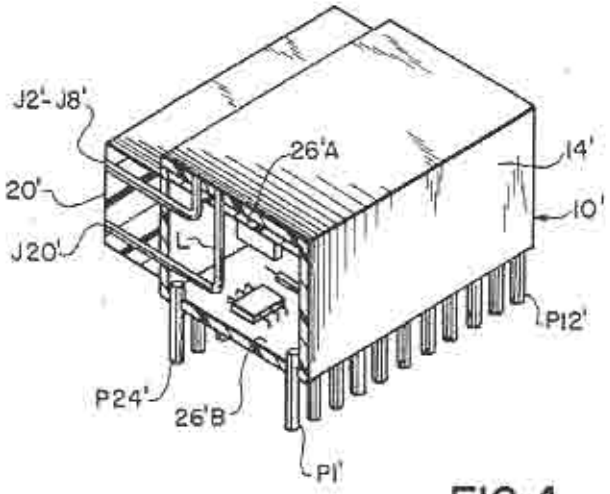


FIG.4

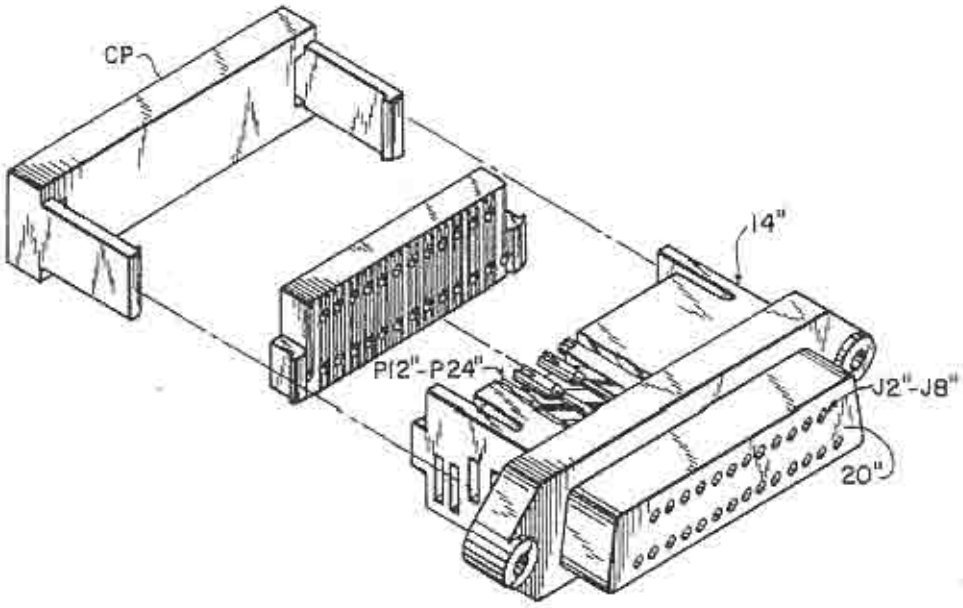
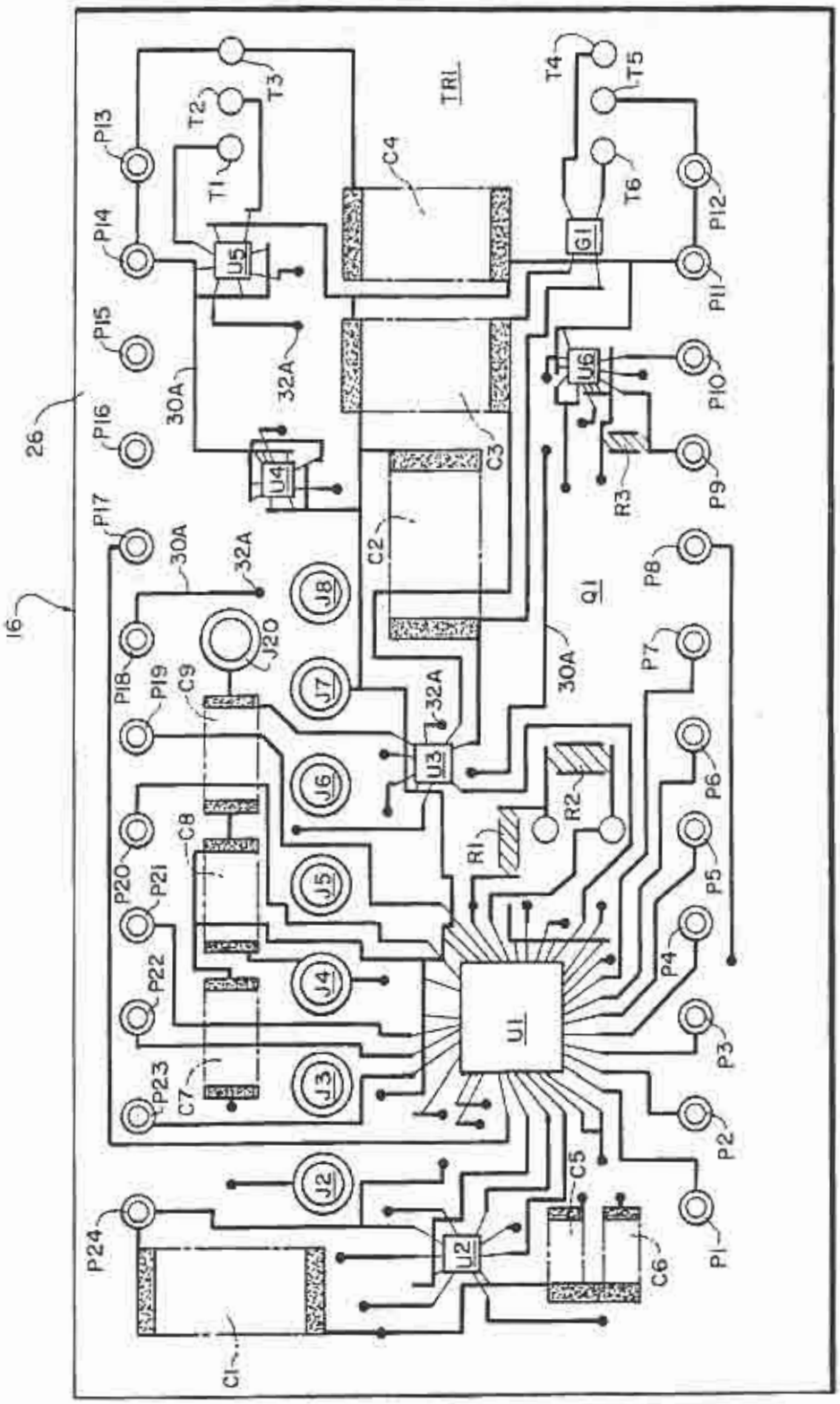


FIG.5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T1
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T3
T4
T5
T6
C1
C2
C3
C4
C5
C6
C7
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R1
R2
R3
Q1
U1
U2
U3
U4
U5
U6
G1
J2
J3
J4
J5
J6
J7
J8
J20
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
P11
P12
P13
P14
P15
P16
P17
P18
P19
P20
P21
P22
P23
P24
16
26
30A
32A

FIG.6A

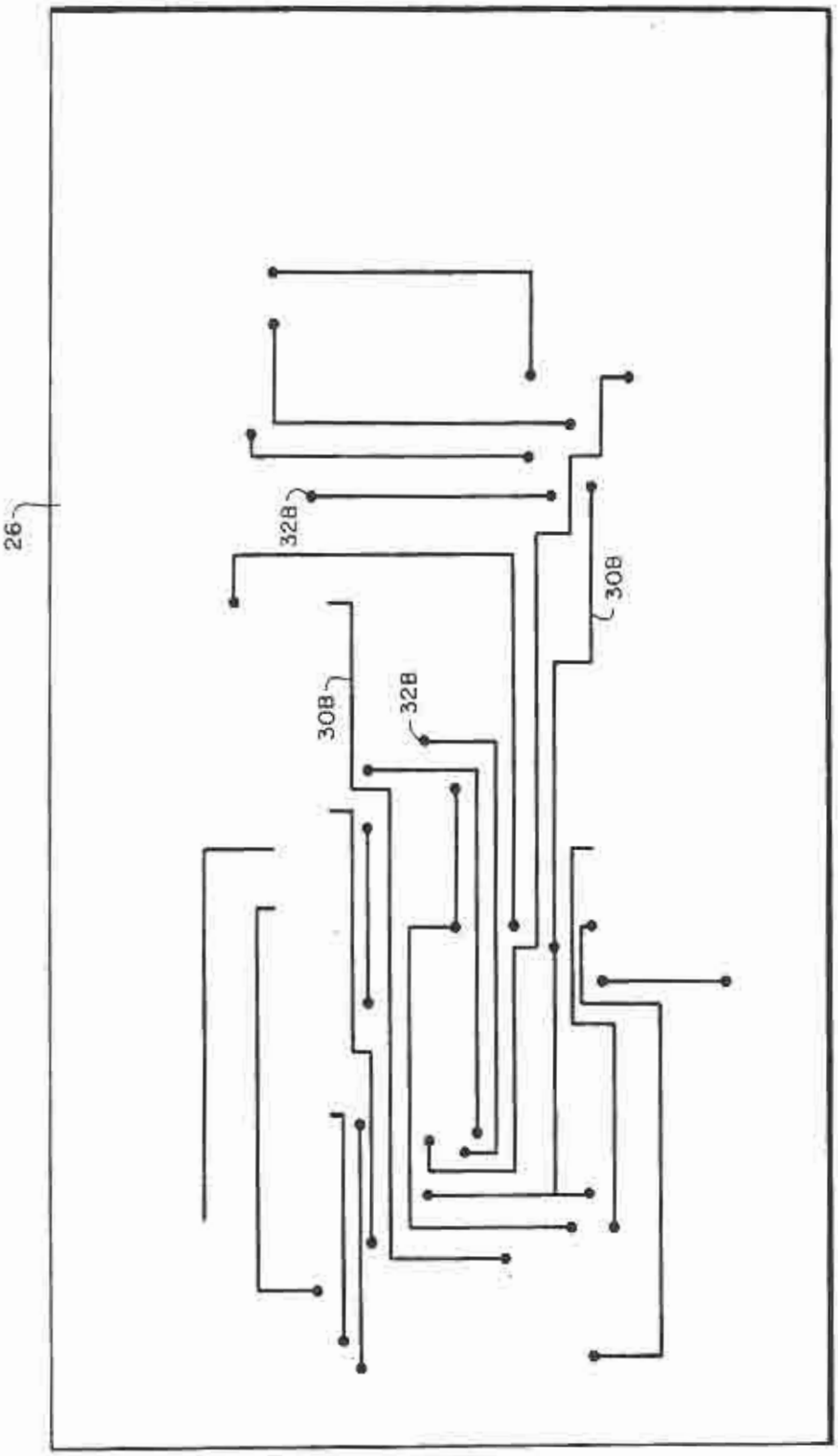

FIG.6B

CONNECTOR INTERFACE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to elelctrical connectors, and particularly to a connector having internal circuitry capable of providing a specified electrical interface between various types of data handling equipment.

2. Description of the Prior Art

The proliferation of digital data processing equipment, first in business and now into the home, has created an ongoing demand for such equipment with ever increased capabilities but at an affordable price. The modern trend to integrate numerous discrete electrical components within single semiconductor integrated circuits or "chips", has provided for greater economies in the manufacture of digital electronic equipment. Not only is the overall physical size and weight of the equipment reduced through use of integrated circuit technology, but manufacturing costs also are alleviated in that the price of each integrated circuit used is but a fraction of the total cost represented by all the components it contains.

Digital data processing systems which are in common use today include portions arranged to allow the user to communicate with the system by way of, for example, a terminal or a printer. The user "talks" or provides information to the system through the terminal, and this information is converted into digital data which the system is capable of understanding. After the data is processed by the system which may include some form of computer, a suitable response is transmitted back to the user in digital form and then properly converted into visibly recognizable words or symbols on the screen of the terminal or on a sheet generated by a printer.

Accordingly, it is often necessary to provide cable interconnections between differently located units of a data processing system to allow the units to transmit and receive digital data to and from one another.

Certain types of digital equipment, e.g. a terminal or a printer, transmit or receive digital data in serial bit format. That is, each character (i.e., letter or numeral) of the data is sent or received one bit at a time. It will be appreciated that in a typical system where each character occupies multiple bits, communicating the characters as serial bits between separately located pieces of equipment reduces significantly the number of separate conductors which must be provided in the connecting cables, allows for the communicating equipments to operate in time synchronism with one another with regard to the data exchanged between them, as well as for the use of parity bits and other common error detecting techniques to be applied for each data character communicated. Other kinds of equipment in data handling systems operate in a parallel bit format. For example, computers operate on data which is loaded in internal registers one full character (i.e., eight bits) at a time, and likewise provide output information a character at a time to internal output registers.

In order to insure compatability between terminals, printers and other input/output data handling equipment which operate in a serial bit format, and computer mainframes and related equipment, the electronic Industries Association promulgated in 1969 a now widely accepted interface standard known as EIA RS-232-C,

the provisions of which are incorporated by reference herein. The RS-232-C Standard, entitled "Interface Between Data Terminal Equipment and Data Communication Equipment Employing Serial Binary Data Interchange", ensures that serial bit format equipment produced by one manufacturer will operate properly with serial bit format equipment of another manufacturer. The RS-232-C Standard applies not only to the interchange of information data signals between data handling equipment, but also to the interchange of timing and control data signals between such equipment (Sec. 1.4 of the Standard).

In order to ensure satisfactory noise immunity of the data signals to be communicated over connecting cables, the RS-232-C Standard provides that the data signals transmitted over the cables have magnitudes of at least ±6 volts (See Sec. 2.3 of the Standard). Since most data handling equipment today operate at five-volt levels, the Standard makes necessary additional power supplies for enabling a voltage level conversion of the data signals to be interchanged over the connecting cable.

With regard to mechanical characteristics of the interface, the RS-232-C Standard states that the interface is "located at a pluggable connector signal interface point between the two equipments. The female connector . . . should be mounted in a fixed position near the data terminal equipment". (Sec. 3.1). FIG. 3.1 within the RS-232-C Standard assigns certain circuit functions to each of 25 connector pins associated with the pluggable connector at the signal interface point. While the Standard does not specify a particular type of multiple pin connector (See Appendix I to the Standard), the "D-type" 25 pin connector (for example, AMP type 206584-1) has essentially become an industry standard.

A printed circuit board together with circuit components and software necessary to achieve an RS-232-C interface between a computer terminal on one side, and modems or serial line printers on the other side, is available from a variety of manufacturers. Such boards are mountable inside the computer, and separate cable is provided. These boards are compatible from the RS-232-C side but they differ on the computer side from computer to computer.

The known RS-232-C interfaces which include a printed circuit board are arranged physically as shown in FIG. 1. The board B can be a "stand alone card" and be connected via a card cage connector (not shown) to various parallel signal bus lines associated with a microprocessor in a computer or other terminal equipment (also not shown). Alternatively, it can be a part of a more complex board. The RS-232-C Standard 25-pin connector CON may be mounted along one edge of the board B as shown, and the pins directly connected electrically to printed conductors on the board by soldering as at points S on the underside of the board B. This leaves a female connector part F fixedly mounted near the data terminal equipment as required by the Standard. The various conductors to which the pins of the connector CON are connected lead to electrical circuitry arranged over other portions of the board B, including, for example, a main logic element chip IC 1, line driver IC 3, line receiver IC 4, crystal oscillator OSC, frequency divider IC 2, and a number of discrete components C.

It will be appreciated that the known RS-232-C interface board arrangements require that a certain amount

of space be allocated in existing equipment for their insertion, such space often being at a premium in units intended to be portable and of small overall dimensions. As far as is known, there has been no attempt to integrate any electrical interface circuitry, including those components required to implement the RS-232-C interface as shown in FIG. 1, within the prescribed interface connector itself such as the 25-pin connector CON.

A connector is known from U.S. Pat. No. 3,790,858 to Brancaleone et al within which RF filter elements are connected to a number of parallel pin-like contact elements which are supported inside and extend axially through a cylindrical shell. The filter elements are connected internally between the contact elements and a common cylindrical metal ground plate.

SUMMARY OF THE INVENTION

A primary object of the present invention is to provide a connector which exhibits simultaneously both the electrical characteristics and the connector requirements of a specified interface between two different data handling systems or equipments.

Another object of the invention is to provide a method wherein electrical circuitry for carrying out a specified function between two different data handling systems is integrated within a connector housing so as to reduce significantly spatial requirements within equipment associated with the systems.

According to one aspect of the invention, a connector includes a housing having a first set and a second set of terminals extending at least partly through wall parts of the housing to engage corresponding terminals of first and second outside connection means associated with first and second data handling systems, respectively. Logic interface circuit means is arranged within the connector housing and coupled between the first and second set of terminals. The circuit means operates to convert data signals transmitted to the first set of terminals from the first data handling system in a first type of format into corresponding data signals in a second type of format, and to provide the corresponding data signals in the second type of format to the second set of terminals for transmisson to the second data handling system. The circuit means also operates to convert data signals transmitted to the second set of terminals from the second data handling system in a second type of format into corresponding data signals in a first type of format, and to provide the corresponding data signals in the first type of format to the first set of terminals for transmission to the first data handling system.

According to another aspect of the invention, a method of implementing a logical interface to enable communications between a first data handling system in which data signals are arranged in a first type of format, and a second data handling system in which data signals are arranged in a second type of format, includes the steps of providing a connector housing; supporting first and second sets of electrical contact elements on the housing; containing electrical circuitry within the connector housing and connecting the circuitry with the first and the second sets of contact elements by arranging conductors inside the housing; converting by way of the electrical circuitry data signals transmitted to the first set of electrical contact elements in a first type of format from a first data handling system outside the connector housing into corresponding data signals in a second type of format and providing same to the second set of electrical contact elements through the conductors inside the connector housing; and converting by way of the electrical circuitry data signals transmitted to the second set of electrical contact elements in the second type of format from a second data handling system outside the connector housing into corresponding data signals in the first type of format and providing same to the first set of electrical contact elements through the conductors inside the connector housing.

The invention will be more clearly understood upon reading the following detailed description of preferred embodiments thereof in conjunction with the accompanying drawing.

BRIEF DESCRIPTION OF THE DRAWING

In the drawing:

FIG. 1 is a perspective view of a conventional serial interface arranged on a portion of a printed circuit board;

FIG. 2 is a perspective view, with parts broken away, showing a first embodiment of a connector according to the present invention mounted on a printed circuit board;

FIG. 3 is a schematic diagram representing electrical circuitry contained in the housing of the connector in FIG. 2;

FIG. 4 is a perspective view of a second embodiment of a connector according to the present invention;

FIG. 5 is a perspective view of a third embodiment of a connector according to the present invention;

FIG. 6A is a top plan view of a printed circuit layout, and the phantom outline of the components, of the electrical circuitry seen in the schematic diagram of FIG. 3; and

FIG. 6B is a bottom plan view of the printed circuit board illustrating the interconnection among the various components.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 2 shows a first embodiment of a connector 10 according to the invention, the connector 10 being mounted on a printed circuit board 12 associated with a data handling system or equipment (not shown) in which data is interchanged in a parallel format. The connector 10 includes a connector housing 14, portions of which are omitted in FIG. 2 for the purpose of illustrating electrical circuitry 16 mounted in the interior space of the housing 14. It is preferable that walls of the housing 14 substantially enclose the interior space so as to protect the circuitry 16 contained therein.

As shown in FIG. 2, the housing 14 is in the form of a generally rectangular hollow block and includes a front wall 18, a part of which projects outwardly to define first outside connection surface 20 parallel to the inside surface of wall 18. Housing 14 also includes a bottom wall 22 the outside surface of which defines a second outside connection surface 24. The outside dimensions of the housing 14, particularly those of the front wall 18 together with the first outside connection surface 20, preferably conform to those of a standard socket connector, thereby being adapted to mate with a standard plug connector or corresponding or complementary configuration. For applications in the RS-232-C interface, the housing 14 should conform to the dimensions of the known 25-pin "D type" subminiature connector mentioned earlier. Typical dimensions for the housing 14 thus may be a height H of about 0.5

inches (12.70 mm.), a depth D of about 1.2 inches (30.48 mm.) and a width W of about 2.0 inches (50.80 mm.).

The electrical circuitry **16** includes, in the embodiment of FIG. 2, a carrier in the form of a single printed circuit board or substrate **26** mounted closely adjacent and parallel to the inside surface of the bottom wall **22**. Various integrated circuits and discrete components are mounted on the board **26**, and are electrically connected by soldering, or by other technology, to conductors on one or both sides of the board **26**.

The various "chips" and components shown in FIG. 2 as contained within the connector housing **14** on the board **26**, and represented schematically in FIG. 3, include integrated circuits U1–U6; four tantalum chip capacitors C1–C4; a set of five chip capacitors C_5–C_9; a quartz crystal Q1; a toroid core transformer TR1 having bifilar wound primary and secondary windings T1–T2 and T4–T6; and a Graetz diode bridge G1. Each of eight conductors L extends from a different one of eight connection points on the printed circuit board **26** (FIG. 2), to corresponding female electrical contact elements or terminals J2–J8 and J20 which extend partly through and are supported in openings in the wall **18**. The outside ends of the female contact elements are exposed at the first outside connection surface **20** to engage corresponding pins of an outside plug connector (not shown). The numbers assigned to the female contact elements J2–J8 and J20 correspond to the pin number-circuit function assigments prescribed in the RS-232-C Standard, mentioned earlier. Further, 24 male electrical contact elements or pins P1–P24 extend in two parallel rows of 12 pins each, downwardly from connection points near the long edges of the board **26** (FIG. 2), to engage openings in printed conductors or a conventional dual in line socket on the outside printed circuit board **12**, at the second outside connection surface **24**.

In accordance with a preferred technique of manufacture, the housing **14**, except for the bottom wall **22**, is molded in one piece; the elements or terminals J2–J8 and J20, as well as the conductors L, being included in the molding operation. Then, the bottom wall **22** and abutting printed circuit board **26** are snapped into position in the housing. By means of localized heating, the bottom wall is fused to the housing so that a completely unitary structure is achieved.

FIG. 3 shows the interconnections between the chips and other electrical components on the printed circuit board **26** contained within the connector housing **14**, together with the female and the male contact elements arranged on the first and the second outside connection surfaces **20**, **24** of the connector **10**, respectively. The circuitry of FIG. 3 is one example of circuitry which functions to provide the electrical characteristics of an RS-232-C interface, but it will be appreciated that different circuitry may be integrated within the connector housing **14** to carry out the same function or other commonly used interfaces including 8-bit Parallel, GPIB (general purpose interface bus-IEEE 488), and Ethernet.

The integrated circuit U1 may be, for example, National Semiconductor type INS 8250A. The circuit U1 serves as a main logic element which handles all data signal interchanges between, e.g., a microprocessor (not shown) which handles data in a parallel bit format and communications equipment (not shown) which sends and receives serial bit data. Circuit U1 contains several programmable registers which determine the communications format and all the necessary information data to perform successfully a two-way data interchange between two data systems of different data formats. Specifically, before sending or receiving any data via an RS-232-C line, a controlling microprocessor (not shown) must load the internal registers with the required commands. The system software contains the following load functions which, when programmed within circuit U1, enable the latter to be used for data communications. The preprogrammed functions are:

1. Baud rate and baud rate factor;
2. Character length;
3. Number of stop bits;
4. Parity enable/disable and parity polarity;
5. Modem control functions; and
6. Additional operational conditions.

Instructions representing the above load functions are transmitted to the circuit U1 from an outside microprocessor (not shown) over data bus lines DO–D7 corresponding to the male contact elements or pins P1–P8 on the second outside connection surface **24** of the connector housing **14** (FIG. 2). The appropriate registers within circuit U1 are selected by the address bus lines A, A1 and A2 (pins P23, P22 and P21), and a write signal ($\overline{WR}$, pin P19) validates the register loadings.

When data characters are transmitted by the outside microprocessor after the foregoing initialization procedure, the circuit U1 performs a parallel-to-serial data conversion. First, the eight-bit parallel data is placed into a transmitter register within circuit U1 which then automatically adds a start bit, followed by the data character bits themselves (least significant first) and the programmed number of stop bits for each character. Also, an even or odd parity bit is inserted prior to the stop bit(s) as defined previously by the system program. The character is then transmitted as a serial data stream on a data output line S_{out} at terminal 11 of the circuit U1. The rate at which the data is shifted out is determined by another previously programmed register within circuit U1. The quartz crystal Q1 coupled to the circuit U1 operates together with a programmable divider within circuit U1 to generate a signal of the appropriate frequency for shifting out the data bits.

The strength or voltage levels of the data bits or signals shifted out from the circuit U1, typically TTL compatible (zero to +5 volts). As mentioned earlier, the RS-232-C Standard requires a stronger signal level so that data can be transmitted over a long cable with the capacity of noise suppression. Accordingly, a line driver circuit U3, e.g., Motorola type MC 1488, is coupled to data output S_{out} and supplementary handshake signals as $\overline{RTS}$ (Request to Send) and $\overline{DTR}$ (Data Terminal Ready) of the circuit U1. When powered by an appropriate power supply, the line driver circuit U3 converts the TTL compatible level (zero to +5 volt) of the serial output from the circuit U1, to a ±12 volt level sufficient to satisfy the RS-232-C Standard. The integral power supply is constructed of a push-pull mode switching scheme, performed by high frequency oscillator derived from U4 (e.g. 4516B RCA), 74C86 exclusive OR gates (U6 e.g. Nat. Semiconductor), high current power transistors within U5 (75951 e.g. Texas Instruments) Tr1 transformer, G1 diode bridge and C2,C3 tantalum capacitors.

When a serial data bit stream is transmitted to the connector **10** from an outside data handling system, specifically to the female contact elements J3 at the first outside connection surface **20** of the housing **14**, the

higher voltage level of the bit streams is converted to a TTL compatible (0 to 5 volt) logic level by way of buffer-inverters within circuit U2 (e.g., Motorola type MC 1489A). Also, high level complementary signals (J5, J6 and J8 are converted down). The serial data is then shifted into a receiver register within the main logic element circuit U1 where the data is converted into a parallel format; however, the start and stop bits and the parity bit are subtracted. Thus, the data is then ready to be sent to the microprocessor or other outside parallel format data system over the data bus lines DO-D7.

The circuit U1 is selected for operation by the microprocessor or other outside parallel data system connected to the pins P1-P24 of the connector 10 by way of a chip select signal ($\overline{CS}$, pin P18). The receiver register within the circuit U1 is selected by a preset combination of the address bus lines (A0, A1, A2; pins P23, P22, P21), and the parallel data is placed on the data bus lines (DO-D7; pins P1-P8) for transmission to the outside microprocessor. A read signal ($\overline{RD}$, pin P20) activates the data reading from the circuit U1 to the microprocessor. Likewise, status information reading procedure can be performed similarly.

There are several control signals, and control and status registers in circuit U1 that determine the bidirectional serial communication procedure. All the necessary signals, including "handshaking", status and command bits, and modem control are included in communications following the preprogrammed functions from the outside microprocessor software.

Those components on the board 16 (FIG. 2) which have not been discussed above in detail but appear in the circuitry of FIG. 3 will be recognized and understood by those skilled in the art. A preferred quartz crystal Q1 is Seiko type DS-MGQ, 1.8432 MHz, series resonant. The chip capacitors C1-C4 may be Arco type ACT, tantalum, and the chip capacitors C5-C9 may be Murata type GR40 Y5 V. Chip resistors R1-R3 can be panasonic type ERJ-86CSJ, or alternatively can be thick film resistors deposited on the board 16.

The toroid transformer TR1 preferably is made from a Ferroxcube core type 266CT125, material 4C4. The primary winding is 2×10 turns and the secondary is 2×25 turns, both bifilar.

FIG. 4 shows a second embodiment of a connector 10' according to the invention. The outside dimensions and overall appearance of the connector 10' are generally similar to those of the connector 10 of FIG. 2. Two printed circuit boards or substrates 26'A and 26'B are, however, provided in housing 14' instead of the single board 26 in FIG. 2. Board 26'A extends at the top of the housing 14' parallel to the board 26'B which extends across the bottom of housing 14'. Board 26'B carries 24 pins P1'-P24' on its bottom outside surface 24' for connection directly to an outside circuit board or into a dual-in-line socket. The board 26'A is coupled by leads L' to female contact elements J2'-J8' and J20' which engage an outside plug connector at connection surface 20' of the connector 10'.

FIG. 5 shows a third embodiment of a connector 10" according to the invention. A single, flexible printed circuit board 26" is contained within the connector housing 14". Conductors at one end of the board 26" are directly to the inside of female contact elements J2"-J8" and J20" which are arranged to engage an outside plug connector at contact surface 20". Conductors at an opposite end of the flexible board 26" are connected directly to the inside ends of insulation displacement type pins P1"-P24". A cap CP is constructed and arranged to clamp a flat insulated cable (not shown) over pointed ends of pins P1"-P24" so that the pins pierce through the cable insulation to electrically contact corresponding conductors of the flat cable.

It will be appreciated that the connector of the present invention provides a completely self-contained interface unit which eliminates all the inconveniences of designing and realizing a data interface such as the RS-232-C Standard. Particular components no longer need be selected to meet the requirements of the Standard, voltage level conversions are provided for, and time consuming test procedures and debugging are eliminated. The present connector thus saves engineering effort, development and production time as well as labor costs. Importantly, a considerable space savings is achieved in terminal equipment which would otherwise require means to accommodate a separate interface board.

In order to enable the man skilled in the art to practice this invention in some detail, a complete printed circuit layout is shown in FIG. 6. This layout conforms with the circuitry previously illustrated in schematic form in FIG. 3. The contact areas J2-J8 and J20, which correspond with the respective female contact elements so designated, will be seen in FIG. 6A. Likewise, contact areas P1-P12 (at the near longitudinal edge) and P13-P24 (at the far edge), which correspond with the respective male contact elements bearing the same designation. Capacitors C1-C9, oscillator Q1, and transformer TR1, are seen in phantom outline while resistors R1, R2 and R3 are represented by means of hatch lines. All the other principal elements are shown by means of rectangles suitably labeled. Appropriate wire bonding from the several integrated circuits U1-U6, as well as from the Graetz bridge G1, is shown in FIG. 6A connected to the conductors 30A on the printed circuit board.

It will be noted by the skilled worker that suitably correlated conductors 30B are provided on the lower surface of the printed circuit board 26 (FIG. 6B) so as to make the requisite interconnections among components. The dots 32 represent so-called "vias" between the upper and lower surfaces of board 26.

It will be appreciated that, for the sake of clarity, the depiction of a printed circuit layout for a circuit board 26 to be housed in connector 10 of FIG. 2 is greatly enlarged (approximately 7 times).

While specific embodiments of the invention have been shown and described in detail to illustrate the application of the inventive principles, it will be understood that the invention may be embodied otherwise without departing from such principles.

I claim:

1. An electrical connector for implementing a direct predetermined logical interface between a first data handling system wherein data signals are arranged in a first type of format, and a second data handling system wherein data signals are arranged in a second type of format, comprising:

a connector housing including a first wall part forming a first outside connection surface and a second wall part forming a second outside connection surface;

a first set of terminals arranged to extend at least partly through said first wall part from inside said connector housing in a given configuration for

engaging in electrical contact with corresponding terminals of first outside connection means associated with the first data handling system, with said first set of terminals forming a single logical interface member for matingly engaging a corresponding single logical interface member formed by said corresponding terminals associated with the first data handling system;

a second set of terminal arranged to extend at least partly through said second wall part from inside said connector housing in a given configuration for engaging in electrical contact with corresponding terminals of second outside connection means associated with the second data handling system, with said second set of terminals forming a single logical interface member for matingly engaging a corresponding single logical interface member formed by said corresponding terminals associated with the second data handling system; and

logic interface circuit means arranged within said connector housing and coupled between said first set of terminals and said second set of terminals for converting data signals transmitted to at least some of said first set of terminals from the first data handling system in the first type of format into corresponding data signals in the second type of format and providing said corresponding data signals in the second type of format to at least some of said second set of terminals for subsequent transmission to the second data handling system, and for converting data signals transmitted to at least some of said second set of terminals from the second data handling system in the second type of format into corresponding data signals in the first type of format and providing said corresponding data signals in the first type of format to at least some of said first set of terminals for subsequent transmission to the first data handling system.

2. A connector according to claim 1, wherein said logic interface circuit means comprises means for converting data signals transmitted to at least some of said first set of terminals in a serial format into corresponding data signals in a parallel format and providing the corresponding parallel data signals to at least some of said second set of terminals, and for converting data signals transmitted to at least some of said second set of terminals in a parallel format into corresponding data signals in a serial format and providing the corresponding serial data signals to at least some of said first set of terminals.

3. A connector according to claim 1, wherein said logic interface circuit means comprises means for converting the voltage level of the data signals transmitted to at least some of said first set of terminals from a first voltage level into a second voltage level and providing the corresponding data signals at the second voltage level to at least some of said second set of terminals, and for converting the voltage level of the data signals transmitted to at least some of said second set of terminals from the second voltage level into the first voltage level and providing the corresponding data signals at the first voltage level to at least some of said first set of terminals.

4. A connector according to claim 1, wherein said logic interface circuit means comprises a printed circuit substrate mounted within said connector housing.

5. A connector according to claim 1, wherein said logic interface circuit means comprises an integrated circuit mounted within said connector housing.

6. A connector according to claim 4, comprising an integrated circuit mounted on said printed circuit substrate.

7. A connector according to claim 1, wherein said first set of terminals comprises a number of female contact elements arranged to mate with corresponding male contact elements of the first outside connection means, said first wall part of said connector housing having a number of openings in said first connection surface within which openings said female contact elements are fixedly supported, and said second set of terminals comprises a number of male contact elements arranged to mate with corresponding female contact elements of the second outside connection means, said second wall part of said connector housing having a number of openings in said second connection surface within which openings said male contact elements are fixedly supported.

8. A connector according to claim 7, wherein said first connection surface extends generally within a first plane, and said second connection surface extends generally within a second plane.

9. A connector according to claim 8, wherein said second plane is perpendicular to said first plane.

10. A connector according to claim 8, wherein said second plane is parallel to said first plane.

11. A connector according to claim 8, wherein said male contact elements are arranged in two parallel rows for engaging corresponding openings formed in the female contact elements of the second outside connection means.

12. A connector according to claim 1 wherein said connector housing has structural dimensions of a height of no more than about 0.5 inches (12.70 mm), a depth of no more than about 1.2 inches (30.48 mm), and a width of no more than about 2.0 inches (50.80 mm).

13. A connector according to claim 1 wherein said connector housing comprises walls forming an enclosure member and wherein said logic interface circuit means are completely enclosed within the walls of said connector housing.

14. The connector of claim 1 wherein said first set of terminals comprises a number of male contact elements adapted for direct integrated electrical mating with a printed circuit board member which handles data in said first type of format and wherein said housing is adapted to be physically supported by said printed circuit board.

15. The connector of claim 1 wherein said first set of terminals comprises a number of male contact pins adapted for direct integrated electrical mating with an insulated ribbon cable connector member, with said pins being adapted to pierce the insulation of said cable to electrically contact conductors of said cable whereby said electrical mating is effected said cable connector member being adapted to be electrically connected to a printed circuit board which handles data in a first format and wherein said connector comprises means to physically enclose a portion of said ribbon cable connector.

16. The connector of claim 13 wherein said logic interface circuit means furthr comprises a power supply, with said power supply being contained within said walls of said connector housing.

17. A "D-type" 25 pin RS-232-C connector having a male connection interface adapted for direct integrated electrical mating with a printed circuit board member which handles data in a parallel format, said connector further having a female connection interface for mating connection with an external male connection interface member from a device which handles data in a serial format, characterized in that means for converting data from said parallel format to said serial format and means for converting data from said serial format to said parallel format are electrically positioned between said male connection interface and said female connection interface within said connector, and wherein said connector is adapted to be physically supported by said printed circuit board.

18. A method of implementing a logical interface to enable communications between first and second data handling systems wherein data signals are arranged in a first type format in the first system and in a second type of format in the second system, comprising the steps of:

providing a connector housing and supporting first and second sets of electrical contact elements on the connector housing;

exposing the first set of electrical contact elements on one portion of the outside surface of the connector housing and exposing the second set of electrical contact elements on another portion of the outside surface of the connector housing;

arranging the first set of electrical contact elements for connection with the first data handling system outside of the connector housing and arranging the second set of electrical contact elements for connection with the second data handling system outside of the connector housing, wherein each of said first and second set of electrical contact elements comprises a single logical interface member, and wherein said interface members of said first and second set of electrical contact elements are matingly electrically connected to a corresponding single logical interface member of said first and second data handling system respectively;

containing electrical circuitry substantially within the connector housing and connecting the electrical circuitry with the first and second sets of electrical contact elements by arranging conductors inside the connector housing;

converting by way of the electrical circuitry data signals transmitted to at least some of the second set of electrical contact elements in the second type of format from the second data handling system into corresponding data signals in the first type of format; and

providing the corresponding data signals in the first type of format from the electrical circuitry through the conductors inside the connector housing to at least some of the first set of electrical contact elements.

19. The method of claim 18, including arranging one of the first and second sets of electrical contact elements for connection to corresponding terminals on an outside printed circuit board associated with one of the first and the second data handling systems.

20. The method of claim 18, including arranging one of the first and second sets of electrical contact elements for connection to an outside cable connector associated with one of the first and the second data handling systems.

21. The method of claim 18, including arranging a selected one of the first and second sets of electrical contact elements in the form of insulation displacement elements, piercing an insulated cable associated with one of the data handling systems with the displacement elements and electrically contacting the displacement elements with corresponding conductors inside the cable.

22. The method of claim 18, wherein one of said converting steps includes converting serial data into corresponding parallel data, and the other one of said converting steps includes converting parallel data into corresponding serial data.

23. The method of claim 12, including converting by way of the electrical circuitry the voltage level of the data signals transmitted to at least some of the first set of electrical contact elements from a first voltage level into a second voltage level and providing the corresponding data signals at the second voltage level to at least some of the second set of electrical contact elements through the conductors inside the connector housing, and converting by way of the electrical circuitry the voltage level of the data signals transmitted to at least some of the second set of electrical contact elements from the second voltage level into the first voltage level and providing the corresponding data signals at the first voltage level to at least some of the first set of electrical contact elements through the conductors inside the connector housing.

* * * * *

United States Patent [19]

Farago

[11] Patent Number: 4,686,506

[45] Date of Patent: Aug. 11, 1987

[54] MULTIPLE CONNECTOR INTERFACE

[75] Inventor: Steven Farago, Mount Kisco, N.Y.

[73] Assignees: Anico Research, Ltd. Inc., Mount Kisco; Rapitech Systems Inc., Suffern, both of N.Y. ; a part interest to each

[21] Appl. No.: 891,190

[22] Filed: Jul. 28, 1986

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 484,823, Apr. 13, 1983, Pat. No. 4,603,320.

[51] Int. Cl.[4] H03K 13/24

[52] U.S. Cl. ..... 340/347 DD; 361/394; 439/620

[58] Field of Search ..... 340/347 DD; 339/17 R, 339/17 C, 17 F, 14 R, 17 M, 17 LC, 17 N, 176 R, 176 M, 176 MP; 361/392-395, 412, 415; 364/705, 771; 179/20 P

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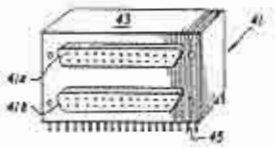
Primary Examiner—Vit W. Miska

Attorney, Agent, or Firm—Israel Nissenbaum

[57] ABSTRACT

A connector interface for enabling multiple conversions between first and second data handling systems wherein the data in the first system is arranged in a first type of format and the data in the second system is arranged in a second type of format, includes a connector housing with first and second sets of electrical contact elements exposed at different portions of the housing. Circuitry contained entirely within the housing operates to convert data transmitted to the first set of contact elements from the first data handling system into corresponding data in the second type of format for transmission to the second data handling system through the second set of contact elements, and to convert data transmitted to the second set of contact elements from the second data handling system into corresponding data in the first format for transmission to the first data handling system. One set of electrical contact elements may, for example, be arranged to extend out from the connector housing in two parallel rows to allow the elements to be directly connected to corresponding terminals arranged in a dual in line configuration on an outside printed circuit board. The other set of electrical contact elements may be arranged for multiple simultaneous or selective output connections for applications such as multiple communication, digital to analog and analog to digital conversions, and a multiple floppy disk controller.

13 Claims, 16 Drawing Figures



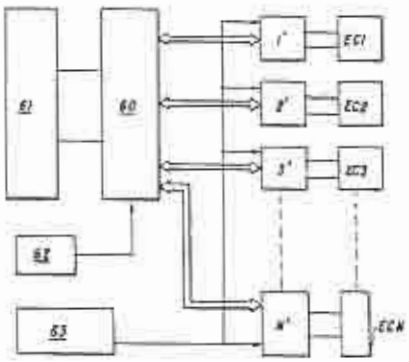


EXHIBIT B

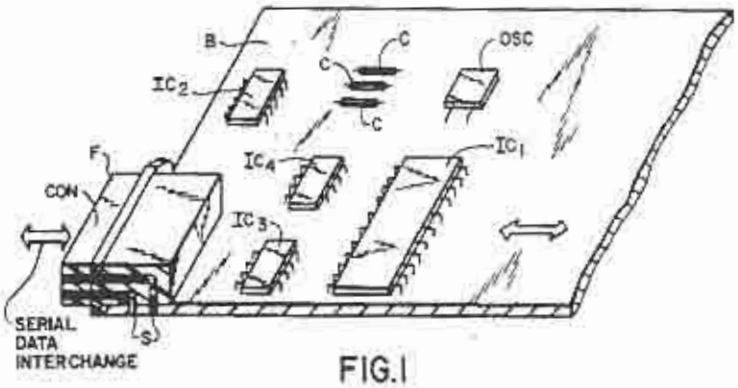
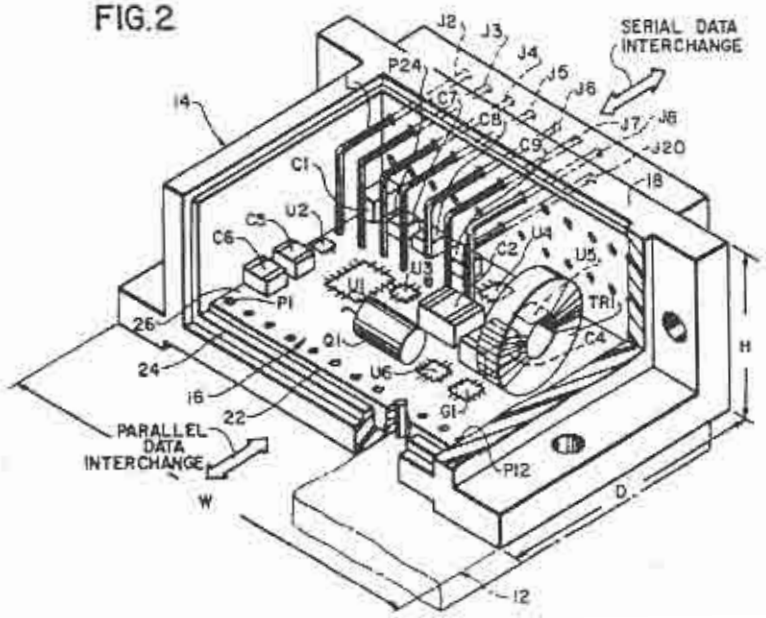
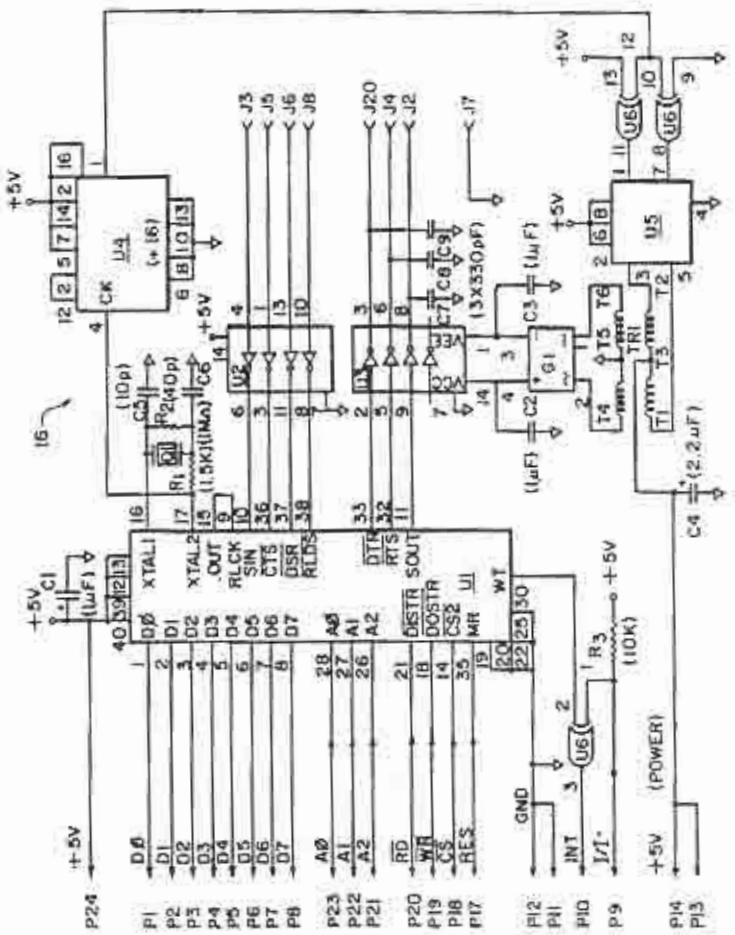


FIG.1
PRIOR ART

FIG.2




+5V
U4
(* 16)
CK
16
(10p)
C5
R2 (40p)
C6
R1 (1.5K)(1MΩ)
XTAL1
XTAL2
OUT
RLCK
SIN
CTS
DSR
RLDS
DTR
RTS
SOUT
WT
C1 (1μF)
D0
D1
D2
D3
D4
D5
D6
D7
A0
A1
A2
RD
WR
CS
RES
GND
INT
INT
(POWER)
R3 (10K)
J3
J5
J6
J8
J20
J4
J2
J7
C7
C8
C9 (3X330pF)
C3 (1μF)
C2 (1μF)
C4 (2.2μF)
G1
T1
T2
T3
T4
T5
T6
TRI
U5
U6
P24
P1
P2
P3
P4
P5
P6
P7
P8
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P12
P11
P10
P9
P14
P13

FIG.3

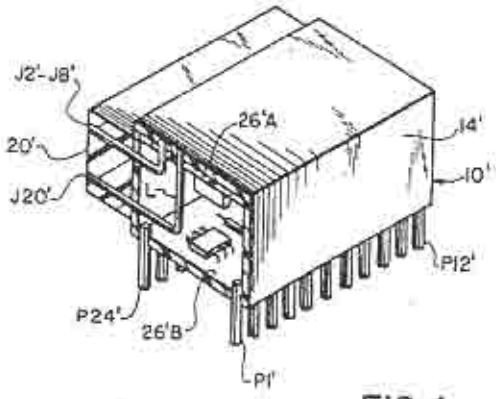


FIG.4

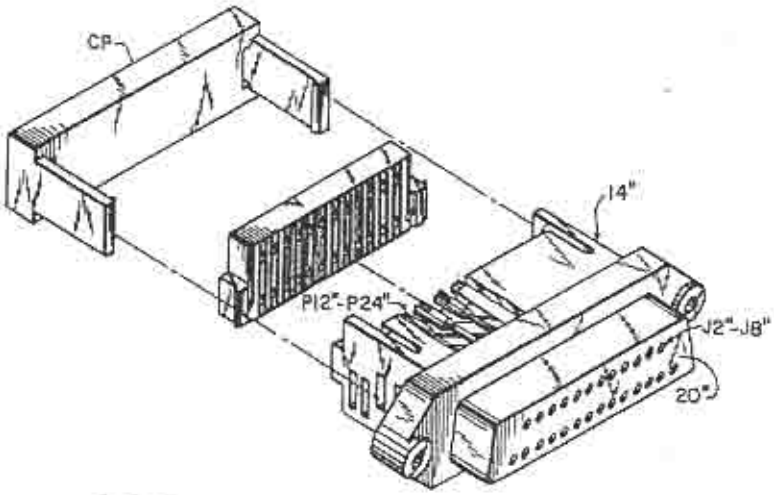
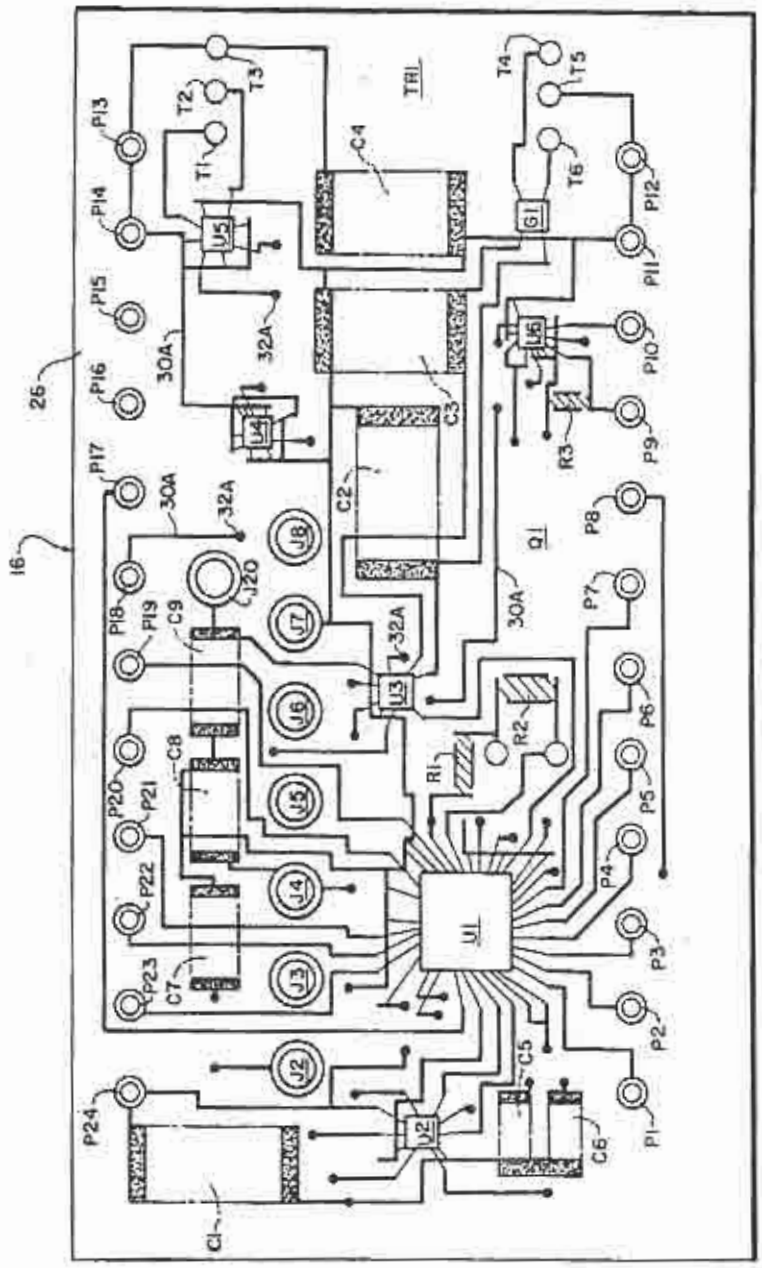


FIG.5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T1
T2
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T4
T5
T6
C1
C2
C3
C4
C5
C6
C7
C8
C9
R1
R2
R3
Q1
U1
U2
U3
U4
U5
U6
G1
J1
J2
J3
J4
J5
J6
J7
J8
J20
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
P11
P12
P13
P14
P15
P16
P17
P18
P19
P20
P21
P22
P23
P24
16
25
30A
32A

FIG.6A

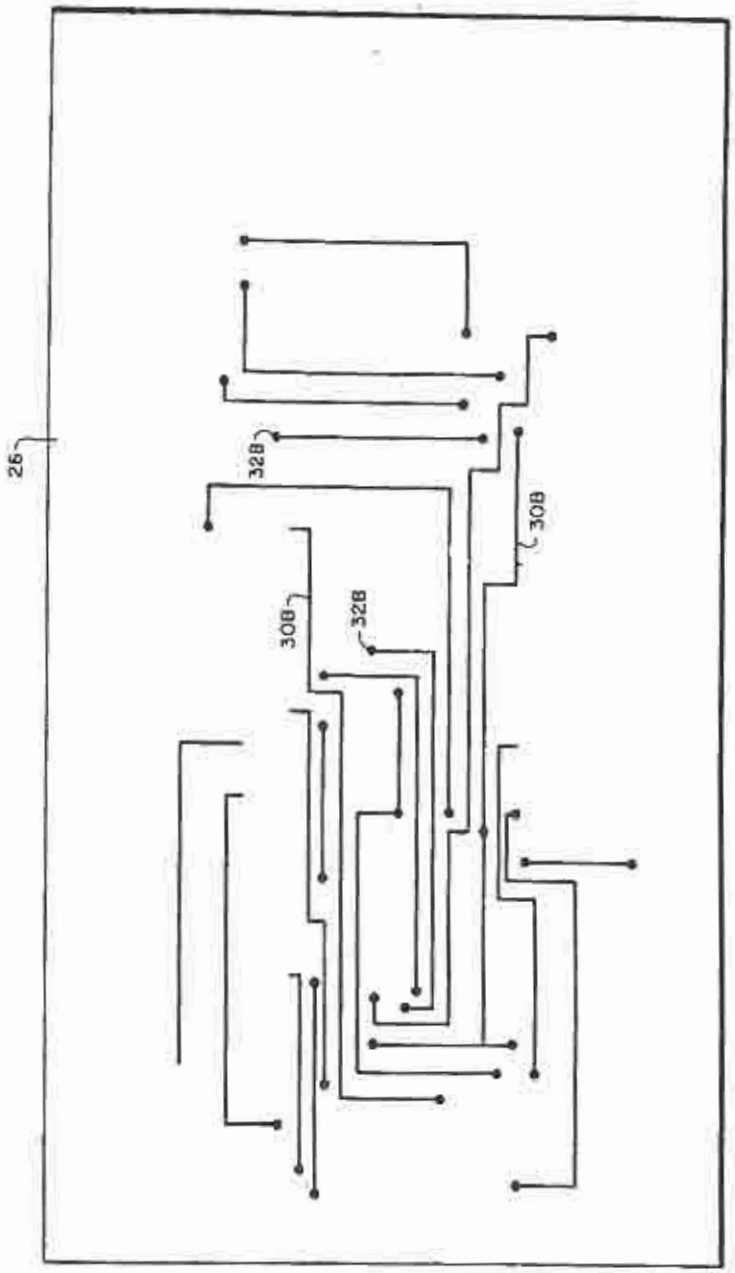
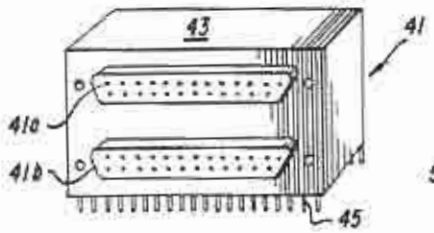


FIG.6B

FIG. 7A



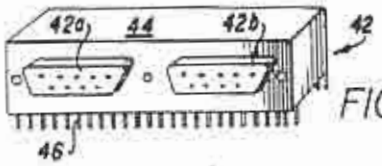


FIG. 7B

FIG. 8A

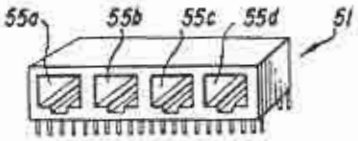


FIG. 8B

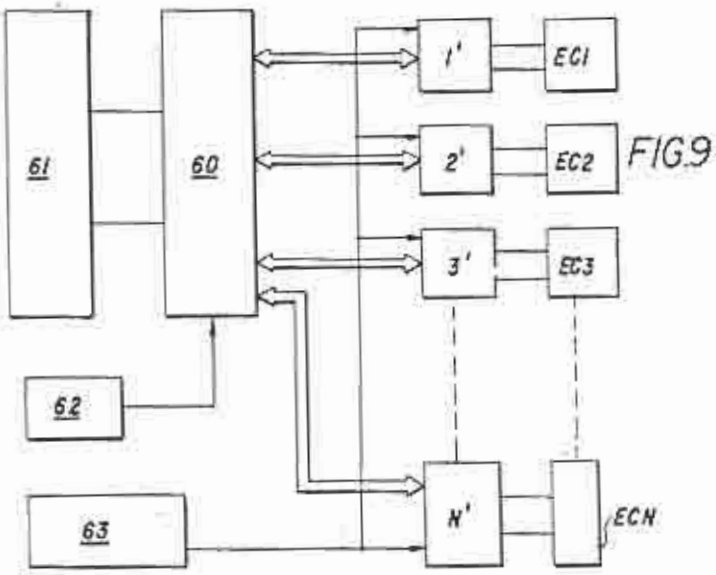


FIG. 9

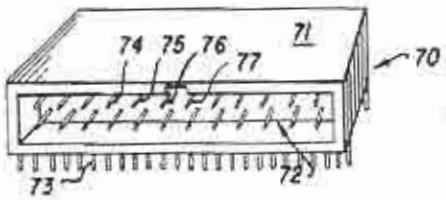


FIG. 10A

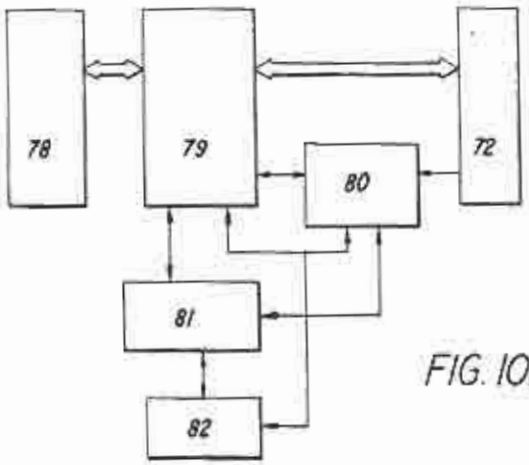


FIG. 10B

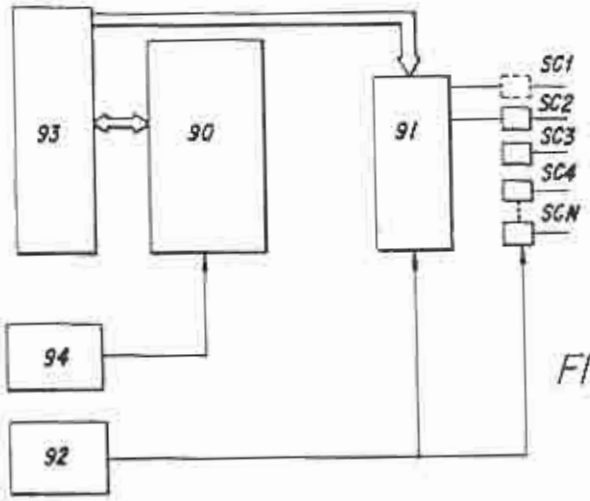


FIG. 11

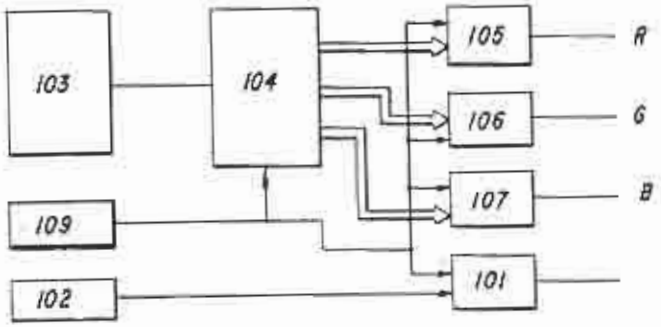


FIG. 12

MULTIPLE CONNECTOR INTERFACE

This is a continuation-in-part of application Ser. No. 484,823 filed April 13, 1983, U.S. Pat. No. 4,603,320.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to electrical connectors, and particularly to a connector having internal circuitry capable of providing a specified electrical interface between various types of data handling equipment.

2. Description of the Prior Art

The proliferation of digital data processing equipment, first in business and now into the home, has created an ongoing demand for such equipment with ever increased capabilities but at an affordable price. The modern trend to integrate numerous discrete electrical components within single semiconductor integrated circuits or "chips", has provided for greater economies in the manufacture of digital electronic equipment. Not only is the overall physical size and weight of the equipment reduced through use of integrated circuit technology, but manufacturing costs also are alleviated in that the price of each integrated circuit used is but a fraction of the total cost represented by all the components it contains.

Digital data processing systems which are in common use today include portions arranged to allow the user to communicate with the system by way of, for example, a terminal or a printer. The user "talks" or provides information to the system through the terminal, and this information is converted into digital data which the system is capable of understanding. After the data is processed by the system which may include some form of computer, a suitable response is transmitted back to the user in digital form and then properly converted into visibly recognizable words or symbols on the screen of the terminal or on a sheet generated by a printer.

Accordingly, it is often necessary to provide cable interconnections between differently located units of a data processing system to allow the units to transmit and receive digital data to and from one another.

Certain types of digital equipment, e.g. a terminal or a printer, transmit or receive digital data in serial bit format. That is, each character (i.e., letter or numeral) of the data is sent or received one bit at a time. It will be appreciated that in a typical system where each character occupies multiple bits, communicating the characters as serial bits between separately located pieces of equipment reduces significantly the number of separate conductors which must be provided in the connecting cables, allows for the communicating equipments to operate in time synchronism with one another with regard to the data exchanged between them, as well as for the use of parity bits and other common error detecting techniques to be applied for each data character communicated. Other kinds of equipment in data handling systems operate in a parallel bit format. For example, computers operate on data which is loaded in internal registers one full character (i.e., eight bits) at a time, and likewise provide output information a character at a time to internal output registers.

In order to insure compatability between terminals, printers and other input/output data handling equipment which operate in a serial bit format, and computer

mainframes and related equipment, the Electronic Industries Association promulgated in 1969 a now widely accepted interface standard known as EIA RS-232-C, the provisions of which are incorporated by reference herein. The RS-232-C Standard, entitled "Interface Between Data Terminal Equipment and Data Communication Equipment Employing Serial Binary Data Interchange", ensures that serial bit format equipment produced by one manufacturer will operate properly with serial bit format equipment of another manufacturer. The RS-232-C Standard applies not only to the interchange of information data signals between data handling equipment, but also to the interchange of timing and control data signals between such equipment (Sec. 1.4 of the Standard).

In order to ensure satisfactory noise immunity of the data signals to be communicated over connecting cables, the RS-232-C Standard provides that the data signals transmitted over the cables have magnitudes of at least ±6 volts (See Sec. 2.3 of the Standard). Since most data handling equipment today operate at five-volt levels, the Standard makes necessary additional power supplies for enabling a voltage level conversion of the data signals to be interchanged over the connecting cable.

With regard to mechanical characteristics of the interface, the RS-232-C Standard states that the interface is "located at a pluggable connector signal interface point between the two equipments. The female connector . . . should be mounted in a fixed position near the data terminal equipment". (Sec. 3.1). FIG. 3.1 within the RS-232-C Standard assigns certain circuit functions to each of 25 connector pins associated with the pluggable connector at the signal interface point. While the Standard does not specify a particular type of multiple pin connector (See Appendix I to the Standard), the "D-type" 25 pin connector (for example, AMP type 206584-1) has essentially become an industry standard.

A printed circuit board together with circuit components and software necessary to achieve an RS-232-C interface between a computer terminal on one side, and modems or serial line printers on the other side, is available from a variety of manufacturers. Such boards are mountable inside the computer, and separate cable is provided. These boards are compatible from the RS-232-C side but they differ on the computer side from computer to computer.

The known RS-232-C interfaces which include a printed circuit board are arranged physically as shown in FIG. 1. The board B can be a "stand alone card" and be connected via a card cage connector (not shown) to various parallel signal bus lines associated with a microprocessor in a computer or other terminal equipment (also not shown). Alternatively, it can be a part of a more complex board. The RS-232-C Standard 25-pin connector CON may be mounted along one edge of the board B as shown, and the pins directly connected electrically to printed conductors on the board by soldering as at points S on the underside of the board B. This leaves a female connector part F fixedly mounted near the data terminal equipment as required by the Standard. The various conductors to which the pins of the connector CON are connected lead to electrical circuitry arranged over other portions of the board B, including, for example, a main logic element chip IC 1, line driver IC 3, line receiver IC 4, crystal oscillator OSC, frequency divider IC 2, and a number of discrete components C.

It will be appreciated that the known RS-232-C interface board arrangements require that a certain amount of space be allocated in existing equipment for their insertion, such space often being at a premium in units intended to be portable and of small overall dimensions. As far as is known, there has been no attempt to integrate any electrical interface circuitry, including those components required to implement the RS-232-C interface as shown in FIG. 1, within the prescribed interface connector itself such as the 25-pin connector CON.

A connector is known from U.S. Pat. No. 3,790,858 to Brancaleone et al within which RF filter elements are connected to a number of parallel pin-like contact elements which are supported inside and extend axially through a cylindrical shell. The filter elements are connected internally between the contact elements and a common cylindrical metal ground plate.

SUMMARY OF THE INVENTION

A primary object of the present invention is to provide a connector which exhibits simultaneously both the electrical characteristics and the connector requirements of a specified interface between two different data handling systems or equipments.

Another object of the invention is to provide a method wherein electrical circuitry for carrying out a specified function between two different data handling systems is integrated within a connector housing so as to reduce significantly spatial requirements within equipment associated with the systems.

It is a still further object of the present invention to provide a connector which provides a conversion interface between two data handling systems with a single input from a first data handling system and either identical and simultaneous multiple outputs to the second data handling system or different multiple outputs with selection between the multiple output interfaces.

Another object of the present invention is to provide said connector with multiple conversions between the two data handling systems.

These and other objects, features and advantages of the present invention will become more evident from the following discussion and the drawings.

According to one aspect of the invention, a connector includes a housing having a first set and a second set of terminals extending at least partly through wall parts of the housing to engage corresponding terminals of first and second outside connection means associated with first and second data handling systems, respectively. With an output signal the output set of terminals may be physically separated into multiple interfaces for simultaneous connection to multiple output devices with each device receiving an identical output. Alternatively, multiple conversions between the first and second data handling system is possible with selective switching for the desired interfacing between the first and second set of terminals. Logic interface circuit means is arranged within the connector housing and coupled between the first and second set of terminals. The circuit means operates to convert data signals transmitted to the first set of terminals from the first data handling system in a first type of format into corresponding data signals in a second type of format, and to provide the corresponding data signals in the second type of format to the second set of terminals for transmission to the second data handling system. The circuit means also operates to convert data signals transmitted to the second set of terminals from the second data handling system in a second type of format into corresponding data signals in a first type of format, and to provide the corresponding data signals in the first type of format to the first set of terminals for transmission to the first data handling system. For some applications the conversion of the data signals, as described, is in one direction to an output device.

According to another aspect of the invention, a method of implementing a logical interface to enable communications between a first data handling system in which data signals are arranged in a first type of format, and a second data handling system in which data signals are arranged in a second type of format, includes the steps of providing a connector housing; supporting first and second sets of electrical contact elements on the housing; containing electrical circuitry within the connector housing and connecting the circuitry with the first and the second sets of contact elements by arranging conductors inside the housing; converting by way of the electrical circuitry data signals transmitted to the first set of electrical contact elements in a first type of format from a first data handling system outside the connector housing into corresponding data signals in a second type of format and providing same to the second set of electrical contact elements through the conductors inside the connector housing; and converting by way of the electrical circuitry data signals transmitted to the second set of electrical contact elements in the second type of format from a second data handling system outside the connector housing into corresponding data signals in the first type of format and providing same to the first set of electrical contact elements through the conductors inside the connector housing. With an output only type of application the conversion between formats is in one direction to an output device and can embody a multiple output set of electrical contact elements for simultaneous identical output. Alternatively, either or both of multiple first and second set of electrical contact elements can be selectively switched as required. In this context, the term "multiple" refers also to contact elements which are electronically converted to different interface elements.

The invention will be more clearly understood upon reading the following detailed description of preferred embodiments thereof in conjunction with the accompanying drawing.

BRIEF DESCRIPTION OF THE DRAWING

In the drawing:

FIG. 1 is a perspective view of a conventional serial interface arranged on a portion of a printed circuit board;

FIG. 2 is a perspective view, with parts broken away, showing a first embodiment of a connector according to the present invention mounted on a printed circuit board;

FIG. 3 is a schematic diagram representing electrical circuitry contained in the housing of the connector in FIG. 2;

FIG. 4 is a perspective view of a second embodiment of a connector according to the present invention;

FIG. 5 is a perspective view of a third embodiment of a connector according to the present invention;

FIG. 6A is a top plan view of a printed circuit layout, and the phantom outline of the components, of the electrical circuitry seen in the schematic diagram of FIG. 3; and

FIG. 6B is a bottom plan view of the printed circuit board illustrating the interconnection among the various components.

FIGS. 7A and 7B are perspective views of alternative multiple RS-232C type connectors in accordance with the present invention.

FIGS. 8A and 8B are perspective views of alternative multiple serial communication connectors using RJ-11 type modular jacks.

FIG. 9 is an electrical block diagram schematically showing the logic interface for the connectors of FIGS. 7A, 7B, 8A and 8B.

FIG. 10A is a perspective view of a connector in accordance with the present invention which provides a multiple daisy-chained floppy drive controller interface.

FIG. 10B is an electrical block diagram schematically depicting operation of the connector of FIG. 10A.

FIG. 11 is an electrical block diagram schematically depicting a multiple channel analog to digital converter within a connector of the present invention.

FIG. 12 is an electrical block diagram schematically depicting a multiple channel digital to analog converter within a connector of the present invention with an RGB output.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 2 shows a first embodiment of a connector **10** according to the invention, the connector **10** being mounted on a printed circuit board **12** associated with a data handling system or equipment (not shown) in which data is interchanged in a parallel format. The connector **10** includes a connector housing **14**, portions of which are omitted in FIG. 2 for the purpose of illustrating electrical circuitry **16** mounted in the interior space of the housing **14**. It is preferable that walls of the housing **14** substantially enclose the interior space so as to protect the circuitry **16** contained therein.

As shown in FIG. 2, the housing **14** is in the form of a generally rectangular hollow block and includes a front wall **18**, a part of which projects outwardly to define a first outside connection surface **20** parallel to the inside surface of wall **18**. Housing **14** also includes a bottom wall **22** the outside surface of which defines a second outside connection surface **24**. The outside dimensions of the housing **14**, particularly those of the front wall **18** together with the first outside connection surface **20**, preferably conform to those of a standard socket connector, thereby being adapted to mate with a standard plug connector or corresponding or complementary configuration. For applications in the RS-232-C interface, the housing **14** should conform to the dimensions of the known 25-pin "D type" subminiature connector mentioned earlier. Typical dimensions for the housing **14** thus may be a height H of about 0.5 inches (12.70 mm.), a depth D of about 1.2 inches (30.48 mm.) and a width W of about 2.0 inches (50.80 mm.).

The electrical circuitry **16** includes, in the embodiment of FIG. 2, a carrier in the form of a single printed circuit board or substrate **26** mounted closely adjacent and parallel to the inside surface of the bottom wall **22**. Various integrated circuits and discrete components are mounted on the board **26**, and are electrically connected by soldering, or by other technology, to conductors on one or both sides of the board **26**.

The various "chips" and components shown in FIG. 2 as contained within the connector housing **14** on the board **26**, and represented schematically in FIG. 3, include integrated circuits U1–U6; four tantalum chip capacitors C1–C4; a set of five chip capacitors C5–C9; a quartz crystal Q1; a toroid core transformer TR1 having bifilar wound primary and secondary windings T1–T2 and T4–T6; and a Graetz diode bridge G1. Each of eight conductors L extends from a different one of eight connection points on the printed circuit board **26** (FIG. 2), to corresponding female electrical contact elements or terminals J2–J8 and J20 which extend partly through and are supported in openings in the wall **18**. The outside ends of the female contact elements are exposed at the first outside connection surface **20** to engage corresponding pins of an outside plug connector (not shown). The numbers assigned to the female contact elements J2–J8 and J20 correspond to the pin number-circuit function assignments prescribed in the RS-232-C Standard, mentioned earlier. Further, 24 male electrical contact elements or pins P1–P24 extend in two parallel rows of 12 pins each, downwardly from connection points near the long edges of the board **26** (FIG. 2), to engage openings in printed conductors or a conventional dual in line socket on the outside printed circuit board **12**, at the second outside connection surface **24**.

In accordance with a preferred technique of manufacture, the housing **14**, except for the bottom wall **22**, is molded in one piece; the elements or terminals J2–J8 and J20, as well as the conductors L, being included in the molding operation. Then, the bottom wall **22** and abutting printed circuit board **26** are snapped into position in the housing. By means of localized heating, the bottom wall is fused to the housing so that a completely unitary structure is achieved.

FIG. 3 shows the interconnections between the chips and other electrical components on the printed circuit board **26** contained within the connector housing **14**, together with the female and the male contact elements arranged on the first and the second outside connection surfaces **20**, **24** of the connector **10**, respectively. The circuitry of FIG. 3 is one example of circuitry which functions to provide the electrical characteristics of an RS-232-C interface, but it will be appreciated that different circuitry may be integrated within the connector housing **14** to carry out the same function or other commonly used interfaces including 8-bit Parallel, GPIB (general purpose interface bus- IEEE 488), and Ethernet.

The integrated circuit U1 may be, for example, National Semiconductor type INS 8250A. The circuit U1 serves as a main logic element which handles all data signal interchanges between, e.g., a microprocessor (not shown) which handles data in a parallel bit format and communications equipment (not shown) which sends and receives serial bit data. Circuit U1 contains several programmable registers which determine the communications format and all the necessary information data to perform successfully a two-way data interchange between two data systems of different data formats. Specifically, before sending or receiving any data via an RS-232-C line, a controlling microprocessor (not shown) must load the internal registers with the required commands. The system software contains the following load functions which, when programmed within circuit U1, enable the latter to be used for data communications. The preprogrammed functions are:

1. Baud rate and baud rate factor;
2. Character length;

3. Number of stop bits,
4. Parity enable/disable and parity polarity;
5. Modem control functions; and
6. Additional operational conditions.

Instructions representing the above load functions are transmitted to the circuit U1 from an outside microprocessor (not shown) over data bus lines DO–D7 corresponding to the male contact elements or pins P1–P8 on the second outside connection surface 24 of the connector housing 14 (FIG. 2). The appropriate registers within circuit U1 are selected by the address bus lines A, A1 and A2 (pins P23, P22 and P21), and a write signal ($\overline{WR}$, pin P19) validates the register loadings.

When data characters are transmitted by the outside microprocessor after the foregoing initialization procedure, the circuit U1 performs a parallel-to-serial data conversion. First, the eight-bit parallel data is placed into a transmitter register within circuit U1 which then automatically adds a start bit, followed by the data character bits themselves (least significant first) and the programmed number of stop bits for each character. Also, an even or odd parity bit is inserted prior to the stop bit(s) as defined previously by the system program. The character is then transmitted as a serial data stream on a data output line S_{out} at terminal 11 of the circuit U1. The rate at which the data is shifted out is determined by another previously programmed register within circuit U1. The quartz crystal Q1 coupled to the circuit U1 operates together with a programmable divider within circuit U1 to generate a signal of the appropriate frequency for shifting out the data bits.

The strength or voltage levels of the data bits or signals shifted out from the circuit U1, typically TTL compatible (zero to +5 volts). As mentioned earlier, the RS-232-C Standard requires a stronger signal level so that data can be transmitted over a long cable with the capacity of noise suppression. Accordingly, a line driver circuit U3, e.g., Motorola type MC 1488, is coupled to data output S_{out} and supplementary handshake signals as $\overline{RTS}$ (Request to Send) and $\overline{DTR}$ (Data Terminal Ready) of the circuit U1. When powered by an appropriate power supply, the line driver circuit U3 converts the TTL compatible level (zero to +5 volt) of the serial output from the circuit U1, to a ±12 volt level sufficient to satisfy the RS-232-C Standard. The integral power supply is constructed of a push-pull mode switching scheme, performed by high frequency oscillator derived from U4 (e.g. 4516 B RCA), 74C86 exclusive OR gates (U6 e.g. Nat. Semiconductor), high current power transistors within U5 (75951 e.g. Texas Instruments) Tr1 transformer, G1 diode bridge and C2,C3 tantalum capacitors.

When a serial data bit stream is transmitted to the connector 10 from an outside data handling system, specifically to the female contact elements J3 at the first outside connection surface 20 of the housing 14, the higher voltage level of the bit streams is converted to a TTL compatible (0 to 5 volt) logic level by way of buffer-inverters within circuit U2 (e.g., Motorola type MC 1489 A). Also, high level complementary signals (J5, J6 and J8 are converted down). The serial data is then shifted into a receiver register within the main logic element circuit U1 where the data is converted into a parallel format; however, the start and stop bits and the parity bit are subtracted. Thus, the data is then ready to be sent to the microprocessor or other outside parallel format data system over the data bus lines DO–D7.

The circuit U1 is selected for operation by the microprocessor or other outside parallel data system connected to the pins P2–P24 of the connector 10 by way of a chip select signal ($\overline{CS}$, pin P18). The receiver register within the circuit U1 is selected by a preset combination of the address bus lines (AO, A1, A2; pins P23, P22, P21), and the parallel data is placed on the data bus lines (DO–D7; pins P1–P8) for transmission to the outside microprocessor. A read signal ($\overline{RD}$, pin P20) activates the data reading from the circuit U1 to the microprocessor. Likewise, status information reading procedure can be performed similarly.

There are several control signals, and control and status registers in circuit U1 that determine the bidirectional serial communication procedure. All the necessary signals, including "handshaking", status and command bits, and modem control are included in communications following the preprogrammed functions from the outside microprocessor software.

Those components on the board 16 (FIG.2) which have not been discussed above in detail but appear in the circuitry of FIG. 3 will be recognized and understood by those skilled in the art. A preferred quartz crystal Q1 is Seiko type DS-MGQ, 1.8432 MHz, series resonant. The chip capacitors C1–C4 may be Arco type ACT, tantalum, and the chip capacitors C5–C9 may be Murata type GR40 Y5V. Chip resistors R1–R3 can be Panasonic type ERJ-86CSJ, or alternatively can be thick film resistors deposited on the board 16.

The toroid transformer TR1 preferably is made from a Ferroxcube core type 266CT125, material 4C4. The primary winding is 2×10 turns and the secondary is 2×25 turns, both bifilar.

FIG. 4 shows a second embodiment of a connector 10' according to the invention. The outside dimensions and overall appearance of the connector 10' are generally similar to those of the connector 10 of FIG. 2. Two printed circuit boards or substrates 26'A and 26'B are, however, provided in housing 14' instead of the single board 26 in FIG. 2. Board 26' A extends at the top of the housing 14' parallel to the board 26'B which extends across the bottom of housing 14'. Board 26' B carries 24 pins P1'–P24' on its bottom outside surface 24' for connection directly to an outside circuit board or into a dual-in-line socket. The board 26' A is coupled by leads L' to female contact elements J2'–J8' and J20' which engage an outside plug connector at connection surface 20' of the connector 10'.

FIG. 5 shows a third embodiment of a connector 10" according to the invention. A single, flexible printed circuit board 26" is contained within the connector housing 14". Conductors at one end of the board 26" are directly to the inside ends of female contact elements J2"–J8" and J20" which are arranged to engage an outside plug connector at contact surface 20". Conductors at an opposite end of the flexible board 26" are connected directly to the inside ends of insulation displacement type pins P1"–P24". A cap CP is constructed and arranged to clamp a flat insulated cable (not shown) over pointed ends of pins P1"–P24" so that the pins pierce through the cable insulation to electrically contact corresponding conductors of the flat cable.

It will be appreciated that the connector of the present invention provides a completely self-contained interface unit which eliminates all the inconveniences of designing and realizing a data interface such as the RS-232-C Standard. Particular components no longer need be selected to meet the requirements of the Stan-

dard, voltage level conversions are provided for, and time consuming test procedures and debugging are eliminated. The present connector thus saves engineering effort, development and production time as well as labor costs. Importantly, a considerable space savings is achieved in terminal equipment which would otherwise require means to accommodate a separate interface board.

In order to enable the man skilled in the art to practice this invention in some detail, a complete printed circuit layout is shown in FIG. 6. This layout conforms with the circuitry previously illustrated in schematic form in FIG. 3. The contact areas J2-J8 and J20, which correspond with the respective female contact elements so designated, will be seen in FIG. 6A. Likewise, contact areas P1–P12 (at the near longitudinal edge) and P13–P24 (at the far edge), which correspond with the respective male contact elements bearing the same designation. Capacitors C1–C9, oscillator Q1, and transformer TR1, are seen in phantom outline while resistors R1, R2 and R3 are represented by means of hatch lines. All the other principal elements are shown by means of rectangles suitably labeled. Appropriate wire bonding from the several integrated circuits U1–U6, as well as from the Graetz bridge G1, is shown in FIG. 6A connected to the conductors 30A on the printed circuit board.

It will be noted by the skilled worker that suitably correlated conductors 30B are provided on the lower surface of the printed circuit board 26 (FIG. 6B) so as to make the requisite interconnections among components. The dots 32 sent so-called "vias" between the upper and lower surfaces of board 26.

It will be appreciated that, for the sake of clarity, the depiction of a printed circuit layout for a circuit board 26 to be housed in connector 10 of FIG. 2 is greatly enlarged (approximately 7 times).

In FIGS. 7A and 7B, dual RS-232-C connectors 41 and 42 are shown with each having the data conversion circuitry contained within the respective housings 43 and 44. In FIG. 7A the connector 41 embodies two standard 25 pin "D" connectors 41*a* and 41*b* in stacked configuration with pins 45 extending for connection to a microprocessor. In a different spatial configuration FIG. 7B depicts connector 42 having a side by side configuration of 9 pin "D" connectors 42*a* and 42*b* and pins 46 for connection to a microprocessor.

The connector embodiment 52 in FIG. 8A is similar to the side by side configuration of connector elements shown in FIG. 7B but with modular RJ-11 type jacks 52*a* and 52*b* in place of the "D" connectors. Connector 51 shown in FIG. 8B is a further modification of the connector shown in FIG. 8A wherein four jacks 55*a-d* are provided for a connection interface.

As schematically shown in FIG. 9, external connector elements EC1-n, corresponding to the "D" connectors or RJ-11 jacks, are individually connected to a multiple channel LSI logic element 60 through corresponding line driver/receivers 1'—*n'*. Logic element 60 is in turn connected to bus interface 61 for interfacing with the microprocessor. In order to minimize size requirements whereby the conversion circuitry may be readily contained within the connector housing there is sharing of components. To wit, there is a single multi-channel LSI logic element 60, bus interface 61, oscillator 62, and power conversion unit 63. The size and output of the power conversion unit is determined by the number of output devices since it must be sufficient to drive "n" number of line driver/receivers. Generally, this requires a maximum power output of about 2 watts for every 4 channels. With the state of current technology, multi-channel LSI logic elements have up to 8 channels and accordingly "n" presently ranges up to 8. However it is understood that the present invention is similarly applicable to connectors having LSI elements with multi-channels in excess thereof.

In the connector embodiments of FIGS. 7A, 7B, 8A, 8B and 9, there is a virtual simultaneous operation of multiple channels and accordingly the connector can provide a simultaneous communications linkage between, for example, one processing computer and multiple data destinations.

The connector of the present invention provides a data conversion interface for applications other than communication such as depicted in 10A, 10B, 11 and 12. These latter embodiments exemplify usage of connectors having various contained conversion elements therewithin.

In FIG. 10A connector 70 provides a floppy drive controller interface. Housing 71 contains floppy interface elements 72 and bus interface pins 73. As schematically shown in FIG. 10B four floppy disk drives are daisy chained and connected to the floppy drive controller 70. Dedicated pins SEL 74-77 select one out of the four drives to be active at a time in the multiplexed series. The connector contains the bus interface 78, floppy controller LSI 79, data separator element 80, phase locked loop 81 and quartz oscillator 82. Again the number of floppy drives capable of being controlled by a single connector element is determined by the current state of the art with regard to the capability of the floppy controller LSI and the number of channels it embodies for driving multiple drives.

FIG. 11 schematically shows the internal circuitry for a multiple channel analog to digital converter for use with, for example different signal conditioning elements, for containment within the connector of the present invention. In FIG. 11 various analog signals from signal conditioning elements SC 1—n are individually connected to analog channel selector 91 and power supply 92. Examples of analog signals include temperature, voltage, amperage etc. Microprocessor bus interface 93 is interfaced with both the analog to digital converter 90 and analog channel selector 91 with the latter connection providing requisite direct channel selection as required. Analog conditioned signals pass from the analog channel selector 91 to the analog to digital converter 90 for conversion and transmission to the microprocessor. Oscillator 94 provides the timing for the converter 90 and power supply 92 provides power for the analog channel selector 91. With the multiplexed arrangement, as shown, only one channel at a time is selected for analog to digital conversion.

As shown in FIG. 12 a multiple channel digital to analog converter within a connector of the present invention provides a multiple simultaneous conversion for an analog output to an RGB monitor. FIG. 12 schematically depicts a multiple channel digital to analog convertor for use with, for example an RGB monitor, for containment within the connector of the present invention. Microprocessor bus interface 103 interfaces, with look up tables 104 and digital to analog converters 105–107 for providing an R G B output respectively at the connector output interface for an attached RGB monitor. Sychronizing generator 101, clock 109, and power supply 102 provide the required timing and

power for the multiple simultaneously processed digital to analog signals.

While specific embodiments of the invention have been shown and described in detail to illustrate the application of the inventive principles, it will be understood that the invention may be embodied otherwise without departing from such principles.

I claim:

1. A connector for implementing a direct predetermined logical interface between a first data handling system wherein data signals are arranged in a first type of format, and a second data handling system wherein data signals are arranged in a second type of format, comprising:

a connector housing including a first wall part forming a first outside connection surface and a second wall part forming a second outside connection surface;

a first set of terminals arranged to extend at least partly through said first wall part from inside said connector housing in a given configuration for engaging in contact with corresponding terminals of first outside connection means associated with the first data handling system, with said first set of terminals forming an interface member for matingly engaging a corresponding interface member formed by said corresponding terminals associated with the first data handling system;

a second set of terminals arranged to extend at least partly through said second wall part from inside said connector housing in a given configuration for engaging in contact with multiple corresponding terminals of second outside connection means associated with the second data handling system, with said second set of terminals forming multiple interface members for matingly engaging corresponding interface members formed by said corresponding terminals associated with the second data handling system; and

interface circuit means arranged within said connector housing and coupled between said first set of terminals and said second set of terminals for converting data signals transmitted to at least some of said first set of terminals from the first data handling system in the first type of format into corresponding data signals in the second type of format and providing said corresponding data signals in the second type of format to at least some of said second set of terminals for subsequent transmission to the second data handling system.

2. A connector according to claim 1 wherein data signals transmitted to at least some of said second set of terminals from the second data handling system in the second type of format are converted by conversion means, within said connector, into corresponding data signals in the first type of format and said corresponding data signals in the first type of format are provided to at least some of said first set of terminals for subsequent transmission to the first data handling system.

3. A connector according to claim 2, wherein said interface circuit means comprises means for converting data signals transmitted to at least some of said first set of terminals in a serial format into corresponding data signals in a parallel format and providing the corresponding parallel data signals to at least some of said second set of terminals for multiple simultaneous output, and for converting data signals transmitted to at least some of said second set of terminals in a parallel format into corresponding data signals in a serial format and providing the corresponding serial data signals to at least some of said first set of terminals.

4. A connector according to claim 1, wherein said interface circuit means comprises means for selectively converting multiple analog data signals into corresponding data signals in a digital format.

5. A connector according to claim 1, wherein said interface circuit means comprises means for converting multiple digital data signals into corresponding analog data signals.

6. A connector according to claim 1, wherein said connector provides a multiple daisy chained floppy drive controller interface.

7. A connector according to claim 1 wherein said connector housing has structural dimensions of a height of no more than about 0.5 inches (12.70 mm), a depth of no more than about 1.2 inches (30.48 mm), and a width of no more than about 2.0 inches (50.80 mm).

8. A connector according to claim 1 wherein said connector housing comprises walls forming an enclosure member and wherein said interface circuit means are completely enclosed within the walls of said connector housing.

9. The connector of claim 1 wherein said first set of terminals comprises a number of male contact elements adapted for direct integrated electrical mating with a printed circuit board member which handles data in said first type of format and wherein said housing is adapted to be physically supported by said printed circuit board.

10. The connector of claim 1 wherein said first set of terminals comprises a number of male contact pins adapted for direct integrated electrical mating with an insulated ribbon cable connector member, with said pins being adapted to pierce the insulation of said cable to electrically contact conductors of said cable whereby said electrical mating is effected, said cable connector member being adapted to be electrically connected to a printed circuit board which handles data in a first format and wherein said connector comprises means to physically enclose a portion, of said ribbon cable connector

11. The connector of claim 1 wherein said interface circuit means further comprises a power supply, with said power supply being contained within said walls of said connector housing.

12. A multiple "D-type" RS-232-C connector having a male connection interface adapted for direct integrated electrical mating with a printed circuit board member which handles data in a parallel format, said connecter further having multiple female connection interfaces for mating connection with corresponding external male connection interface members from one or more external devices which handle data in a serial format, characterized in that means for converting data from said parallel format to said serial format and means for converting data from said serial format to said parallel format are electrically positioned between said male connection interface and said female connection interfaces within said connector, and wherein said connector is adapted to be physically supported by said printed circuit board.

13. A multiple "RJ-11" connector having a male connection interface adapted for direct integrated electrical mating with a printed circuit board member which handles data in a parallel format, said connecter further having multiple female connection interfaces for

mating connection with corresponding external male connection interface members from one or more external devices which handle data in a serial format, characterized in that means for converting data from said parallel format to said serial format and means for converting data from said serial format to said parallel format are electrically positioned between said male connection interface and said female connection interfaces within said connector, and wherein said connector is adapted to be physically supported by said printed circuit board.

* * * * *

United States Patent [19]

Farago

[11] Patent Number: 4,972,470

[45] Date of Patent: Nov. 20, 1990

[54] PROGRAMMABLE CONNECTOR

[76] Inventor: Steven Farago, 171 Forest Dr., Mount Kisco, N.Y. 10549

[21] Appl. No.: 83,258

[22] Filed: Aug. 6, 1987

[51] Int. Cl.[5] H04L 9/00

[52] U.S. Cl. 380/3; 380/52; 310/71; 439/189; 364/240.8

[58] Field of Search 380/3, 52; 310/71; 439/189; 364/240.8

[56] References Cited

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Primary Examiner—Thomas H. Tarcza
Assistant Examiner—David Cain
Attorney, Agent, or Firm—Israel Nissenbaum

[57] ABSTRACT

A configurable connector between two or more devices with at least one of the devices being capable of programming the connector through an interface therewith. The connector contains programmable electronic circuitry capable of being instructed by the device whereby the connector assumes a desired connecting configuration and/or function. In one embodiment the connector is programmed to inquire and determine the configuration of the device to which it is connected. With the results of its analysis the connector adapts the necessary timing, pin-outs, voltages, and other parameters to assure proper communication between the connected devices. In other embodiments the connector contains electronic components to add specific functions for data exchange, such as data buffering, data encryption and the like. In addition, the connector is programmable with interchangeable pin designations thereby obviating the need for rewiring for different applications and physical connections.

13 Claims, 4 Drawing Sheets

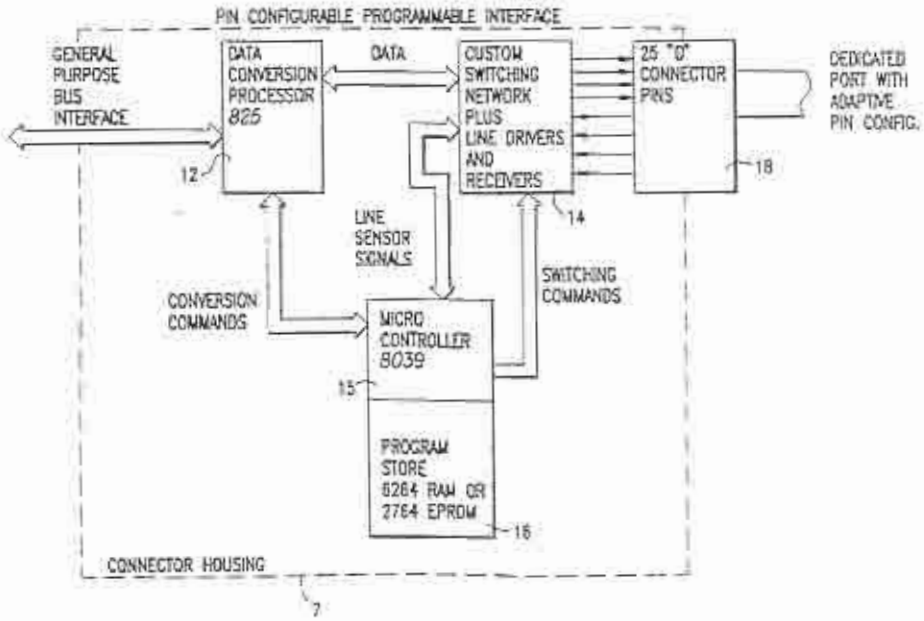

EXHIBIT C

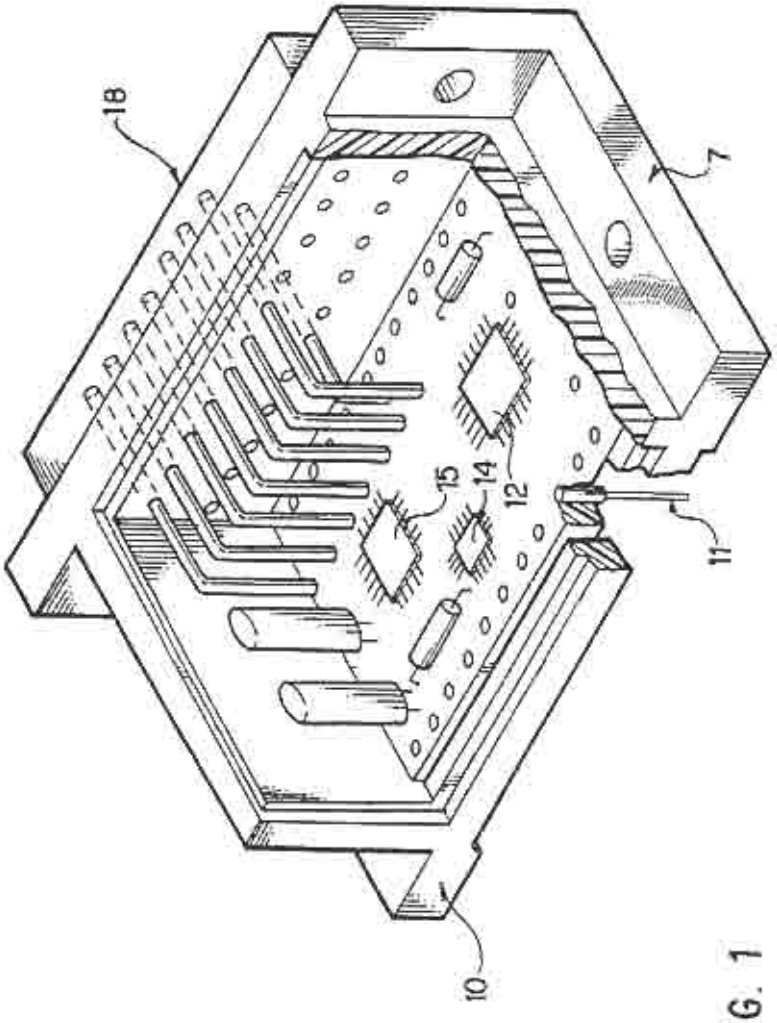

FIG. 1

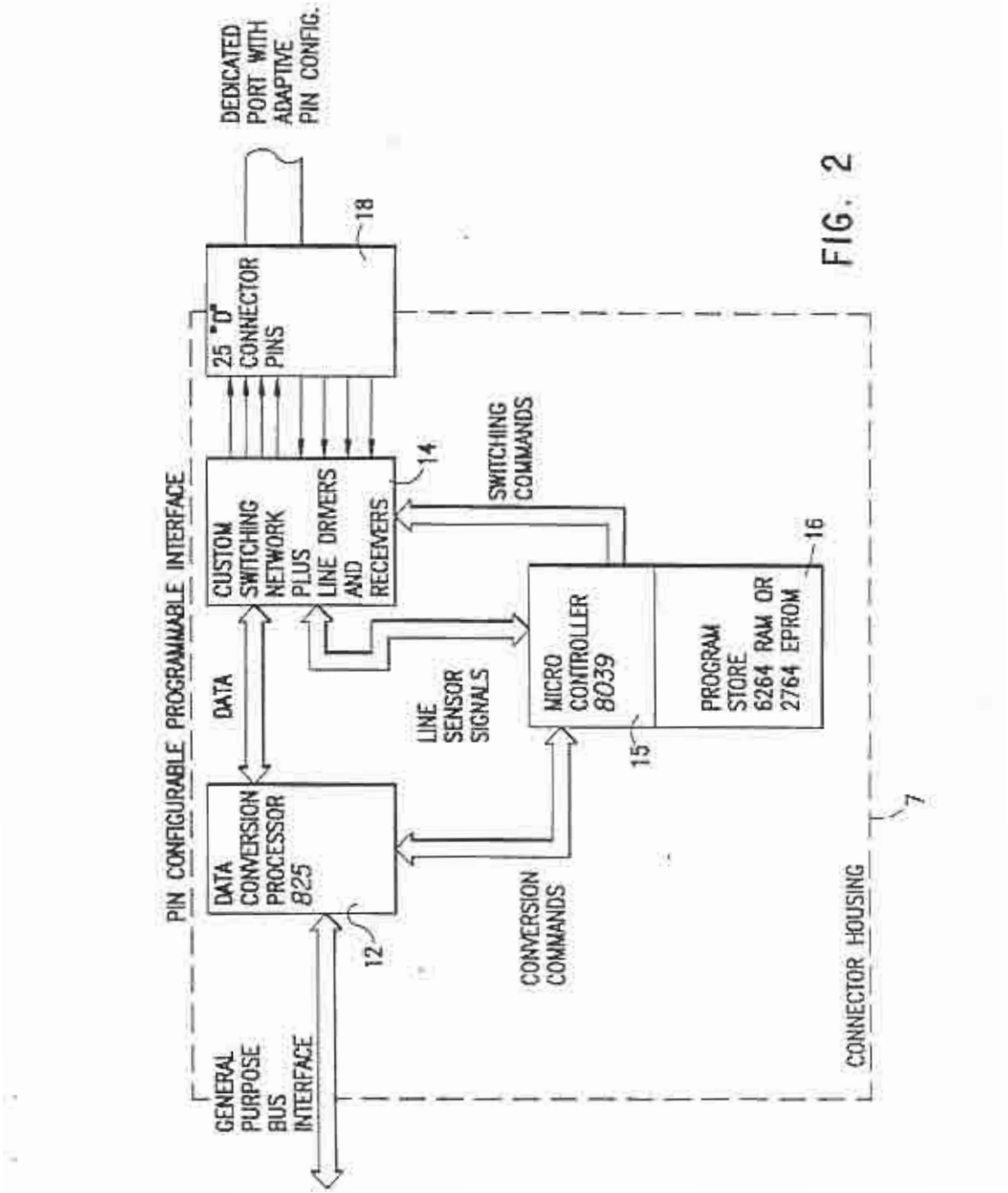
DEDICATED PORT WITH ADAPTIVE PIN CONFIG.
18
25 "D" CONNECTOR PINS
14
CUSTOM SWITCHING NETWORK PLUS LINE DRIVERS AND RECEIVERS
SWITCHING COMMANDS
16
MICRO CONTROLLER 8039
PROGRAM STORE 6264 RAM OR 2764 EPROM
15
DATA
LINE SENSOR SIGNALS
DATA CONVERSION PROCESSOR 825
12
CONVERSION COMMANDS
PIN CONFIGURABLE PROGRAMMABLE INTERFACE
GENERAL PURPOSE BUS INTERFACE
CONNECTOR HOUSING
7

FIG. 2

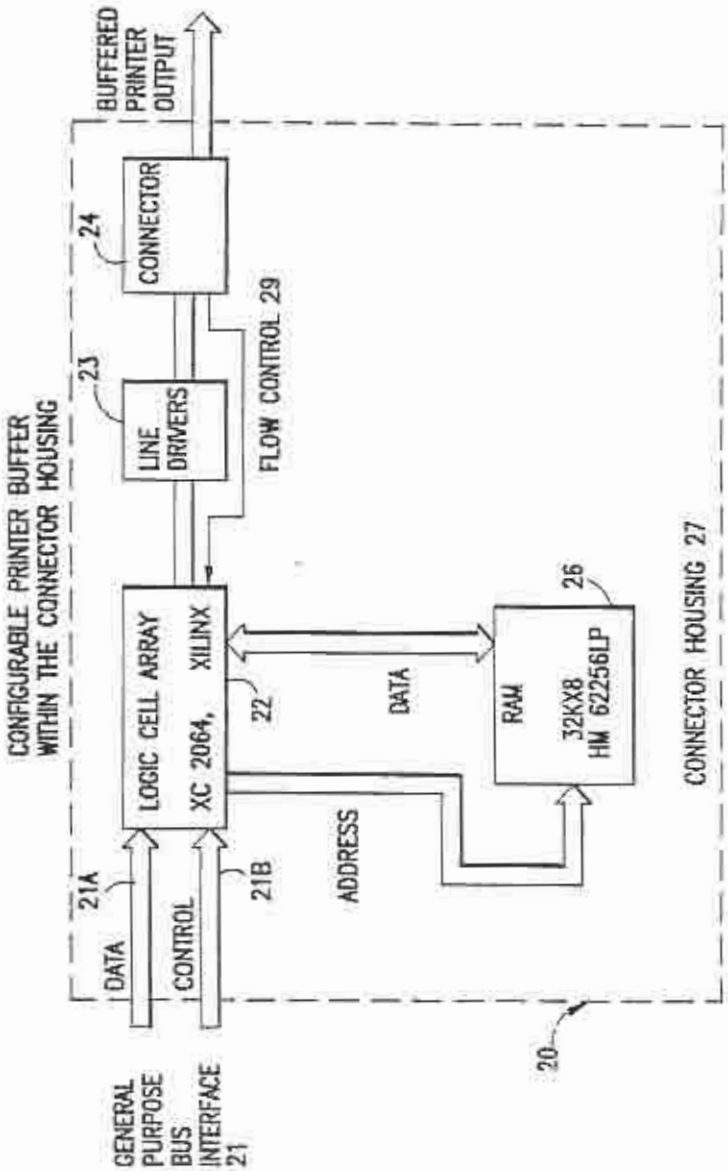
BUFFERED PRINTER OUTPUT
24
CONNECTOR
23
LINE DRIVERS
FLOW CONTROL 29
CONFIGURABLE PRINTER BUFFER WITHIN THE CONNECTOR HOUSING
LOGIC CELL ARRAY XC 2064, XILINX
22
DATA
26
RAM 32KX8 HM 62256LP
CONNECTOR HOUSING 27
21A
DATA
CONTROL
21B
ADDRESS
GENERAL PURPOSE BUS INTERFACE 21
20

FIG. 3a

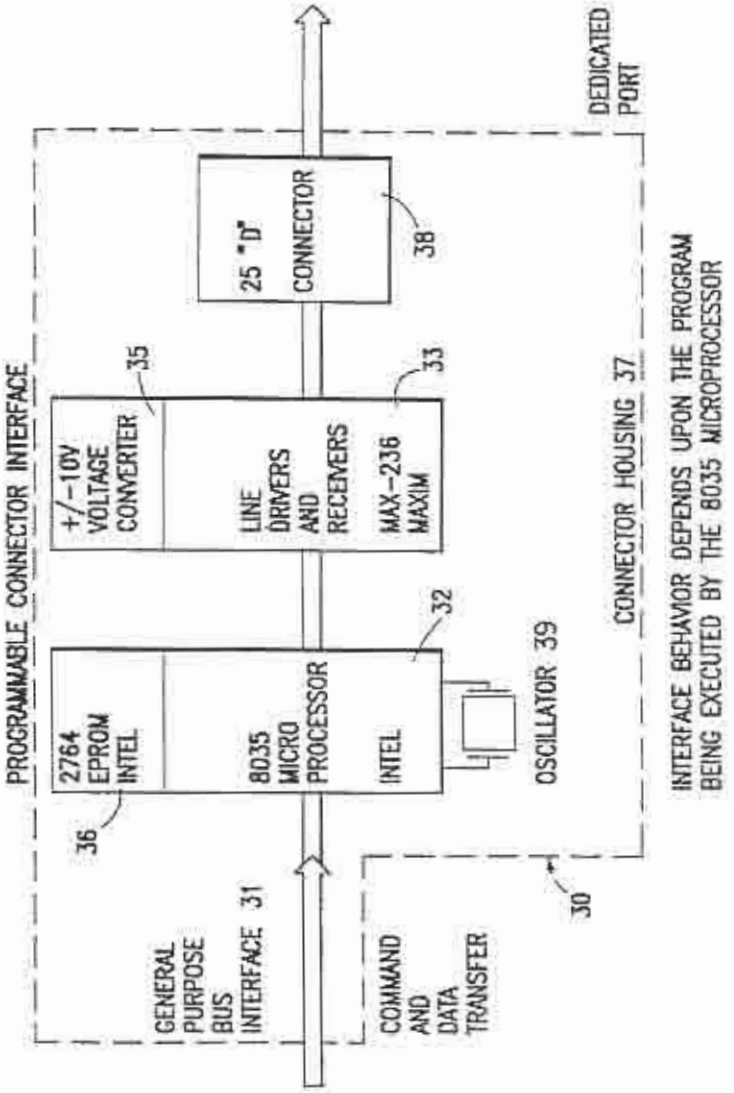
PROGRAMMABLE CONNECTOR INTERFACE
2764 EPROM INTEL
36
8035 MICRO PROCESSOR
INTEL
32
OSCILLATOR 39
+/-10V VOLTAGE CONVERTER
35
LINE DRIVERS AND RECEIVERS
MAX-236 MAXIM
33
25 "D" CONNECTOR
38
GENERAL PURPOSE BUS INTERFACE 31
COMMAND AND DATA TRANSFER
30
CONNECTOR HOUSING 37
DEDICATED PORT
INTERFACE BEHAVIOR DEPENDS UPON THE PROGRAM BEING EXECUTED BY THE 8035 MICROPROCESSOR

FIG. 3b

PROGRAMMABLE CONNECTOR

This invention relates to connectors between devices for the transfer of information therebetween and in particular to the interconnection of computer devices to peripheral devices.

In U.S. Pat. No. 4,603,320, issued on July 29, 1986 and copending application no. 891,190, filed July 28, 1986, a "smart" connector was disclosed wherein the connector contained, within the housing thereof, the requisite electronic circuitry for providing a data conversion between two or more interfaced devices. Such conversions included a conversion between parallel and serial and between analog and digital data formats. These connectors were however limited to a single hard wired-in conversion application. Thus, while they provided an improvement over the common simple electrical current connectors, they were nevertheless limited to a single operative function.

It is an object of the present invention to provide a connector between devices which is capable of being externally programmed or instructed to adapt itself into a desired connecting configuration and/or function between the devices.

It is a further object of the present invention to provide a connector which, when externally activated, is programmed to inquire and determine the requisite connecting function and to reconfigure itself accordingly.

These and other objects, features and advantages of the present invention will become more evident from the following discussion and drawings in which:

FIG. 1 schematically depicts the internal components of a programmable connector in accordance with the present invention;

FIG. 2 is a block diagram showing the program/configuration supplied to the device of FIG. 1; and

FIGS. 3*a*–*b* are block diagrams showing specific programmable connector functions.

Generally the present invention comprises a connector having a housing which contains at least two physical interface connection elements such as electrical pins and socket connections, through the walls thereof, for connection to at least two external devices. The connector further contains, within the housing thereof, programmable means remotely accessible by at least one of said devices whereby instructions are sent to the programmable means whereby the function or configuration of the connector is changed thereby as desired. The programmable means is preferably a general purpose electrical circuitry with or without the ability to erase and reprogram it. The loaded program determines the specific function of the connector and the programming can be performed in several ways. For example, the connector may be one-time programmed. In another embodiment the connector is electrically programmed and later erased for reconfiguration. If desired, the program is either downloaded at every power-on cycle, or reconfigured "on the fly".

A significant feature is the ability of the programmable connector of the present invention to inquire and determine the characteristics of the interfaced devices whereby intelligent firmware can find the right connection without cable swapping or rewiring. In addition, the connector automatically adapts the necessary timing, voltages etc. to ensure a proper connection. A suitable algorithm is incorporated or downloaded and

stored in a non-volatile manner such as an EPROM or by battery backed RAM. In such embodiments a microprocessor with EPROM is located within the connector housing with the EPROM (or factory programmed mask prom/rom) containing the program that performs the desired interface function. Different programs in the EPROM result in different interface functions. Alternatively, there is a programmable logic array inside the connector housing which is for example, one time programmed (PLA) or is RAM based. The RAM based method results in flexibility with the connector being capable of being configured and reconfigured by a simple instruction for changing protocol, parameters or pin-outs. In some embodiments, the external device such as a computer provides for an input means such as a keyboard or a downloading from a storage device which accesses the connector and instructs it to assume the requisite interface function and/or configuration. In other embodiments the connector is programmed to conduct its own inquiries regarding the nature of the connection interface and adapt itself accordingly. In such embodiments the simple act of powering on is considered herein to be an initiation instruction.

Examples of interfaced devices through which interface instructions may be transmitted to the connector include the aforementioned computer with peripheral input devices. Other commonly interfaced devices include modems, printers and the like to which a transmission of data is required. Data input peripherals for such devices as well as hard wired controls can be utilized in properly instructing the connector to assume the requisite interface function and/or configuration.

It is understood that while the functions of pins of a specific interface can be programmed, according to the present invention, to assume a desired electrical connection configuration, the physical characteristics remain unchanged.

In accordance with the present invention several features are embodied within the connector. A programmable and/or configurable device is contained within the housing of the connector. The configurable device is supplied with a program and/or configuration, with the device and the supplied program and/or configuration, performing a specific predetermined function inside the connector. Different programs and/or configurations result in different functions being performed or executed by the connector.

Programmable and/or configurable electronic devices suitable for use within the connector of the present invention include microprocessor chips with program storage memory. Examples of such chips include the Intel 8035, 8049 and 8031 designated chips. The Intel 2764 Eprom is an example of the program storage memory.

A further example of such programmable and/or configurable electronic devices is a microcontroller with downloadable code storage e.g. the Intel 8031 with an 8k x 8 static RAM memory and the Hitachi HM 2-62256. Other examples include programmable array logic (e.g. MMI LCA ZPAL20L8), custom gate array, programmable logic cell array (e.g. XILINK XC-2064 or 2018, MMI LCA M-2064) and erasable programmable logic device (e.g. ALTERA EP-1210 and 1280, and INTEL 5C180).

Various means may be utilized to supply the program or configuration to the programmable or configurable devices. For example, a custom mask is programmed at the manufacturing site and configured into silicon dur-

ing wafer fabrication (ROM principle). Alternatively, the programmable and/or configurable electronic device is one time programmable at the user level by utilizing the fusible link programming method. EPROM technology, as embodied in the 2764 Eprom or Altera EP-1210 parts, is utilizable for electrically programmable and u.v. light erasable devices. A further example is a RAM based configuration storage with downloadable feature, such as the XILINX XC-2064 and the 8031 micro plus 6264 Static RAM. In order to maintain a non-volatile program/configuration an alternative battery backup storage device such as is available from Dallas Semiconductor may be utilized.

Various specific, predetermined programmable functions of the programmable connector of the present invention include:

(a) a user programmable port interface, e.g. serial, parallel, etc;

(b) adaptive pin arrangement via software algorithm and hardware switching network of an input-output structure with the connected device and an algorithm to configure the connector to match the network;

(c) a buffered port interface with the connector providing temporary storage of data to accommodate devices operating at different speeds; and

(d) a data encryption device incorporated in the connector to provide higher levels of security during data transfer.

In accordance with the present invention, different programs installed in the connector can result in different functions of the connector. For example the connector may function as a reconfigurable port whereby one physical hardware interface can change configuration with the same port becoming an RS-232, RS-422, RS-485 protocol or it can even become a Centronic interface. Such configurations and reconfigurations are accomplished by dowaloading the proper configuration into the programmable connector as desired.

With specific reference to the drawings, FIG. **1** depicts a pin configurable programmable interface connector **10** with housing **7** in which are contained a general purpose bus interface **11** extending through one wall of housing **7** and a second dedicated port **18** with an adaptive pin configuration. As schematically depicted in FIG. **2**, connector housing **7** further contains a data conversion processor **12** having a data interface with custom switching network **14** with line drivers and receivers which, in turn, are interfaced with the connector pins **18**. Microcontroller **15** provides switching commands to the switching network **14** and conversion commands to the data conversion processor **12** and receives line sensor signals from the switching network. Microchip **16** contains an EPROM (e.g. 2764 Eprom) or (6264 Static RAM) RAM to provide the requisite programmed and programmable commands.

FIG. **3***a* schematically depicts the electronic configuration of a printer buffer **20** within a connector housing **27**. A logic cell array **22** (XILINX XC-2064) receives data and control commands from a connected device such as a computer with an input device such as a keyboard or storage element such as a disk drive (not shown), through connections **21***a* and **21***b* respectively of the general purpose bus interface **21**. The logic cell array is in turn linked with a 32k x 8 RAM chip **26** (Hitachi HM-62256 type) which it addresses and sends to and receives data from. The logic cell array sends signals to a buffered printer output **24**, via line drivers **23**, which is in turn connected to the printer for the desired output. A flow control **29** is interfaced between the connector output **24** and the logic cell array **22**. In such embodiment the connector may similarly function as a buffer element between a printer and a data transmitting modem. The logic cell array **22** is configured at every "power-up" sequence via the general purpose bus interface **21** to perform the printer buffer function. The configuration accomplishes a hardware data-control path which is responsible for the desired buffering feature.

FIG. **3***b* further schematically depicts a pin configurable programmable connector interface device **30**. A connector housing **37** contains a general purpose bus interface **31** and a **25** pin "D" connector **38** with a dedicated port for connection to external devices. A microprocessor **32** (Intel 8035) sends and receives commands through bus interface **31** and is in turn electrically connected to line drivers and receivers **33**. EPROM **36** (2764 Eprom) provides the requisite program for the microprocessor **32** to execute. Voltage converter (+10 V) **35** provides power for line drivers and receivers **33** and oscillator **38** povides the timing for the microprocessor **32**. The interface behavior of the connector **30** is dependent upon the program being executed by microprocessor **32**. Thus, EPROM **36** can provide a protocol selection program whereby different connection protocols may be selected for a single connector such as serial, and various serial interface standards such as RS-232, RS-422, RS-485, or even a Centronics parallel interface, etc. for a completely compatible connection between interfaced devices. In a particularly useful embodiment, as data is transmitted through the connector, generally from a computer to a modem for retransmission over communication lines, the program causes the data to be encrypted for secured transmission. With a similarly programmed connector at the receiving end, the data is translated into usable form.

It is understood that the above description and drawings are illustrative of the present invention and details contained therein are not to be construed as limitations on the present invention. Variations in programs, components and structural configurations and the like may be made without departing from the scope of the present invention as defined in the following claims.

What is claimed is:

1. An electronically configurable connector, for connecting at least two discrete external electronic devices, said devices having individual housings and said connector having its own housing which contains at least two physical interface connection elements through the walls thereof, wherein, with the connection of one of the physical interface connection elements with a first one of said devices, at least one other of the physical interface connection elements is exposed externally to said first one of said devices for physical electrical connection with another of said devices; characterized in that said devices, when initially physically connected by said connector, do not electronically communicate with each other as desired; and wherein the connector further comprises electrically programmable means, comprising electronic circuitry with a loaded program, said electronic circuitry being remotely accessible by at least one of said connected devices whereby electrical instructions are sent thereto for interpretation by the loaded program, with operational instructions being generated, whereby the electronic circuitry causes modification of the connection between the connected devices to provide the function or configuration of the

connector for communication between the connected devices as desired.

2. The connector of claim 1 wherein said programmable electrically means, after receiving said electrical instructions, causes said connector to function as a printer buffer between a printer, which comprises one of said external devices, and a data transmission device which comprises another of said external devices.

3. The connector of claim 2 wherein said data transmission device comprises a computer.

4. The connector of claim 2 wherein said data transmission device comprises a modem.

5. The connector of claim 1 wherein said electrically programmable means, after receiving said electrical instructions, causes said connector to function as an encryption device for data transmitted between said external devices.

6. The connector of claim 1 wherein at least one of said physical interface connection elements comprises multiple pin outputs and wherein said electrically programmable means, after receiving said electrical instructions, causes said connector to electrically reconfigure itself between said physical interface connection elements whereby the configuration of said multiple pin outputs is reconfigured as desired.

7. The connector of claim 1 wherein said electrically programmable means comprises a microprocessor with program storage memory.

8. The connector of claim 1 wherein said electrically programmable means comprises a microcontroller with downloadable code storage.

9. The connector of claim 1 wherein said electrically programmable means comprises a programmable array logic.

10. The connector of claim 1 wherein said electrically programmable means comprises a custom gate array.

11. The connector of claim 1 wherein said electrically programmable means comprises a programmable logic cell array.

12. The connector of claim 1 wherein said electrically programmable means comprises an erasable programmable logic device.

13. The connector of claim 1 wherein the connector and its housing are external to all of the connected devices.

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