

**IN THE UNITED STATES DISTRICT COURT  
FOR THE EASTERN DISTRICT OF TEXAS  
MARSHALL DIVISION**

PACT XPP TECHNOLOGIES, AG,	§	
	§	Civil Action No. 2:07cv563 (TJW)
Plaintiff,	§	
	§	Hon. T. John Ward
vs.	§	
	§	Assigned to Hon. Chad Everingham
XILINX, INC. & AVNET, INC.	§	
	§	JURY TRIAL DEMANDED
Defendants.	§	
	§	

**FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT**

**I. NATURE OF THE ACTION**

1. Plaintiff PACT XPP Technologies, AG (“PACT”), brings this action against defendants Xilinx, Inc. (“Xilinx”) and Avnet, Inc. (“Avnet”) (collectively, “Defendants”), for patent infringement under the laws of the United States, Title 35, United States Code.

**II. JURISDICTION AND VENUE**

2. This is an action under the laws of the United States, 35 U.S.C. § 101 *et seq.* This Court has subject matter jurisdiction of this action under 28 U.S.C. §§ 1331, 1337 and 1338(a).

3. Venue is proper in this judicial District pursuant to 28 U.S.C. §§1391(b)-(c) and 1400(b) because Defendants Xilinx and Avnet have done business in this District, have committed acts of infringement in this District, and continue to commit acts of infringement in this District, entitling PACT to relief.

**III. PARTIES**

4. PACT alleges all facts herein on information and belief, except those facts concerning the activities of PACT.

5. PACT is a German corporation, with its principal place of business at Muthmannstr. 1, D-80939 Munich, Germany.

6. PACT is the assignee and owner of eleven patents at issue in this action: U.S. Patent Nos. 6,088,795; 6,728,871 B1; 6,119,181; 6,542,998 B1; 5,943,242; 6,859,869 B1; 7,028,107; 6,338,106 B1; 6,513,077 B2; 6,526,520 B1; and 7,237,087 B2. PACT was assigned these eleven patents by the inventors of each of those patents and/or by a predecessor legal entity (PACT GmbH).

7. On information and belief, Xilinx is a Delaware corporation with its principal place of business at 2100 Logic Drive, San Jose, CA, 95124-3400. Xilinx designs, develops and markets programmable logic devices, including field programmable gate arrays (“FPGAs”). Xilinx also provides design services, customer training, field engineering and technical support for its programmable logic devices. Xilinx’s products are designed to provide high integration and quick time-to-market for electronic equipment manufacturers in end markets such as communications, industrial, consumer, automotive and data processing. Xilinx sells its products both directly to customers and through independent distributors, such as Avnet.

8. On information and belief, Avnet is a New York corporation with its principal place of business at 2211 South 47th Street, Phoenix, AZ, 85034. Avnet is one of the largest industrial distributors of electronic components. Avnet distributes Xilinx’s infringing products to customers in the United States and worldwide. Additionally, Avnet provides engineering design services for Xilinx’s infringing products.

#### **IV. CAUSES OF ACTION**

##### **A. INFRINGEMENT OF U.S. PATENT NO. 6,088,795**

9. On July 11, 2000, United States Patent No. 6,088,795 (the “795 patent”) was duly and legally issued for an invention entitled “Process for Automatic Dynamic Reloading of Data Flow Processors (DFPs) and Units with Two or Three-Dimensional Programmable Cell Architectures (FPGAs, DPGAs and the Like).” PACT was assigned the ‘795 patent and

continues to hold all rights and interest in the '795 patent. A true and correct copy of the '795 patent is attached hereto as **Exhibit A**.

10. Defendants have infringed and continue to infringe the '795 patent by the manufacture, use, sale, importation, and/or offer for sale of products and services, including the Virtex and Spartan lines of FPGAs, and by contributing to and inducing others to infringe the '795 patent. Defendants are liable for infringement of the '795 patent pursuant to 35 U.S.C. § 271.

11. Defendants' acts of infringement have caused damage to PACT, and PACT is entitled to recover from Defendants the damages sustained by PACT as a result of Defendants' wrongful acts in an amount subject to proof at trial. Defendants' infringement of PACT's exclusive rights under the '795 patent will continue to damage PACT, causing irreparable harm for which there is no adequate remedy at law, unless enjoined by this Court.

12. Upon information and belief, Defendants' infringement of the '795 patent is willful and deliberate, entitling PACT to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

**B. INFRINGEMENT OF U.S. PATENT NO. 6,728,871 B1**

13. On April 27, 2004, United States Patent No. 6,728,871 B1 (the "'871 patent") was duly and legally issued for an invention entitled "Runtime Configurable Arithmetic and Logic Cell." PACT was assigned the '871 patent and continues to hold all rights and interest in the '871 patent. A true and correct copy of the '871 patent is attached hereto as **Exhibit B**.

14. Defendants have infringed and continue to infringe the '871 patent by the manufacture, use, sale, importation, and/or offer for sale of products and services, including the Virtex and Spartan lines of FPGAs, and by contributing to and inducing others to infringe the

'871 patent. Defendants are liable for infringement of the '871 patent pursuant to 35 U.S.C. § 271.

15. Defendants' acts of infringement have caused damage to PACT, and PACT is entitled to recover from Defendants the damages sustained by PACT as a result of Defendants' wrongful acts in an amount subject to proof at trial. Defendants' infringement of PACT's exclusive rights under the '871 patent will continue to damage PACT, causing irreparable harm for which there is no adequate remedy at law, unless enjoined by this Court.

16. Upon information and belief, Defendants' infringement of the '871 patent is willful and deliberate, entitling PACT to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

**C. INFRINGEMENT OF U.S. PATENT NO. 6,119,181**

17. On September 12, 2000, United States Patent No. 6,119,181 (the "'181 patent'") was duly and legally issued for an invention entitled "I/O and Memory Bus System for DFPs and Units with Two- or Multi-Dimensional Programmable Cell Architectures." PACT was assigned the '181 patent and continues to hold all rights and interest in the '181 patent. A true and correct copy of the '181 patent is attached hereto as **Exhibit C**.

18. Defendants have infringed and continue to infringe the '181 patent by the manufacture, use, sale, importation, and/or offer for sale of products and services, including the Virtex lines of FPGAs, and by contributing to and inducing others to infringe the '181 patent. Defendants are liable for infringement of the '181 patent pursuant to 35 U.S.C. § 271.

19. Defendants' acts of infringement have caused damage to PACT, and PACT is entitled to recover from Defendants the damages sustained by PACT as a result of Defendants' wrongful acts in an amount subject to proof at trial. Defendants' infringement of PACT's

exclusive rights under the '181 patent will continue to damage PACT, causing irreparable harm for which there is no adequate remedy at law, unless enjoined by this Court.

20. Upon information and belief, Defendants' infringement of the '181 patent is willful and deliberate, entitling PACT to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

**D. INFRINGEMENT OF U.S. PATENT NO. 6,542,998 B1**

21. On April 1, 2003, United States Patent No. 6,542,998 B1 (the "'998 patent") was duly and legally issued for an invention entitled "Method of Self-Synchronization of Configurable Elements of a Programmable Module." PACT was assigned the '998 patent and continues to hold all rights and interest in the '998 patent. A true and correct copy of the '998 patent is attached hereto as **Exhibit D**.

22. Defendants have infringed and continue to infringe the '998 patent by the manufacture, use, sale, importation, and/or offer for sale of products and services, including the Virtex and Spartan lines of FPGAs, and by contributing to and inducing others to infringe the '998 patent. Defendants are liable for infringement of the '998 patent pursuant to 35 U.S.C. § 271.

23. Defendants' acts of infringement have caused damage to PACT, and PACT is entitled to recover from Defendants the damages sustained by PACT as a result of Defendants' wrongful acts in an amount subject to proof at trial. Defendants' infringement of PACT's exclusive rights under the '998 patent will continue to damage PACT, causing irreparable harm for which there is no adequate remedy at law, unless enjoined by this Court.

24. Upon information and belief, Defendants' infringement of the '998 patent is willful and deliberate, entitling PACT to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

**E. INFRINGEMENT OF U.S. PATENT NO. 5,943,242**

25. On August 24, 1999, United States Patent No. 5,943,242 (the “‘242 patent”) was duly and legally issued for an invention entitled “Dynamically Reconfigurable Data Processing System.” PACT was assigned the ‘242 patent and continues to hold all rights and interest in the ‘242 patent. A true and correct copy of the ‘242 patent is attached hereto as **Exhibit E**.

26. Defendants have infringed and continue to infringe the ‘242 patent by the manufacture, use, sale, importation, and/or offer for sale of products and services, including the Virtex and Spartan lines of FPGAs, and by contributing to and inducing others’ infringement of the ‘242 patent. Defendants are liable for infringement of the ‘242 patent pursuant to 35 U.S.C. § 271.

27. Defendants’ acts of infringement have caused damage to PACT, and PACT is entitled to recover from Defendants the damages sustained by PACT as a result of Defendants’ wrongful acts in an amount subject to proof at trial. Defendants’ infringement of PACT’s exclusive rights under the ‘242 patent will continue to damage PACT, causing irreparable harm for which there is no adequate remedy at law, unless enjoined by this Court.

28. Upon information and belief, Defendants’ infringement of the ‘242 patent is willful and deliberate, entitling PACT to increased damages under 35 U.S.C. § 284 and to attorneys’ fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

**F. INFRINGEMENT OF U.S. PATENT NO. 6,859,869 B1**

29. On February 22, 2005, United States Patent No. 6,859,869 B1 (the “‘869 patent”) was duly and legally issued for an invention entitled “Data Processing System.” PACT was assigned the ‘869 patent and continues to hold all rights and interest in the ‘869 patent. A true and correct copy of the ‘869 patent is attached hereto as **Exhibit F**.

30. Defendants have infringed and continue to infringe the ‘869 patent by the manufacture, use, sale, importation, and/or offer for sale of products and services, including the Virtex and Spartan lines of FPGAs, and by contributing to and inducing others’ infringement of the ‘869 patent. Defendants are liable for its infringement of the ‘869 patent pursuant to 35 U.S.C. § 271.

31. Defendants’ acts of infringement have caused damage to PACT, and PACT is entitled to recover from Defendants the damages sustained by PACT as a result of Defendants’ wrongful acts in an amount subject to proof at trial. Defendants’ infringement of PACT’s exclusive rights under the ‘869 patent will continue to damage PACT, causing irreparable harm for which there is no adequate remedy at law, unless enjoined by this Court.

32. Upon information and belief, Defendants’ infringement of the ‘869 patent is willful and deliberate, entitling PACT to increased damages under 35 U.S.C. § 284 and to attorneys’ fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

**G. INFRINGEMENT OF U.S. PATENT NO. 7,028,107 B2**

33. On April 11, 2006, United States Patent No. 7,028,107 B2 (the “‘107 patent”) was duly and legally issued for an invention entitled “Process for Automatic Dynamic Reloading of Data Flow Processors (DFPs) and Units with Two- or Three-Dimensional Programmable Cell Architectures (FPGAs, DPGAs, and the like).” PACT was assigned the ‘107 patent and continues to hold all rights and interest in the ‘107 patent. A true and correct copy of the ‘107 patent is attached hereto as **Exhibit G**.

34. Defendants have infringed and continue to infringe the ‘107 patent by the manufacture, use, sale, importation, and/or offer for sale of products and services, including the Virtex and Spartan lines of FPGAs, and by contributing to and inducing others’ infringement of

the '107 patent. Defendants are liable for its infringement of the '107 patent pursuant to 35 U.S.C. § 271.

35. Defendants' acts of infringement have caused damage to PACT, and PACT is entitled to recover from Defendants the damages sustained by PACT as a result of Defendants' wrongful acts in an amount subject to proof at trial. Defendants' infringement of PACT's exclusive rights under the '107 patent will continue to damage PACT, causing irreparable harm for which there is no adequate remedy at law, unless enjoined by this Court.

36. Upon information and belief, Defendants' infringement of the '107 patent is willful and deliberate, entitling PACT to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

#### **H. INFRINGEMENT OF U.S. PATENT NO. 6,338,106 B1**

37. On January 8, 2002, United States Patent No. 6,338,106 B1 (the "'106 patent'") was duly and legally issued for an invention entitled "I/O and Memory Bus System for DFPS and Units with Two or Multi-Dimensional Programmable Cell Architectures." PACT was assigned the '106 patent and continues to hold all rights and interest in the '106 patent. A true and correct copy of the '106 patent is attached hereto as **Exhibit H**.

38. Defendants have infringed and continue to infringe the '106 patent by the manufacture, use, sale, importation, and/or offer for sale of products and services, including the Virtex lines of FPGAs, and by contributing to and inducing others' infringement of the '106 patent. Defendants are liable for its infringement of the '106 patent pursuant to 35 U.S.C. § 271.

39. Defendants' acts of infringement have caused damage to PACT, and PACT is entitled to recover from Defendants the damages sustained by PACT as a result of Defendants' wrongful acts in an amount subject to proof at trial. Defendants' infringement of PACT's



exclusive rights under the '106 patent will continue to damage PACT, causing irreparable harm for which there is no adequate remedy at law, unless enjoined by this Court.

40. Upon information and belief, Defendants' infringement of the '106 patent is willful and deliberate, entitling PACT to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

**I. INFRINGEMENT OF U.S. PATENT NO. 6,513,077 B2**

41. On January 28, 2003, United States Patent No. 6,513,077 B2 (the "'077 patent") was duly and legally issued for an invention entitled "I/O and Memory Bus System for DFPS and Units with Two or Multi-Dimensional Programmable Cell Architectures." PACT was assigned the '077 patent and continues to hold all rights and interest in the '077 patent. A true and correct copy of the '077 patent is attached hereto as **Exhibit I**.

42. Defendants have infringed and continue to infringe the '077 patent by the manufacture, use, sale, importation, and/or offer for sale of products and services, including the Virtex lines of FPGAs, and by contributing to and inducing others' infringement of the '077 patent. Defendants are liable for its infringement of the '077 patent pursuant to 35 U.S.C. § 271.

43. Defendants' acts of infringement have caused damage to PACT, and PACT is entitled to recover from Defendants the damages sustained by PACT as a result of Defendants' wrongful acts in an amount subject to proof at trial. Defendants' infringement of PACT's exclusive rights under the '077 patent will continue to damage PACT, causing irreparable harm for which there is no adequate remedy at law, unless enjoined by this Court.

44. Upon information and belief, Defendants' infringement of the '077 patent is willful and deliberate, entitling PACT to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

**J. INFRINGEMENT OF U.S. PATENT NO. 6,526,520 B1**

45. On February 25, 2003, United States Patent No. 6,526,520 B1 (the “‘520 patent”) was duly and legally issued for an invention entitled “Method of Self-Synchronization of Configurable Elements of a Programmable Unit.” PACT was assigned the ‘520 patent and continues to hold all rights and interest in the ‘520 patent. A true and correct copy of the ‘520 patent is attached hereto as **Exhibit J**.

46. Defendants have infringed and continue to infringe the ‘520 patent by the manufacture, use, sale, importation, and/or offer for sale of products and services, including the Virtex and Spartan lines of FPGAs, and by contributing to and inducing others’ infringement of the ‘520 patent. Defendants are liable for its infringement of the ‘520 patent pursuant to 35 U.S.C. § 271.

47. Defendants’ acts of infringement have caused damage to PACT, and PACT is entitled to recover from Defendants the damages sustained by PACT as a result of Defendants’ wrongful acts in an amount subject to proof at trial. Defendants’ infringement of PACT’s exclusive rights under the ‘520 patent will continue to damage PACT, causing irreparable harm for which there is no adequate remedy at law, unless enjoined by this Court.

48. Upon information and belief, Defendants’ infringement of the ‘520 patent is willful and deliberate, entitling PACT to increased damages under 35 U.S.C. § 284 and to attorneys’ fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

**K. INFRINGEMENT OF U.S. PATENT NO. 7,237,087 B2**

49. On June 26, 2007, United States Patent No. 7,237,087 B2 (the “‘087 patent”) was duly and legally issued for an invention entitled “Reconfigurable Multidimensional Array Processor Allowing Runtime Reconfiguration of Selected Individual Array Cells.” PACT was

assigned the '087 patent and continues to hold all rights and interest in the '087 patent. A true and correct copy of the '087 patent is attached hereto as **Exhibit K**.

50. Defendants have infringed and continue to infringe the '087 patent by the manufacture, use, sale, importation, and/or offer for sale of products and services, including the Virtex and Spartan lines of FPGAs, and by contributing to and inducing others' infringement of the '087 patent. Defendants are liable for its infringement of the '087 patent pursuant to 35 U.S.C. § 271.

51. Defendants' acts of infringement have caused damage to PACT, and PACT is entitled to recover from Defendants the damages sustained by PACT as a result of Defendants' wrongful acts in an amount subject to proof at trial. Defendants' infringement of PACT's exclusive rights under the '087 patent will continue to damage PACT, causing irreparable harm for which there is no adequate remedy at law, unless enjoined by this Court.

52. Upon information and belief, Defendants' infringement of the '087 patent is willful and deliberate, entitling PACT to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

#### **V. WILLFULNESS ALLEGATIONS**

53. Representatives of PACT met and communicated with representatives of Xilinx on multiple occasions between 2001 and 2006. These meetings were conducted under Nondisclosure Agreements and other mutual assurances of confidentiality.

54. Through these meetings and communications, PACT disclosed to Xilinx details of PACT's proprietary technology. PACT specifically disclosed to Xilinx the existence of its issued patents and pending patent applications. It also disclosed to Xilinx certain aspects of PACT's technology not covered by any of PACT's patents.

55. Upon information and belief, despite direct knowledge of PACT's patent portfolio and despite having had PACT's technology explained to it in detail under assurances of confidentiality, Xilinx proceeded to infringe PACT's patents in a willful and deliberate manner.

**VI. JURY DEMAND**

56. PACT demands a trial by jury.

**VII. PRAYER FOR RELIEF**

57. WHEREFORE, PACT requests entry of judgment in its favor and against Defendants as follows:

- a. Declaring that Defendants have infringed U.S. Patent Nos. 6,088,795; 6,728,871 B1; 6,119,181; 6,542,998 B1; 5,943,242; 6,859,869 B1; 7,028,107; 6,338,106 B1; 6,513,077 B2; 6,526,520 B1; and 7,237,087 B2;
- b. Permanently enjoining Defendants, and the respective officers, agents, employees, and those acting in privity with it, from further infringement, contributory infringement and/or inducing infringement of U.S. Patent Nos. 6,088,795; 6,728,871 B1; 6,119,181; 6,542,998 B1; 5,943,242; 6,859,869 B1; 7,028,107; 6,338,106 B1; 6,513,077 B2; 6,526,520 B1; and 7,237,087 B2;
- c. Awarding the damages arising out of Defendants' infringement of U.S. Patent Nos. 6,088,795; 6,728,871 B1; 6,119,181; 6,542,998 B1; 5,943,242; 6,859,869 B1; 7,028,107; 6,338,106 B1; 6,513,077 B2; 6,526,520 B1; and 7,237,087 B2, including enhanced damages pursuant to 35 U.S.C. § 284, to PACT, together with prejudgment and post-judgment interest, in an amount according to proof;
- d. Awarding attorneys' fees pursuant to 35 U.S.C. § 285 or as otherwise permitted by law; and

- e. Awarding such other costs and further relief as the Court may deem just and proper.

DATED: FEBRUARY 16, 2009

Respectfully submitted,

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**CERTIFICATE OF SERVICE**

The undersigned certifies that all counsel of record are being served on this date with a copy of this First Amended Complaint via the Court's ECF/PACER system and/or email.

DATED: FEBRUARY 16, 2009

/s/ John M. Neukom  
John M. Neukom