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Attorneys For Plaintiffs
AGERE SYSTEMS INC.
LSI CORPORATION

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

AGERE SYSTEMS INC., a Delaware corporation, and

LSI CORPORATION, a Delaware corporation,

Plaintiffs,

v.

UNITED MICROELECTRONICS CORPORATION, a corporation organized under the laws of Taiwan, Republic of China, and

UMC GROUP (USA), a corporation organized under the laws of California

Defendants

Case No. _____

COMPLAINT FOR PATENT INFRINGEMENT

DEMAND FOR JURY TRIAL

Plaintiffs Agere Systems Inc. and LSI Corporation (collectively, "Plaintiffs") state the following as their complaint against Defendants UMC Corporation and UMC Group (USA) (collectively, "Defendants").

THE PARTIES

1. Agere Systems Inc. is a corporation organized under the laws of Delaware. Agere Systems Inc. is engaged in the business of designing, developing, marketing, and selling semiconductor products. Agere Systems Inc. is a wholly-owned subsidiary of LSI Corporation.

2. LSI Corporation is a corporation organized under the laws of Delaware with a principal place of business at 1621 Barber Lane, Milpitas, California, 95035. LSI Corporation is engaged in the business of designing, developing, marketing, and selling semiconductor products.

3. On information and belief, UMC Corporation is a corporation organized and existing under the laws of Taiwan, with a principal place of business at No. 3 Li-Hsin 2nd Road, Hsinchu Science Park, Hsinchu, Taiwan. UMC Corporation provides, among other services and products, microchip foundry services to other semiconductor firms, including through its subsidiaries such as, but not limited to, UMC Group (USA).

4. On information and belief, UMC Group (USA) is a corporation organized and existing under the laws of California, with a principal place of business at 488 De Guigne Dr., Sunnyvale, California, 94085. UMC Group (USA) is a wholly-owned subsidiary of UMC Corporation. UMC Group (USA) provides, among other services and products, microchip foundry services to other semiconductor firms through UMC Corporation and UMC Corporation's other subsidiaries.

NATURE OF THE ACTION

5. This is an action for patent infringement.

6. Defendants have infringed and continue to infringe, have actively induced and continue to actively induce others to infringe, U.S. Pat. Nos. 5,149,672, 6,153,543, 5,599,739, and 5,693,561 (collectively, "Plaintiffs' patents").

JURISDICTION AND VENUE

7. This action is for injunctive relief and damages for patent infringement and arises under the United States patent laws (35 U.S.C. §§ 271, *et seq.*). This Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338.

8. Venue is proper in this judicial district under 28 U.S.C. §§ 1391 and 1400(b).

9. On information and belief, Defendants regularly solicit and conduct business in California and within this judicial district and committed, and continue to commit, tortuous acts of patent infringement within and outside of California and this judicial district. This Court has personal jurisdiction over Defendants.

INTRADISTRICT ASSIGNMENT

10. Assignment of the case in this division is appropriate because Intellectual Property cases are assigned on a district wide basis. *See* Civil L.R. 3-2(c).

PLAINTIFFS' PATENTS

11. U.S. Patent No. 5,149,672 ("the '672 patent") entitled "Process for Fabricating Integrated Circuits Having Shallow Junctions" was duly and legally issued to Nadia Lifshitz and Ronald Schutz on September 22, 1992, and has been assigned to Agere Systems Inc. A true and correct copy of the '672 patent is attached as Exhibit A.

12. U.S. Patent No. 6,153,543 ("the '543 patent") entitled "High Density Plasma Passivation Layer and Method of Application" was duly and legally issued to Daniel Chesire, Edward Martin, Jr., Leonard Olmer, Barbara Kotzias, and Rafael Barba on November 28, 2000, and has been assigned to Agere Systems Inc. A true and correct copy of the '543 patent is attached as Exhibit B.

13. U.S. Patent No. 5,599,739 ("the '739 patent") entitled "Barrier Layer Treatments for Tungsten Plug" was duly and legally issued to Sailesh Merchant, Arun Nanda, and Pradip Roy on February 4, 1997, and has been assigned to Agere Systems Inc. A true and correct copy of the '739 patent is attached as Exhibit C.

14. U.S. Patent No. 5,693,561 ("the '561 patent") entitled "Method of Integrated Circuit Fabrication Including a Step of Depositing Tungsten" was duly and legally issued to Sailesh

Merchant, Leonard Olmer, and Ronald Schutz on December 2, 1997, and has been assigned to Agere Systems Inc. A true and correct copy of the '561 patent is attached as Exhibit D.

FACTUAL BACKGROUND

15. As more fully described below, Defendants have been and still are carrying out processes or methods that infringe Plaintiffs' patents, and offering for sale, selling, using, or importing into the United States products made by the processes patented in Plaintiffs' patents, without Plaintiffs' authorization. Such products include microchips and products, systems, and apparatuses that incorporate the microchips. Defendants' infringement has caused and will continue to cause irreparable harm to Plaintiffs unless enjoined by this Court.

16. On information and belief, Defendants without authorization practice processes or methods that infringe the '672 patent, and offer for sale, sell, use, or import into the United States products made by the processes patented in the '672 patent, including, but not limited to, microchips for Novatek, package part number NT7534H; Davicom, package part number DM9331AEP; Trident, package part number SVP-PX58; Matrox, package part number MGA-G450-F; Broadcom, package part number BCM7412; and Xilinx, package part numbers XC3S1400A and XC5VLX50. Defendants' infringement has caused and will continue to cause irreparable harm to Plaintiffs unless enjoined by this Court.

17. On information and belief, Defendants without authorization practice processes or methods that infringe the '543 patent, and offer for sale, sell, use, or import into the United States products made by the processes patented in the '543 patent, including, but not limited to, microchips for Trident, package part number SVP-PX58; and Matrox, package part number MGA-G450-F. Defendants' infringement has caused and will continue to cause irreparable harm to Plaintiffs unless enjoined by this Court.

18. On information and belief, Defendants without authorization practice processes or methods that infringe the '739 patent, and offer for sale, sell, use, or import into the United States products made by the processes patented in the '739 patent, including, but not limited to, microchips for Davicom, package part numbers DM9101FP, DM8203EP, and DM9000BEP; Alpha and Omega

Semiconductor, package part number AOZ80001JI; Novatek, package part number NT7534H; Trident, package part numbers SVPLX7102, SVP-EX52, and SVP-PX58; Matrox, package part number MGA-G450-F; Mediatek, package part number MT1888E; Xilinx, package part numbers XC2S50E, XC2VP2, XC3S50A, XC3S200, SC3S500E, and XC3S700A; and Broadcom, package part number BCM7412. Defendants' infringement has caused and will continue to cause irreparable harm to Plaintiffs unless enjoined by this Court.

19. On information and belief, Defendants without authorization practice processes or methods that infringe the '561 patent, and offer for sale, sell, use, or import into the United States products made by the processes patented in the '561 patent, including, but not limited to, microchips for Davicom, package part numbers DM9101FP and DM9331AEP; Alpha and Omega Semiconductor, package part number AOZ80001JI; Novatek, package part number NT7534H; Trident, package part number SVP-PX58; Matrox, package part number MGA-G450-F; Broadcom, package part number BCM7412; and Xilinx, package part numbers XC3S1400A and XC5VLX50. Defendants' infringement has caused and will continue to cause irreparable harm to Plaintiffs unless enjoined by this Court.

20. On information and belief, Defendants without authorization have been and are actively inducing one or more third parties to infringe Plaintiffs' patents.

21. On information and belief, Defendants' acts set forth above have been willful, wanton, and deliberate. Defendants' continued infringement has caused and will continue to cause irreparable harm to Plaintiffs unless enjoined by this Court.

FIRST CLAIM FOR RELIEF

(Infringement of U.S. Patent No. 5,149,672)

22. Plaintiffs incorporate by reference in this claim for relief the averments contained in the paragraphs above.

23. The acts of Defendants described above constitute direct infringement under 35 U.S.C. § 271(a), inducement of infringement under § 271(b), and infringement under § 271(g) of the '672 patent.

SECOND CLAIM FOR RELIEF

(Infringement of U.S. Patent No. 6,153,543)

24. Plaintiffs incorporate by reference in this claim for relief the averments contained in the paragraphs above.

25. The acts of Defendants described above constitute direct infringement under 35 U.S.C. § 271(a), inducement of infringement under § 271(b), and infringement under § 271(g) of the '543 patent.

THIRD CLAIM FOR RELIEF

(Infringement of U.S. Patent No. 5,599,739)

26. Plaintiffs incorporate by reference in this claim for relief the averments contained in the paragraphs above.

27. The acts of Defendants described above constitute direct infringement under 35 U.S.C. § 271(a), inducement of infringement under § 271(b), and infringement under § 271(g) of the '739 patent.

FOURTH CLAIM FOR RELIEF

(Infringement of U.S. Patent No. 5,693,561)

28. Plaintiffs incorporate by reference in this claim for relief the averments contained in the paragraphs above.

29. The acts of Defendants described above constitute direct infringement under 35 U.S.C. § 271(a), inducement of infringement under § 271(b), and infringement under § 271(g) of the '561 patent.

PRAYER FOR RELIEF

WHEREFORE, Plaintiffs respectfully requests that this Court enter judgment in favor of Plaintiffs, and against Defendants, as follows:

1. That Defendants have infringed, directly or indirectly, and continue to infringe Plaintiffs' patents, and that Defendants induced and continue to induce others to infringe Plaintiffs' patents;

2. That Defendants and any and all persons and entities acting in privity or concert with Defendants or otherwise controlled by Defendants are enjoined against continued infringement of Plaintiffs' patents;

3. That Plaintiffs are awarded their money damages and injuries caused by Defendants' acts;

4. That this case is exceptional, and accordingly the damages awarded Plaintiffs against Defendants be increased three (3) times pursuant to 35 U.S.C. § 284, and that Plaintiffs be awarded their reasonable attorneys' fees and their costs pursuant to 35 U.S.C. § 285;

5. That Plaintiffs are awarded pre-judgment and post-judgment interest on any and all money damages awarded to Plaintiffs; and

6. That Plaintiffs are awarded such other relief as the Court may deem just and proper.

DEMAND FOR JURY TRIAL

Plaintiffs demand a trial by jury as to all claims and all issues in this Complaint.

Respectfully submitted,

DATED: January 15, 2009 By: Spencer Ririe

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LSI Corporation

EXHIBIT A

US005149672A

United States Patent [19]

Lifshitz et al.

[11] Patent Number: 5,149,672

[45] Date of Patent: Sep. 22, 1992

[54] **PROCESS FOR FABRICATING INTEGRATED CIRCUITS HAVING SHALLOW JUNCTIONS**

[76] Inventors: **Nadia Lifshitz**, 1591 Longhill Rd., Millington, N.J. 07946; **Ronald J. Schutz**, 14 Upper Warren Way, Warren, N.J. 07060

[21] Appl. No.: **754,361**

[22] Filed: **Aug. 29, 1991**

Related U.S. Application Data

[63] Continuation of Ser. No. 617,464, Nov. 19, 1990, which is a continuation of Ser. No. 226,917, Aug. 1, 1988, abandoned.

[51] **Int. Cl.**[5] **H01L 21/44**

[52] **U.S. Cl.** **437/189**; 437/192; 437/190; 437/194; 148/DIG. 20

[58] **Field of Search** ..... 437/189, 192, 190, 194; 148/DIG. 20, DIG. 26

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,887,993	6/1975	Okada et al.	437/160
4,486,946	12/1984	Jopke, Jr. et al.	437/177
4,597,167	7/1986	Moriya et al.	437/187
4,624,864	11/1986	Hartmann	437/193
4,845,050	7/1989	Kim et al.	437/192

FOREIGN PATENT DOCUMENTS

267730	5/1988	European Pat. Off.	437/192
0181571	10/1984	Japan	437/189
0219945	9/1987	Japan	437/192
2181456	4/1987	United Kingdom .	

OTHER PUBLICATIONS

N. E. Miller and I. Beinglass, *Solid State Technol.*, 25(12) 85 (1982).

E. K. Broadbent and C. L. Ramiller, *J. Electrochem. Soc.*, 131, 1427 (1984).

E. K. Broadbent and W. T. Stacy, *Solid State Technol.*, 49(12), 51 (1985).

M. L. Green and R. A. Levy, *Semicon East 1985 Technical Proceedings*, 57 (1985).

M. L. Green and R. A. Levy, *J. Electrochem. Soc.*, 132, 1243 (1985).

G. E. Georgiou, et al., *Tungsten and Other Refractory Metals for VLSI Applications II*, E. K. Broadbent, Editor, p. 225, MRS, Pittsburgh, Pa. (1987).

N. Lifshitz et al. *Tungsten and Other Refractory Metals for VLSI Applications III*, V. A. Wells, Editor, p. 225, MRS, Pittsburgh, Pa. 1988.

VLSI Technology, 2nd Edition, edited by S. M. Sze, McGraw-Hill, 1988, p. 364.

Materials Research Society Symposia Proceedings, 18, 89 (1982).

P. B. Ghate, et al, *Thin Solid Films*, 53, 117 (1978).

M. Maenpaa, et al, *Proceedings of the Symposium on Thin Film Interfaces and Interactions*, 80-2, 316 (1980).

M. L. Hammond, *Introduction to Chemical Vapor Deposition*, Solid State Technology, Dec. 1979, p. 61.

J. F. O'Hanlon, *A User's Guide to Vacuum Technology*, Wiley, New York, 1980, (Table of Contents).

Handbook of Thin Film Technology, S. M. Sze, ed. Maissel and Clang McGraw-Hill, New York, 1970.

Sze, supra, Chapters 4, 9.

Rana et al., "Thin layers of TiN and Al as glue layers for blanket tungsten deposition", 1987 Material Research Soc., pp. 187-195.

VLSI Science & Technology—1984, Proc. of 2nd Int. Symp. on VLSI Science and Technology May 6-11, 1984, Electrochem. Soc., Pennington, N.J., pp. 404-419.

Primary Examiner—Brian E. Hearn

Assistant Examiner—Tuan Nguyen

[57] **ABSTRACT**

For integrated circuit devices with strict design rules, junctions defining the source and drain are typically more shallow than 0.25 μm and are made through vias having an aspect ratio greater than 1.1. Suitable electrical contact to such a shallow junction is quite difficult. To ensure an appropriate contact, an adhesion barrier layer such as titanium nitride or an alloy of titanium and tungsten is first deposited. Tungsten is then deposited under conditions which produce a self-limiting effect in a prototypical deposition on silicon. Additionally, these tungsten deposition conditions are adjusted to higher rather than lower deposition temperatures. Subsequent deposition of aluminum if desired, completes the contact.

6 Claims, 1 Drawing Sheet

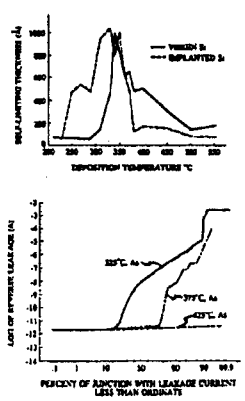


FIG. 1

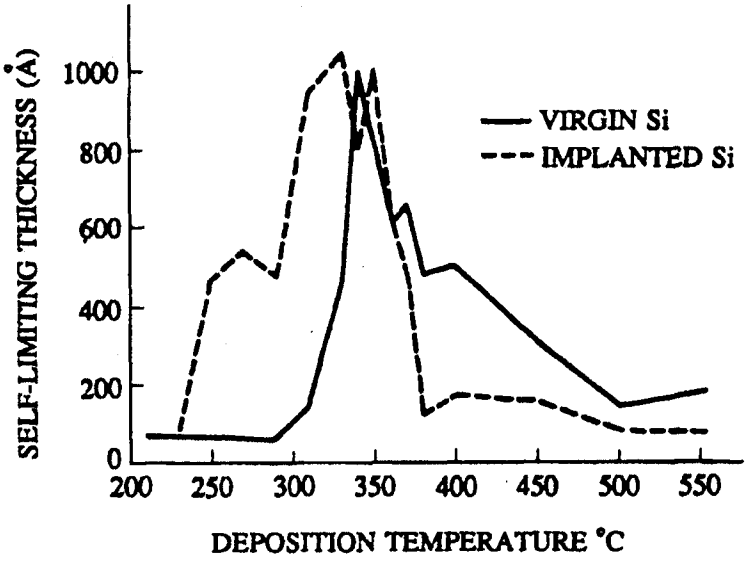
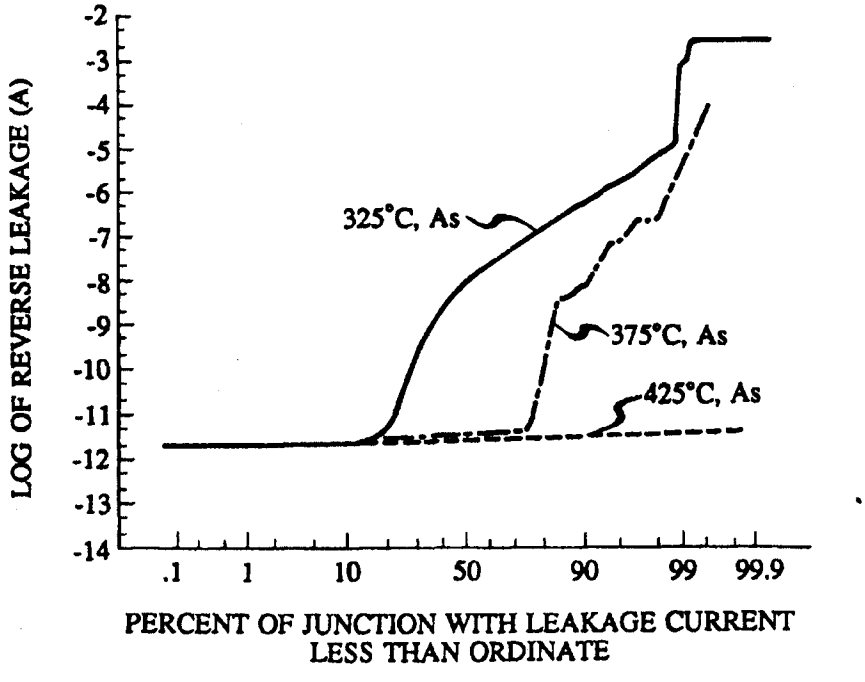

SELF-LIMITING THICKNESS (Å)
1000
800
600
400
200
0
200
250
300
350
400
450
500
550
VIRGIN Si
IMPLANTED Si
DEPOSITION TEMPERATURE °C

FIG. 2


LOG OF REVERSE LEAKAGE (A)
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
-13
-14
.1
1
10
50
90
99
99.9
325°C, As
375°C, As
425°C, As
PERCENT OF JUNCTION WITH LEAKAGE CURRENT LESS THAN ORDINATE

PROCESS FOR FABRICATING INTEGRATED CIRCUITS HAVING SHALLOW JUNCTIONS

This application is a continuation of application Ser. No. 07/617,464, filed on Nov. 19, 1990 which is a continuation of Ser. No. 07/226,917, filed Aug. 1, 1988 (now abandoned).

BACKGROUND OF THE INVENTION

1. Technical Field

This invention relates to integrated circuit manufacture and, in particular, manufacture of integrated circuits having shallow junctions.

2. Art Background

In the manufacture of integrated circuits, electrical contact to junctions such as the source and drain of field effect transistors is required. For these devices desirable electrical properties include a junction contact resistance less than 10 ohms and a junction leakage current less than 10^{-7} amps/cm^2. Complexities inherent in strict design rules make satisfaction of these requirements significantly more difficult. (The device design rule is the smallest lateral dimension for all features within the device circuit.) For example, since the source and drain junctions are typically no deeper than 0.25 μm at submicrons design rules, any undesirable chemical reaction with the junction induced by the fabrication process quickly destroys it. Additionally, electrical contact is made through an opening in an overlying dielectric to the underlying junction region, e.g., drain or source junction region. Typically, as a consequence of strict design rules, this opening (via) has a high aspect ratio, i.e., greater than 1.1. (Aspect ratio is defined as the thickness of the dielectric at the junction divided by the effective diameter of the via at the junction, i.e., the diameter of a circle having the same area as the via at the junction.) To contact the junction through a high aspect ratio opening requires deposition of a conductive material that conforms to or fills the opening so that the conducting cross-section in the via is adequate to maintain an acceptably low current density and contact resistance. Thus, in summary, to ensure a suitable contact, undesirable chemical reaction with the junction should be avoided while a coating that conforms to or fills the via should be produced.

Generally, it is desirable to utilize aluminum as the electrically conductive contact material because of its high conductivity, etchability, excellent adhesion to silicon oxide, and nominal cost. However, direct deposition of aluminum to produce a suitable coating in a via that has an aspect ratio greater than 1.1 has not been reported. Thus, the simplicity and desirable characteristics of direct aluminum deposition is not available.

Other contact materials have been investigated. For example, the deposition of tungsten by a low pressure chemical vapor deposition (LPCVD) technique has been reported. (See, for example, N. E. Miller and I. Beinglass, *Solid State Technol.*, 25 (12), 85 (1982), E. K. Broadbent and C. L. Ramiller, *J. Electrochem. Soc.*, 131, 1427 (1984), and E. K. Broadbent and W. T. Stacy, *Solid State Technol.*, 49(12), 51 (1985). This technique has the advantage of allowing deposition into vias that have aspect ratios greater than 1.1. However, there is a substantial undesirable interaction between the junction (including a silicide overlying the silicon) and chemical entities introduced during deposition of the tungsten. (See, for example, M. L. Green and R. A. Levy, *Semicon East* 1985 *Technical Proceedings*, 57 (1985), M. L. Green and R. A. Levy, *J. Electrochem. Soc.*, 132, 1243 (1985), G. E. Georgiou et al, *Tungsten and Other Refractory Metals for VLSI Applications II*, E. K. Broadbent, Editor, page 225, MRS, Pittsburgh, PA, 1987, and N. Lifshitz et al, *Tungsten and Other Refractory Metals for VLSI Applications* III, V. A. Wells, Editor, page 225, MRS, Pittsburgh, PA, 1988.) Under certain conditions this interaction is self limiting. That is, the amount of junction silicon consumed during the deposition reaches a maximum value that depends on the reaction conditions. Despite this self-limiting effect, the damage produced is still too extensive for junctions, such as source and drain junctions, shallower than 0.25 μm. Additionally, the adhesion between the deposited tungsten material and the dielectric material, e.g., silicon dioxide, is not entirely desirable. Thus, although tungsten under appropriate conditions produces a conformal coating, this coating still produces a device with unacceptable characteristics.

SUMMARY OF THE INVENTION

It is possible through the use of specific expedients to utilize a deposition of tungsten from tungsten hexafluoride to form an acceptable shallow junction contact through a high aspect ratio via. In particular, before tungsten deposition a layer that promotes adhesion between tungsten and silicon dioxide should be deposited. Suitable layers include titanium nitride and alloys of titanium and tungsten. These layers are perceived as barriers to diffusion of tungsten entities. Nevertheless, unless the subsequent tungsten deposition using tungsten hexafluoride is done under appropriate conditions, suitable electrical properties are not obtained.

A self-limiting reaction during deposition from tungsten hexafluoride is required despite the presence of a material considered a barrier to tungsten diffusion. Even more surprisingly, appropriate conditions for tungsten deposition are discernible utilizing a controlled experiment involving silicon without such a barrier layer, and improved yield is generally obtained at higher, rather than the expected lower, deposition temperatures.

Appropriate conditions for tungsten deposition are determined by reference to results achieved when deposition is done directly on a prototypical silicon substrate implanted with the same total dose used in the device ultimately to be manufactured. The deposition for producing the desired contact to a shallow junction is performed under conditions that produce a suitable self-limiting effect when deposition is induced on a silicon substrate. The tungsten deposition further 1) should be performed in a temperature range between 250° C. and 600° C. and 2) in this range an appropriate temperature should preferably be determined by noting the self-limiting thickness as deposition temperatures increase.

After a suitable tungsten deposition has been performed, it is possible, if desired, to increase the thickness of the metallization by depositing an overlying metal, such as aluminum directly on all the deposited material or onto the deposited material remaining after removal of tungsten on lateral surfaces. The combination of an adhesion layer, a tungsten layer deposited under appropriate conditions, and, if desired, an overlying metal layer, such as aluminum, produces juctions having a contact resistance less than 10 ohms, and a junction leakage current less than 10^{-7} amps/cm^2.

BRIEF DESCRIPTION OF THE DRAWING

FIGS. 1 and 2 illustrate properties involved in the invention.

DETAILED DESCRIPTION

The processing of integrated circuits has been extensively discussed in the literature. Suitable conditions for producing structures having shallow junctions, i.e., junctions shallower than 0.25 μm, with overlying dielectric regions are discussed, for example, in *VLSI Technology*, 2nd Edition, edited by S. M. Sze, McGraw-Hill, 1988, page 364. Conventional methods are suitable for making the via through the overlying dielectric region. Generally, techniques such as reactive ion etching or plasma etching are utilized. The inventive process is useful for making contact through a via having an aspect ratio greater than 1.1 to any shallow junction including transistor source and drain—structures typically including a silicide region overlying a silicon region.

A layer is first deposited to ensure adequate adhesion between subsequently deposited layers and the dielectric. For dielectrics such as a silicon oxide, e.g., silicon dioxide, an appropriate adhesion layer includes compositions previously believed to be barriers to diffusion of tungsten entities. These compositions encompass materials such as titanium nitride or titanium/tungsten alloys. Conventional methods of depositing these layers are acceptable. Typically, processes such as magnetron sputtering for titanium nitride and for tungsten/titanium alloys as described in *Materials Research Society Symposia Proceedings*, 18, 89 (1982) and by P. B. Ghate et al, *Thin Solid Films*, 53, 117 (1978) respectively are useful. Generally, the adhesion layer should have a thickness (measured on large lateral device surfaces) in the range 100 to 1500 Å. Layers thinner than 100 Å are not desirable because they lack reliable continuity, while thicknesses greater than 1500 Å are not desirable because they unacceptably complicate subsequent processing such as etching. The composition and structure of suitable titanium nitride or titanium/tungsten alloys are extensively described in papers such as M. Maenpaa et al, *Proceedings of the Symposium on Thin Film Interfaces and Interactions*, 80-2, 316 (1980).

Tungsten is then deposited by LPCVD using a precursor composition including tungsten hexafluoride and a reducing agent such as hydrogen. The conditions utilized for this deposition are important. Generally, the deposition substrate should be heated to temperatures in the range 250° C. to 600° C. Temperatures less than 250° C. lead to inadequate deposition rates while temperatures greater than 600° C. lead to undesirable interdiffusions in the structure being formed and/or in other device structures present on the wafer being processed.

The precise conditions suitable for the tungsten deposition vary with reactor design. Appropriate conditions are determined by performing a control sample in the desired deposition apparatus utilizing 1) a precursor composition including only tungsten hexafluoride and argon and 2) a bare silicon prototype wafer that has been subjected to an implant dose equivalent to the total implant dose that is ultimately to be employed in the device. Conditions should be chosen such that a self-limiting effect with a self-limiting thickness smaller than the junction thickness is achieved on the silicon prototype wafer in the 250° C. to 600° C. temperature range. (The self-limiting effect is characterized by a tungsten formation rate at 10 minutes that is less than 10% of the initial equilibrium rate. The self-limiting thickness is the tungsten thickness under these conditions achieved at 10 minutes.) For example, when a hot wall, e.g., tube reactor (see, M. L. Hammond, *Introduction to Chemical Vapor Deposition*, Solid State Technology, Dec. 1979, p. 61), is employed with tungsten hexafluoride and argon, the self-limiting thickness vs. temperature is shown in FIG. 1. Similarly, when a cold wall reactor (see, Hammond Supra) is utilized in the temperature range 250° C. to 600° C. no self-limiting effect is observed and thus under these conditions this reactor should not be employed. (A proposed mechanism for this phenomenon is that the presence of hot elemental tungsten induces the desired self limitation. The self-limiting effect does not occur in the absence of hot (above 400° C.) tungsten, e.g., where in-situ generation of tungsten does not occur or where hot elemental tungsten is not otherwise introduced. Indeed, the presence of a substantial amount of elemental tungsten on the wafer before deposition decreases the self-limiting thickness.)

Within the desired temperature range generally one extremum in self limiting thickness is observed. Beyond the extremum the higher the temperature, typically, the smaller the self-limiting thickness. This is contrary to what typically would be expected from general trends of increased reactivity and diffusion with higher temperatures. A temperature should be chosen so that the self-limiting thickness is less than the junction depth and so that the deposition rate is adequate. Typically, beyond this junction thickness limit, the thinner the self-limiting thickness the higher the device yield. The temperature should preferably be chosen such that the device yield of working test junctions decreases no more than 10% compared to the yield obtained for the same junction having a via aspect ratio of 0.75 and with a contact of only aluminum. (A test junction is an identical structure to the junction being contacted in the device but with no surrounding device structures and with suitable leads or contact pads for making electrical measurements.) If a range of temperatures yields approximately the same self-limiting thickness on the prototype wafer, the lowest of these temperatures should preferably be employed for device fabrication since lower temperature processing is generally preferred. However, temperatures below the self-limiting thickness extremum (and above 250° C.) although no precluded yield slower deposition and are not preferred.

The determination of suitable temperatures for a given deposition procedure is exemplified in FIG. 1. To increase yield, it is desirable to perform the inventive fabrication processes at temperatures of approximately 425° C. where the self-limiting thickness is at a relatively minimum value. Since the self-limiting thickness does not decrease significantly, in this example, above 425° C. and since for processing reasons unrelated to self-limiting thickness it is generally desirable to deposit at lower temperatures, 425° C. is a preferred temperature for this example.

In one embodiment, deposition of tungsten is performed in a hot wall reactor utilizing a gas composition including a tungsten hexafluoride flow in the range 40 to 200 sccm and a reducing gas, e.g., hydrogen flow, in the range 500 to 2000 sccm with a total pressure in the range 0.2 to 1 Torr. (The addition of other gases is not precluded.) The thickness of the deposited tungsten should typically be in the range from 2000 Å to 0.6 times the via effective diameter. Thicknesses less than

2000 Å yield unacceptably high contact resistance or current densities while thicknesses greater than 0.6 times the via effective diameter lead to difficulties in subsequent processing. In any case, the maximum thickness of the final metallized region should not be greater than the minimum lateral dimension of a metallized region in the device.

It is possible, if desired, to deposit a further metallic material. It has been found advantageous to utilize aluminum as this material. Aluminum deposition such as magnetron sputtering described in J. F. O'Hanlon, *A User's Guide to Vacuum Technology*, Wiley, N.Y., 1980 and *Handbook of Thin Film Technology*, S. M. Sze, ed. Maissel and Glang, McGraw-Hill, New York, 1970 is typically employed. Total metal thickness should not exceed the limit discussed above. The final metallic contact is then patterned to produce the desired device configuration by conventional lithographic processes such as described in Sze, supra, Chapter 4.

The following examples are illustrative of conditions useful in the inventive process.

EXAMPLE 1

Sixteen wafers having a 3500 Å thick thermal SiO_2 dielectric with vias of various sizes were processed. The active junctions were first formed on the wafers by depositing 300 Å of cobalt using a sputtering process as described in Sze, supra, Chapter 9. The cobalt was sintered at 450° C. for 90 minutes to form cobalt monosilicide in the vias. Elemental cobalt present on the SiO_2 was selectively removed by immersing the wafer in a 16:1:1:2 by volume mixture of phosphoric acid, nitric acid, glacial acetic acid and dionized water. This monosilicide was implanted with arsenic using an ion implanter with a 100 KeV acceleration voltage and a total dose of 5×10^{15} cm^{-2}. Cobalt disilicide was formed by annealing the wafers at 700° C. in argon for 30 minutes. (For another description of this process see Hillenius et al., Abstract 10-5, IEDM 1986.) The implanted arsenic was then driven into the silicon substrate at 800° C. for 120 minutes in hydrogen. Subsequently, a 1 μm thick silicon dioxide layer was deposited by LPCVD in a tetraethoxysilane environment. The conditions utilized for this deposition were a deposition substrate temperature of 730° C. and gas flow of 480 SCCM of N_2 together with the vapor pumped from over liquid TEOS to yield a total chamber pressure of 580 mTorr. Holes having various aspect ratios ranging from 1.25 to 0.2 were then formed through the silicon dioxide to the underlying cobalt silicide using standard lithographic techniques and a reactive ion etching procedure. Approximately 1000 Å of titanium nitride was deposited on the wafers by the magnetron sputtering. This procedure was performed with 1) a substrate temperature of 80° C., 2) RF voltage of 150 V and a DC power of 2 KW and 3) a 10:1 by volume flow of Ar and N_2 yielding a total pressure of 2.2×10^{-2} Torr.

The 16 wafers were positioned in the deposition boat, of a hot wall reactor. The boat had provision for holding 40 parallel wafers in a vertical plane. The wafers being processed were positioned in slots number 5 through 21 spaced approximately 1 cm apart and the remaining spaces were occupied with unprocessed silicon wafers having a tungsten coating. A nitrogen flow of 1000 sccm was established in a reactor heated to 300° C. and the boat was put in the deposition position. The nitrogen flow was discontinued and the reactor was evacuated to a pressure of approximately 15 mTorr. The reactor was then brought to a temperature of 325° C. and maintained at this temperature for 15 minutes for thermal stabilization. A flow of 100 sccm of WF_6 and 1000 sccm of hydrogen was introduced to produce a total pressure of 0.2 Torr. This flow was then continued until between 1000 and 2000 Å were deposited on the wafers being processed. After the first deposition, the placement of the wafers in positions 5 through 21 were reversed under nitrogen and a second deposition of tungsten was initiated under the same deposition conditions as the first tungsten deposition. Deposition was continued until the total deposited tungsten thickness was approximately 2500 Å. (The reversal of wafers was done to average any thickness nonuniformities due to the loading effect. Final thicknesses varied no more than 5% between wafers.) The total deposition time was approximately 40 minutes.

Approximately 1 micron of aluminum was magnetron sputtered onto the wafers using an initial cleaning by inducing backsputtering in an RF plasma and then magnetron sputtering in 7 mTorr of Ar at room temperature. The deposited aluminum was then annealed in a tube furnace at 450° C. using a hydrogen ambient. This aluminum layer was patterned to make electrical connections suitable for testing the junctions. The properties of the resulting p-n junctions were measured by applying a reverse bias of 3.5 volts on the device array. (Each wafer had 98 devices with a device occupying an area of approximately 5 μm on a side.) The electrical properties were measured with a Keithley Model 617 Electrometer and Programmable Voltage Source through an automatic wafer probe. Reverse voltage was applied for 5 seconds on each device and 10 readings of the current were taken in rapid succession. The average value was then recorded. The statistical distribution of the measured leakage current is shown in FIG. 2.

EXAMPLE 2

The same procedure as described in Example 1 was followed except the deposition took a total of 32 minutes and was performed at 375° C. The resulting electrical properties are shown in FIG. 2.

EXAMPLE 3

The procedure of Example 1 was followed except a total deposition time of 28 minutes at a temperature of 425° C. was utilized. The resulting electrical properties are shown in FIG. 2.

We claim:

1. A process for fabricating a semiconductor device comprising the steps of treating a substrate by forming a passage through a region overlying a device junction, depositing a material over at least a portion of said region to form an electrical contact to said junction together with an electrical conducting region on the surface of said overlying region and progressing towards completing said device, characterized in that said passage has an aspect ratio of at least 1.1, said junction has a depth shallower than 2500 Å, and said electrical contact and said conductive region on said surface comprises a deposition of 1) a material that presents a barrier to the solid-state diffusion of tungsten and 2) a deposition of tungsten by interaction of said substrate with a deposition comprising WF_6 entities and a reducing agent wherein said substrate is heated to a deposition temperature in the range 250° C. to 600° C. during said tungsten deposition wherein said deposition temperature and environment is controlled such that said

interaction is self-limiting with a self-limiting thickness less than said junction depth and wherein said deposition temperature is chosen such that the yield of said junctions decrease not more than 10% compared to the yield obtained for the same function having a via aspect ratio of 0.75 and having a contact of only aluminum.

2. The process of claim 1 wherein said reducing agent comprises hydrogen.

3. The process of claim 2 wherein said diffusion barrier comprises titanium nitride.

4. The process of claim 2 wherein said diffusion barrier comprises a titanium/tungsten alloy.

5. The process of claim 1 wherein said diffusion barrier comprises titanium nitride.

6. The process of claim 1 wherein said diffusion barrier comprises a titanium/tungsten alloy.

* * * * *

EXHIBIT B

US006153543A

United States Patent [19]

Chesire et al.

[11] **Patent Number: 6,153,543**

[45] **Date of Patent: Nov. 28, 2000**

[54] **HIGH DENSITY PLASMA PASSIVATION LAYER AND METHOD OF APPLICATION**

[75] Inventors: **Daniel P. Chesire**; **Edward P. Martin, Jr.**; **Leonard J. Olmer**; **Barbara D. Kotzias**, all of Orlando; **Rafael N. Barba**, Apopka, all of Fla.

[73] Assignee: **Lucent Technologies Inc.**, Murray Hill, N.J.

[21] Appl. No.: **09/370,422**

[22] Filed: **Aug. 9, 1999**

[51] **Int. Cl.**[7] **H01L 21/4763**; H01L 21/31

[52] **U.S. Cl.** **438/791**; 438/624; 438/787

[58] **Field of Search** 438/763, 787, 438/791, 624

[56] **References Cited**

U.S. PATENT DOCUMENTS

5,716,888	2/1998	Lur et al.	438/619
5,804,259	9/1998	Robles	427/577
5,937,323	8/1999	Orezyk et al.	438/624
5,968,610	10/1999	Liu et al.	427/579

OTHER PUBLICATIONS

Nguyen, S.V., "High-Density Plasma Chemical Vapor Deposition of Silicon-Based Dielectric Films for Integrated Circuits," *IBM Journal of Research & Development*, vol. 43, No. 1/2 (1998). no month.

Primary Examiner—John F. Niebling
Assistant Examiner—Alexander G. Ghyka

[57] **ABSTRACT**

A method of forming a passivation layer over features located on a top layer on a semiconductor device comprises depositing a first void-free layer of a dielectric over the top layer using high density plasma chemical vapor deposition. A second void-free layer can additionally be deposited over the first void-free layer. The first void-free layer can be formed from a silicon oxide, and the second void-free layer can be formed from a silicon nitride. The first void-free layer has a top surface that is disposed at a height higher than the features. The first void-free layer can be applied in two steps. First, the void-free layer is deposited at a D/S ratio between 3.0 and 4.0 to a depth of at least 40% of the feature's height, and then deposited at a D/S ratio of between 6.0 and 7.0.

9 Claims, 1 Drawing Sheet

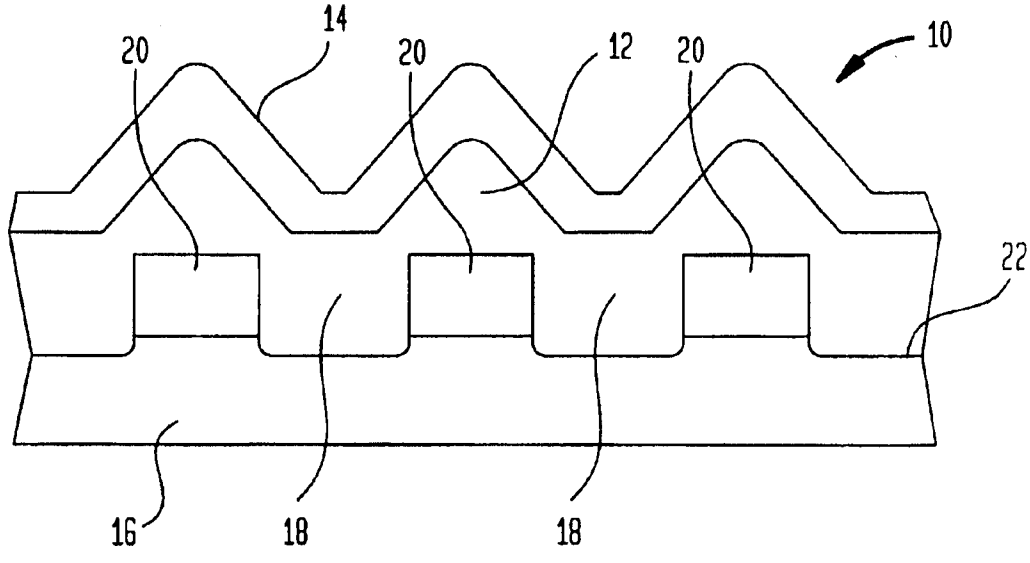


FIG. 1
(PRIOR ART)

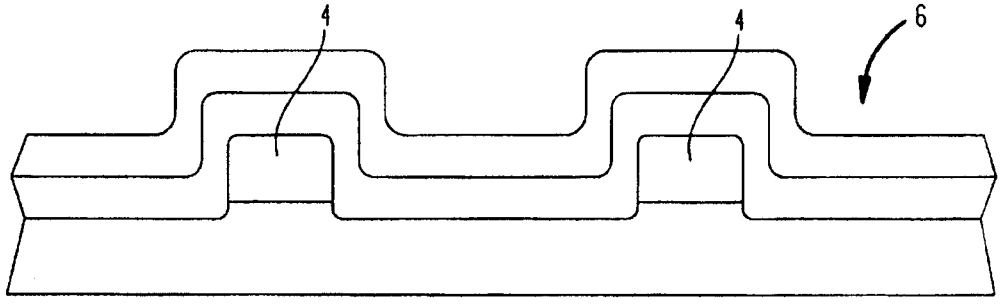


FIG. 2
(PRIOR ART)

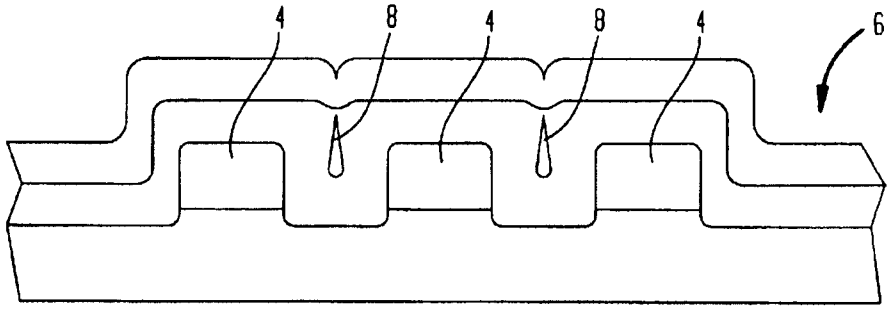
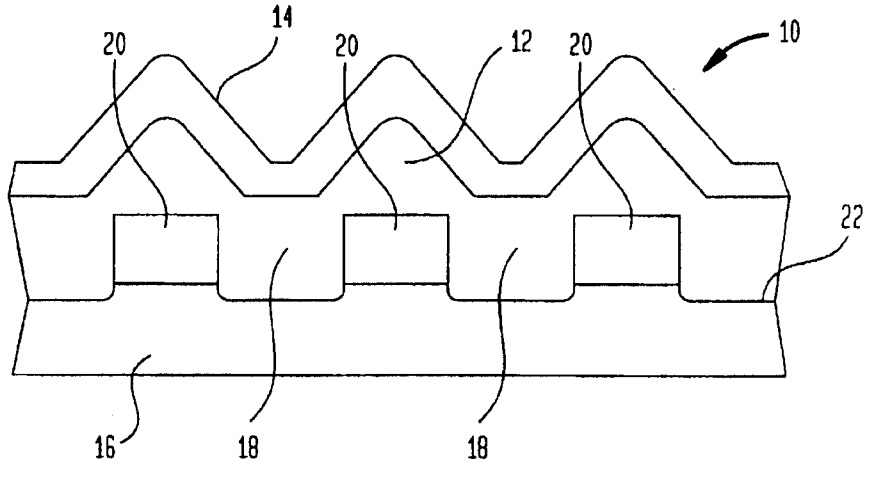


FIG. 3



HIGH DENSITY PLASMA PASSIVATION LAYER AND METHOD OF APPLICATION

CROSS-REFERENCE TO RELATED APPLICATION

Not Applicable

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH AND DEVELOPMENT

Not Applicable

FIELD OF THE INVENTION

This invention relates to the manufacturing of semiconductors. More specifically, the invention relates to a high density plasma passivation layer and method of application that provides a cap over the top layer of a semiconductor device.

BACKGROUND OF THE INVENTION

During the manufacturing of semiconductor devices, layers of dielectrics and metal are added onto a wafer until a final layer of metal is added, hereinafter referred to as the top metal level or layer. Over this top metal layer is typically placed a barrier, passivation or CAPS (Coat and Protective Seal) layer. This passivation layer acts to maintain the mechanical integrity of the semiconductor device, prevent mobile ion diffusion, and provide some radiation protection for the semiconductor device.

Several types of methods for applying passivation layers over a top metal layer have been used in the semiconductor industry. One such passivation level is a bi-layer in which the bottom layer is a silicon dioxide and the top layer is a silicon nitride. The silicon dioxide layer is flexible and acts as a buffer to relieve stress between the silicon nitride and the top metal layer. Thus, this bottom layer reduces the impact of the mechanisms that result in the stress void migration of the metal and also acts as a mechanical protector for the underlying structures. Although the top silicon nitride layer is more brittle, the silicon nitride layer has the advantage of being resistant to moisture and sodium penetration. Additionally, the bi-layer structure inherently eliminates the coincident occurrence of pin-hole defects.

One method of applying the silicon dioxide layer of this particular bi-layer passivation level is to use plasma enhanced chemical vapor deposition (PECVD) with tetraethlorthosilicate (TEOS) chemistry. The use of TEOS chemistry advantageously results in superior film step coverage over the patterned metal-interconnects (runners) of the top metal layer as compared to silicon nitride.

As illustrated in FIG. **1**, the current methods of applying passivation layers **6** are capable of filling the gap between adjacent features **4**, such as the runners, when the distance between the features is large. However, FIG. **2** illustrates a problem with current methods, including TEOS chemistry. This problem is that the gap cannot be filled as the size of features and gaps becomes smaller. These unfilled gaps subsequently become voids **8** in the passivation layer. The existence of these voids can cause reliability problems due to entrapment of gases or liquids in the voids. Also, these voids can act as stress raisers, which can result in inferior mechanical strength of the passivation layer and allow metal interconnects to stress relieve into the voids.

The inferior mechanical strength caused by the voids can be a problem when the chip is removed from the wafer and

pressed into the die assembly or other chip carrier. This pressing of the chip transmits a significant force to the passivation level of the chip. A common result of such a transmission of force is damage to the runners in the top metal layer. This damage can be even more prevalent when the runners have high aspect ratios such that the height dimension is significantly greater than the width dimension. Features having this type of aspect ratio are more susceptible to a force applied in the vertical or transverse direction, which occurs when the chip is pressed. One method of compensating for the voids has been to provide a very thick passivation level. However, a thick passivation level, besides being more costly, does not solve the problems associated with the voids.

Although the previously discussed passivation layer is one type of passivation layer used in the semiconductor industry, other passivation layers are also used. Once such passivation layer is formed from polymers or other plastic-like materials. Passivation layers formed from these plastics suffer from many problems. For example, plastic contains many organic compounds which may contaminate the semiconductor device. Some of these compounds are not stable at the temperatures required for the board solder assembly process. Also, these plastic-like materials tend to absorb excessive moisture, which can also contaminate the semiconductor device and cause device degradation and interfacial damage in a package environment.

A recently introduced process to apply oxides on semiconductor devices is high density plasma chemical vapor deposition (HDP CVD). This process is described by S. V. Nguyen, "High-Density Plasma Chemical Vapor Deposition of Silicon-Based Dielectric Films for Integrated Circuits," in *IBM Journal of Research & Development*, Vol. 43, No. ½ (1998) and is incorporated by reference herein.

HDP CVD has been used to fill and locally planarize high-aspect-ratio (i.e., up to 4:1) sub-half-micron structures. Generally with HDP CVD, ions and electrons are generated by means of an rf power source. Also, a rf biasing power source is applied to an electrode holding the wafer to create a significant ion bombardment (sputter-etching) during deposition. As such, when HDP CVD is used for gap filling, this is a technique in which deposited films are sputtered off by reactive ions and radicals during deposition.

The deposition/sputtering-rate ratio (D/S) is a commonly used measure of the gap-filling capability of the process. This ratio is defined as:

D/S=(net deposition rate+blanket sputtering rate)/blanket sputtering rate.

In general, the use of a lower D/S ratio facilitates the filling of a structure with a higher aspect ratio, but at a lower net deposition rate.

A typical HDP CVD process uses a relatively low pressure of 2–10 mTorr to achieve a high electron density (10^{10}–10^{12} cm^3) and a high fractional ionization rate (10^{-4} to 10^{-1}). As a high film-deposition rate is required for most applications, the process typically uses simple initial reactant gases such as silane, silicon tetrafluoride, and oxygen. Argon is added to raise the sputter rate due to its large mass. To achieve a significant deposition rate while maintaining a reasonably high sputter-etching rate for gap-filling purposes, a significant amount of initial reactant (i.e., deposited species in the plasma) must flow through the reactor. However, the system should be kept at low pressure constantly during deposition to facilitate high sputter rates. Therefore, the vacuum system for such a system typically has a high

pumping capability. Also, the pumping system is generally designed to withstand the high temperature and high reactivity of the reaction by-products while removing them at a high rate. For an HDP CVD system, an advanced turbomolecular pump is generally required to achieve a suitable gap fill rate (at low pressure) and acceptable pumping reliability

As previously stated, the use of HDP CVD of silicon oxide, particularly during high rf biasing gap-fill conditions, produces simultaneous deposition and etching. This result has been used to provide void-free gap fill during the processing of semiconductor devices. Current developments in HDP CVD are working to provide void-free gap fill of high-aspect-ratio (>2:1) sub-half-micron structures. However, these techniques have generally been limited to interlevel insulation, gate conductors, and shallow-trench isolation structures and has not been used to apply a dielectric layer to a top metal layer.

SUMMARY OF THE INVENTION

It is therefore an object of the invention to provide a passivation layer and method of applying the passivation layer capable of filling voids and gaps between closely spaced features such as metal runners disposed on the top metal layer of a semiconductor device.

It is another object of the invention to provide a passivation layer and method of applying the passivation layer that prevents damage of the top metal layer of a semiconductor device from moisture, mobile ions, and radiation.

It is yet another object of the invention to provide a passivation layer and method of applying the passivation layer, the passivation layer providing excellent mechanical protection against mechanical damage during the assembly and plastic encapsulation of the semiconductor device.

It is a further object of the invention to provide a passivation layer and method of applying the passivation layer that places the dominant and transverse stress gradients above the surface of the top metal layer.

These and other objects of the invention are achieved by the subject method which comprises depositing a first void-free layer of a dielectric over the top layer using high density plasma chemical vapor deposition. This passivation layer acts to protect the top layer of the semiconductor device. Additional layers, including a second void-free layer, can also be deposited over the first void-free layer to provide additional protection for the semiconductor device and the top layer.

The first void-free layer is preferably formed from a silicon oxide, and the second void-free layer is preferably formed from a silicon nitride. Also, the first void-free layer has a top surface that is disposed at a height higher than the features. By having the first void-free layer positioned above the features, cracks propagating through layers disposed on top of the first void-free layer will end at a height above the features. This advantageously keeps the stress gradient created by the crack above the level of the features.

The first void-free layer can be applied in two steps. First, the void-free layer is preferably deposited at a D/S ratio of between approximately 3.0 and 4.0 to a depth of at least 40% of the feature's height. In this manner, gaps between the features can be sufficiently filled before the second step. During the second step, the void-free layer is preferably deposited at a higher D/S ratio of between approximately 6.0 and 7.0. This higher D/S ratio allows the void-free layer to be deposited at a higher rate, which increases the thruput of the process.

BRIEF DESCRIPTION OF THE DRAWINGS

There are shown in the drawings embodiments of the invention that are presently preferred, it being understood, however, that the invention is not limited to the precise arrangements and instrumentalities shown.

FIG. 1 shows a prior art passivation layer deposited over a top metal layer of a semiconductor device. The semiconductor device has runners spaced apart so that the gap between the runners has a low aspect ratio.

FIG. 2 shows a prior art passivation layer deposited over a top layer of a semiconductor device. The semiconductor device has runners spaced apart so that the gap between the runners has a high aspect ratio.

FIG. 3 illustrates a passivation layer disposed over a top metal layer of a semiconductor device according to the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. 3, a method for applying a passivation layer on a top metal layer of a semiconductor device, according to the present invention, is illustrated. The passivation layer **10** comprises a first layer **12** over a top layer **16** of the semiconductor device. The top layer **16** of a semiconductor device typically includes metal features **20** extending above the surface **22** of the top layer **16**. Although the features **20** are typically constructed from electrically conductive materials, for example copper, tungsten, or aluminum, the invention is not limited in this regard. The invention can also be used to provide a passivation layer **10** over any feature **20** extending above the surface **22** of a top layer **16**.

The invention is also not limited as to the size or type of feature **20** on the top layer **16** over which the passivation layer **10** will be deposited. In the semiconductor industry, a typical feature **20** disposed on the top layer **16** is a runner. Although the invention is not limited as to the type of feature over which the passivation layer **10** is deposited, feature **20** is hereinafter referred to as runner **20**. Although the runners **20** vary in size, the invention is not limited as to the size of the runner **20** disposed on the top layer **16**. However, runners **20** typically have a height measured in the thousands of Angstroms (Å). In a preferred embodiment, the runners **20** over which the passivation layer **10** will be deposited have a height of approximately 8000 Å.

The dimensions of the gap **18** between adjacent runners **20** are important factors in determining the likelihood of void formation, in particular the aspect ratio of the gap **18** (aspect ratio being defined as the height of the gap divided by the width of the gap). As the aspect ratio increases from <1 to >4, applying a passivation layer **10** over the top layer **16** without forming voids using current techniques becomes increasingly difficult. For example, current techniques of applying a barrier layer **10** creates voids when the gap **18** between runners **20** has a dimension of 4000 Å in width and 8000 Å in height (aspect ratio of 2.0).

The current invention is capable of filling gaps **18** having aspect ratios at least as great as 4.0. Although the absolute width of the gap **18** is currently limited by semiconductor manufacturing techniques, the invention is not limited to a minimum width of the gap **18**. As manufacturing techniques reduce the minimum width of the gap **18**, this invention can still be used to apply a passivation layer **10** over the top layer **16** without the formation of voids.

The passivation layer **10** can perform many functions. These functions can include, but are not limited to acting as a barrier to prevent moisture, mobile ions, and radiation from reaching the top layer **16** and also providing mechanical protection to the top metal layer **20**. It is known in the art

that a passivation layer **10** with such characteristics can be made from many different materials, for example a dielectric, and this invention is not limited as to a particular material or combination of materials.

The presently preferred passivation layer **10** includes an oxide layer. Although the passivation layer **10** can be formed from other oxides, such as an aluminum oxide, the presently preferred passivation layer **10** includes a layer of a silicon oxide. Most preferably, the first layer **12** of the passivation layer **10** is formed from a silicon oxide, specifically silicon dioxide (SiO_2) . An advantage of having the first layer **12** formed from silicon dioxide is that silicon dioxide tends to be compliant. In this manner, the first layer **12** can resist deformation caused by a force being transmitted to the first layer **12**, which could otherwise cause cracks in the first layer **12** and/or damage the underlying top layers **16** and **20** of the semiconductor device.

The passivation layer **10** can also include subsequent layers disposed over the first layer **12**. In a presently preferred embodiment, a second layer **14** is disposed over the first layer **12**. This second layer **14** is preferably formed from a silicon nitride. Although a silicon nitride tends to be brittle, forming the second layer **14** from a silicon nitride has the advantage of providing a moisture, mobile ions, and radiation resistant barrier.

The passivation layer **10** can also be constructed with a nitride layer first and then an oxide layer. An additional nitride layer can then be deposited over the oxide layer to form an nitride-oxide-nitride structure. A oxide-nitride-oxide structure is also possible.

The first layer **12** can be formed using any process that deposits a layer of dielectric material over the top layer **16**. However, the first layer **12** is preferably formed using a HDP CVD process. Advantageously, by using the HDP CVD process, gaps **18** between adjacent features, for example runners **20**, in the top layer **16** of the semiconductor device can be filled without the formation of voids. Voids (as best illustrated in FIG. 2) are formed when other deposition processes, for example TEOS, are used and the aspect ratio (height to width) of the gap **22** between two adjacent features **24** is sufficiently large. However, use of the HDP CVD process can be used to fill gaps **18** having high aspect ratios between adjacent runners **20**.

The invention is not limited as to the variation in D/S ratio during the application of the first layer **12**. For example, the D/S ratio can remain constant during the deposition process. Alternatively, the D/S ratio can be changed multiple times during the deposition process. In a preferred embodiment of the invention, the first layer **12** is applied in two steps. During the first step, the material is deposited using the HDP CVD process and with a relatively small D/S ratio of approximately 3.0–4.0. In this manner, the gap **18** can be at least partially filled. During the second step, the remainder of the material for the first layer **12** is deposited at a higher deposition rate. Although during the second step the material is preferably deposited also using the HDP CVD process, the invention is not limited in this manner. The material could be deposited using other conventional depositing process, for example PECVD TEOS. By using the HDP CVD process for the second step but with a higher D/S ratio, the need to transfer the semiconductor device to another apparatus is advantageously eliminated.

When the HDP CVD process is used to apply the material during the second step, the preferred D/S ratio is approximately 6.0–7.0. By using a higher D/S ratio during the second step than the first step, a higher throughput can be achieved.

The following table illustrates the result of applying the first layer **12** using the aforementioned two-step process. This table shows the effect of varying the depth to which each step deposits the material. For each example, the total depth was approximately 8000 Å of silicon dioxide. The D/S ratio during the first step was 3.0–4.0, and the D/S ratio for the second step was 6.0–7.0. The gap **18** had dimensions of approximately 2100 Å in width and 8000 Å in height.

	Example 1	Example 2	Example 3	D/S Ratio
Step 1 Thickness	4000Å	3000Å	2000Å	3.0–4.0
Step 2 Thickness	4000Å	5000Å	6000Å	6.0–7.0
Result	No Voids	No Voids	Voids	

As illustrated in the table, the creation of voids in the first layer **12** was prevented when the thickness of the material deposited during the first step exceeded approximately 40% of the height of the gap. As a lower D/S ratio indicates a slower deposition rate, the throughput of the semiconductor device can be increased through the HDP CVD process by maximizing the deposition of material at the highest D/S ratio. Thus, to increase the throughput and prevent formation of voids, the presently preferred two-step process deposits the material in the first layer **12** during the first step to approximately a thickness of 40% of the height of the gap **18**.

The deposition of the first layer **12** onto the top layer **16** is not limited to a particular thickness. However, in a preferred embodiment of the invention, the first layer **12** is applied to a thickness at least as great as the height of the runners **20** disposed on the top layer **16**. Applying the material to a height above the runners **20** provides better mechanical protection to the runners **20**. For example, if a second layer **14** was provided above the first layer **12**, and a crack propagated through, the second layer **14**, the crack would end at a height above the runners **20**. Thus, the stress gradient created by the crack would remain above the level of the runners **20**.

It should be understood that the examples and embodiments described herein are for illustrative purposes only and that various modifications or changes in light thereof will be suggested to persons skilled in the art and are to be included within the sprint and purview of this application. The invention can take other specific forms without departing from the spirit or essential attributes thereof for an indication of the scope of the invention.

What is claimed is:

1. A method of forming a passivation layer over features located on a top layer of a semiconductor device, comprising the steps of:

depositing a first void-free layer of a first dielectric over said top layer using high density plasma chemical vapor deposition at a first D/S ratio, and

depositing a second void-free layer of a second dielectric over said first void-free layer at a second D/S ratio, wherein said second D/S ratio is greater than said first D/S ratio.

2. The method according to claim **1**, wherein said dielectrics are at least one selected from the group consisting of silicon dioxide and silicon nitride.

3. The method according to claim **1**, wherein said first D/S ratio is between approximately 3.0 and 4.0 and the second D/S ratio is between approximately 6.0 and 7.0.

4. The method according to claim **1**, wherein the sum of thickness of said void free first and second layers is between approximately 8000 Å to 12000 Å.

5. The method according to claim 1, wherein said first layer is applied with a thickness of at least 40% of the height of said features.

6. The method according to claim 1, further comprising the step of depositing a third void-free layer over said second void-free layer.

7. The method according to claim 6, wherein said third void-free layer is a nitride.

8. The method according to claim 7, wherein said nitride is silicon nitride.

9. The method according to claim 6, wherein the sum of said first void-free layer thickness and second void free layer thickness is between approximately 8000 Å to 12000 Å and said third void-free layer has a thickness of between approximately 2600 Å to 3400 Å.

* * * * *

EXHIBIT C

US005599739A

United States Patent [19]

Merchant et al.

[11] **Patent Number: 5,599,739**

[45] **Date of Patent: Feb. 4, 1997**

[54] **BARRIER LAYER TREATMENTS FOR TUNGSTEN PLUG**

[75] Inventors: **Sailesh M. Merchant**, Orlando, Fla.; **Arun K. Nanda**, Austin; **Pradip K. Roy**, Orlando, both of Tex.

[73] Assignee: **Lucent Technologies Inc.**, Murray Hill, N.J.

[21] Appl. No.: **366,867**

[22] Filed: **Dec. 30, 1994**

[51] **Int. Cl.**[6] **H01L 21/443**

[52] **U.S. Cl.** **437/190**; 437/192; 437/246

[58] **Field of Search** 437/192, 246, 437/190

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,532,702	8/1985	Gigante et al. .	
4,782,380	11/1988	Shankar et al.	357/71
4,804,560	2/1989	Shioya et al. .	
5,143,861	9/1992	Turner .	
5,164,330	11/1992	Davis et al. .	
5,164,333	11/1992	Schwalke et al.	437/200
5,175,126	12/1992	Ho et al.	437/190
5,183,782	2/1993	Onishi et al. .	
5,200,360	4/1993	Bradbury et al. .	
5,202,579	4/1993	Fujii et al. .	
5,232,871	8/1993	Ho	437/190
5,232,873	8/1993	Geva et al. .	
5,233,223	8/1993	Murayama .	
5,244,534	9/1993	Yu et al. .	
5,260,232	11/1993	Muroyama et al. .	
5,312,775	5/1994	Fujii et al. .	
5,327,011	7/1994	Iwamatsu .	
5,332,691	7/1994	Kinoshita et al.	437/192
5,397,742	3/1995	Kim	437/190
5,407,698	4/1995	Emesh .	

FOREIGN PATENT DOCUMENTS

5152292	6/1993	Japan .	
5-347272	12/1993	Japan	H01L 21/28
5-326517	12/1993	Japan	H01L 21/3205
6-275624	9/1994	Japan	H01L 21/3205

Primary Examiner—Robert Kunemund
Assistant Examiner—Matthew Whipple

[57] **ABSTRACT**

Tungsten plugs are formed by passivating a substrate having a contact hole with SiH_4, forming a nucleation layer on the passivated substrate by reducing WF_6 with SiH_4 at relatively low pressures and depositing tungsten to substantially fill the contact hole by reducing WF_6 with H_2 at relatively high pressures. Alternatively, rapid thermal annealing is used to cure pinhole defects in a titanium nitride layer on a substrate to avoid the formation of unwanted tungsten volcanoes.

34 Claims, 4 Drawing Sheets

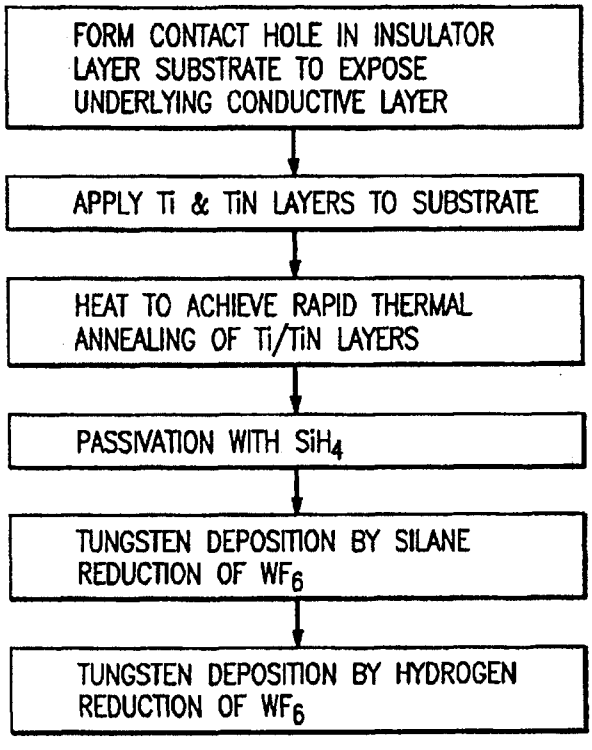


FIG. 1A
(PRIOR ART)

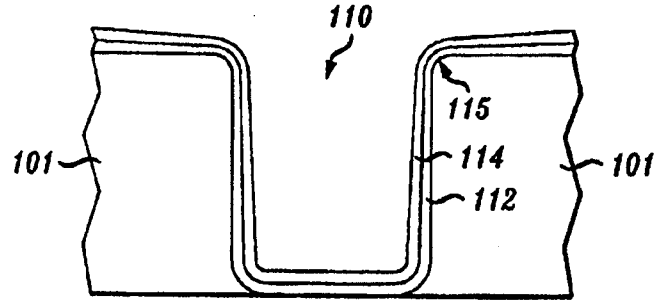


FIG. 1B
(PRIOR ART)

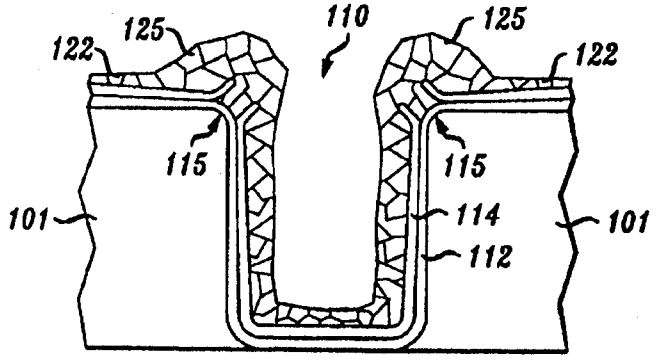


FIG. 1C
(PRIOR ART)

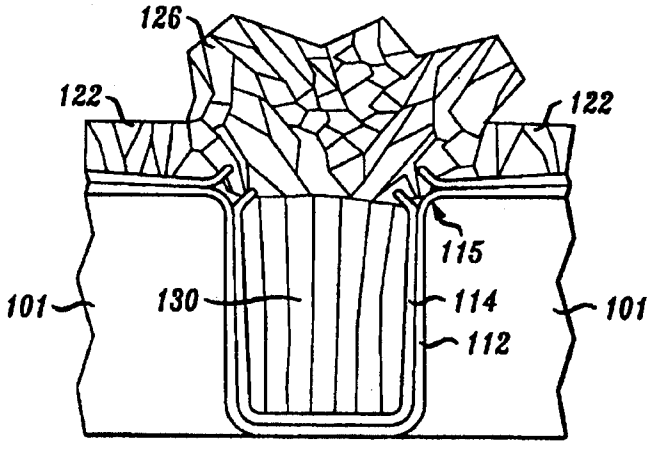


FIG. 2

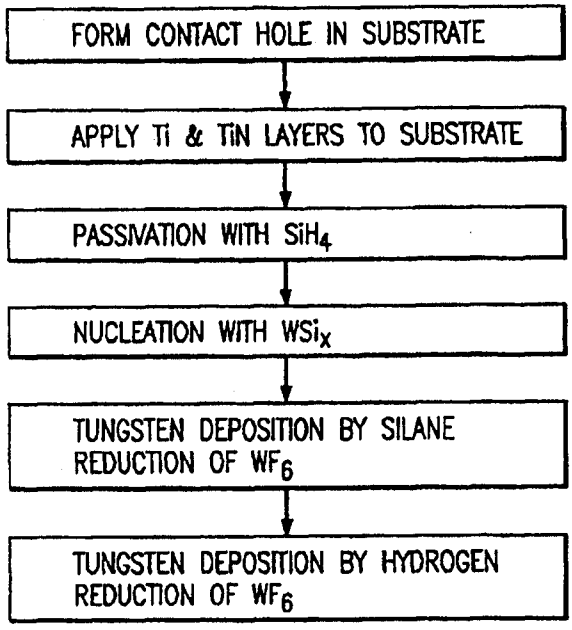

FORM CONTACT HOLE IN SUBSTRATE
APPLY Ti & TiN LAYERS TO SUBSTRATE
PASSIVATION WITH SiH_4
NUCLEATION WITH WSi_x
TUNGSTEN DEPOSITION BY SILANE REDUCTION OF WF_6
TUNGSTEN DEPOSITION BY HYDROGEN REDUCTION OF WF_6

FIG. 3

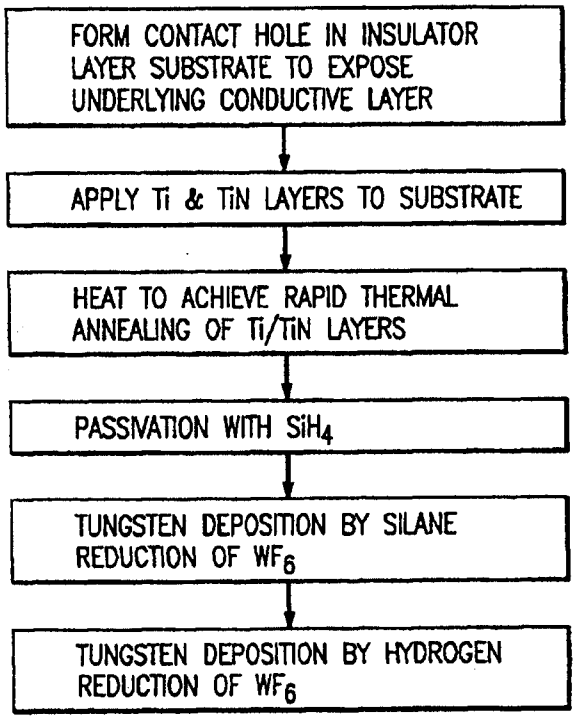

FORM CONTACT HOLE IN INSULATOR LAYER SUBSTRATE TO EXPOSE UNDERLYING CONDUCTIVE LAYER
APPLY Ti & TiN LAYERS TO SUBSTRATE
HEAT TO ACHIEVE RAPID THERMAL ANNEALING OF Ti/TiN LAYERS
PASSIVATION WITH SiH_4
TUNGSTEN DEPOSITION BY SILANE REDUCTION OF WF_6
TUNGSTEN DEPOSITION BY HYDROGEN REDUCTION OF WF_6

FIG. 4A

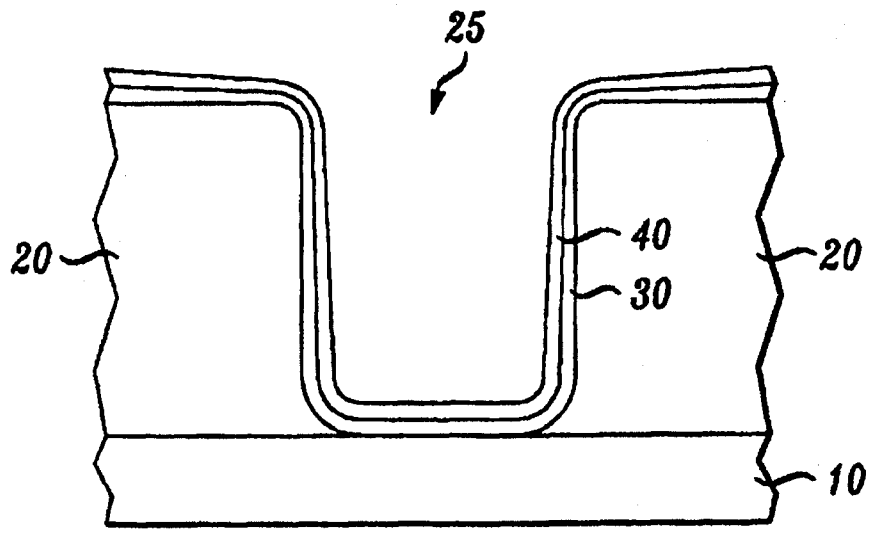


FIG. 4B

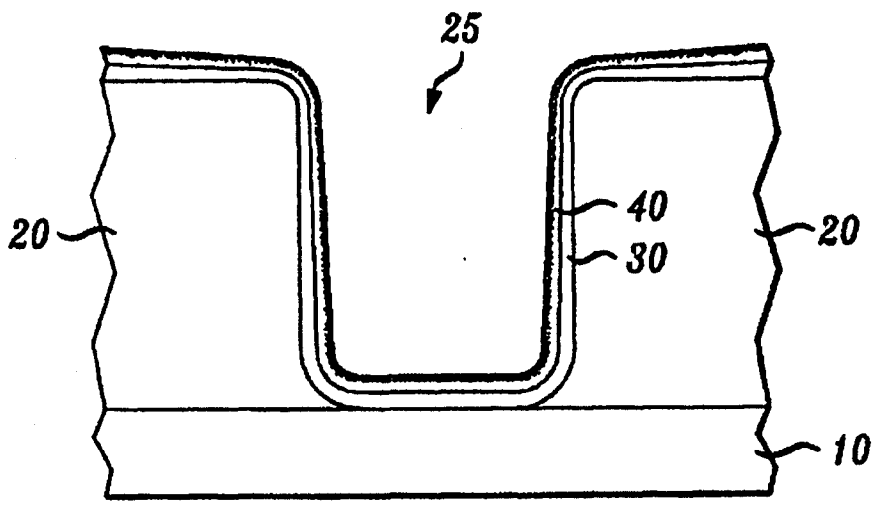


FIG. 4C

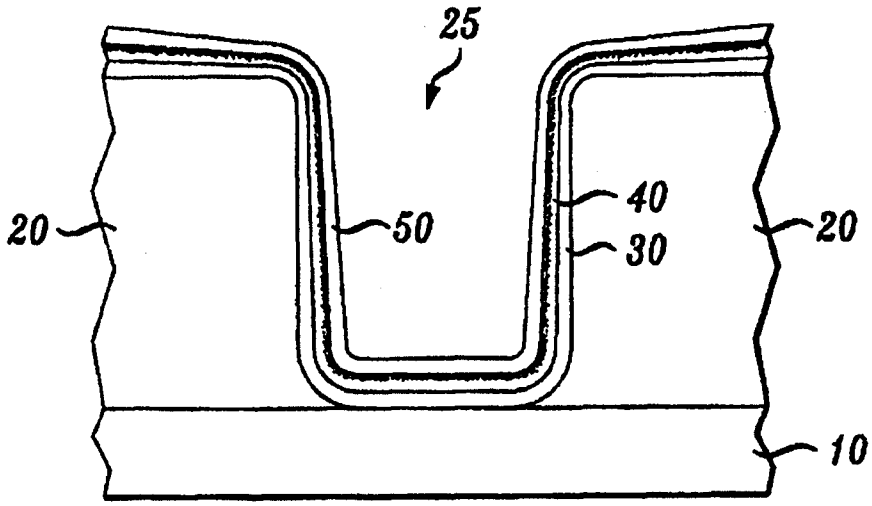
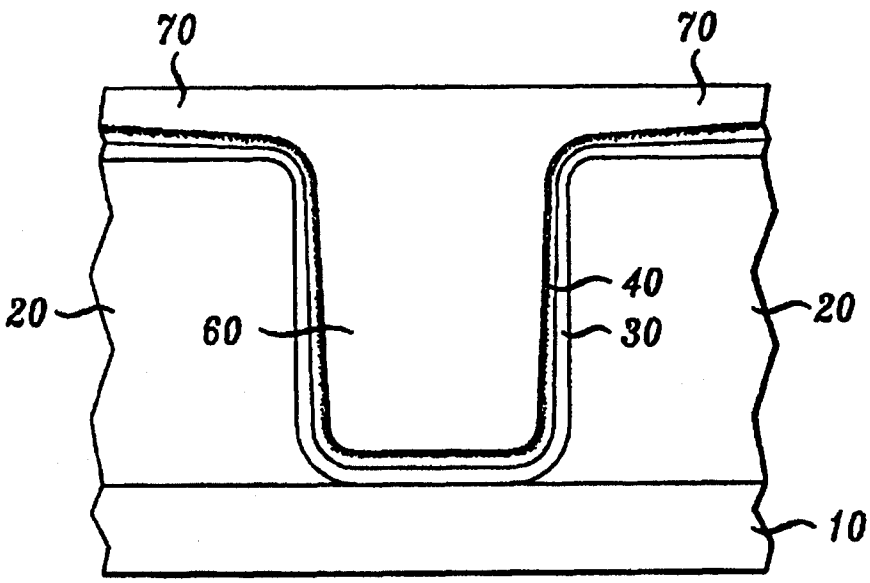


FIG. 4D



BARRIER LAYER TREATMENTS FOR TUNGSTEN PLUG

BACKGROUND

1. Technical Field

This disclosure relates generally to the manufacture of semiconductor devices having a multilayer interconnection structure. More specifically, this disclosure relates to novel methods of making tungsten plugs in such devices.

2. Background of Related Art

In the manufacture of a conventional tungsten plug or stud, a substrate **101** has a contact hole **110** formed therein as shown in FIG. **1A**. A titanium layer **112** and a titanium nitride layer **114** are sequentially deposited on the substrate. Near the top edge **115** of contact hole **110**, layers **112** and **114** are normally quite thin. Tungsten is then deposited, for example via chemical vapor deposition, to fill contact hole **110**. Depending on the position of the substrate within the device, the structure shown in FIG. **1A** can be used to produce a tungsten plug at the window level or a tungsten plug at the via level.

Tungsten deposition by CVD involves the use of tungsten hexafluoride, and subjects the coated substrate to fluorine and hydrofluoric acid. Diffusion of fluorine gas through pinhole defects in titanium nitride layer **114** causes excessive tungsten growth at the location of the defect.

Specifically, as shown in FIG. **1B**, rupture in titanium nitride layer **114** may occur, particularly at the top edge **115** of contact hole **110**. Where such ruptures occur, volcanoes **125** are formed which are areas of thick tungsten growth compared to tungsten layer produced within the contact hole **110** and the portion **122** of the tungsten layer produced on the surface of the substrate **101**. Hole **110** may not be completely filled with tungsten if growth is sufficiently rapid to cover the opening of the contact hole and thereby partially or completely block any further tungsten deposition within the hole. However, even where the contact hole is completely filled by a tungsten plug **130**, a large tungsten growth **126** is formed, the thickness of which far exceeds the thickness of the portion **122** of the tungsten layer on the surface of substrate **101**, as shown in FIG. **1C**. Ultimately, the device may have to be discarded due to the presence of the volcanoes. Where it is possible to salvage the device, additional steps must be taken to remove growth **126** from the surface of the device, adding to the cost of producing the device.

It would be desirable to provide a tungsten plug by a method which does not produce volcanoes or undesired tungsten growths on the surface of the device.

SUMMARY

Novel techniques for forming tungsten plugs are disclosed herein which avoid the formation of volcanoes and unwanted, excessive tungsten growths on the surface of the substrate.

In one aspect, it has been discovered that by carefully controlling the chemistry during chemical vapor deposition of tungsten, the integrity of the titanium nitride layer is preserved and the formation of volcanoes is avoided. Specifically, tungsten plugs are formed at the window or via level in accordance with one aspect of this disclosure by passivating a substrate having a contact hole formed therein by contacting the substrate with silane gas. A nucleation or seed layer of WSi_x is then applied to the passivated substrate by reducing tungsten hexafluoride with silane. In particularly useful embodiments, the ratio of silane to tungsten hexafluoride is in the ratio of 4:1 to 6:1 and pressures of 1 Torr or less are used during formation of the nucleation or seed layer. Tungsten is then deposited to at least substantially fill the contact hole. In a particularly useful embodiment, tungsten is deposited by reducing tungsten hexafluoride with hydrogen gas using pressures of 20 Torr or greater.

In another aspect, it has been discovered that tungsten plugs can be formed at the via level without the growth of volcanoes by subjecting a substrate coated with a titanium layer and then a titanium nitride layer to rapid thermal annealing to cure pinhole defects in the titanium and titanium nitride layers prior to passivation, nucleation and deposition steps.

BRIEF DESCRIPTION OF THE DRAWINGS

Various embodiments are described herein with reference to the drawings, wherein:

FIGS. **1A–1C** are schematic representations of structures at various stages during the formulation of tungsten plugs (either at the window level or at the via level) using conventional, prior art techniques;

FIG. **2** is a flow diagram showing the steps for forming a tungsten plug (at the window or via level) in accordance with a method disclosed herein;

FIG. **3** is a flow diagram showing the steps for forming a tungsten plug at the via level in accordance with another method disclosed herein; and

FIGS. **4A–4D** are schematic representations of structures at various stages during the formulation of a tungsten plug in accordance with the methods of this disclosure.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Two different novel via filling processes are disclosed herein. One method includes the formation of a WSi_x nucleation layer on a substrate prior to tungsten deposition. The other method involves rapid thermal annealing of a titanium nitride layer on a substrate prior to tungsten deposition. The deposition of a WSi_x nucleation layer and rapid thermal annealing of the titanium nitride layer are steps in two separate via filling processes which can be successfully used to prevent volcano formation. It should be understood that the two process steps can, if desired, be used together in a single via filling process.

FIG. **2** is a flow diagram summarizing the steps in one method of forming a tungsten plug in accordance with this disclosure. First, a contact hole is formed in the insulator layer of a substrate to expose a portion of a conductive layer or active layer of the device on which the insulator layer has been deposited. Next, titanium and titanium nitride layers are applied to the substrate. The coated substrate is then optionally subjected to rapid thermal annealing. Next, the coated substrate is passivated by contact with SiH_4. Then a nucleation or seed layer of WSi_x is applied by silane reduction of tungsten hexafluoride at a relatively low pressure, followed by tungsten deposition by silane reduction of tungsten hexafluoride. Finally, the contact hole is at least substantially filled with tungsten by hydrogen reduction of tungsten hexafluoride at relatively high pressures.

The steps of another method in accordance with this disclosure, is shown in the flow diagram of FIG. **3**. The method of FIG. **3** is particularly useful in forming a tungsten

plug at the via level and does not include the step of depositing a WSi_x nucleation layer. Rather, the method represented in FIG. 3 includes the step of thermal annealing to cure pinhole defects in the titanium nitride layer. The conditions for performing the various steps set forth in FIGS. 2 and 3 are set forth below and will be explained by reference to FIGS. 4A–D.

Referring to FIG. 4A, a substrate useful in forming a layered semiconductor device is shown wherein a first conductive layer **10** has an insulator layer **20** formed thereon. Insulator layer **20** can be made from any typical and well-known dielectric material used in wafer fabrication, but is preferably PETEOS.SiO_2.

A contact hole **25** extending down to the first conductive layer **10** is formed in insulator layer **20** using known photolithographic techniques. Since the contact hole extends down to a conductive layer, it will be appreciated by those skilled in the art that the structure shown in FIGS. 4A–D is used to form a tungsten plug at the via level. It should be understood, however, that tungsten plugs can also be formed at the window level using the methods disclosed herein. Preferably, the method shown in FIG. **3** is used to form tungsten plugs at the via level.

A titanium film **30** is deposited on the exposed surfaces. Titanium film **30** can be applied, for example, using a vacuum deposition technique, e.g., sputtering (with or without collimation). The thickness of titanium film can be in the range of about 50 Å to about 750 Å, preferably 500–600 Å.

A titanium nitride (TiN) film **40** is then deposited on all exposed surfaces of titanium film **30**. Titanium nitride film **40** can be formed using any known technique such as a reactive sputtering process (with or without collimation) wherein sputtering is carried out in $Ar+N_2$ atmosphere using a Ti target. The thickness of titanium nitride film **40** can be in the range of about 50 Å to about 1500 Å, preferably from 600 Å to about 1200 Å. TiN film **40** serves as an adhesion layer, facilitating deposition of tungsten onto the substrate.

Prior to beginning the tungsten deposition process, rapid thermal annealing (RTA) of the titanium/titanium nitride coated substrate can be carried out. RTA can be accomplished by exposing the coated substrate to temperatures of 450° to 550° C. for a period of time ranging from 5 to 60 seconds. The particular time and temperature employed will vary based on a number of factors including the thickness of the titanium and titanium nitride layers. In a particularly useful embodiment, substrates containing titanium nitride layers less than 600 Å thick can be annealed at 550° C. for 20 seconds. While not wishing to be bound to any theory, it is believed that RTA tends to cure pinhole defects in the titanium nitride layer, thereby reducing the likelihood of volcano growth during tungsten deposition. For the process shown in FIG. **2**, annealing is an optional step.

The TiN surface is then passivated by bringing silane (SiH_4) gas into contact with the TiN surface. Specifically, the Ti/TiN coated substrate is placed within a vacuum chamber and silane is introduced into the chamber at a flow rate ranging from 75 to 300 standard cubic centimeters per minute ("SCCM") for anywhere from 25 to 150 seconds. Preferably, the passivation process produces a discontinuous monolayer of silicon on the titanium nitride layer. The passivated, coated substrate is shown in FIG. 4B.

After passivation, a nucleation layer is formed by performing WF_6 reduction by SiH_4 at relatively low pressures. During the nucleation step, the flow of silane into the chamber is in the range of 75 to 300 SCCM and the flow of WF_6 into the chamber is in the range 35 to 300 SCCM. Preferably, the ratio of SiH_4:WF_6 flow rates is from about 6:1 to 4:1. Hydrogen (H_2) gas is also introduced into the chamber during nucleation at a rate of from 1000 to 6000 SCCM, preferably from 1500 to 3000 SCCM. The duration of the nucleation step is from 10 to 150 seconds at pressure ranging from 0.1 to 1.0 Torr. The temperature is during nucleation should be maintained between about 400°–450° C., preferably 420°–430° C. The nucleation step is believed to provide a WSi_x seed layer **50** on the passivated TiN surface (See FIG. 4C). While seed layer **50** is shown in FIG. 4C as a continuous layer, it should be understood that seed layer **50** can be a discontinuous layer applied to the TiN adhesion layer **40**. Preferably, the thickness of seed layer **50** is up to 30 Å, more preferably 2.5 Å to 25 Å. In the process of FIG. **3**, the step of forming a WSi_x nucleation layer need not be performed.

Simply by adjusting the relative flow rates of SiH_4 and WF_6, tungsten deposition can be initiated. The conditions suitable for tungsten deposition by silane reduction of tungsten hexafluoride are known to those skilled in the art.

Rapid deposition of tungsten is then achieved by WF_6 reduction with H_2 at a relatively high total pressure. To achieve tungsten deposition, H_2 is introduced into the chamber at flow rates of from 6000 to 7500 SCCM, preferably 6500 to 7000 SCCM, and WF_6 is introduced into the chamber at flow rates of 300 to 500 SCCM, preferably, about 400 SCCM. The total pressure during this deposition step is in the range 10 Torr to 100 Torr, preferably 20–50 Torr, most preferably 25–35 Torr.

Tungsten deposition is continued for a period of time sufficient to substantially fill the contact hole. In particularly useful embodiments, the tungsten deposition is continued until the contact hole is completely filled with a tungsten plug **60** and a substantially even layer **70** of tungsten is deposited on the upper surface of the structure as shown in FIG. 4D. Upon deposition of tungsten plug **60**, seed layer **50** may no longer be noticeable. While not wishing to be bound to any theory, it is believed that the WSi_x seed layer is converted to metallic tungsten during the H_2 reduction.

It will be understood that various modifications may be made to the embodiments disclosed herein. For example, while this disclosure has been presented in terms of a portion of a specific structure, it will be appreciated that the methods disclosed herein can be practiced on any type of device where it is necessary to make electrical contact to regions or layers under one or more insulator layers. Therefore, the above description should not be construed as limiting, but merely as exemplifications of preferred embodiments. Those skilled in the art will envision other modifications within the scope and spirit of the claims appended hereto.

What is claimed is:

1. A method of forming a tungsten plug comprising:

providing a substrate having a contact hole formed therein;

applying an adhesion layer of titanium nitride to at least a portion of the substrate;

contacting the substrate with SiH_4 to passivate the titanium nitride surface of the substrate;

reducing WF_6 with SiH_4 at a pressure of 1 Torr or less in the presence of the passivated substrate to form a nucleation layer on the passivated substrate; and

reducing WF_6 with H_2 at a pressure of at least 10 Torr to deposit tungsten to at least substantially fill the contact hole.

2. A method as in claim **1**, wherein the layer of titanium nitride is at least about 600 Å thick.

3. A method as in claim 1, wherein the step of reducing WF_6 with SiH_4 is conducted at a pressure less than about 0.5 Torr.

4. A method as in claim 1, wherein the step of reducing WF_6 with H_2 is conducted at a pressure of at least about 10 Torr.

5. A method as in claim 1, wherein the step of reducing WF_6 with H_2 is conducted at a pressure of at least 25 Torr.

6. A method as in claim 1, wherein the steps of reducing WF_6 with SiH_4 and reducing WF_6 with H_2 are both conducted at temperatures greater than about 400° C.

7. A method as in claim 1, further comprising the step of annealing the adhesion layer prior to passivation.

8. A method as in claim 7, wherein the annealing is conducted at a temperature ranging from 450° C. to 550° C. for a time ranging from 5 seconds to about 60 seconds.

9. A method of forming a tungsten plug comprising:

placing a substrate within a chamber, the substrate comprising a conductive layer, an insulator layer formed on the conductive layer, the insulator layer having a contact hole formed therein, the contact hole extending through the insulator layer and exposing a portion of the conductive layer;

applying an adhesion layer Of titanium nitride to at least a portion of the substrate;

introducing SiH_4 gas into the chamber to passivate the titanium nitride layer of the substrate;

introducing SiH_4 gas and WF_6 gas into the chamber, whereby WF_6 is reduced thereby nucleating the passivated substrate;

depositing tungsten to at least substantially fill the contact hole.

10. A method as in claim 9, wherein the layer of titanium nitride is at least about 600 Å thick.

11. A method as in claim 9, further comprising the step of annealing the adhesion layer prior to the step of introducing SiH_4 gas into the chamber.

12. A method as in claim 11, wherein the annealing step comprises heating the coated substrate to a temperature between about 450° C. and about 550° C. for a period of time from about 5 seconds to about 60 seconds.

13. A method as in claim 9, wherein the step of introducing SiH_4 and WF_6 gas into the chamber comprises introducing SiH_4 into the chamber at a flow rate of about 75 SCCM to about 300 SCCM and introducing WF_6 into the chamber at a flow rate of about 35 SCCM to about 300 SCCM.

14. A method as in claim 9, wherein the step of introducing SiH_4 gas and WF_6 gas comprises introducing SiH_4 gas and WF_6 gas in a ratio of about 4:1 to about 6:1.

15. A method as in claim 9, wherein the pressure within the chamber during the step of introducing SiH_4 and WF_6 does not exceed about 1 Torr.

16. A method as in claim 9, wherein the pressure within the chamber during the step of introducing H_2 gas and WF_6 gas is at least about 20 Torr.

17. A method of forming a tungsten plug comprising:

providing a coated substrate, the coated substrate comprising a conductive layer, an insulator layer formed on the conductive layer, a contact hole formed through the insulator layer to expose a portion of the conductive layer, a layer of titanium coating at least a portion of the insulator layer and the exposed portion of the conductive layer and a layer of titanium nitride applied to the titanium layer;

passivating the coated substrate by contacting the layer of titanium nitride with silane;

depositing a nucleation layer on the passivated, coated substrate by reducing tungsten hexafluoride with silane at a pressure of about 1 Torr or less in the presence of the passivated, coated substrate, the ratio of silane to tungsten hexafluoride being in the range of 4:1 to 6:1 during the deposition of the nucleation layer; and

depositing tungsten to at least substantially fill the contact hole by reducing tungsten hexafluoride with hydrogen gas a pressure of at least about 20 Torr.

18. A method as in claim 17, wherein the layer of titanium nitride is at least about 600 Å thick.

19. A method as in claim 17, wherein the step of reducing WF_6 with SiH_4 is conducted at a pressure less than about 0.5 Torr.

20. A method as in claim 17, wherein the step of reducing WF_6 with H_2 is conducted at a pressure of at least about 10 Torr.

21. A method as in claim 17, wherein the step of reducing WF_6 with H_2 is conducted at a pressure of at least 25 Torr.

22. A method as in claim 17, wherein the steps of reducing WF_6 with SiH_4 and reducing WF_6 with H_2 are both conducted at temperatures greater than about 400° C.

23. A method as in claim 17, further comprising the step of annealing the layer of titanium nitride prior to passivation.

24. A method as in claim 23, wherein the annealing is conducted at a temperature ranging from 450° C. to 550° C. for a time ranging from 5 seconds to about 60 seconds.

25. A method as in claim 17, wherein the layer of titanium nitride is applied to the substrate by a reactive sputtering process with collimation.

26. A method as in claim 17, wherein the layer of titanium nitride is applied to the substrate by a reactive sputtering process without collimating.

27. A method of forming a tungsten plug at the via level comprising:

providing a coated substrate, the coated substrate comprising a conductive layer, an insulator layer formed on the conductive layer, a contact hole formed through the insulator layer to expose a portion of the conductive layer, a layer of titanium coating at least a portion of the insulator layer and the exposed portion of the conductive layer and a layer of titanium nitride applied to the titanium layer;

heating the coated substrate to achieve rapid thermal annealing of the layers of titanium and titanium nitride by exposing the substrate to a temperature in the range of 450° to 550° C. for a period of time between 5 and 60 seconds; and

depositing tungsten to at least substantially fill the contact hole.

28. A method as in claim 27, further comprising the step of passivating the coated substrate by contacting the annealed layer of titanium nitride with silane.

29. A method as in claim 28, further comprising the step of depositing a nucleation layer on the passivated, coated substrate by reducing tungsten hexafluoride with silane.

30. A method as in claim 27, wherein the step of depositing tungsten comprises reducing tungsten hexafluoride with hydrogen gas.

31. A method of forming a tungsten plug at the via level comprising:

providing a coated substrate, the coated substrate comprising a conductive layer, an insulator layer formed on the conductive layer, a contact hole formed through the insulator layer to expose a portion of the conductive layer, a layer of titanium coating at least a portion of the

insulator layer and the exposed portion of the conductive layer and a layer of titanium nitride applied to the titanium layer;

heating the coated substrate to achieve rapid thermal annealing of the layers of titanium and titanium nitride;

passivating the coated substrate by contacting the annealed layer of titanium nitride with silane;

depositing a nucleation layer on the passivated, coated substrate by reducing tungsten hexafluoride with silane; and depositing tungsten to at least substantially fill the contact hole.

32. A method as in claim **31**, wherein the step of heating comprises exposing the substrate to a temperature in the range of 450° to 50° C. for a period of time between 5 and 60 seconds.

33. A method as in claim **31**, wherein the step of depositing tungsten comprises reducing tungsten hexafluoride with hydrogen gas.

34. A method of forming a tungsten plug comprising:

providing a substrate having a contact hole formed therein;

applying an adhesion layer of titanium nitride to at least a portion of the substrate prior to passivation;

contacting the substrate with SiH_4 to passivate the titanium nitride surface of the substrate;

reducing WF_6 with SiH_4 in the presence of the passivated substrate to form a nucleation layer on at least the passivated titanium nitride surface of the substrate; and depositing tungsten to at least substantially fill the contact hole.

* * * * *

EXHIBIT D

US005693561A

United States Patent [19]

Merchant et al.

[11] Patent Number: 5,693,561

[45] Date of Patent: Dec. 2, 1997

[54] **METHOD OF INTEGRATED CIRCUIT FABRICATION INCLUDING A STEP OF DEPOSITING TUNGSTEN**

[75] Inventors: **Sailesh Mansinh Merchant; Leonard Jay Olmer; Ronald Joseph Schutz**, all of Orlando, Fla.

[73] Assignee: **Lucent Technologies Inc.**, Murray Hill, N.J.

[21] Appl. No.: **645,852**

[22] Filed: **May 14, 1996**

[51] Int. Cl.[6] **H01L 21/283**

[52] U.S. Cl. **437/190**; 437/192; 437/195; 437/228

[58] Field of Search ..... 437/189, 190, 437/192, 195, 228 ST; 257/751, 752, 763

[56] **References Cited**

U.S. PATENT DOCUMENTS

5,143,861	9/1992	Turner	437/52
5,164,330	11/1992	Davis et al.	437/192
5,175,126	12/1992	Ho et al.	437/190
5,183,782	2/1993	Onishi et al.	437/192
5,200,360	4/1993	Bradbury et al.	437/192
5,202,579	4/1993	Fujii	257/751
5,232,871	8/1993	Ho	437/190
5,232,873	8/1993	Geva	437/192
5,233,223	8/1993	Murayama	257/770
5,236,869	8/1993	Takagi et al.	437/190
5,244,534	9/1993	Yu et al.	156/636
5,260,232	11/1993	Muroyama et al.	437/187
5,312,775	5/1994	Fujii et al.	437/192
5,327,011	7/1994	Iwamatsu	257/750
5,552,339	9/1996	Hsieh	437/190

OTHER PUBLICATIONS

"Failure of Titanium Nitride Diffusion Barriers During Tungsten Chemical Vapor Deposition: Theory and Practice", Matthew Rutten et al., Conference Proceedings ULSI–VII, 1992 Materials Research Society.

Primary Examiner—T. N. Quach
Attorney, Agent, or Firm—John T. Rehberg

[57] **ABSTRACT**

Integrated circuit fabrication includes the formation of tungsten contacts in windows. Between the tungsten and the contact region are Ti and TiN layers. Defects are prevented or reduced by sealing grain boundaries in the TiN layer prior to tungsten deposition. Grain boundaries are sealed by rinsing the TiN layer in water at ambient temperature or above.

6 Claims, 1 Drawing Sheet

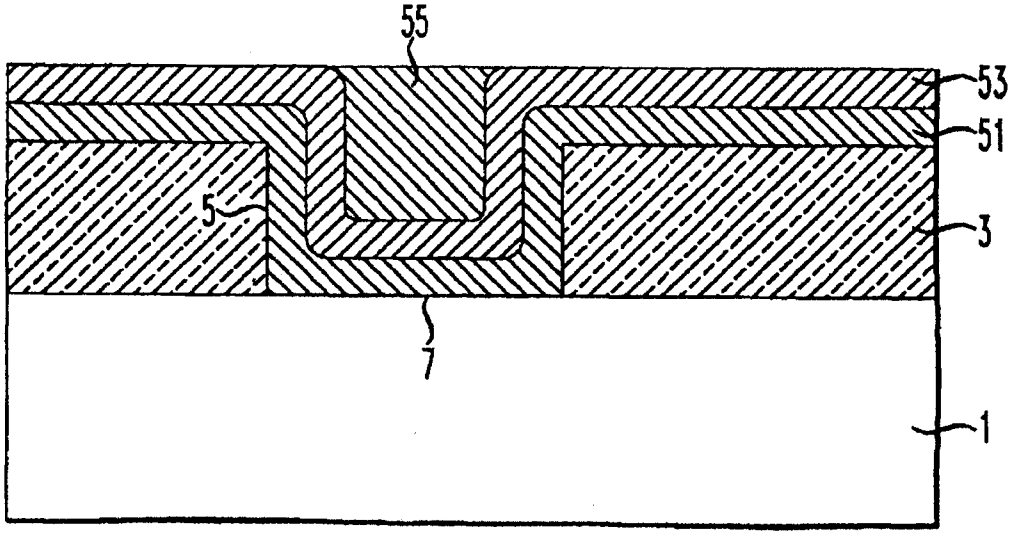
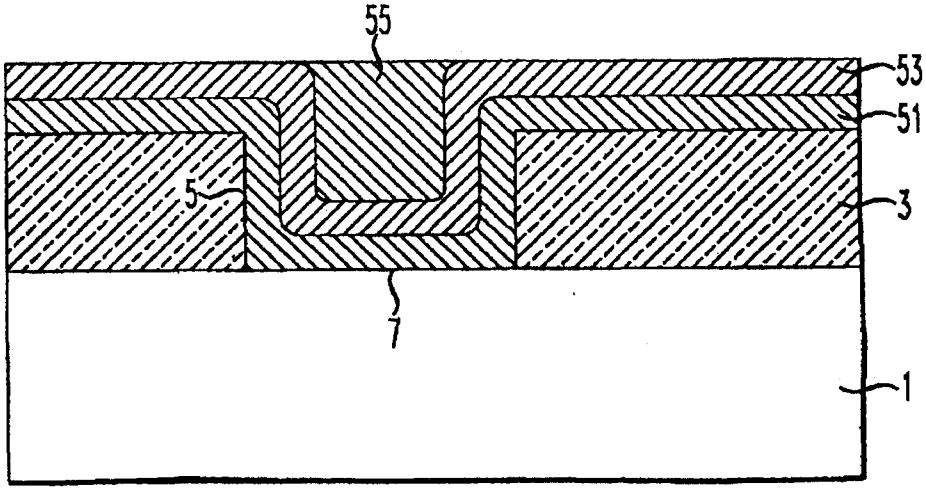


FIG. 1



METHOD OF INTEGRATED CIRCUIT FABRICATION INCLUDING A STEP OF DEPOSITING TUNGSTEN

TECHNICAL FIELD

This invention relates generally to a method of integrated circuit fabrication that includes a step of tungsten deposition and particularly to such a method that includes a step that reduces the defect density of the deposited tungsten.

BACKGROUND OF THE INVENTION

Integrated circuits frequently form electrical contacts to components, such as field effect transistor, by depositing a dielectric layer over the transistor and then patterning the dielectric layer to form openings or windows which expose elements; for example, gate, source or drain, of the transistor. Metal is then deposited in the windows to form the contacts. As integrated circuits have increased in complexity, multilevel metallizations have been developed. In such metallizations, an electrical conductor, rather than a device element, is contacted. Aluminum was the metal initially used because of its good electrical characteristics and relative ease of handling. However, as device dimensions have shrunk, sputtered or physically vapor deposited (PVD) aluminum and its alloys (such as Al—Cu or Al—Si—Cu) have exhibited drawbacks, such as a tendency to form re-entrant angles, which make it difficult to obtain adequate filling of the window. Accordingly, alternatives to aluminum and its alloys have been sought.

One alternative that has been extensively investigated is tungsten. Tungsten may be deposited by a variety of techniques including chemical vapor deposition (CVD) which may be either a blanket or a selective deposition. CVD decomposes a tungsten-containing precursor gas, such as WF_6, and the tungsten is deposited on the surface. The blanket deposition of tungsten using WF_6 is the most common method of depositing CVD tungsten in the prior art. In the case of selective tungsten, a method not commonly used, tungsten is not deposited on dielectric surfaces but only on the conducting surfaces. CVD tungsten does not have either the re-entrant angles or poor step coverage exhibited by PVD aluminum. Tungsten is not generally deposited directly onto silicon, a dielectric, or aluminum. Typically, intermediate layers, such as Ti or TiN or combinations thereof, are present between the tungsten and the underlying layer for reasons of adhesion or barrier properties.

See, for example, U.S. Pat. No. 5,260,232 issued on Nov. 9, 1993 to Muroyama for description of a technique for filling windows by selective CVD tungsten. In some embodiments, Muroyama formed a TiN layer which functioned both as a barrier layer and as an adhesion layer. U.S. Pat. No. 5,202,579 issued on Apr. 13, 1993 to Fujii used both Ti and TiN between the tungsten and the aluminum.

However, it has been found that the tungsten plugs (where tungsten is used to fill an opening, at the window or via level, hereafter referred to collectively as openings, unless otherwise stated) obtained by the CVD deposition process frequently have defects. The source of the defects is not known with certainty, but it is believed that the defects are caused by a reaction of the WF_6 precursor gas or some F_2-containing species used in the CVD process with the Ti layer in the Ti/TiN composite film. The defects are often called volcanoes, and are undesirable because the Ti/TiN film may peel off and thereby allow tungsten growth on both sides of the film. Adverse effects that may result include blockage or partial filling of the openings so that tungsten deposition does not completely fill the openings where desired, or, in the worst case, formation of tungsten mounds large enough so that there are inadvertent electrical shorts between adjacent openings. These large mounds are called volcanoes because of their morphology. The presence of these defects can reduce device yield.

Various proposals have been made to either solve or alleviate the adverse effects described. For example, a N_2 anneal following the Ti/TiN film deposition has been proposed. Alternatively, the thickness of the Ti layer may be reduced. Additionally collimated Ti/TiN layers have been used.

However, these proposals suffer drawbacks. For example, the annealing process can not be used when aluminum interconnects are present because of the relatively high temperature used for the anneal. A reduced Ti thickness may result in poor junction yield, especially in non-salicided junctions, where a non-optimal Ti thickness at the bottom of the window from lack of adequate step coverage, will result in a high contact resistance problem.

SUMMARY OF THE INVENTION

According to the invention, a method of integrated circuit fabrication includes forming tungsten contacts in windows by depositing Ti and TiN layers in windows formed in a patterned dielectric that expose selected conducting portions; for example, of the substrate or of material on the substrate, and sealing TiN grain boundaries prior to tungsten deposition. The conducting portions are under the dielectric layer. Sealing of the TiN grain boundaries prevents attack of the underlying Ti layer by the WF_6 used in the CVD tungsten deposition process. In an exemplary embodiment, the grain boundaries are sealed by rinsing in water having at least the ambient temperature. The rinsing may be with or without CO_2 bubbling through the water. In another embodiment, the temperature is approximately 80° C. and the time is approximately 10 minutes. In yet another embodiment, the wafer is heated in an oxygen containing environment.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a sectional view of a portion of an integrated circuit having a tungsten contact formed according to this invention.

For reasons of clarity, the elements depicted are not drawn to scale.

DETAILED DESCRIPTION

The invention will be described by reference to an exemplary embodiment used to form the contact, which is a portion of an integrated circuit, depicted in FIG. 1. Depicted are substrate 1, dielectric layer 3 which has been patterned to form window 5 which exposes contact area 7 in the substrate. The window thus exposes selected conducting portions of the substrate or of material on the substrate. The conducting portions are under the dielectric layer. The term substrate is used to mean a material that lies underneath and supports another material. The substrate may thus be the silicon wafer, an epitaxial layer on the wafer, or a dielectric layer on which a metal has been deposited. The contact area 7 is conducting although it is to be understood that the window may also expose some nonconducting area. Within window 5 and present on dielectric layer 3 are Ti layer 51, TiN layer 53 and tungsten 55. The substrate 1 may be silicon and the contact areas 7 may be the source/drain regions of

a field effect transistor. Alternatively, the contact area may be formed by an aluminum interconnect present on a dielectric layer.

The structure described, except for sealing of the TiN grain boundaries, will be readily formed by those skilled in the art. For example, the windows in the dielectric layer 3 are formed by conventional and well known techniques which need not be further described for those skilled in the art to practice the invention. Conventional and well known techniques are used to deposit the Ti and TiN layers, and well known chemical vapor deposition (CVD) techniques are used to deposit the tungsten.

It has been found that a step that is hypothesized to seal the grain boundaries in the TiN layer prevents the adverse effects described in the Background of the Invention. It is believed that the defects are formed because WF_6 or other F_2-containing species penetrates the TiN layer and reacts with the underlying Ti. However, all the processes that prevent the adverse effects are consistent with grain boundary sealing. Hence, the invention is described in terms of sealing grain boundaries.

The grain boundaries are sealed by exposure to oxygen; that is, by oxygenating the grain boundaries. This may be done by several embodiments. In one embodiment, the grain boundaries are sealed by rinsing in water. The temperature of the water is at least the ambient temperature. The rinsing is for a period of at least 10 seconds. Elevated temperatures may also be used. For example, a temperature of 80° C. may be used with a rinsing time of approximately 600 seconds. Bubbling CO_2 through the water may also be performed. This step appears to improve grain boundary sealing.

In yet another embodiment, the grain boundaries are sealed by heating the wafer in an oxygen containing environment. The oxygen is in relatively low concentration; that is the oxygen concentration may be approximately 2% with the remainder of the atmosphere being an inert carrier gas such as nitrogen. The temperature is desirably between 300° and 500° C. although temperatures outside this range may be used.

After the grain boundaries have been sealed, the CVD tungsten deposition is performed. Convention and now well known deposition techniques may be used. After tungsten deposition has been completed, the remainder of the integrated circuit fabrication is completed. For example, the tungsten is patterned and another dielectric layer is deposited and so forth.

Variations in the embodiments described will be apparent to those skilled in the art. For example, the grain boundaries may be sealed by exposure to oxidizing agents other than oxygen. Additionally, the tungsten may be deposited only in the windows. Furthermore, inert gases other than nitrogen may be used as a carrier gas.

The invention claimed is:

1. A method of integrated circuit fabrication comprising the steps of:

forming a dielectric layer on a substrate;

forming windows in said dielectric layer to expose selected conducting portions under said dielectric layer;

depositing layers of Ti and TiN on said dielectric layer and in said windows;

sealing TiN grain boundaries by rinsing the TiN layer with water; and

depositing tungsten on said TiN layer by chemical vapor deposition.

2. A method as recited in claim 1 in which said sealing step comprises rinsing in water having at least ambient temperature.

3. A method as recited in claim 2 in which said rinsing is for at least 10 seconds.

4. A method as recited in claim 2 in which said ambient temperature is approximately 80° C.

5. A method as recited in claim 4 in which said rinsing is for approximately 600 seconds.

6. A method as recited in claim 2 further comprising the step of:

bubbling CO_2 through said water.

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