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Attorney for the Plaintiff

UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

C 05 5313 EDL

JAMES B. GOODMAN,

Plaintiff,

vs.

NANOAMP SOLUTIONS, INC.,

Defendant.

Civil Action No.

COMPLAINT FOR PATENT INFRINGEMENT AND DEMAND FOR JURY TRIAL

NOW COMES Plaintiff, JAMES B. GOODMAN ("Goodman"), through his attorneys, and files this Complaint for Patent Infringement and Demand for Jury Trial against NANOAMP SOLUTIONS, INC. ("NANOAMP"), and in support thereof Goodman states as follows:

JURISDICTION

1. This is an action for patent infringement of United States Patent No. 6,243,315 (hereinafter "The '315 Patent") pursuant to the laws of the United States of America as set forth in Title 35 Sections 271 and 281 of the United States Code. This court has subject matter jurisdiction over this action pursuant to 28 U.S.C. Sec. 1338(a) and 28 U.S.C. Sec. 1331.

2. Venue is proper in this judicial district under 28 U.S.C. §§§ 1391(b), (c) and 1400(b). On information and belief, Defendant NANOAMP maintains a principal place of business at 670 North McCarthy Blvd., Suite 220, Milpitas, California 95035.

3. Plaintiff Goodman is an individual residing in the State of Texas.

INTRADISTRICT ASSIGNMENT

4. This is an action for Patent Infringement, which is an excepted category under Civil L.R. 3-2(c). Pursuant to Civil L.R. 3-2(c), this action is assigned on a district-wide basis.

CAUSES OF ACTION FOR PATENT INFRINGEMENT

5. On June 5, 2001, the '315 Patent entitled "COMPUTER MEMORY SYSTEM WITH A LOW POWER MODE", was duly and legally issued to James B. Goodman, as the sole patentee.

6. Goodman is the sole owner of the '315 Patent, and has standing to bring this action.

COUNT ONE

7. Plaintiff, Goodman repeats and incorporates herein the allegations contained in paragraphs 1 through 6 above.

8. Defendant NANOAMP is infringing, at least claim 1 of the '315 Patent by making, using, offering for sale, and selling within the United States of America infringing computer memory products including its line of Low Power 1T-based Pseudo SRAMs.

9. Upon information and belief, NANOAMP manufactures, uses, offers for sale and sells a memory system called Low Power 1T-based Pseudo SRAMs for use in a computer system including the following products: N08T1630CxB and N16T1630C2B ("the NANOAMP PSRAM").

10. Upon information and belief, the NANOAMP PSRAM has is a volatile solid state memory device that retains information when an electrical power source is applied to it within a predetermined voltage range. The NANOAMP PSRAM contains a memory array and is capable of implementing an automatic self-refresh mode and have address lines and control lines.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff respectfully requests this Court to:

a. enter judgment for Plaintiff on this Complaint;

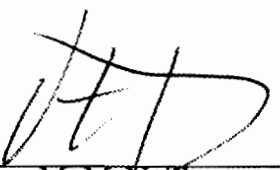
b. enter a permanent injunction to enjoin the Defendant and those in privity with or acting in concert with Defendant from further infringement of the '315 Patent during the remainder of the term for which the patent has been granted;

c. order that an accounting be had for the damages caused to the Plaintiff by the infringing activities of the Defendant;

d. award Plaintiff interest and costs; and

e. award Plaintiff such other and further relief as this Court may deem just and equitable.

THE PLAINTIFF
JAMES B. GOODMAN



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11. Upon information and belief, the NANOAMP PSRAM has a control logic sub-system that is able to selectively electrically isolate the device's address lines and respective control lines so that signals are ignored or go unnoticed. For example, according to the N08T1630CxB Datasheet Page 2, Functional Description Note 3 "When the device is in standby mode, control inputs (WE, OE, UB, and LB), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally." Moreover, according to the N16T1630C2B Datasheet Page 2, Functional Description Note 2, "When the device is in standby mode, control inputs (WE, OE, UB, and LB), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally."

12. Upon information and belief, when a deselect signal is detected a determination is made by a sub-system of the control logic to place the NANOAMP PSRAM system in standby power mode. "When the device is in standby mode, control inputs (WE, OE, UB, and LB), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally." The NANOAMP PSRAM memory array is placed in standby power mode thereby reducing the amount of electrical energy being drawn from an electrical power supply for the computer system.

JURY DEMAND

13. Pursuant to Fed. R. Civ. P. 38, Plaintiff hereby demands a jury trial as to all issues in this lawsuit.