IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

SIGMATEL, INC.,

Plaintiff,

v.

ACTIONS SEMICONDUCTOR COMPANY, LTD., and SONIC IMPACT TECHNOLOGIES, LLC,

Defendants.

A05CA 008LY

COMPLAINT AND JURY DEMAND

Plaintiff SigmaTel, Inc. ("SigmaTel"), by and through its undersigned attorneys, for its Complaint against Actions Semiconductor Company, Ltd. and Sonic Impact Technologies, LLC, demand a jury trial and allege as follows:

NATURE OF THE ACTION

1. This is an action for patent infringement arising out of the Patent Laws of the United States, 35 U.S.C. §§ 1, *et seq.*

PARTIES

2. SigmaTel is a corporation organized and existing under the laws of the State of Delaware, having its principal place of business at 1601 South Mo-Pac Expressway, Suite 100, Austin, Texas 78746.

3. On information and belief, Defendant Actions Semiconductor Company, Ltd. ("Actions") is a corporation organized and existing under the laws of the country of China,

having its principal place of business at 15-1 No. 1, HIT Road, Tangja, Zhuhai, Guangdong, China 519085.

4. On information and belief, Defendant Sonic Impact Technologies, LLC ("Sonic Impact") is a limited liability company organized and existing under the laws of the State of California, and having a principal place of business at 2555 State Street, San Diego 92101.

JURISDICTION AND VENUE

5. This Court has jurisdiction over the subject matter of this Complaint, which arises under the Patent Act of the United States, in accordance with 28 U.S.C. §§ 1331 and 1338(a).

6. This Court has personal jurisdiction over Actions and Sonic Impact because, among other things, on information and belief, Actions and Sonic Impact have in the past physically conducted and continue to conduct business throughout the United States, including within this judicial district.

7. Venue is proper in this judicial district pursuant to 28 U.S.C. §§ 1391(c), 1391(d), and 1400(b).

BACKGROUND

8. SigmaTel was founded in 1993, in Austin, Texas, focused on designing, developing, and marketing mixed-signal integrated circuits ("ICs") for leading portable and consumer audio applications throughout the world.

9. Initially, SigmaTel designed and sold audio codecs for incorporation into personal computers.

10. Most recently, SigmaTel has focused its expertise on the design and development of ICs to address control and audio processing requirements for digital audio players – *i.e.*, MP3-style players – and for infrared communications interface products, which facilitate use of high-speed infrared connections between personal computers and peripheral devices.

11. SigmaTel has established a very strong reputation as an innovator and industry leader in the development of mixed signal IC technology, and has long recognized the value and importance of its technological innovations. It is frequently the first to market with high-performance, cost-effective devices and applications, and has achieved substantial success from the commercialization of its innovative designs.

12. For this reason, SigmaTel has expended considerable resources to appropriately protect its innovations and inventions in accordance with intellectual property laws of this country and others in which it conducts business. For example, SigmaTel owns more than 100 U.S. patents or pending U.S. patent applications, and similarly takes all necessary actions to protect its valuable trademarks and trade secrets

THE PATENTS-IN-SUIT

13. On October 24, 2000, United States Patent No. 6,137,279 ("the '279 Patent"), entitled "Adjustable Power Control Module and Applications Thereof" and naming as inventors Kenneth Gozie Ifesinachukwa and Mathew A. Rybicki, was duly and legally issued by the United States Patent and Trademark Office to SigmaTel. Since that time, SigmaTel has been and continues to be the sole owner of the '279 Patent. A true and correct copy of the '279 Patent is attached to this Complaint as Exhibit A.

14. The '279 Patent is valid and enforceable.

15. On October 14, 2003, United States Patent No. 6,633,187 ("the '187 Patent"), entitled "Method and Apparatus for Enabling a Stand Alone Integrated Circuit" and naming as inventors Michael R. May and Marcus W. May, was duly and legally issued by the United States Patent and Trademark Office to SigmaTel. Since that time, SigmaTel has been and continues to be the sole owner of the '187 Patent. A true and correct copy of the '187 Patent is attached to this Complaint as Exhibit B.

16. The '187 Patent is valid and enforceable.

17. On April 2, 2002, United States Patent No. 6,366,522 ("the '522 Patent"), entitled "Method and Apparatus for Controlling Power Consumption of an Integrated Circuit" and naming as inventors Marcus W. May and Daniel Mulligan, was duly and legally issued by the United States Patent and Trademark Office to SigmaTel. Since that time, SigmaTel has been and continues to be the sole owner of the '522 Patent. A true and correct copy of the '522 Patent is attached to this Complaint as Exhibit C.

18. The '522 Patent is valid and enforceable.

DEFENDANTS' INFRINGING ACTS

19. On information and belief, Sonic Impact is engaged in the business of using, offering for sale, and selling in the United States, and/or importing into the United States an MP3 player incorporating the inventions of one or more of SigmaTel's valuable U.S. patents. Sonic Impact's infringing TM884B MP3 Portable System is sold throughout the United States and in this judicial district through at least one major retail department store chain, as well as directly from Sonic Impact via the Internet.

20. Sonic Impact's infringing TM884B MP3 Portable System includes an MP3 player that incorporates an ATJ2075 semiconductor and corresponding circuit board.

21. On information and belief, the ATJ2075 semiconductor and corresponding circuit board has been and continue to be designed, manufactured, offered for sale, sold, and/or imported into the United States by Actions.

22. The ATJ2075 semiconductor and corresponding circuit board infringes, either directly or indirectly, one or more claims of SigmaTel's '279 Patent.

23. On information and belief, Actions has actively sought to enter into relationships with companies in the United States other than Sonic Impacts for purposes of using, offering for sale, and selling within the United States and/or importing into the United States ATJ2075 semiconductors and circuit boards, as well as other semiconductor devices that incorporate one or more inventions of SigmaTel's U.S. patents.

24. On information and belief, Actions has in the past and continues to physically offer for sale or sells in the United States, and/or imports into the United States such infringing semiconductor devices. For example, on information and belief, Actions recently approached in the United States one or more brand name distributor of portable MP3 devices and offered to sell its ATJ2085, ATJ2087, and/or ATJ2089 semiconductor devices. Each of these Actions semiconductors infringes, directly or indirectly, one or more claims of SigmaTel's '279, '187, and '522 Patents.

25. On information and belief, Sonic Impact and Actions have had actual or constructive knowledge of each of SigmaTel's '279, '187, and '522 Patents at all times relevant to the allegations of this Complaint.

COUNT I
Sonic Impact's Infringement of U.S. Patent No. 6,137,279

26. SigmaTel repeats and realleges the allegations of Paragraphs 1 through 25, as if fully set forth herein.

27. Sonic Impact has infringed and is currently infringing, directly and/or indirectly, SigmaTel's '279 Patent by, among other things, making, using, offering for sale, and/or selling in the United States, or importing into the United States products such as Sonic Impact's TM884B MP3 Portable System, which incorporate the inventions of one or more claims of the '279 Patent.

28. Sonic Impact's infringement is causing and will continue to cause damage and irreparable injury to SigmaTel, unless and until such infringing activity is enjoined by this Court.

29. On information and belief, Sonic Impact is engaging in willful and deliberate infringement, supporting an award of enhanced damages under 35 U.S.C. § 284, and making this case exceptional for purposes of 35 U.S.C. § 285.

COUNT II
Actions' Infringement of U.S. Patent No. 6,137,279

30. SigmaTel repeats and realleges the allegations of Paragraphs 1 through 29, as if fully set forth herein.

31. Actions has infringed and is currently infringing, directly or indirectly, SigmaTel's '279 Patent by, among other things, making, using, offering for sale, and/or selling in the United States, or importing into the United States ATJ2075, ATJ2085, ATJ2087, and/or ATJ2089 semiconductor devices, corresponding circuit boards, and/or products such as Sonic Impact's TM884B MP3 Portable System, which incorporate the inventions of one or more claims of the '279 Patent.

32. Actions' infringement is causing and will continue to cause damage and irreparable injury to SigmaTel, unless and until such infringing activity is enjoined by this Court.

33. On information and belief, Actions is engaging in willful and deliberate infringement, supporting an award of enhanced damages under 35 U.S.C. § 284, and making this case exceptional for purposes of 35 U.S.C. § 285.

COUNT III
Actions' Infringement of U.S. Patent No. 6,633,187

34. SigmaTel repeats and realleges the allegations of Paragraphs 1 through 33, as if fully set forth herein.

35. Actions has infringed and is currently infringing, directly or indirectly, SigmaTel's '187 Patent by, among other things, making, using, offering for sale, and/or selling in the United States, or importing into the United States ATJ2085, ATJ2087, and/or ATJ2089 semiconductor devices, corresponding circuit boards, and/or products featuring such semiconductor devices, which incorporate the inventions of one or more claims of the '187 Patent.

36. Actions' infringement is causing and will continue to cause damage and irreparable injury to SigmaTel, unless and until such infringing activity is enjoined by this Court.

37. On information and belief, Actions is engaging in willful and deliberate infringement, supporting an award of enhanced damages under 35 U.S.C. § 284, and making this case exceptional for purposes of 35 U.S.C. § 285.

COUNT IV
Actions' Infringement of U.S. Patent No. 6,366,522

38. SigmaTel repeats and realleges the allegations of Paragraphs 1 through 37, as if fully set forth herein.

39. Actions has infringed and is currently infringing, directly or indirectly, SigmaTel's '522 Patent by, among other things, making, using, offering for sale, and/or selling in the United States, or importing into the United States ATJ2085, ATJ2087, and/or ATJ2089 semiconductor devices, corresponding circuit boards, and/or products featuring such semiconductor devices, which incorporate the inventions of one or more claims of the '522 Patent.

40. Actions' infringement is causing and will continue to cause damage and irreparable injury to SigmaTel, unless and until such infringing activity is enjoined by this Court.

41. On information and belief, Actions is engaging in willful and deliberate infringement, supporting an award of enhanced damages under 35 U.S.C. § 284, and making this case exceptional for purposes of 35 U.S.C. § 285.

PRAYER FOR RELIEF

WHEREFORE, SigmaTel respectfully requests that this Court:

A. Enter judgment that Actions and Sonic Impact have infringed the '187, '279, and '522 Patents;

B. Enter Orders preliminarily and permanently enjoining Actions and Sonic Impact, as well as all of their respective affiliates, parents, subsidiaries, partners, officers, directors, employees, agents, consultants, contractors, attorneys, successors, and assigns, from making, using, selling, and offering for sale in the United States, and from importing into the United States any device that infringes, directly or indirectly, SigmaTel's '187, '279, and '522 Patents;

C. Award SigmaTel its damages in amounts sufficient to compensate it for Actions and Sonic Impact infringement of the '187, '279, and '522 Patents;

D. Award treble damages to SigmaTel for willful infringement by Actions and Sonic Impact, in accordance with 35 U.S.C. § 284;

E. Assess pre-judgment and post-judgment interest and costs against Actions and Sonic Impact, together with an award of such interests and costs, in accordance with 35 U.S.C. § 284;

F. Declare this case to be exceptional under 35 U.S.C. § 285 and to award SigmaTel its attorneys' fees, expenses, and costs incurred in connection with this action; and

G. Award SigmaTel such other and further relief as this Court deems just and proper.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure, SigmaTel respectfully demands a jury trial of any and all issues on which a trial by jury is available under applicable law.

Dated: January 4, 2005

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EXHIBIT A

US006137279A

United States Patent [19]

Ifesinachukwa et al.

[11] Patent Number: 6,137,279

[45] Date of Patent: Oct. 24, 2000

[54] **ADJUSTABLE POWER CONTROL MODULE AND APPLICATIONS THEREOF**

[75] Inventors: **Kenneth Gozie Ifesinachukwa**; **Mathew A Rybicki**, both of Austin, Tex.

[73] Assignee: **Sigmatel, Inc.**, Austin, Tex.

[21] Appl. No.: **09/376,501**

[22] Filed: **Aug. 18, 1999**

[51] **Int. Cl.**[7] **G05F 3/16**

[52] **U.S. Cl.** **323/317**; 323/274

[58] **Field of Search** 323/317, 316, 323/315, 274

[56] **References Cited**

U.S. PATENT DOCUMENTS

5,063,342	11/1991	Hughes et al.	323/315
5,142,219	8/1992	Hsu et al.	323/317
5,796,276	8/1998	Phillips et al.	323/317

Primary Examiner—Shawn Riley

Attorney, Agent, or Firm—Timothy W. Markison

[57] **ABSTRACT**

An adjustable power control module includes a supply voltage comparison circuit, a signal dependent current source, and a power regulation module. The supply voltage comparison circuit is operably coupled to compare a supply voltage with a low-powered threshold. When the supply voltage is less than the low-power threshold, the supply voltage comparison circuit provides a corresponding indication to the signal dependent current source. The signal dependent current source generates a first regulated current when the supply voltage is less than the low powered threshold based on the indication and generates a second regulated current when the supply voltage is above the low power threshold The second regulated current is larger than the first regulated current. The power regulation module provides the first or second regulated current to an associated circuit. As such, the current supplied to the circuit is regulated based on operating conditions for the circuit. As such, when operating conditions dictate that more power can be provided to the circuit, the adjustable power control module provides more current conversely when the operating conditions indicate less power, the adjustable power control module provides less power.

15 Claims, 2 Drawing Sheets

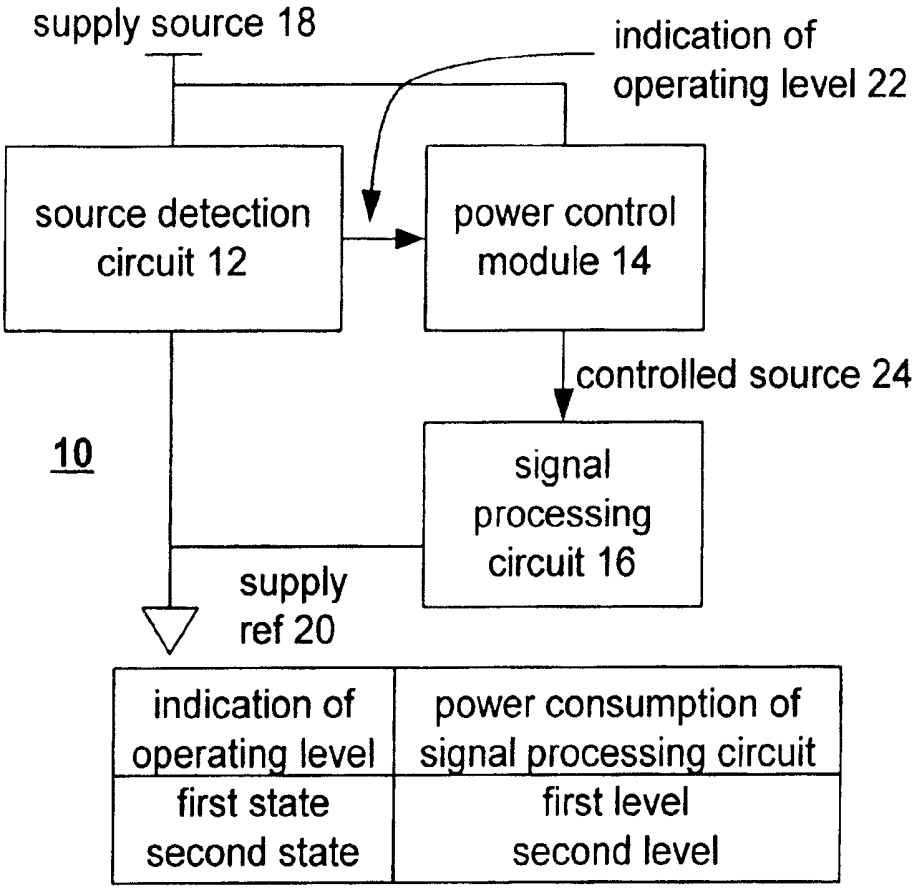

EXHIBIT A

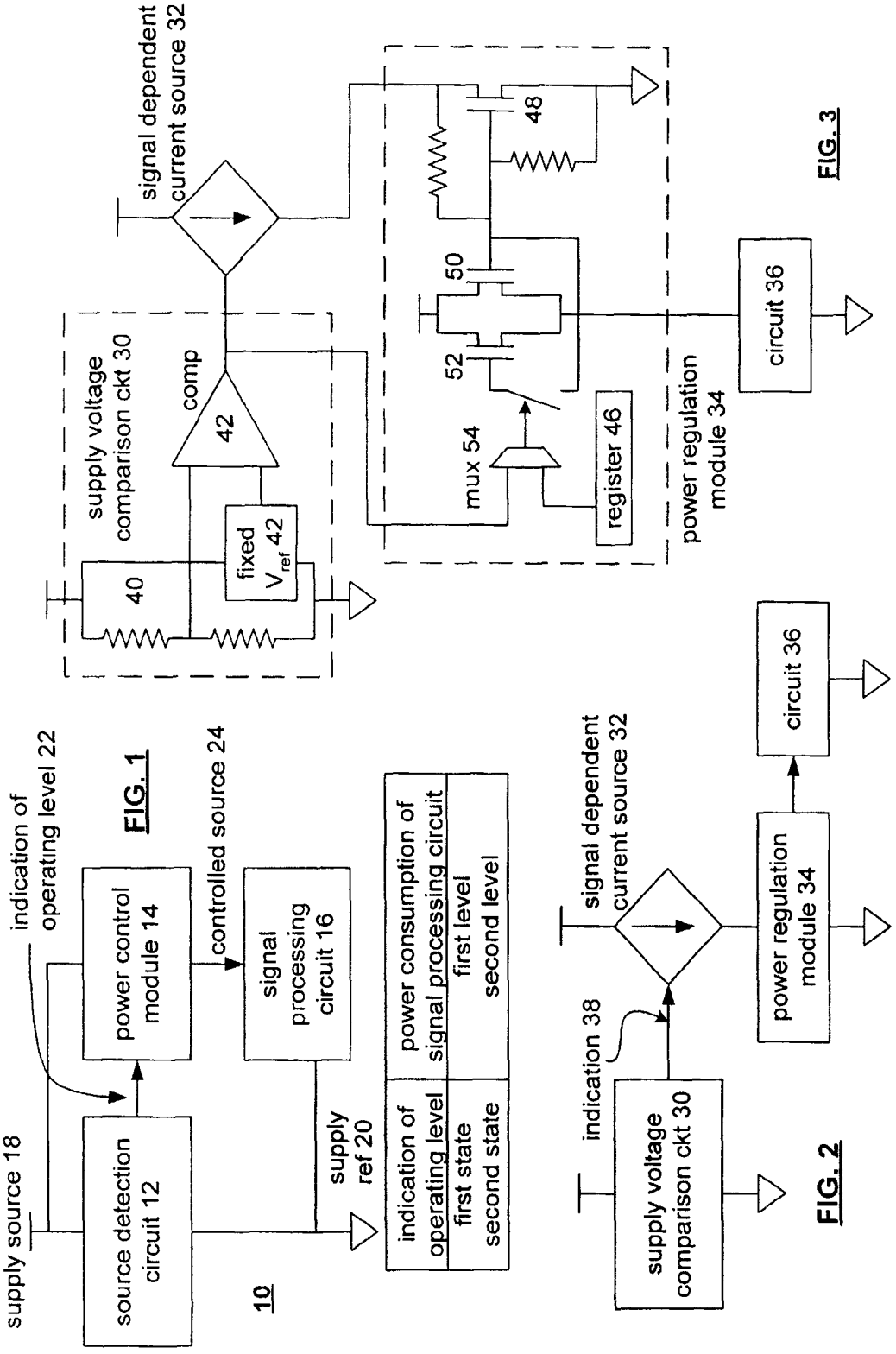

FIG. 1

FIG. 2

FIG. 3

EXHIBIT A

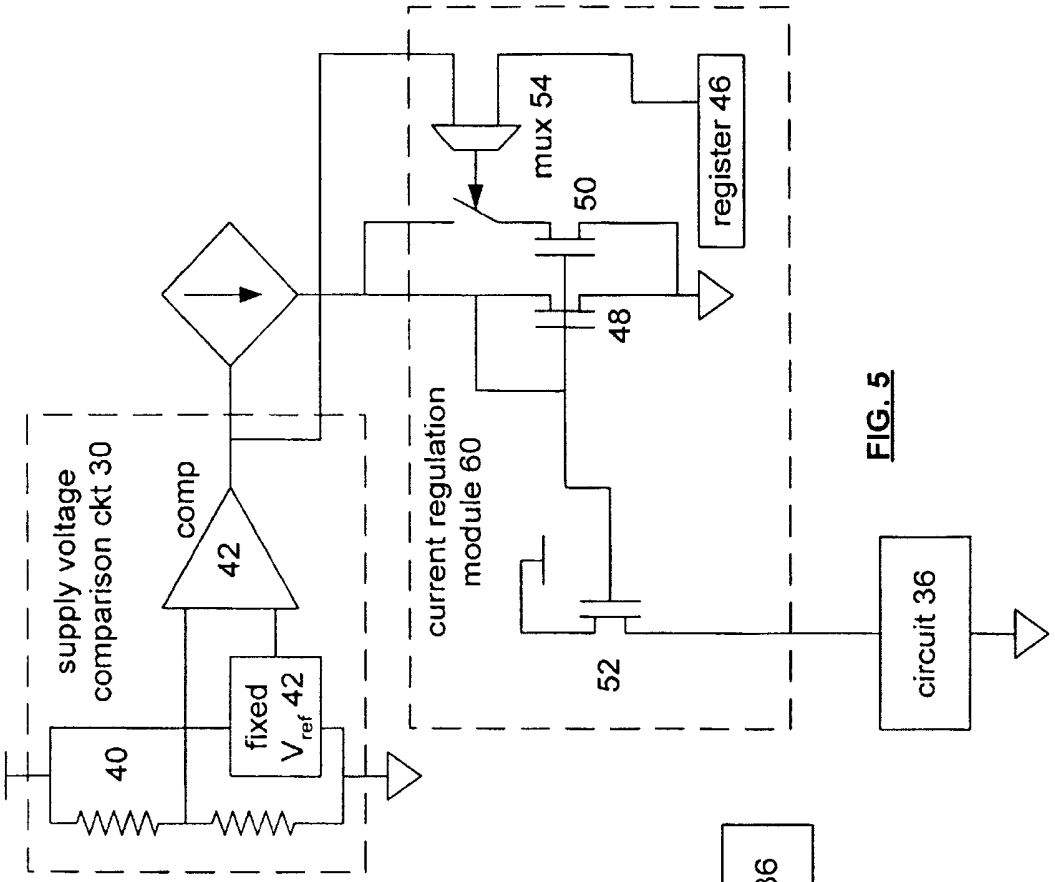

FIG. 5

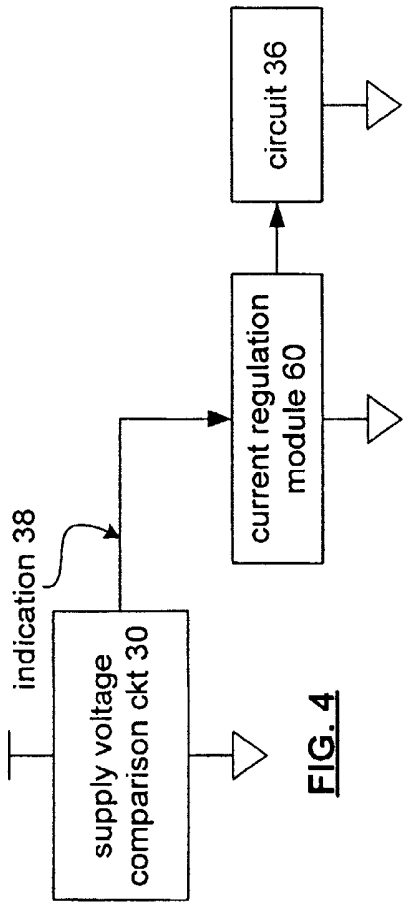

FIG. 4

EXHIBIT A

ADJUSTABLE POWER CONTROL MODULE AND APPLICATIONS THEREOF

TECHNICAL FIELD OF THE INVENTION

The present invention relates generally to power savings techniques and more particularly to an adjustable power control module that controls power consumption of an associated circuit based on certain operating conditions.

BACKGROUND OF THE INVENTION

As is known, the current trend in the design of battery operated electronic equipment is to provide enhanced performance in smaller packages, while consuming less power. Accordingly, the components comprising the electronic equipment must provide enhanced performance in smaller packages, while consuming less power. As such, designers of electronic equipment and the corresponding components have created a multitude of power saving techniques. Such techniques, however, are usually specific to a particular set of operating conditions that include supply voltage, desired performance level, and usage. For example, when a component or circuit within the electronic equipment is intermittently used, a power regulation circuit disables the component or circuit during times when it is not in use. When the component is enabled, it draws the power it needs to operate.

As is also known, many types of battery operated electronic equipment may also be externally powered (e.g., by a power supply) or may have externally powered equivalents. Such powered devices typically include similar functionality and, hence, include similar components. Components for externally powered devices, however, have less stringent power consumption requirements and typically do not employ power conservation techniques. Components of battery operated electronic equipment that may also be powered by an external source may have different power consumption requirements depending on whether the electronic equipment is being powered by a battery or an external source. Typically, components function better when supplied with more power. For example, an amplifier has lower offset and greater drive capability when supplied with greater power.

As such, the component manufacturer may make several versions of the same component, one for each of the various operating conditions and types of power sources. For integrated circuits, this requires separate mask sets, packaging, and testing, which adds to the overall cost of the component. Therefore, a need exists for an adjustable power control circuit that is adjustable based on operating conditions and the types of power sources.

BRIEF DESCRIPTION OF THE DRAWING

FIG. **1** illustrates a schematic block diagram of an adjustable power control module in accordance with the present invention;

FIG. **2** illustrates an alternate embodiment of an adjustable power control module in accordance with the present invention;

FIG. **3** illustrates a more detailed schematic block diagram of the adjustable power control module of FIG. **2**;

FIG. **4** illustrates another embodiment of an adjustable power control module in accordance with the present invention; and

FIG. **5** illustrates a more detailed schematic block diagram of the adjustable power control module of FIG. **4**.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Generally, the present invention provides an adjustable power control module that includes a supply voltage comparison circuit, a signal dependent current source, and a power regulation module. The supply voltage comparison circuit is operably coupled to compare a supply voltage with a low-powered threshold. When the supply voltage is less than the low-power threshold, the supply voltage comparison circuit provides a corresponding indication to the signal dependent current source. The signal dependent current source generates a first regulated current when the supply voltage is less than the low power threshold based on the indication and generates a second regulated current when the supply voltage is above the low power threshold. The second regulated current is larger than the first regulated current. The power regulation module provides the first or second regulated current to an associated circuit. As such, the current supplied to the circuit is regulated based on operating conditions for the circuit. As such, when operating conditions dictate that more power can be provided to the circuit, the adjustable power control module provides more current. Conversely when the operating conditions indicate less power, the adjustable power control module provides less power. In this instance, the adjustable power control module regulates the amount of power received by the circuit.

The present invention can be more fully described with reference to FIGS. **1** through **5**. FIG. **1** illustrates a schematic block diagram of an adjustable power control module **10** that includes a source detection circuit **12**, and a power control module **14**, which are coupled to a signal processing circuit **16**. The source detection circuit **12** is operably coupled between a supply source **18** and a supply reference **20**. The supply source **18** may be from a battery that produces 1.5 volts, 2.2 volts, 3 volts, 3.3 volts, 4.5 volts, 5 volts, 6 volts, 9 volts, etc. or may be from an external power supply. Regardless of the type of source, the source detection circuit provides an indication of the operating level **22** to the power control module **14**. The indication of operating level **22** may be based on the magnitude of the supply source **18**, which may be voltage and/or current. The source detection circuit **12** may further generate the indication of operating level **22** based on user inputs. For example, the user may select a desired power level to achieve a particular performance. Based on these inputs, the source detection circuit **12** produces the corresponding indication. Such will be discussed in greater detail with reference to FIG. **3**.

The power control module **14**, based on the indication of operating level **22**, generates a controlled source **24**. The signal processing circuit **16** may be digital-to-analog converter, analog-to-digital converter, digital logic circuit, an analog circuit, an amplifier, a gain stage, an adjustable gain stage, a mixing circuit, and/or any other type of digital and/or analog circuit. As such, the control source **24** dictates the power consumption of the signal processing circuit **16**. The control module **14** provides a first level of the controlled source **24** when the indication is in a first state and provides a second level of the controlled source **24** when the indication is in the second state. For example, if the first state indicates that a low power operation is to be performed, the power control module **14** provides a first low power controlled source to the signal processing circuit. Conversely, the second state of the indication may indicate a higher power of operation. As such, the second level of control source **24** is higher than the first. As one of average skill in the art will appreciate, more that two levels may be used.

As one of average skill in the art would readily appreciate the source detection circuit **12** may be implemented as further described with reference to FIGS. **2** through **5**, may be hard wired into an incorporating circuit, or may be

triggered by an external input from the adjustable power circuit. In addition, the controlled source **24** may be a controlled current and/or a controlled voltage.

FIG. **2** illustrates a schematic block diagram of an alternate embodiment of the adjustable power control module that includes a supply voltage comparison circuit **30**, a signal dependent current source **32**, a power regulation module **34**, and a circuit **36**. Note that the circuit **36** may be similar to the signal processing circuit **16** of FIG. **1**. The supply voltage comparison circuit **30** is operably coupled between the supply source and supply reference. By monitoring the supply, the supply voltage comparison circuit generates an indication **38**. The indication **38** drives the signal dependent current source **32** to produce a corresponding controlled current. The power regulation module **34** is operably coupled to receive the controlled current produced by the current source **32** which in turn provides it to the circuit **36**.

FIG. **3** illustrates a more detailed schematic block diagram of the adjustable power control module of FIG. **2**. In this illustration, the supply voltage comparison circuit **30** is shown to include a voltage divider **40**, a fixed voltage reference module **42** and a comparator **43**. The voltage divider **40** produces a representation of the supply voltage which is fed to one input of the comparator **43** and the second input of the comparator **43** is coupled to the fixed voltage reference **42**. When the representation of the supply voltage exceeds the fixed reference voltage **42**, the comparator **43** drives the signal dependent current source into a higher state. In addition, the output of comparator **43** may be provided to the power regulation module **34**. As one of average skill in the art would appreciate, the divider **40** may include more than one tab and the comparator **43** may be a plurality of comparators. In such an embodiment, one comparator may provide the control signal to the signal dependent current source **32** while a second comparator provides the signal to the power regulation module **34**. In this multi-comparator embodiment several different levels of power regulation may be achieved.

The power regulation module **34** includes a current mirror, which is comprised of transistors **48**, **50** and **52**, a multiplexor **54** and a register **46**. The register **46** is operable to receive user inputs as to the desired power consumption level The transistors **48**, **50** and **52** of the current mirror may be sized to provide a particular current ratio between the current generated by the current source **32** and the current supplied to circuit **36** Such a ratio may be in the range of 1 to 10 or 10 to 1. In operation, when the switch is open, thereby disabling transistor **52**, the current mirror is comprised of transistors **48** and **50**. If the signal dependent current source **32** generates current, it is received by transistor **48** and mirrored by transistor **50** based on the ratio between transistors **48** and **50**. The regulated current is then provided to the circuit **36**.

The switch may be closed by either information contained within register **46** or the output of comparator **43**. In either case, when the switch is closed, transistor **52** is in parallel with transistor **50** thereby changing the ratio between the transistors in the current mirror.

FIG. **4** illustrates a schematic block diagram of another embodiment of the adjustable power control module. This embodiment includes a supply voltage comparison circuit **30**, a current regulation module **60** and a circuit **36**. The supply voltage comparison circuit **30** provides an indication **38** to the current regulation module **60**. In response, the current regulation module provides a controlled source to circuit **36**

FIG. **5** illustrates a more detailed schematic block diagram of the adjustable power control module of FIG. **4**. As shown, the supply voltage comparison circuit **30** is similar to the circuit described in FIG. **3**. The current regulation module **60** is similar to the power regulation module **34** of FIG. **3** but differs in the doubling of the transistors within the current mirror. In this embodiment, the current regulation module includes a current mirror that includes transistors **48**, **50** and **52**. In this embodiment, the transistors **48** and **50** are operably coupled to the current source while transistor **52** is coupled to the circuit. In this embodiment, when transistor **50** is open, the current mirror has a ratio between transistor **48** and **52**. When the switch is closed, thereby paralleling transistor **50** with transistor **48**, the current ratio in the current mirror is based on the parallel combination of transistor **50** and **48** to the transistor **52**. If transistors **50** and **52** are of the same size, by paralleling transistor **52**, the supply current is doubled.

The preceding discussion has presented various embodiments of an adjustable power control module. By utilizing such a power control module in integrated circuit design, a single integrated circuit may be generated and used with various power sources and under various operating conditions. As one of average skill in the art would appreciate, other embodiments may be derived from the teachings presented herein without deviating from the scope of the present invention.

What is claimed is:

1. An adjustable power control module comprises:

a supply voltage comparison circuit operably coupled to compare a supply voltage with a low power threshold, wherein the supply voltage comparison circuit provides a low power indication when the supply voltage compares unfavorably with the low power threshold;

a signal dependent current source operably coupled to provide a regulated current, wherein the signal dependent current source provides a first regulated current when the low power indication indicates the unfavorable comparison and provides a second regulated current when the low power indication indicates a favorable comparison; and

power regulation module operably coupled to the signal dependent current source and to a circuit, wherein the power regulation module regulates power consumption of the circuit in accordance with the first or second regulated currents.

2. The adjustable power control module of claim **1**, wherein the supply voltage comparison circuit further comprises a fixed reference voltage, a comparator, and a voltage divider, wherein a first input of the comparator is operably coupled to the fixed reference voltage, and a second input of the comparator is operably coupled to the voltage divider that divides the supply voltage.

3. The adjustable power control module of claim **1**, wherein the power regulation module further comprises a current mirror circuit having a predetermined current ratio, wherein a first transistor of the current mirror is operably coupled to the supply voltage and the circuit, and wherein a second transistor of the current mirror is operably coupled to the signal dependent current source.

4. The adjustable power control module of claim **3**, wherein the power regulation module further comprises a third transistor operably coupled to provide a second predetermined current ratio, wherein the third transistor is enable to provide the second predetermined current ratio when the supply voltage compared favorably with the low power threshold.

EXHIBIT A

5. The adjustable power control module of claim 4, wherein the power regulation module further comprises a register that stores power setting, wherein when the power setting are enabled to select the first or second predetermined current ratio, the power regulation circuit provides the first or second predetermined current in accordance with the power setting.

6. An adjustable power control module comprises:

a supply voltage comparison circuit operably coupled to compare a supply voltage with a low power threshold, wherein the supply voltage comparison circuit provides a first power indication when the supply voltage compares unfavorably with the low power threshold and provides a second power indication when the supply voltage compares favorably with the low voltage power threshold; and

current regulation module operably coupled to the supply voltage comparison circuit and to a circuit, wherein the current regulation module regulates current provided to the circuit in accordance with the first or second power indications.

7. The adjustable power control module of claim 6, wherein the supply voltage comparison circuit further comprises a fixed reference voltage, a comparator, and a voltage divider, wherein a first input of the comparator is operably coupled to the fixed reference voltage, and a second input of the comparator is operably coupled to the voltage divider that divides the supply voltage.

8. The adjustable power control module of claim 6, wherein the current regulation module further comprises a current mirror that includes first, second, and third transistors, wherein the first transistor is operably coupled to the supply voltage and the circuit, wherein the second transistor is operably coupled to the supply voltage comparison circuit, wherein the third transistor is operably coupled to the supply voltage comparison circuit, and wherein the first transistor mirrors a first current through the second transistor when the supply voltage comparison circuit provides the first power indication and the first transistor mirrors a second current through the second and third transistors when the supply voltage comparison circuit provides the second power indication.

9. The adjustable power control module of claim 8, wherein the current regulation module further comprises a register that stores power setting, wherein, when the power setting are enabled to override the first or second power indications, the current regulation module provides the first or second current in accordance with the power setting.

10. A circuit having controlled power consumption comprises:

source detection circuit operable to detect an operating level of a supply source and to provide an indication of the operating level of the supply source;

a signal processing circuit operably coupled to receive a signal and to produce therefrom a processed signal; and

power control module operably coupled to the source detection circuit and to the signal processing circuit, wherein the power control module controls the power consumption of the signal processing circuit to a first power consumption level when the indication of the operating level of the supply source is in a first state and controls the power consumption of the signal processing circuit to a second power consumption level when the indication of the operating level of the supply source is in a second state.

11. The circuit of claim 10, wherein the signal processing circuit comprises at least one of: a digital to analog converter, an analog to digital converter, a digital logic circuit, an analog circuit, an amplifier, a gain stage, an adjustable gain state, and a mixing circuit.

12. The circuit of claim 10, wherein the source detection circuit comprises a comparison circuit that includes a fixed reference voltage, a comparator, and a voltage divider, wherein a first input of the comparator is operably coupled to the fixed reference voltage, and a second input of the comparator is operably coupled to the voltage divider that divides a supply voltage.

13. The circuit of claim 10, wherein the source detection circuit comprises a comparison circuit that includes a fixed reference current, a comparator, and a current divider, wherein a first input of the comparator is operably coupled to the fixed reference current, and a second input of the comparator is operably coupled to the current divider that divides a supply current.

14. The circuit of claim 10, wherein the source detection circuit comprises an analog to digital converter operably coupled to convert the supply source into a digital signal that provides the indication of the operating level of the supply source.

15. The circuit of claim 10, wherein the power control module comprises:

a signal dependent current source operably coupled to provide a regulated current, wherein the signal dependent current source provides a first regulated current when the indication of the operating level of the supply source is in the first state and provides a second regulated current when the indication of the operating level of the supply source is in the second state; and

power regulation module operably coupled to the signal dependent current source and to the signal processing circuit, wherein the power regulation module regulates the power consumption of the signal processing circuit in accordance with the first or second regulated currents.

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EXHIBIT A

EXHIBIT B

(12) **United States Patent**
May et al.

(10) **Patent No.: US 6,633,187 B1**
(45) **Date of Patent: Oct. 14, 2003**

(54) **METHOD AND APPARATUS FOR ENABLING A STAND ALONE INTEGRATED CIRCUIT**

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(73) Assignee: **Sigmatel, Inc.**, Austin, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 186 days.

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(22) Filed: **Nov. 20, 2000**

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(52) **U.S. Cl.** **327/198**; 327/544
(58) **Field of Search** 327/142, 143, 327/198, 538, 539, 540, 544, 545

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Primary Examiner—Timothy P. Callahan
Assistant Examiner—An T. Luu
(74) *Attorney, Agent, or Firm*—Timothy W. Markison

(57) **ABSTRACT**

A method and apparatus for enabling a stand-alone integrated circuit (IC) includes processing that begins by establishing an idle state that holds at least a portion of the stand-alone integrated circuit in a reset condition when a power source is operably coupled to the stand-alone integrated circuit. A stand-alone integrated circuit includes generally an on-chip power converter, a reset circuit and some functional circuitry, which may be a microprocessor, digital signal processor digital circuitry, state machine, logic circuitry, analog circuitry, and/or any type of components and/or circuits that perform a desired electrical function. When a power enable signal is received, the on-chip power converter is enabled to generate at least 1 supply from the power source. The processing continues by enabling functionality of the stand-alone integrated circuit when the at least one supply has substantially reached a steady state condition.

20 Claims, 4 Drawing Sheets

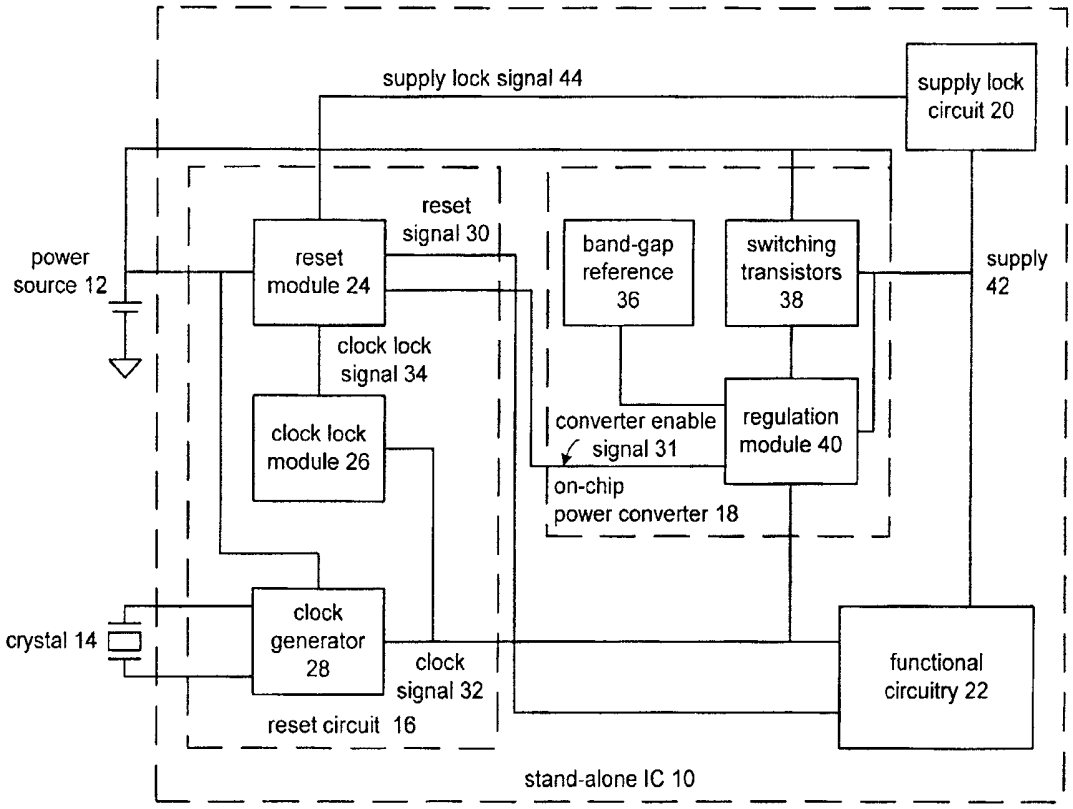

EXHIBIT B

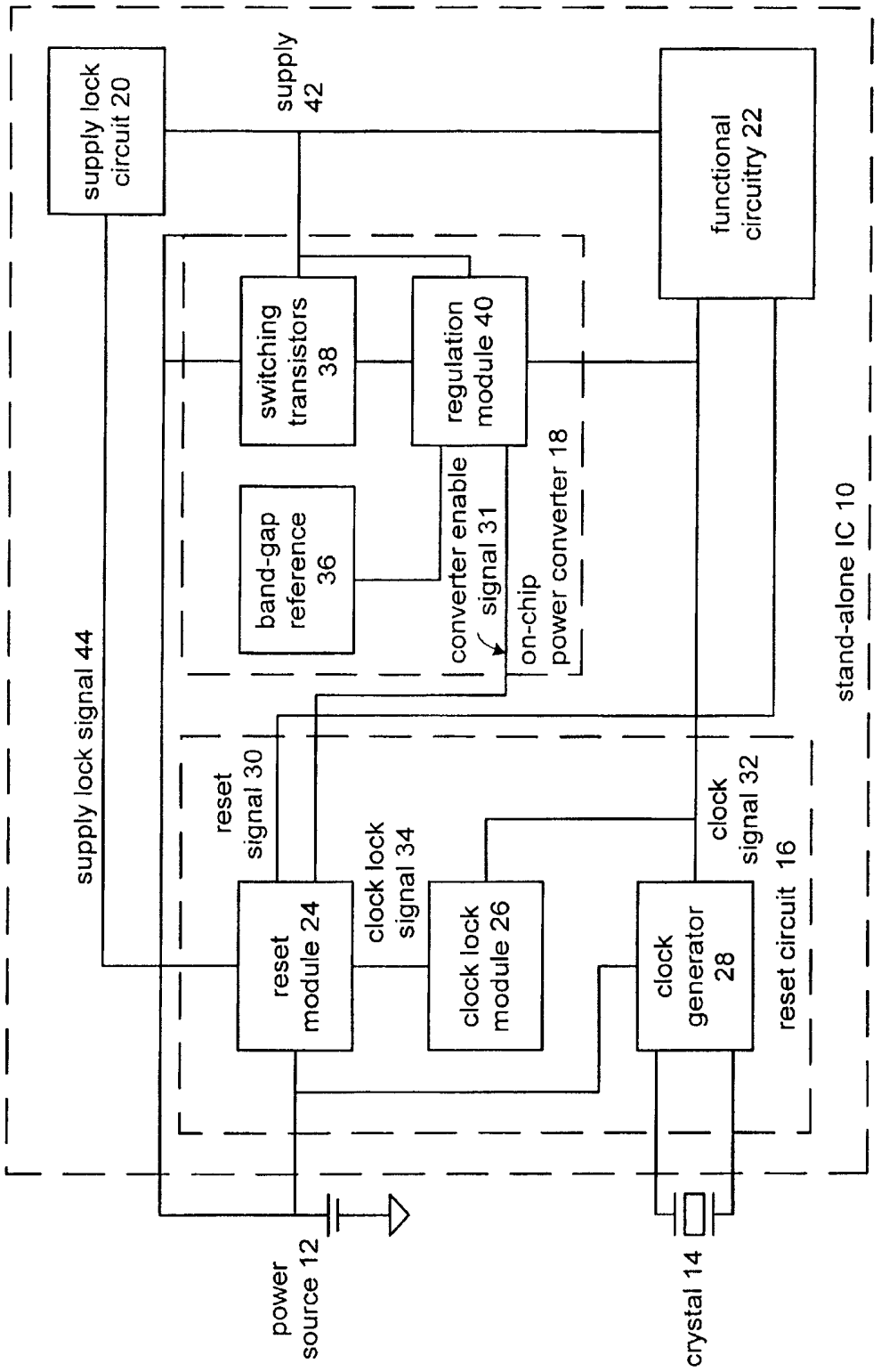

FIG. 1

EXHIBIT B

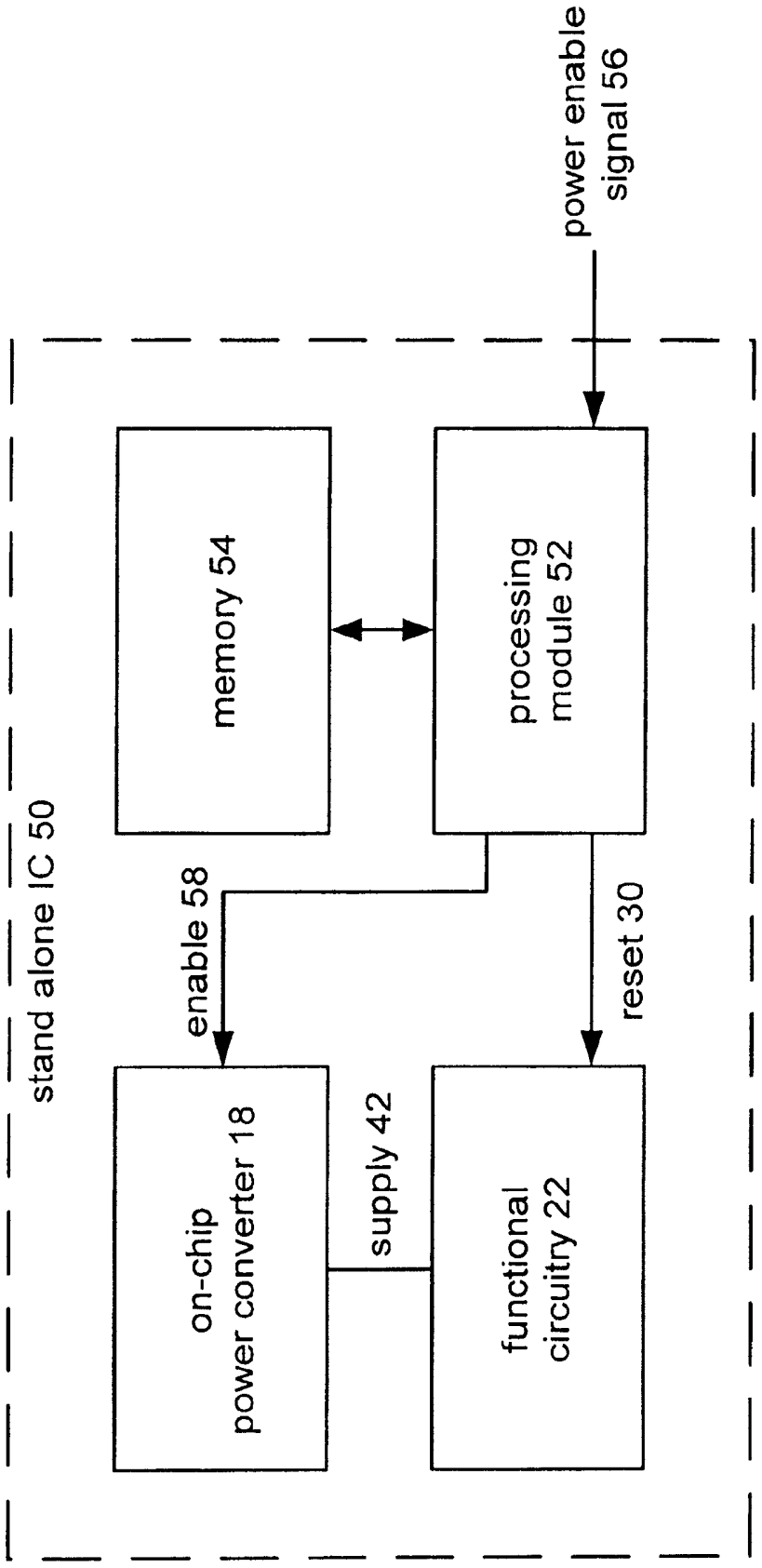

FIG. 2

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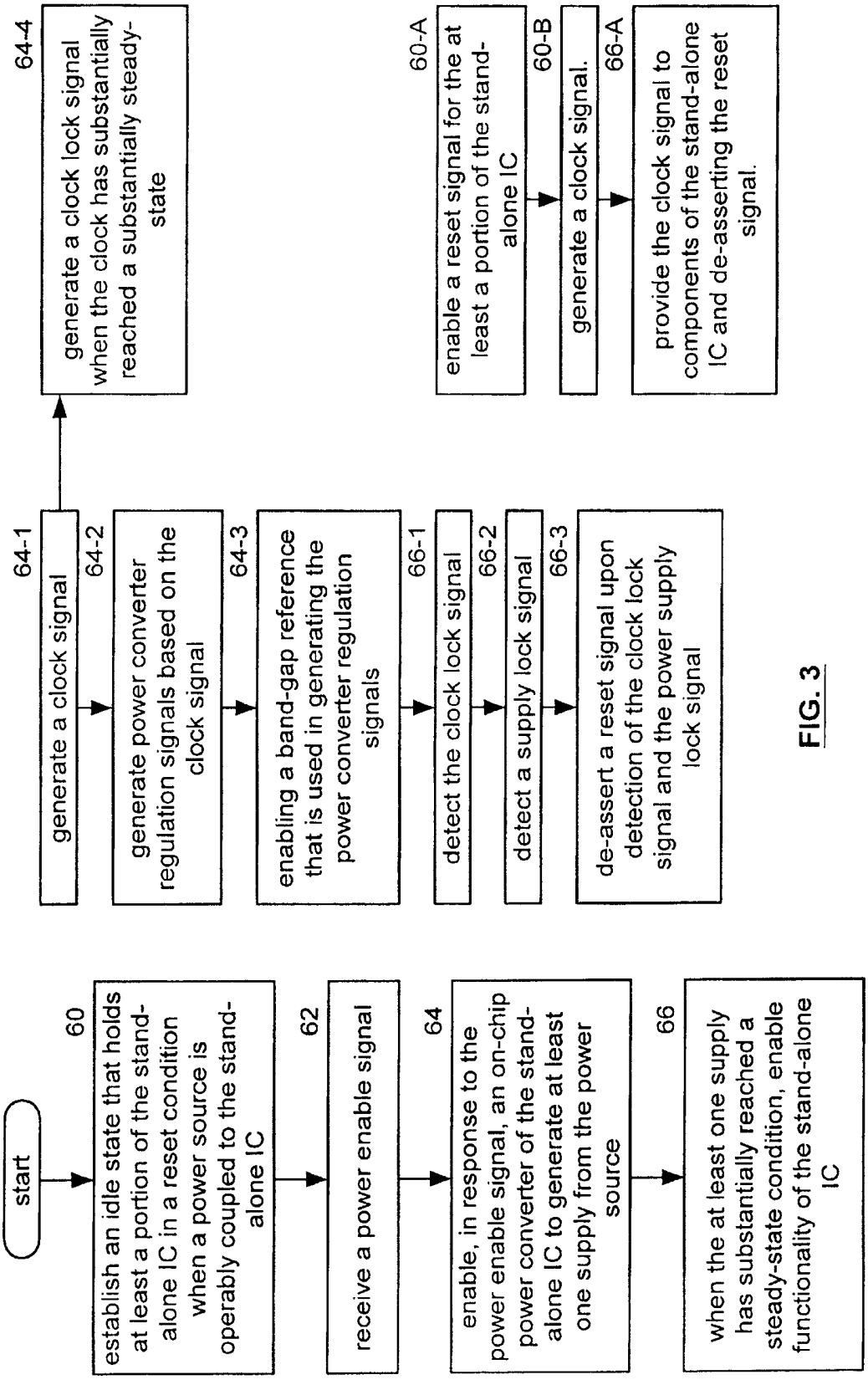

FIG. 3

EXHIBIT B

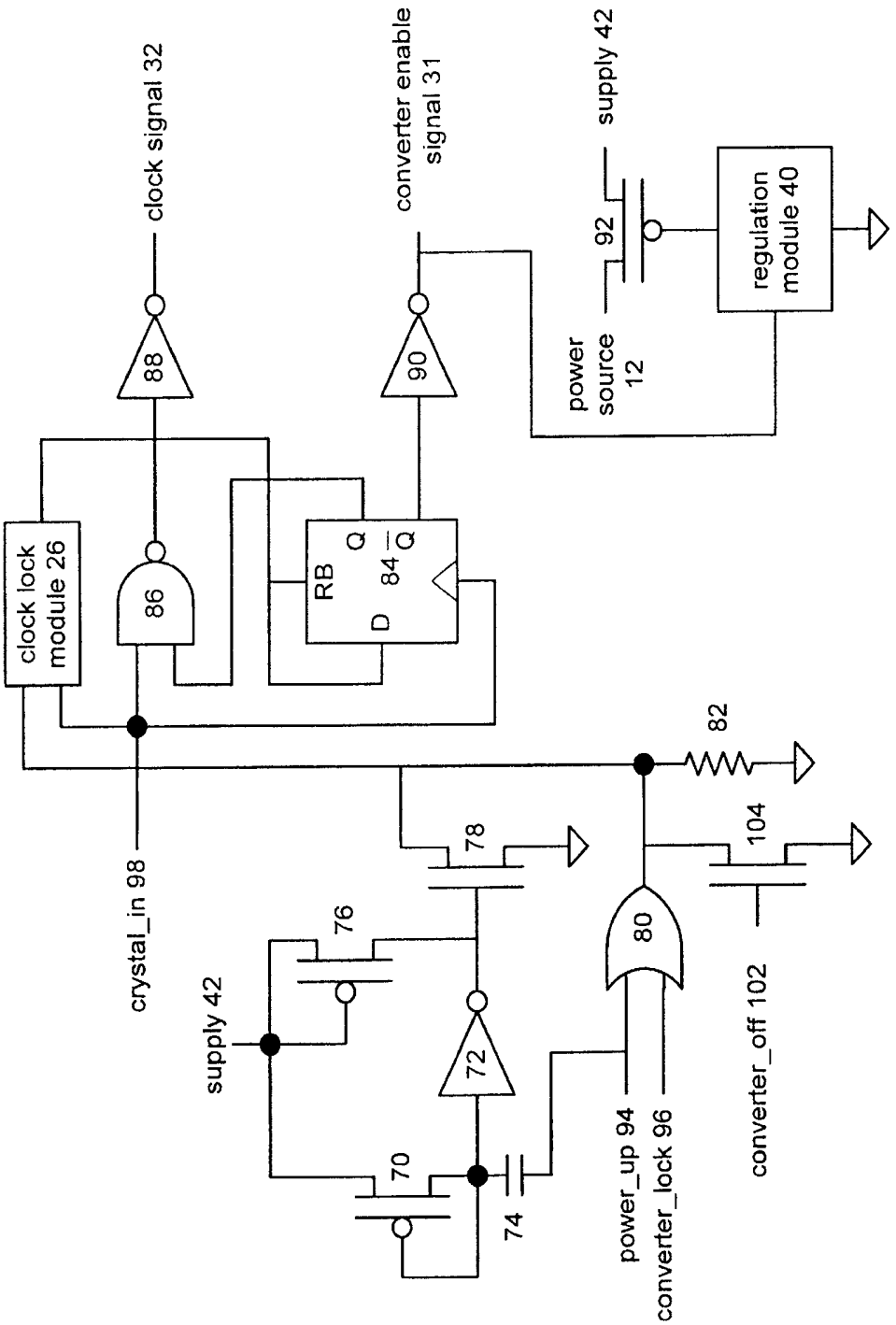

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FIG. 4

EXHIBIT B

METHOD AND APPARATUS FOR ENABLING A STAND ALONE INTEGRATED CIRCUIT

TECHNICAL FIELD OF THE INVENTION

This invention relates generally to integrated circuits and more particularly to enabling a stand-alone integrated circuit.

BACKGROUND OF THE INVENTION

Integrated circuits are known to include a large amount of circuitry in a very small area. The circuitry may perform a wide variety of functions such as a microprocessor, digital signal processor, operational amplifier, integrator, audio encoder, audio decoder, video encoder, video decoder, et cetera To power such integrated circuits, the integrated circuits include power pins for a power input (typically V_{dd}) and a return pin (typically V_{ss}). The power is typically provided by a regulated external power supply. As such, once the external power supply is up and running, the integrated circuit may be activated in a known state.

For most digital circuits on an integrated circuit, a clock signal is needed. The clock is typically generated once an external power supply is producing a regulated supply voltage to the integrated circuit (IC) and the IC has been activated. To ensure that the digital circuitry begins functioning in a known state, it is important to delay activation of the digital circuit until the power supply is producing a stable supply voltage and the clock is operating properly. Once these operating parameters are ensured, the digital circuitry may be activated.

Insuring the proper enablement of an IC is relatively straightforward when the power supply is external to the IC. If, however, the power converter is on-chip with the digital circuitry and the power converter requires a clock signal to produce a supply voltage, a difficulty arises in enabling such a stand-alone integrated circuit.

Therefore, a need exists for a method and apparatus for enabling a stand-alone integrated circuit that includes an on-chip power converter.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a schematic block diagram of a stand-alone integrated circuit in accordance with the present invention;

FIG. 2 illustrates a schematic block diagram of an alternate stand-alone integrated circuit in accordance with the present invention;

FIG. 3 illustrates a logic diagram of a method for enabling a stand-alone integrated circuit in accordance with the present invention; and

FIG. 4 illustrates a schematic block diagram of an embodiment of the reset circuit of FIG. 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Generally, the present invention provides a method and apparatus for enabling a stand-alone integrated circuit (IC). Such a method and apparatus includes processing that begins by establishing an idle state that holds at least a portion of the stand-alone integrated circuit in a reset condition when a power source is operably coupled to the stand-alone integrated circuit. A stand-alone integrated circuit includes generally an on-chip power converter, a reset circuit and some functional circuitry which may be a microprocessor, digital signal processor, digital circuitry, state machine, logic circuitry, analog circuitry, and/or any type of components and/or circuits that perform a desired electrical function. When a power enable signal is received, the on-chip power converter is enabled to generate at least 1 supply (e.g. a voltage supply or current supply) from the power source (e.g. a battery). The processing continues by enabling functionality of the stand-alone integrated circuit when the at least one supply has substantially reached a steady state condition. With such a method and apparatus, a stand-alone integrated circuit may be properly enabled such that when the functional circuitry of a stand-alone integrated circuit is enabled it is enabled in a known state to ensure proper operation of the integrated circuit.

The present invention can be more fully described with reference to FIGS. **1** through **4**. FIG. **1** illustrates a schematic block diagram of a stand-alone integrated circuit **10** that includes a reset circuit **16**, an on-chip power converter **18**, functional circuitry **22**, and a supply lock circuit **20**. The stand-alone integrated circuit **10** is operably coupled to an external power source **12**, which may be a battery, solar power generator, or other power source that produces a voltage that is not the proper voltage for powering at least a portion of the stand-alone integrated circuit **10**. The stand-alone integrated circuit **10** is also operably coupled to an external crystal **14** that provides an oscillation to the reset circuit **16**.

The reset circuit **16** includes a reset module **24**, a clock lock module **26**, and a clock generator **28**. When the power source **12** and the crystal **14** are coupled to the stand-alone integrated circuit **10**, the clock generator **28** produces a clock signal **32**. The clock lock module **26** monitors the clock signal **32** to determine when it has reached a steady state condition. The clock signal **32** has reached a steady state condition typically when it is producing a clock signal at approximately 10% of the ideal frequency of the desired clock signal. Note that the reset circuit **16** will hold the power converter enable signal **31** in an inactive state until the clock lock signal **34** is asserted.

The reset module **24** holds the reset signal **30** low such that the functional circuitry **22** is held in an idle condition until the supply lock signal **44** is asserted as well as the clock lock signal **34**. The function of circuitry **22** may be a microprocessor, digital signal processor, state machine, logic circuitry, analog circuitry, and/or any combination of electrical components to perform a desired electrical response given an electrical stimulus.

The on-chip power converter **18** includes a band-gap reference **36**, switching transistors **38** and a regulation module **40**. The on-chip power converter **18** remains inactive until a power enable signal is asserted. Once asserted, the band-gap reference **36** generates a reference voltage that is supplied to the regulation module **40**. The regulation module **40** receives the clock signal **32** and generates control signals that are provided to the switching transistors **38**. Based on the control signals, the switching transistors **38** produce a regulated supply **42**. The supply lock signal **20** and the functional circuitry **22** receive the regulated supply **42**. For a more detailed discussion of the on-chip power converter **18**, refer to co-pending patent application having a docket number of SIG000010, entitled METHOD AND APPARATUS FOR REGULATING A DC OUTPUT VOLTAGE, having a Ser. No. of 09/551,123, and a filing date of Apr. 18, 2000.

The supply lock circuit **20** receives the supply **42** and determines when it has reached a steady state. The supply

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lock circuit **20** determines that the supply **42** reaches a steady state when the supply reaches at least 90% of its desired value. When this occurs, the supply lock circuit **20** generates a supply lock signal **44**.

The reset module **24** receives the supply lock signal **44** and, if the clock lock signal **34** is enabled, the reset module **24** clears the reset signal **30** thus removing the functional circuitry **22** from the idle state. Once removed from the idle state, the functional circuitry **22** may perform its desired function(s). As one of average skill in the art will appreciate, multiple functional circuits may be included on the stand-alone integrated circuit where each functional circuit may be controlled by the reset circuit **16** or may each have its own corresponding reset circuit **16**. The on-chip power converter **18** may produce multiple supply voltages for powering different types of functional circuitries. For example, analog circuitry may require a 5 volt supply while digital circuitry may require a 3 volt supply. As one of average skill in the art may further appreciate, the clock signal **32** may be delayed from generation until the power enable signal is activated as opposed to being generated upon application of power source **12**.

FIG 2 illustrates a schematic block diagram of an alternate stand-alone integrated circuit **50**. The stand-alone integrated circuit **50** includes the on-chip power converter **18**, the functional circuitry **22**, a processing module **52**, and memory **54**. The processing module **52** may be a single processing device or a plurality of processing devices. Such a processing device may be a microprocessor, microcomputer, digital signal processor, state machine, logic circuitry, and/or any device that manipulates signals (analog or digital) based on operational instructions. The memory **54** may be a single memory device or a plurality of memory devices. Such a memory device may be read only memory, random access memory, system memory, and/or any device that stores digital information. Note that when the processing module **52** implements one or more of its functions via a state machine or logic circuit, the memory storing the corresponding operational instruction is embedded within the circuitry comprising the state machine and/or logic circuit.

In general, the processing module **52** receives a power enable signal **56**. Based on the power enable signal, the processing module performs a plurality of processing steps, which are discussed in greater detail with reference to FIG. **3**, to produce an enable signal **58**. The enable signal **58** causes the on-chip power converter **18** to produce supply **42**. Once the supply **42** reaches a steady state, the processing module **52** clears the reset signal **30** such that the functional circuit **22** may become active.

FIG. **3** illustrates a logic diagram of a method for enabling a stand-alone integrated circuit. The process begins at Step **60** where an idle state is established. The idle state holds at least a portion of the stand-alone integrated circuit in a reset condition when a power source is operably coupled to the stand-alone integrated circuit. For example, when a battery is coupled to the stand-alone integrated circuit the functional circuitry is held in an idle, or inactive state. The process then proceeds to Step **62** where a power enable signal is received. The process then proceeds to Step **64** where, in response to the power enable signal, an on-chip power converter of the stand-alone integrated circuit is enabled to generate at least one supply from the power source. The on-chip power converter may produce one or more supplies, which may be a voltage supply, or a current supply, for powering different functional circuits of the stand-alone integrated circuit. The process then proceeds to Step **56** where the functional circuitry of the stand-alone circuit is enabled when the at least one supply has substantially reached a steady state condition.

Processing Steps **64** and **66** may be described in further detail with reference to Steps **64-1** through **64-4** and Steps **66-1** through **66-3**. At Step **64-1**, a clock signal is generated. The processing then proceeds to Step **64-2** and Step **64-4**. At Step **64-4**, a clock lock signal is generated when the clock has substantially reached a steady state condition. At Step **64-2**, power converter regulation signals are generated based on the clock signal. The process then proceeds to Step **64-3** where a band-gap reference is enabled. The band-gap reference is used to generate the power converter regulation signals. The process then proceeds to Step **66-1** where the clock lock signal is detected. The process then proceeds to Step **66-2** where a supply lock signal is detected. The process then proceeds to Step **66-3** where the reset signal is de-asserted upon detection of the clock lock signal and the power supply lock signal.

The processing of Step **60** may further be described with reference to Steps **60-A** to Step **60-B** and Step **66-A**. At Step **60-A**, a reset signal is enabled for at least a portion of the stand-alone integrated circuit. The portion of the stand-alone integrated circuit may be for a corresponding functional circuitry where each functional circuitry has its own reset signal or the reset signal may be applicable for the entire integrated circuit. The process then proceeds to Step **60-B** where a clock signal is generated. The process then proceeds to Step **66-A** where the clock signal is provided to the components of the stand-alone integrated circuit and the reset signal is de-asserted.

FIG. **4** illustrates a schematic block diagram of an embodiment of the reset circuit **16**. The reset circuit **16** includes P-channel transistors **70** and **76**, N-channel transistors **78** and **104**, and logic elements **72, 80, 86, 88, 84**, and **90**. Also shown in FIG. **4** are the regulation module **40**, a transistor **92** of the switching transistors **38**, and the clock lock module **26**.

When the power source **12** is coupled to the stand-alone integrated circuit and the power enable, or power-up signal **94**, has not been activated, resistor **82** holds the output of OR gate **80** low such that the power converter enable signal **31** is low. The regulation module **40** then pulls the gate of transistor **92** low, making the power source **12** substantially equal to the power supply **42**. By enabling the power source to be coupled to the supply **42** in this manner, power can be provided to limited portions of the stand-alone integrated circuit including portions of the reset circuit **16** and the clock generator **28**. With the power source connected to the stand-alone integrated circuit and the crystal **14** connected to the stand-alone integrated circuit, a crystal input **98** is provided to an input of a NAND gate **86** and to an input of the clock lock module **26**. The other input of NAND gate **86** is received from the non-inverting output of D flip-flop **84**. The output of NAND gate **86** is coupled to inverter **88** wherein the output of inverter **88** is the clock signal **32**. The inverting output of D flip-flop **84** is coupled to inverter **90** wherein the output of inverter **90** corresponds to the power converter enable signal **31**. The other input of the clock lock module **26** is the output of the logic gate **38**. The output of the clock lock module **26** is connected to the RB and D inputs of the D-flip-flop **84**.

When the power-up signal **94** is enabled, the output of OR gate **80** goes high thereby enabling the clock lock module **26**. Once the output of the clock lock module **26** goes high, the power converter enable signal **31** is activated. This

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causes the regulation module **40** to provide a control signal to transistor **92** such that the supply **42** is generated at the desired output level. Once the supply has reached a steady state condition, the converter lock signal **96** is generated thereby holding the output of OR gate **80** high. Note that the reset signal **30** could be generates as a signal equivalent to the converter lock signal **96** or as a logic AND of the converter lock signal **96** and the output of the clock lock module **26**.

When the on-chip converter is turned off, the converter off signal **102** is activated high thereby enabling transistor **104**. This actively pulls down on the output of logic gate **80** causing the clock lock module **26** to be disabled. This, in turn, resets the D flip-flop **84** and returns the regulation module **40** to a reset condition.

The preceding discussion has presented a method and apparatus for enabling a stand-alone integrated circuit. A stand-alone integrated circuit includes its own on-chip power converter such that an appropriate sequence of enabling the circuitry is performed to conserve power and to insure accurate startup of the integrated circuit As one of average skill in the art will appreciate, other embodiments may be derived from the teaching of the present invention without deviating from the scope of the claims or spirit of the invention.

What is claimed is:

1. A method for enabling a stand-alone integrated circuit (IC), the method comprises the steps of:

a) establishing an idle state that holds at least a portion of the stand-alone IC in a reset condition when a power source is operably coupled to the stand-alone IC;

b) receiving a power enable signal;

c) enabling, in response to the power enable signal, an on-chip power converter of the stand-alone IC to generate at least one supply from the power source, wherein the enabling includes:

generating a clock signal;

generating power converter regulation signals based on the clock signal;

enabling a band-gap reference that is used in generating the power converter regulation signals; and

d) when the at least one supply has substantially reached a steady-state condition, enabling functionality of the stand-alone IC.

2. The method of claim **1**, wherein the establishing the idle state further comprises enabling a reset signal for the at least a portion of the stand-alone IC.

3. The method of claim **2**, wherein the establishing the idle state further comprises generating a clock signal.

4. The method of claim **3**, wherein the enabling of the functionality of the stand-alone IC further comprises providing the clock signal to components of the stand-alone IC and de-asserting the reset signal.

5. The method of claim **2**, wherein the establishing the idle state further comprises generating a clock signal.

6. The method of claim **1**, wherein the enabling the on-chip converter further comprises:

generating a first supply from the power source; and

generating a second supply from the power source, wherein the first and second supplies are produced by regulating energy transfer from a single inductor.

7. The method of claim **1** further comprises generating a clock lock signal when the clock has substantially reached a substantially steady-state.

8. The method of claim **7**, wherein the enabling functionality of the stand-alone IC further comprises:

detecting the clock lock signal; and

detecting a supply lock signal; and

de-asserting a reset signal upon detection of the clock lock signal and the power supply lock signal.

9. A stand-alone integrated circuit (IC) comprises:

a reset circuit operable to place the stand-alone IC in an idle state until a supply lock signal is enabled;

an on-chip power converter that generates a supply from an external power source upon assertion of a power enable signal; and

supply lock circuit operably coupled to enable the supply lock signal when the supply substantially reaches a steady-state condition.

10. The stand-alone IC of claim **9**, wherein the on-chip power converter further comprises:

switching transistors operably coupled to produce a first supply and a second supply from the external power source and a single inductor, and

regulation module operably coupled to the switching transistors, wherein the regulation module produces control signals that enable and disable transistors of the switching transistors to regulate the first and second supplies.

11. The stand-alone IC of claim **9**, wherein the reset circuit further comprises:

clock generator operably coupled to produce a clock signal when the external power source is coupled to the standalone IC, wherein the clock signal is provided to the on-chip power converter such that the on-chip power converter generates the supply;

clock lock module operably coupled to generate a clock lock signal when the clock signal has substantially reached a steady-state condition;

reset module operably coupled to assert a reset signal when the external power source is coupled to the stand-alone IC, wherein the reset module de-asserts the reset signal when the clock lock signal and the supply lock signal are asserted such that functionality of the stand-alone IC is enabled.

12. The stand-alone IC of claim **9**, wherein the on-chip power converter further comprises:

a band-gap reference that produces a reference voltage upon assertion of the power enable signal.

13. A stand-alone IC comprises:

on-chip power converter;

processing module; and

memory operably coupled to the processing module, wherein the memory includes operational instructions that cause the processing module to:

establish an idle state that holds at least a portion of the stand-alone IC in a reset condition when a power source is operably coupled to the stand-alone IC;

receive a power enable signal;

enable, in response to the power enable signal, the on-chip power converter of the stand-alone IC to generate at least one supply from the power source; and

when the at least one supply has substantially reached a steady-state condition, enable functionality of the stand-alone IC.

14. The stand-alone IC of claim **13**, wherein the memory further comprises operational instructions that cause the processing module to enable the on-chip converter further comprises:

EXHIBIT B

causes the regulation module **40** to provide a control signal to transistor **92** such that the supply **42** is generated at the desired output level. Once the supply has reached a steady state condition, the converter lock signal **96** is generated thereby holding the output of OR gate **80** high. Note that the reset signal **30** could be generates as a signal equivalent to the converter lock signal **96** or as a logic AND of the converter lock signal **96** and the output of the clock lock module **26**.

When the on-chip converter is turned off, the converter off signal **102** is activated high thereby enabling transistor **104**. This actively pulls down on the output of logic gate **80** causing the clock lock module **26** to be disabled. This, in turn, resets the D flip-flop **84** and returns the regulation module **40** to a reset condition.

The preceding discussion has presented a method and apparatus for enabling a stand-alone integrated circuit. A stand-alone integrated circuit includes its own on-chip power converter such that an appropriate sequence of enabling the circuitry is performed to conserve power and to insure accurate startup of the integrated circuit. As one of average skill in the art will appreciate, other embodiments may be derived from the teaching of the present invention without deviating from the scope of the claims or spirit of the invention.

What is claimed is:

1. A method for enabling a stand-alone integrated circuit (IC), the method comprises the steps of:

a) establishing an idle state that holds at least a portion of the stand-alone IC in a reset condition when a power source is operably coupled to the stand-alone IC;

b) receiving a power enable signal;

c) enabling, in response to the power enable signal, an on-chip power converter of the stand-alone IC to generate at least one supply from the power source, wherein the enabling includes:

generating a clock signal;

generating power converter regulation signals based on the clock signal;

enabling a band-gap reference that is used in generating the power converter regulation signals; and

d) when the at least one supply has substantially reached a steady-state condition, enabling functionality of the stand-alone IC.

2. The method of claim **1**, wherein the establishing the idle state further comprises enabling a reset signal for the at least a portion of the stand-alone IC.

3. The method of claim **2**, wherein the establishing the idle state further comprises generating a clock signal.

4. The method of claim **3**, wherein the enabling of the functionality of the stand-alone IC further comprises providing the clock signal to components of the stand-alone IC and de-asserting the reset signal.

5. The method of claim **2**, wherein the establishing the idle state further comprises generating a clock signal.

6. The method of claim **1**, wherein the enabling the on-chip converter further comprises:

generating a first supply from the power source; and

generating a second supply from the power source, wherein the first and second supplies are produced by regulating energy transfer from a single inductor.

7. The method of claim **1** further comprises generating a clock lock signal when the clock has substantially reached a substantially steady-state.

8. The method of claim **7**, wherein the enabling functionality of the stand-alone IC further comprises:

detecting the clock lock signal; and

detecting a supply lock signal; and

de-asserting a reset signal upon detection of the clock lock signal and the power supply lock signal.

9. A stand-alone integrated circuit (IC) comprises:

a reset circuit operable to place the stand-alone IC in an idle state until a supply lock signal is enabled;

an on-chip power converter that generates a supply from an external power source upon assertion of a power enable signal; and

supply lock circuit operably coupled to enable the supply lock signal when the supply substantially reaches a steady-state condition.

10. The stand-alone IC of claim **9**, wherein the on-chip power converter further comprises:

switching transistors operably coupled to produce a first supply and a second supply from the external power source and a single inductor, and

regulation module operably coupled to the switching transistors, wherein the regulation module produces control signals that enable and disable transistors of the switching transistors to regulate the first and second supplies.

11. The stand-alone IC of claim **9**, wherein the reset circuit further comprises:

clock generator operably coupled to produce a clock signal when the external power source is coupled to the standalone IC, wherein the clock signal is provided to the on-chip power converter such that the on-chip power converter generates the supply;

clock lock module operably coupled to generate a clock lock signal when the clock signal has substantially reached a steady-state condition;

reset module operably coupled to assert a reset signal when the external power source is coupled to the stand-alone IC, wherein the reset module de-asserts the reset signal when the clock lock signal and the supply lock signal are asserted such that functionality of the stand-alone IC is enabled.

12. The stand-alone IC of claim **9**, wherein the on-chip power converter further comprises:

a band-gap reference that produces a reference voltage upon assertion of the power enable signal.

13. A stand-alone IC comprises:

on-chip power converter;

processing module; and

memory operably coupled to the processing module, wherein the memory includes operational instructions that cause the processing module to:

establish an idle state that holds at least a portion of the stand-alone IC in a reset condition when a power source is operably coupled to the stand-alone IC;

receive a power enable signal;

enable, in response to the power enable signal, the on-chip power converter of the stand-alone IC to generate at least one supply from the power source; and

when the at least one supply has substantially reached a steady-state condition, enable functionality of the stand-alone IC.

14. The stand-alone IC of claim **13**, wherein the memory further comprises operational instructions that cause the processing module to enable the on-chip converter further comprises:

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generate a first supply from the power source; and

generate a second supply from the power source, wherein the first and second supplies are produced by regulating energy transfer from a single inductor.

15. The stand-alone IC of claim **13**, wherein the memory further comprises operational instructions that cause the processing module to establish the idle state by enabling a reset signal for the at least a portion of the stand-alone IC.

16. The stand-alone IC of claim **15**, wherein the memory further comprises operational instructions that cause the processing module to enable the functionality of the stand-alone IC by providing the clock signal to components of the stand-alone IC and de-asserting the reset signal.

17. The stand-alone IC of claim **13**, wherein the memory further comprises operational instructions that cause the processing module to enable the on-chip power converter by:

generating a clock signal; and

generating power converter regulation signals based on the clock signal.

18. The stand-alone IC of claim **17**, wherein the memory further comprises operational instructions that cause the processing module to enable the on-chip power converter by enabling a band-gap reference that is used in generating the power converter regulation signals.

19. The stand-alone IC of claim **17**, wherein the memory further comprises operational instructions that cause the processing module to generate a clock lock signal when the clock has substantially reached a substantially steady-state.

20. The stand-alone IC of claim **19**, wherein the memory further comprises operational instructions that cause the processing module to enable functionality of the stand-alone IC further comprises:

detect the clock lock signal; and

detect a supply lock signal; and

de-assert a reset signal upon detection of the clock lock signal and the power supply lock signal.

* * * * *

EXHIBIT B

EXHIBIT C

(12) **United States Patent**
May et al.

(10) **Patent No.: US 6,366,522 B1**
(45) **Date of Patent: Apr. 2, 2002**

(54) **METHOD AND APPARATUS FOR CONTROLLING POWER CONSUMPTION OF AN INTEGRATED CIRCUIT**

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(73) Assignee: **Sigmatel, Inc**, Austin, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/716,616**

(22) Filed. **Nov. 20, 2000**

(51) **Int. Cl.**[7] **G06F 1/26**
(52) **U.S. Cl.** **365/227**; 713/320; 713/322
(58) **Field of Search** 365/226, 227, 365/228, 229; 713/320, 322

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* cited by examiner

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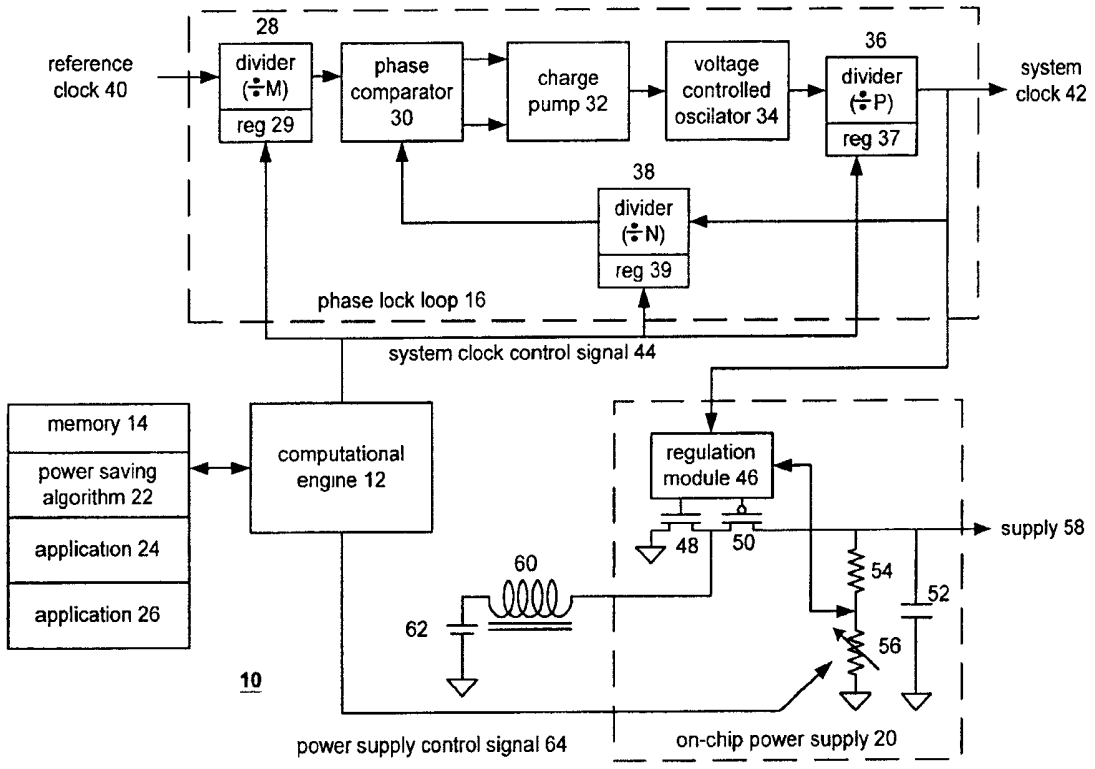
(57) **ABSTRACT**

A method and apparatus for controlling power consumption of an integrated circuit include processing that begins by producing a system clock from a reference clock based on a system clock control signal. The reference clock may be generated from an external crystal oscillator circuit operable to produce a reference clock at a desired frequency. The processing continues by regulating at least one supply from a power source and an inductor based on a power supply control signal. The processing continues by producing the system clock control signal and the power supply control signal based on a processing transfer characteristic of a computational engine and processing requirements associated with processing at least a portion of an application by the computational engine.

22 Claims, 5 Drawing Sheets



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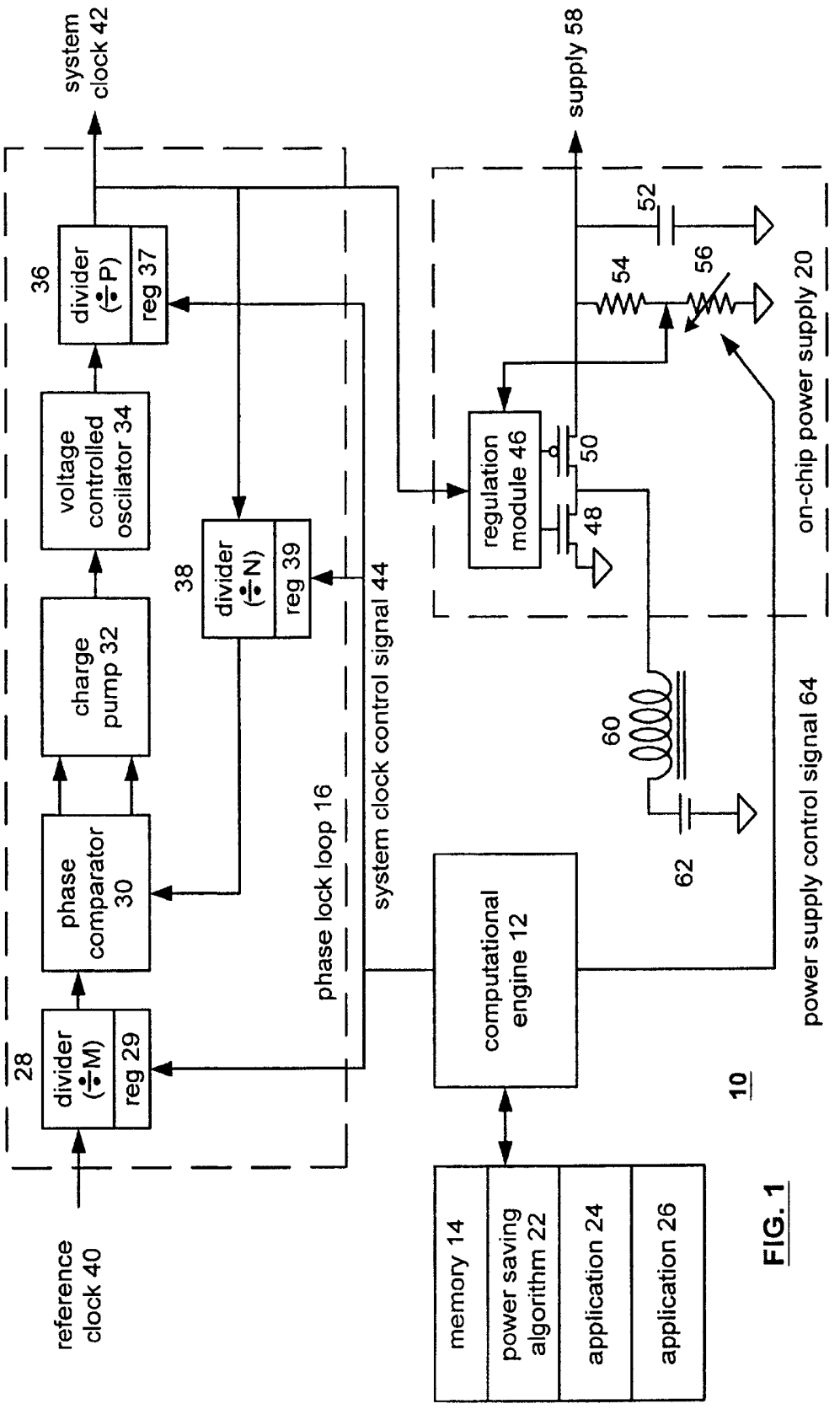

FIG. 1

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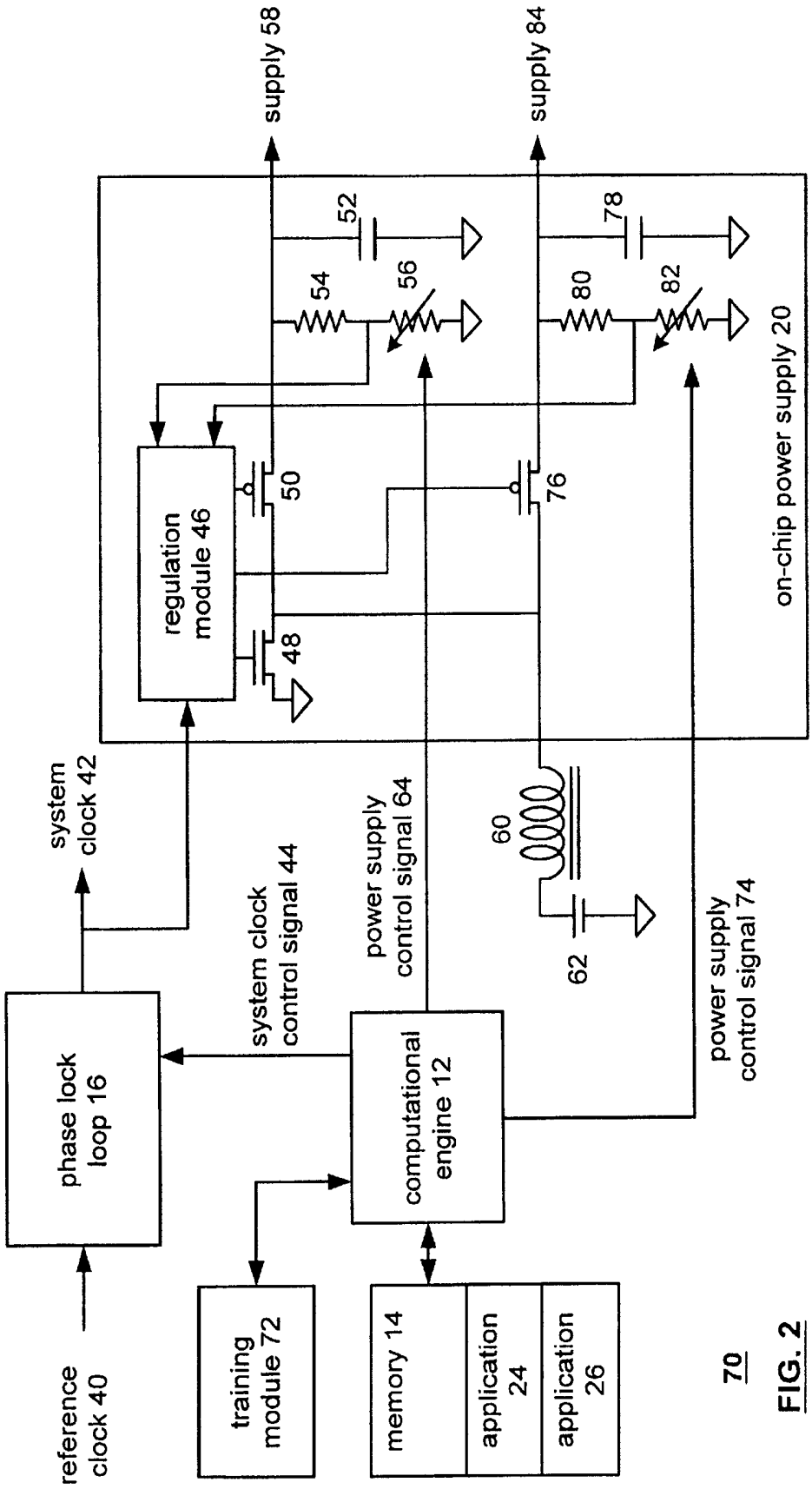

FIG. 2

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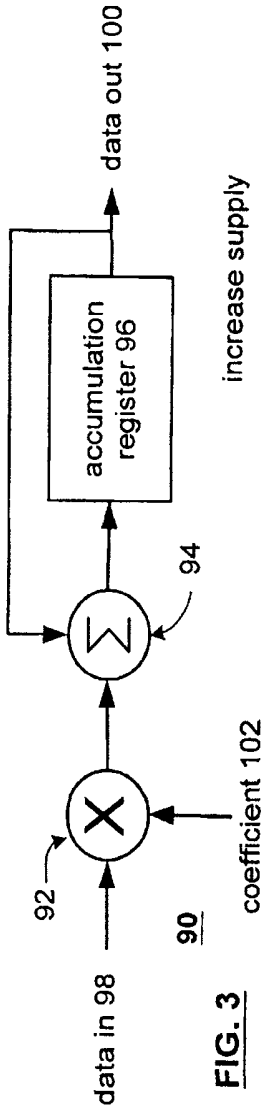

FIG. 3

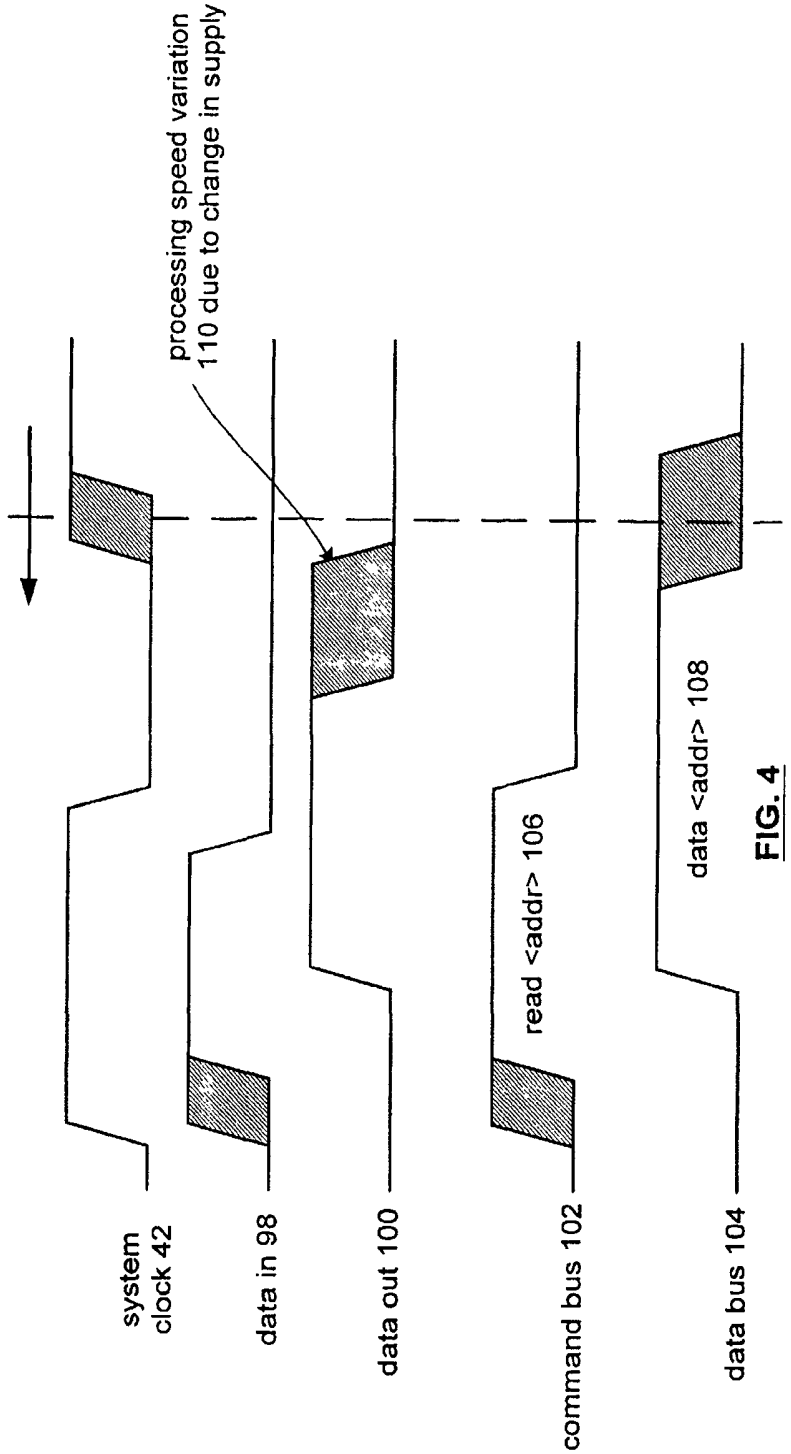

FIG. 4

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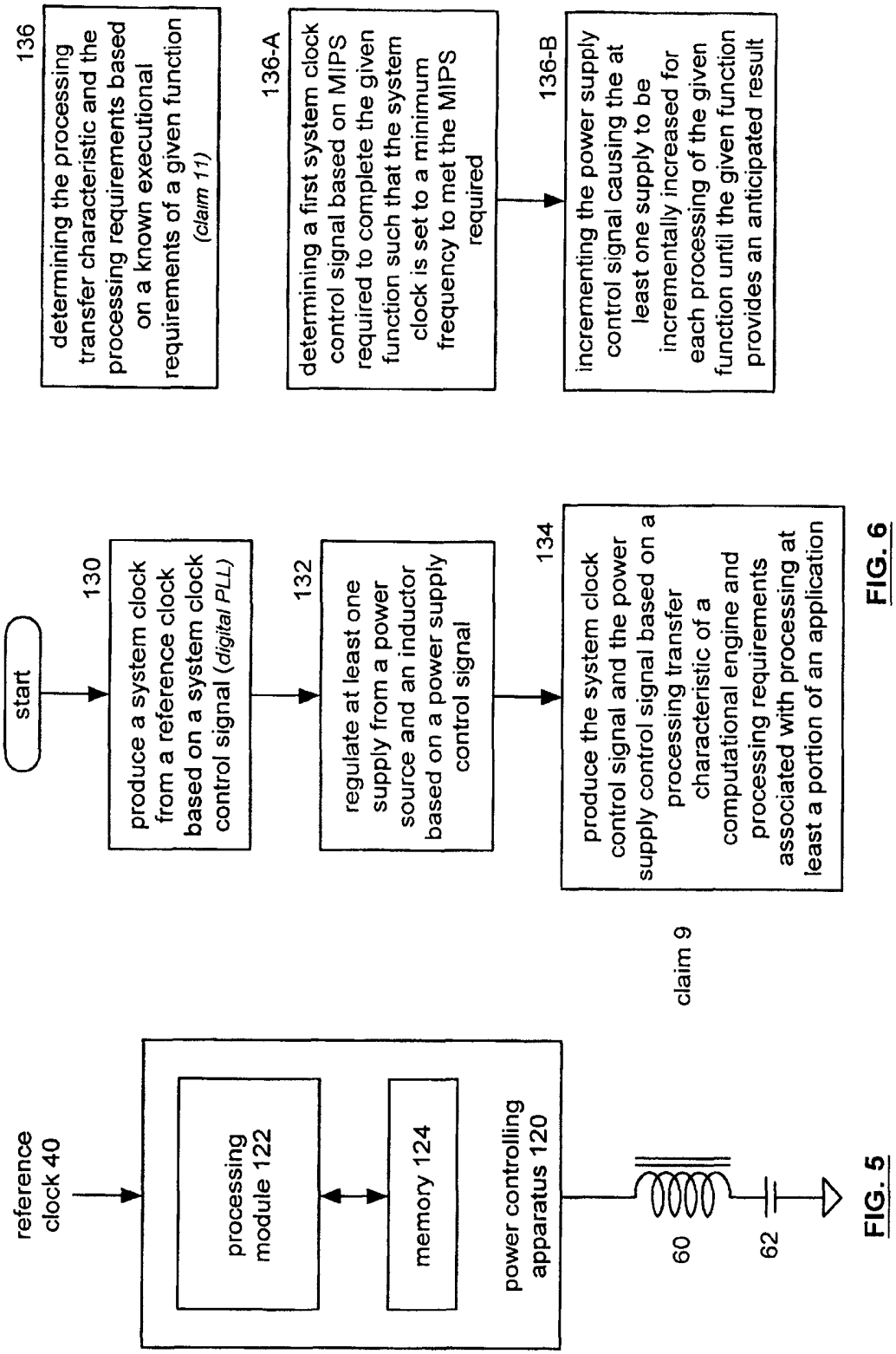

FIG. 5

FIG. 6

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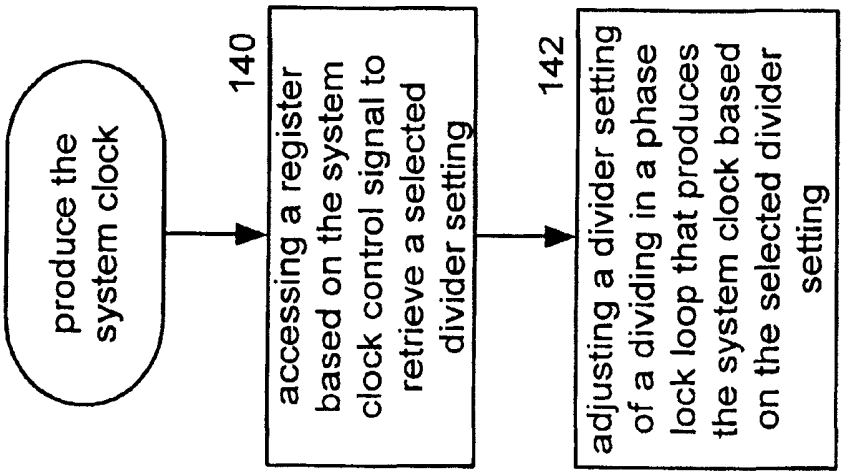

FIG. 7

132-A
regulating at least one supply further comprises adjusting a programmable divider circuit of an on-chip power converter based on the power supply control signal

132-B
regulating the at least one supply further comprises regulating multiple supplies from the system clock and multiple power supply control signals, wherein each of the multiple power supply control signals corresponds to a unique one of the multiple supplies

EXHIBIT C

METHOD AND APPARATUS FOR CONTROLLING POWER CONSUMPTION OF AN INTEGRATED CIRCUIT

TECHNICAL FIELD OF THE INVENTION

This invention relates generally to integrated circuits and more particularly to controlling power consumption by an integrated circuit.

BACKGROUND OF THE INVENTION

Integrated circuits (IC's) are known to be used in a wide variety of electronic devices. For example, personal computers, cellular telephones, compact disk players, MP3 players, et cetera all include integrated circuits. Such integerated circuits are comprised of a plurality of functional circuit blocks that perform desired functions. Transistors, resistors and capacitors generally comprise the circuitry found in each circuit block

As is known, transistor performance (e.g. transfer characteristics, on resistance, slew rate, et cetera) varies depending on the supply voltage. The lower the supply voltage, the lower the transistor performance and slew rate, but the less power it consumes. Conversely, the higher the supply voltage, the higher the performance and slew rate, but more power is consumed as such, the power consumption by an integrated circuit is very much dependent on the supply voltage and transistors that comprise the circuit blocks.

As processing speeds of microprocessors, digital signal processors, et cetera increase, such devices are capable of processing larger software applications in less time. While some applications push the processing engine to its processing speed limits, most applications do not. However, the processing engine must be designed to support the highest processing requirements. Thus, the processing engine needs to have a supply voltage and system clock to handle the most taxing applications. When the processing engine is executing less taxing applications, the voltage and system clock remain the same, thus power consumption of the integrated circuit remains the same even though the application could accurately be performed with a lower supply voltage and/or a lower system clock.

Therefore, a need exists for a method and apparatus that adjust the system clock and/or the supply voltage based on the processing capabilities of an integrated circuit and the application being performed to conserve power.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates a schematic block diagram of an integrated circuit in accordance with the present invention;

FIG. **2** illustrates a schematic block diagram of an alternate integrated circuit in accordance with the present invention;

FIG. **3** illustrates a schematic block diagram of a multiply accumulator in accordance with the present invention;

FIG. **4** illustrates a graphical representation of adjusting the supply clock and/or the supply in accordance with the present invention;

FIG. **5** illustrates a schematic block diagram of a power controlling apparatus in accordance with the present invention:

FIG. **6** illustrates a logic diagram of a method for controlling power consumption of an integrated circuit in accordance with the present invention; and

FIG. **7** illustrates a logic diagram of further processing of steps in FIG. **6**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Generally, the present invention provides a method and apparatus for controlling power consumption of an integrated circuit. Such a method and apparatus include processing that begins by producing a system clock from a reference clock based on a system clock control signal. The reference clock may be generated from an external crystal oscillator circuit operable to produce a reference clock at a desired frequency. The processing continues by regulating at least one supply from a power source and an inductor based on a power supply control signal, or a linear regulator. The processing continues by producing the system clock control signal and the power supply control signal based on a processing transfer characteristic of a computational engine and processing requirements associated with processing at least a portion of an application by the computational engine. With such a method and apparatus, power consumption of an integrated circuit can be controlled, and thereby reduced, based on the application being performed by the computational engine and the capabilities of the computational engine within the integrated circuit thereby reducing power consumption.

The present invention can be more fully described with reference to FIGS. **1** through **7**. FIG. **1** illustrates an integrated circuit **10** that includes a phase lock loop **16**, a computational engine **12**, memory **14** and an on-chip power supply **20**. The integrated circuit **10** is operably coupled to an external inductor **60** and an external power source **62** (e.g. a battery). The computational engine **112** may be a microprocessor, compressor, digital signal processor, logic circuit, state machine, analog circuit, and/or any circuitry that manipulates signals (analog or digital) based on operational instructions. The memory **14** may be on-chip or off-chip and stores a power savings algorithm **22**, and at least one application. In this illustration the memory is storing two applications **24** and **26**. As one of average skill in the art will appreciate, many more applications may be stored in memory **14** than the two illustrated.

The phase lock loop **16** is shown to include a 1^{st} divider **28**, a 1^{st} register **29**, a phase comparator **30**, a charge pump **32**, a voltage controlled oscillator **34**, a 2^{nd} divider **36**, a 2^{nd} register **37**, a 3^{rd} divider **38**, and a 3^{nd} register **39**. In practice, the phase lock loop **16** may include one, two, or three of the dividers **28**, **36** and **38** to produce the system clock **42** from the reference clock **40**. The registers **29**, **37** and **39** each store values to represent the corresponding divider value. For example, divider **28** utilizes one of the values in register **29** to produce a (÷M) function. Similarly, divider **36** utilizes values in register **37** to produce a (÷P) value and divider **38** utilizes values in register **39** to produce a (÷N) value.

In operation, the computational engine **12**, based on the execution of the power saving algorithm **22**, produces a system clock control signal **44**. The system clock control signal **44** is determined based on the particular application or applications being performed by the computational engine **12** and the processing requirements associated therewith. For example, if the computational engine is performing application **24**, and application **24** has a processing requirement of five MIPS (millions of instructions per second), the power savings algorithm **22** would cause the computational engine **12** to set the system clock control signal **44** such that the system clock **42** produces at least a 5 Mhz clock. The

phase lock loop **16** receives the system clock control signal **44**, which is used to address at least one of registers **29**, **37** or **39**. Based on the addressed value in the corresponding register, the divider **28**, **36** or **38** is set to the corresponding value. Once this is done, the phase lock loop **16** performs in a conventional manner.

In addition to generating the system clock control signal **44**, the computational engine **12** also produces a power supply control signal **64**. The computational engine **12** provides the power supply control signal **64** to the on-chip power supply **20**. The on-chip power supply **20** includes a regulation module **46**, an N-channel transistor **48**, a P-channel transistor **50**, a programmable divider network **54** and **56** and a capacitor **52**.

Based on the power supply control signal **64**, the on-chip power supply **20** sets the programmable divider such that the regulation module produces supply **58** at a desired value. For example, once the system clock **42** has been set, the supply **58** may be varied such that the processing of the application **24** with the computational engine **12** is optimized. This concept will be discussed in treater detail with reference to FIGS. **3**, **4**, **6** and **7**. For a more detailed discussion on the on-chip power supply **20**, refer to co-pending Patent Application, entitled METHOD AND APPARATUS FOR REGULATING A DC OUTLET VOLTAGE, having a Ser. No. of 09/551,123, and a filing date of Apr. 18, 2000.

FIG. **2** illustrates a schematic block diagram of an alternate integrated circuit in accordance with the present invention. The integrated circuit **70** includes the memory **14**, the computational engine **12**, the phase lock loop **16**, the on-chip power supply **20** and a training module **72**. The integrated circuit **70** is coupled to an external inductor **60** and an external power source **62**. As with the integrated circuit **10** of FIG. **1**, the memory **14** may also include an off-chip portion for storing multiple applications. In this configuration, the training module **72** establishes the rate at which the system clock **42** will be generated and the values of supply **58** and supply **84**.

In this embodiment, the on-chip power supply **20** produces two supplies **58** and **84**. The regulation module **46** regulates the supplies **58** and **84** by controlling switching of transistors **48**, **50** and **76**. A 2^{nd} feedback divider **80** and **82** is provided to sample the supply **84**, which is produced across capacitor **78**.

The training module **72**, based on the application to be executed by the computational engine **12** establishes the rate of the system clock **42** and the values of supplies **58** and **84**. To do this, the training module **72** determines the processing transfer characteristics of the computational engine. The processing transfer characteristics of the computational engine include propagation delays through logic circuits, slew rates of transistors within memory, logic circuits, read/write processing speed, et cetera, and any other characteristic of a logic circuit, digital signal processor, microprocessor, et cetera that corresponds to the speed at which digital information may be processed. FIGS. **3** and **4** illustrate embodiments performed by the training **2** module **72**.

FIG. **3** illustrates a schematic block diagram of a multiply accumulator **90** that may be contained within computational engine **12** or within the training module **72**, which may be used in a particular application. The multiply accumulator **90** includes a multiplier **92**, an adder **94**, and an accumulation register **96**. In operation, a data input **98** is multiplied with a coefficient **102** to produce a resultant. The resultant is summed via adder **94** with previous summed data **100** to produce a new accumulated value that is stored in accumulation register **96**. The processing transfer characteristics of the computational engine will map the processing characteristics of the multiply accumulator **90** and will vary depending on the voltage set for the supply. What voltage to set for the supply is determined by experimentation once the processing requirements of an application are determined (i e. the MIPS required). For example, if the MIPS required is one, then the clock rate is set to 1 MHz, thus yielding a period of 1 microsecond. The supply voltage is set for a predetermined low value, then a multiply accumulate function is processed in a known number of clock cycles. If the accumulated value is as expected, the supply voltage is set to this predetermined low level. If, on the other hand, the accumulated value is not as expected, the supply voltage is increased at an incremental rate of 10 mVolts to 500 mVolts, and the accumulation process is repeated. Once the accumulated value is as expected, i.e., the correct value has been accumulated, the supply is set to this value.

FIG. **4** illustrates a graphical representation of determining the processing transfer characteristics and processing requirements associated with processing at least a portion of an application. The application may include the MIPS required for processing the entire application or it may include separate indications for each sub routine contained therein. Alternatively, a default processing requirement may be selected for certain applications or all applications. As one of average skill in the art will appreciate, there is a multitude of ways in which the processing requirements associated with an application may be derived.

Based on the most difficult processing requirements of an application, the system clock **42** is set to provide a clock that at least meets the processing requirements. For example, if the processing requirement is 6 MIPS, the system clock will be set at a rate of at least 6 Mhz. Having done this, the supply **58** or **84**, which may be a regulated voltage supply or a regulated current output, is varied to change the processing speed of the circuitry within the computational engine. As shown in FIG. **4**, the processing speed of data input **98** may vary **110** due to changes in the supply. As is known, the lower the supply, the longer it takes digital circuitry to reach a final logic 0 or logic 1 state. As such, as the supply is increased, the processing speed of inputting data and outputting data **100** is increased. The cross hatched areas of data in **98** and data out **100** correspond to the variations in processing speeds of inputting, data and outputting data of the multiply accumulator **90** of FIG. **3** as the supply voltage is varied. The lower the supply voltage is, the longer it takes to input data and output data. If the supply is too low, the data output **100** will not occur before the next given number of cycles of the system clock **42**, i.e., operational period of the system. When this occurs, the supply is set too low. Accordingly, the supply is increased, as shown by the arrow associated with the vertical dash line until the processing speed of the multiply accumulator **90** produces a digital output **100** that occurs just within the period of the system clock **42**. A further increase in supply provides no added processing benefit; it only increases the power consumption.

Thus, the supply is set so that the data output **100** just completes prior to the beginning of the next clock cycle of system clock **42**.

As an alternate processing of the training module **72**, a read function may be processed by the computational engine in conjunction with the transfer module. On the command bus **102**, a read instruction **106** is placed. Again, based on the supply voltage, the speed of placing of an instruction on the command bus varies. The higher the voltage, the more

quickly the command is placed on the bus. Once the read instruction **106** has been interpreted by memory, a data word **108** is placed on a data bus **104**. Similarly, the speed at which data may be placed on the data bus **104** is dependent on the supply voltage. The lower the supply voltage, the longer it takes. Thus, to optimize power consumption, the supply voltage is increased until the point where the data word **108** is placed on the data bus **104** is just within the end of the current clock cycle **42** or the clock cycle when the data is expected. By controlling the system clock and supply voltage in this manner, power consumption of an integrated circuit may be optimized based on the corresponding application being performed and the processing characteristics of the computational engine. As one of average skill in the art will appreciate, the computational engine may process multiple applications at a given time. Accordingly, the clock rate would be set such that the speed needed for processing multiple applications is met

FIG. **5** illustrates a schematic block diagram of a power efficient integrated circuit that includes a power controlling apparatus **120** operably coupled to an external inductor **60** and an external power source **62**. The power controlling apparatus **120** includes a processing module **122** and a memory **124**. The power controlling apparatus **120** is also operably coupled to receive a reference clock **40**.

The processing module **122** may be a single processing device or a plurality of processing devices. The processing device may be a microprocessor, microcontroller, microcomputer, digital signal processor, logic circuit, state machines, and/or any device that manipulates signals (analog or digital) based on operational instructions. The memory **124** may be a single memory device or a plurality of memory devices. Such a memory device may be a read only memory, floppy disk memory, random access memory, external memory, and/or any device that stores digital information. Note that when the processing module **122** implements one or more of its functions via a state machine or logic circuit, the memory storing the corresponding operational instructions is embedded within the circuitry comprised in the state machine or logic circuit. The operational instructions stored in memory **124** and executed by processing module **122** are further illustrated in FIGS. **6** and **7**.

FIG. **6** illustrates a logic diagram of a method for controlling power consumption of an integrated circuit. The process begins at Step **130** where a system clock is produced from a reference clock based on a system clock control signal. As is known, a processing module may include functional components to perform a digital, or analog, phase lock loop that is controlled by the system control clock signal. The process then proceeds to Step **132** where at least one supply is regulated from a power source and an inductor based on a power supply control signal or from a linear regulator.

The process then proceeds to Step **134** where the system clock control signal and the power supply control signal are produced based on a processing transfer characteristic of a computational engine and processing requirements associated with processing at least a portion of an application. Note that the computational engine may be included within the processing module **122** or a separate device that includes logic circuitry a state machine, digital signal processor, digital circuitry, analog circuitry, and/or a combination thereof.

The processing transfer characteristics of the computational engine may be further determined as described in Step **136**. At Step **136** the processing transfer characteristic and the processing requirements are determined based on a known executional requirements of a given function. The known executional requirement includes at least one of a specification of millions of instructions per second (MIPS) required to process at least a portion of an application, timings requirement between dependent operations (e.g. the timing requirement between inputting a request to RAM and receive data back), and speed of execution (e.g. slew rate of transistors within the circuitry comprising the computational engine).

Steps **136**-A and **136**-B further illustrate the determination of the transfer characteristics and the processing requirements. At Step **136**-*a* a 1st system clock control signal is determined based on the MIPS required to complete the given function such that the system clock is set to a minimum frequency to meet the MIPS required. For example, if the processing requirements of the known function is 6 MIPS, the system clock is set to a value of 6 Mhz or slightly greater than 6 Mhz. At Step **136**-B, the power supply control signal is incremented causing the at least one supply to be incrementally increased for each processing of the given function until the given function provides an anticipated result. This was illustrated and discussed with reference to FIG. **4** when processing the multiplied accumulate function and/or the read function.

FIG. **7** illustrates various processing steps that further describe corresponding steps of FIG. **6**. Step **132**-A further describes the regulation of at least one supply by adjusting a programmable divider circuit of the on-clip power supply based on thecontrol signal. Step **132**-B further includes regulating the at least one supply by regulating multiple supplies from the system clock and multiple power supply control signals, where each of the multiple power supply control signals corresponds to an unique one of the multiple supplies. This was illustrated in FIG. **2** where power supply control signal **64** regulates supply **58** and power supply control signal **74** regulates supply **84**.

The production of the system clock may be further described with reference to Steps **140** and **142**. At Step **140**, a register is accessed based on the system clock control signal to retrieve a selected divider setting. The process then proceeds to Step **142** where a divider setting of a divider in the phase lock loop is adjusted to produce the system clock in accordance with the selected divider setting.

The preceding discussion has presented a method and apparatus for controlling power consumption within an integrated circuit. By adjusting the system clock and/or the supply based on application being executed by the intergated circuit, power consumption may be optimized. As one of average skill in the art will appreciate, other embodiments may be derived from the teachings of the present invention without deviating from the scope of the claims. For example a buck converter may be instead of a boost converter, or a combination of a buck and boost converter may be used.

What is claimed is:

1. A power efficient integrated circuit comprising:

phase lock loop operably coupled to receive a reference clock and to produce therefrom a system clock based on a system clock control signal;

on-chip power supply control module operably coupled to regulate at least one supply from a power source and an inductance based on a power supply control signal;

memory operably coupled to store at least one application; and

computational engine operably coupled to produce the system clock control signal and the power supply

control signal based on a processing transfer characteristic of the computation engine and processing requirements associated with processing at least a portion of the at least one application.

2. The power efficient integrated circuit of claim 1, wherein each of the at least one application comprises the processing requirements for at least one of: each sub-routine contained in the application and the application.

3. The power efficient integrated circuit of claim 1, wherein the computational engine further comprises:

training module operably coupled to determine the processing transfer characteristic and the processing requirements based on a known executional requirements of a given function, wherein the known executional requirements includes at least one of: millions of instructions per second (MIPS), timing requirement between dependent operations, and speed of execution.

4. The power efficient integrated circuit of claim 3, wherein the given function further comprises at least one of: reading from memory, executing a test multiply-accumulate function, and propagating data through combinational logic circuit.

5. The power efficient integrated circuit of claim 4, wherein the training module further comprises:

system clock determining module operably coupled to determine a first system clock control signal based on MIPS required to complete the given function such that the system clock is set to a minimum frequency to met the MIPS required; and

power supply determining module operably coupled to increment the power supply control signal causing the at least one supply to be incrementally increased for each processing of the given function until the given function provides an anticipated result.

6. The power efficient integrated circuit of claim 1, wherein the phase lock loop further comprises:

at least one divider module; and

a register operably coupled to the at least one divider module, wherein the register stores various divider values that are selected based on the system clock control signal.

7. The power efficient integrated circuit of claim 1, wherein the on-chip power supply further comprises a programmable divider circuit that is programmed based on the power supply control signal.

8. The power efficient integrated circuit of claim 1, wherein the at least one supply further comprises multiple supplies that are produced from the system clock and multiple power supply control signals, wherein each of the multiple power supply control signals corresponds to a unique one of the multiple supplies.

9. A method for controlling power consumption of an integrated circuit, the method comprises the steps of:

producing a system clock from a reference clock based on a system clock control signal;

regulating at least one supply from at least one of: a linear regulator and a power source and an inductance based on a power supply control signal; and

producing the system clock control signal and the power supply control signal based on a processing transfer characteristic of a computation engine and processing requirements associated with processing at least a portion of an application by the computation engine.

10. The method of claim 9 further comprises retrieving the processing requirements from the application.

11. The method of claim 9 further comprises:

determining the processing transfer characteristic and the processing requirements based on a known executional requirements of a given function, wherein the known executional requirements includes at least one of: millions of instructions per second (MIPS), timing relationship between dependent operations, and speed of execution.

12. The method of claim 11 further comprises:

determining a first system clock control signal based on MIPS required to complete the given function such that the system clock is set to a minimum frequency to met the MIPS required; and incrementing the power supply control signal causing the at least one supply to be incrementally increased for each processing of the given function until the given function provides an anticipated result.

13. The method of claim 9, wherein the producing the system clock from a reference clock based on a system clock control signal further comprises:

accessing a register based on the system clock control signal to retrieve a selected divider setting; and

adjusting a divider setting of a dividing in a phase lock loop that produces the system clock based on the selected divider setting.

14. The method of claim 9, wherein the regulating at least one supply further comprises adjusting a programmable divider circuit of an on-chip power converter based on the power supply control signal.

15. The method of claim 9, wherein the regulating the at least one supply further comprises regulating multiple supplies from the system clock and multiple power supply control signals, wherein each of the multiple power supply control signals corresponds to a unique one of the multiple supplies.

16. An apparatus for controlling power consumption of an integrated circuit, the apparatus comprises:

a processing module; and

memory operably coupled to the processing module, wherein the memory includes operational instructions that cause the processing module to:

produce a system clock from a reference clock based on a system clock control signal;

regulate at least one supply from at least one of: a linear regulator and a power source and an inductance based on a power supply control signal, and

produce the system clock control signal and the power supply control signal based on a processing transfer characteristic of a computation engine and processing requirements associated with processing at least a portion of an application by the computation engine.

17. The apparatus of claim 16, wherein the memory further comprises operational instructions that cause the processing module to retrieve the processing requirements from the application.

18. The apparatus of claim 16, wherein the memory further comprises operational instructions that cause the processing module to:

determine the processing transfer characteristic and the processing requirements based on a known executional requirements of a given function, wherein the known executional requirements includes at least one of: millions of instructions per second (MIPS), timing relationship between dependent operations, and speed of execution.

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19. The apparatus of claim 18, wherein the memory further comprises operational instructions that cause the processing module to:

determine a first system clock control signal based on MIPS required to complete the given function such that the system clock is set to a minimum frequency to met the MIPS required; and

increment the power supply control signal causing the at least one supply to be incrementally increased for each processing of the given function until the given function provides an anticipated result.

20. The apparatus of claim 16, wherein the memory further comprises operational instructions that cause the processing module to produce the system clock from a reference clock based on a system clock control signal by:

accessing a register based on the system clock control signal to retrieve a selected divider setting; and

adjusting a divider setting of a dividing in a phase lock loop that produces the system clock based on the selected divider setting.

21. The apparatus of claim 16, wherein the memory further comprises operational instructions that cause the processing module to regulate at least one supply by adjusting a programmable divider circuit of an on-chip power converter based on the power supply control signal

22. The apparatus of claim 16, wherein the memory further comprises operational instructions that cause the processing module to regulate the at least one supply by regulating multiple supplies from the system clock and multiple power supply control signals, wherein each of the multiple power supply control signals corresponds to a unique one of the multiple supplies.

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