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UNITED STATES DISTRICT COURT
CENTRAL DISTRICT OF CALIFORNIA
WESTERN DIVISION

MONOLITHIC POWER SYSTEMS, INC.

Plaintiff,

v.

SILERGY CORPORATION and SILERGY TECHNOLOGY

Defendants.

Case No. CV-10-01533 CAS (AGRx)s

SECOND AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Monolithic Power Systems, Inc. ("MPS) hereby pleads the following claim against Defendants Silergy Corporation ("Silergy Corp.") and Silergy Technology ("Silergy Tech") and alleges as follows.

PARTIES

1. Plaintiff MPS is a California corporation having a principal place of business at 6409 Guadalupe Mines Road, San Jose, California 95120.

2. Defendant Silergy Corp. is, upon information and belief, a corporation organized and existing under the laws of the Cayman Islands with a principal place of business at 7F.-1 No. 202, Sec. 3, Beixin Road, Xindian City, Taipei County 231, Taipei, Taiwan. On information and belief, Silergy Corp. also has headquarters at No. 6, 5th Floor, Shun An Street, Xindian City, Taipei County 231, Taipei, Taiwan. On information and belief, Silergy Corp. also has a United States headquarters at 1879 Lundy Avenue, #126, San Jose, California 95131, and was a registered entity with the State of California (Entity No. C3181618) at least as of December 5, 2008. Silergy Corp. has since surrendered its status; however, Silergy Corp. continues to publicly identify its United States headquarters as the same address it previously listed for its agents for service of process. Upon information and belief, Silergy Corp. has operated and continues to operate from its United States headquarters, and is doing business throughout this judicial district and around the world.

3. Defendant Silergy Tech is, upon information and belief, a corporation organized and existing under the laws of the state of California, with a principal place of business at 1309 S. Mary Ave., #215, Sunnyvale, CA, 94087. Silergy Tech has appointed its agent for service as follows: Xin Shao, 2570 N. First Street, #208, San Jose, California 95131. Upon information and belief, Silergy Tech is an affiliated entity to Silergy Corp., including being under at least partially common control with Silergy Corp., and obtaining United States Patents for Silergy Corp.'s benefit.

4. Silergy Corp. and Silergy Tech are hereinafter referred to collectively as "Silergy."

JURISDICTION AND VENUE

5. This court has subject matter jurisdiction over the action at least under 28 U.S.C. §§ 1331 and 1338(a) because the action concerns a federal question arising under the patent laws of the United States, including 35 U.S.C. § 271.

6. Venue is proper in this judicial district under 28 U.S.C. §§ 1391(d) and 1400(b) because, among other reasons and based on information and belief, Silergy is subject to personal jurisdiction in this judicial district, has committed acts of infringement in this judicial district, and because Silergy Corp. is an alien subject to suit in this judicial district.

7. Upon information and belief, Silergy has designed, manufactured, and placed infringing products into the stream of commerce by shipping those products into this judicial district (and other judicial districts) or knowing that such products would be shipped into this judicial district (and other judicial districts) by third parties, including at least placing the infringing Silergy products in Acer® AO533 notebook computers manufactured by third party Acer Inc. for shipping into this judicial district.

CLAIM I: INFRINGEMENT OF U.S. PATENT NO. 6,897,643

8. MPS incorporates by reference the allegations of paragraphs 1-7 above as fully set forth herein.

9. MPS is the owner by assignment of all right, title, and interest in and to United States Patent No. 6,897,643 ("the '643 Patent") entitled "Integrated Circuit Driver Having Stable Bootstrap Power Supply," which was duly and legally issued by the United States Patent and Trademark Office on May 24, 2005. A copy of the '643 Patent is attached hereto as Exhibit A.

10. Silergy has infringed and continues to directly infringe, literally and/or under the doctrine of equivalents, one or more claims of the '643 Patent by making,

using, offering to sell, selling, and/or other acts constituting infringement under 35 U.S.C. § 271 in the United States, including this judicial district, or importing into the United States, step-down DC to DC converters including, but not limited to, the Silergy SY8101, SY8132, and SY8133 product families.

11. Upon information and belief, Silergy's acts of infringement have been with knowledge of the '643 Patent.

12. Upon information and belief, Silergy has been and is currently indirectly infringing, in violation of 35 U.S.C. § 271, the '643 Patent. Upon information and belief, the '643 Patent is directly infringed by, without limitation, manufacturers and others in the distribution channel of notebook computers using, selling, offering for sale and/or importing in the United States Silergy's step-down DC to DC converters employing the methods and apparatuses claimed in the '643 Patent, including but not limited to the Silergy SY8101, SY8132, and SY8133 product families. Upon information and belief, Silergy induces that infringement through its intentional marketing, sale and/or support, including technical support, of such devices in the United States and abroad to induce direct infringement in the United States. Upon information and belief, Silergy's inducement includes, without limitation, active encouragement of the use, sale, offer for sale and/or importation in the United States, of such devices that infringe the '643 Patent, including the use of technical specifications that induce direct infringement. Upon information and belief, Silergy has known or should have known that these actions would cause direct infringement of the '643 Patent and did so with specific intent to encourage direct infringement.

13. Upon information and belief, Silergy has been and is currently indirectly infringing, in violation of 35 U.S.C. § 271, the '643 Patent. Upon information and belief, the '643 Patent is directly infringed by, without limitation, manufacturers and others in the distribution channel of notebook computers using, selling, offering for sale and/or importing in the United States Silergy's step-down DC to DC converters employing the methods and apparatuses claimed in the '643 Patent, including but not

limited to the Silergy SY8101, SY8132, and SY8133 product families. Upon information and belief, Silergy contributes to that infringement through its marketing, sale and/or support, including technical support, of such devices in the United States and abroad. Upon information and belief, such devices are a component of the notebook computers and are a material part of the invention claimed in the '643 Patent. Upon information and belief, Silergy has known or should have known that such devices were made or especially adapted for infringement of the '643 Patent, and that such devices are not a staple article or commodity of commerce suitable for substantial noninfringing use.

14. Upon information and belief, Silergy's infringement of the '643 Patent have been and continue to be willful.

15. Silergy's infringement of the '643 Patent has injured and damaged, and continue to injure and damage, MPS.

16. Silergy's infringement of the '643 Patent has caused and will continue to cause irreparable injury to MPS unless and until enjoined by this Court.

CLAIM II: INFRINGEMENT OF U.S. PATENT NO. 7,714,558

17. MPS incorporates by reference the allegations of paragraphs 1-14 above as fully set forth herein.

18. MPS is the owner by assignment of all right, title, and interest in and to United States Patent No. 7,714,558 ("the '558 Patent") entitled "Short circuit current ratcheting in switch mode DC/DC voltage regulators," which was duly and legally issued by the United States Patent and Trademark Office on May 11, 2010. A copy of the'558 Patent is attached hereto as Exhibit B.

19. Silergy has infringed and continues to directly infringe, literally and/or under the doctrine of equivalents, one or more claims of the '558 Patent by making, using, offering to sell, selling, and/or other acts constituting infringement under 35 U.S.C. § 271 in the United States, including this judicial district, or importing into the

United States, synchronous step-down DC/DC regulators including, but not limited to, the Silergy SY8033 product family.

20. Upon information and belief, Silergy's acts of infringement has been with knowledge of the '558 Patent.

21. Upon information and belief, Silergy has been and is currently indirectly infringing, in violation of 35 U.S.C. § 271, the '558 Patent. Upon information and belief, the '558 Patent is directly infringed by, without limitation, manufacturers and others in the distribution channel of notebook computers using, selling, offering for sale and/or importing in the United States Silergy's step-down DC to DC converters employing the methods and apparatuses claimed in the '558 Patent, including but not limited to the Silergy SY8101, SY8132, and SY8133 product families. Upon information and belief, Silergy induces that infringement through its intentional marketing, sale and/or support, including technical support, of such devices in the United States and abroad to induce direct infringement in the United States. Upon information and belief, Silergy's inducement includes, without limitation, active encouragement of the use, sale, offer for sale and/or importation in the United States, of such devices that infringe the '558 Patent, including the use of technical specifications that induce direct infringement. Upon information and belief, Silergy has known or should have known that these actions would cause direct infringement of the '558 Patent and did so with specific intent to encourage direct infringement.

22. Upon information and belief, Silergy has been and is currently indirectly infringing, in violation of 35 U.S.C. § 271, the '558 Patent. Upon information and belief, the '558 Patent is directly infringed by, without limitation, manufacturers and others in the distribution channel of notebook computers using, selling, offering for sale and/or importing in the United States Silergy's step-down DC to DC converters employing the methods and apparatuses claimed in the '558 Patent, including but not limited to the Silergy SY8101, SY8132, and SY8133 product families. Upon information and belief, Silergy contributes to that infringement through its marketing,

sale and/or support, including technical support, of such devices in the United States and abroad. Upon information and belief, such devices are a component of the notebook computers and are a material part of the invention claimed in the '558 Patent. Upon information and belief, Silergy has known or should have known that such devices were made or especially adapted for infringement of the '558 Patent, and that such devices are not a staple article or commodity of commerce suitable for substantial noninfringing use.

23. Upon information and belief, Silergy's infringement of the '558 Patent has been and continues to be willful.

24. Silergy's infringement of the '558 Patent has injured and damaged, and continues to injure and damage, MPS.

25. Silergy's infringement of the '558 Patent has caused and will continue to cause irreparable injury to MPS unless and until enjoined by this Court.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff MPS prays that this Honorable Court enter judgment as follows:

1. That Silergy has infringed one or more claims of the '643 Patent;

2. That Silergy's infringement of the '643 Patent has been and/or is willful;

3. That Silergy has infringed one or more claims of the '558 Patent;

4. That Silergy's infringement of the '558 Patent has been and/or is willful;

5. That Silergy, and their respective agents, servants, officers, directors, employees, and all persons acting in concert with them directly or indirectly, be enjoined from infringing the '643 Patent and/or '558 Patent;

6. That Silergy be ordered to account for and pay to MPS damages arising out of Silergy's infringing activities, together with interest and costs, and all other damages permitted by 35 U.S.C. § 284, including enhanced damages up to three times the amount of damages found or measured;

7. That this action be adjudged an exceptional case and that MPS be awarded its attorneys' fees and costs in this action pursuant to 35 U.S.C. § 285; and

8. That MPS be awarded such other equitable or legal relief as this Court deems just and proper under the circumstances.

DEMAND FOR JURY TRIAL

Plaintiff Monolithic Power Systems, Inc. demands a jury trial on all claims and issues so triable.

Dated: June 30, 2011

Respectfully submitted,
FISH & RICHARDSON P.C.

By: _____

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EXHIBIT A

(12) **United States Patent**
Stone

(10) **Patent No.: US 6,897,643 B2**
(45) **Date of Patent: May 24, 2005**

(54) **INTEGRATED CIRCUIT DRIVER HAVING STABLE BOOTSTRAP POWER SUPPLY**

(75) Inventor: **Marshall David Stone**, Fremont, CA (US)

(73) Assignee: **Monolithic Power Systems, Inc.**, Los Gatos, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 91 days.

(21) Appl. No.: **10/269,617**

(22) Filed: **Oct. 11, 2002**

(65) **Prior Publication Data**

US 2004/0070383 A1 Apr. 15, 2004

(51) **Int. Cl.**[7] **G05F 1/40; H03K 17/60**

(52) **U.S. Cl.** **323/288**; 323/224; 327/390; 327/589

(58) **Field of Search** 323/288, 224, 323/286, 282, 289, 225, 284, 285, 287; 363/60, 98, 17, 56, 132; 327/387, 390, 374–377, 434, 589, 537, 538, 536; 307/910, 475, 482, 578

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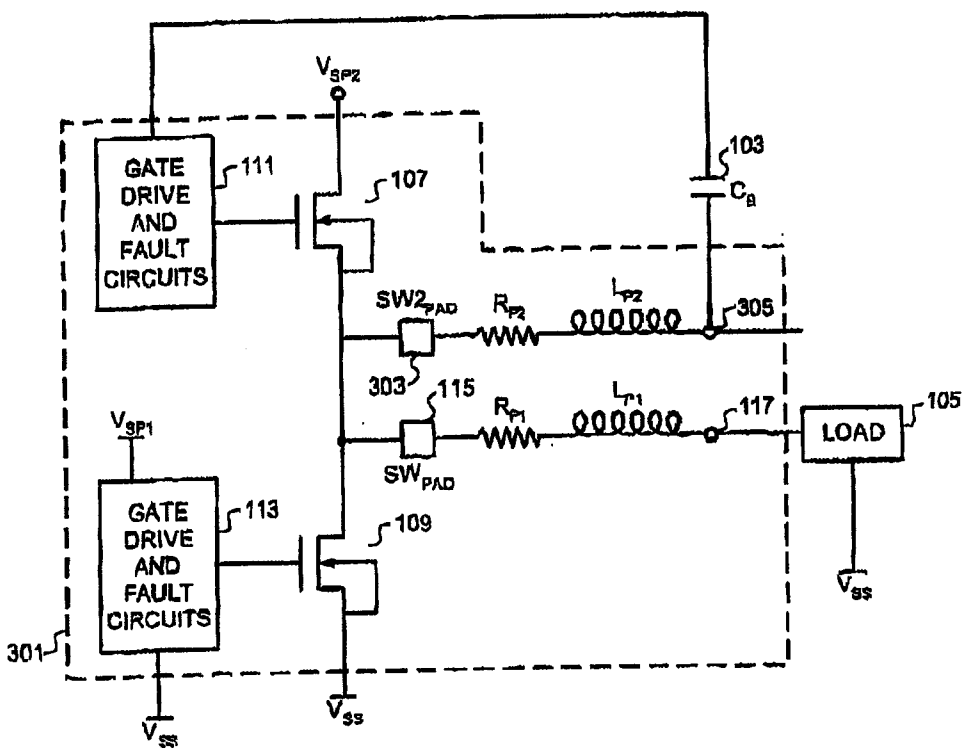
Primary Examiner—Rajnikant B. Patel
(74) *Attorney, Agent, or Firm*—Perkins Coie LLP

(57) **ABSTRACT**

An integrated circuit driver is disclosed. The driver comprises a high side transistor and a low side transistor connected in series. The output of the driver is taken from the source of the high side transistor and the drain of the low side transistor. A bootstrap contact pad is connected to the output node. Connected to the bootstrap contact pad is a bootstrap capacitor that is also connected to a high side gate drive that selectively controls the high side transistor.

14 Claims, 4 Drawing Sheets



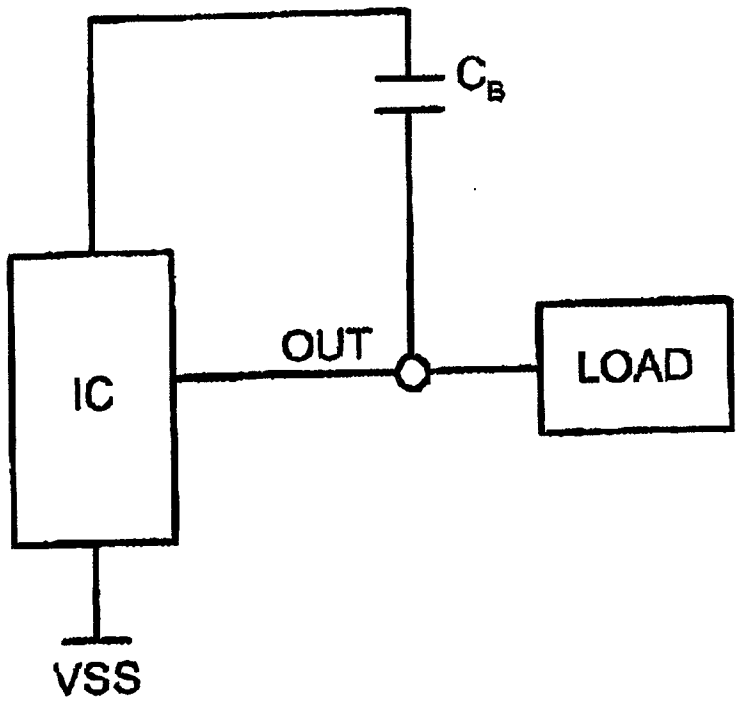


FIGURE 1
(PRIOR ART)

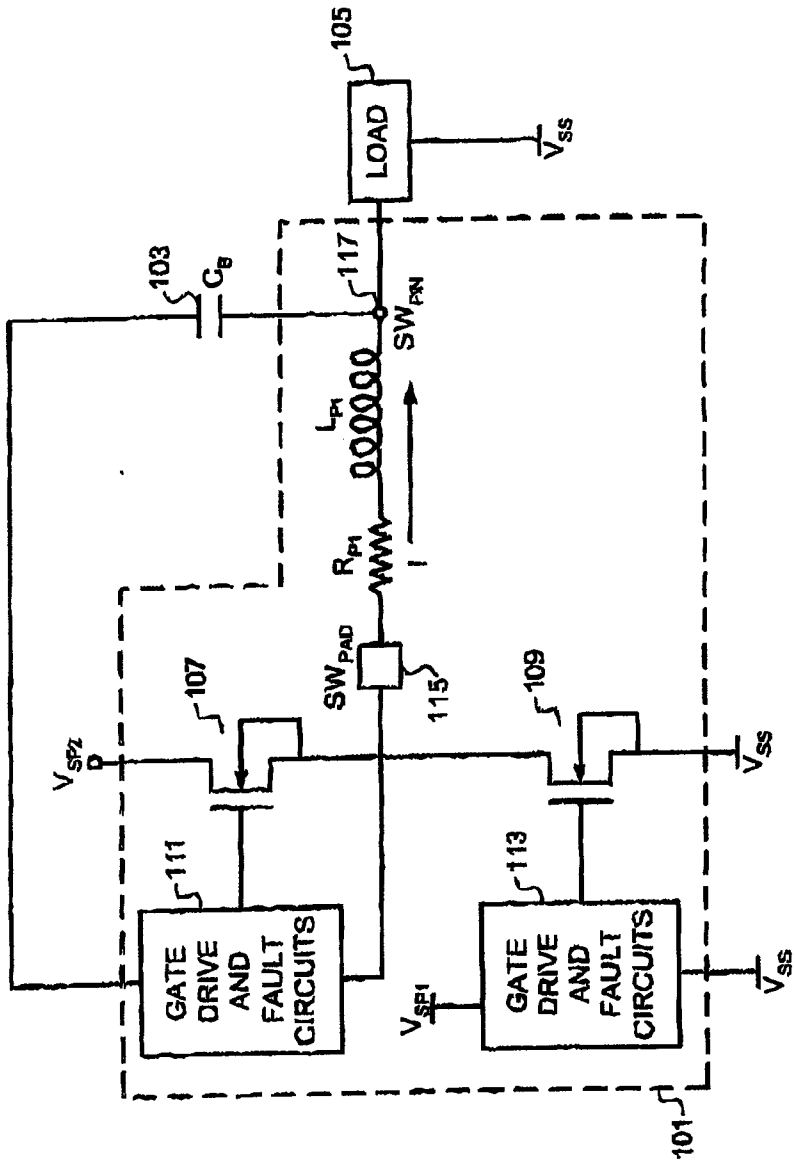


FIGURE 2
(PRIOR ART)

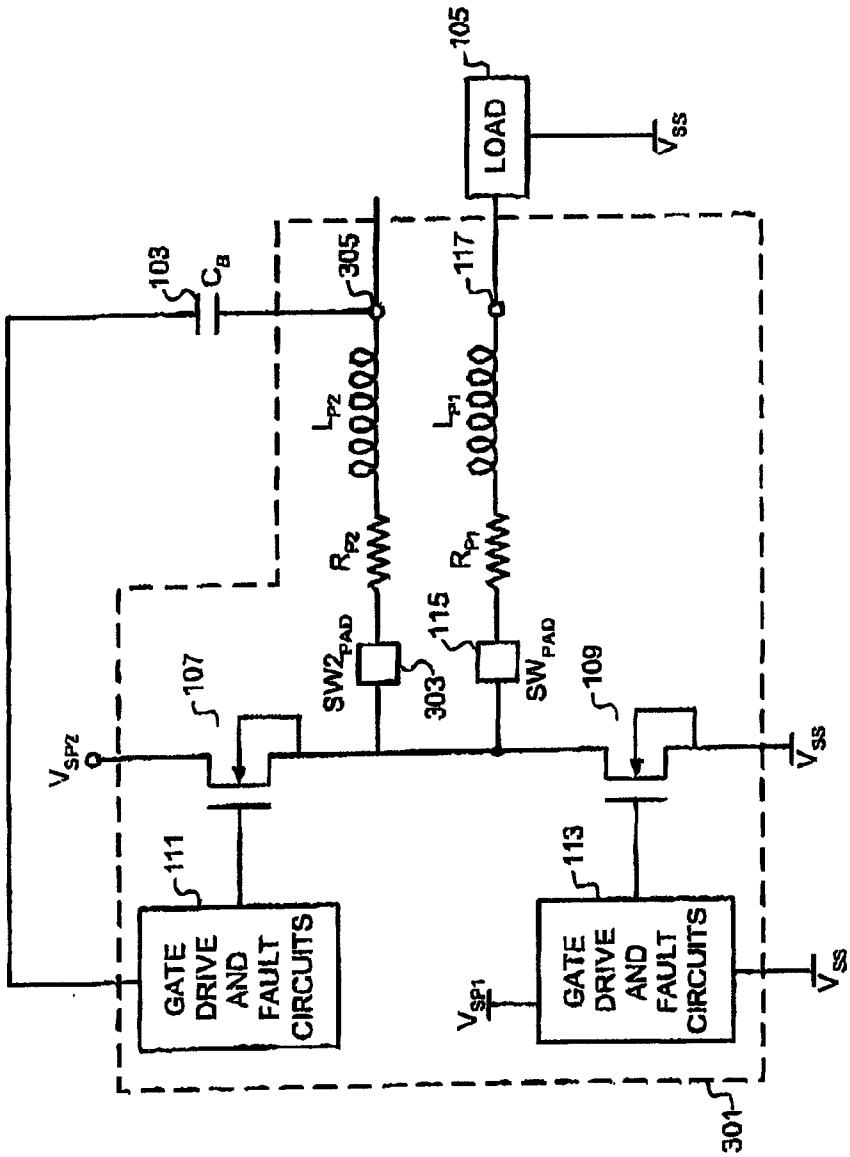

105
LOAD
V_{SS}
103
C_B
305
117
L_{P2}
L_{P1}
R_{P2}
R_{P1}
$SW2_{PAD}$
115
303
SW_{PAD}
107
109
V_{SP2}
V_{SS}
111
113
GATE DRIVE AND FAULT CIRCUITS
GATE DRIVE AND FAULT CIRCUITS
V_{SP1}
V_{SS}
301

FIGURE 3

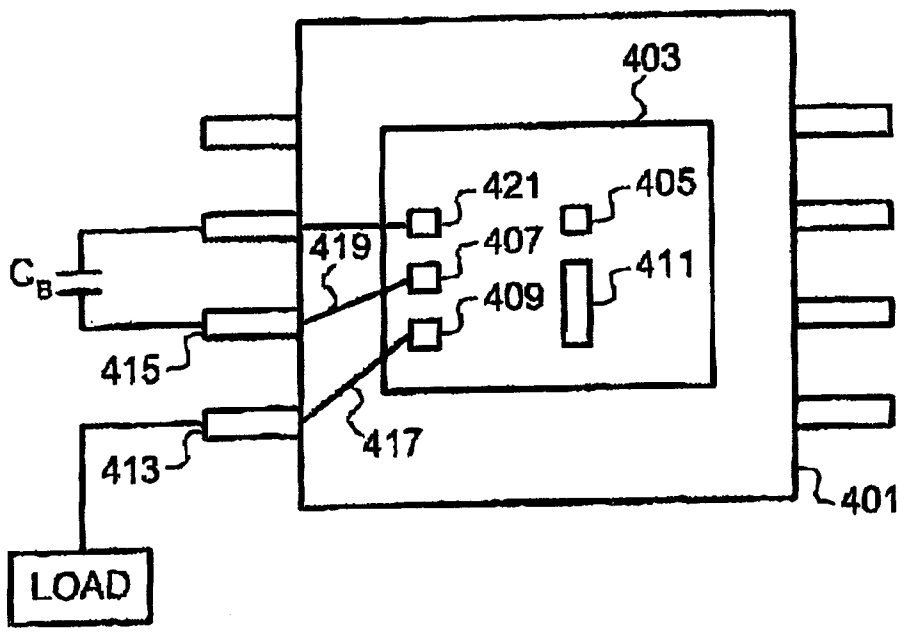


FIGURE 4

INTEGRATED CIRCUIT DRIVER HAVING STABLE BOOTSTRAP POWER SUPPLY

TECHNICAL FIELD

The present invention relates to integrated circuit drivers that use a bootstrap supply to drive the gate of the high side switch, and more particularly, to a method and apparatus for providing a stable bootstrap voltage to the gate of the high side switch.

BACKGROUND

One common type of integrated circuit driver utilizes two power MOSFET switches in a totem pole (half-bridge) topology. The MOSFET switches are typically NMOS switches that are connected in series. The power MOSFET switches are driven to conduct alternately. One of the MOSFET switches is designated as a high side switch, and the other MOSFET switch is designated as the low side switch. In one application, by selectively switching the power MOSFET switches in an alternating fashion, a load can be driven with an alternating current. In such a manner, a DC to AC inverter is formed. Likewise by controlling the switches according to an input signal (such as an acoustic signal), a class D audio amplifier is formed. Further, the same half bridge topology using a stable DC reference as the input can be used to create a DC power supply.

The gate of the high side switch is typically driven by a bootstrapped power supply. This is done to allow use of an NMOS switch, which has roughly half the on resistance of a PMOS switch of the same area. A bootstrap capacitor is used to increase the voltage available to the gate of the high side switch. FIG. 1 shows a prior art simplified schematic of an integrated circuit driver (IC) used in conjunction with a bootstrap capacitor to drive a load. The IC driver provides current to drive a load. A bootstrap capacitor C_b has one terminal connected to the output of the IC driver. The other terminal of the bootstrap capacitor C_b is provided back to the IC driver to drive the gate of the high side switch.

A more detailed schematic of the IC driver of FIG. 1 is shown in FIG. 2. As seen in FIG. 2, the IC driver **101** includes the high side switch **107** and the low side switch **109**. The high side switch **107** is driven by gate drive and fault circuit **111**. Similarly, the low side switch **109** is driven by gate drive and fault circuit **113**. The gate drive and fault circuits **111** and **113** are operative to control the switching of the high side and low side switches **107** and **109**. In addition, the gate drive and fault circuits **111** and **113** typically include fault detection circuitry and a bootstrap supply monitor. These additional functions are generally needed to measure whether there is a fault condition on the switch or whether the bootstrap supply is sufficient for the IC to operate properly.

The precise configuration of the gate drive and fault circuits **111** and **113** may be varied, but generally the configuration and operation is well known in the prior art. Note that the gate drive and fault circuit **113** used to control the low side switch **109** operates using a first supply voltage V_{p1}. The low side switch **109** does not require a bootstrapped power supply. In contrast, the gate drive and fault circuit **111** that controls the high side switch **107** is connected to the bootstrap capacitor **103**.

The output of the IC driver **101** is taken from the node connecting the high side switch and the low side switch. In physical terms, the output node is a conductive pad on the integrated circuit, designated in FIG. 2 as SW_{pad} **115**. The

integrated circuit die is then set into a package wherein the pad SW_{pad} **115** is connected to a package pin SW_{pin} **117**. The connection between the pad **115** and the package pin **117** is typically made through a bond wire formed of gold, copper, or other highly conductive material.

Nevertheless, the bond wire between the pad **115** and the package pin **117** includes some finite amount of parasitic inductance L_{p1} and parasitic resistance R_{p1}. When current is supplied through the pin **117** to the load **105**, invariably there will be a loss of voltage across the parasitic inductance L_{p1} and parasitic resistance R_{p1}.

The amount of the voltage drop is important because any voltage that develops across the bond wire between SW pad and SW pin, subtracts directly and instantaneously from the bootstrap supply. Because of the large value of current and high rate of change of that current in the bondwire, the voltage drop can be significant, on the order of two or more volts. This sudden drop in the internal bootstrap supply voltage will adversely affect any signal processing operating under the internal bootstrap supply, such as the bootstrap supply monitor and fault check circuits.

Therefore, the arrangement shown in FIG. 2 having an imprecise and noisy bootstrap supply is undesirable.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram showing a bootstrap capacitor and an integrated circuit driver for driving a load.

FIG. 2 is a detailed schematic of the integrated circuit driver of FIG. 1.

FIG. 3 is a schematic circuit diagram illustrating one embodiment of the present invention.

FIG. 4 is an illustration of an integrated circuit die mounted on an integrated circuit package.

DETAILED DESCRIPTION

The present invention is an integrated circuit driver having a "quieter" bootstrap power supply. The integrated circuit driver has an output pin and output pad that is dedicated to the bootstrap capacitor thereby maintaining a stable bootstrap supply voltage. In the following description, some specific details, such as example values for the circuit components, are provided to provide a thorough understanding of embodiments of the invention. One skilled in the relevant art will recognize, however, that the invention can be practiced without one or more of the specific details, or with other methods, components, materials, etc. In other instances, well-known structures, materials, or operations are not shown or described in detail to avoid obscuring aspects of the invention.

Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, the appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments. One skilled in the relevant art will recognize, however, that the invention can be practiced without one or more of the specific details, or with other methods, components, materials, etc. In other instances, well-known structures, materials, or operations are not shown or described in detail to avoid obscuring aspects of the invention.

FIG. 3 shows one embodiment of the present invention. As seen, FIG. 3 is substantially similar to the prior art IC driver **101**, except that an additional pad $SW2_{pad}$ **303** is also attached to the output node between the high side switch **107** and the low side switch **109**. Additionally, a second output pin **305** is provided from the IC driver **301**. Having the second pad **303** and the second package pin **305** connected to the bootstrap capacitor **103**, the bootstrap capacitor **103** is not affected by any voltage drop caused by current flowing to the load **105** through a first package pin **117**.

Note that substantially all the current provided by the high side switch **107** and the low side switch **109** flows to the load **105** through the package pin **117**. Little if any current flows through the second package pin **305**, thereby eliminating any voltage drop through the parasitic resistance and inductance of the bond wire connecting the second package pin **305** to the second pad **303**. Thus, the bootstrap supply voltage provided by the bootstrap capacitor **103** maintains its value and is less noisy.

As seen, the IC driver **301** of the present invention includes an additional package pin **305** that is connected directly to the bootstrap capacitor **103**. In an alternative embodiment, the second package pin **305** has a bond wire directly attached to the same pad **115** as the first package pin **117**. This saves the requirement for forming the second pad **303**. In one embodiment, the IC driver **301** may be used to drive, for example, a cold-cathode fluorescent lamp. However, typically, the lamp is connected through a secondary winding of a transformer whose primary winding is connected to the output of the IC driver **301**.

FIG. 4 further illustrates the arrangement of the present invention. In FIG. 4, an integrated circuit package **401** is adapted to mount an integrated circuit die **403**. The integrated circuit die **403** includes various circuitry, such as the low side switch, the high side switch, and the gate drive and fault circuitry. In addition, the integrated circuit die **403** includes an output contact pad **409**, a bootstrap contact pad **407** (referred to as a second pad $SW2_{pad}$ **303** in FIG. 3), a high side gate drive input pad **421**, and various other contact pads **405** and **411**.

The output contact pad **409** is connected to an output pin **413** of the integrated circuit package **401** by an output bond wire **417**. The output bond wire **417** is secured to the output pin **413** and the output contact pad **409**. The bootstrap contact pad **407** is connected to bootstrap pin **415** of the integrated circuit package **401** by a bootstrap bond wire **419**. The bootstrap bond wire **419** is secured to the bootstrap pin **415** and the bootstrap contact pad **407**.

The bootstrap capacitor C_b is connected between the bootstrap pin **415** and the gate drive circuitry on the integrated circuit **403** through another package pin and high side gate drive input pad **421**. Finally, the load is connected to the output pin **413**. The other various pins of the integrated circuit package **401** are used in known configurations, such as for power supply, ground, control lines, and such.

As noted above, in an alternate embodiment, the output contact pad **409** and the bootstrap contact pad **407** is one and the same. Whichever pad conducts current to the load is made large, such as contact pad **411**, but not changed in size if also attached to C_b.

Thus, the above described IC driver provides a stable bootstrap power supply, even when large amounts of power are being delivered. This is accomplished by connecting the bootstrap capacitor to a dedicated bootstrap pin and contact pad.

From the foregoing, it will be appreciated that specific embodiments of the invention have been described herein for purposes of illustration, but that various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

I claim:

1. An integrated circuit driver comprising:

a high side transistor;

a low side transistor connected in series to said high side transistor such that the source of said high side transistor is connected to the drain of said low side transistor, the source of the high side transistor and the drain of the low side transistor forming an output node;

a bootstrap contact pad connected to the output node;

a bootstrap capacitor having a first terminal connected to said bootstrap contact pad, wherein the bootstrap capacitor couples to the gate and the source of the high side transistor;

a high side gate drive for selectively controlling the high side transistor, said high side gate drive having as an input a signal from a second terminal of said bootstrap capacitor;

a low side gate drive for selectively controlling the low side transistor; and

an output contact pad connected to the output node, said output contact pad providing an output signal to a load.

2. The driver of claim 1 wherein said high side transistor and said low side transistor are NMOS transistors.

3. The driver of claim 1 wherein said output contact pad and said bootstrap contact pad are the same.

4. The driver of claim 1 further including an output package pin connected to said output pad by an output bond wire.

5. The driver of claim 1 further including a bootstrap package pin connection to said bootstrap contact pad by a bootstrap bond wire.

6. The driver of claim 3 further including an output package pin connected to said output pad by an output bond wire.

7. The driver of claim 3 further including a bootstrap package pin connection to said bootstrap contact pad by a bootstrap bond wire.

8. An integrated circuit package comprising:

(a) an integrated circuit die, said die having formed thereon:

(1) a high side transistor;

(2) a low side transistor connected in series to said high side transistor such that the source of said high side transistor is connected to the drain of said low side transistor, the source of the high side transistor and the drain of the low side transistor forming an output node;

(3) a set of two bootstrap contact pads connected to the output node;

(4) a high side gate drive for selectively controlling the high side transistor;

(5) a low side gate drive for selectively controlling the low side transistor; and

(6) a set of two output contact pads connected to the output node, said output contact pads providing output signals to a load;

(b) a set of two carrier packages having a plurality of package pins including at least a bootstrap package pin and an output package pin, said carrier packages for securing said integrated circuit die;

(c) a set of two output bond wires connecting said output contact pads with said output package pins; and

(d) a set of two bootstrap bond wires connecting said bootstrap contact pads with said bootstrap package pins.

9. The package of claim 8 wherein said high side transistor and said low side transistor are NMOS transistors.

10. The package of claim 8 wherein said output contact pad and said bootstrap contact pad are the same.

11. The package of claim 8 wherein a first terminal of a bootstrap capacitor is connected to said bootstrap package pin and a second terminal of said bootstrap capacitor is connected to an input to said high side gate drive.

12. A method for driving a load using a high side switch and a low side switch connected in series, the source of said high side switch connected to the drain of said low side switch, the connection of said high side switch and said low side switch being an output node, the method comprising:

providing a bootstrap contact pad connected to said output node;

providing an output pad connected to said output node;

connecting a bootstrap capacitor to said bootstrap contact pad, said bootstrap capacitor used to provide a bootstrap power supply to a gate drive of said high side switch, wherein the bootstrap capacitor couples to the gate and the source of the high side transistor; and

connecting said output pad to said load.

13. An integrated circuit driver comprising:

a high side transistor;

a low side transistor connected in series to said high side transistor such that the source of said high side transistor is connected to the drain of said low side transistor, the source of the high side transistor and the drain of the low side transistor forming an output node;

a combination bootstrap/output contact pad connected to the output node;

a bootstrap capacitor having a first terminal connected to said bootstrap/output contact pad via a bootstrap capacitor package pin, wherein the bootstrap capacitor couples to the gate and the source of the high side transistor;

a high side gate drive for selectively controlling the high side transistor, said high side gate drive having as an input a signal from a second terminal of said bootstrap capacitor;

a low side gate drive for selectively controlling the low side transistor; and

an output package pin connecting said bootstrap/output contact pad to a load.

14. The driver of claim 13 wherein said high side transistor and said low side transistor are NMOS transistors.

* * * * *

EXHIBIT B

(12) **United States Patent**
Wu

(10) **Patent No.: US 7,714,558 B2**
(45) **Date of Patent: May 11, 2010**

(54) **SHORT CIRCUIT CURRENT RATCHETING IN SWITCH MODE DC/DC VOLTAGE REGULATORS**

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(73) Assignee: **Monolithic Power Systems, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 544 days.

(21) Appl. No.: **11/216,276**

(22) Filed: **Aug. 30, 2005**

(65) **Prior Publication Data**

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Related U.S. Application Data

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(51) **Int. Cl.**
G05F 1/00 (2006.01)

(52) **U.S. Cl.** **323/284**

(58) **Field of Classification Search** 323/282–286; 361/794, 762, 782; 363/65, 67, 71, 72, 13
See application file for complete search history.

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Primary Examiner—Bao Q Vu
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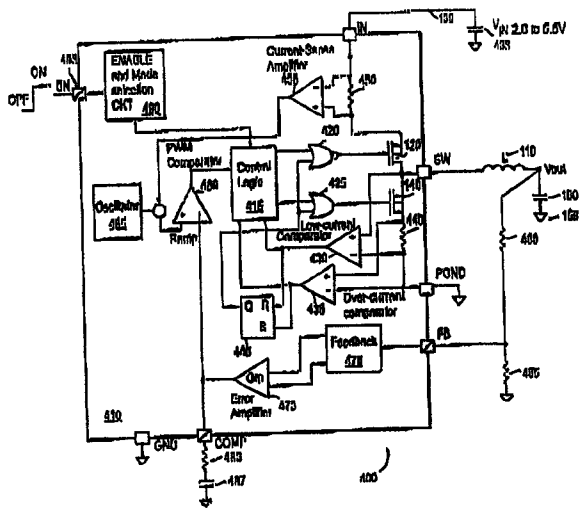
(74) *Attorney, Agent, or Firm*—Perkins Coie LLP

(57) **ABSTRACT**

In an embodiment, an apparatus is provided. The apparatus includes a high side pass device. The apparatus also includes a low side pass device coupled in series to the high side pass device. The apparatus further includes a control module coupled to the high side pass device and the low side pass device. The control module is coupled to the high side pass device and the low side pass device to control the high side pass device and the low side pass device.

Additionally, the apparatus includes a first resistor coupled in series with the high side pass device and the low side pass device. Furthermore, the apparatus includes a first comparator coupled in parallel with the first resistor. The first comparator has a threshold voltage input differential corresponding to a first current limit, and an output of the first comparator is coupled to the control module. Moreover, the apparatus includes a second comparator coupled to sense current of the high side pass device as a voltage. The second comparator has a threshold voltage input differential corresponding to a second current limit. An output of the second comparator is coupled to the control module. The second current limit is higher than the first current limit. Also, the control module is operable to lock out the high side pass device responsive to the output of the first comparator until a reset signal is received and is operable to lock out the high side pass device responsive to the output of the second comparator until a low current signal is received.

10 Claims, 7 Drawing Sheets



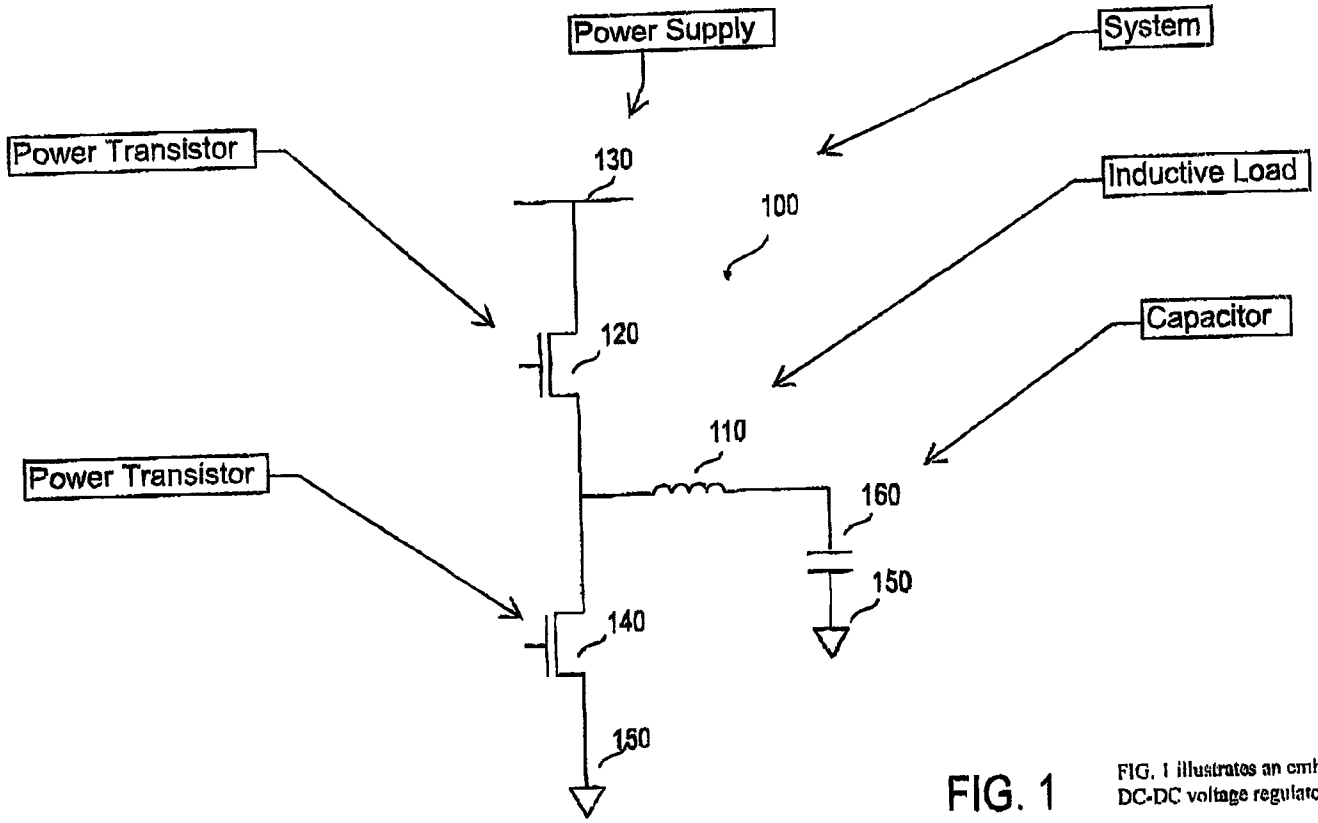


FIG. 1

FIG. 1 illustrates an embodiment of a DC-DC voltage regulator output.

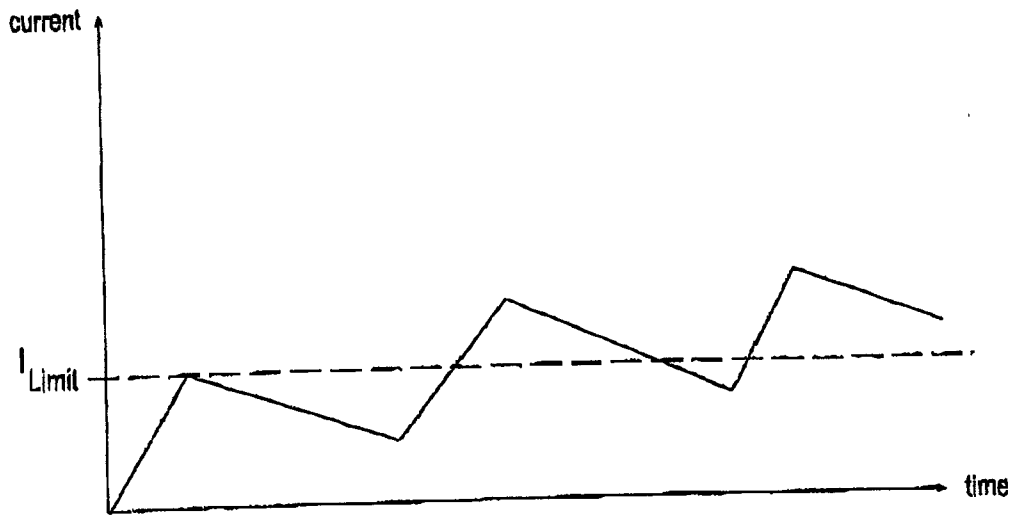


FIG. 2

FIG. 3

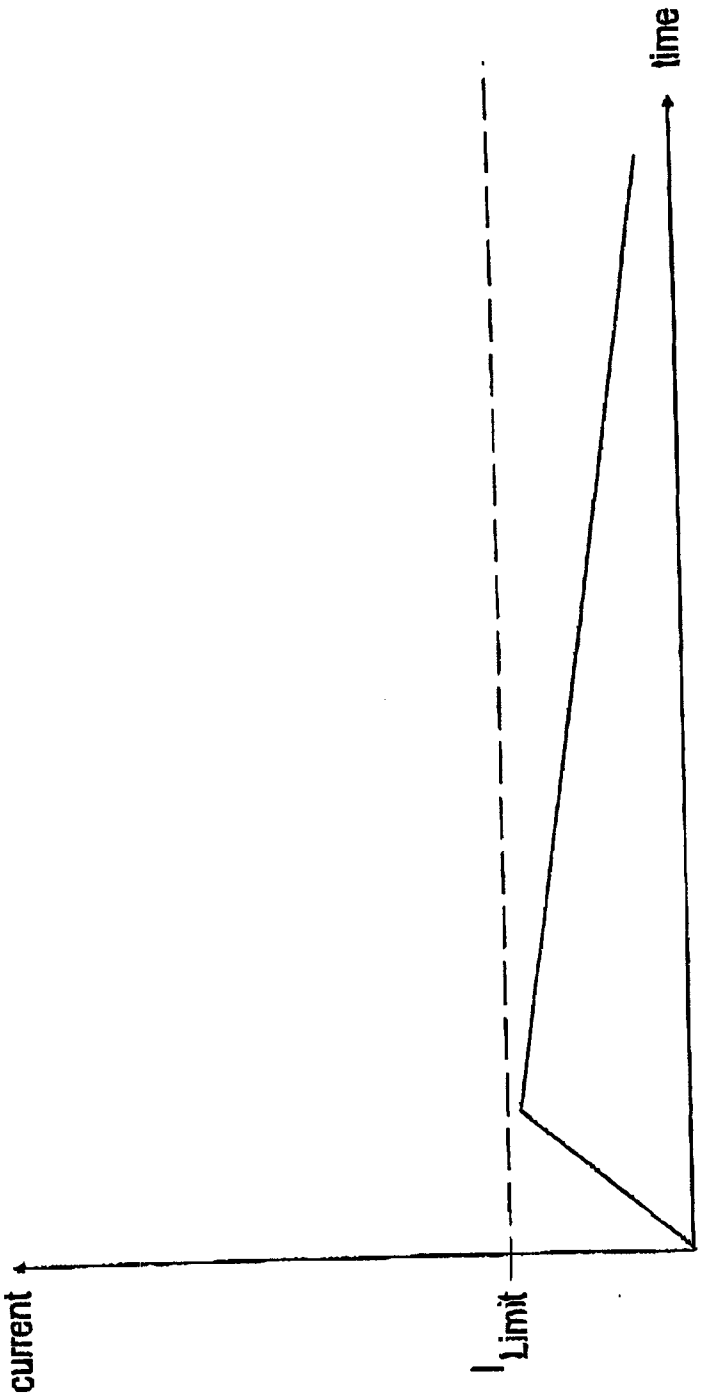


FIG. 3 illustrates frequency folding in the embodiment of FIG. 1.

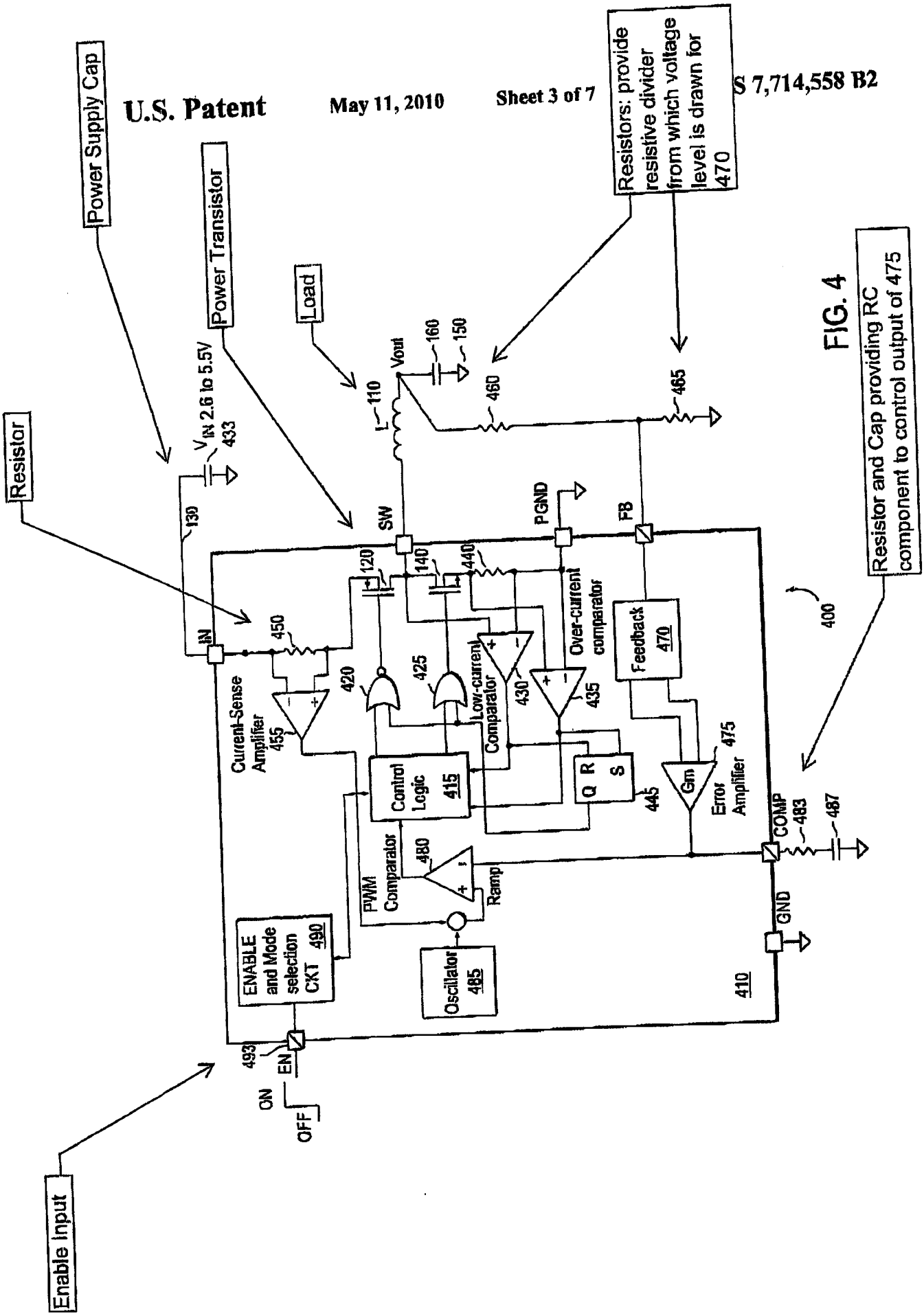


FIG. 4

FIG. 4 illustrates an embodiment of a current overload protection apparatus for the DC-DC voltage regulator output of FIG. 1.

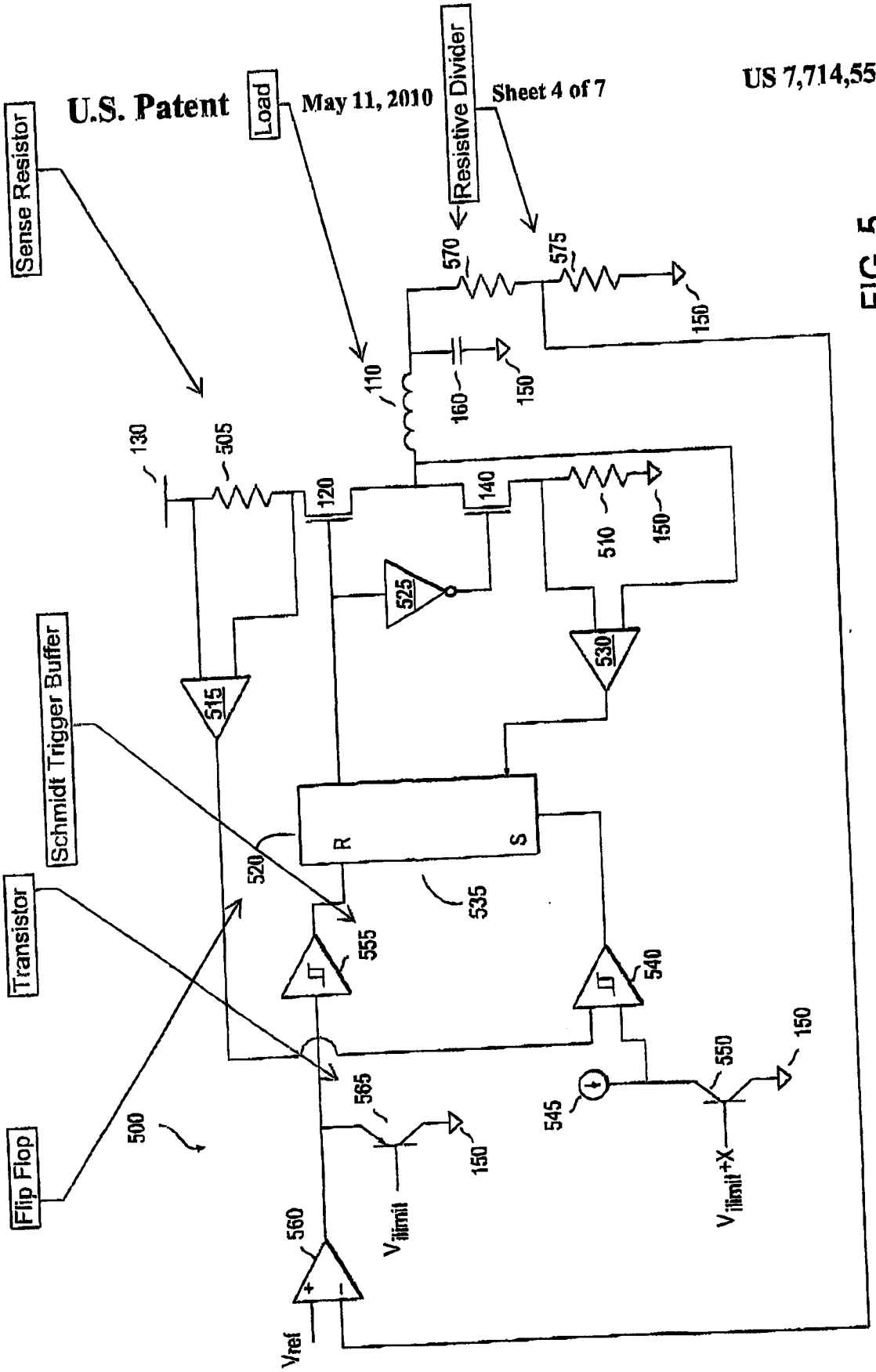
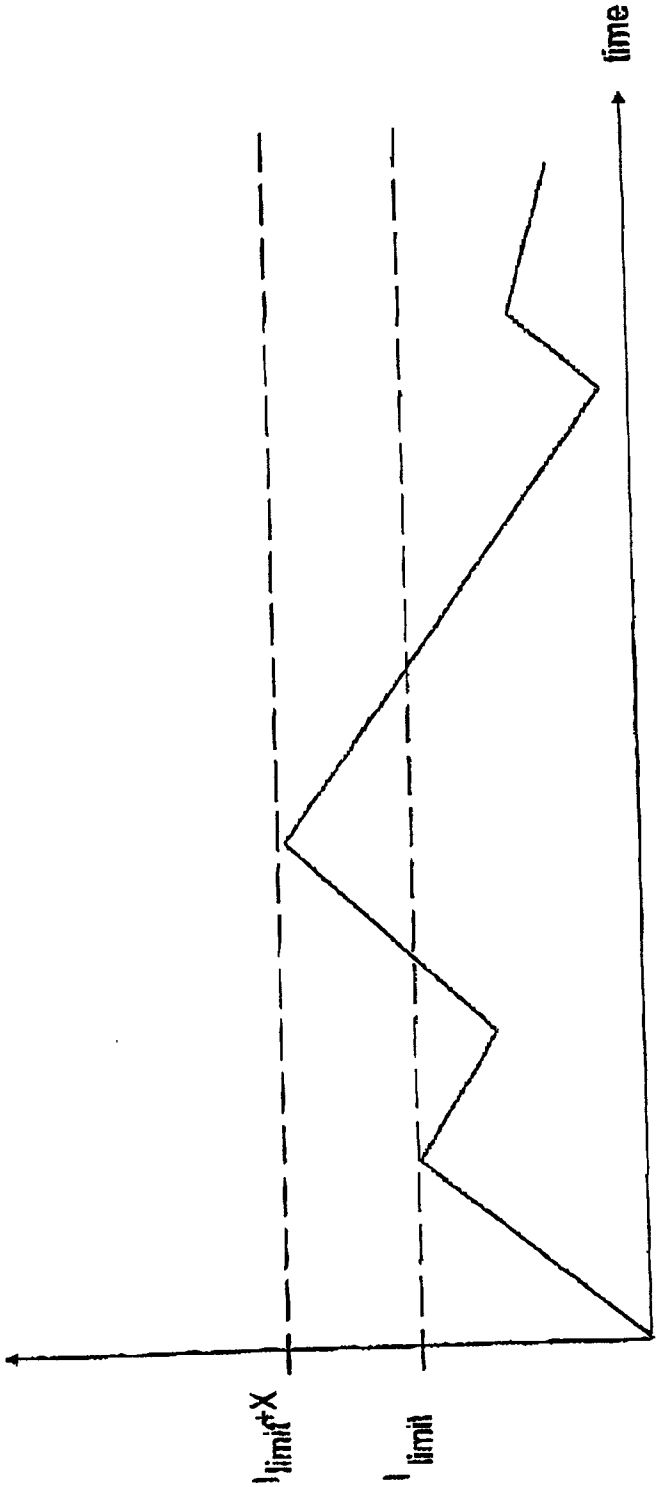


FIG. 5

FIG. 5 illustrates an alternate embodiment of the current overload protection apparatus for the DC-DC voltage regulator output of FIG. 1.

FIG. 6



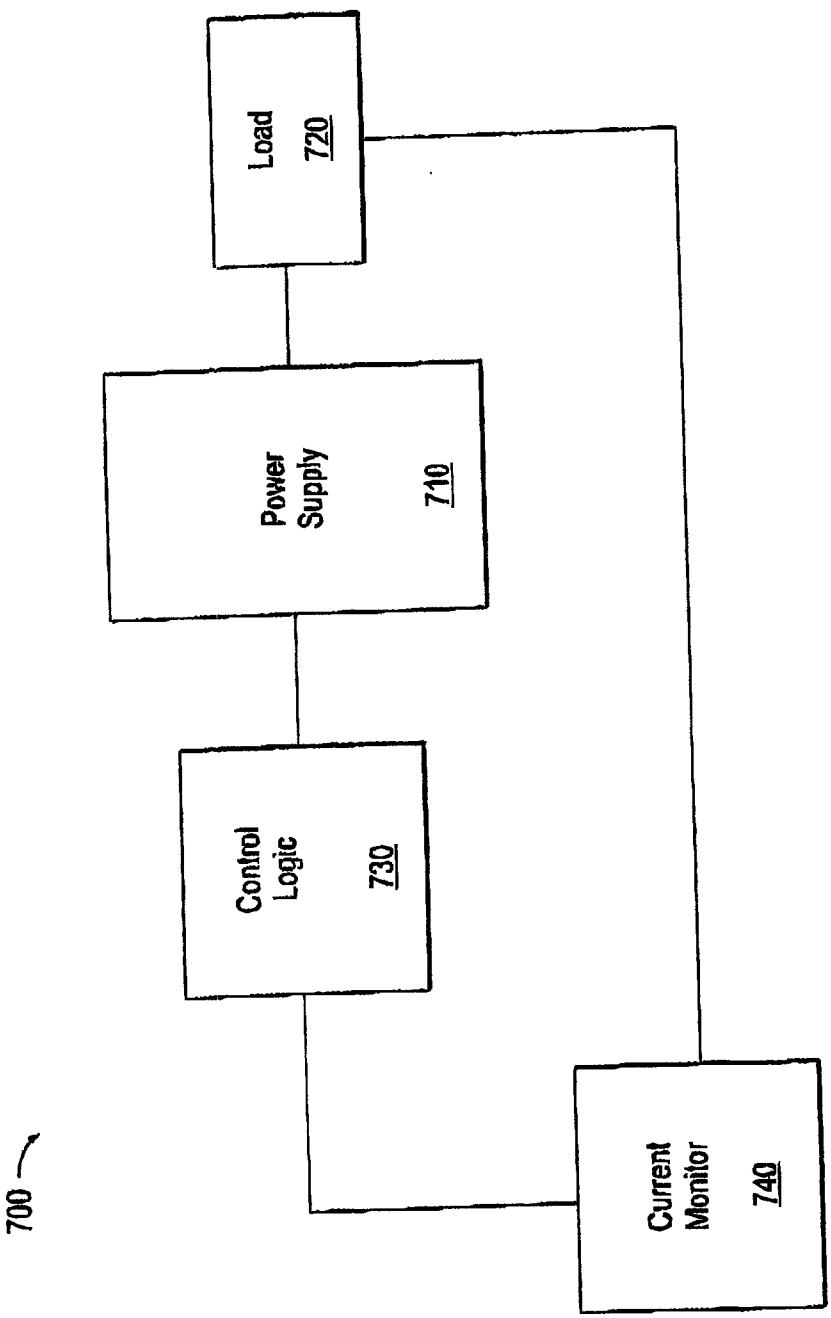


FIG. 7

FIG. 7 illustrates another alternate embodiment of the current overload protection apparatus for the DC-DC voltage regulator output of FIG. 1.

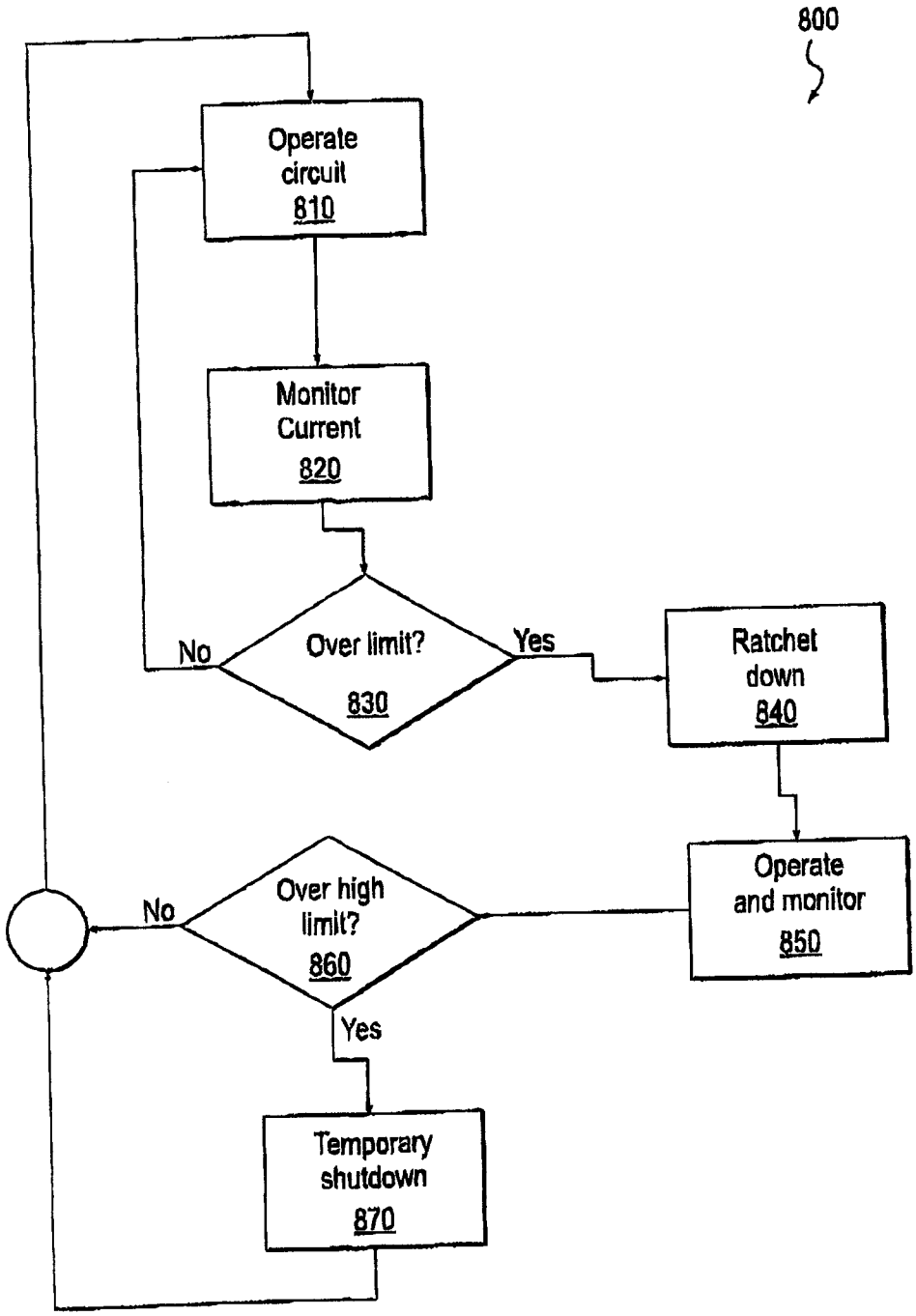


FIG. 8

FIG. 8 illustrates an embodiment of a process of current limiting.

SHORT CIRCUIT CURRENT RATCHETING IN SWITCH MODE DC/DC VOLTAGE REGULATORS

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority to U.S. provisional patent application No. 60/605,423, filed on Aug. 30, 2004, which is hereby incorporated herein by reference.

BACKGROUND

A DC/DC voltage regulator is operative to maintain a level output voltage despite variations in power supply voltage or current drawn by a load. Many portable devices require a steady voltage supply such as that provided by a DC/DC voltage regulator. Switch mode regulators can be subject to a phenomenon of current ratcheting at shorted loads due to finite on times to determine an over current condition. Nearly every switch-mode device has a finite loop response time to measure current in the inductor. Depending on the input voltage, the current can rise high enough to cause a catastrophic failure in a device.

For this reason, in fixed frequency parts, it is common to use frequency fold-back to change the amount of current ratcheting that a part can see. A common problem caused by frequency fold-back is a large current ripple in the inductor. For this reason, a larger than normal bypass or output capacitor is chosen to reduce the ripple voltage. And if the frequency is folded back too much, the loop may become unstable. Thus, choosing the correct fold-back frequency range for wide application is not an easy task.

SUMMARY

The present invention is described and illustrated in conjunction with systems, apparatuses and methods. In addition to the aspects of the present invention described in this summary, further aspects of the invention will become apparent by reference to the drawings and by reading the detailed description that follows.

In an embodiment, a DC/DC switch mode voltage regulator with a high side pass device and a low side pass device is provided. The voltage regulator includes means for detecting an over current condition over a current limit on the high side pass. The voltage regulator also includes means for locking out the high side pass device and turning on the low side pass device until a second current limit located on the low side pass device is reached if the over current condition is detected.

In another embodiment, a method implemented on a DC/DC switch mode voltage regulator with a high side pass device and a low side pass device is provided. The method includes detecting an over current condition over a current limit on the high side pass. The method also includes locking out the high side pass device and turning on the low side pass device until a second current limit located on the low side pass device is reached if the over current condition is detected.

In still another embodiment, an apparatus is provided. The apparatus includes a high side pass device. The apparatus also includes a low side pass device coupled in series to the high side pass device. The apparatus further includes a control module coupled to the high side pass device and the low side pass device. The control module is coupled to the high side pass device and the low side pass device to control the high side pass device and the low side pass device.

Additionally, the apparatus includes a first resistor coupled in series with the high side pass device and the low side pass device. Furthermore, the apparatus includes a first comparator coupled in parallel with the first resistor. The first comparator has a threshold voltage input differential corresponding to a first current limit, and an output of the first comparator is coupled to the control module. Moreover, the apparatus includes a second comparator coupled to sense current of the high side pass device as a voltage. The second comparator has a threshold voltage input differential corresponding to a second current limit. An output of the second comparator is coupled to the control module. The second current limit is higher than the first current limit. Also, the control module is operable to lock out the high side pass device responsive to the output of the first comparator until a reset signal is received and is operable to lock out the high side pass device responsive to the output of the second comparator until a low current signal is received.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated in an exemplary manner by the accompanying drawings. The drawings should be understood as exemplary rather than limiting, as the scope of the invention is defined by the claims.

FIG. 1 illustrates an embodiment of a DC-DC voltage regulator output.

FIG. 2 illustrates current overload in the embodiment of FIG. 1.

FIG. 3 illustrates frequency folding in the embodiment of FIG. 1.

FIG. 4 illustrates an embodiment of a current overload protection apparatus for the DC-DC voltage regulator output of FIG. 1.

FIG. 5 illustrates an alternate embodiment of the current overload protection apparatus for the DC-DC voltage regulator output of FIG. 1.

FIG. 6 illustrates current ratcheting in the embodiment of FIG. 4.

FIG. 7 illustrates another alternate embodiment of the current overload protection apparatus for the DC-DC voltage regulator output of FIG. 1.

FIG. 8 illustrates an embodiment of a process of current limiting.

DETAILED DESCRIPTION

A system, method and apparatus is provided for Short Circuit Current Ratcheting in Switch Mode DC/DC Voltage Regulators. The specific embodiments described in this document represent exemplary instances of the present invention, and are illustrative in nature rather than restrictive.

In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the invention. It will be apparent, however, to one skilled in the art that the invention can be practiced without these specific details. In other instances, structures and devices are shown in block diagram form in order to avoid obscuring the invention.

Reference in the specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment, nor are separate or alternative embodiments mutually exclusive of other embodiments.

The present invention describes, in some embodiments, a new scheme that eliminates frequency fold-back from the protection scheme of switch-mode regulators and allows for a clean startup without the need for a change in switching frequency for the entire duration of operation.

In some embodiments, a sense element is used to measure the current in the inductor. A comparator is used to compare the sense element to another matching element that depicts a finite known current threshold indicating the overcurrent conditions. When this current threshold is exceeded, the comparator signals the logic to latch the low side switch on until a low side current limit is reached. This current limit on the low side can be set to any value positive, negative, or zero inductor current depending on the application.

A DC/DC switching voltage regulator, in some embodiments, consists of a PWM controller, two controlled pass devices that are connected in series between a supply voltage and ground, an inductor that is connected to the common point between the two pass devices, and a capacitor connected between the output node and ground after the inductor. By modulating the pass devices, the inductor will build up energy and discharge it into the capacitor. The charge and discharge rates are governed by the equation:

$$V = L\frac{dI}{dT}$$

The increase in current in the inductor is

$$dI_{charge} = \frac{Vin - R_{ramp} \times dI_{charge} - Vout}{L} dT_{on}$$

where Vin is the supply voltage, Vout is the output voltage, and Ramp is the resistance in the upper pass device. The discharge current in the inductor is defined by the equation:

$$dI_{discharge} = \frac{Vout + R_{rondwn} \times dI_{discharge}}{L} dT_{off}$$

where Rondwn is the resistance in the lower pass device. During normal operation dIcharge=dIdischarge and dTon and dToff is a function of the switching frequency. Since the loop takes a finite time to respond there is a minimum on time for the switch. This time can be as low as 20 nanoseconds but as high as 200 nanoseconds. This is due to the fact that the upper pass element needs to be turned on to detect the amount of current in the inductor, and then turned off. The length of the minimum on time can be attributed to driver delays, PWM comparator delays, current sense amplifier delays, and so on.

Current ratcheting is a condition that exists when dIcharge>dIdischarge. This can occur when the output is shorted to ground, then dTon=dTmin, and Vout is 0. Then the amount of energy discharged by the inductor during the dToff is small, and the current continues to rise cycle by cycle. The conventional ways to make sure that the inductor is discharged are by increasing the dToff time, and by lowering the frequency of operation. In accordance with various embodiments, the inductor current is sensed and if the current ratchets above a fixed value, the loop will lock out the upper pass device and latch the lower pass device until the current has decayed to a preset limit.

Reference to the figures may provide further understanding of various embodiments. FIG. **1** illustrates an embodiment of a DC-DC voltage regulator output. System **100** includes high and low supply transistors between a power rail and ground, an inductive load and a capacitor. Inductive load **110** may be an actual inductor or a component which operates in a manner similar to an inductor. Capacitor **160** is coupled between inductive load **110** and ground **150**. Power is supplied to load **110** through power transistor **120** (current is sourced) from power supply **130**. Current may be sunk from inductive load **110** through power transistor **140** to ground **150**.

This design involves a potential problem, in that the time it takes to turn transistors **120** and **140** on and off may be long enough to allow currents to overload inductor **110**. FIG. **2** illustrates current overload in the embodiment of FIG. **1**. Current levels approach a limit value, and the system reduces the current level. However, the decay time for the current may not allow the current level to drop to zero. As a result, the device may then increase the current level again, this time overshooting the maximum current limit before the system reduces current again. This typically happens as a result of the frequency at which the system operates—it may react the voltage regulator before the current decays to an acceptable level.

A common response to this problem is to fold frequency—to reduce the operating frequency of the system so that current levels can be reduced acceptably in overlimit situations. FIG. **3** illustrates frequency folding in the embodiment of FIG. **1**. Instead of allowing the system to react and have the current level ratchet up, the current is allowed to decay over a longer time until an acceptable limit is reached. Not shown is the lead-up to this situation, where the device may run to the limit, and then be reduced to a level too high to avoid an overcurrent situation. Frequency folding can avoid the overcurrent situation, but it also slows down operation of the system and the load to which power is supplied.

As an alternative, circuitry may be introduced to sense the current level and ensure that overcurrent situations are allowed to decay appropriately. FIG. **4** illustrates an embodiment of a current overload protection apparatus for the DC-DC voltage regulator output of FIG. **1**. System **400** includes device **410** (a DC-DC voltage regulator) and various exterior circuitry which may be supplied as part of an overall system. Device **410** may be enabled by enable input **493**, which is tied to internal enable circuitry **490**. Power may be supplied from a power supply which is modeled as capacitor **433**.

Current into the load **110** through power transistor **120** is monitored passing that current through resistor **450** which is sensed in current sense amplifier **455** (an amplifier which level-shifts the voltage across its inputs and amplifies that voltage). The output of comparator **455** is mixed with the output of an oscillator **485** and provided as input to comparator **480**. Along with feedback through feedback module **470** and error amplifier **475**, comparator **480** and control module **415**, this provides the feedback loop for the pulse width modulator of device **410**. Resistors **460** and **465** provide a resistive divider from which a voltage level is drawn for feedback component **470**. Similarly, resistor **483** and capacitor **487** provide an RC component which controls the output of comparator **475**.

Comparator **435** senses current from resistor **440**, which is coupled in series with power transistor **140**, and provides a set input to flip-flop **445**. Comparator **430** senses current through resistor **440** and power transistor **140** (the same current) and provides a reset input to flip-flop **445**. These outputs are also provided to control logic **415**. Typically, control logic **415** operates gates **420** and **425** to turn power transistors **120** and

140 on and off. However, when an overcurrent condition is sensed, the output of flip-flop 445 causes transistor 140 to turn on and transistor 120 to turn off. Once current through transistor 140 has decayed sufficiently, flip-flop 445 is reset, and normal operation returns. Thus, by altering trip points of comparators 430 and 435, various current levels for overlimit and low current can be set.

An alternate embodiment of regulation circuitry may be described without reference to the surrounding pulse width modulation circuitry. FIG. 5 illustrates an alternate embodiment of the current overload protection apparatus for the DC-DC voltage regulator output of FIG. 1. System 500 operates the power supply to load 110. Resistive divider 570 and 575 provides a voltage which is fed back and compared with a reference voltage at comparator 560. The output of comparator 560 is biased with transistor 565, which receives a Vilimit voltage input to determine the bias level. Schmitt-triggered buffer 555 then provides the biased output of comparator 560 as a logic input to flip-flop 530. Flip-flop 520 then controls transistors 120 and 140 (through inverter 525). Note that in a full implementation of this device, buffer 555 may be an error amplifier similar to amplifier 475 of FIG. 4, which would then be integrated into the PWM feedback loop of the over all system. In the illustration of FIG. 5, the PWM feedback loop and other details are not illustrated to avoid obscuring details of the embodiment.

Current through transistor 120 can be measured using sense resistor 505 (coupled in series with transistor 120), comparator 515, and Schmitt-triggered comparator 540. Comparator 540 also receives as input the output of transistor 550, which is biased by a voltage Vilimit+X. Current source 545 completes the bias circuitry of this component. Thus, when current through sense resistor 505 causes a voltage exceeding the bias voltage of transistor 550, comparator 540 can set (or reset) the flip-flop 520. This allows for turning off supply of current to load 110. Similarly, when current has decayed sufficiently, this may be sensed through comparator 530, using sense resistor 510 and the output node coupled to load 110, for example. Thus, comparator 530 may reset (or set) flip-flop 520, allowing normal operation to continue.

Where exactly sense resistors 505 and 510 are placed, and how exactly overcurrent and undercurrent conditions are sensed may vary in different embodiments. Likewise, the values of Vilimit and Vilimit+X may be chosen as appropriate in various embodiments. Typically, Vilimit+X will be a higher value than Vilimit, and will provide a higher current limit as a limit which can be used to shut down the system and avoid a current overload.

Operation of the device or system may be understood with reference to FIG. 6. FIG. 6 illustrates current ratcheting in the embodiment of FIG. 4. Current may rise to Ilimit, and then be ratcheted back down. If the device is operating at too high a frequency, then the current can increase to Ilimit+X. At this point, the device can be shut down (by turning off the high pass transistor 120 and turning on the low pass transistor 140) until the current decays to an acceptable level (as may be defined by a low current value).

Various embodiments can be implemented with the same general approach. FIG. 7 illustrates another alternate embodiment of the current overload protection apparatus for the DC-DC voltage regulator output of FIG. 1. System 700 includes a power supply, control logic, load, and current monitor. Power supply module 710 supplies power to load 720 under control of control logic 730. Current monitor 740 monitors supply of current to load 720, and interrupts control logic 730 to shut down power supply 710 when an overcurrent condition exists.

The process by which these circuits operate may also be illustrative. FIG. 8 illustrates an embodiment of a process of current limiting. Process 800 includes operating the device, monitoring current, ratcheting current down, further operation, determining if a high limit has been exceeded, and temporarily shutting down the device. Process (method) 800 and other processes of this document are implemented as a set of modules, which may be process modules or operations, software modules with associated functions or effects, hardware modules designed to fulfill the process operations, or some combination of the various types of modules, for example. The modules of process 800 and other processes described herein may be rearranged, such as in a parallel or serial fashion, and may be reordered, combined, or subdivided in various embodiments.

Process 800 begins with operation of the circuit at module 810. The current load of the circuit is monitored at module 820. If the current is not over a first limit, the circuit continues operation at module 810. If the current is over the first limit, the current is ratcheted down at module 840. The circuit then continues to operate at module 850. A determination is made at module 860 as to whether a high or second current limit has been exceeded. If not, the circuit continues operation at module 810. If the second current limit has been exceeded, then a temporary shutdown at module 870 occurs until the current load decays to an acceptable level.

In one embodiment, this is accomplished by using a first current limit of 1.7 A and a second current limit of 2.2 A. Thus, if the current exceeds 1.7 A, the system is turned off normally. If the current exceeds 2.2 A, then the system is turned off until the current decays to a low value.

Features and aspects of various embodiments may be integrated into other embodiments, and embodiments illustrated in this document may be implemented without all of the features or aspects illustrated or described. One skilled in the art will appreciate that although specific examples and embodiments of the system and methods have been described for purposes of illustration, various modifications can be made without deviating from the spirit and scope of the present invention. For example, embodiments of the present invention may be applied to many different types of databases, systems and application programs. Moreover, features of one embodiment may be incorporated into other embodiments, even where those features are not described together in a single embodiment within the present document. Accordingly, the invention is described by the appended claims.

What is claimed is:

1. A method implemented on a DC/DC switch mode voltage regulator with a high side pass device and a low side pass device, the method comprising:

detecting an over current condition over a current limit on the high side pass; and

if the over current condition is detected, locking out the high side pass device and turning on the low side pass device until an undercurrent condition under a second current limit located on the low side pass device is reached, wherein once said second current limit is reached on the low side pass device, the high side pass device can be turned back on such that the states of said high side pass device and low side pass device are interdependent and cannot be controlled independently.

2. The method of claim 1, further comprising:

detecting an over current condition over a lower current limit; and

if the over current condition over the lower current limit is detected, locking out the high side pass device and turning on the low side pass device until a reset signal is received.

3. The method of claim 2, further comprising:

resetting the DC/DC switch mode voltage regulator, the resetting providing the reset signal.

4. The method of claim 3, further comprising:

providing power through the high side pass device.

5. The method of claim 4, further comprising:

operating the DC/DC switch mode voltage regulator responsive to an enable signal.

6. A DC/DC switch mode voltage regulator with a high side pass device and a low side pass device comprising:

means for detecting an over current condition over a current limit on the high side pass device; and

if the over current condition is detected, means for locking out the high side pass device and turning on the low side pass device until an undercurrent condition under a second current limit located on the low side pass device is

reached, wherein once said second current limit is reached on the low side pass device, the high side pass device can be turned back on such that the states of said high side pass device and low side pass device are interdependent and cannot be controlled independently.

7. The apparatus of claim 6, wherein

the means for detecting includes a sense element and a finite current level comparator to determine an over current condition.

8. The apparatus of claim 6, further comprising:

a means for determining when the over current condition has been removed.

9. The apparatus of claim 6, further comprising:

a latch for overriding the control of a PWM system to keep the high side pass device off and keep the low side pass device on.

10. The apparatus of claim 6, further comprising:

means for enabling the DC/DC switch mode voltage regulator.

* * * * *