HENNIGAN, BENNETT & DORMAN LLP
RODERICK G. DORMAN (SBN 96908)
dormanr@hbdlawyers.com
LAWRENCE M. HADLEY (SBN 157728)
hadleyl@hbdlawyers.com
OMER SALIK (SBN 223056)
saliko@hbdlawyers.com
865 South Figueroa Street, Suite 2900
Los Angeles, California 90017
(213) 694-1200 - Telephone
(213) 694-1234 - Facsimile

Attorneys for Plaintiffs and Counterdefendants, MICROPROCESSOR ENHANCEMENT CORPORATION and MICHAEL H. BRANIGIN

UNITED STATES DISTRICT COURT

CENTRAL DISTRICT OF CALIFORNIA

SACV08-1123 DOC

MICROPROCESSOR ENHANCEMENT CORPORATION and MICHAEL H. BRANIGIN, Plaintiffs, vs. TEXAS INSTRUMENTS INCORPORATED Defendant.	Case No. **COMPLAINT FOR PATENT INFRINGEMENT** **DEMAND FOR JURY TRIAL**

For their complaint against Texas Instruments Incorporated ("TI" or "Defendant"), Plaintiffs Microprocessor Enhancement Corporation and Michael H. Branigin (collectively "Plaintiffs") allege as follows:

THE PARTIES

1. Plaintiff Microprocessor Enhancement Corporation ("MEC") is a corporation duly organized and existing under the laws of the State of Delaware, with its principal place of business at 500 Newport Center Drive, Newport Beach, California 92660. MEC holds an exclusive license to U.S. Patent No. 5,471,593 ("the '593 patent" or "Patent-in-Suit"). MEC's exclusive license includes the rights to sublicense the '593 patent and to enforce the '593 patent against alleged infringers.

2. Plaintiff Michael H. Branigin is an individual residing at 151 Ivy Hills Rd., Southbury, Connecticut 06488. Mr. Branigin is the inventor, owner, and licensor of the '593 Patent.

3. Defendant Texas Instruments Incorporated ("TI") is a corporation in the State of Delaware, with its place of business at 12500 TI Boulevard, Dallas, Texas 75243.

NATURE OF THE ACTION

4. In this civil action, Plaintiffs seek damages and injunctive relief against Defendant for acts of patent infringement in violation of the Patent Act of the United States, 35 U.S.C. §§ 1 et seq.

JURISDICTION AND VENUE

5. This Court has subject matter jurisdiction of such federal question claims pursuant to 28 U.S.C. §§ 1331 and 1338(a).

6. Venue is proper under 28 U.S.C. §§ 1391(c) and 1400(b), in that the acts and transactions complained of herein were conceived, carried out, made effective, or had effect within the State of California and within this district, among other places. On information and belief, Defendant has distribution facilities in this district and resides in this judicial district by virtue of its business activities in this district.

Defendant is licensed to do business in California by the California Secretary of State. Defendant maintains a registered agent for service of process within this judicial district – namely, CT Corporation System, 818 West Seventh Street Los Angeles, California 90017.

7. On information and belief, this Court has personal jurisdiction over Defendant.

BACKGROUND

8. On November 28, 1995, the United States Patent & Trademark Office duly and legally issued United States Letters Patent No. 5,471,593 ("the '593 Patent"), entitled "COMPUTER PROCESSOR WITH AN EFFICIENT MEANS OF EXECUTING MANY INSTRUCTIONS SIMULTANEOUSLY." A true and correct copy of the '593 Patent is attached as Exhibit 1 and incorporated herein by reference.

9. The '593 Patent claims a pipelined processor as well as a method for executing instructions in a pipelined processor.

10. Defendant TI has received written notice of the '593 Patent and an offer to license the technology on commercially reasonable terms. To date, Defendant TI has not obtained a license under the '593 Patent from Plaintiff MEC.

FIRST CLAIM FOR RELIEF

INFRINGEMENT OF U.S. PATENT NO. 5,471,593

11. Plaintiffs incorporate herein by reference the allegations set forth in paragraphs 1-10 of this Complaint as though fully set forth herein.

12. Plaintiff MEC is the owner by exclusive license of the entire right, title, and interest, including the right to enforce, in and to the '593 Patent.

13. Plaintiff Branigin is the inventor and exclusive licensor of the '593 Patent.

14. TI has actual knowledge of the '593 Patent.

15. TI has directly infringed and continues to directly infringe the '593 Patent by making, using, selling, or offering for sale in or importing into the United

States electronic microprocessor and core logic devices known as the OMAP 2 and OMAP 3 family of processors, that embody or otherwise practice one or more of the claims of the '593 Patent.

16. On information and belief, TI has indirectly infringed and continues to indirectly infringe the '593 Patent by actively inducing direct infringement by other persons who operate and/or use the OMAP 2 and OMAP 3 family of processors, or otherwise practice one or more of the claims of the '593 Patent with respect to the OMAP 2 and OMAP 3 family of processors, when TI had knowledge of the '593 Patent and knew or should have known that its actions would induce direct infringement by others and intended that its actions would induce direct infringement by others.

17. On information and belief, TI has indirectly infringed and continues to indirectly infringe the '593 Patent by contributory infringement by providing non-staple articles of commerce to others for use in an infringing system or method with respect to the OMAP 2 and OMAP 3 family of processors with knowledge of the '593 Patent and knowledge that these non-staple articles of commerce are used as a material part of the claimed inventions of the '593 Patent.

18. On information and belief, TI will continue to infringe the '593 Patent as alleged in this Complaint unless enjoined by this Court.

19. On information and belief, TI's infringement of the '593 Patent is, has been, and continues to be willful and deliberate.

20. As a direct and proximate result of TI's infringement of the '593 Patent, Plaintiffs have been and continue to be damaged in an amount yet to be determined.

21. Unless a preliminary and permanent injunction are issued enjoining TI and its respective officers, agents, servants, and employees, and all persons acting in concert with TI, from infringing the '593 patent, Plaintiffs will be greatly and irreparably harmed.

22. By reason of the above acts, Plaintiffs are entitled to injunctive relief

enjoining and restraining TI, and its respective officers, agents, servants, and employees, and all persons acting in concert with TI, from further infringement of the '593 Patent with respect to the OMAP 2 and OMAP 3 family of processors.

PRAYER FOR RELIEF

WHEREFORE, Plaintiffs pray for judgment against Defendant as follows:

1. For a judicial determination and declaration that Defendant directly infringes United States Letters Patent No. 5,471,593 by making, using, offering to sell and/or selling the OMAP 2 and OMAP 3 family of processors;

2. For a judicial determination and declaration that Defendant induces direct infringement of United States Letters Patent No. 5,471,593 with respect to the OMAP 2 and OMAP 3 family of processors;

3. For a judicial determination and declaration that Defendant commits contributory infringement of United States Letters Patent No. 5,471,593 with respect to the OMAP 2 and OMAP 3 family of processors;

4. For a judicial determination and decree that Defendant's infringement of United States Letters Patent No. 5,471,593 is willful;

5. For damages resulting from Defendant's past and present infringement of United States Letters Patent No. 5,471,593, and the trebling of such damages because of the willful and deliberate nature of its infringement;

6. For injunctive relief preliminarily and permanently enjoining against further infringement of United States Letters Patent No. 5,471,593 by Defendant, its respective officers, directors, shareholders, agents, servants, employees, and all other entities and individuals acting in concert with the enjoined entities or on their behalf;

7. For a declaration that this is an exceptional case under 35 U.S.C. § 285 and for an award of attorneys' fees and costs in this action;

8. For an assessment of prejudgment interest; and

9. For such other and further relief as the Court may deem just and proper under the circumstances.

DATED: October 9, 2008

HENNIGAN BENNETT & DORMAN LLP

By _____
Lawrence M. Hadley
Omer Salik

Attorneys for Plaintiffs, MICROPROCESSOR ENHANCEMENT CORPORATION and MICHAEL H. BRANIGIN

DEMAND FOR JURY TRIAL

Plaintiffs hereby demand a jury trial pursuant to Rule 38 of the Federal Rules of Civil Procedure as to all issues in this lawsuit.

DATED: October 9, 2008

HENNIGAN BENNETT & DORMAN LLP

By _____
Lawrence M. Hadley
Omer Salik
Attorneys for Plaintiffs and Counterdefendants, MICROPROCESSOR ENHANCEMENT CORPORATION and MICHAEL H. BRANIGIN

EXHIBIT 1

US005471593A

United States Patent [19]

Branigin

[11] **Patent Number: 5,471,593**

[45] **Date of Patent: Nov. 28, 1995**

[54] **COMPUTER PROCESSOR WITH AN EFFICIENT MEANS OF EXECUTING MANY INSTRUCTIONS SIMULTANEOUSLY**

[76] Inventor: **Michael H. Branigin**, 151 Ivy Hills Rd., Southbury, Conn. 06488

[21] Appl. No.: **184,355**

[22] Filed: **Jan. 21, 1994**

Related U.S. Application Data

[63] Continuation of Ser. No. 448,720, Dec. 11, 1989, abandoned.

[51] **Int. Cl.**[6] **G06F 9/38**

[52] **U.S. Cl.** **395/375**; 364/231.8; 364/261.3; 364/261.4; 364/261.5; 364/DIG. 1

[58] **Field of Search** 395/375

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Primary Examiner—Parshotam S. Lall
Assistant Examiner—Ayni Mohamed

[57] **ABSTRACT**

To increase the performance of a pipelined processor executing instructions, conditional instruction execution issues and executes instructions, including but not limited to branches, before the controlling conditions may be available and makes the decision to update the destination as late as possible in the pipeline. Conditional instruction execution is further improved by a condition code mask field in instructions to choose those condition code bits to be involved in the decision; by a set condition code flag to enable or disable the setting of a condition code; by stale condition code handling to determine if the logically previous conditionally executing instruction was successful or unsuccessful in setting the condition code and to conditionally execute accordingly; by multiple condition codes so that independent instruction sequences can use condition codes in parallel; and by condition code reservation stations to capture a needed condition code as soon as it becomes available and hold that captured value until needed, thus freeing the condition code as soon as possible for use by other instructions. Moving the conditional decision from the point of instruction issue to the point of instruction completion permits branch instructions to be eliminated in many cases; permits conditionally executing instructions directly in line; permits filling the branch umbra following a delayed branch with conditionally executing instructions; and reduces the latency from condition code generation to condition code use.

12 Claims, 62 Drawing Sheets

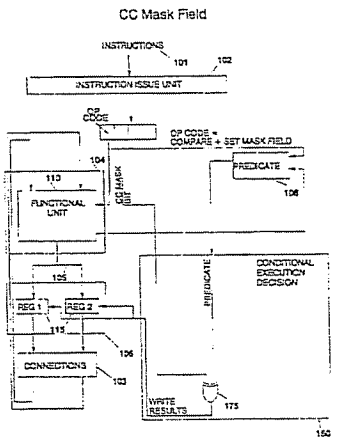

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Figure 1.
PERFORMANCE CAPACITY, THE GOAL

Perf = N•I•C

Perf = Performance Capacity,
OPERATIONS/SECOND

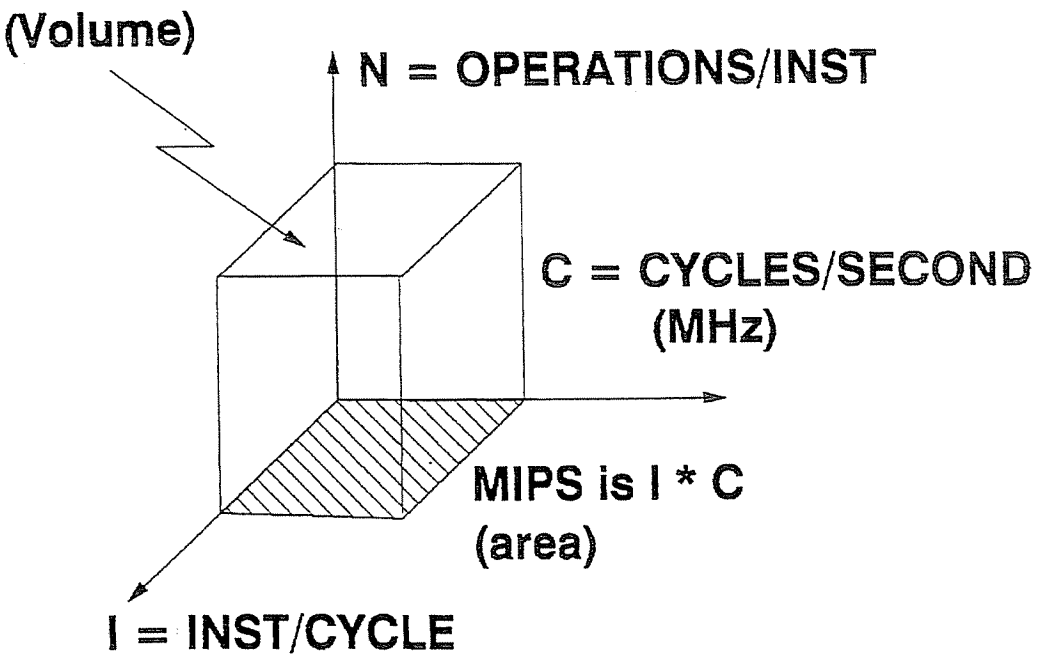


Figure 2. Prior Art
BASIC MULTI-FUNCTIONAL UNIT PROCESSOR

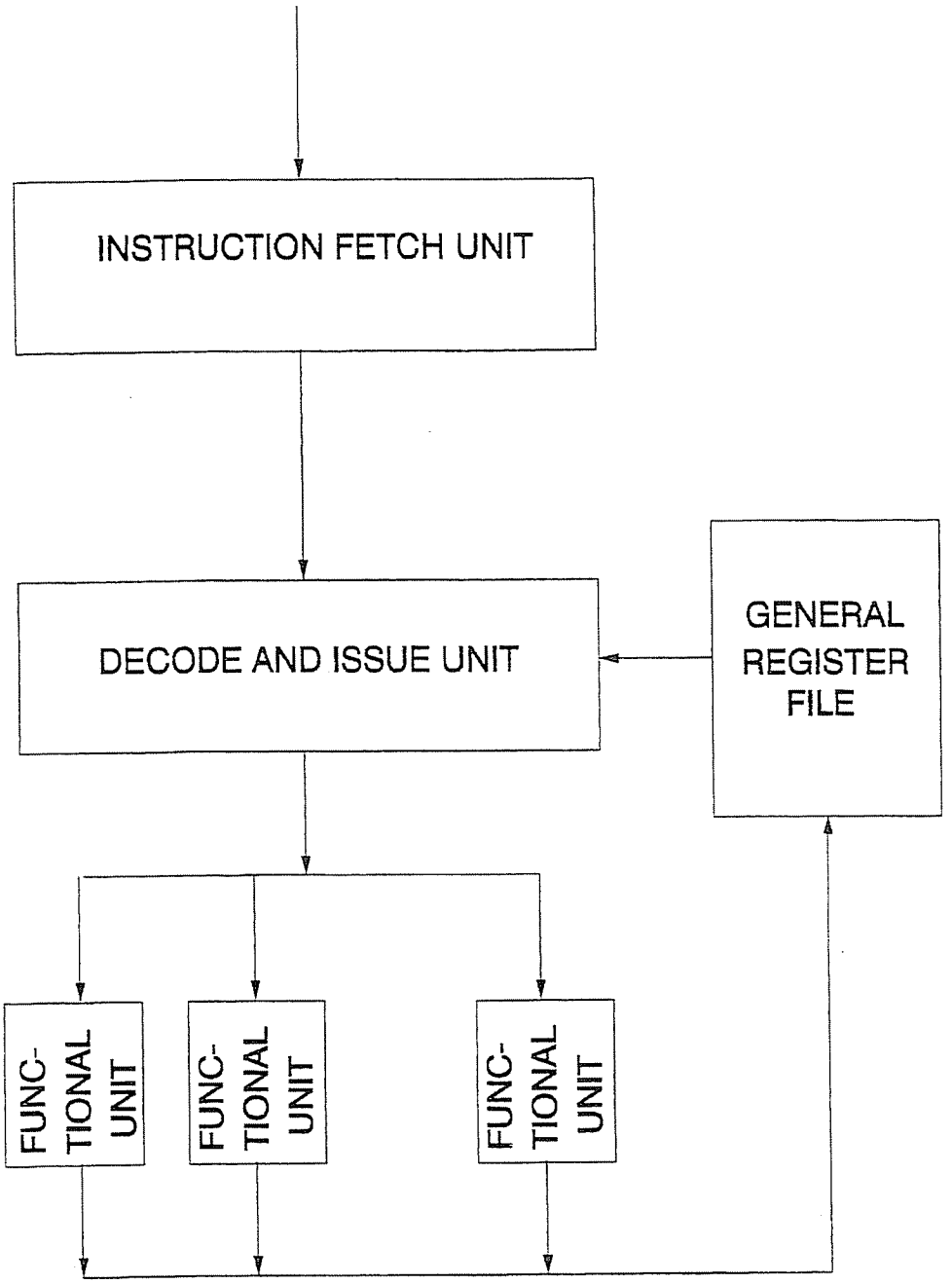


Figure 3. Prior Art,
WISQ PROCESSOR ARCHITECTURE

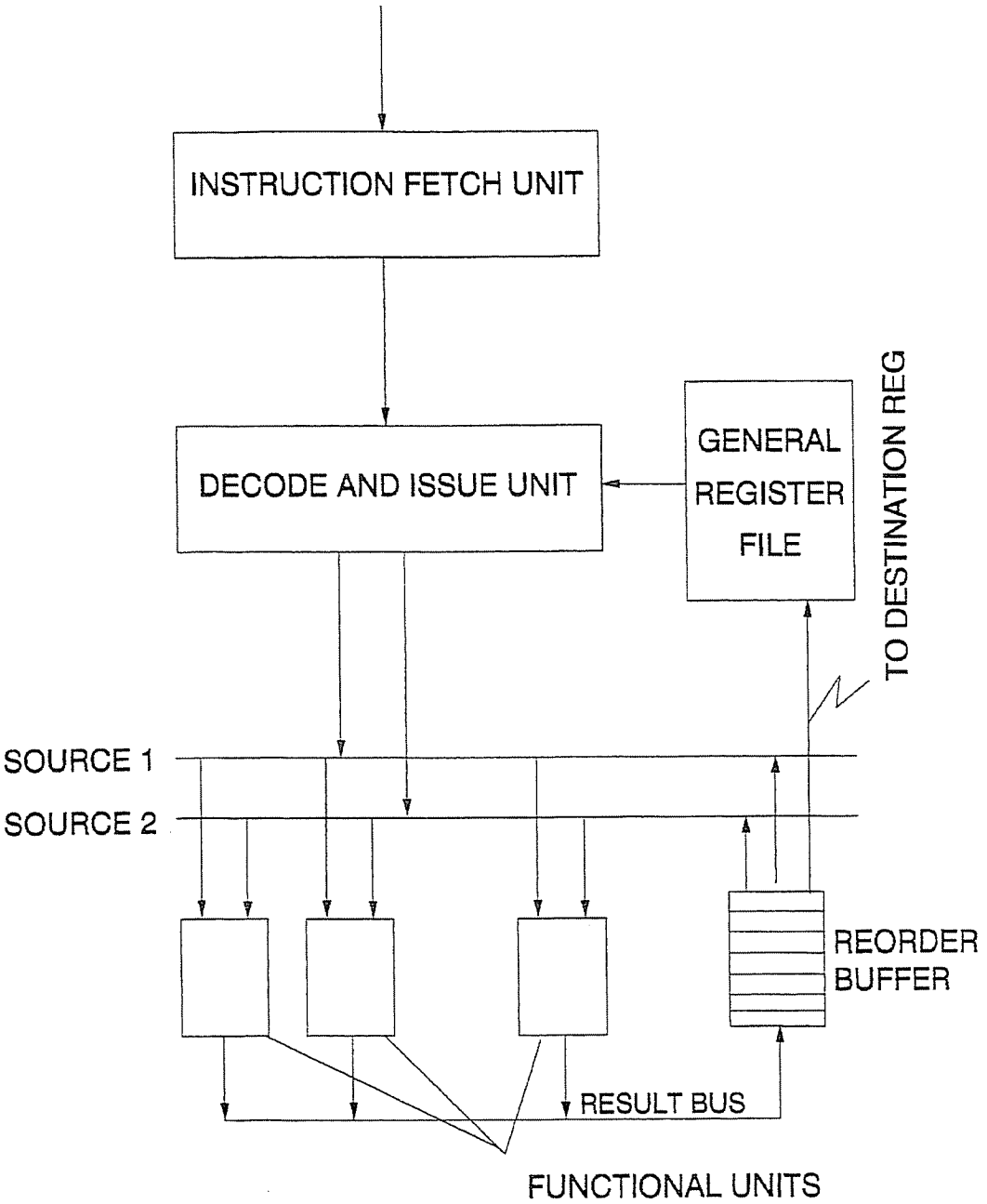


Figure 4. Prior Art,
PROCESSOR WITH SCOREBOARDING

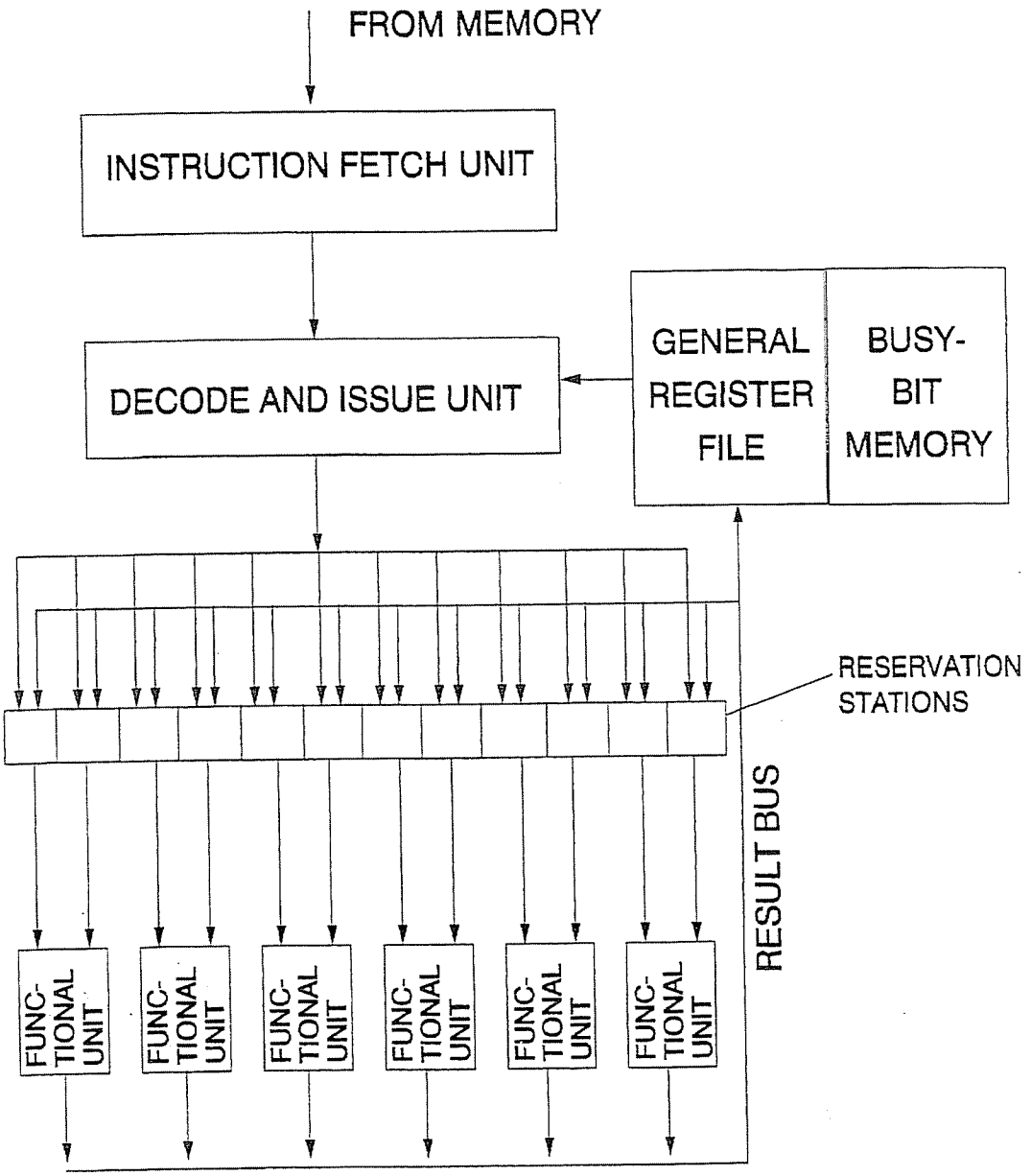


Figure 5. Prior Art

PROCESSOR WITH TOMASULO'S ALGORITHM

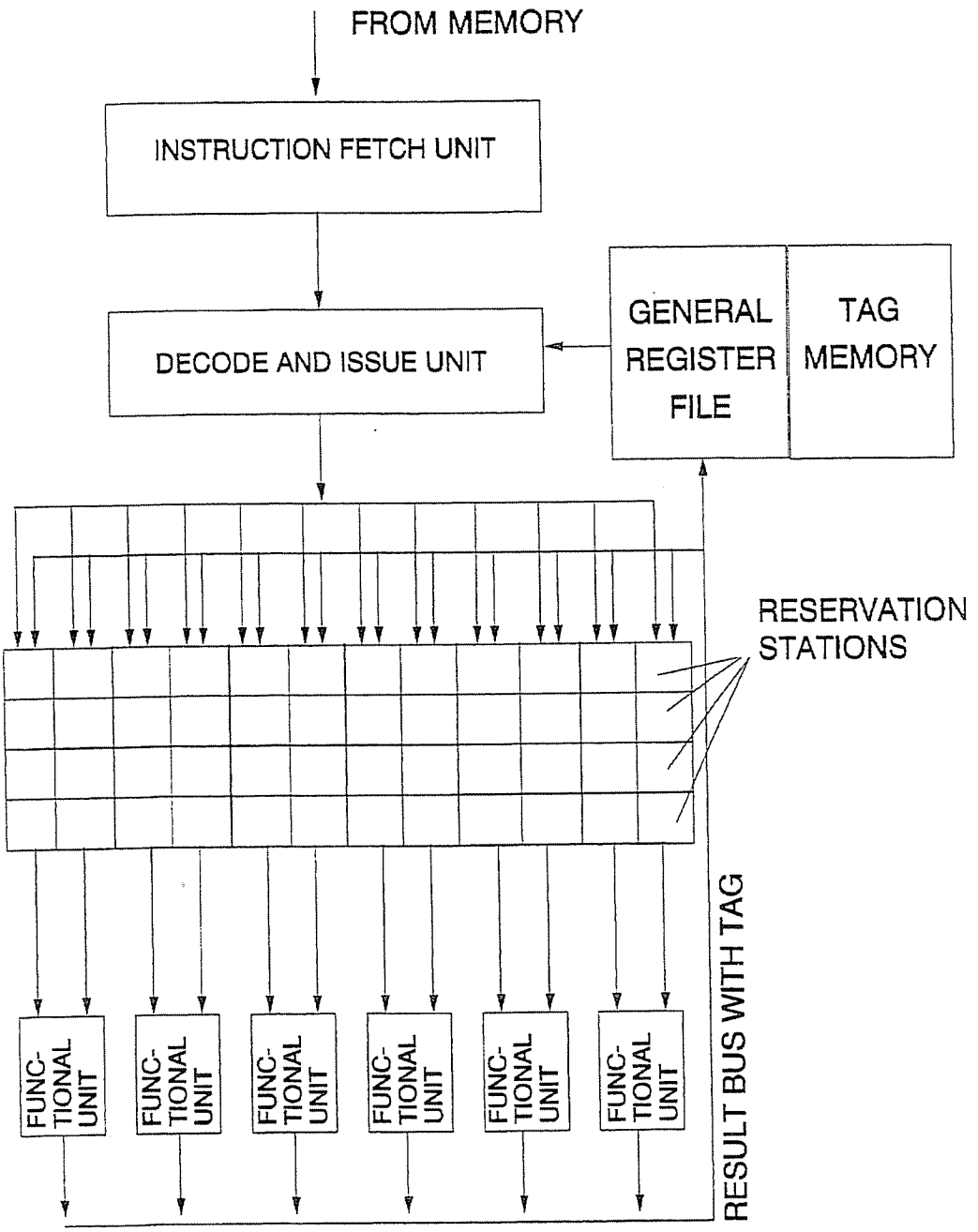


Figure 6a. Prior Art,
CENTRAL REGISTER VLIW PROCESSOR

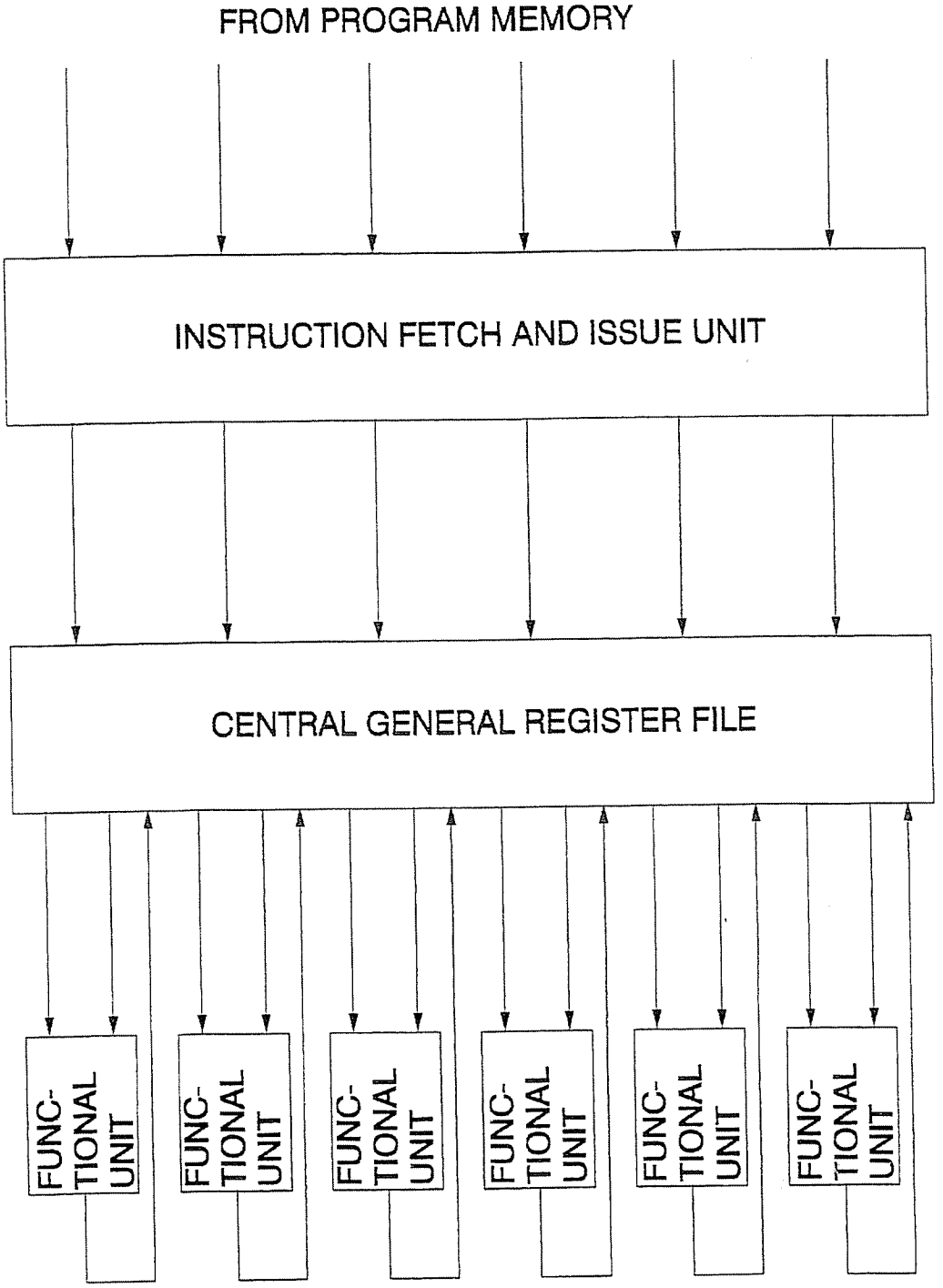


Figure 6b. Prior Art,
CENTRAL REGISTER VLIW PROCESSOR

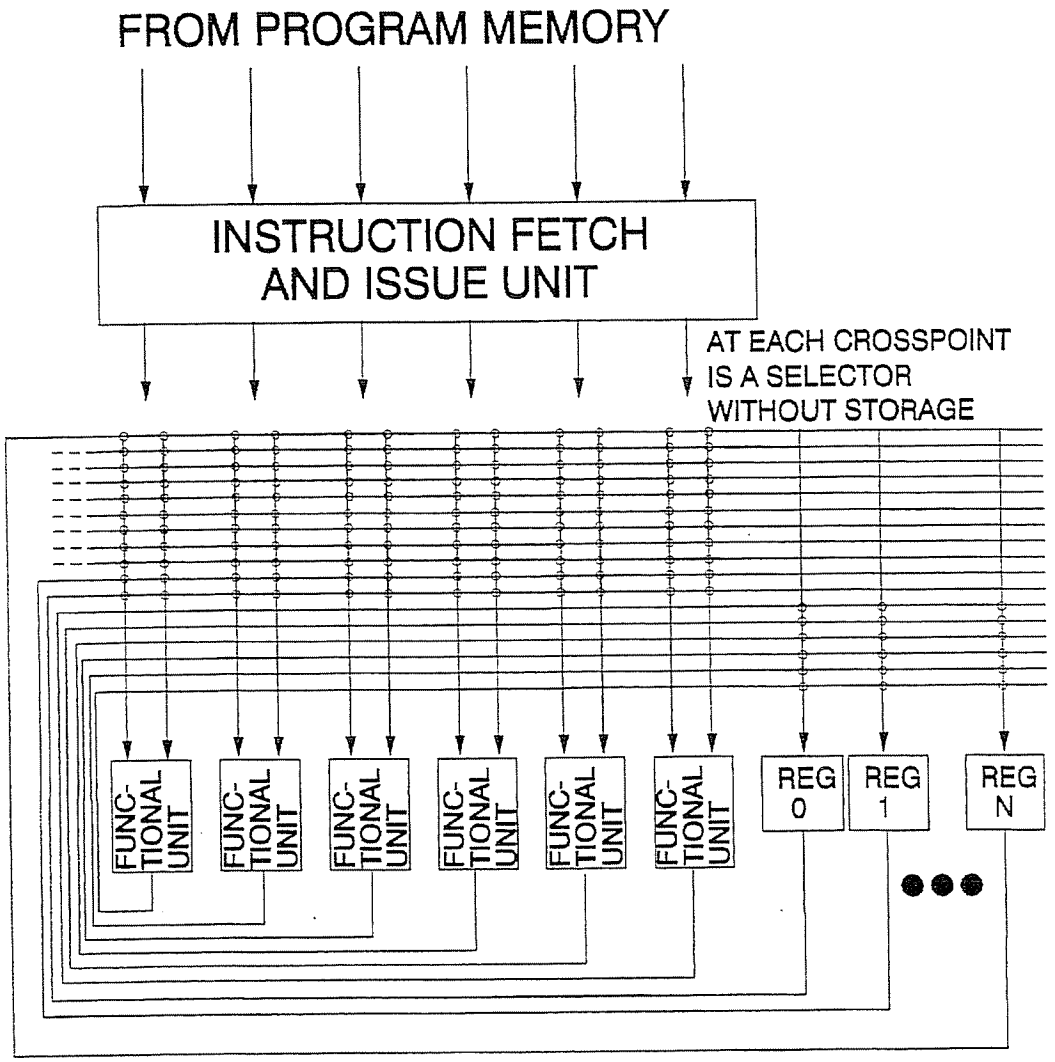


Figure 7. Prior Art,
CROSSBAR NETWORK PROCESSOR

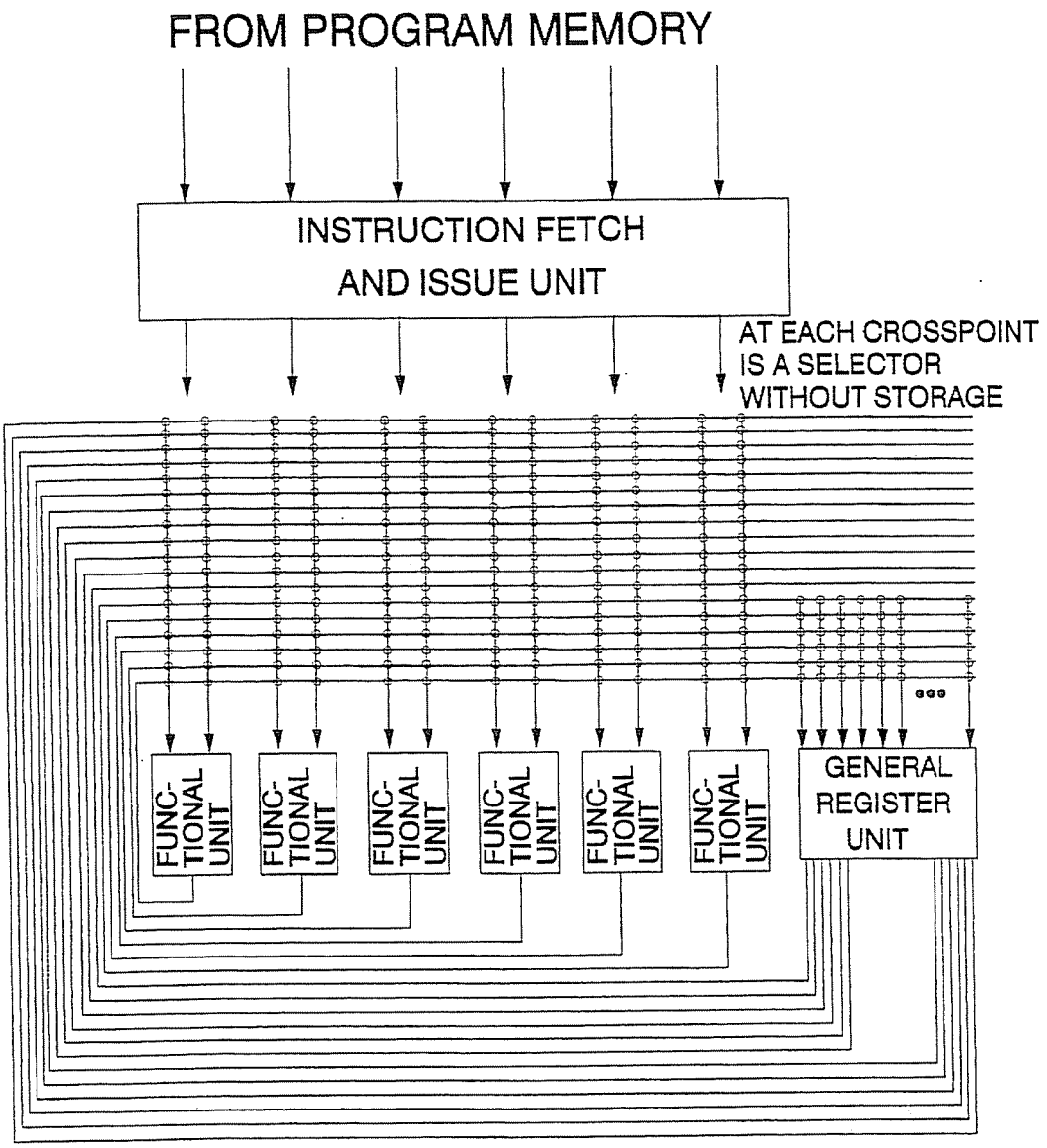


Figure 8a. Prior Art,
REGISTERED CROSSBAR NETWORK PROCESSOR

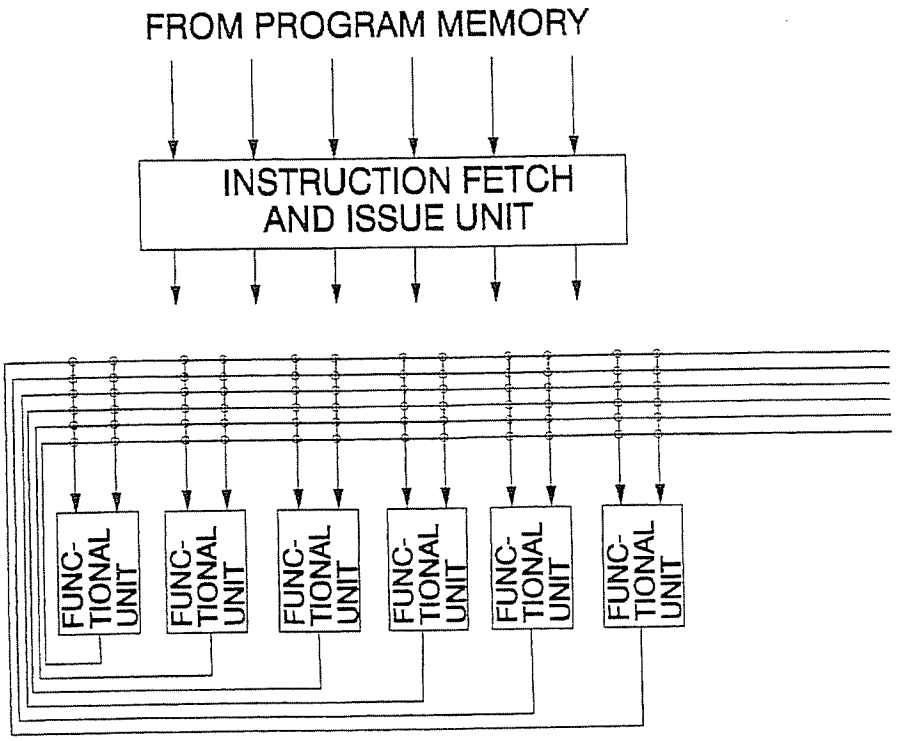


Figure 8b. Prior Art,
EACH CROSSPOINT OF A
REGISTERED CROSSBAR NETWORK PROCESSOR

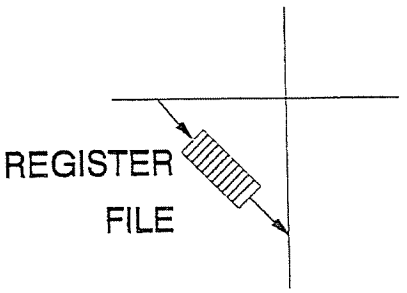


Figure 9a. Prior Art,
PROCESSOR WITH REGISTER UPDATE UNIT

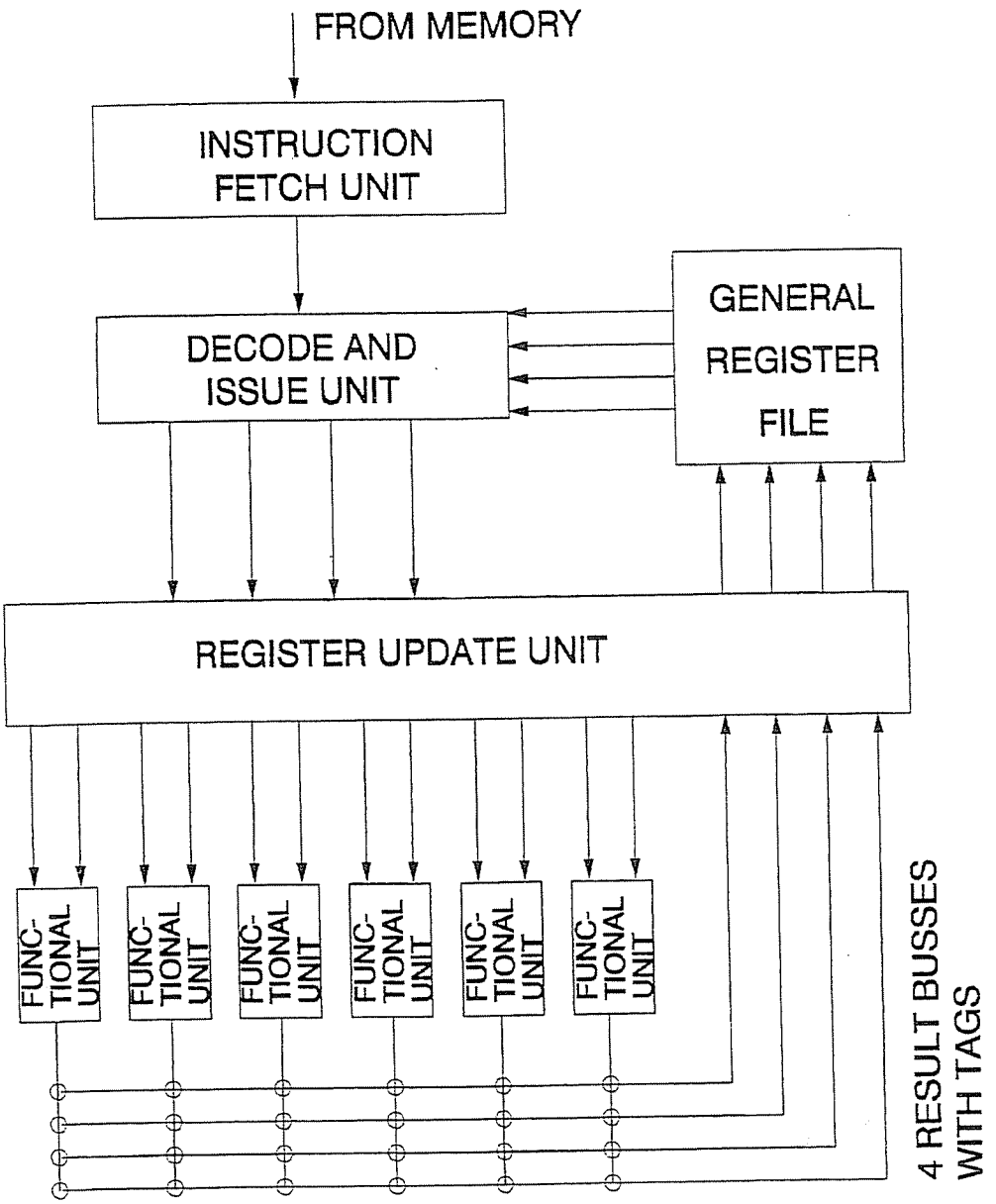


Figure 9b. Prior Art,
Processor with Register Update Unit

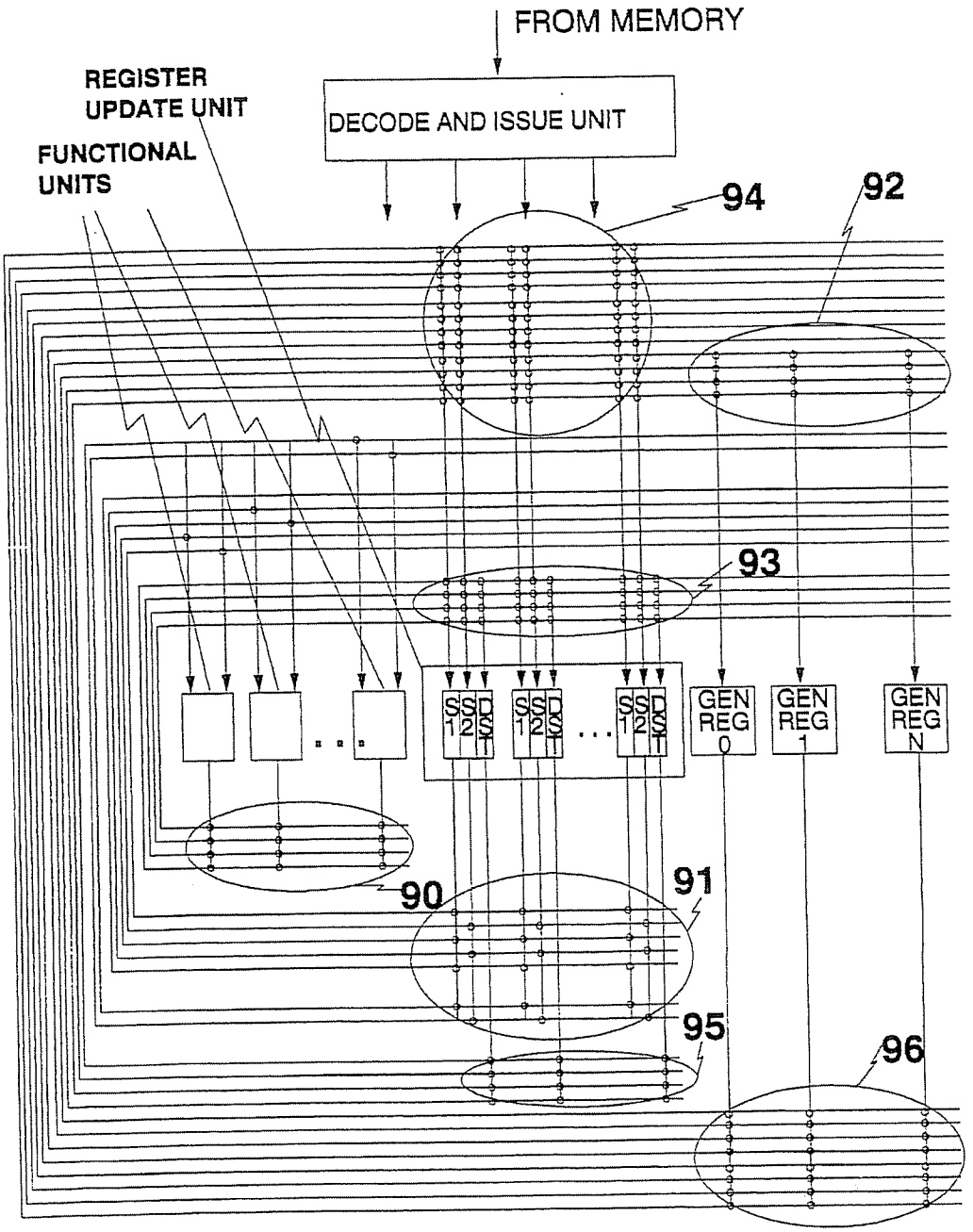


Figure 10a. Prior Art
Data Synchronized Pipelined Architecture

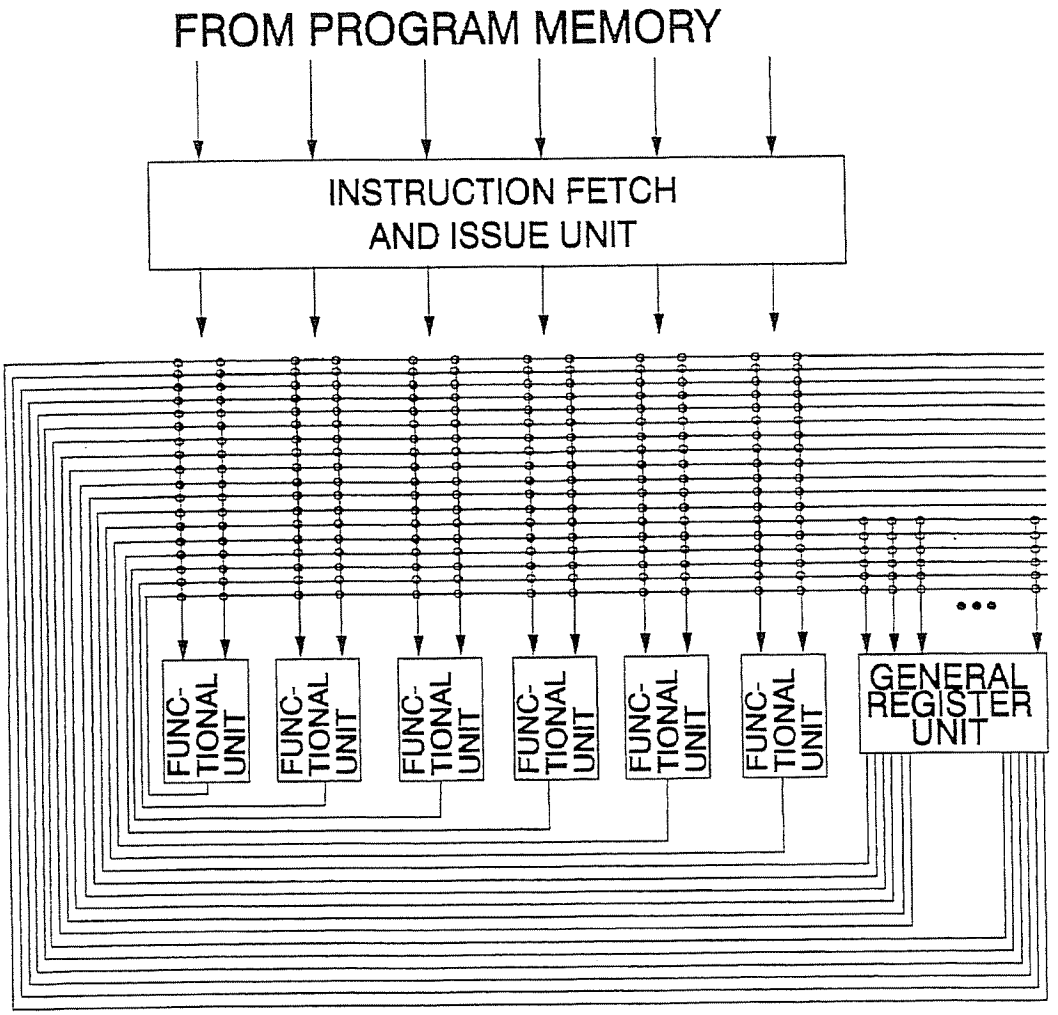


Figure 10b. Prior Art
Each Crosspoint of Figure 10a

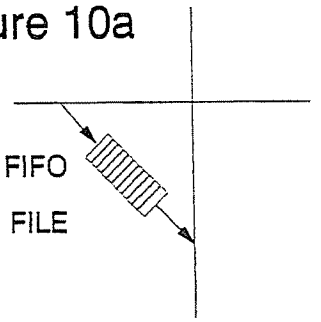


Figure 11a. Prior Art,
QVC Processor Architecture

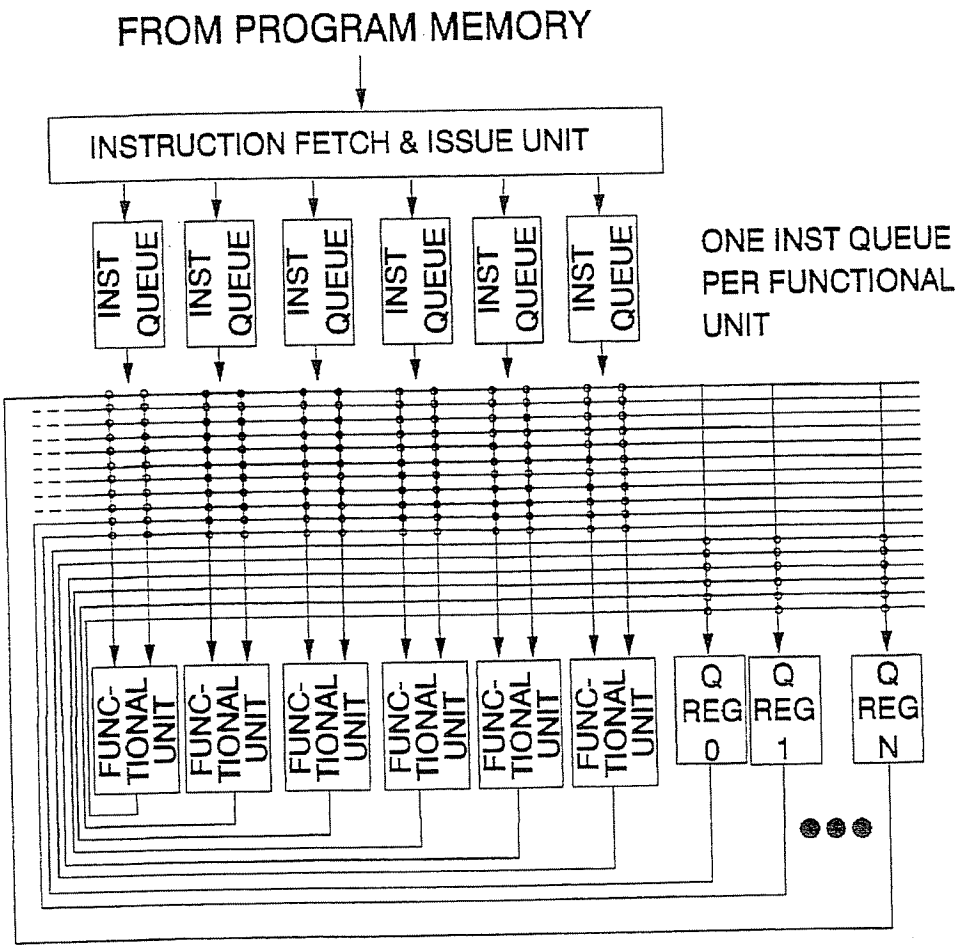


Figure 11b. Prior Art,
Queue Register of Figure 11a

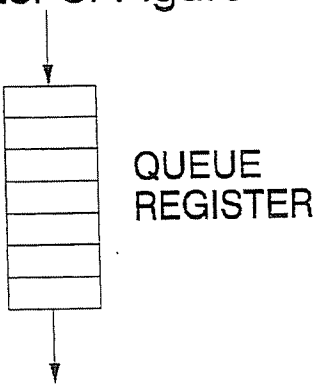
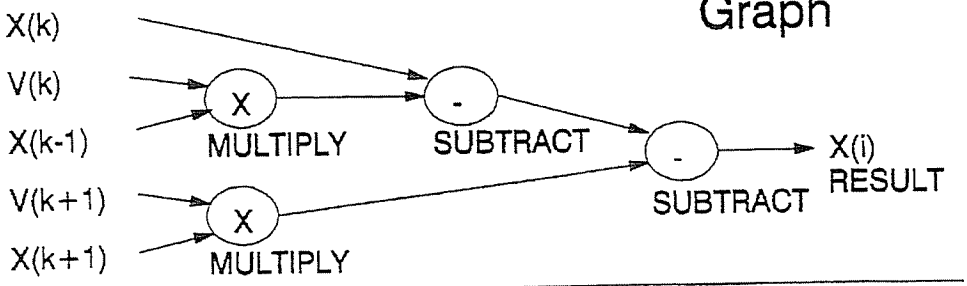


Figure 12. Prior Art,
Mapping to Systolic Pipeline

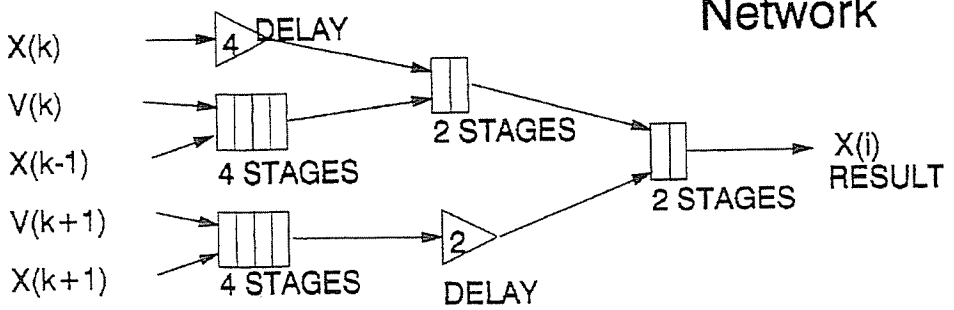
Program

```
DO 10  k = 1, Loop, 2
       X(i) = X(k) - V(k)*X(k-1) - V(k+1)*X(k+1)
         i = i + 1
10 CONTINUE
```

Program Graph



Systolic Pipeline Network



Network Implementation

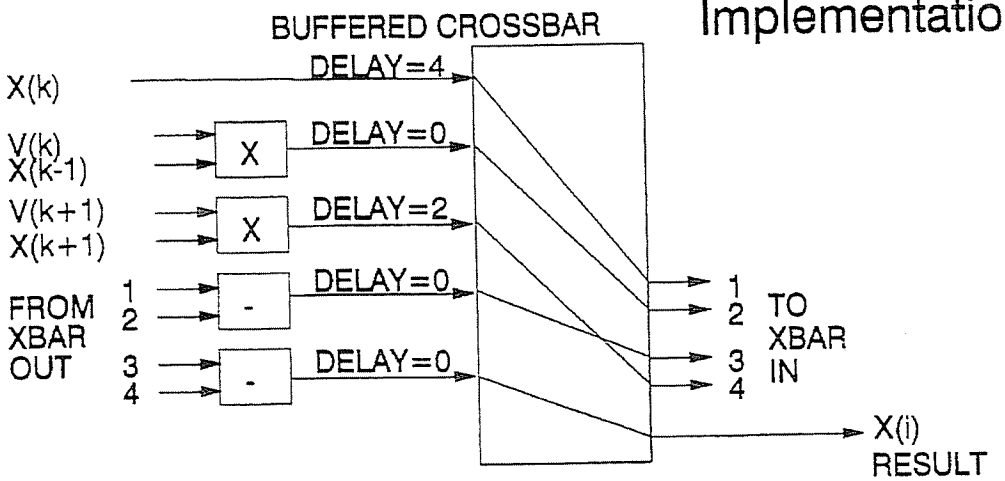


Figure 13a. Invention,
Dedicated Result Storage

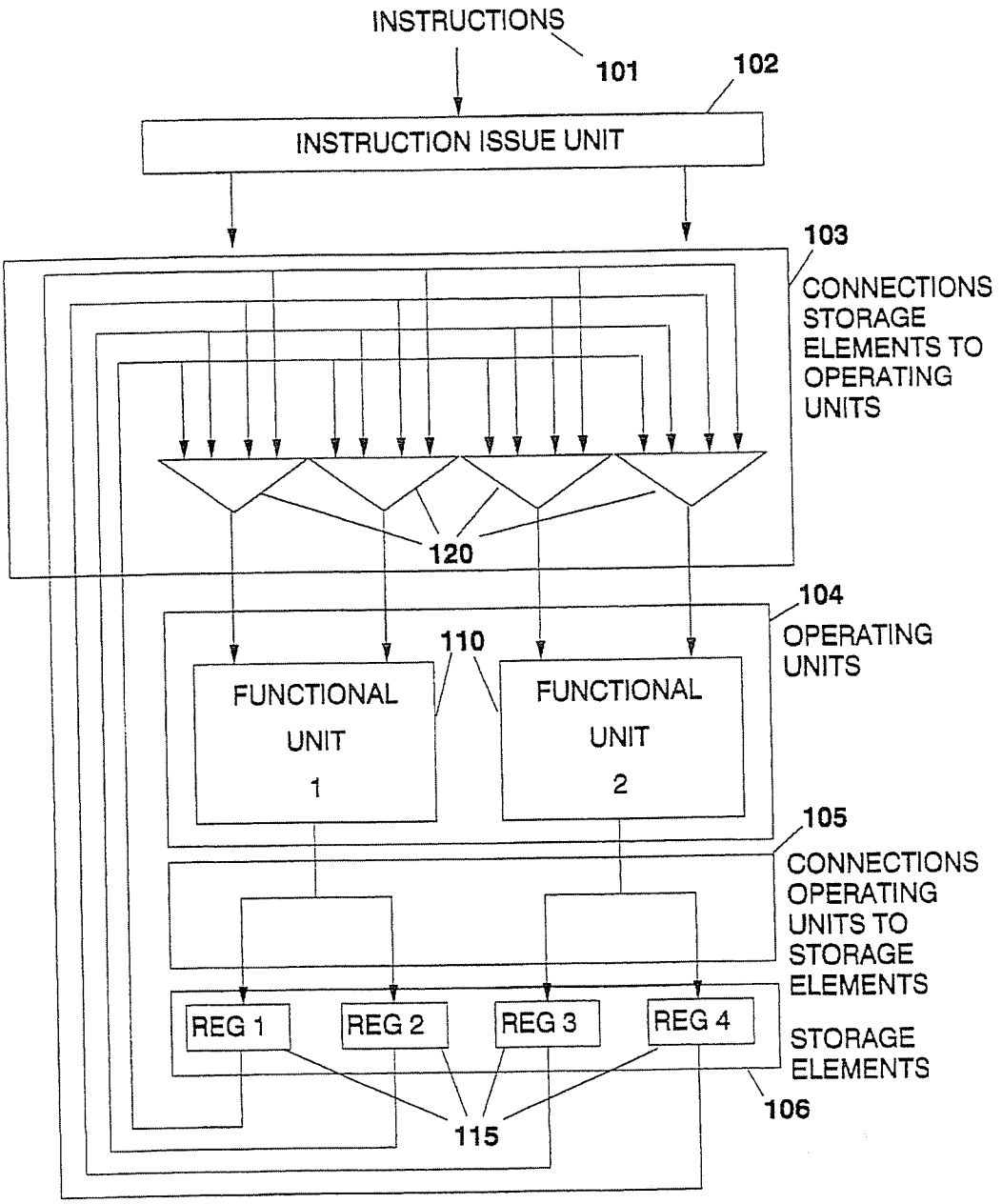


Figure 13b. Invention,
Storage Copy Selection

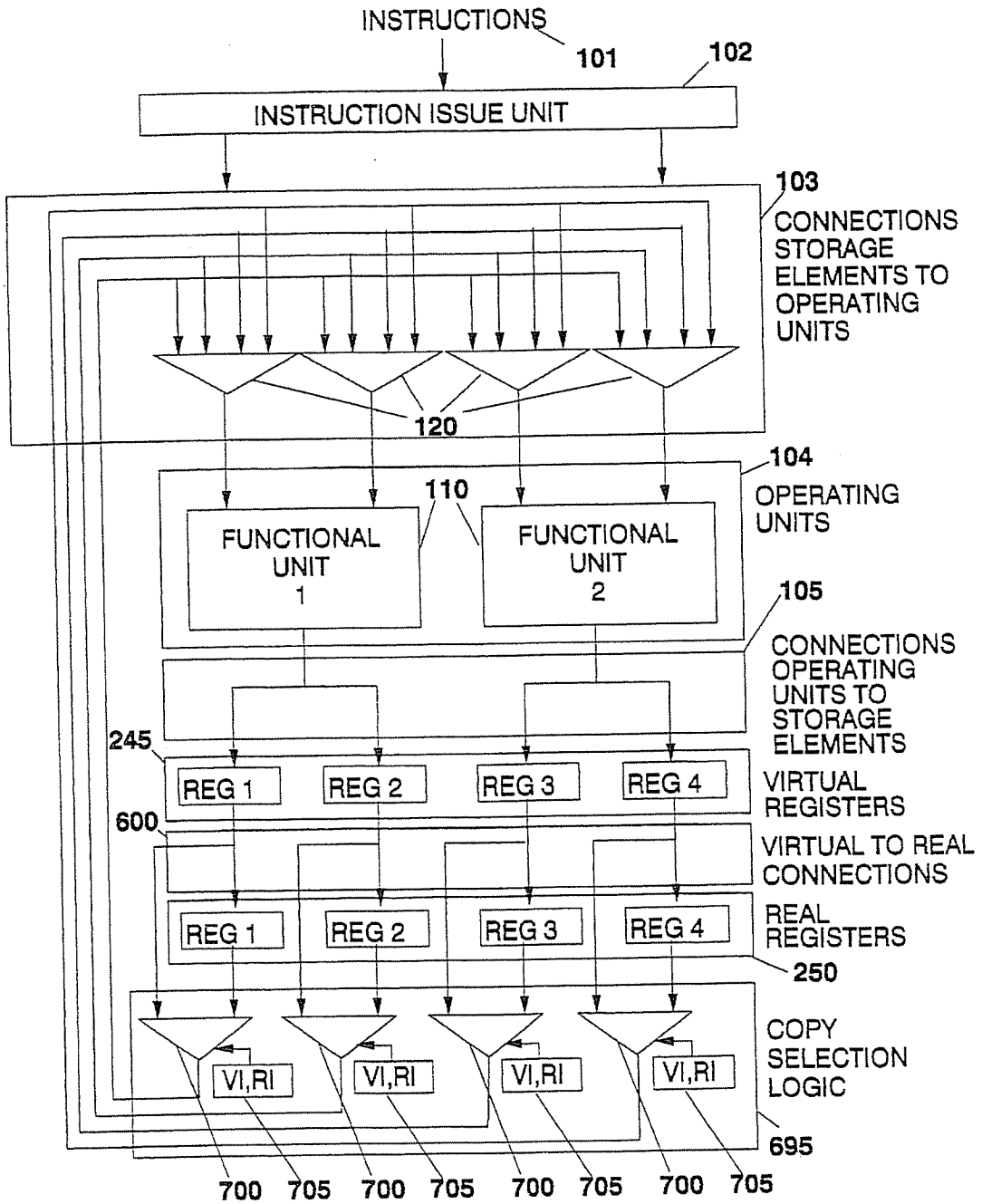


Figure 13c. Invention,
Reservation Station Scheduling

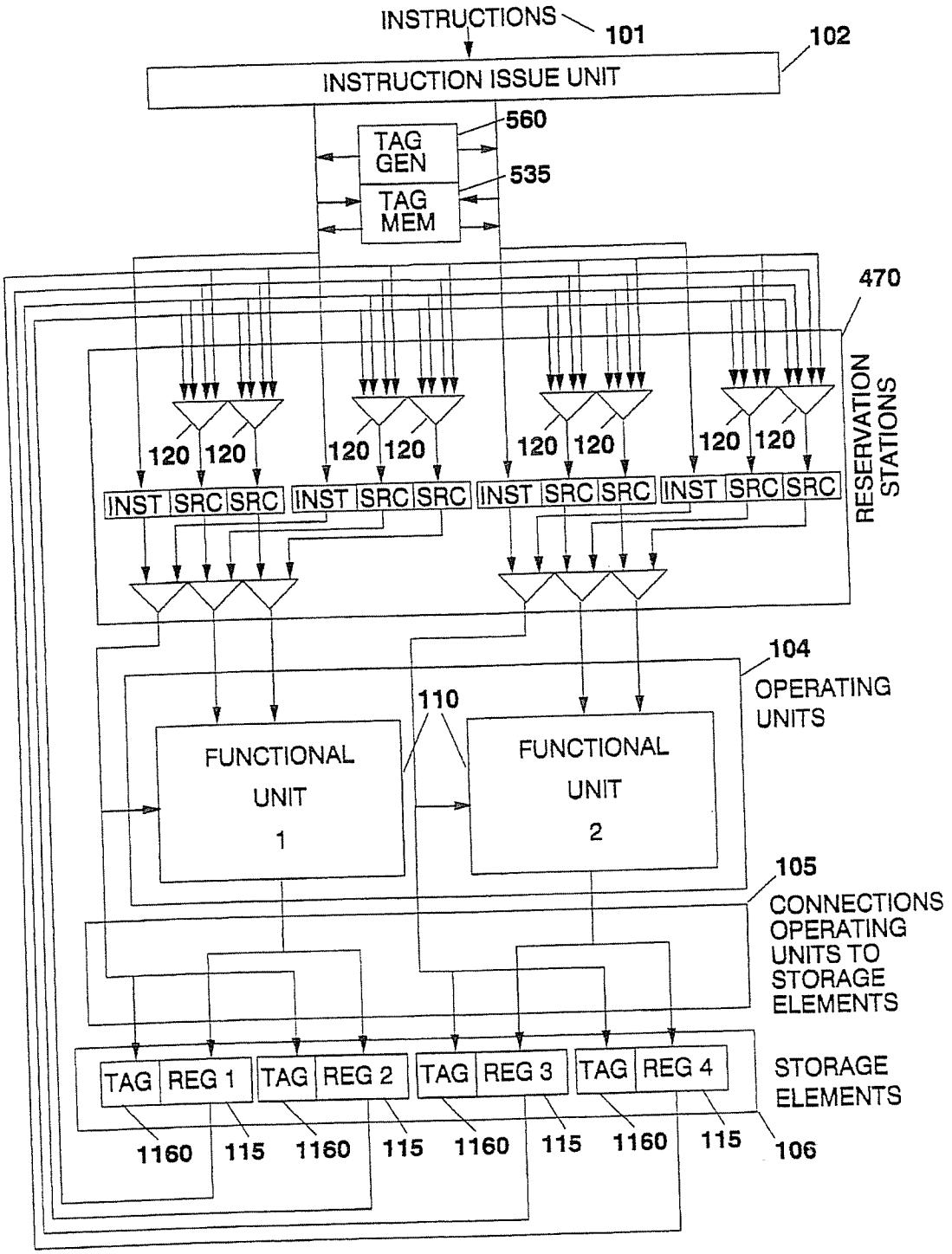


Figure 14a. Invention,
Folded Connections

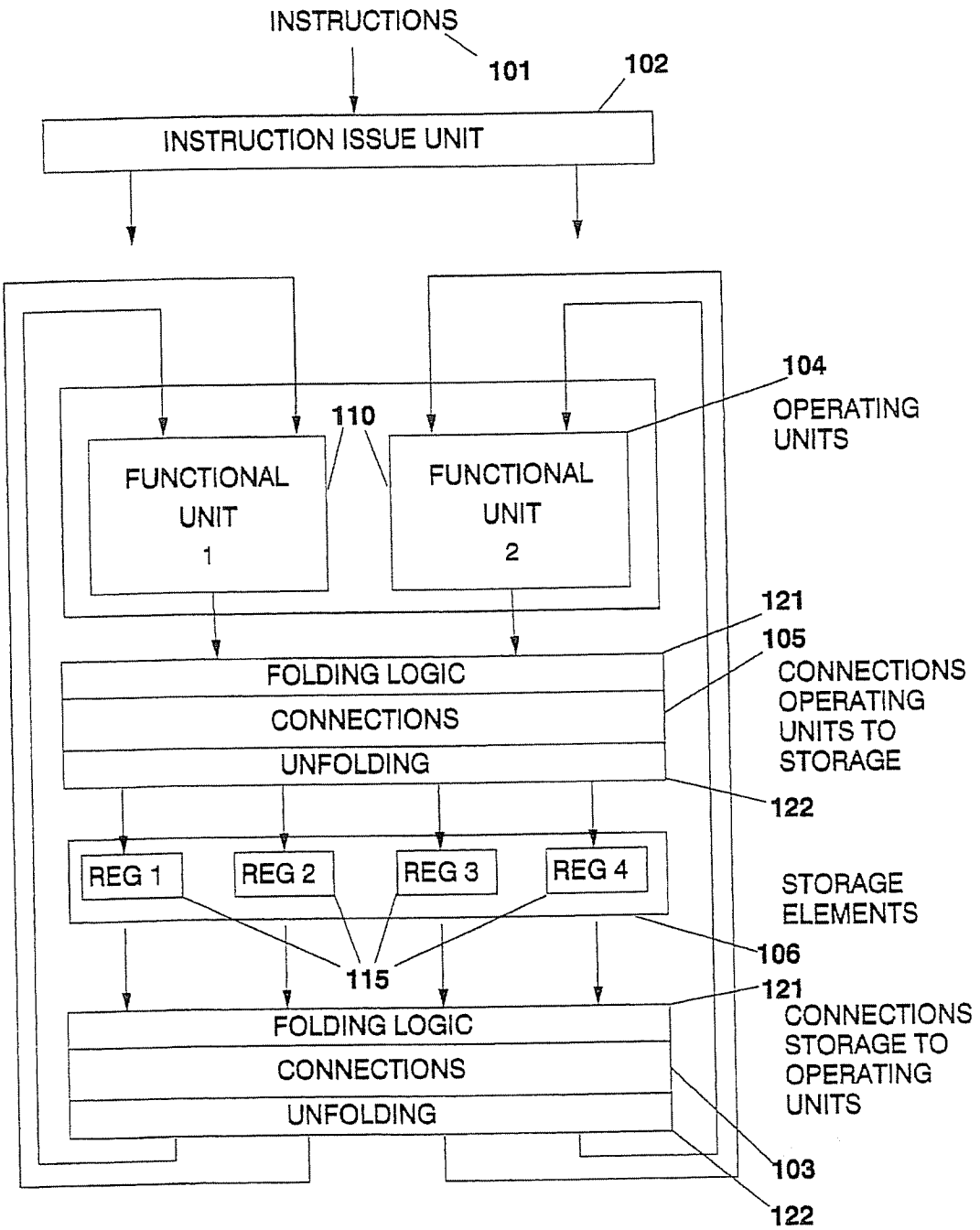


Figure 14b. Invention,
FOLDED CONNECTIONS DETAILS

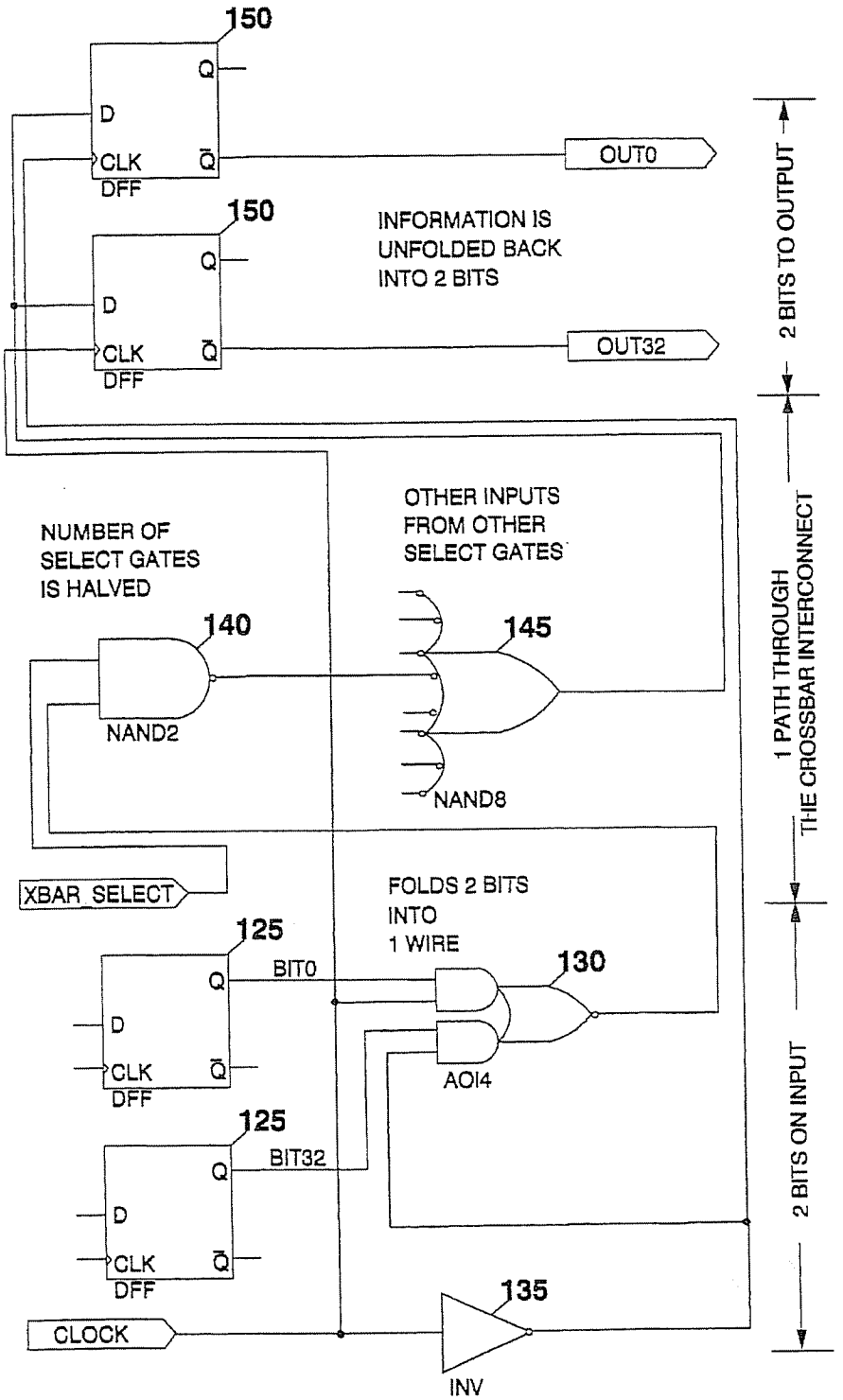


Figure 15a. Invention, Conditional Execution

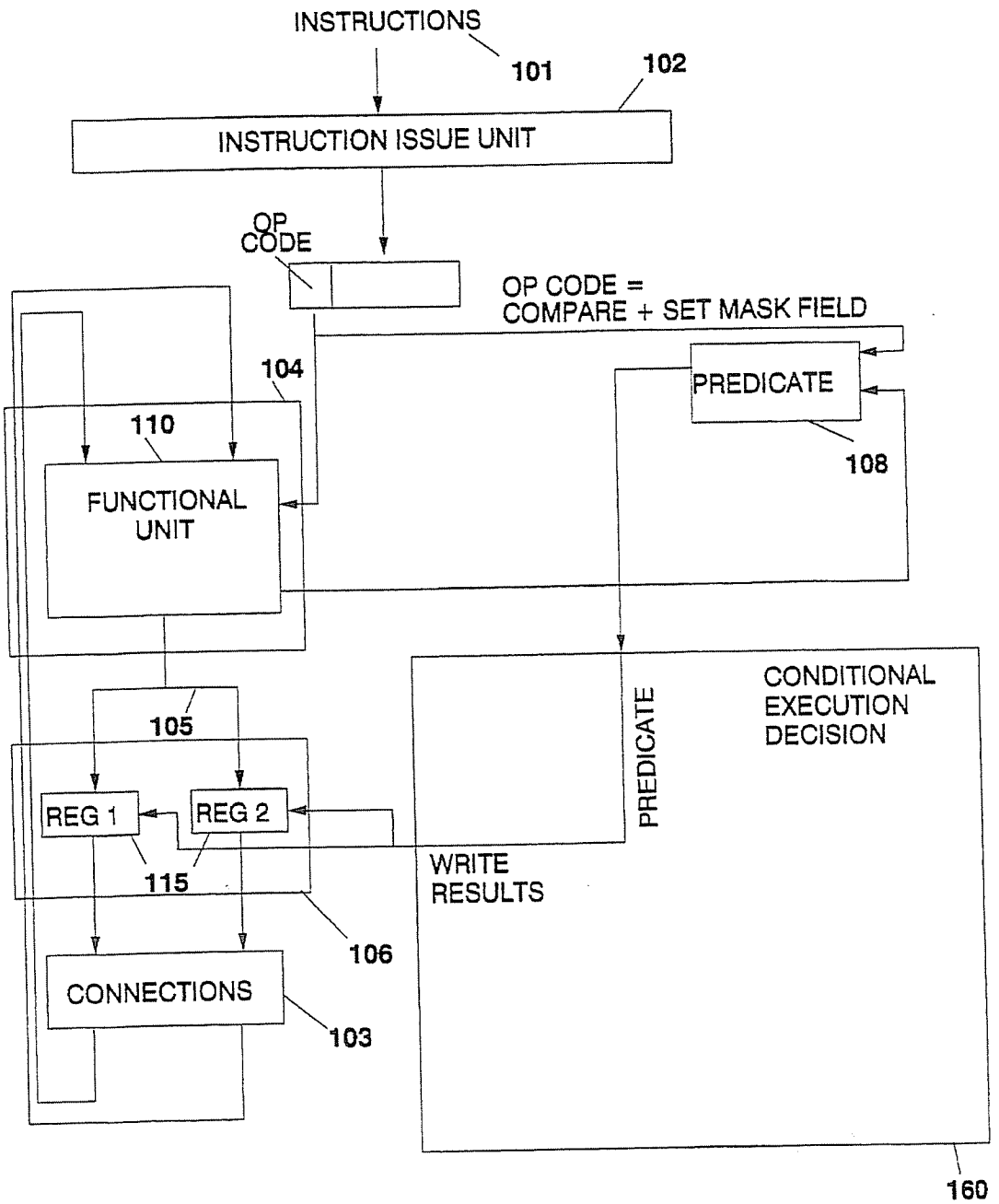


Figure 15b. Invention,
CC Mask Field

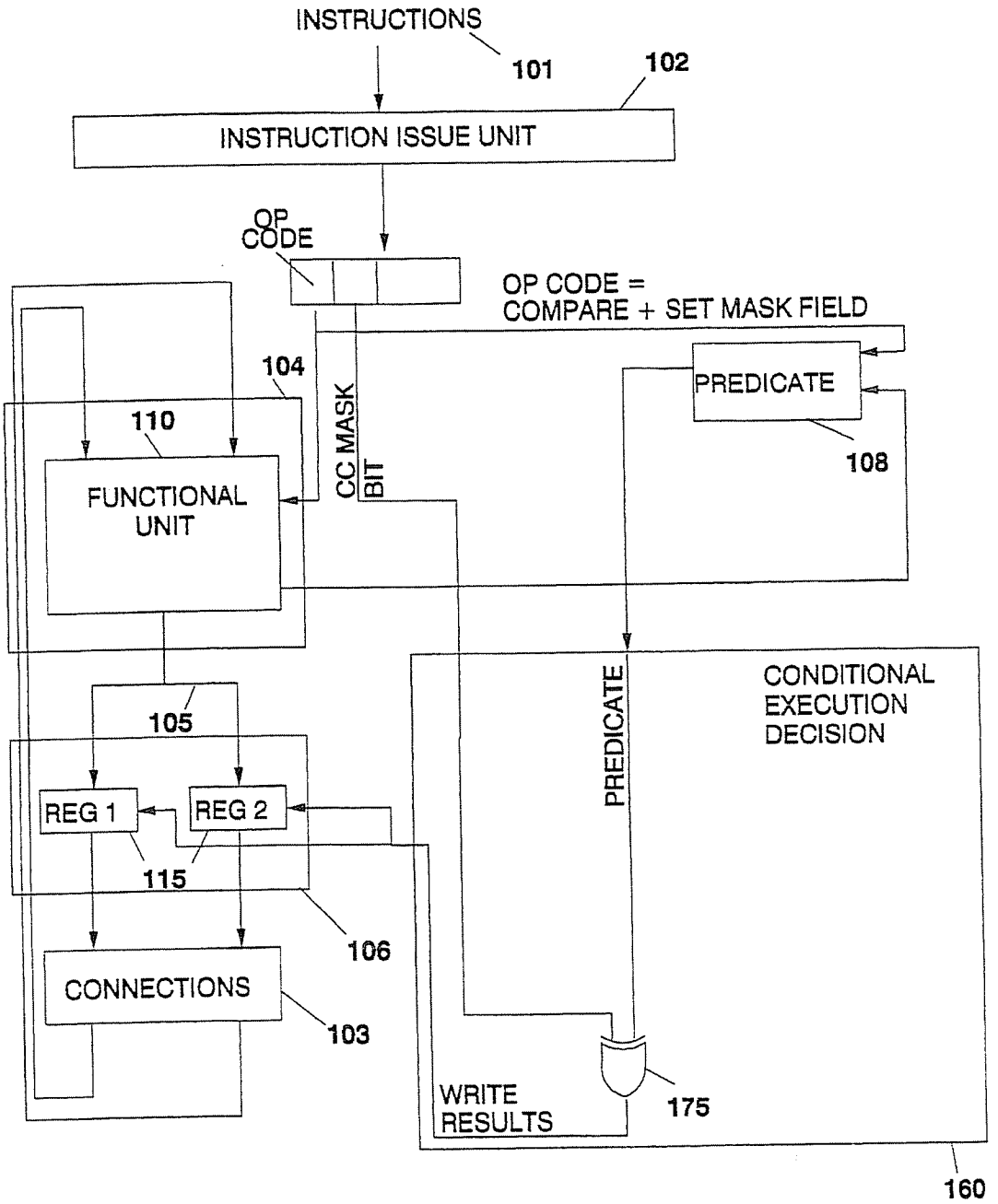


Figure 15c. Invention,
Set CC Field

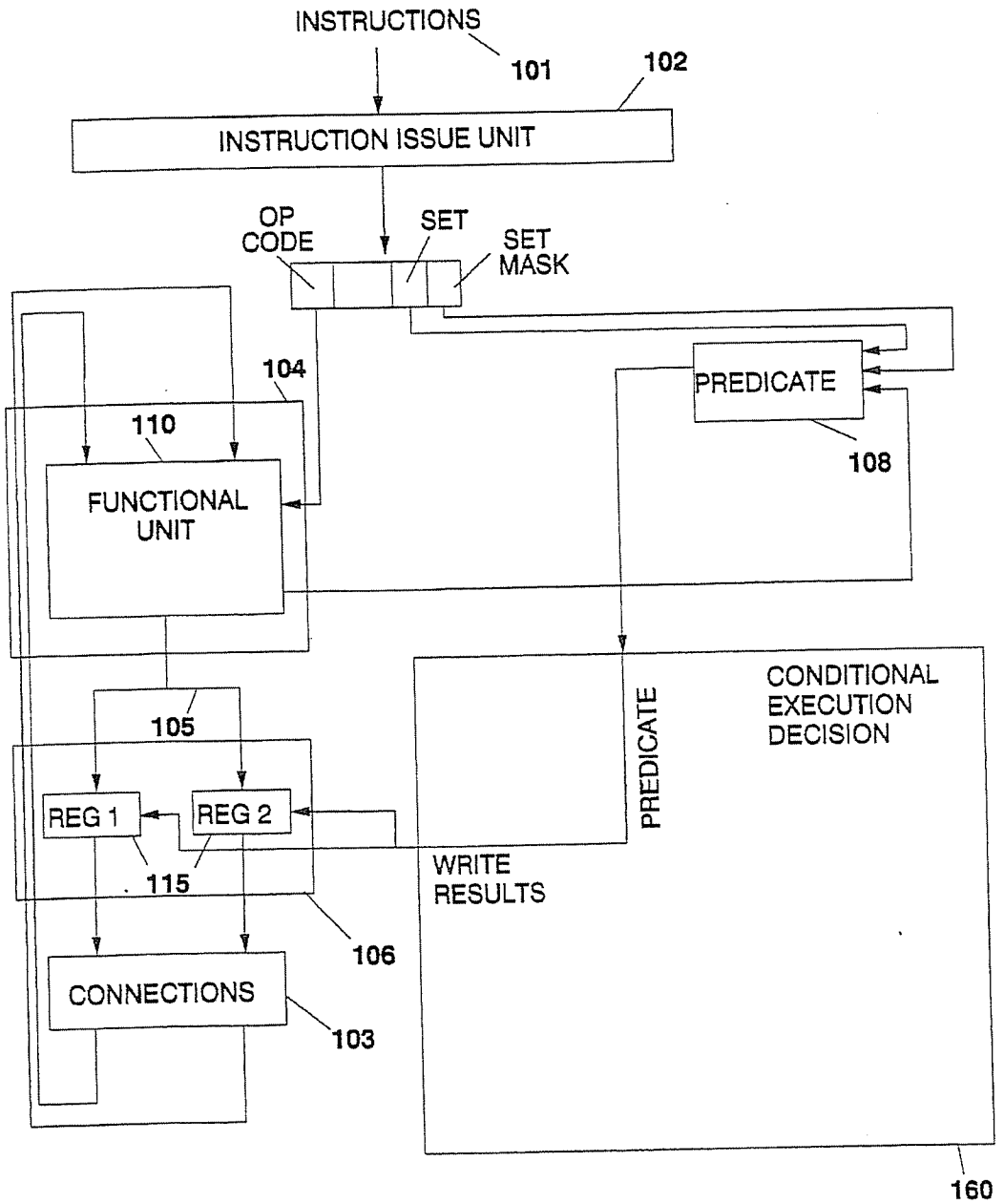


Figure 15d. Invention,
Conditional Execution with
CC Mask Field & Set CC Field

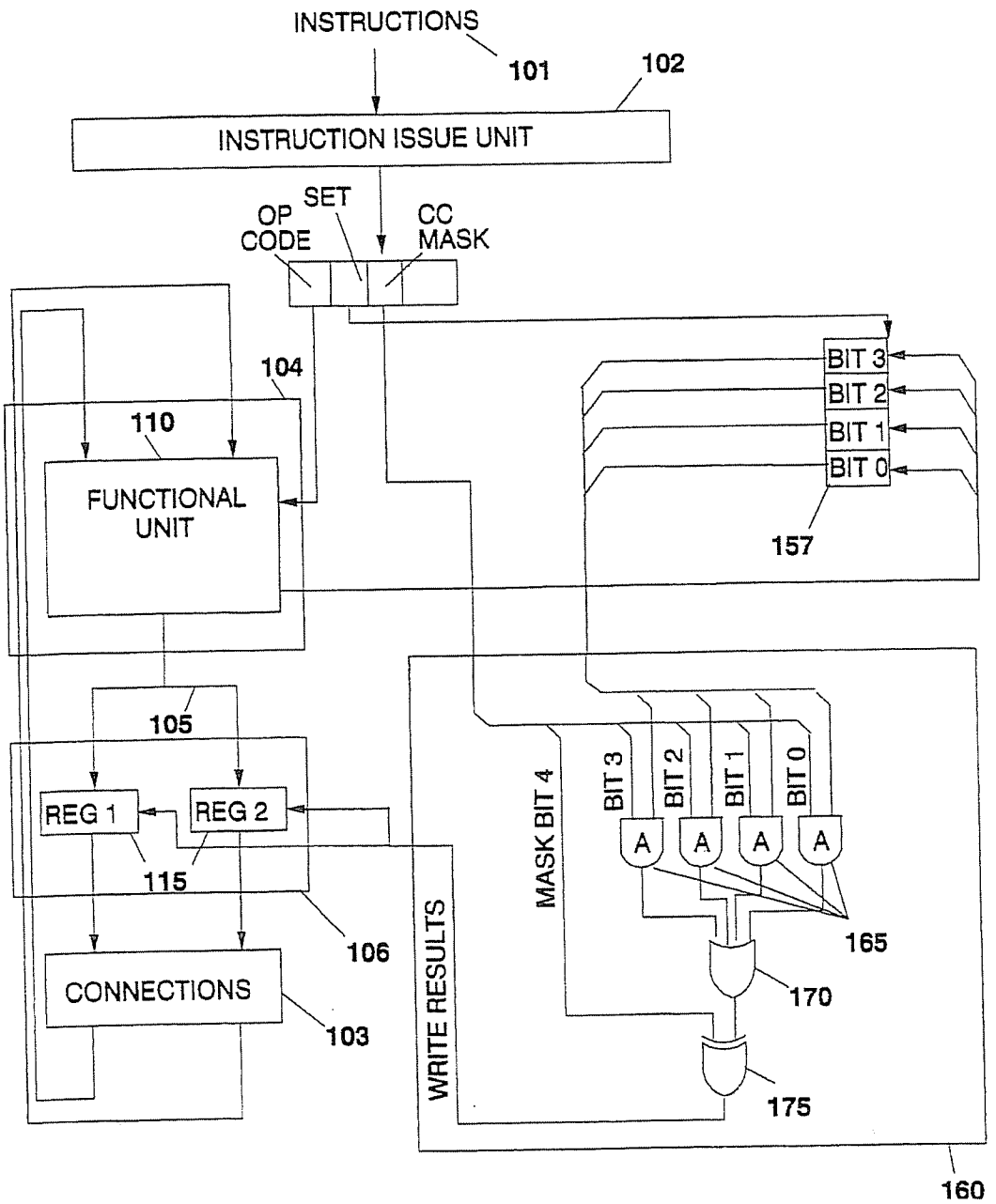


Figure 15e. Invention,
Stale Condition Code Handling

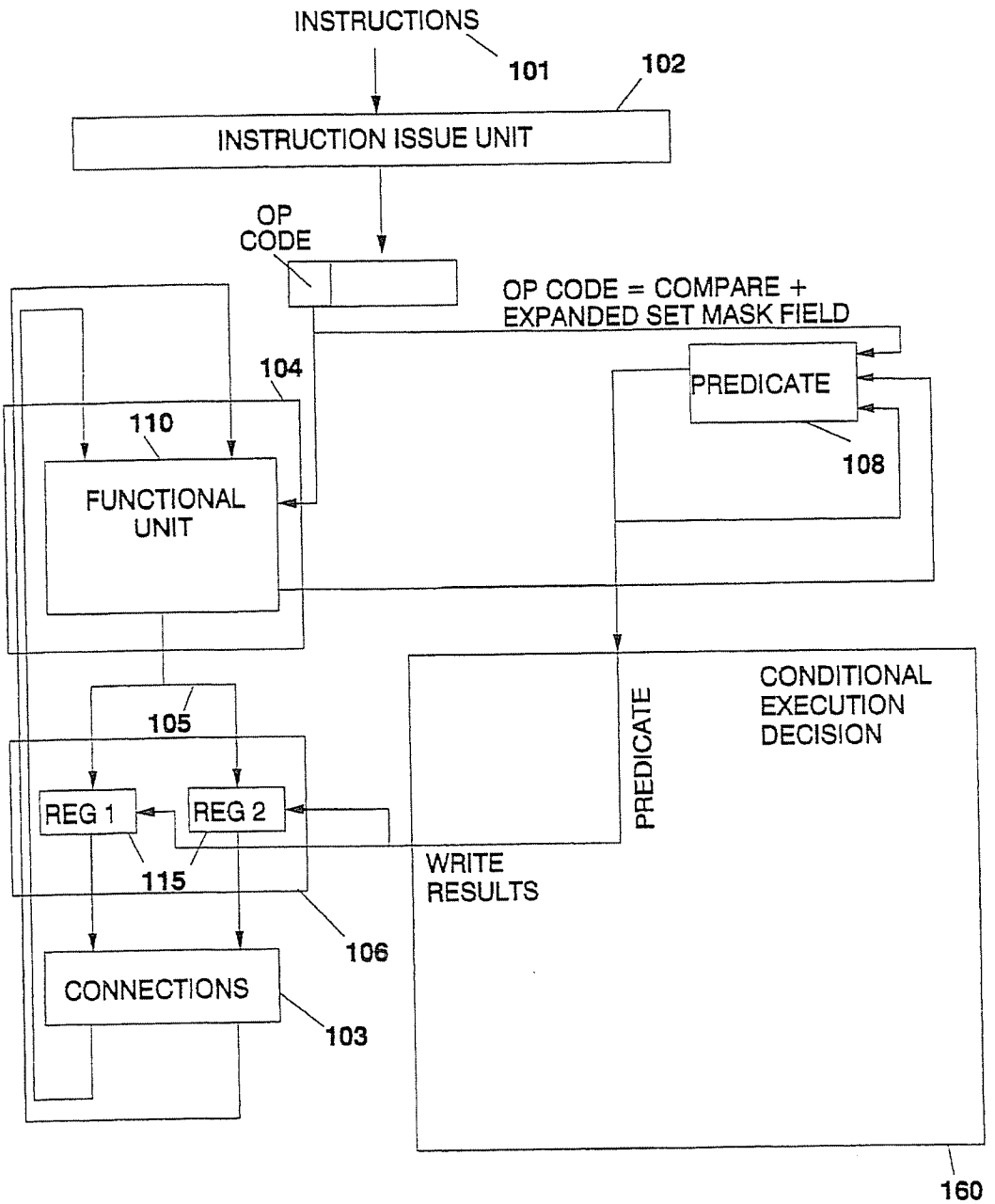


Figure 15f. Invention, Multiple CCs

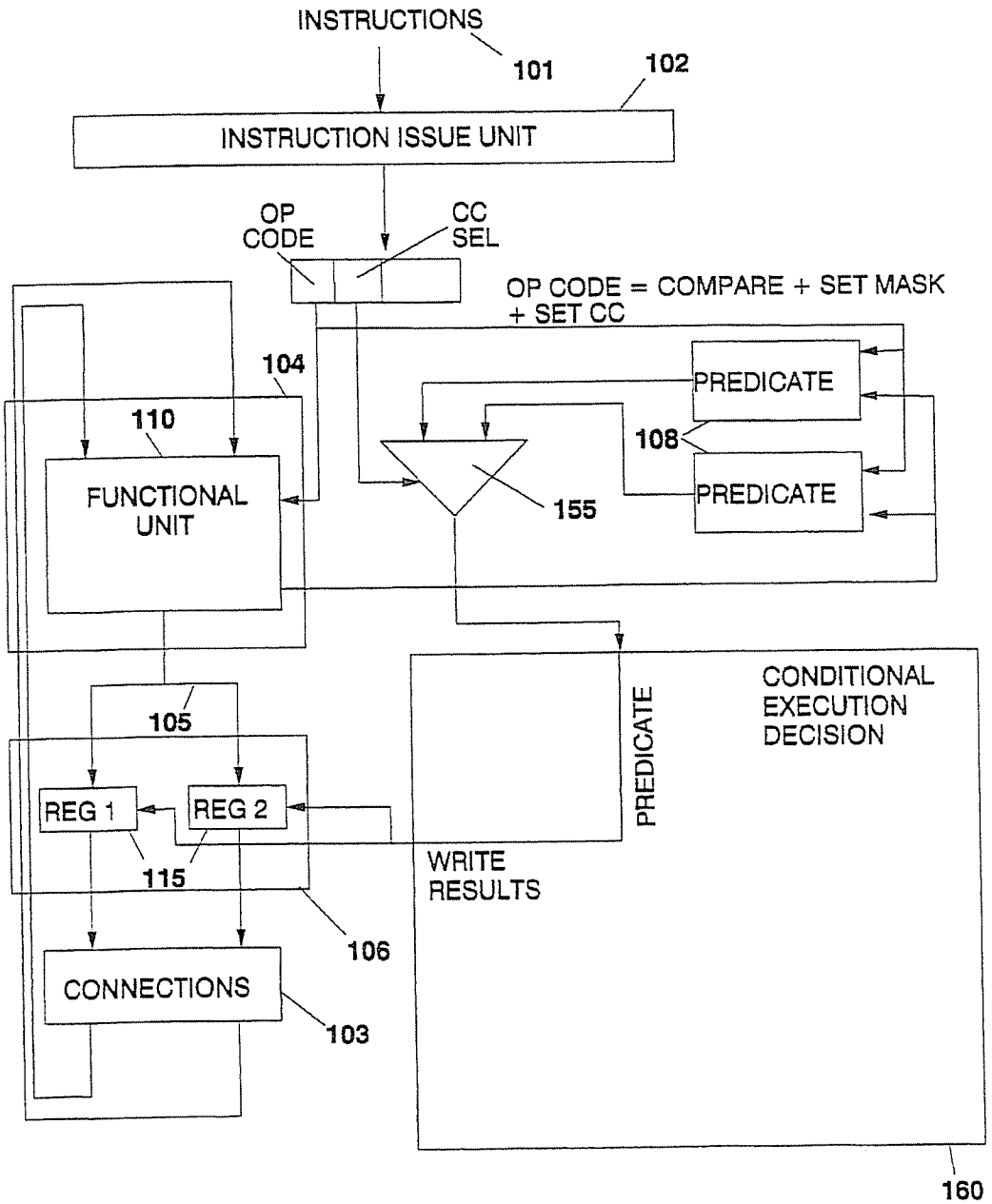


Figure 15g. Invention,
CC Reservation Stations

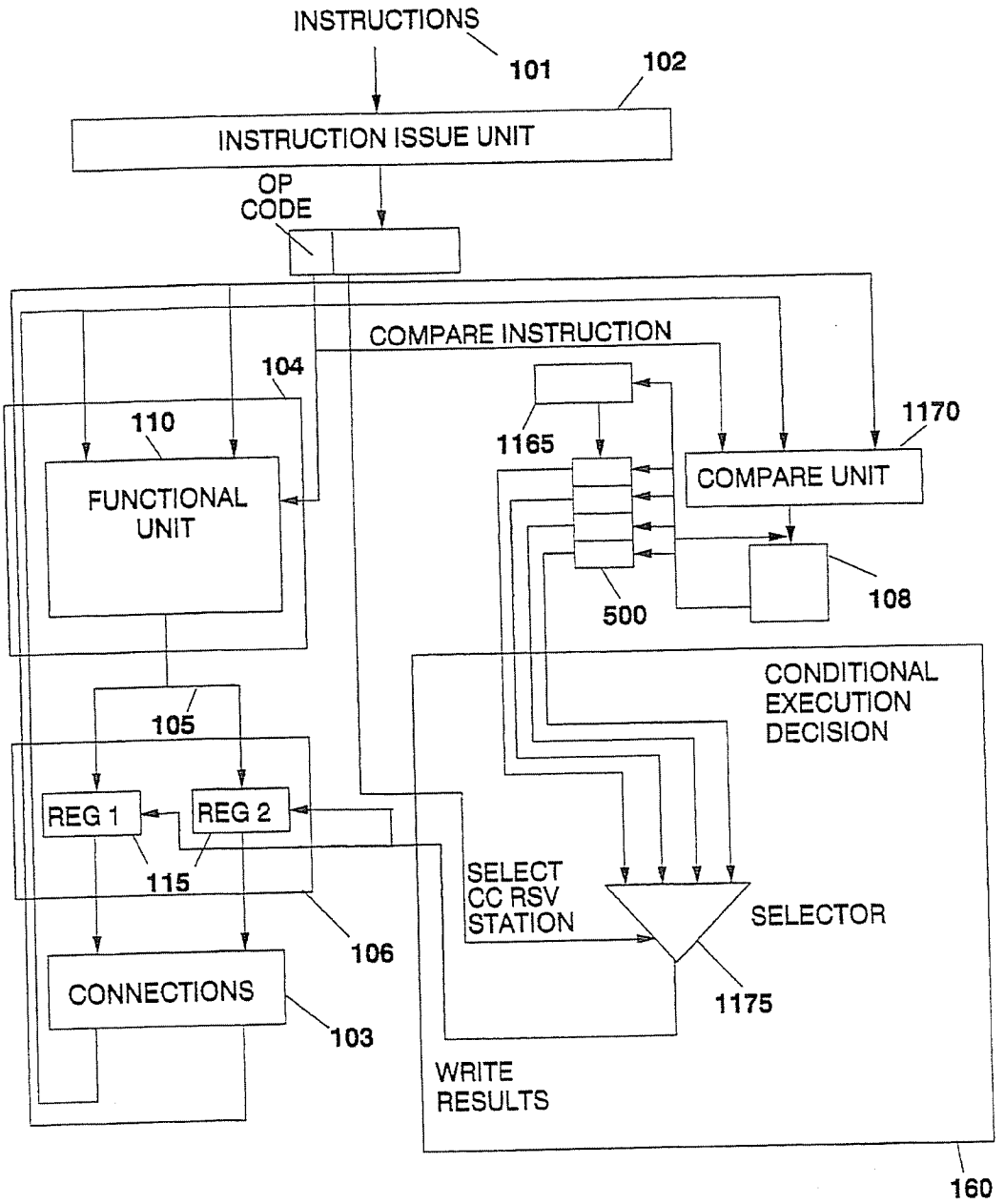


Figure 16. Invention,
Indicator Based Commit

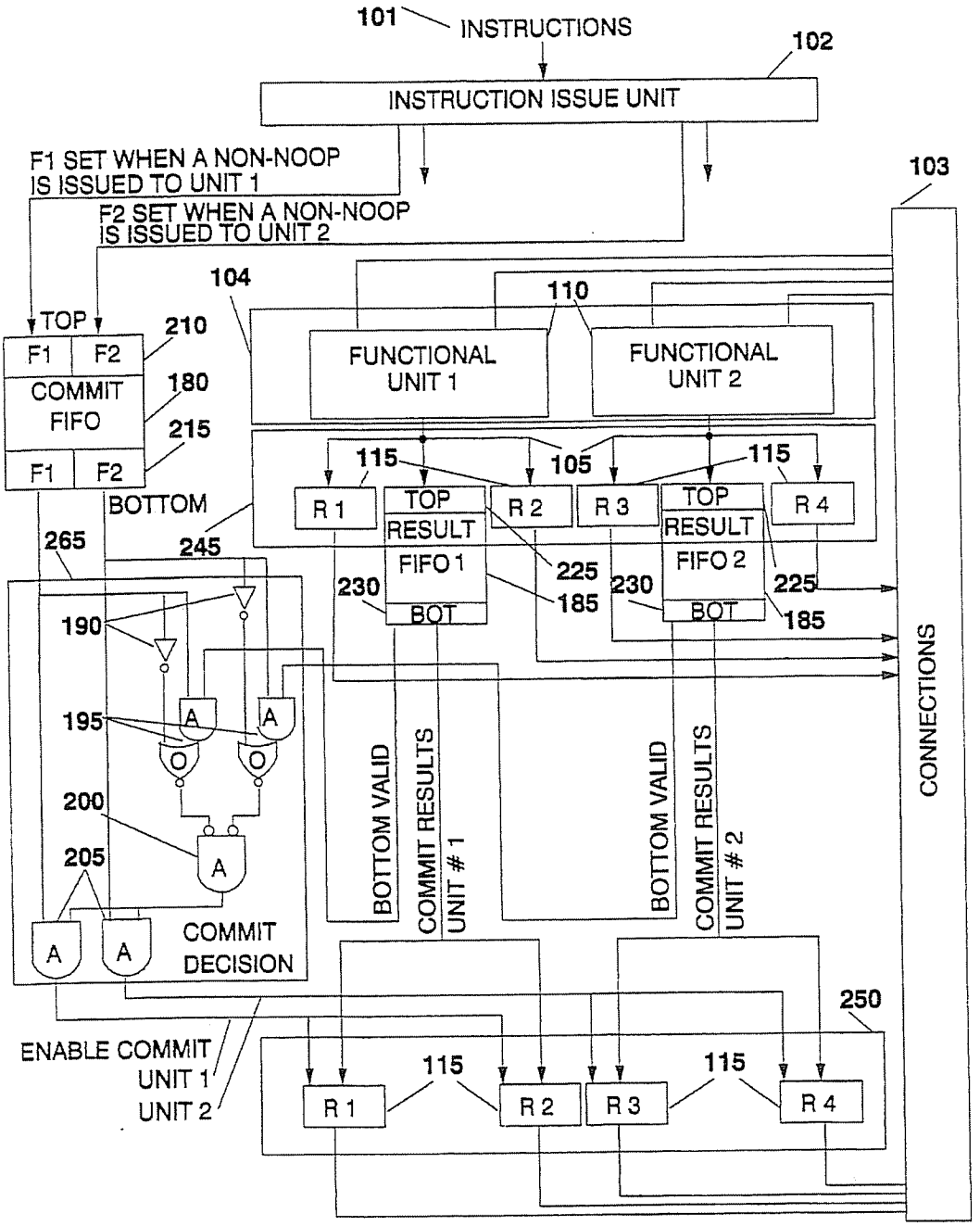


Figure 17. Invention,
High Bandpass Commit

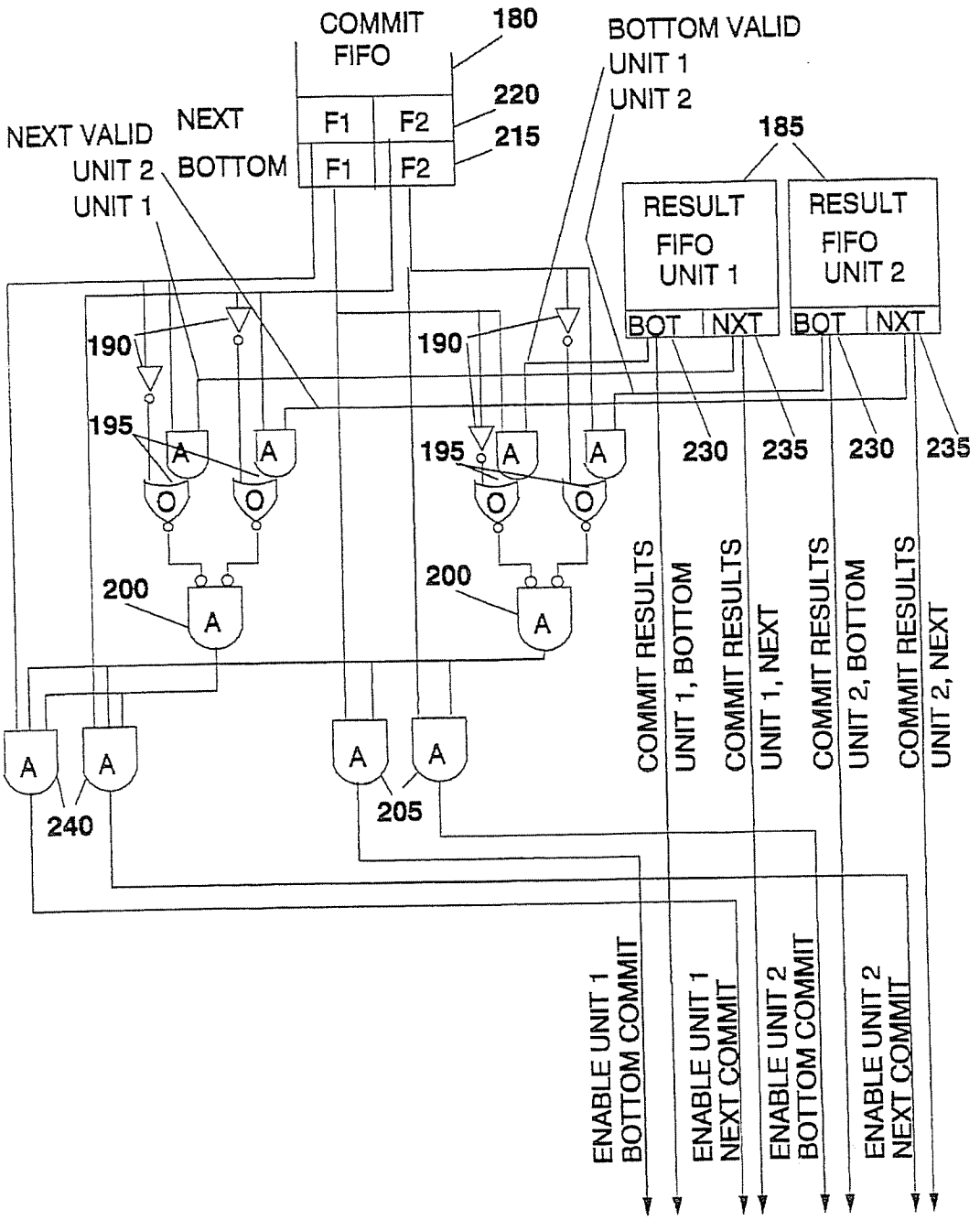


Figure 18. Invention,
Sequential Coherency Memory Tagging

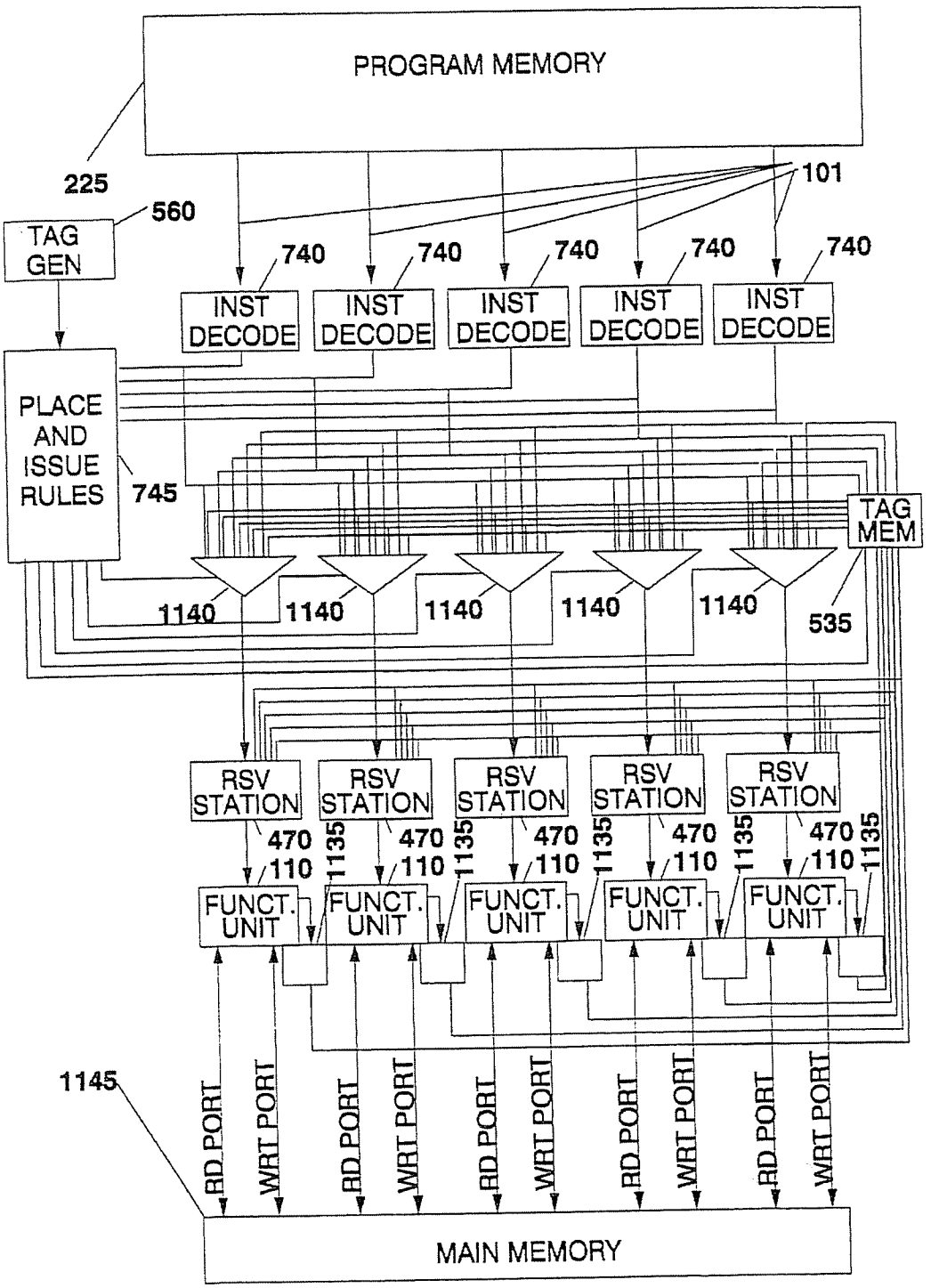
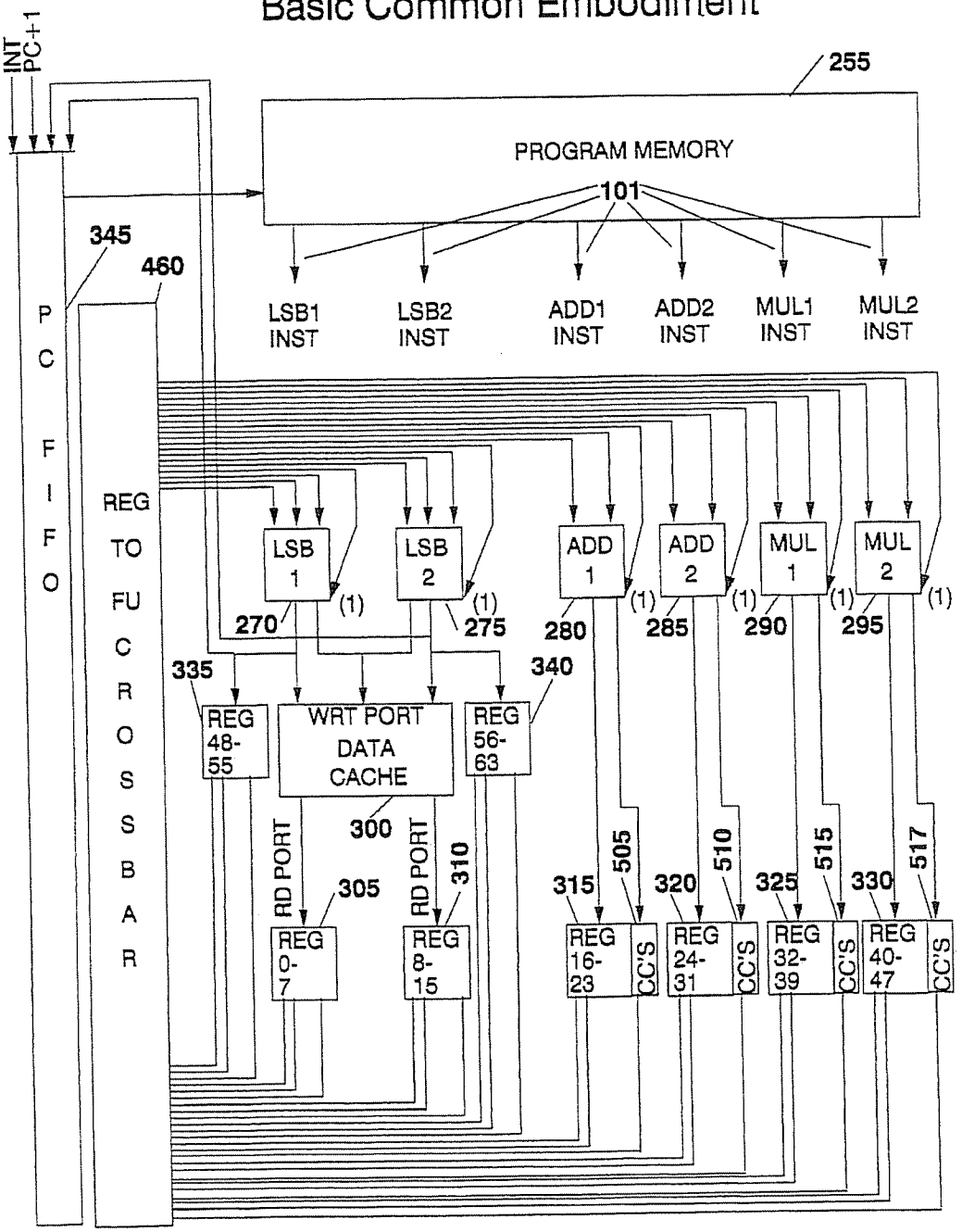


Figure 19. Invention,
Basic Common Embodiment



NOTE:
(1) CONDITION CODES CONTROL RESULTS

Figure 20. Invention,
Virtual-to-Real Address Translation
of Basic Common Embodiment

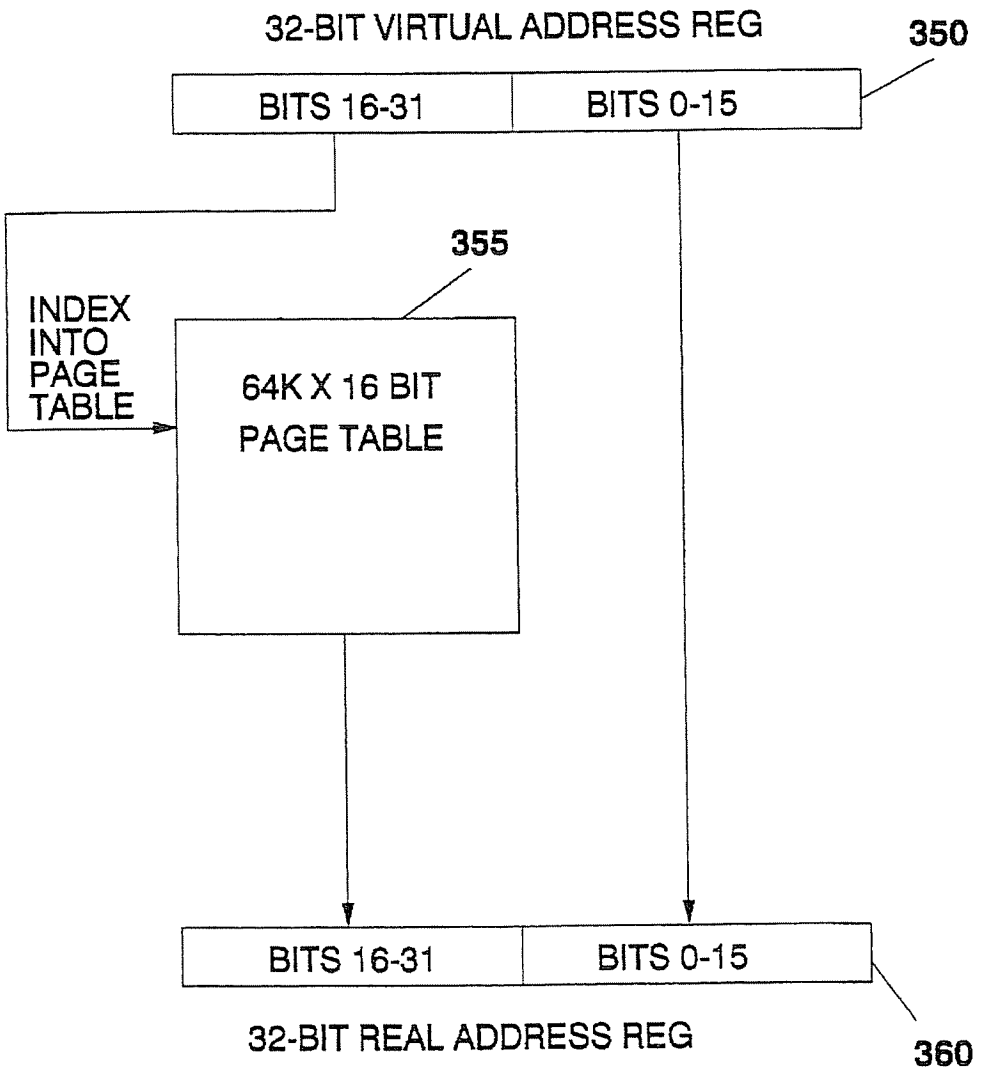


Figure 21. Invention,
Data Cache Organization
of Basic Common Embodiment

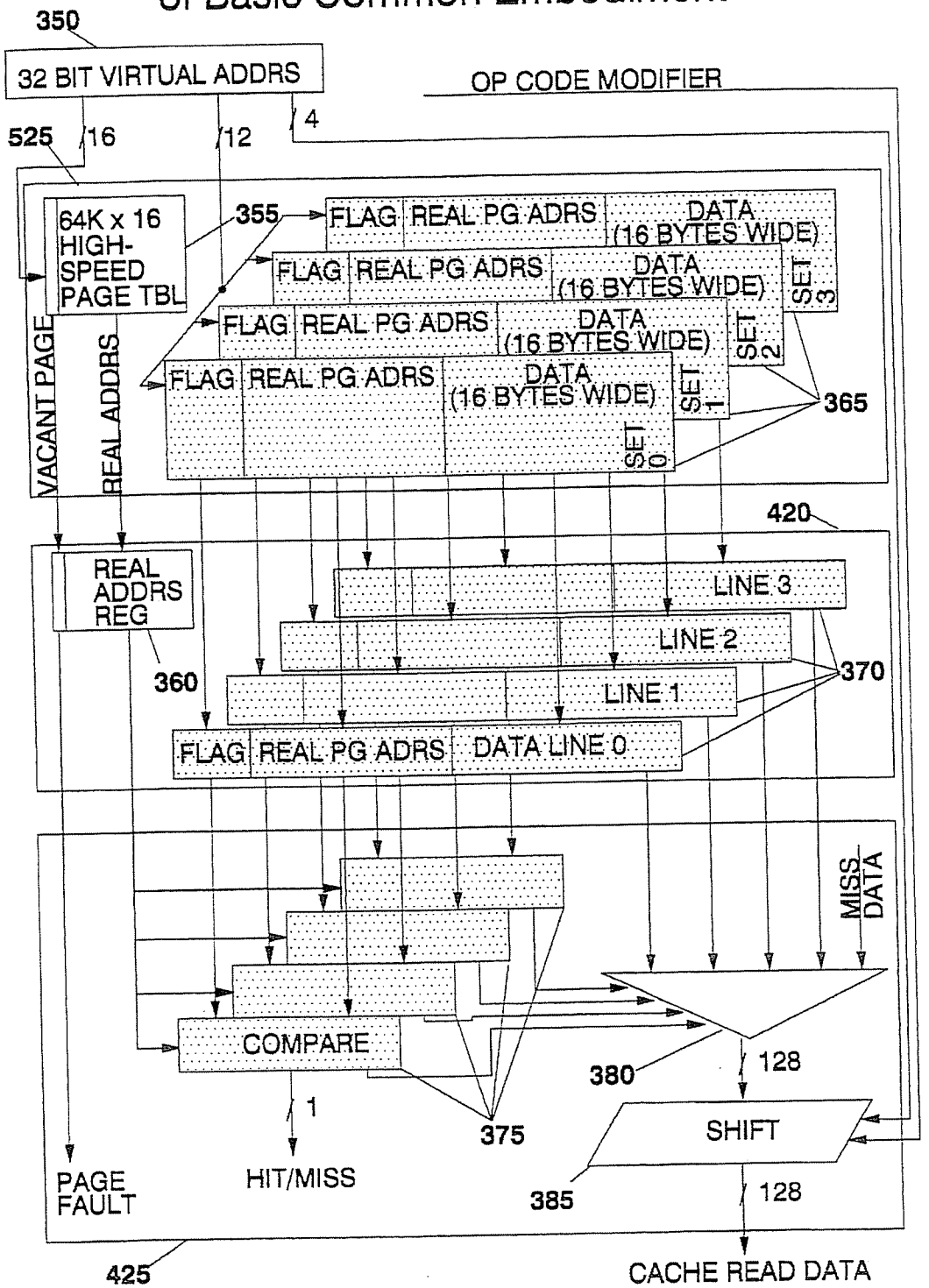


Figure 22. Invention,
LOAD/STORE/BRANCH UNITS
of Basic Common Embodiment

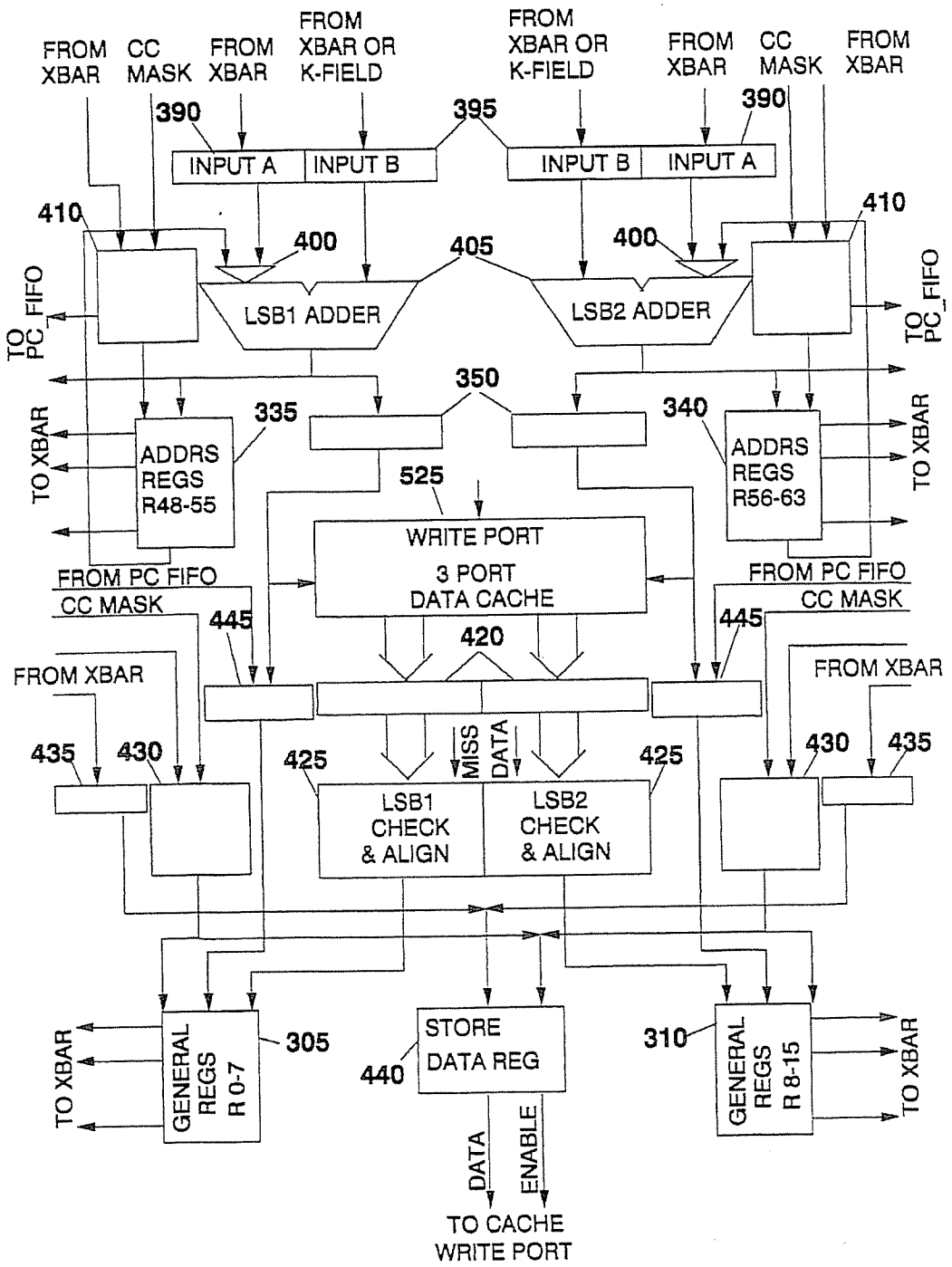


Figure 23a. Invention,
Improved Parallel Issue, Static Scheduling

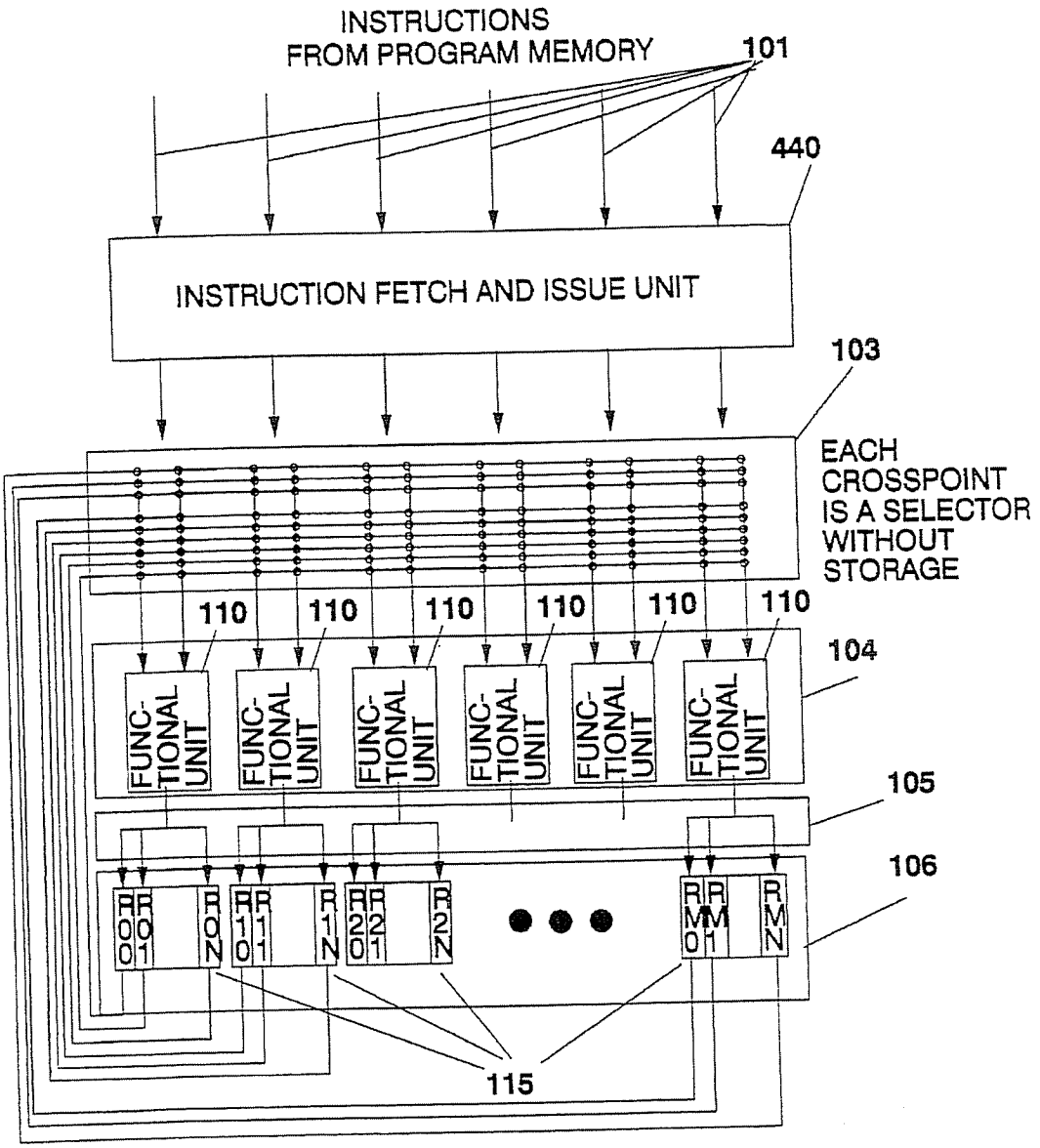


Figure 23b. Invention,
Improved Figure 23a

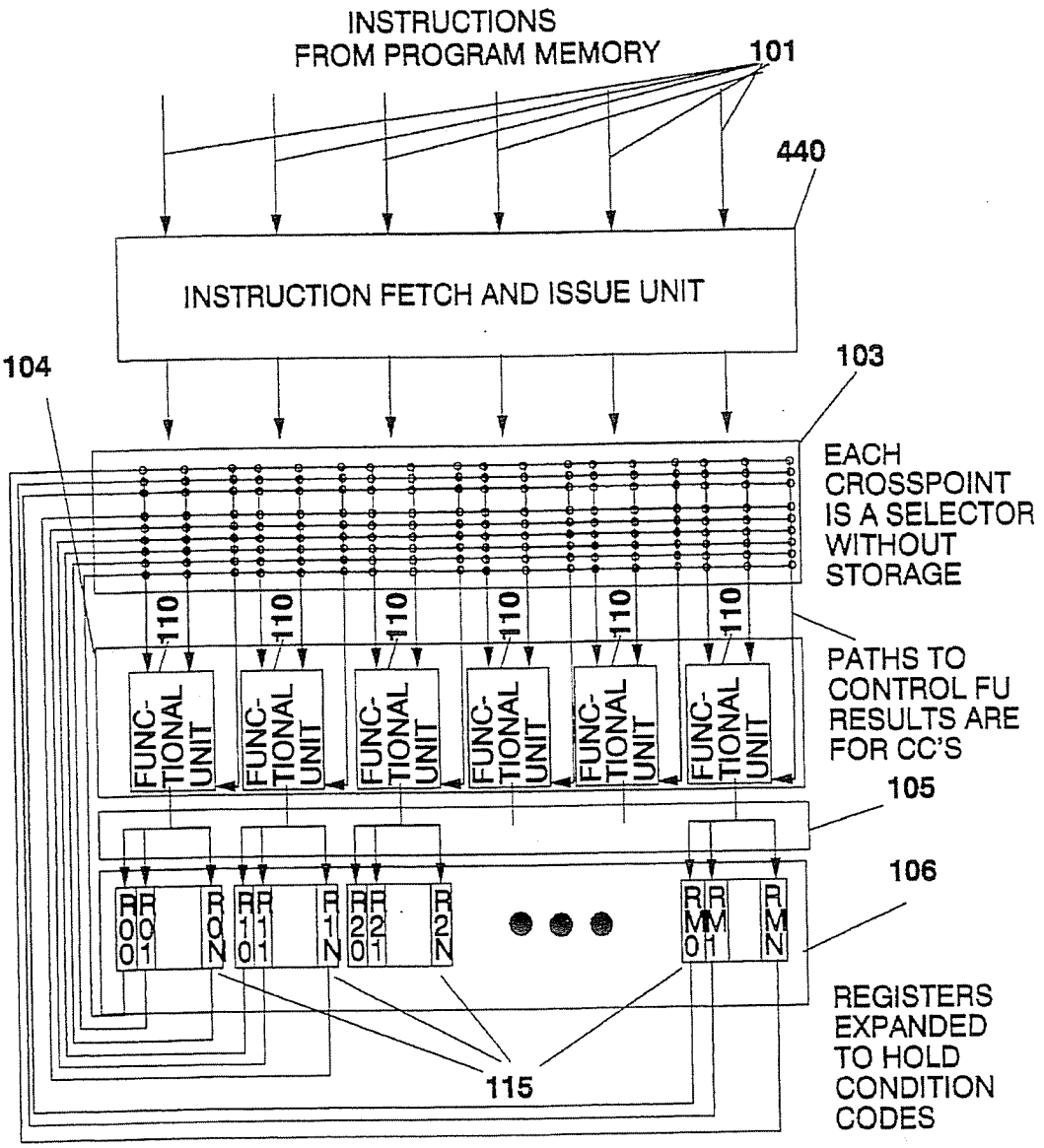
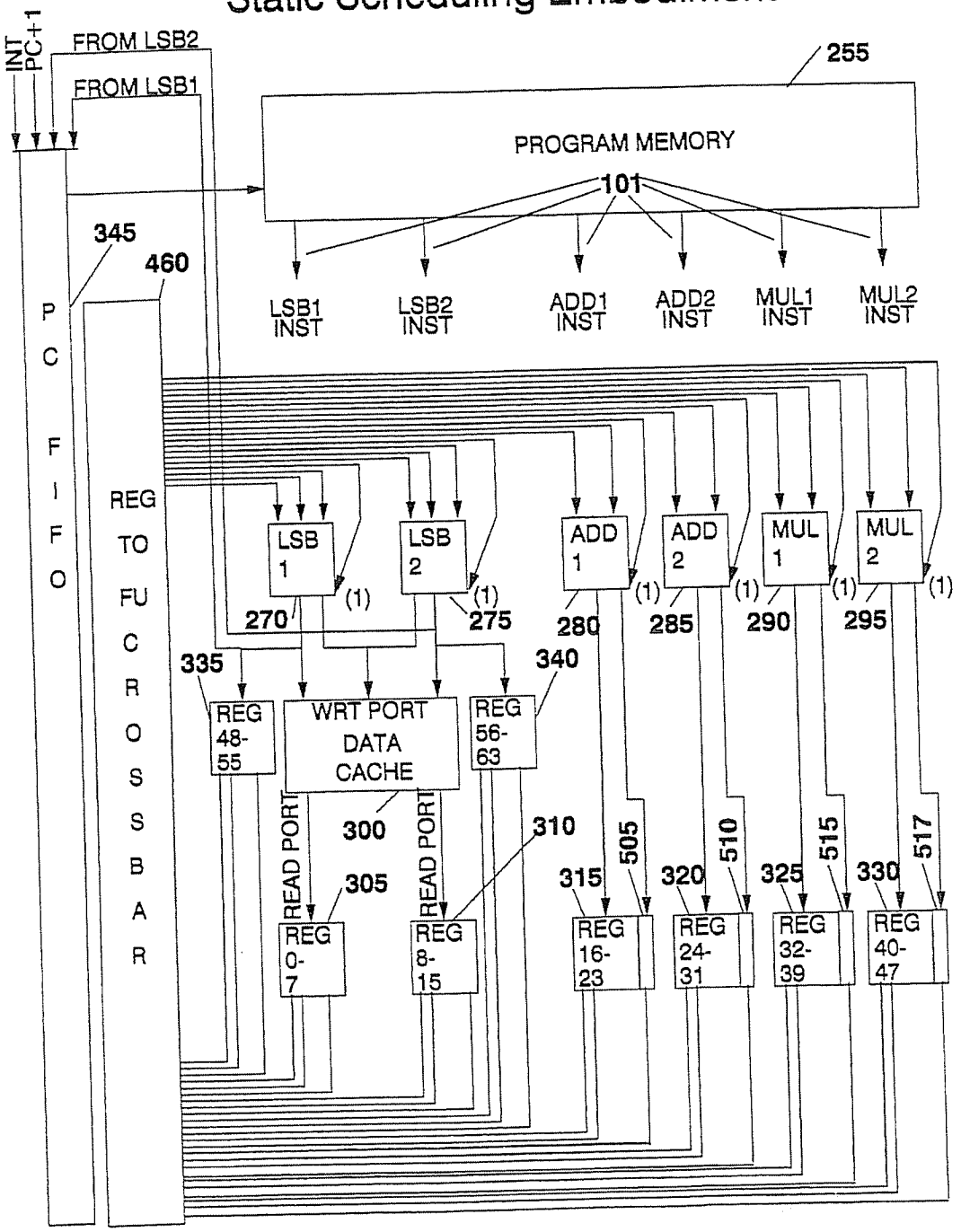


Figure 23c. Invention,
Static Scheduling Embodiment



NOTE:
(1) CC'S CONTROL RESULTS

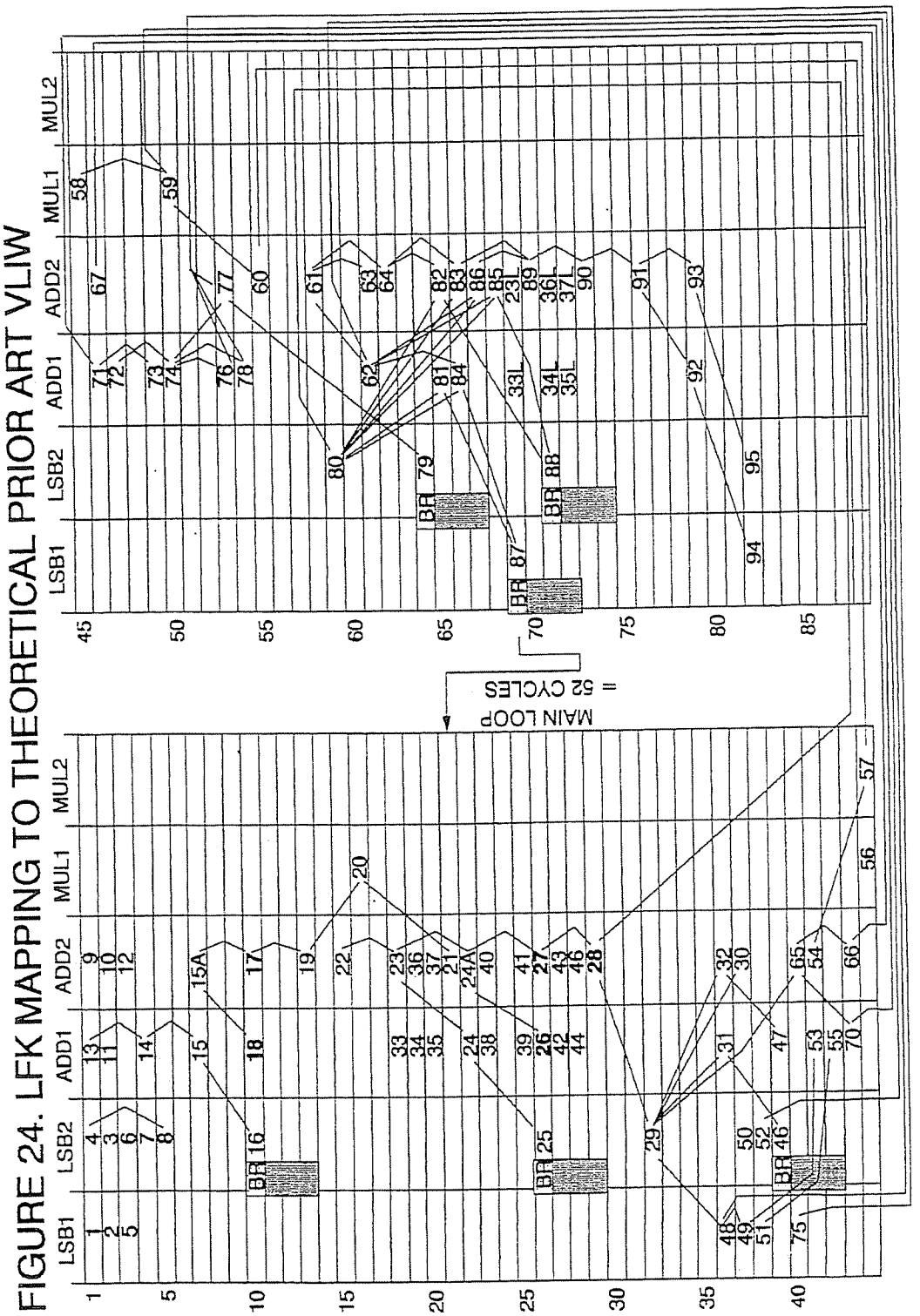


FIGURE 24. LFK MAPPING TO THEORETICAL PRIOR ART VLIW
LSB1
LSB2
ADD1
ADD2
MUL1
MUL2
BR
MAIN LOOP
= 52 CYCLES

Figure 25. Invention,
LFK16 Mapping,
Static Scheduling Embodiment

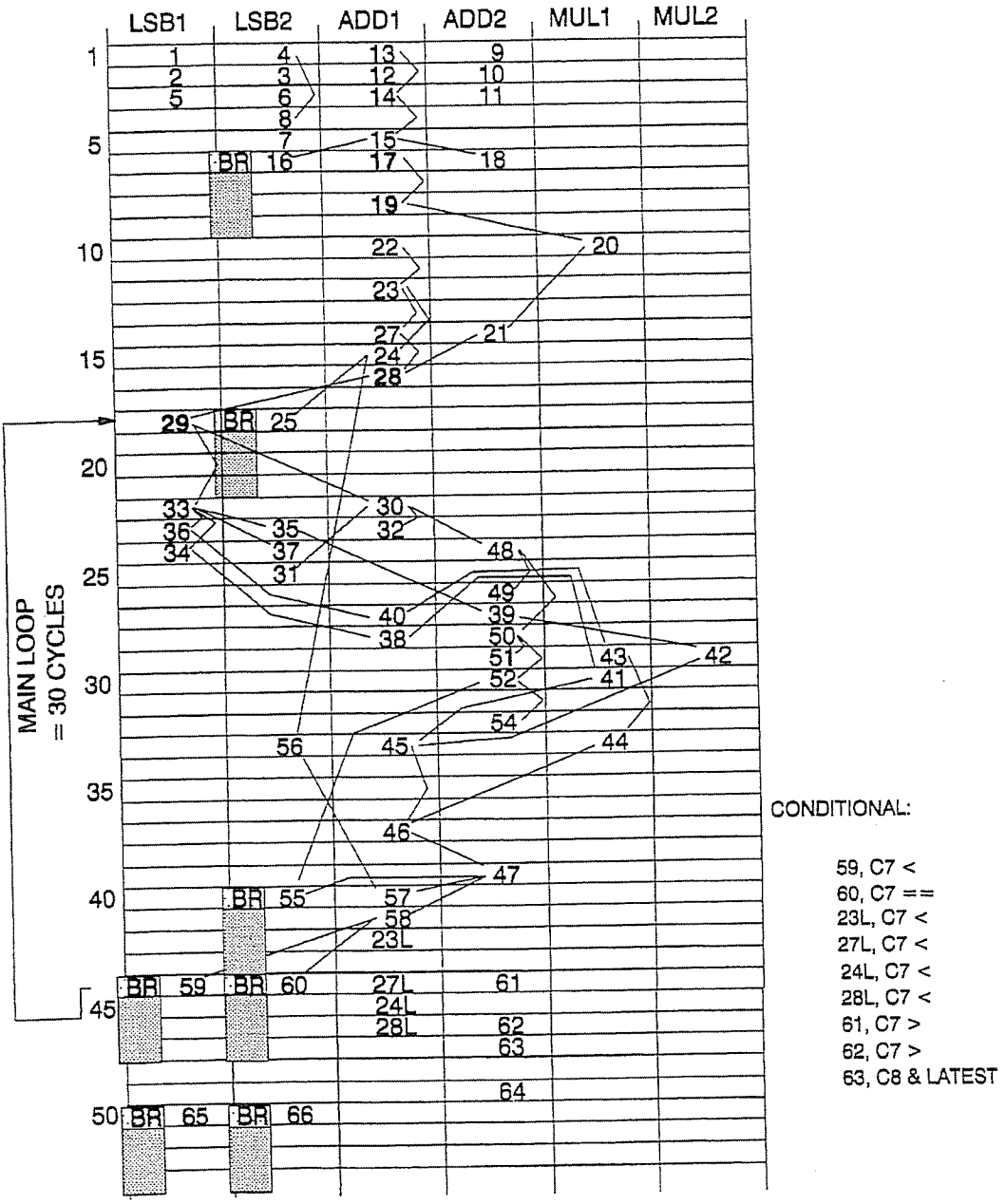


Figure 26a. Invention,
Generalized Dynamic Scheduling Embodiment

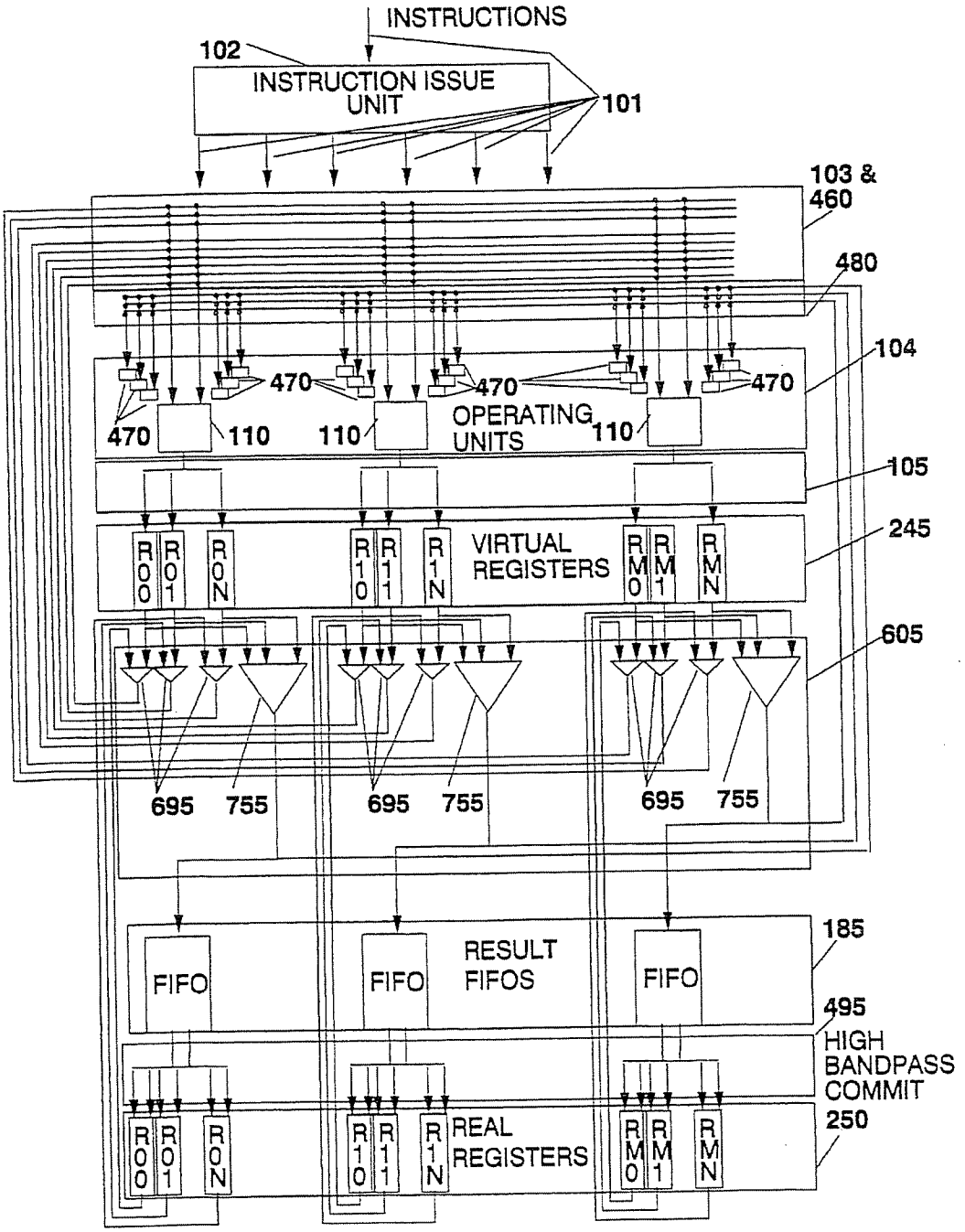


Figure 26b. Invention,
Figure 26a Improved with Conditional Execution

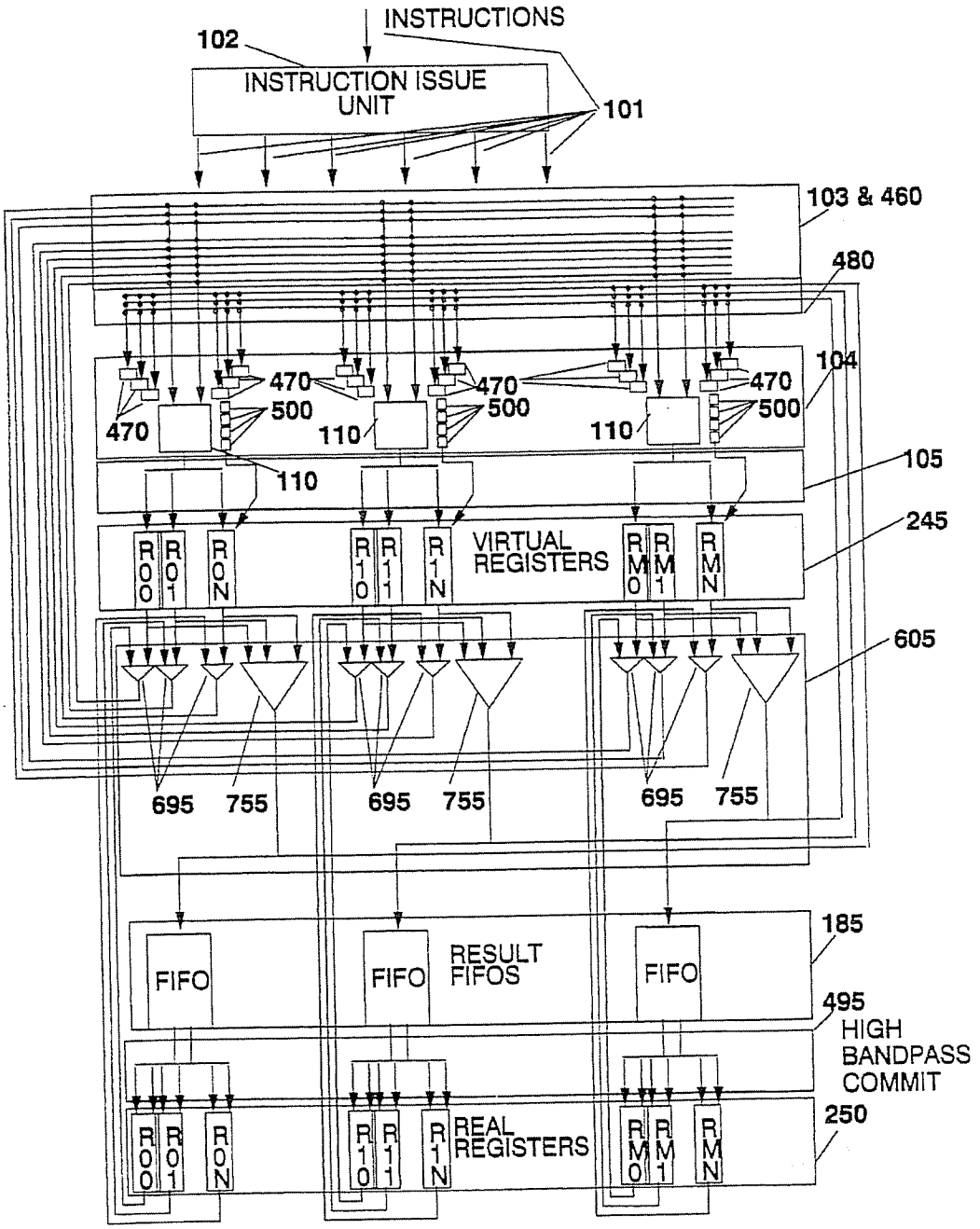


Figure 27a. Invention,
Dynamic Scheduling Embodiment

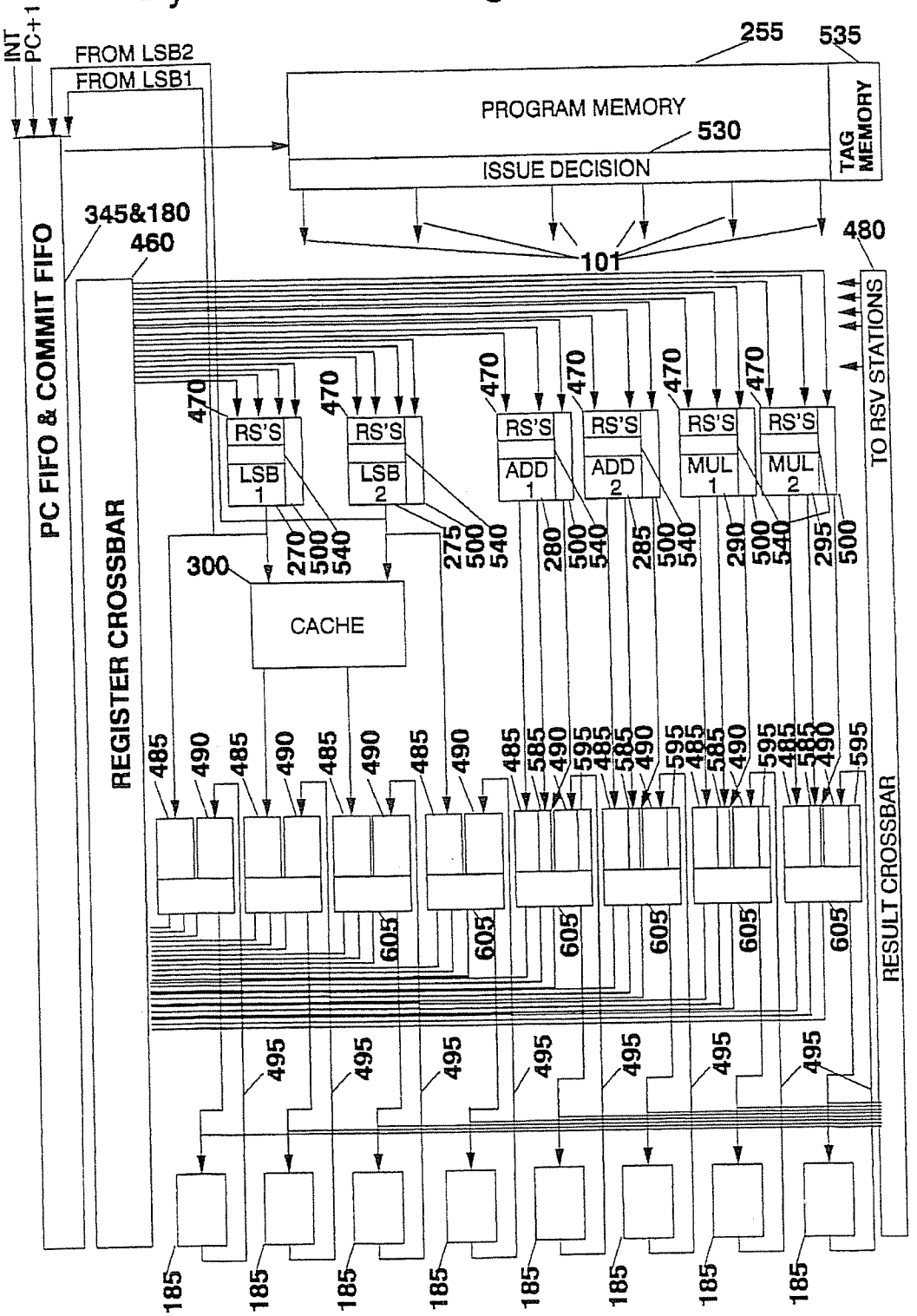


Figure 27b. Invention,
Instruction Issue, Dynamic Scheduling Embodiment

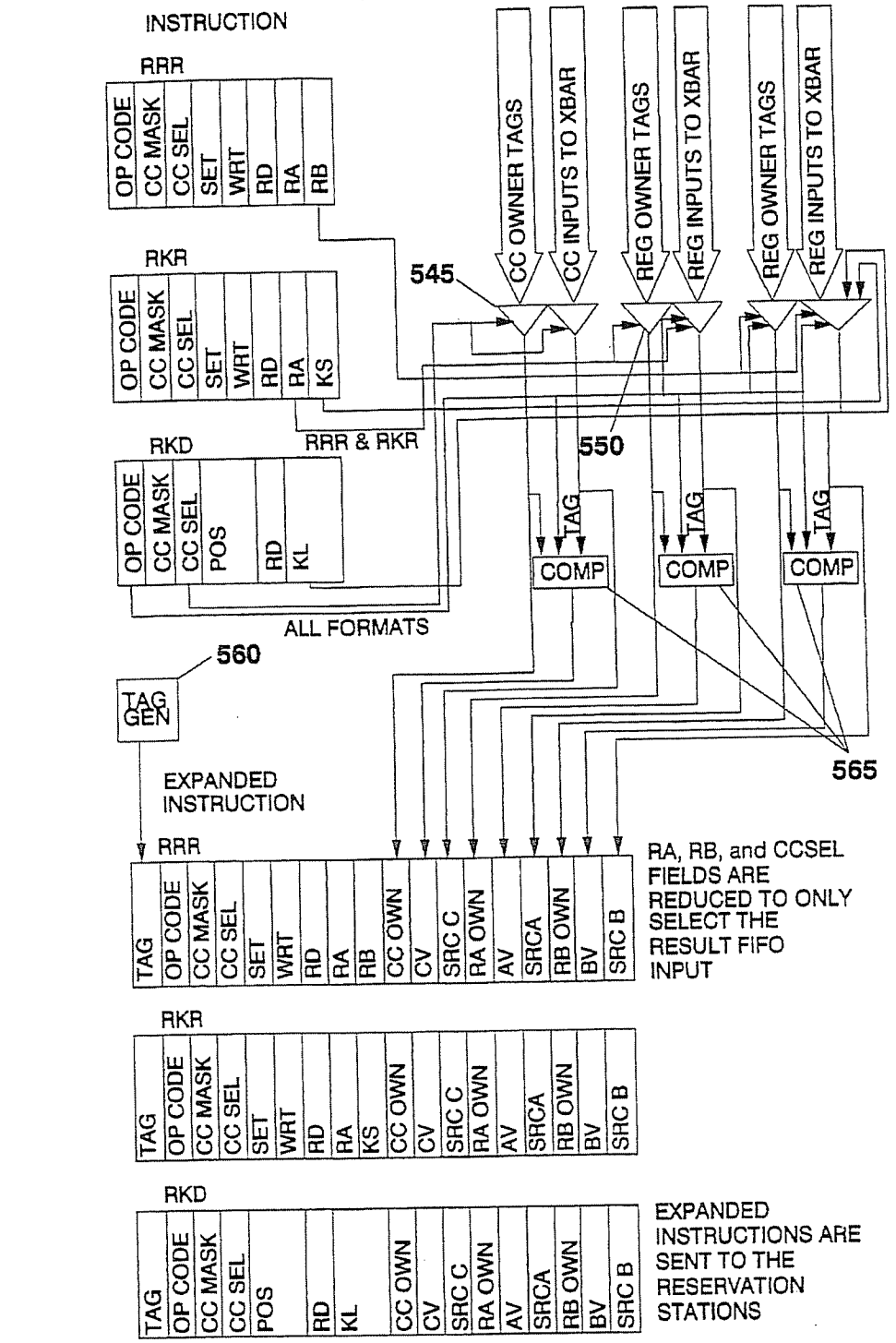


Figure 27c. Invention, Reservation Stations, Dynamic Scheduling Embodiment

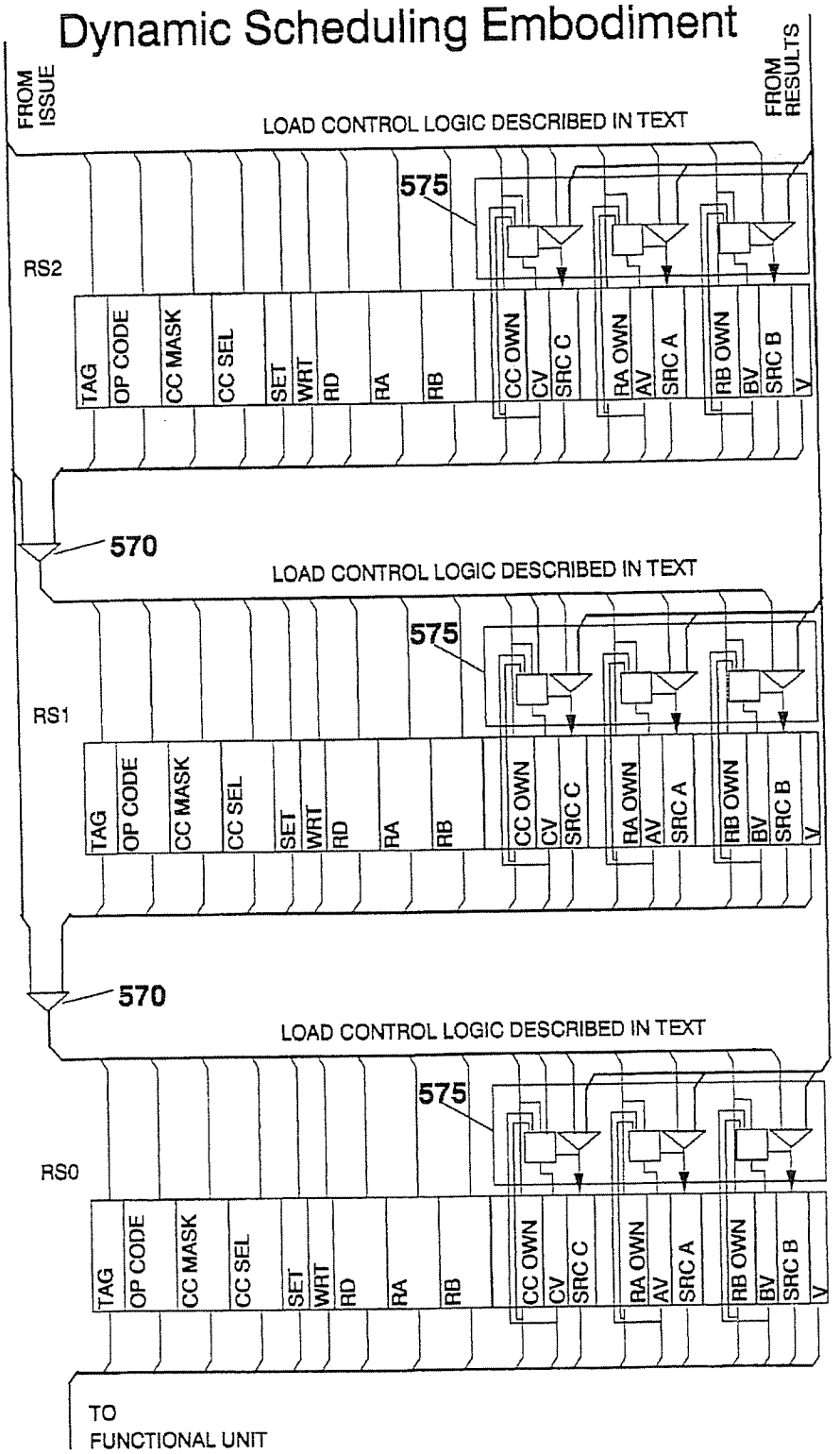


Figure 27d. Invention,
Functional Unit, Dynamic Scheduling Embodiment

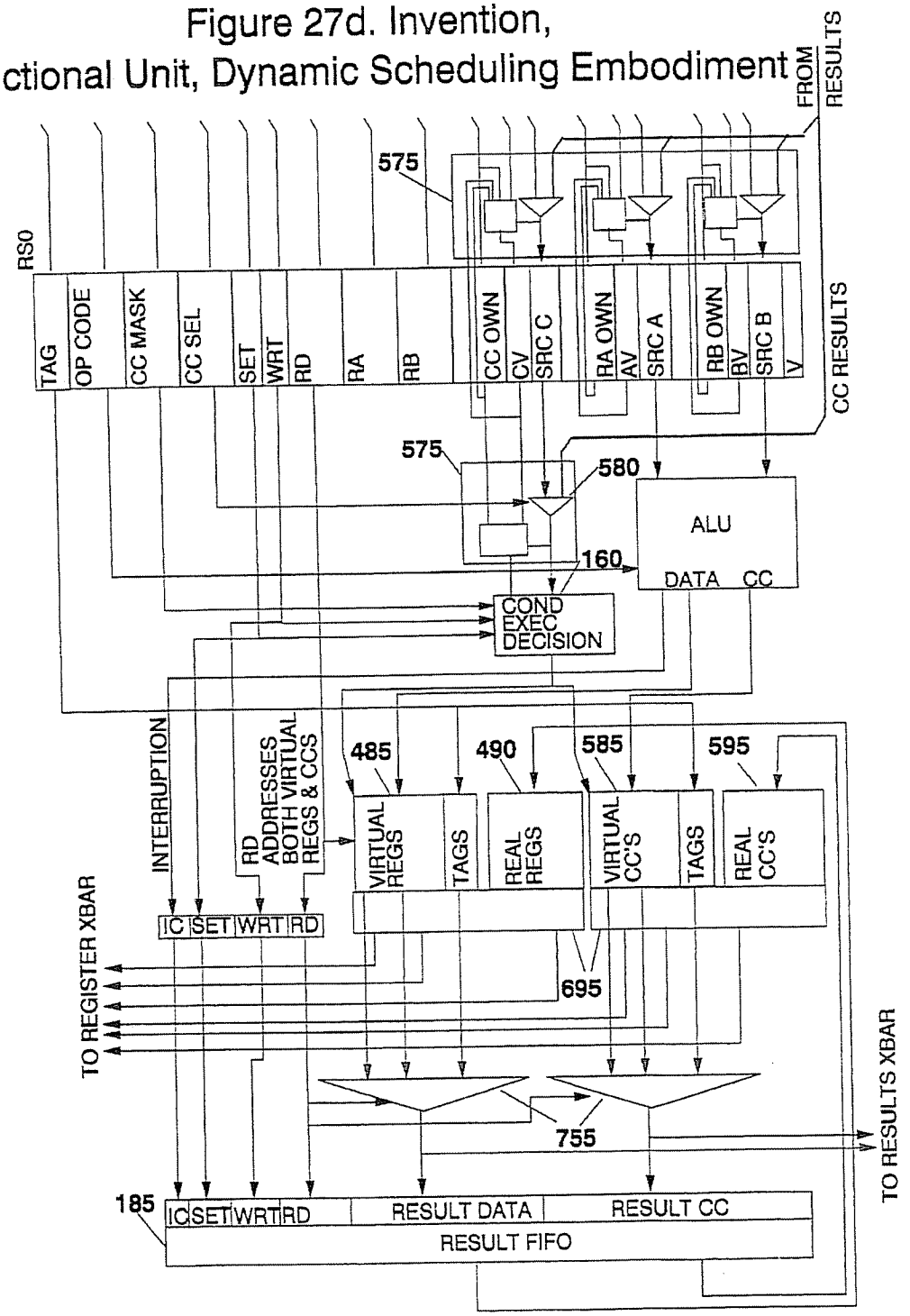
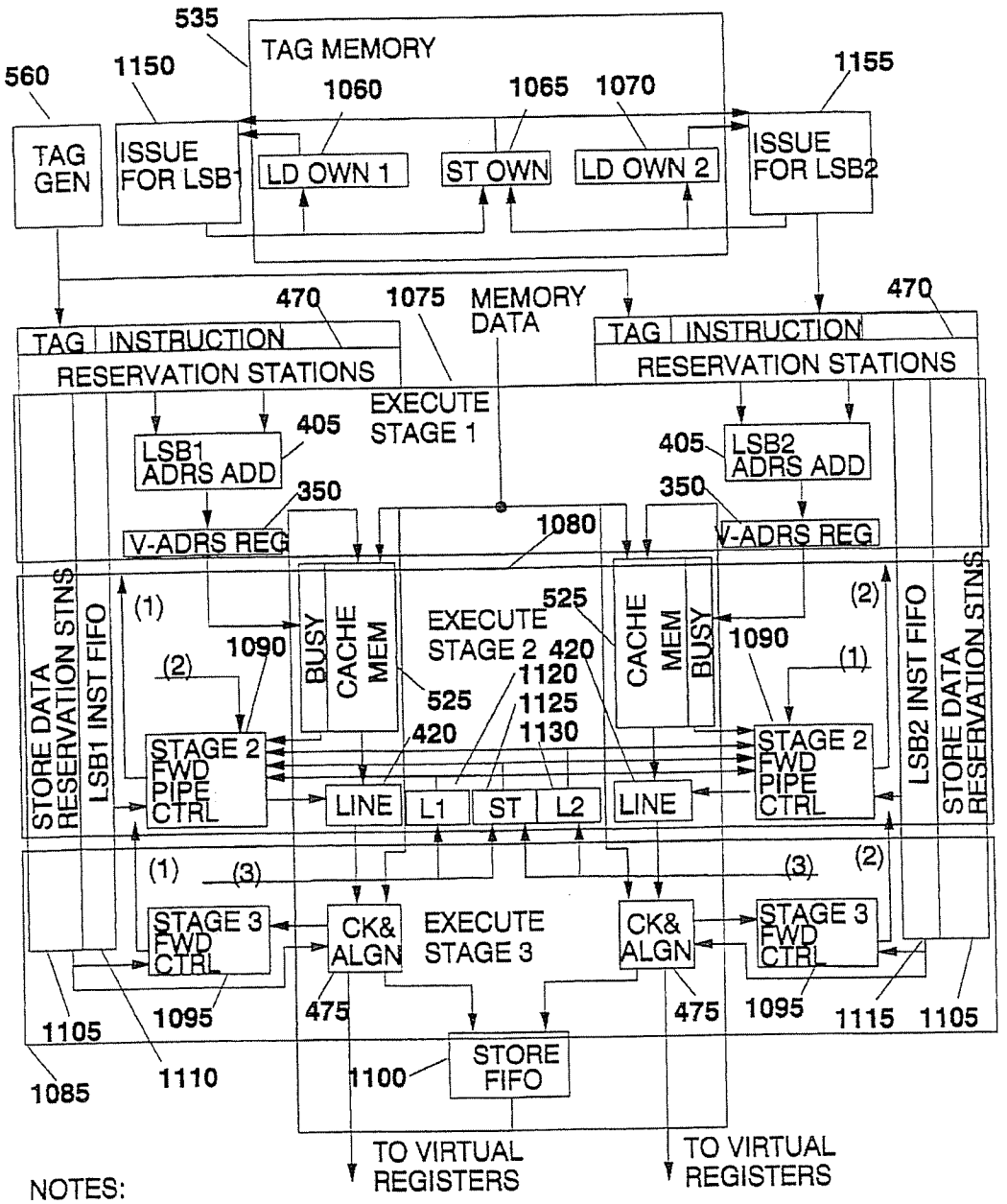


Figure 27e. Invention,
Dynamic Scheduling Embodiment,
Main Memory Tagging



NOTES:
(1) GENERATE & PROPAGATE
(2) PREVIOUS OWNER TAG(S) FROM INST
(3) TAG FROM THE INSTRUCTION

Figure 27f. Invention,
Real Registers and CCs,
Dynamic Scheduling Embodiment

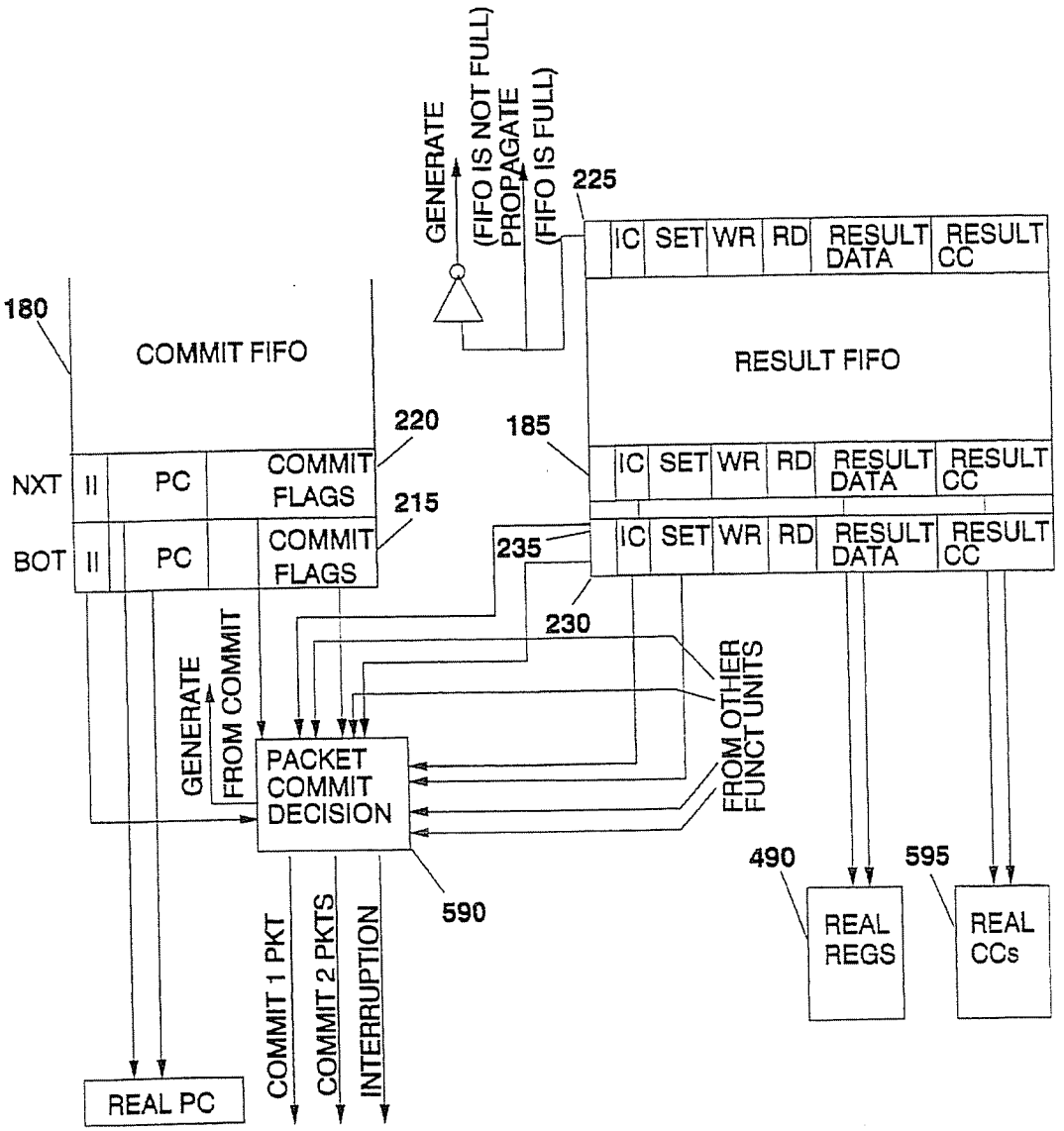


Figure 28. Invention, Vector Embodiment

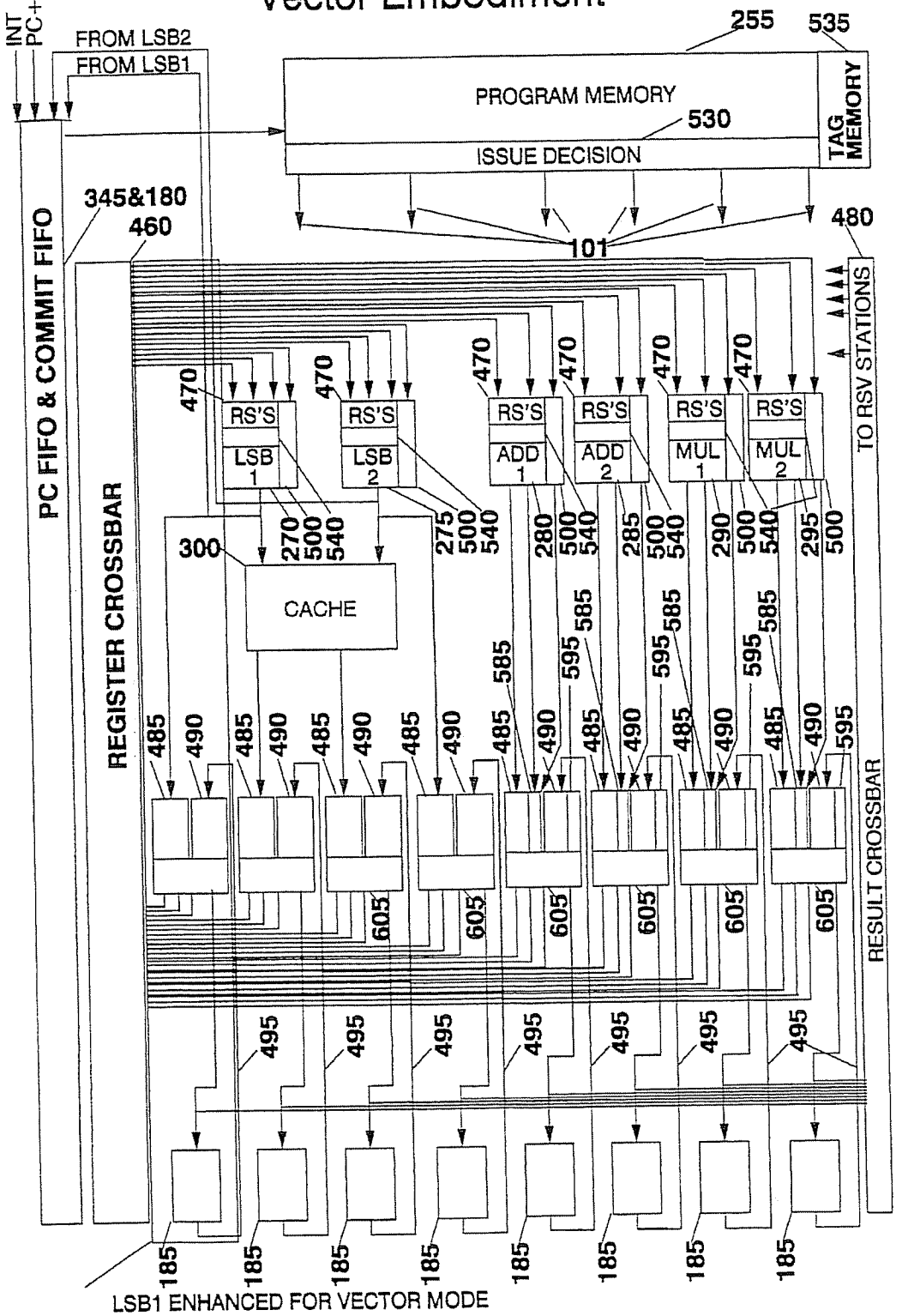


Figure 29. Invention, One-Packet Vector Loop Example

R48 = 6-3 R49 = 104 R50 = 104

ADDRS	LSB1 INST	LSB2 INST
100	LOOP 104	STORE RK,RA,1,IRA
101	ANY	STORE RK,RA,1,IRA
102	ANY	STORE RK,RA,1,IRA
103	ANY	STORE RK,RA,1,IRA
104	DEC/SET	STORE RK,RA,1,IRA
105	ANY	ANY
106	ANY	ANY
107	ANY	ANY

STORE TO 4 LOCATIONS (OUTSIDE THE LOOP)

STORE TO 6 LOCATIONS (INSIDE THE LOOP)

TOTAL OF 10 LOCATIONS

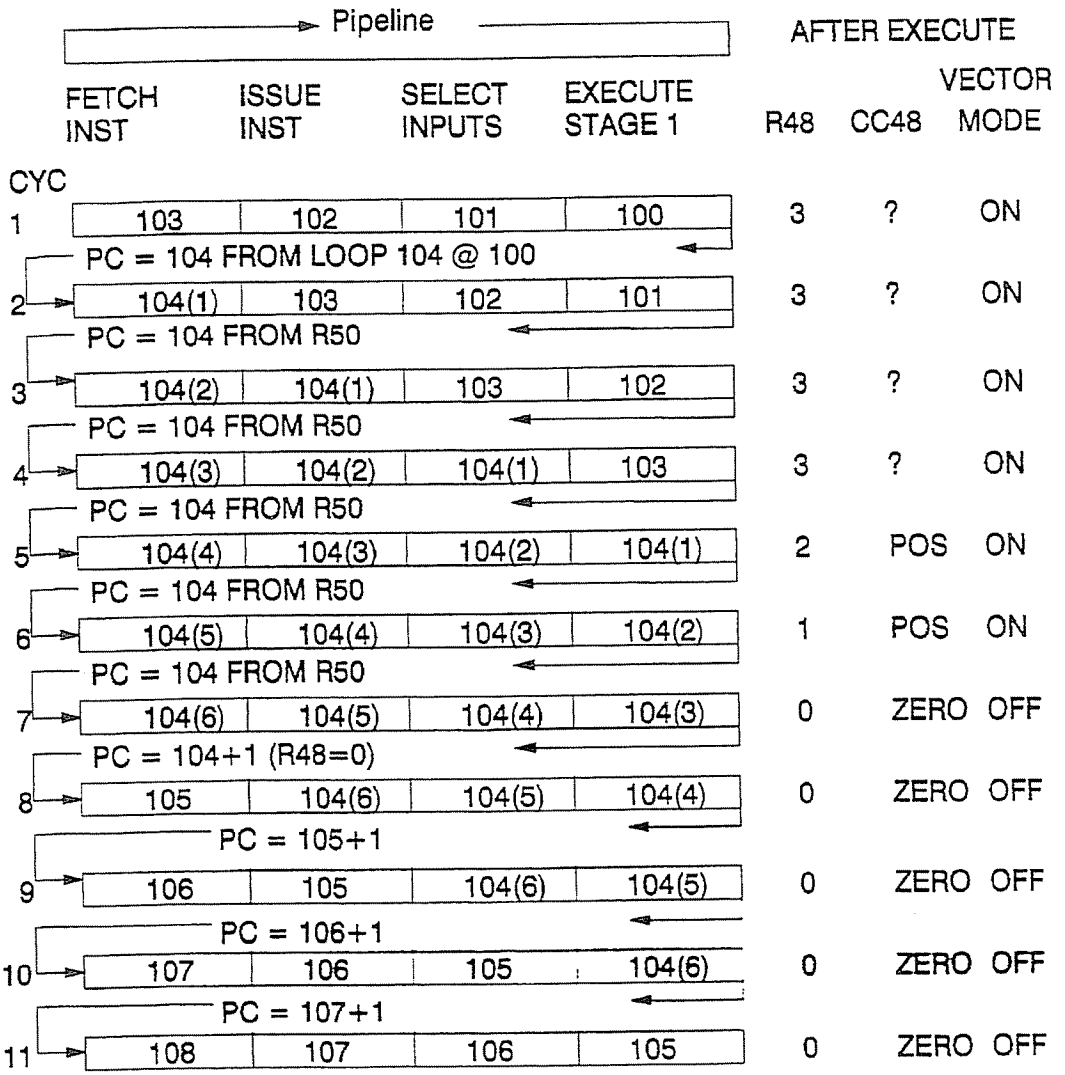


Figure 30. Invention,
LFK24 Main Loop Mapping,
Vector Embodiment

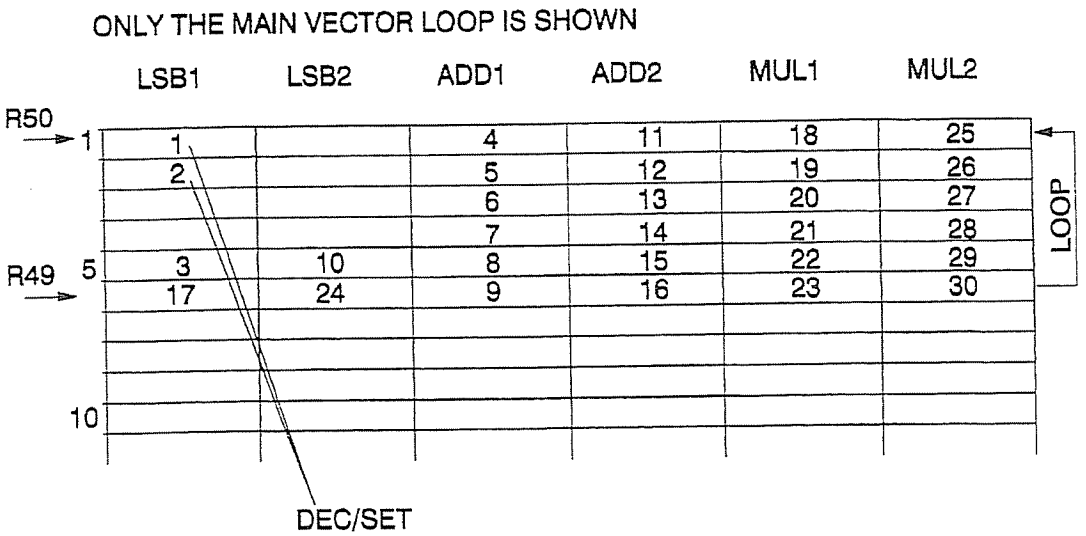


Figure 31a. Invention,
IBM 370-XA CISC Embodiment

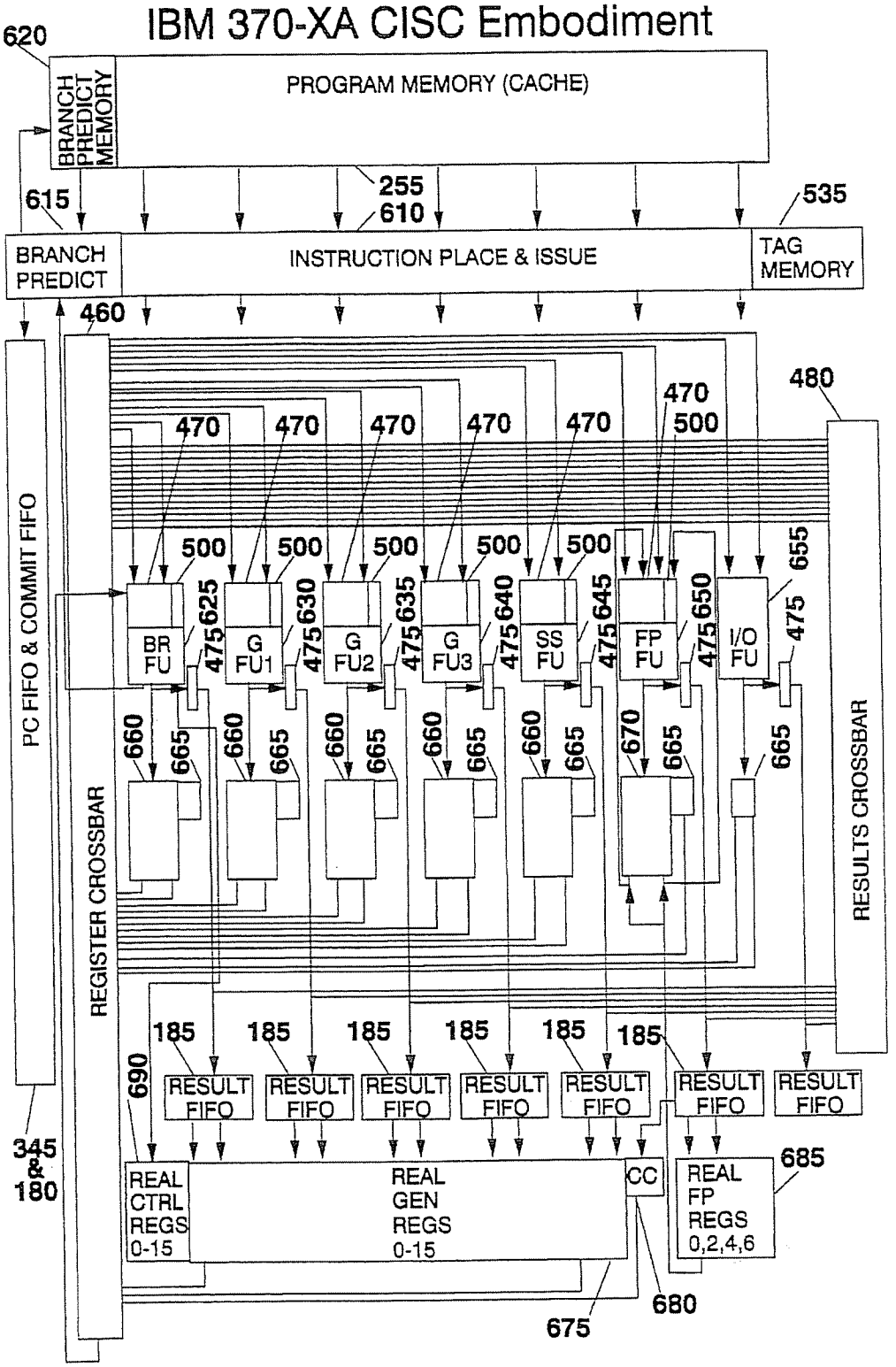


Figure 31b. Invention,
IBM 370-XA Embodiment, Issue Logic

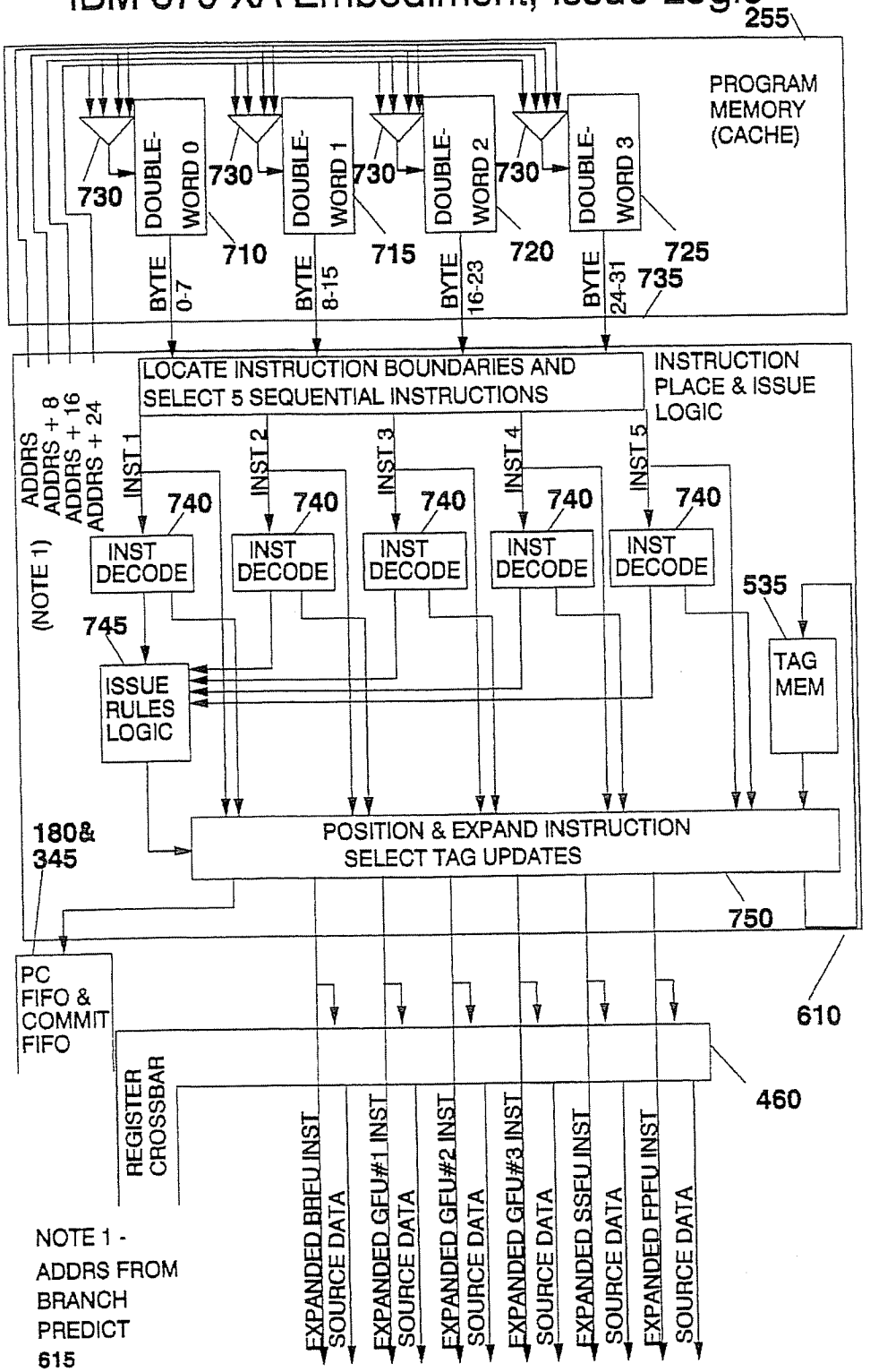


Figure 31c. Invention, IBM 370-XA Branch Functional Unit

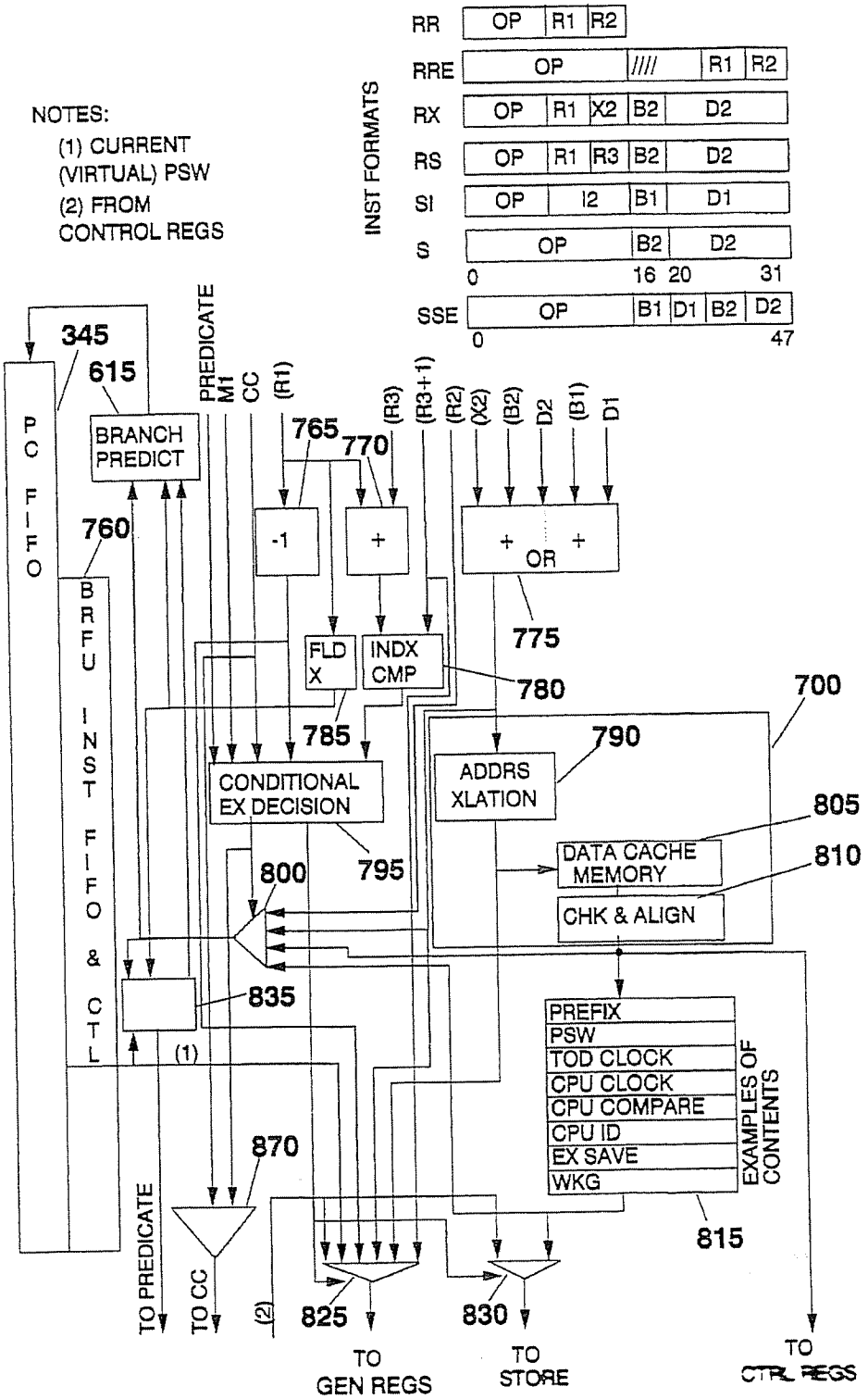


Figure 31d. Invention, IBM 370-XA General Functional Unit

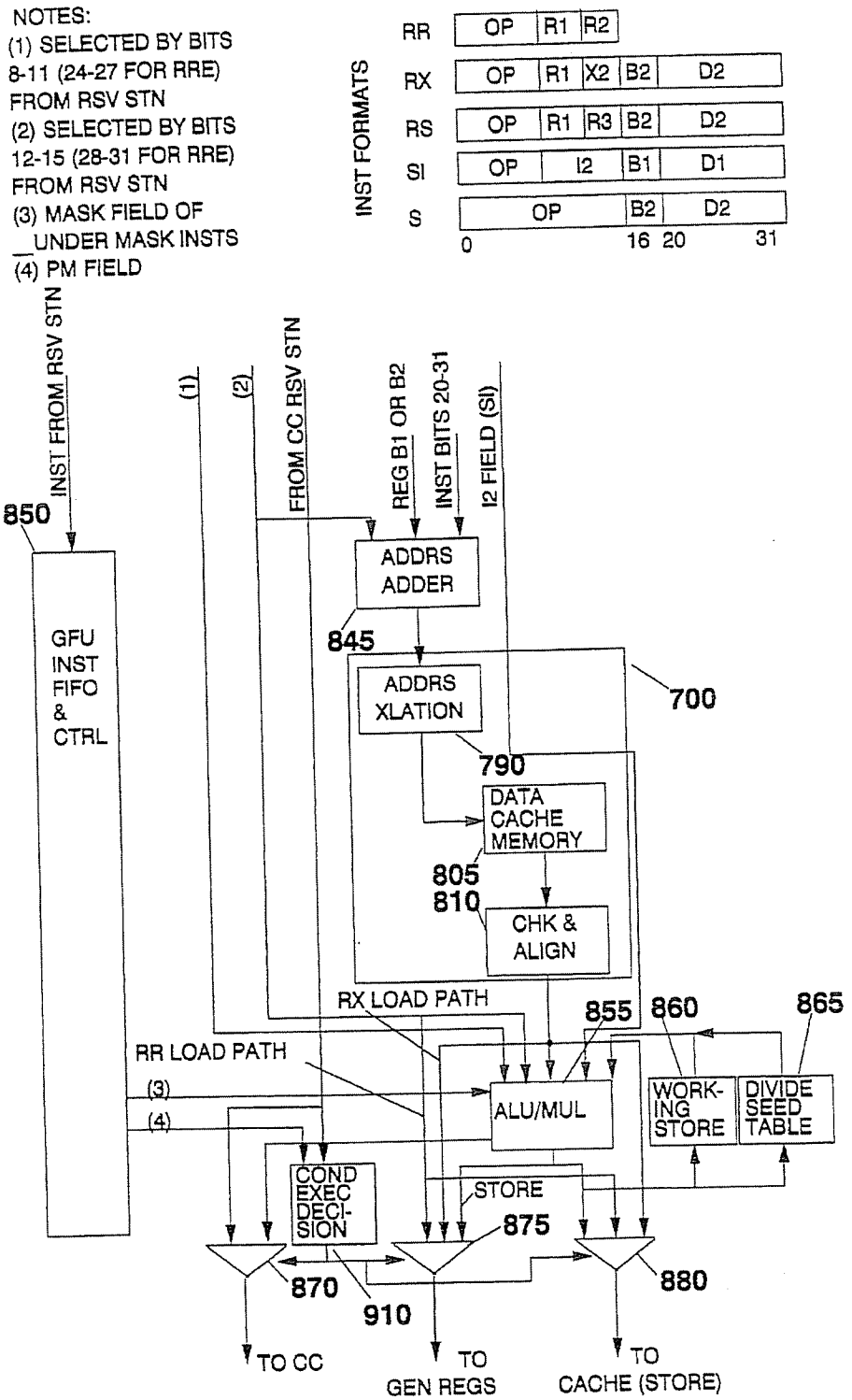


Figure 31e. Invention, IBM 370-XA SS Functional Unit

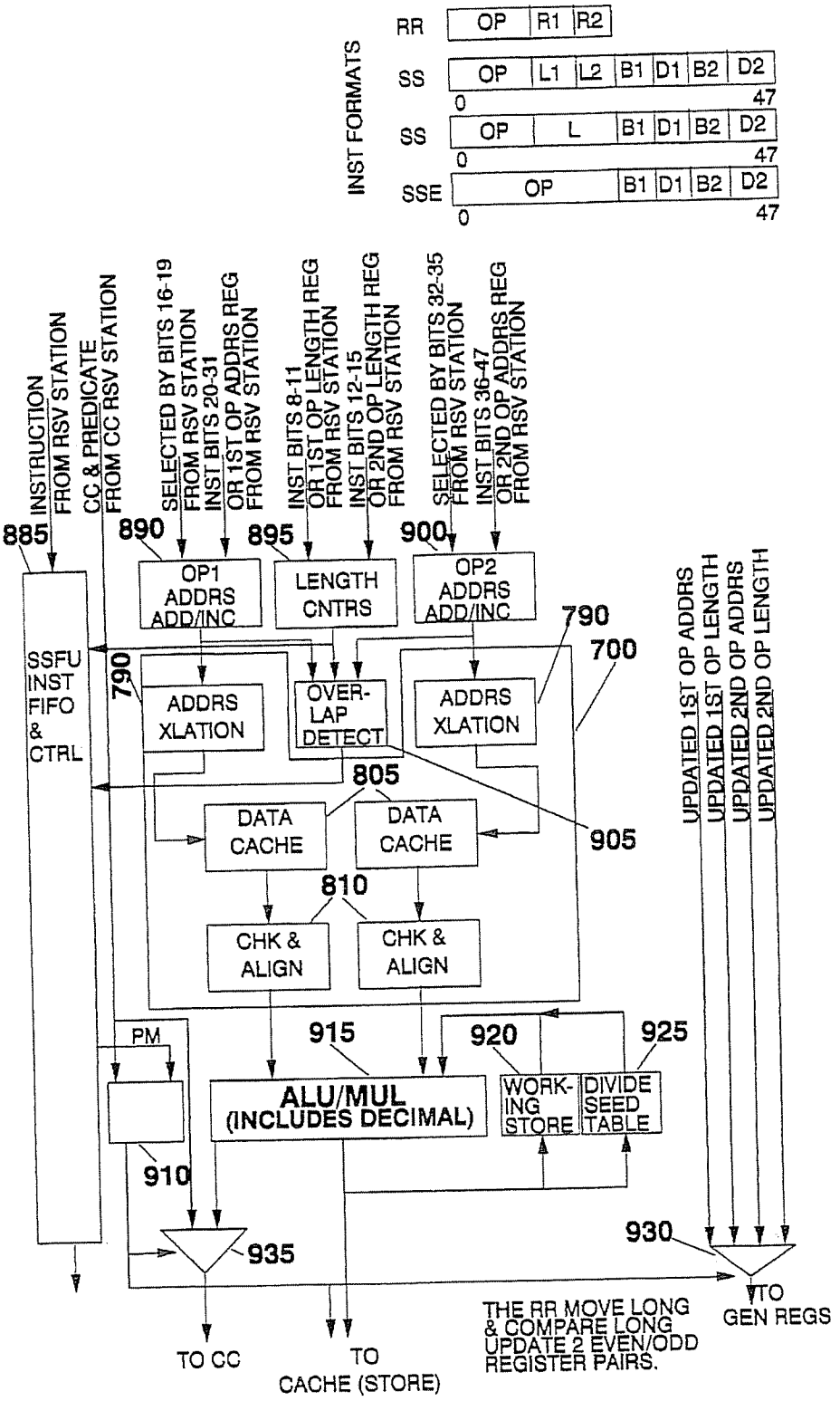


Figure 31f. Invention,
IBM 370-XA
Floating-Point Functional Unit

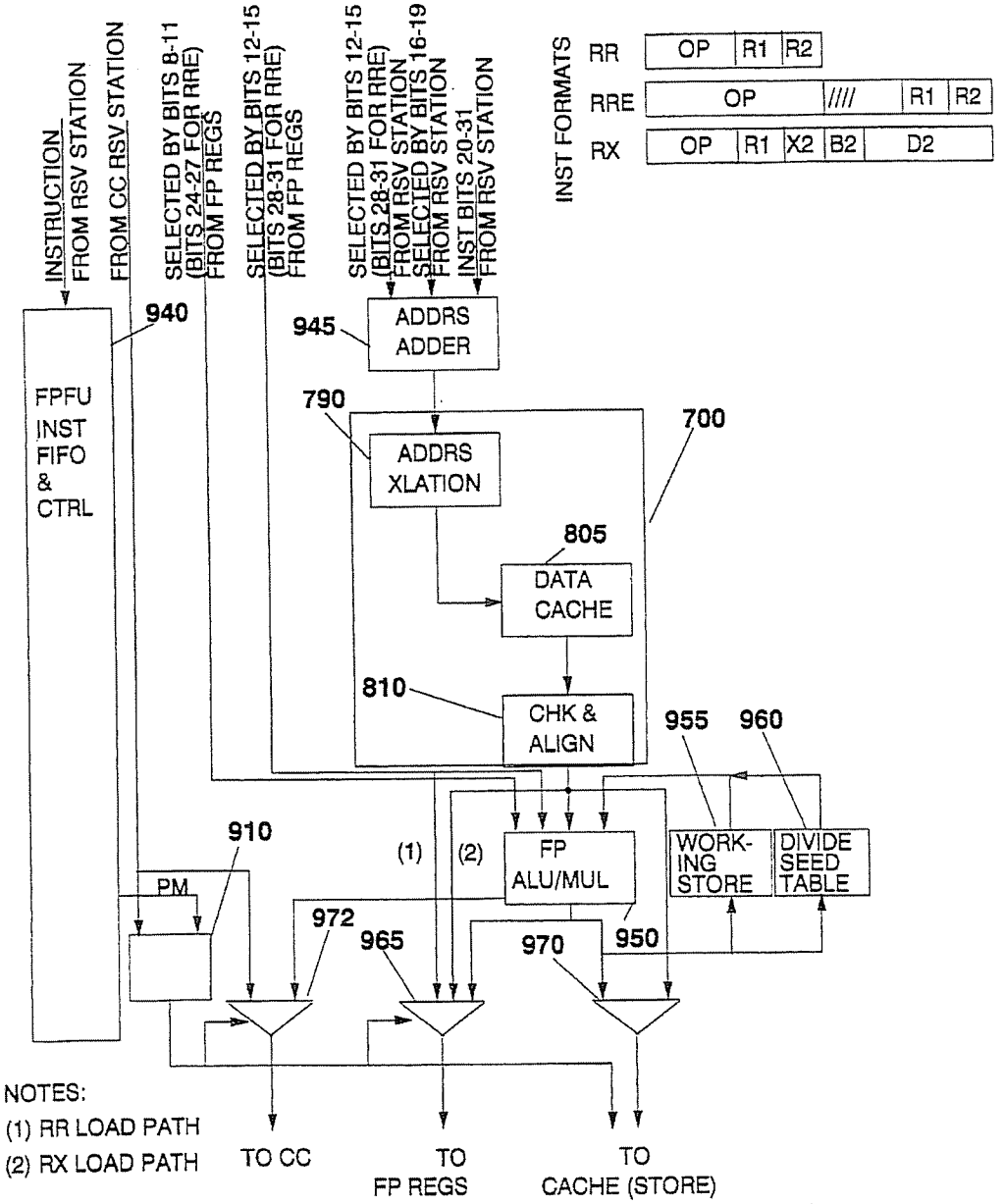


Figure 31g. Invention,
IBM 370-XA Embodiment,
Data Cache Ports

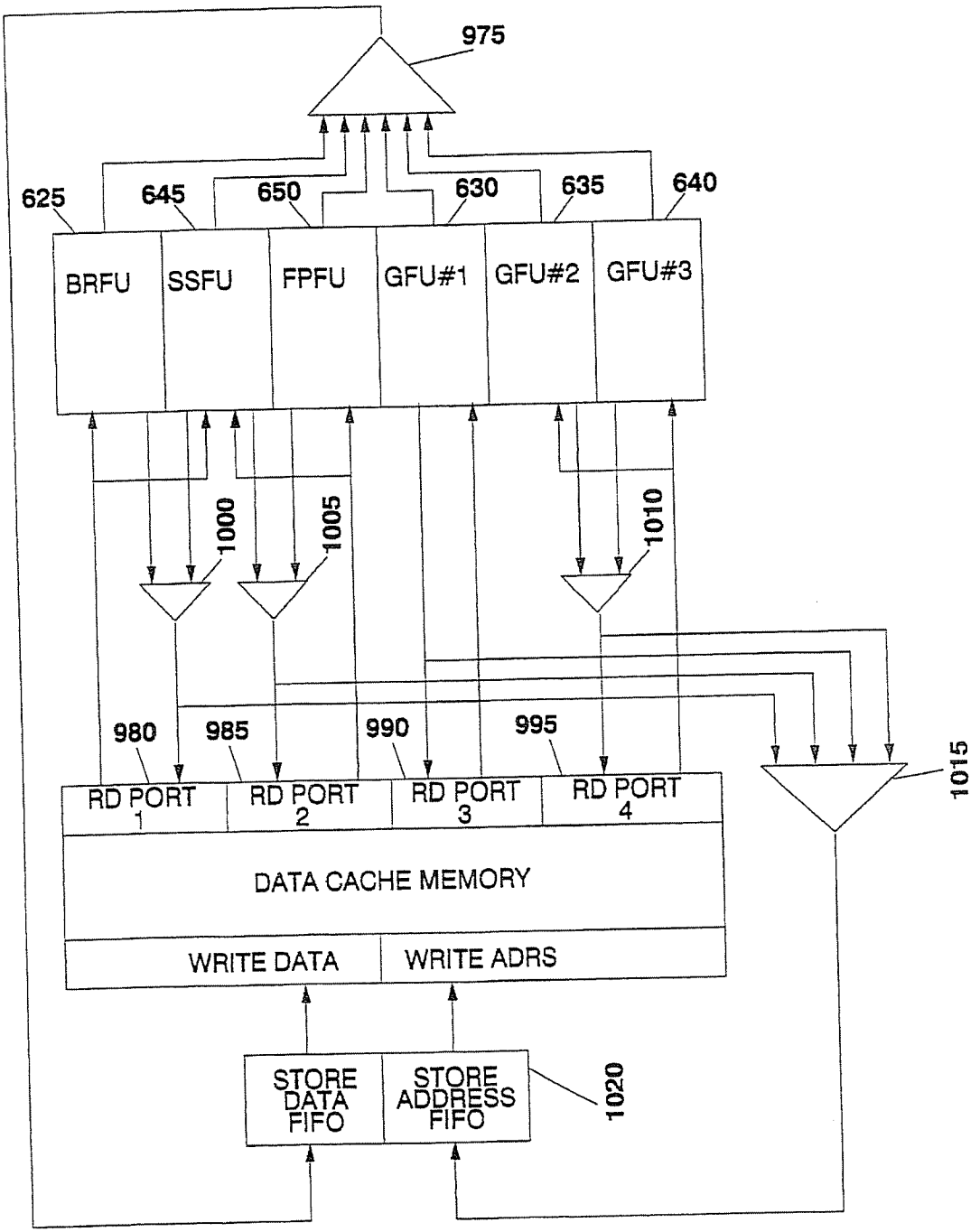


Figure 31h. Invention, IBM 370-XA Embodiment, VLSI Chip Gates and Pins

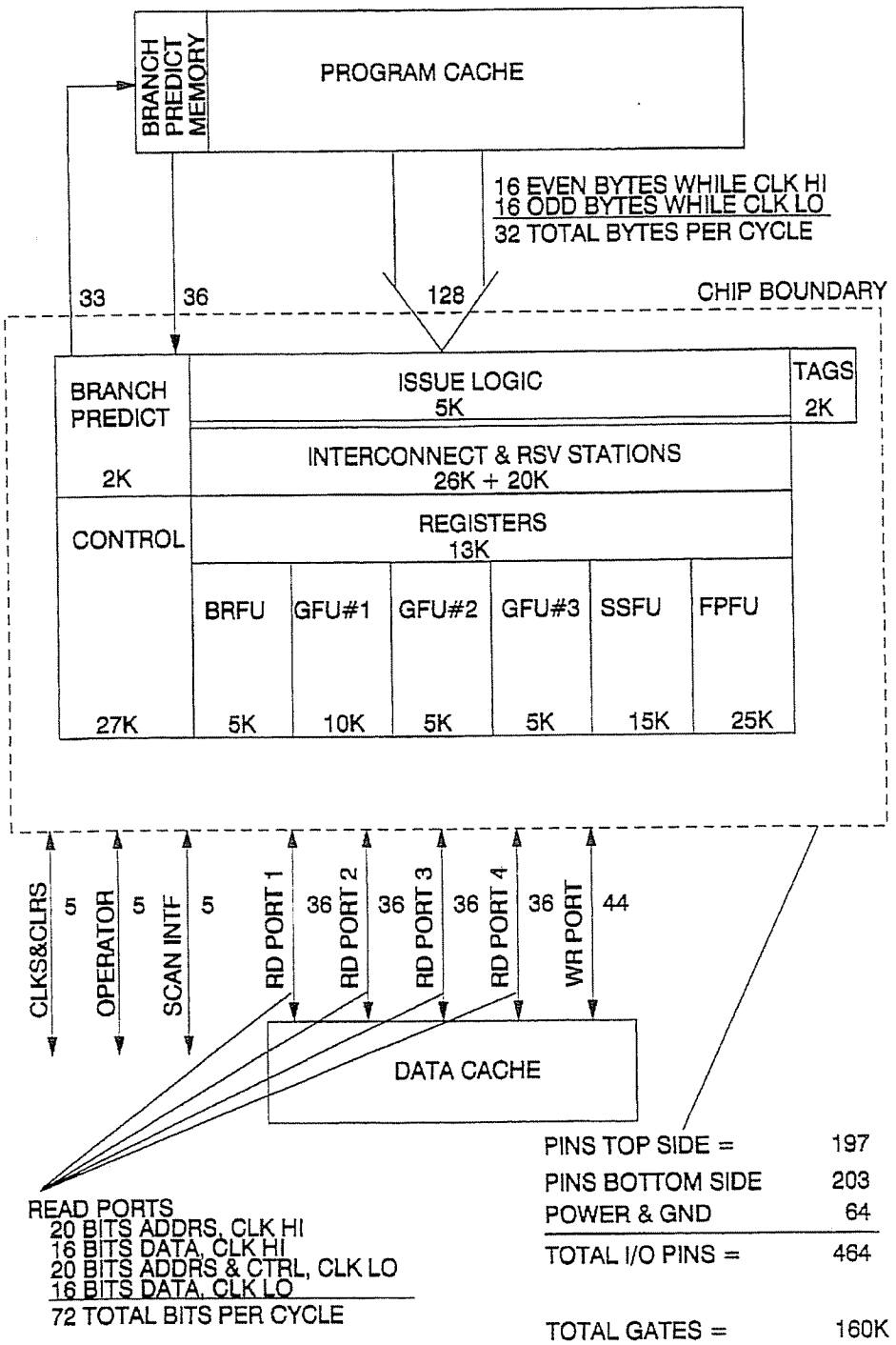


Figure 32. Invention,
Simple RISC Processor Embodiment

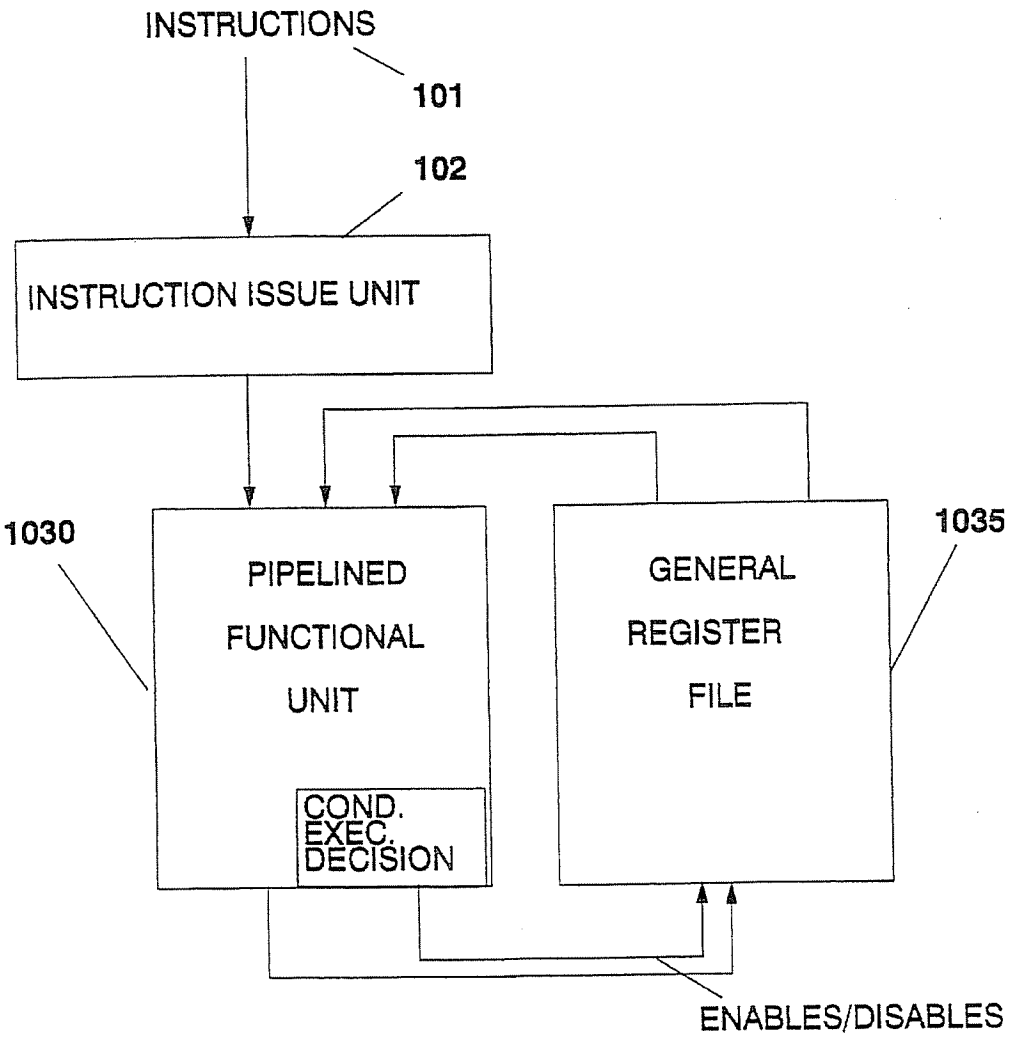


Figure 33. Invention,
Improved Registered Crossbar Processor

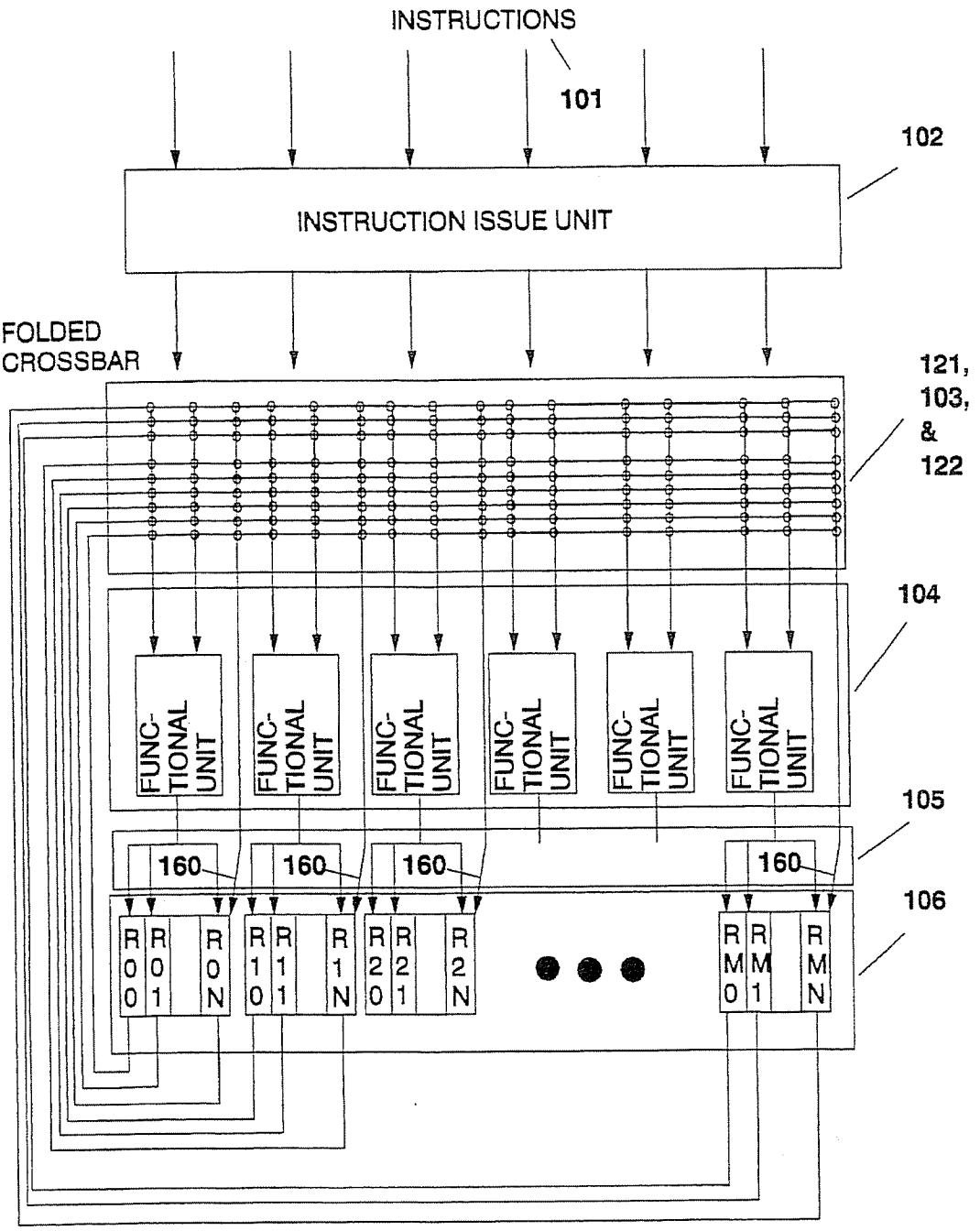


Figure 34a. Invention, Improved DSPA

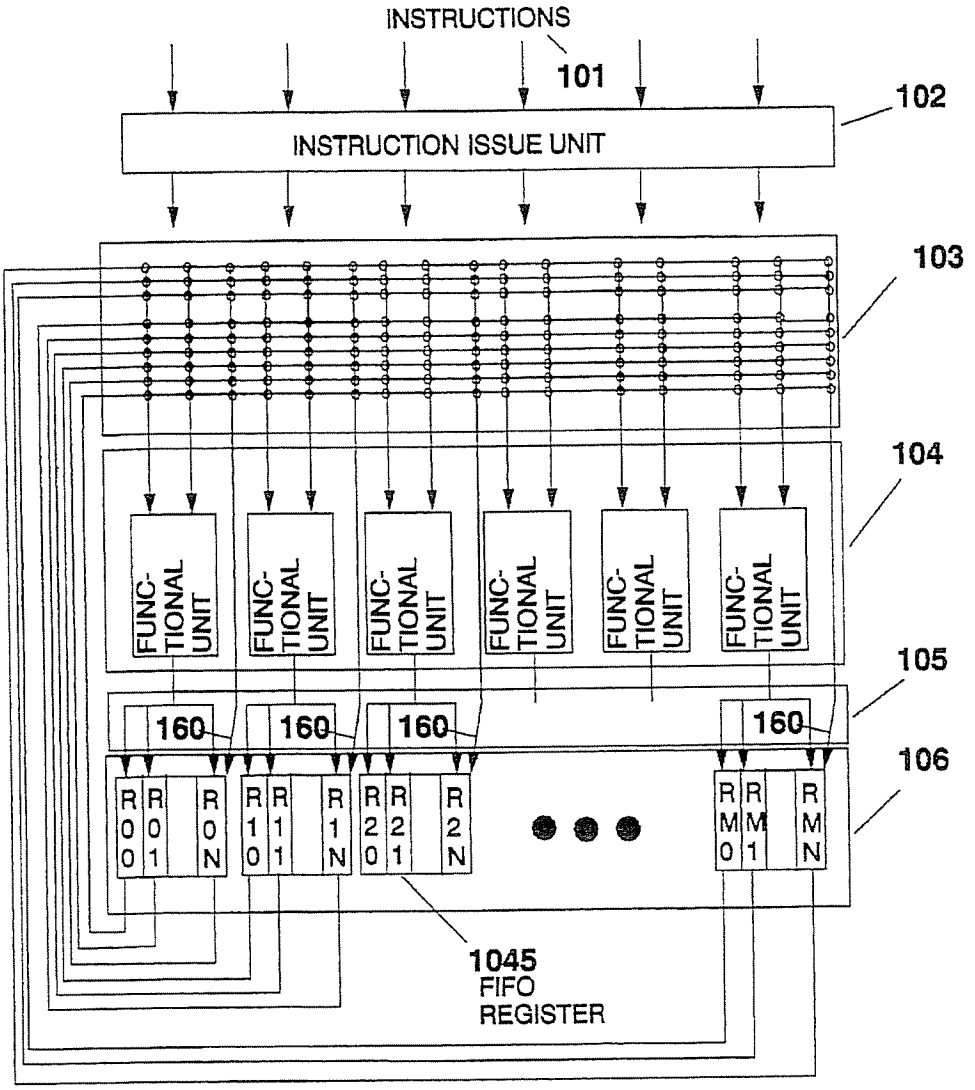


Figure 34b. Invention, FIFO Register File of Fig. 34a.

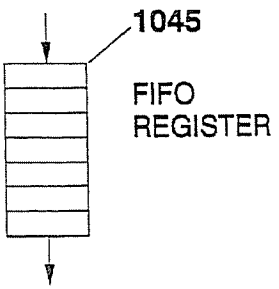


Figure 35a. Invention,
Improved Queue Based Vector Processor

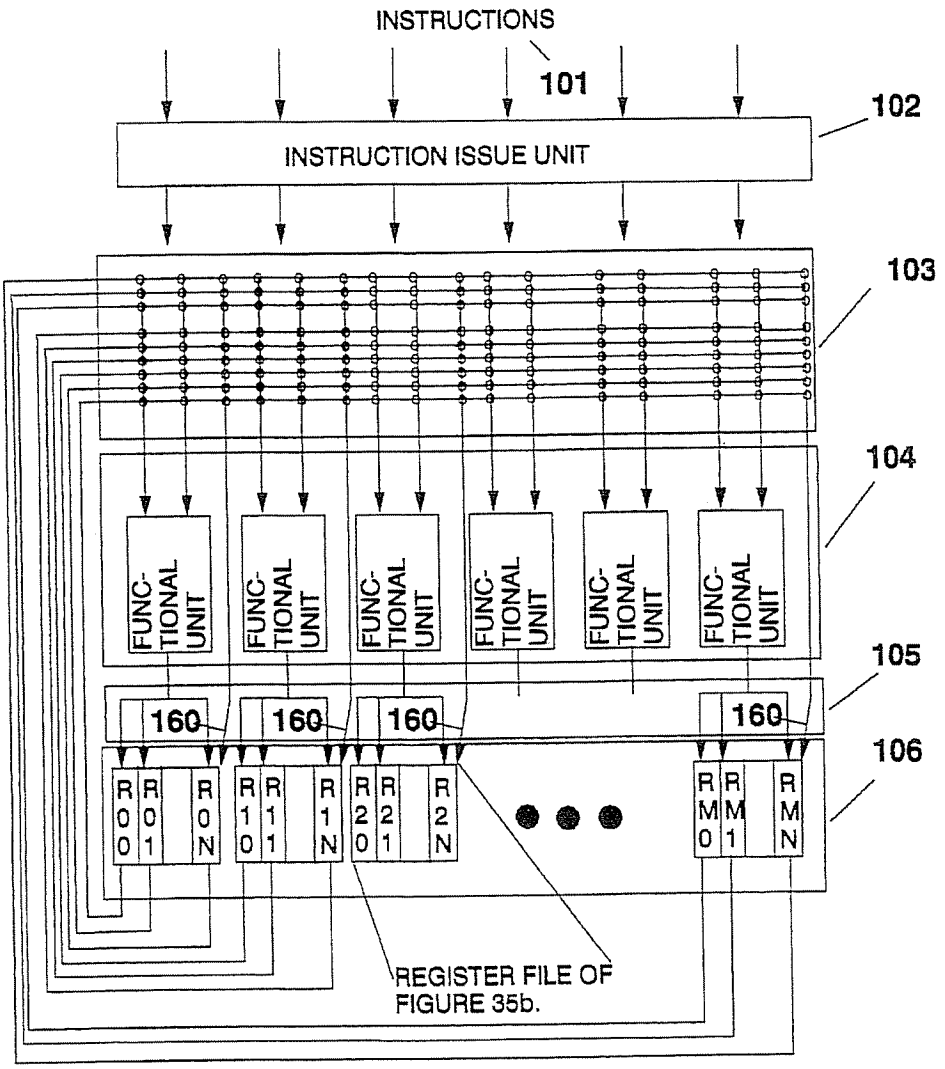


Figure 35b. Invention,
Register File of Fig. 35a.