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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACTICON TECHNOLOGIES LLC,

Plaintiff,

v.

PRETEC ELECTRONICS CORPORATION, a dissolved California corporation; PTI GLOBAL, INC., a California corporation; C-ONE TECHNOLOGY CORPORATION, a foreign corporation; CHIU FENG CHEN, an individual; GORDON YU, an individual; TOMMY HO, an individual; ROBERT WU, an individual; GRACE YU, an individual; KUEI LU, an individual; and DOES 1 through 20,

Defendants.

CASE NO. C 07-4507 JF (HRL)

FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT; SUCCESSOR LIABILITY; VICARIOUS LIABILITY; ALTER EGO; FRAUDULENT TRANSFERS (CIVIL CODE SECTION 3439, ET SEQ.); IMPROPER DISSOLUTION; CONSPIRACY

JURY TRIAL DEMANDED

Plaintiff ACTICON TECHNOLOGIES LLC, for its Complaint against Defendant PRETEC ELECTRONICS CORPORATION, Defendant PTI GLOBAL, INC., Defendant C-ONE TECHNOLOGY CORPORATION, Defendant CHIU FENG CHEN, Defendant GORDON YU, Defendant TOMMY HO, Defendant ROBERT WU, Defendant GRACE YU, Defendant KUEI LU and Defendants DOES 1 through 20, (collectively, "DEFENDANTS") alleges as follows:

INTRODUCTION

1. This action is brought by ACTICON TECHNOLOGIES LLC (hereinafter "ACTICON") against DEFENDANTS for damages arising out of Defendant PRETEC ELECTRONICS CORPORATION's ("PRETEC"), Defendant C-ONE TECHNOLOGY CORPORATION's ("C-ONE") and Defendant PTI GLOBAL, INC.'s infringement of certain ACTICON patents and for DEFENDANTS' fraudulent transfer of corporate assets in order to evade court process and avoid liability for such damages.

2. As set forth in detail below, ACTICON is the owner of the entire right, title and interest in U.S. Patent Nos. 4,603,320 (the "'320 Patent"); 4,543,450 (the "'450 Patent"); 4,972,470 (the "'470 Patent"); and 4,686,506 (the "'506 Patent") (collectively, the "Patents-in-Suit"), which describe various forms of electronic connectors. True and correct copies of the Patents-in-Suit are attached hereto as Exhibits "A," "B," "C," and "D," respectively.

3. PRETEC, prior to its dissolution on or about November 28, 2006, made, imported, offered for sale, sold and/or distributed various electronic connectors that embody the technology of the Patents-in-Suit.

4. ACTICON is informed and believes, and thereon alleges, that Defendants CHIU FENG CHEN, TOMMY HO, ROBERT WU, GORDON YU, GRACE YU, KUEI LU and DOES 1 through 20 were officers, directors and/or majority shareholders of PRETEC prior to PRETEC's dissolution.

5. Subsequent to PRETEC's dissolution on or about November 28, 2006, PRETEC and/or DEFENDANTS continued to make, import, offer for sale, sell and/or distribute various electronic connectors that embody the technology of the Patents-in-Suit as a manufacturer or distributor operating as the business entities PTI GLOBAL, INC. and/or the unknown business entities named as Defendants DOES 1 through 20.

6. At all times relevant hereto, C-ONE manufactured, imported, offered for sale, sold and/or distributed to PRETEC and PTI GLOBAL the various electronic connectors that embody the technology of the Patents-in-Suit which were sold, offered for sale and/or distributed by PRETEC and PTI GLOBAL.

7. PRETEC and/or DEFENDANTS continued to make, import, offer for sale, sell and/or distribute various electronic connectors that embody the technology of the Patents-in-Suit despite the fact that PRETEC received notice of the complaint for Patent Infringement in *Acticon Technologies LLC v. Pretec Electronics Corporation, et al.*, United States District Court Case No. C 06-4679 JF (HRL).

JURISDICTION

8. The Court has jurisdiction and supplemental jurisdiction over this matter because it is an infringement action arising under the United States Patent Act (35 U.S.C. § 271 *et seq.*). Accordingly, this Court has jurisdiction pursuant to 28 U.S.C. sections 1331 and 1338(a).

9. ACTICON is informed and believes, and thereon alleges, that DEFENDANTS are subject to personal jurisdiction in this District, because Defendant PTI GLOBAL, INC. is located in this District and PRETEC ELECTRONICS CORPORATION was located in this District prior to its dissolution. ACTICON is further informed and believes, and thereon alleges, that DEFENDANTS have caused tortious injury in this District by acts both inside and outside the District and regularly solicit business in this District or derive substantial revenue from sales of goods, including infringing goods in this District, or otherwise have engaged in a persistent course of conduct in this District.

VENUE

10. Venue is proper in this District pursuant to 28 U.S.C. § 1391 because PRETEC ELECTRONICS CORPORATION was headquartered in this District prior to its corporate dissolution and Defendant PTI GLOBAL, INC. is headquartered in this District.

INTRA-DISTRICT ASSIGNMENT

11. For the purposes of Civil L.R. 3-2(c) and (d), this Intellectual Property action may be assigned to any division of this District.

PARTIES

12. Plaintiff ACTICON is a limited liability company, which has its principal place of business in Suffern, New York.

13. ACTICON is informed and believes, and thereon alleges, that Defendant PRETEC was a California corporation, which had its principal place of business at 46791 Fremont Boulevard, Fremont, California, until its dissolution on or about November 28, 2006. Plaintiff is further informed and believes, and thereon alleges, that PRETEC designed, manufactured, marketed, distributed, imported, sold and/or offered for sale in the United States PCMCIA, CompactFlash and Secure Digital I/O form factor electronic connectors.

14. The products referenced above in paragraph 13 (hereinafter, the "Accused Products") employ an electronic connector that connects a computer and one or more external devices, whereby such electronic connector converts signals between the computer and external devices in order to obtain a desired connecting configuration and/or function.

15. ACTICON is informed and believes, and thereon alleges, that Defendant CHIU FENG CHEN was a Director of PRETEC. Plaintiff is informed and believes, and thereon alleges, that during the time that Defendant CHIU FENG CHEN worked in the capacity as a Director of PRETEC, he either resided and/or did business in or around Fremont, California.

16. ACTICON is informed and believes, and thereon alleges, that Defendant TOMMY HO was an Operations Manager for PRETEC. ACTICON is further informed and believes, and thereon alleges, that Defendant TOMMY HO also was a Director and/or Officer of Pretec Technology, Inc., which subsequently changed its corporate name to PTI GLOBAL, INC. Plaintiff is informed and believes, and thereon alleges, that during the time that Defendant TOMMY HO worked in the capacity as an Operations Manager and/or Director of PRETEC and as an Officer and/or Director of PTI GLOBAL, INC., he either resided and/or did business in or around Fremont, California.

17. ACTICON is informed and believes, and thereon alleges, that Defendant ROBERT WU was an Operations Manager for PRETEC. ACTICON is further informed and believes, and thereon alleges, that Defendant ROBERT WU also was a Director and/or Officer of Pretec

Technology, Inc., which subsequently changed its corporate name to PTI GLOBAL, INC. Plaintiff is informed and believes, and thereon alleges, that during the time that Defendant ROBERT WU worked in the capacity as an Operations Manager and/or Director of PRETEC and as an Officer and/or Director of PTI GLOBAL, INC., he either resided and/or did business in or around Fremont, California.

18. ACTICON is informed and believes, and thereon alleges, that Defendant PTI GLOBAL, INC. is a California corporation with its principal place of business located at 231 Whitney Place, Fremont, California. ACTICON is further informed and believes, and thereon alleges, that PTI GLOBAL, INC. was originally incorporated under the name Pretec Technology, Inc.

19. ACTICON is informed and believes, and thereon alleges, that Defendant PTI GLOBAL, INC. manufactures, uses, imports, distributes, offers for sale and/or sells PCMCIA, CompactFlash and Secure Digital I/O form factor electronic connectors under the PRETEC brand name.

20. ACTICON is informed and believes, and thereon alleges, that Defendant GRACE YU was the President, Secretary, Chief Executive Officer and Chief Financial Officer of Pretec Technology, Inc., which subsequently changed its name to PTI GLOBAL, INC., until in or about November 2006.

21. ACTICON is informed and believes, and thereon alleges, that Defendant KUEI LU has been the Chief Executive Officer, Secretary and Financial Officer of PTI GLOBAL, INC. since in or about November 2006.

22. ACTICON is informed and believes, and thereon alleges, that Defendant C-ONE TECHNOLOGY CORPORATION ("C-ONE") is a foreign corporation, which has its principal place of business in Taiwan. ACTICON is further informed and believes, and thereon alleges, that C-ONE has conducted, and continues to conduct, continuous business activity in the United States.

23. ACTICON is informed and believes, and thereon alleges, that C-ONE is or was a sister subsidiary company of PRETEC or C-ONE is the parent company of PRETEC.

24. ACTICON is informed and believes, and thereon alleges, that Defendant GORDON

YU was the President, a director, an officer and/or a majority shareholder of C-ONE during the period of time between 2002 through 2007, inclusive.

25. Plaintiff is informed and believes, and thereon alleges, that during a period of time prior to 2006, Defendant GORDON YU was the President of PRETEC and that Defendant GORDON YU was an officer, director and/or majority shareholder of PRETEC.

26. ACTICON is informed and believes, and thereon alleges, that at all relevant times hereto, C-ONE was in the business of designing, manufacturing, marketing, distributing, importing, selling and/or offering for sale in the United States PCMCIA, CompactFlash and Secure Digital I/O form factor electronic connectors.

27. ACTICON is informed and believes, and thereon alleges, that C-ONE imported, distributed, sold and/or offered for sale PCMCIA, CompactFlash and Secure Digital I/O form factor electronic connector products to PRETEC and PTI GLOBAL.

28. ACTICON is informed and believes, and thereon alleges, that DOES 1 through 20 were officers, directors and/or majority shareholders of PRETEC and/or are unknown business entities in the business of designing, manufacturing, marketing, distributing, importing, selling and/or offering for sale in the United States PCMCIA, CompactFlash and Secure Digital I/O form factor electronic connectors.

29. ACTICON is informed and believes, and thereon alleges, that at all times relevant hereto, each of the Defendants was the agent, affiliate or co-conspirator of the other defendants and in committing the acts hereinafter set forth, acted within the scope of such agency, affiliation or conspiracy and/or ratified or acquiesced in the acts of the other defendants.

30. ACTICON is unaware of the true names or capacities of remaining Defendants Does 1 through 20, whether corporate, individual, partner, employee, agent, co-conspirator, or otherwise, and prays leave of court to allege said true names and capacities when the same have been ascertained.

31. ACTICON is informed and believes, and thereon alleges, that in doing the things herein alleged, the named defendants and Does 1 through 20, inclusive, were each the agent, employee or servant of the remaining of said Defendants or that Defendants Does 1 through 20 are

in some other means or manner responsible for the acts and conduct hereinafter alleged.

GENERAL ALLEGATIONS

32. ACTICON is informed and believes, and thereon alleges, that PRETEC was named as a Defendant in the Complaint entitled *Acticon Technologies LLC v. Pretec Electronics Corp., et al*., filed on August 1, 2006, in the United States District Court for the Northern District of California, Case No. C 06-4679 JF (HRL) ("FIRST COMPLAINT"). ACTICON is informed and believes, and thereon further alleges, that Defendant ROBERT WU (as corporate representative of PRETEC) was personally served with the summons and FIRST COMPLAINT at 46791 Fremont Boulevard, Fremont, California, on or about August 17, 2006.

33. PRETEC did not respond to the FIRST COMPLAINT on or before September 6, 2006, the deadline for PRETEC to answer or otherwise respond to the FIRST COMPLAINT.

34. On or about September 13, 2006, ACTICON filed a Request for Entry of Default against PRETEC. On or about September 15, 2006, ACTICON filed a Second Request for Entry of Default against PRETEC.

35. On September 19, 2006, the Clerk of the United States District Court, Northern District of California entered the default of PRETEC in *Acticon Technologies LLC v. Pretec Electronics Corp., et al*., Case No. C 06-4679 JF (HRL), as Docket Entry 13.

36. On or about October 5, 2006, counsel for ACTICON sent a letter to PRETEC via certified U.S. mail advising that ACTICON would request entry of default judgment against PRETEC if PRETEC did not respond to ACTICON's communication on or before October 11, 2006. PRETEC did not respond to ACTICON's October 5, 2006 letter.

37. Notwithstanding the default entered against PRETEC, on or about October 19, 2006, PRETEC filed a motion captioned, "Motion to Change Time," requesting a sixty-day continuance of the November 29, 2006 Case Management Conference in *Acticon Technologies LLC v. Pretec Electronics Corp., et al*., Case No. C 06-4679 JF (HRL), (Docket Entry 21). This motion was signed by Defendant TOMMY HO and Defendant GORDON YU. A true and correct copy of the Motion to Change Time is attached hereto as Exhibit "E", and incorporated by reference.

38. On October 24, 2006, Defendant TOMMY HO contacted counsel for ACTICON via telephone. The following day, in a telephone conference between counsel for ACTICON and Defendant TOMMY HO, Defendant TOMMY HO requested a description of the Accused Products in the FIRST COMPLAINT and agreed to provide ACTICON with six years of annual sales information for PRETEC's Accused Products.

39. On October 26, 2007, Defendant TOMMY HO wrote in an e-mail message to counsel for ACTICON, "Thanks for the information. We will study the accused products as you claimed. If we agree, then we will prepare the past years of sales information. If we disagree on some of the accused products, we will contact you to discuss. We will try to get as much sales information as possible."

40. Based on Defendant TOMMY HO's agreement on behalf of PRETEC to provide sales information for the Accused Products to ACTICON, ACTICON did not oppose PRETEC's Motion to Change Time and filed a Statement of Non-Opposition to Pretec's Motion to Change Time on October 27, 2007 in *Acticon Technologies LLC v. Pretec Electronics Corp., et al*., Case No. C 06-4679 JF (HRL), (Docket Entry 22).

41. That same day, October 27, 2007, Pretec Technology, Inc. filed a Certificate of Amendment of Articles of Incorporation with the California Secretary of State to change its corporate name to PTI GLOBAL, INC.,

42. On or about October 31, 2006, the Court granted PRETEC's motion in *Acticon Technologies LLC v. Pretec Electronics Corp., et al*., Case No. C 06-4679 JF (HRL), and continued the initial Case Management Conference scheduled for November 29, 2006 to February 2, 2007. (Docket Entry 24).

43. On or about November 28, 2006, one day prior to the originally scheduled Case Management Conference, PRETEC filed a Certificate of Dissolution in the office of the Secretary of State of California. A true and correct copy of the Certificate of Dissolution is attached hereto as Exhibit "F". Despite PRETEC having been placed on actual notice of the patent infringement lawsuit pending against it in the United States District Court for the Northern District of California, Defendant CHIU FENG CHEN certified and declared under penalty of perjury in the Certificate of

Dissolution that, *inter alia*, "THE CORPORATION'S KNOWN DEBTS AND LIABILTIES HAVE BEEN ACTUALLY PAID."

44. PRETEC did not appear at the February 2, 2007 Case Management Conference in *Acticon Technologies LLC v. Pretec Electronics Corp., et al*., Case No. C 06-4679 JF (HRL).

45. ACTICON is informed and believes, and thereon alleges, that Defendants PTI GLOBAL, INC., C-ONE, CHIU FENG CHEN, ROBERT WU, TOMMY HO, KUEI LU, GRACE YU, GORDON YU and DOES 1 through 20 and each of them, continue to make, use, import, distribute, offer for sale and/or sell the Accused Products, and possibly other products that infringe the Patents-in-Suit, in the United States through Defendant PTI GLOBAL, INC..

46. ACTICON is informed and believes, and thereon alleges, that Defendants PTI GLOBAL, INC., C-ONE, CHIU FENG CHEN, ROBERT WU, TOMMY HO, KUEI LU, GRACE YU, GORDON YU and DOES 1 through 20 and each of them, continue to make, use, import, distribute, offer for sale and/or sell the Accused Products, and possibly other products that infringe the Patents-in-Suit, in the United States through one or more unknown business entities.

47. ACTICON is informed and believes, and thereon alleges, that DEFENDANTS fraudulently transferred nearly all of PRETEC's assets to Defendants PTI GLOBAL, INC. and/or C-ONE in order to continue operating PRETEC's business, including the manufacture, distribution and sale of PCMCIA, CompactFlash and Secure Digital I/O form factor electronic connectors in the United States, after PRETEC's corporate dissolution.

GENERAL PATENT CLAIMS ALLEGATIONS

48. ACTICON is the sole and exclusive owner of United States Patent No. 4,603,320, issued on July 29, 1986, entitled "Connector Interface."

49. ACTICON is the sole and exclusive owner of United States Patent No. 4,543,450, issued on September 24, 1985, entitled "Integrated Connector and Modem."

50. ACTICON is the sole and exclusive owner of United States Patent No 4,972,470, issued on November 20, 1990 entitled "Programmable Connector."

51. ACTICON is the sole and exclusive owner of United States Patent No. 4,686,506,

issued on August 11, 1987, entitled "Multiple Connector Interface."

52. The Patents-in-Suit describe various electronic connectors that convert signals between a computer and certain external devices in order to obtain a desired connecting configuration and/or function.

53. ACTICON is informed and believes, and thereon alleges, that prior to on or about November 28, 2006, PRETEC made, used, imported, distributed, offered for sale and/or sold certain products in the United States that infringe upon the Patents-in-Suit, including, but not limited to, CompactFlash form factor I/O devices such as Ethernet and Modem cards, Secure Digital form factor I/O devices such as the Whanto Modem, PCMCIA form factor devices such as Ethernet, Modem and Combo cards, as well as other CompactFlash, SDIO and PCMCIA form factor devices which may be further identified during the course of discovery.

54. Despite PRETEC having been placed on actual notice as to its infringing activity prior to the filing of the FIRST COMPLAINT, PRETEC and/or DEFENDANTS, and each of them, continued to refuse to cease and desist from their manufacture, distribution, importation, sale, or offer for sale of the above-referenced Accused Products, and refused to enter into any licensing agreements with ACTICON.

55. After the filing of the FIRST COMPLAINT in *Acticon Technologies LLC v. Pretec Electronics Corp., et al*., Case No. C 06-4679 JF (HRL), PRETEC and/or DEFENDANTS, and each of them, failed and/or refused to cease and desist from their manufacture, distribution, importation, sale, or offer for sale of the above-referenced Accused Products, and refused to enter into any licensing agreements with ACTICON.

56. ACTICON is informed and believes, and thereon alleges, that after PRETEC's alleged dissolution on or about November 28, 2006, PTI GLOBAL, INC., the successor to PRETEC, continued to make, use, import, distribute, offer for sale and/or sell certain PRETEC brand products in the United States that infringe upon the Patents-in-Suit, including, but not limited to, PRETEC brand CompactFlash form factor I/O devices such as Ethernet and Modem cards, Secure Digital form factor I/O devices such as the Whanto Modem, PCMCIA form factor devices such as Ethernet, Modem and Combo cards, as well as other CompactFlash, SDIO and PCMCIA

form factor devices which may be further identified during the course of discovery.

57. ACTICON is informed and believes, and thereon alleges, that after PRETEC's dissolution on or about November 28, 2006, Defendants CHIU FENG CHEN, TOMMY HO, ROBERT WU, KUEI LU, GRACE YU, GORDON YU and DOES 1 through 20, on behalf of PTI GLOBAL, INC. and/or DOES 1 through 20, continued to make, use, import, distribute, offer for sale and/or sell certain PRETEC brand products in the United States that infringe upon the Patents-in-Suit, including, but not limited to, PRETEC brand CompactFlash form factor I/O devices such as Ethernet and Modem cards, Secure Digital form factor I/O devices such as the Whanto Modem, PCMCIA form factor devices such as Ethernet, Modem and Combo cards, as well as other CompactFlash, SDIO and PCMCIA form factor devices which may be further identified during the course of discovery.

COUNT I

Direct Infringement – All Patents-in-Suit
(Against C-ONE)

58. ACTICON repeats and realleges each of the allegations set forth in paragraphs 1 through 57, as though fully set forth herein.

59. ACTICON is informed and believes, and thereon alleges, that C-ONE makes, uses, imports, distributes, offers for sale and/or sells the Accused Products, and possibly other products that infringe the Patents-in-Suit, and will continue to do so unless enjoined by this Court.

60. C-ONE's conduct in making, using, importing, distributing, offering for sale and/or selling the Accused Products, and possibly other infringing products, constitutes an infringement of ACTICON'S rights under the Patents-in-Suit.

61. ACTICON is informed and believes, and thereon alleges, that C-ONE is actively inducing others to infringe, and/or committing acts of contributory infringement of one or more claims of the Patents-in-Suit, through its activities related to making, using, importing, distributing, offering for sale and/or selling the Accused Products, all in violation of 35 U.S.C. § 271.

62. ACTICON has been damaged by C-ONE's infringing conduct, and C-ONE is therefore liable to ACTICON for actual damages suffered by ACTICON, and any profits realized

on the sale of the Accused Products which are not taken into account in the computation of actual damages, as well as any statutory damages, such as treble damages. Moreover, such conduct is likely to cause substantial harm to ACTICON, unless this Court enjoins the infringing conduct.

63. ACTICON is informed and believes, and thereon alleges, that C-ONE's infringement of the Patents-in-Suit has been, and continues to be, willful and deliberate.

WHEREFORE, ACTICON seeks relief as set forth in the Prayer, below.

COUNT II

Successor Liability – All Patents-in-Suit
(Against PTI GLOBAL and C-ONE)

64. ACTICON repeats and realleges each of the allegations set forth in paragraphs 1 through 63, as though fully set forth herein.

65. ACTICON is informed and believes, and thereon alleges, that prior to PRETEC'S dissolution on or about November 28, 2006, PRETEC made, used, imported, distributed, offered for sale and/or sold the Accused Products, and possibly other products that infringe the Patents-in-Suit through PTI GLOBAL, INC., and/or DOES 1 through 20.

66. ACTICON is informed and believes, and thereon alleges, that PRETEC and PTI GLOBAL, INC. share the same shareholders and directors.

67. ACTICON is informed and believes, and thereon alleges, that PRETEC transferred its assets to PTI GLOBAL and/or C-ONE for the fraudulent and wrongful purpose of avoiding liability on the claims ACTICON asserted against PRETEC in the FIRST COMPLAINT in *Acticon Technologies LLC v. Pretec Electronics Corp., et al*., Case No. C 06-4679 JF (HRL).

68. ACTICON is informed and believes, and thereon alleges, that PTI GLOBAL, INC. is a mere continuation of PRETEC. ACTICON is further informed and believes, and thereon alleges, that PTI GLOBAL, INC. carries on the same business that PRETEC was engaged in prior to PRETEC's dissolution, namely the manufacture, use, importation, distribution, offering for sale and/or selling of PCMCIA, CompactFlash and Secure Digital I/O form factor electronic connectors.

69. ACTICON is informed and believes, and thereon alleges, that PTI GLOBAL, INC. continues to make, use, import, distribute, offer for sale and/or sell the Accused Products under the

PRETEC brand, and possibly other products that infringe the Patents-in-Suit. ACTICON is informed and believes, and thereon alleges, that PTI GLOBAL, INC. sells exclusively PRETEC products, including, but not limited to, the Accused Products.

70. ACTICON is informed and believes, and thereon alleges, that PTI GLOBAL, INC. sells PRETEC products online at various locations on the world wide web, including, but not limited to, PTI GLOBAL, INC.'s web site, located at www.ptiglobalusa.com. The homepage of PTI GLOBAL, INC.'s web site contains the header, "Flash Memory Innovation by PRETEC."

71. ACTICON is informed and believes, and thereon alleges, that PTI GLOBAL, INC. also sells PRETEC products online at PTI GLOBAL, INC.'s storefront in Amazon.com's online marketplace, located at http://www.amazon.com/shops/pti_global. The "About PTI Global Inc." section of PTI GLOBAL, INC.'s storefront, states, "Since 1993, PRETEC brand has been recognized internationally for it's [sic] experience in pioneering innovative and quality products offered to the data storage, mobile computing and industrial markets. PRETEC brand is focused on global markets providing it's [sic] full-line of own brand-name products: USB device storage, Flash memory Card storage, Multi-Media solution, Mobile Peripherals, Multi-Function, Industrial storage and Accessory. PRETEC brand products with unique ID design and highest reliability create PRETEC's winning formula, reaching the customer's needs and enhancing your digital world."

72. ACTICON is informed and believes, and thereon alleges, that PTI GLOBAL, INC.'s web site lists PTI GLOBAL, INC.'s address as "231 Whitney Place, Fremont, CA 94539" and lists PTI GLOBAL, INC.'s telephone number as "510-249-9055." *See http://www.ptiglobalusa.com/info.html*. ACTICON is informed and believes, and thereon alleges, that the Technical Contact for PRETEC listed on the WHOIS record for "pretec.com" is an individual whose address is "231 Whitney Place, Fremont, CA 94539" and whose telephone number is "510-249-9055."

73. ACTICON is informed and believes, and thereon alleges, that an Internet search for "Pretec Electronics Corporation" in "Fremont, California," performed at the web site www.google.com/maps returns an address of "231 Whitney Place, Fremont, CA 94539" and a

phone number of "(510) 249-9055." ACTICON is informed and believes, and thereon alleges, that an Internet search for "Pretec Electronics Corporation" in "Fremont, California," performed at the web site www.maps.yahoo.com also returns an address of "231 Whitney Place, Fremont, CA 94539" and a phone number of "(510) 249-9055."

74. ACTICON is informed and believes, and thereon alleges, that PTI GLOBAL, INC. is a successor corporation to PRETEC. ACTICON is informed and believes, and thereon alleges, that (1) PTI GLOBAL INC. shares practically the same shareholders and directors as PRETEC; (2) that PRETEC transferred substantially all of its assets to PTI GLOBAL, INC. and/or C-ONE, but neither PTI GLOBAL, INC. nor C-ONE paid certain of PRETEC's debts or liabilities; and (3) that PTI GLOBAL, INC. carries on the same business as PRETEC conducted prior to PRETEC's dissolution.

75. PRETEC's conduct in making, using, importing, distributing, offering for sale and/or selling the Accused Products, and possibly other infringing products, constituted an infringement of ACTICON'S rights under the Patents-in-Suit.

76. ACTICON has been damaged by PRETEC's infringing conduct, and as PRETEC's successor, PTI GLOBAL, INC. therefore is liable to ACTICON for actual damages suffered by ACTICON and any profits realized on the sale of the Accused Products which are not taken into account in the computation of actual damages, as well as any statutory damages, such as treble damages.

77. ACTICON is informed and believes, and thereon alleges, that PRETEC's infringement of the Patents-in-Suit prior to PRETEC's dissolution was willful and deliberate.

WHEREFORE, ACTICON seeks relief as set forth in the Prayer, below.

COUNT III

Patent Infringement (Alter Ego) – All Patents-in-Suit
(Against CHIU FENG CHEN, TOMMY HO, ROBERT WU, GRACE YU, KUEI LU and GORDON YU)

78. ACTICON repeats and realleges each of the allegations set forth in paragraphs 1 through 77, as though fully set forth herein.

79. ACTICON is informed and believes, and thereon alleges, that Defendants CHIU

FENG CHEN, TOMMY HO, ROBERT WU, GRACE YU, KUEI LU and GORDON YU (hereinafter collectively "INDIVIDUAL DEFENDANTS") were officers, directors and/or majority shareholders of PRETEC.

80. ACTICON is informed and believes, and thereon alleges, that the INDIVIDUAL DEFENDANTS, and each of them, are the alter ego of PRETEC in that the INDIVIDUAL DEFENDANTS, among other actions and omissions: (1) commingled funds and other assets, failed to segregate funds of separate entities, and made unauthorized diversions of corporate funds and assets to other than corporate uses; (2) treated the assets of PRETEC as their own; (3) failed to maintain minutes and adequate corporate records and caused the confusion of the records of separate entities; (4) used PRETEC as a mere shell, instrumentality and conduit for a single venture and business of their own device; (5) disregarded the legal formalities of the corporation, and failed to maintain arms-length relationships with PRETEC and their other affiliate entities; (6) used PRETEC's corporate entity to procure labor, services and merchandise for their own benefit and the benefit of their other affiliated entities; and (7) diverted assets of PRETEC to themselves and/or their other affiliated entities, including C-ONE, to the detriment of PRETEC's creditors.

81. ACTICON is informed and believes, and thereon alleges, that PRETEC was influenced and governed by the INDIVIDUAL DEFENDANTS and that there is such a unity of interest and ownership that the individuality, or separateness of PRETEC and the INDIVIDUAL DEFENDANTS has ceased and that the INDIVIDUAL DEFENDANTS are the alter ego of PRETEC. ACTICON is further informed and believes, and thereon alleges, that the facts are such that an adherence to the fiction of the separate existence of the PRETEC corporation from the INDIVIDUAL DEFENDANTS would sanction fraud and promote injustice.

82. ACTICON is informed and believes, and thereon alleges, that the INDIVIDUAL DEFENDANTS, in their capacities as officers, directors and/or majority shareholders of PRETEC, had been placed on notice of the FIRST COMPLAINT in *Acticon Technologies LLC v. Pretec Electronics Corp., et al*., Case No. C 06-4679 JF (HRL), and of PRETEC's alleged infringing activity.

83. ACTICON is informed and believes, and thereon alleges, that despite the

INDIVIDUAL DEFENDANTS having been placed on notice of the FIRST COMPLAINT, the INDIVIDUAL DEFENDANTS continued to allow and/or assented to PRETEC's making, using, importing, distributing, offering for sale and/or selling the Accused Products.

84. PRETEC's conduct in making, using, importing, distributing, offering for sale and/or selling the Accused Products, and possibly other infringing products, constituted an infringement of ACTICON'S rights under the Patents-in-Suit.

85. ACTICON is informed and believes, and thereon alleges, that the INDIVIDUAL DEFENDANTS actively induced others to infringe, and/or commit acts of contributory infringement of one or more claims of the Patents-in-Suit, through their activities related to making, using, importing, distributing, offering for sale and/or selling the Accused Products, all in violation of 35 U.S.C. § 271.

86. ACTICON has been damaged by PRETEC's infringing conduct, and as the officers, directors and/or majority shareholders of PRETEC, the INDIVIDUAL DEFENDANTS therefore are liable to ACTICON for actual damages suffered by ACTICON, and any profits realized on the sale of the Accused Products which are not taken into account in the computation of actual damages, as well as any statutory damages, such as treble damages.

87. ACTICON is informed and believes, and thereon alleges, that PRETEC's infringement of the Patents-in-Suit prior to PRETEC's dissolution was willful and deliberate.

88. ACTICON has been damaged by the actions of the INDIVIDUAL DEFENDANTS in that the INDIVIDUAL DEFENDANTS have transferred the assets and corporate funds of PRETEC to deprive PRETEC of the monies and ability to meet its obligations for liability under the FIRST COMPLAINT in *Acticon Technologies LLC v. Pretec Electronics Corp., et al*., Case No. C 06-4679 JF (HRL).

89. ACTICON hereby asserts its claim to recovery of any sums not paid by PRETEC for PRETEC's infringing conduct against the officer, director and majority shareholder INDIVIDUAL DEFENDANTS.

WHEREFORE, ACTICON seeks relief as set forth in the Prayer, below.

COUNT IV

Patent Infringement (Vicarious Liability) – All Patents-in-Suit (Against CHIU FENG CHEN, TOMMY HO, ROBERT WU, GRACE YU, KUEI LU and GORDON YU)

90. ACTICON repeats and realleges each of the allegations set forth in paragraphs 1 through 89, as though fully set forth herein.

91. ACTICON is informed and believes, and thereon alleges, that the INDIVIDUAL DEFENDANTS fraudulently and wrongfully transferred the assets of PRETEC to PTI GLOBAL, INC. and/or C-ONE and committed other acts not yet known to Plaintiff in order to avoid liability on the claims asserted against PRETEC in the FIRST COMPLAINT in *Acticon Technologies LLC v. Pretec Electronics Corp., et al*., Case No. C 06-4679 JF (HRL).

92. ACTICON is informed and believes, and thereon alleges, that the INDIVIDUAL DEFENDANTS are the officers, directors and/or majority shareholders of PTI GLOBAL, INC.

93. ACTICON is informed and believes, and thereon alleges, that PTI GLOBAL, INC.'s infringement of the Patents-in-Suit subsequent to PRETEC's dissolution has been and continues to be willful and deliberate.

94. ACTICON has been damaged by the actions of the INDIVIDUAL DEFENDANTS in that the INDIVIDUAL DEFENDANTS have transferred substantially all of the assets and corporate funds of PRETEC to deprive PRETEC of the monies and ability to meet its obligations for liability under the FIRST COMPLAINT in *Acticon Technologies LLC v. Pretec Electronics Corp., et al*., Case No. C 06-4679 JF (HRL).

95. ACTICON hereby asserts its claim to recovery of any sums not paid by PRETEC for PRETEC's infringing conduct against the officer, director and majority shareholder INDIVIDUAL DEFENDANTS.

WHEREFORE, ACTICON seeks relief as set forth in the Prayer, below.

COUNT V

Fraudulent Transfer – Civil Code § 3439 et seq. (Against ALL DEFENDANTS)

96. ACTICON repeats and realleges each of the allegations set forth in paragraphs 1

through 95, as though fully set forth herein.

97. ACTICON is informed and believes, and thereon alleges, that PRETEC, PTI GLOBAL, INC., C-ONE and/or the INDIVIDUAL DEFENDANTS fraudulently transferred PRETEC's assets to C-ONE and/or PTI GLOBAL, INC. with the intent to hinder, delay or defraud ACTICON in pursuing its claims arising out of the FIRST COMPLAINT against PRETEC in *Acticon Technologies LLC v. Pretec Electronics Corp., et al.*, Case No. C 06-4679 JF (HRL).

98. ACTICON is informed and believes, and thereon alleges, that in order to remove its assets and conceal the transfer of its assets, PRETEC filed for corporate dissolution with the California Secretary of State in November 2006.

99. ACTICON is informed and believes, and thereon alleges, that PRETEC, PTI GLOBAL, INC. and/or the INDIVIDUAL DEFENDANTS transferred substantially all of PRETEC's assets to PTI GLOBAL, INC. and/or C-ONE without receiving a reasonably equivalent value in exchange for the transfer and were engaged in a transaction (or series of transactions) for which its remaining assets were unreasonably small in relation to the transactions.

100. ACTICON is informed and believes, and thereon alleges, that PTI GLOBAL, INC. shares the same officers, directors and majority shareholders as the officers, directors and majority shareholders that PRETEC possessed prior to PRETEC's dissolution.

101. ACTICON is informed and believes, and thereon alleges, that the INDIVIDUAL DEFENDANTS were officers, directors and/or majority shareholders of PRETEC prior to PRETEC's dissolution in or about November 2006. ACTICON is informed and believes, and thereon alleges, that the INDIVIDUAL DEFENDANTS were officers, directors and/or majority shareholders of C-ONE prior to PRETEC's dissolution in or about November 2006.

102. ACTICON is informed and believes, and thereon alleges, that the INDIVIDUAL DEFENDANTS are the officers, directors and/or majority shareholders of PTI GLOBAL, INC.

103. ACTICON is informed and believes, and thereon alleges, that PRETEC did not cease its business operations despite filing a Certificate of Corporate Dissolution with the California Secretary of State. ACTICON is informed and believes, and thereon alleges, that

PRETEC continues to do business in the United States under the PRETEC ELECTRONICS CORPORATION brand and name and also does business as PTI GLOBAL, INC.

104. ACTICON is informed and believes, and thereon alleges, that PTI GLOBAL, INC. sells only PRETEC brand products on its web site, located at www.ptiglobalusa.com. ACTICON is further informed and believes, and thereon alleges, that PTI GLOBAL, INC.'s web site was registered in or about February 2007, approximately two months after PRETEC's dissolution.

105. ACTICON is further informed and believes, and thereon alleges, that PRETEC issued a press release on or about April 4, 2007, announcing its new Ruggedized Industrial CompactFlash card. A true and correct copy of the April 4, 2007 press release is attached hereto as Exhibit "G", and incorporated by reference.

106. ACTICON is informed and believes, and thereon alleges, that PTI GLOBAL, INC. has been and continues to be PRETEC's United States company headquarters office.

107. ACTICON is informed and believes, and thereon alleges, that C-ONE was a transferee of PRETEC's fraudulently transferred assets and did not receive a reasonably equivalent value in exchange for the transfer.

108. ACTICON has been damaged by PRETEC's, C-ONE's and/or the INDIVIDUAL DEFENDANTS' fraudulent and wrongful transfer of assets to PTI GLOBAL, INC. and/or C-ONE, which prevents ACTICON from collecting any monies due to ACTICON for PRETEC's liabilities under the FIRST COMPLAINT in *Acticon Technologies LLC v. Pretec Electronics Corp., et al.*, Case No. C 06-4679 JF (HRL).

109. ACTICON hereby asserts its claim to recovery of any sums not paid by PRETEC ELECTRONICS CORPORATION against the officer, director and majority shareholder INDIVIDUAL DEFENDANTS, C-ONE and PTI GLOBAL.

WHEREFORE, ACTICON seeks relief as set forth in the Prayer, below.

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COUNT VI

Conspiracy to Fraudulently Transfer Assets
(Against ALL DEFENDANTS)

110. ACTICON repeats and realleges each of the allegations set forth in paragraphs 1 through 109, as though fully set forth herein.

111. ACTICON is informed and believes, and thereon alleges, that DEFENDANTS agreed to engage in and engaged in a common course of conduct to fraudulently transfer PRETEC's assets to PTI GLOBAL, INC. and/or C-ONE with the intent to hinder, delay or defraud ACTICON in pursuing its claims against PRETEC arising out of the FIRST COMPLAINT in *Acticon Technologies LLC v. Pretec Electronics Corp., et al*., Case No. C 06-4679 JF (HRL).

112. ACTICON is informed and believes, and thereon alleges, that in furtherance of the conspiracy, DEFENDANTS transferred PRETEC's assets without receiving a reasonably equivalent value in exchange for the transfer and were engaged in a transaction (or series of transactions) for which PRETEC's remaining assets were unreasonably small in relation to the transactions.

113. ACTICON is informed and believes, and thereon alleges, that DEFENDANTS committed the acts described in paragraphs 111and 112 intentionally and in furtherance of the conspiracy to commit the unlawful transfer of PRETEC's assets.

114. As a result of the above-described fraudulent conveyance, ACTICON has been damaged in an amount according to proof at trial.

WHEREFORE, ACTICON seeks relief as set forth in the Prayer, below.

COUNT VII

Improper Dissolution
(Against ALL DEFENDANTS)

115. ACTICON repeats and realleges each of the allegations set forth in paragraphs 1 through 114, as though fully set forth herein.

116. ACTICON is informed and believes, and thereon alleges, that the INDIVIDUAL DEFENDANTS and/or DOES 1 THROUGH 20 participated in a voluntary proceeding for winding

up PRETEC.

117. ACTICON is informed and believes, and thereon alleges, that PRETEC failed to cease business, all in violation of California Corporations Code Section 1903(c).

118. ACTICON is informed and believes, and thereon alleges, that PRETEC improperly filed for corporate dissolution with the California Secretary of State despite knowing of PRETEC's potential liabilities under the claims set forth in the FIRST COMPLAINT in *Acticon Technologies LLC v. Pretec Electronics Corp., et al.*, Case No. C 06-4679 JF (HRL).

119. ACTICON is informed and believes, and thereon alleges, that PRETEC fraudulently signed a certificate of dissolution stating that PRETEC's known debts and liabilities have been actually paid, or adequately provided for, or paid or adequately provided for as far as its assets permitted or that it has incurred no known debts or liabilities when in fact, PRETEC's liabilities under the claims set forth in the FIRST COMPLAINT in *Acticon Technologies LLC v. Pretec Electronics Corp., et al.*, Case No. C 06-4679 JF (HRL), had not been paid or adequately provided for, all in violation of California Corporations Code Section 1905(a)(2).

120. ACTICON is informed and believes, and thereon alleges, that PRETEC dissolved its corporation and fraudulently and wrongfully transferred its assets to PTI GLOBAL, INC. and/or C-ONE in order to avoid liability for the claims set forth in the FIRST COMPLAINT in *Acticon Technologies LLC v. Pretec Electronics Corp., et al.*, Case No. C 06-4679 JF (HRL).

121. ACTICON has been damaged by the actions of the INDIVIDUAL DEFENDANTS and/or DOES 1 through 20 in that the INDIVIDUAL DEFENDANTS and/or DOES 1 through 20, having fraudulently and wrongfully executed PRETEC's certificate of dissolution and having transferred the assets and corporate funds of PRETEC to deprive PRETEC of the monies and ability to meet its obligations for liability under the FIRST COMPLAINT in *Acticon Technologies LLC v. Pretec Electronics Corp., et al.*, Case No. C 06-4679 JF (HRL), improperly filed for the corporate dissolution of PRETEC.

WHEREFORE, ACTICON seeks relief as set forth in the Prayer, below.

PRAYER FOR RELIEF

WHEREFORE, ACTICON prays for judgment against DEFENDANTS as follows:

1. On Count I, for judgment that C-ONE has infringed the Patents-in-Suit;

2. On Count I, for judgment that C-ONE has induced infringement of the Patents-in-Suit;

3. On Count I, for judgment that C-ONE's infringement of the Patents-in-Suit is, and has been, willful and deliberate;

4. On Count II, for judgment that PTI GLOBAL, INC., PRETEC and C-ONE have infringed the Patents-in-Suit.

5. On Count II for judgment that PTI GLOBAL, INC., PRETEC and C-ONE have induced infringement of the Patents-in-Suit;

6. On Count II, for judgment that PTI GLOBAL, INC.'s, PRETEC's and C-ONE's infringement of the Patents-In-Suit is, and has been, willful and deliberate;

7. On Count III, for judgment that the INDIVIDUAL DEFENDANTS, and each of them, are the alter ego of PRETEC, for damages suffered by ACTICON as a consequence of DEFENDANTS' actions herein and for exemplary and punitive damages;

8. On Counts III and IV, for judgment that the INDIVIDUAL DEFENDANTS, and each of them, have infringed the Patents-in-Suit;

9. On Counts III and IV, for judgment that the INDIVIDUAL DEFENDANTS, and each of them, induced the infringement of the Patents-in-Suit;

10. On Counts III and IV, for judgment that the INDIVIDUAL DEFENDANTS, and each of them, contributorily infringed the Patents-in-Suit;

11. On Count IV, for judgment that the INDIVIDUAL DEFENDANTS, and each of them, are vicariously liable for the damage and harm caused by PRETEC's, PTI GLOBAL's and C-ONE's infringing conduct;

12. On Count V, for judgment that DEFENDANTS, and each of them, fraudulently transferred the assets of PRETEC, for damages suffered by ACTICON as a consequence of DEFENDANTS' actions herein and for exemplary and punitive damages;

13. On Count VI, for judgment that DEFENDANTS, and each of them, conspired to fraudulently transfer the assets of PRETEC;

14. On Count VII, for judgment that DEFENDANTS, and each of them, improperly dissolved PRETEC; for damages suffered by ACTICON as a consequence of DEFENDANTS' actions herein and for exemplary and punitive damages.

15. On Counts I, II, III and IV, for an award of damages pursuant to 35 U.S.C. § 284 adequate to compensate ACTICON for DEFENDANTS' infringement of the Patents-In-Suit; but not less than a reasonable royalty, with interest, including pre-judgment interest, and a trebling of such damages in view of the willful and deliberate nature of the infringement;

16. On Counts I, II, III and IV, for costs, including expenses and reasonable attorney's fees pursuant to 35 U.S.C. §§ 284 and 285; and

17. For further and/or alternative relief as deemed just and proper.

Dated: June 16, 2008

CARR & FERRELL *LLP*

By: 

ROBERT J. YORIO
COLBY B. SPRINGER
CHRISTINE S. WATSON

Attorneys for Plaintiff
ACTICON TECHNOLOGIES LLC

DEMAND FOR JURY TRIAL

Plaintiff ACTICON TECHNOLOGIES LLC hereby demands a jury trial of all issues in the above-captioned action which are triable to a jury.

Dated: June 16, 2008

CARR & FERRELL *LLP*

By: 

ROBERT J. YORIO
COLBY B. SPRINGER
CHRISTINE S. WATSON

Attorneys for Plaintiff
ACTICON TECHNOLOGIES LLC

United States Patent [19]

Farago

[11] **Patent Number: 4,603,320**

[45] **Date of Patent: Jul. 29, 1986**

[54] **CONNECTOR INTERFACE**

[75] Inventor: **Steven Farago**, Mount Kisco, N.Y.

[73] Assignees: **Anico Research, Ltd. Inc.**, Mount Kisco; **Rapitech Systems Inc.**, New York, both of N.Y.

[21] Appl. No.: **484,823**

[22] Filed: **Apr. 13, 1983**

[51] **Int. Cl.**[4] **H03K 13/24**

[52] **U.S. Cl.** ..... **340/347 DD**; 339/176 MP; 361/394

[58] **Field of Search** ..... 340/347 DD; 339/17 R, 339/17 C, 17 F, 14 R, 17 M, 17 LC, 17 N, 176 R, 176 M, 176 MP; 361/392-395, 412, 415; 364/705-771; 179/20 P

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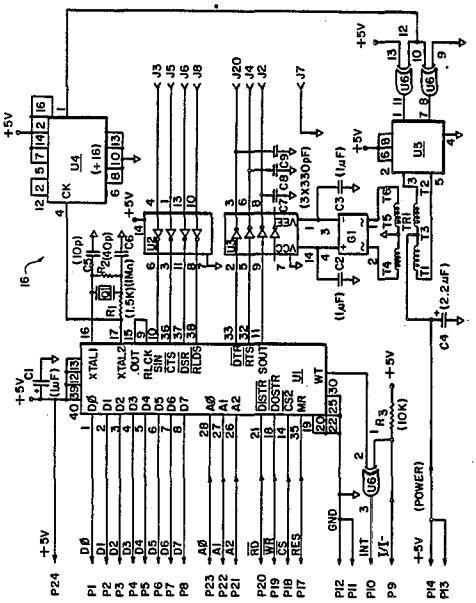
Primary Examiner—Vit W. Miska

Attorney, Agent, or Firm—Israel Nissenbaum

[57] **ABSTRACT**

A connector interface for enabling communications between first and second data handling systems wherein the data in the first system is arranged in a first type of format and the data in the second system is arranged in a second type of format, includes a connector housing with first and second sets of electrical contact elements exposed at different portions of the housing. Circuitry contained entirely within the housing operates to convert data transmitted to the first set of contact elements from the first data handling system into corresponding data in the second type of format for transmission to the second data handling system through the second set of contact elements, and to convert data transmitted to the second set of contact elements from the second data handling system into corresponding data in the first format for transmission to the first data handling system. One set of electrical contact elements may, for example, be arranged to extend out from the connector housing in two parallel rows to allow the elements to be directly connected to corresponding terminals arranged in a dual in line configuration on an outside printed circuit board. The connector arrangement greatly simplifies the design and construction of data processing systems requiring specific interfaces between certain parts of the systems, such as between data terminal equipment and data communication equipment employing serial binary data interchange.

23 Claims, 7 Drawing Figures



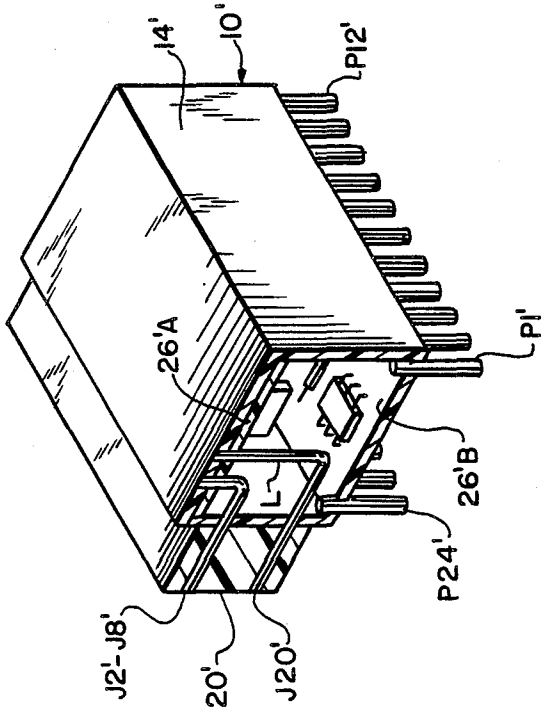


EXHIBIT A

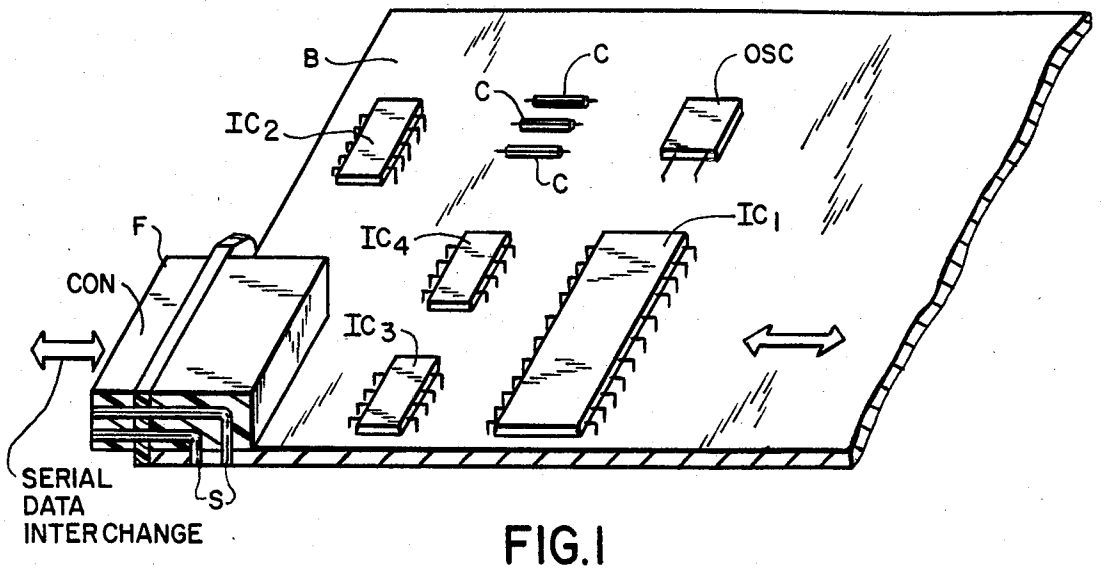
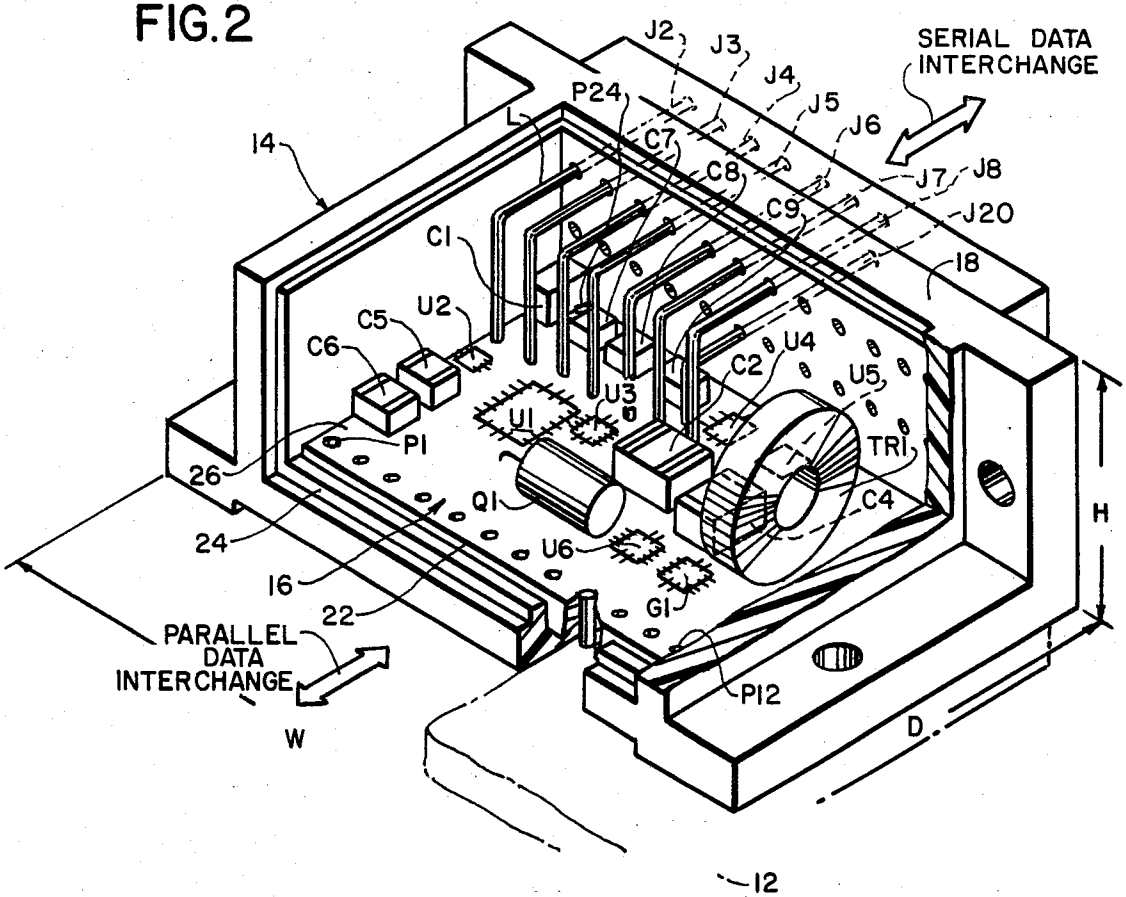


FIG.1

PRIOR ART

FIG.2



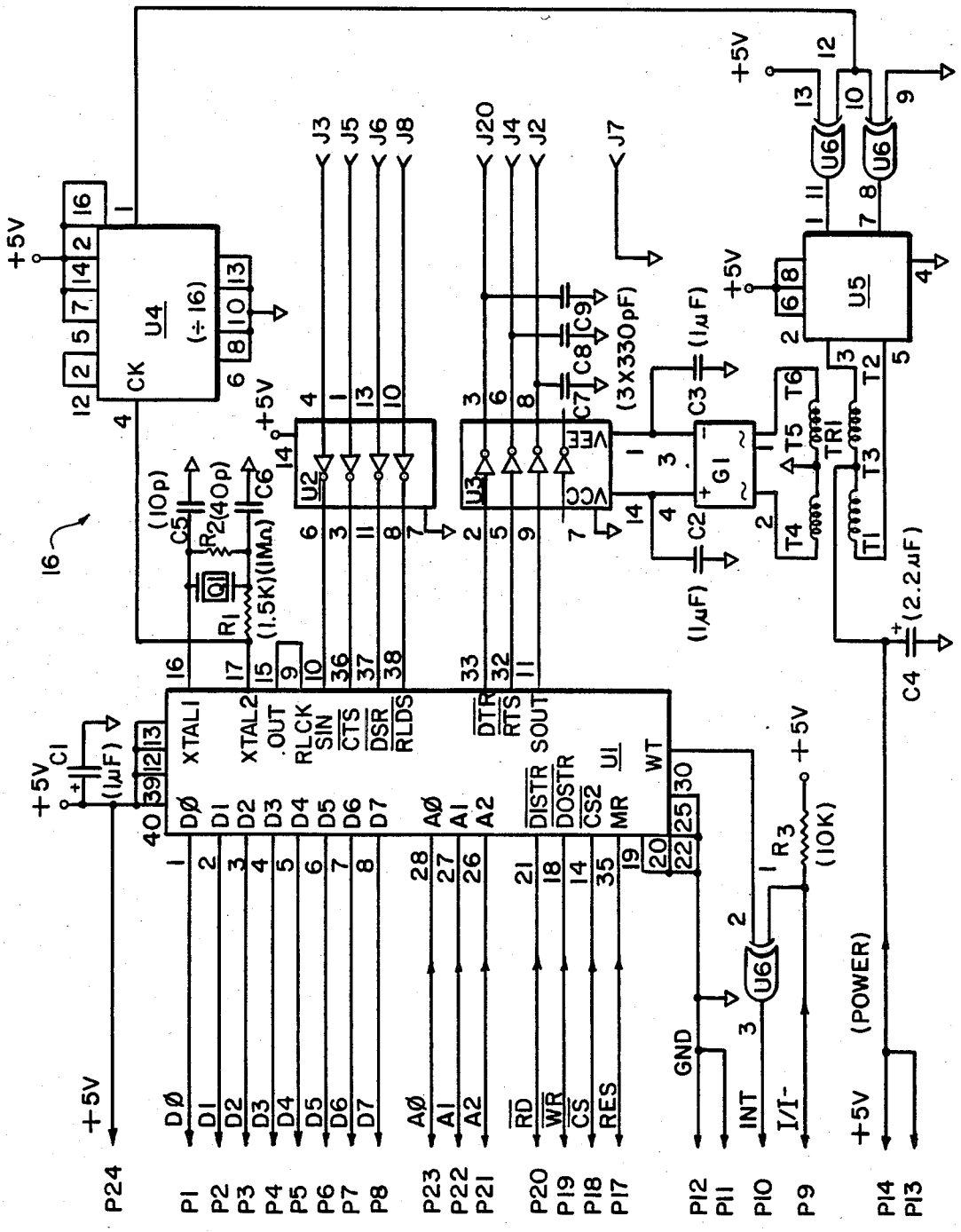

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FIG.3

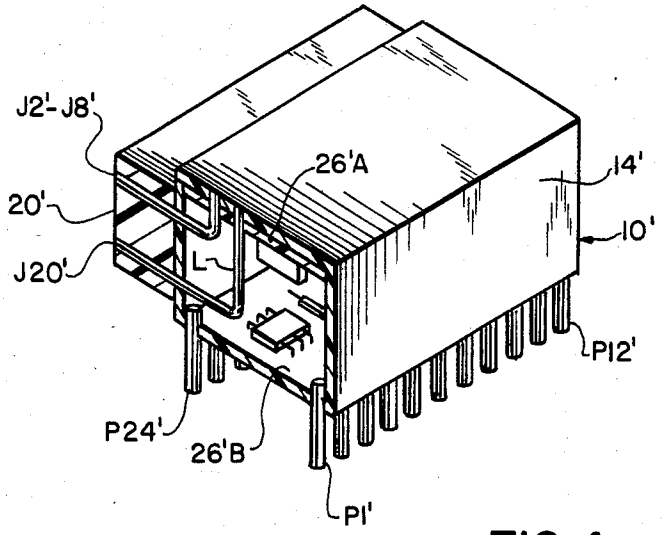


FIG.4

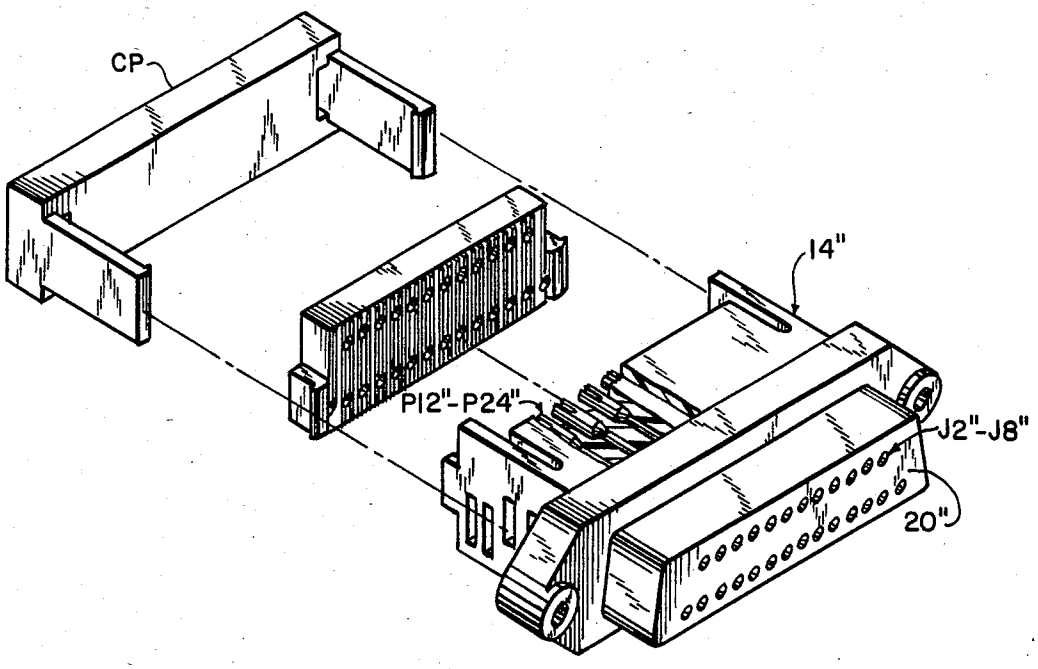
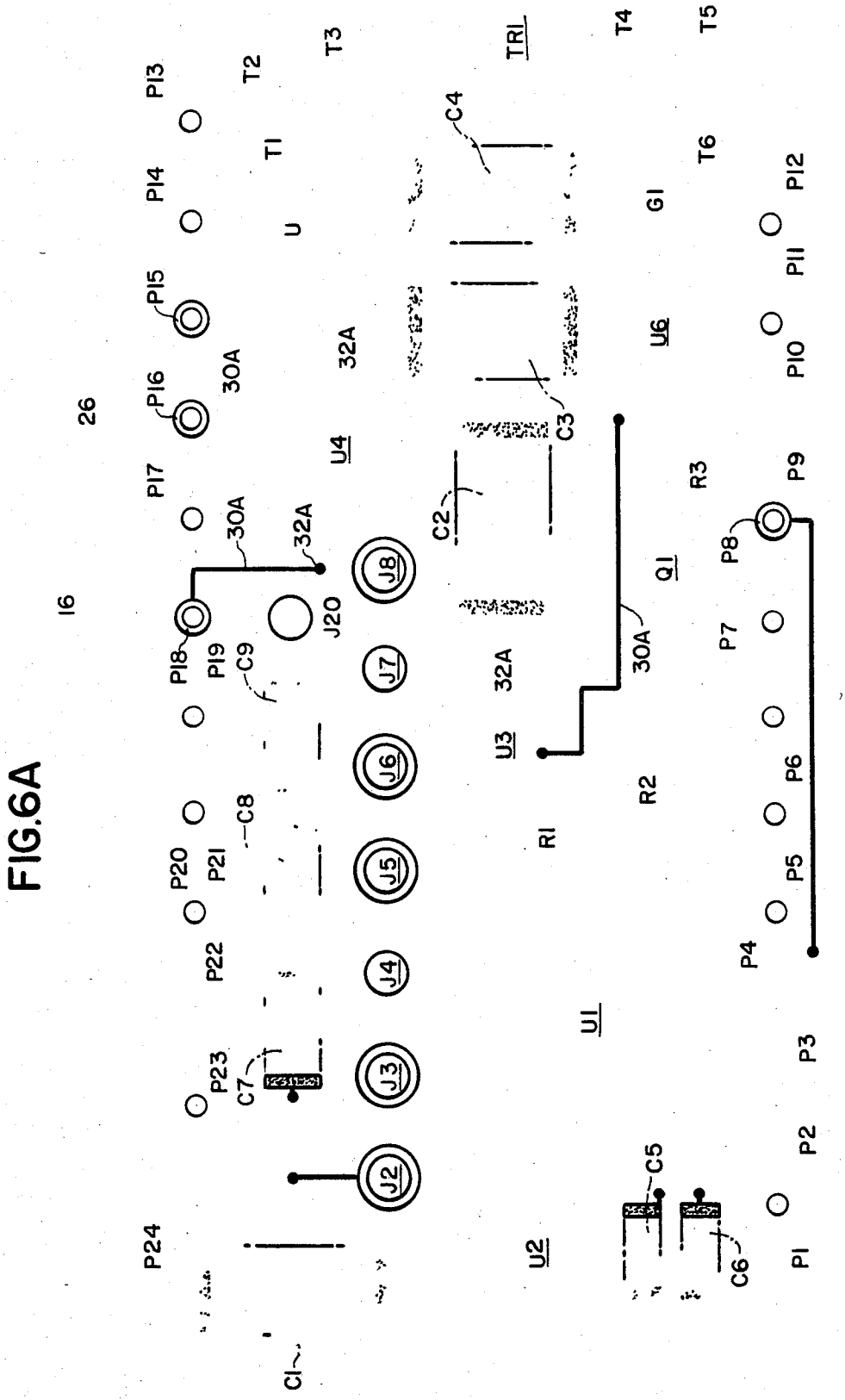


FIG.5

FIG.6A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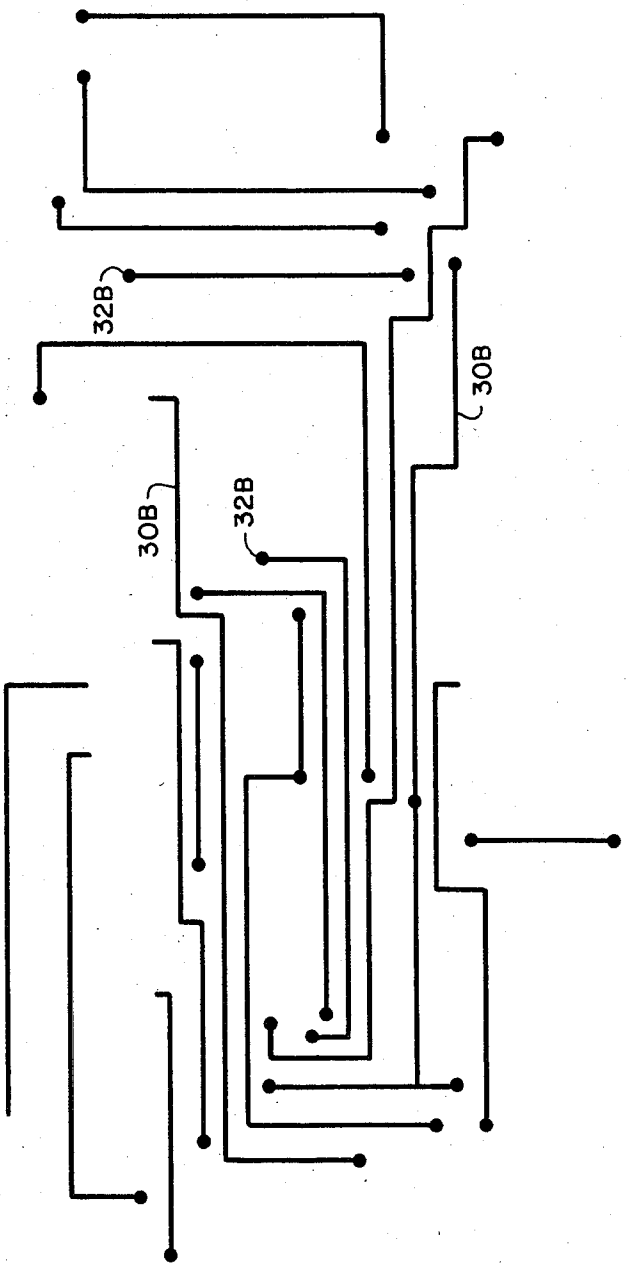

FIG.6B

CONNECTOR INTERFACE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to elelctrical connectors, and particularly to a connector having internal circuitry capable of providing a specified electrical interface between various types of data handling equipment.

2. Description of the Prior Art

The proliferation of digital data processing equipment, first in business and now into the home, has created an ongoing demand for such equipment with ever increased capabilities but at an affordable price. The modern trend to integrate numerous discrete electrical components within single semiconductor integrated circuits or "chips", has provided for greater economies in the manufacture of digital electronic equipment. Not only is the overall physical size and weight of the equipment reduced through use of integrated circuit technology, but manufacturing costs also are alleviated in that the price of each integrated circuit used is but a fraction of the total cost represented by all the components it contains.

Digital data processing systems which are in common use today include portions arranged to allow the user to communicate with the system by way of, for example, a terminal or a printer. The user "talks" or provides information to the system through the terminal, and this information is converted into digital data which the system is capable of understanding. After the data is processed by the system which may include some form of computer, a suitable response is transmitted back to the user in digital form and then properly converted into visibly recognizable words or symbols on the screen of the terminal or on a sheet generated by a printer.

Accordingly, it is often necessary to provide cable interconnections between differently located units of a data processing system to allow the units to transmit and receive digital data to and from one another.

Certain types of digital equipment, e.g. a terminal or a printer, transmit or receive digital data in serial bit format. That is, each character (i.e., letter or numeral) of the data is sent or received one bit at a time. It will be appreciated that in a typical system where each character occupies multiple bits, communicating the characters as serial bits between separately located pieces of equipment reduces significantly the number of separate conductors which must be provided in the connecting cables, allows for the communicating equipments to operate in time synchronism with one another with regard to the data exchanged between them, as well as for the use of parity bits and other common error detecting techniques to be applied for each data character communicated. Other kinds of equipment in data handling systems operate in a parallel bit format. For example, computers operate on data which is loaded in internal registers one full character (i.e., eight bits) at a time, and likewise provide output information a character at a time to internal output registers.

In order to insure compatability between terminals, printers and other input/output data handling equipment which operate in a serial bit format, and computer mainframes and related equipment, the electronic Industries Association promulgated in 1969 a now widely accepted interface standard known as EIA RS-232-C,

the provisions of which are incorporated by reference herein. The RS-232-C Standard, entitled "Interface Between Data Terminal Equipment and Data Communication Equipment Employing Serial Binary Data Interchange", ensures that serial bit format equipment produced by one manufacturer will operate properly with serial bit format equipment of another manufacturer. The RS-232-C Standard applies not only to the interchange of information data signals between data handling equipment, but also to the interchange of timing and control data signals between such equipment (Sec. 1.4 of the Standard).

In order to ensure satisfactory noise immunity of the data signals to be communicated over connecting cables, the RS-232-C Standard provides that the data signals transmitted over the cables have magnitudes of at least ±6 volts (See Sec. 2.3 of the Standard). Since most data handling equipment today operate at five-volt levels, the Standard makes necessary additional power supplies for enabling a voltage level conversion of the data signals to be interchanged over the connecting cable.

With regard to mechanical characteristics of the interface, the RS-232-C Standard states that the interface is "located at a pluggable connector signal interface point between the two equipments. The female connector . . . should be mounted in a fixed position near the data terminal equipment". (Sec. 3.1). FIG. **3.1** within the RS-232-C Standard assigns certain circuit functions to each of **25** connector pins associated with the pluggable connector at the signal interface point. While the Standard does not specify a particular type of multiple pin connector (See Appendix I to the Standard), the "D-type" 25 pin connector (for example, AMP type 206584-1) has essentially become an industry standard.

A printed circuit board together with circuit components and software necessary to achieve an RS-232-C interface between a computer terminal on one side, and modems or serial line printers on the other side, is available from a variety of manufacturers. Such boards are mountable inside the computer, and separate cable is provided. These boards are compatible from the RS-232-C side but they differ on the computer side from computer to computer.

The known RS-232-C interfaces which include a printed circuit board are arranged physically as shown in FIG. **1**. The board B can be a "stand alone card" and be connected via a card cage connector (not shown) to various parallel signal bus lines associated with a microprocessor in a computer or other terminal equipment (also not shown). Alternatively, it can be a part of a more complex board. The RS-232-C Standard 25-pin connector CON may be mounted along one edge of the board B as shown, and the pins directly connected electrically to printed conductors on the board by soldering as at points S on the underside of the board B. This leaves a female connector part F fixedly mounted near the data terminal equipment as required by the Standard. The various conductors to which the pins of the connector CON are connected lead to electrical circuitry arranged over other portions of the board B, including, for example, a main logic element chip IC **1**, line driver IC **3**, line receiver IC **4**, crystal oscillator OSC, frequency divider IC **2**, and a number of discrete components C.

It will be appreciated that the known RS-232-C interface board arrangements require that a certain amount

of space be allocated in existing equipment for their insertion, such space often being at a premium in units intended to be portable and of small overall dimensions. As far as is known, there has been no attempt to integrate any electrical interface circuitry, including those components required to implement the RS-232-C interface as shown in FIG. 1, within the prescribed interface connector itself such as the 25-pin connector CON.

A connector is known from U.S. Pat. No. 3,790,858 to Brancaleone et al within which RF filter elements are connected to a number of parallel pin-like contact elements which are supported inside and extend axially through a cylindrical shell. The filter elements are connected internally between the contact elements and a common cylindrical metal ground plate.

SUMMARY OF THE INVENTION

A primary object of the present invention is to provide a connector which exhibits simultaneously both the electrical characteristics and the connector requirements of a specified interface between two different data handling systems or equipments.

Another object of the invention is to provide a method wherein electrical circuitry for carrying out a specified function between two different data handling systems is integrated within a connector housing so as to reduce significantly spatial requirements within equipment associated with the systems.

According to one aspect of the invention, a connector includes a housing having a first set and a second set of terminals extending at least partly through wall parts of the housing to engage corresponding terminals of first and second outside connection means associated with first and second data handling systems, respectively. Logic interface circuit means is arranged within the connector housing and coupled between the first and second set of terminals. The circuit means operates to convert data signals transmitted to the first set of terminals from the first data handling system in a first type of format into corresponding data signals in a second type of format, and to provide the corresponding data signals in the second type of format to the second set of terminals for transmisson to the second data handling system. The circuit means also operates to convert data signals transmitted to the second set of terminals from the second data handling system in a second type of format into corresponding data signals in a first type of format, and to provide the corresponding data signals in the first type of format to the first set of terminals for transmission to the first data handling system.

According to another aspect of the invention, a method of implementing a logical interface to enable communications between a first data handling system in which data signals are arranged in a first type of format, and a second data handling system in which data signals are arranged in a second type of format, includes the steps of providing a connector housing; supporting first and second sets of electrical contact elements on the housing; containing electrical circuitry within the connector housing and connecting the circuitry with the first and the second sets of contact elements by arranging conductors inside the housing; converting by way of the electrical circuitry data signals transmitted to the first set of electrical contact elements in a first type of format from a first data handling system outside the connector housing into corresponding data signals in a second type of format and providing same to the second set of electrical contact elements through the conductors inside the connector housing; and converting by way of the electrical circuitry data signals transmitted to the second set of electrical contact elements in the second type of format from a second data handling system outside the connector housing into corresponding data signals in the first type of format and providing same to the first set of electrical contact elements through the conductors inside the connector housing.

The invention will be more clearly understood upon reading the following detailed description of preferred embodiments thereof in conjunction with the accompanying drawing.

BRIEF DESCRIPTION OF THE DRAWING

In the drawing:

FIG. 1 is a perspective view of a conventional serial interface arranged on a portion of a printed circuit board;

FIG. 2 is a perspective view, with parts broken away, showing a first embodiment of a connector according to the present invention mounted on a printed circuit board;

FIG. 3 is a schematic diagram representing electrical circuitry contained in the housing of the connector in FIG. 2;

FIG. 4 is a perspective view of a second embodiment of a connector according to the present invention;

FIG. 5 is a perspective view of a third embodiment of a connector according to the present invention;

FIG. 6A is a top plan view of a printed circuit layout, and the phantom outline of the components, of the electrical circuitry seen in the schematic diagram of FIG. 3; and

FIG. 6B is a bottom plan view of the printed circuit board illustrating the interconnection among the various components.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 2 shows a first embodiment of a connector **10** according to the invention, the connector **10** being mounted on a printed circuit board **12** associated with a data handling system or equipment (not shown) in which data is interchanged in a parallel format. The connector **10** includes a connector housing **14**, portions of which are omitted in FIG. 2 for the purpose of illustrating electrical circuitry **16** mounted in the interior space of the housing **14**. It is preferable that walls of the housing **14** substantially enclose the interior space so as to protect the circuitry **16** contained therein.

As shown in FIG. 2, the housing **14** is in the form of a generally rectangular hollow block and includes a front wall **18**, a part of which projects outwardly to define first outside connection surface **20** parallel to the inside surface of wall **18**. Housing **14** also includes a bottom wall **22** the outside surface of which defines a second outside connection surface **24**. The outside dimensions of the housing **14**, particularly those of the front wall **18** together with the first outside connection surface **20**, preferably conform to those of a standard socket connector, thereby being adapted to mate with a standard plug connector or corresponding or complementary configuration. For applications in the RS-232-C interface, the housing **14** should conform to the dimensions of the known 25-pin "D type" subminiature connector mentioned earlier. Typical dimensions for the housing **14** thus may be a height H of about 0.5

inches (12.70 mm.), a depth D of about 1.2 inches (30.48 mm.) and a width W of about 2.0 inches (50.80 mm.).

The electrical circuitry **16** includes, in the embodiment of FIG. **2**, a carrier in the form of a single printed circuit board or substrate **26** mounted closely adjacent and parallel to the inside surface of the bottom wall **22**. Various integrated circuits and discrete components are mounted on the board **26**, and are electrically connected by soldering, or by other technology, to conductors on one or both sides of the board **26**.

The various "chips" and components shown in FIG. **2** as contained within the connector housing **14** on the board **26**, and represented schematically in FIG. **3**, include integrated circuits U1–U6; four tantalum chip capacitors C1–C4; a set of five chip capacitors C_5–C_9; a quartz crystal Q1; a toroid core transformer TR1 having bifilar wound primary and secondary windings T1–T2 and T4–T6; and a Graetz diode bridge G1. Each of eight conductors L extends from a different one of eight connection points on the printed circuit board **26** (FIG. **2**), to corresponding female electrical contact elements or terminals J2–J8 and J20 which extend partly through and are supported in openings in the wall **18**. The outside ends of the female contact elements are exposed at the first outside connection surface **20** to engage corresponding pins of an outside plug connector (not shown). The numbers assigned to the female contact elements J2–J8 and J20 correspond to the pin number-circuit function assigments prescribed in the RS-232-C Standard, mentioned earlier. Further, 24 male electrical contact elements or pins P1–P24 extend in two parallel rows of 12 pins each, downwardly from connection points near the long edges of the board **26** (FIG. **2**), to engage openings in printed conductors or a conventional dual in line socket on the outside printed circuit board **12**, at the second outside connection surface **24**.

In accordance with a preferred technique of manufacture, the housing **14**, except for the bottom wall **22**, is molded in one piece; the elements or terminals J2–J8 and J20, as well as the conductors L, being included in the molding operation. Then, the bottom wall **22** and abutting printed circuit board **26** are snapped into position in the housing. By means of localized heating, the bottom wall is fused to the housing so that a completely unitary structure is achieved.

FIG. **3** shows the interconnections between the chips and other electrical components on the printed circuit board **26** contained within the connector housing **14**, together with the female and the male contact elements arranged on the first and the second outside connection surfaces **20**, **24** of the connector **10**, respectively. The circuitry of FIG. **3** is one example of circuitry which functions to provide the electrical characteristics of an RS-232-C interface, but it will be appreciated that different circuitry may be integrated within the connector housing **14** to carry out the same function or other commonly used interfaces including 8-bit Parallel, GPIB (general purpose interface bus-IEEE 488), and Ethernet.

The integrated circuit U1 may be, for example, National Semiconductor type INS 8250A. The circuit U1 serves as a main logic element which handles all data signal interchanges between, e.g., a microprocessor (not shown) which handles data in a parallel bit format and communications equipment (not shown) which sends and receives serial bit data. Circuit U1 contains several programmable registers which determine the communications format and all the necessary information data to perform successfully a two-way data interchange between two data systems of different data formats. Specifically, before sending or receiving any data via an RS-232-C line, a controlling microprocessor (not shown) must load the internal registers with the required commands. The system software contains the following load functions which, when programmed within circuit U1, enable the latter to be used for data communications. The preprogrammed functions are:

1. Baud rate and baud rate factor;
2. Character length;
3. Number of stop bits;
4. Parity enable/disable and parity polarity;
5. Modem control functions; and
6. Additional operational conditions.

Instructions representing the above load functions are transmitted to the circuit U1 from an outside microprocessor (not shown) over data bus lines DO–D7 corresponding to the male contact elements or pins P1–P8 on the second outside connection surface **24** of the connector housing **14** (FIG. **2**). The appropriate registers within circuit U1 are selected by the address bus lines A, A1 and A2 (pins P23, P22 and P21), and a write signal ($\overline{WR}$, pin P19) validates the register loadings.

When data characters are transmitted by the outside microprocessor after the foregoing initialization procedure, the circuit U1 performs a parallel-to-serial data conversion. First, the eight-bit parallel data is placed into a transmitter register within circuit U1 which then automatically adds a start bit, followed by the data character bits themselves (least significant first) and the programmed number of stop bits for each character. Also, an even or odd parity bit is inserted prior to the stop bit(s) as defined previously by the system program. The character is then transmitted as a serial data stream on a data output line S_{out} at terminal **11** of the circuit U1. The rate at which the data is shifted out is determined by another previously programmed register within circuit U1. The quartz crystal Q1 coupled to the circuit U1 operates together with a programmable divider within circuit U1 to generate a signal of the appropriate frequency for shifting out the data bits.

The strength or voltage levels of the data bits or signals shifted out from the circuit U1, typically TTL compatible (zero to +5 volts). As mentioned earlier, the RS-232-C Standard requires a stronger signal level so that data can be transmitted over a long cable with the capacity of noise suppression. Accordingly, a line driver circuit U3, e.g., Motorola type MC 1488, is coupled to data output S_{out} and supplementary handshake signals as $\overline{RTS}$ (Request to Send) and $\overline{DTR}$ (Data Terminal Ready) of the circuit U1. When powered by an appropriate power supply, the line driver circuit U3 converts the TTL compatible level (zero to +5 volt) of the serial output from the circuit U1, to a ±12 volt level sufficient to satisfy the RS-232-C Standard. The integral power supply is constructed of a push-pull mode switching scheme, performed by high frequency oscillator derived from U4 (e.g. 4516B RCA), 74C86 exclusive OR gates (U6 e.g. Nat. Semiconductor), high current power transistors within U5 (75951 e.g. Texas Instruments) Tr1 transformer, G1 diode bridge and C2,C3 tantalum capacitors.

When a serial data bit stream is transmitted to the connector **10** from an outside data handling system, specifically to the female contact elements J3 at the first outside connection surface **20** of the housing **14**, the

higher voltage level of the bit streams is converted to a TTL compatible (0 to 5 volt) logic level by way of buffer-inverters within circuit U2 (e.g., Motorola type MC 1489A). Also, high level complementary signals (J5, J6 and J8 are converted down). The serial data is then shifted into a receiver register within the main logic element circuit U1 where the data is converted into a parallel format; however, the start and stop bits and the parity bit are subtracted. Thus, the data is then ready to be sent to the microprocessor or other outside parallel format data system over the data bus lines DO–D7.

The circuit U1 is selected for operation by the microprocessor or other outside parallel data system connected to the pins P1–P24 of the connector 10 by way of a chip select signal ($\overline{CS}$, pin P18). The receiver register within the circuit U1 is selected by a preset combination of the address bus lines (AO, A1, A2; pins P23, P22, P21), and the parallel data is placed on the data bus lines (DO–D7; pins P1–P8) for transmission to the outside microprocessor. A read signal ($\overline{RD}$, pin P20) activates the data reading from the circuit U1 to the microprocessor. Likewise, status information reading procedure can be performed similarly.

There are several control signals, and control and status registers in circuit U1 that determine the bidirectional serial communication procedure. All the necessary signals, including "handshaking", status and command bits, and modem control are included in communications following the preprogrammed functions from the outside microprocessor software.

Those components on the board 16 (FIG. 2) which have not been discussed above in detail but appear in the circuitry of FIG. 3 will be recognized and understood by those skilled in the art. A preferred quartz crystal Q1 is Seiko type DS-MGQ, 1.8432 MHz, series resonant. The chip capacitors C1–C4 may be Arco type ACT, tantalum, and the chip capacitors C5–C9 may be Murata type GR40 Y5 V. Chip resistors R1–R3 can be panasonic type ERJ-86CSJ, or alternatively can be thick film resistors deposited on the board 16.

The toroid transformer TR1 preferably is made from a Ferroxcube core type 266CT125, material 4C4. The primary winding is 2×10 turns and the secondary is 2×25 turns, both bifilar.

FIG. 4 shows a second embodiment of a connector 10′ according to the invention. The outside dimensions and overall appearance of the connector 10′ are generally similar to those of the connector 10 of FIG. 2. Two printed circuit boards or substrates 26′A and 26′B are, however, provided in housing 14′ instead of the single board 26 in FIG. 2. Board 26′A extends at the top of the housing 14′ parallel to the board 26′B which extends across the bottom of housing 14′. Board 26′B carries 24 pins P1′–P24′ on its bottom outside surface 24′ for connection directly to an outside circuit board or into a dual-in-line socket. The board 26′A is coupled by leads L′ to female contact elements J2′–J8′ and J20′ which engage an outside plug connector at connection surface 20′ of the connector 10′.

FIG. 5 shows a third embodiment of a connector 10″ according to the invention. A single, flexible printed circuit board 26″ is contained within the connector housing 14″. Conductors at one end of the board 26″ are directly to the inside of female contact elements J2″–J8″ and J20″ which are arranged to engage an outside plug connector at contact surface 20″. Conductors at an opposite end of the flexible board 26″ are connected directly to the inside ends of insulation displacement type pins P1″–P24″. A cap CP is constructed and arranged to clamp a flat insulated cable (not shown) over pointed ends of pins P1″–P24″ so that the pins pierce through the cable insulation to electrically contact corresponding conductors of the flat cable.

It will be appreciated that the connector of the present invention provides a completely self-contained interface unit which eliminates all the inconveniences of designing and realizing a data interface such as the RS-232-C Standard. Particular components no longer need be selected to meet the requirements of the Standard, voltage level conversions are provided for, and time consuming test procedures and debugging are eliminated. The present connector thus saves engineering effort, development and production time as well as labor costs. Importantly, a considerable space savings is achieved in terminal equipment which would otherwise require means to accommodate a separate interface board.

In order to enable the man skilled in the art to practice this invention in some detail, a complete printed circuit layout is shown in FIG. 6. This layout conforms with the circuitry previously illustrated in schematic form in FIG. 3. The contact areas J2–J8 and J20, which correspond with the respective female contact elements so designated, will be seen in FIG. 6A. Likewise, contact areas P1–P12 (at the near longitudinal edge) and P13–P24 (at the far edge), which correspond with the respective male contact elements bearing the same designation. Capacitors C1–C9, oscillator Q1, and transformer TR1, are seen in phantom outline while resistors R1, R2 and R3 are represented by means of hatch lines. All the other principal elements are shown by means of rectangles suitably labeled. Appropriate wire bonding from the several integrated circuits U1–U6, as well as from the Graetz bridge G1, is shown in FIG. 6A connected to the conductors 30A on the printed circuit board.

It will be noted by the skilled worker that suitably correlated conductors 30B are provided on the lower surface of the printed circuit board 26 (FIG. 6B) so as to make the requisite interconnections among components. The dots 32 represent so-called "vias" between the upper and lower surfaces of board 26.

It will be appreciated that, for the sake of clarity, the depiction of a printed circuit layout for a circuit board 26 to be housed in connector 10 of FIG. 2 is greatly enlarged (approximately 7 times).

While specific embodiments of the invention have been shown and described in detail to illustrate the application of the inventive principles, it will be understood that the invention may be embodied otherwise without departing from such principles.

I claim:

1. An electrical connector for implementing a direct predetermined logical interface between a first data handling system wherein data signals are arranged in a first type of format, and a second data handling system wherein data signals are arranged in a second type of format, comprising:

a connector housing including a first wall part forming a first outside connection surface and a second wall part forming a second outside connection surface;

a first set of terminals arranged to extend at least partly through said first wall part from inside said connector housing in a given configuration for

engaging in electrical contact with corresponding terminals of first outside connection means associated with the first data handling system, with said first set of terminals forming a single logical interface member for matingly engaging a corresponding single logical interface member formed by said corresponding terminals associated with the first data handling system;

a second set of terminal arranged to extend at least partly through said second wall part from inside said connector housing in a given configuration for engaging in electrical contact with corresponding terminals of second outside connection means associated with the second data handling system, with said second set of terminals forming a single logical interface member for matingly engaging a corresponding single logical interface member formed by said corresponding terminals associated with the second data handling system; and

logic interface circuit means arranged within said connector housing and coupled between said first set of terminals and said second set of terminals for converting data signals transmitted to at least some of said first set of terminals from the first data handling system in the first type of format into corresponding data signals in the second type of format and providing said corresponding data signals in the second type of format to at least some of said second set of terminals for subsequent transmission to the second data handling system, and for converting data signals transmitted to at least some of said second set of terminals from the second data handling system in the second type of format into corresponding data signals in the first type of format and providing said corresponding data signals in the first type of format to at least some of said first set of terminals for subsequent transmission to the first data handling system.

2. A connector according to claim **1**, wherein said logic interface circuit means comprises means for converting data signals transmitted to at least some of said first set of terminals in a serial format into corresponding data signals in a parallel format and providing the corresponding parallel data signals to at least some of said second set of terminals, and for converting data signals transmitted to at least some of said second set of terminals in a parallel format into corresponding data signals in a serial format and providing the corresponding serial data signals to at least some of said first set of terminals.

3. A connector according to claim **1**, wherein said logic interface circuit means comprises means for converting the voltage level of the data signals transmitted to at least some of said first set of terminals from a first voltage level into a second voltage level and providing the corresponding data signals at the second voltage level to at least some of said second set of terminals, and for converting the voltage level of the data signals transmitted to at least some of said second set of terminals from the second voltage level into the first voltage level and providing the corresponding data signals at the first voltage level to at least some of said first set of terminals.

4. A connector according to claim **1**, wherein said logic interface circuit means comprises a printed circuit substrate mounted within said connector housing.

5. A connector according to claim **1**, wherein said logic interface circuit means comprises an integrated circuit mounted within said connector housing.

6. A connector according to claim **4**, comprising an integrated circuit mounted on said printed circuit substrate.

7. A connector according to claim **1**, wherein said first set of terminals comprises a number of female contact elements arranged to mate with corresponding male contact elements of the first outside connection means, said first wall part of said connector housing having a number of openings in said first connection surface within which openings said female contact elements are fixedly supported, and said second set of terminals comprises a number of male contact elements arranged to mate with corresponding female contact elements of the second outside connection means, said second wall part of said connector housing having a number of openings in said second connection surface within which openings said male contact elements are fixedly supported.

8. A connector according to claim **7**, wherein said first connection surface extends generally within a first plane, and said second connection surface extends generally within a second plane.

9. A connector according to claim **8**, wherein said second plane is perpendicular to said first plane.

10. A connector according to claim **8**, wherein said second plane is parallel to said first plane.

11. A connector according to claim **8**, wherein said male contact elements are arranged in two parallel rows for engaging corresponding openings formed in the female contact elements of the second outside connection means.

12. A connector according to claim **1** wherein said connector housing has structural dimensions of a height of no more than about 0.5 inches (12.70 mm), a depth of no more than about 1.2 inches (30.48 mm), and a width of no more than about 2.0 inches (50.80 mm).

13. A connector according to claim **1** wherein said connector housing comprises walls forming an enclosure member and wherein said logic interface circuit means are completely enclosed within the walls of said connector housing.

14. The connector of claim **1** wherein said first set of terminals comprises a number of male contact elements adapted for direct integrated electrical mating with a printed circuit board member which handles data in said first type of format and wherein said housing is adapted to be physically supported by said printed circuit board.

15. The connector of claim **1** wherein said first set of terminals comprises a number of male contact pins adapted for direct integrated electrical mating with an insulated ribbon cable connector member, with said pins being adapted to pierce the insulation of said cable to electrically contact conductors of said cable whereby said electrical mating is effected said cable connector member being adapted to be electrically connected to a printed circuit board which handles data in a first format and wherein said connector comprises means to physically enclose a portion of said ribbon cable connector.

16. The connector of claim **13** wherein said logic interface circuit means furthr comprises a power supply, with said power supply being contained within said walls of said connector housing.

17. A "D-type" 25 pin RS-232-C connector having a male connection interface adapted for direct integrated electrical mating with a printed circuit board member which handles data in a parallel format, said connector further having a female connection interface for mating connection with an external male connection interface member from a device which handles data in a serial format, characterized in that means for converting data from said parallel format to said serial format and means for converting data from said serial format to said parallel format are electrically positioned between said male connection interface and said female connection interface within said connector, and wherein said connector is adapted to be physically supported by said printed circuit board.

18. A method of implementing a logical interface to enable communications between first and second data handling systems wherein data signals are arranged in a first type format in the first system and in a second type of format in the second system, comprising the steps of:

providing a connector housing and supporting first and second sets of electrical contact elements on the connector housing;

exposing the first set of electrical contact elements on one portion of the outside surface of the connector housing and exposing the second set of electrical contact elements on another portion of the outside surface of the connector housing;

arranging the first set of electrical contact elements for connection with the first data handling system outside of the connector housing and arranging the second set of electrical contact elements for connection with the second data handling system outside of the connector housing, wherein each of said first and second set of electrical contact elements comprises a single logical interface member, and wherein said interface members of said first and second set of electrical contact elements are matingly electrically connected to a corresponding single logical interface member of said first and second data handling system respectively;

containing electrical circuitry substantially within the connector housing and connecting the electrical circuitry with the first and second sets of electrical contact elements by arranging conductors inside the connector housing;

converting by way of the electrical circuitry data signals transmitted to at least some of the second set of electrical contact elements in the second type of format from the second data handling system into corresponding data signals in the first type of format; and

providing the corresponding data signals in the first type of format from the electrical circuitry through the conductors inside the connector housing to at least some of the first set of electrical contact elements.

19. The method of claim 18, including arranging one of the first and second sets of electrical contact elements for connection to corresponding terminals on an outside printed circuit board associated with one of the first and the second data handling systems.

20. The method of claim 18, including arranging one of the first and second sets of electrical contact elements for connection to an outside cable connector associated with one of the first and the second data handling systems.

21. The method of claim 18, including arranging a selected one of the first and second sets of electrical contact elements in the form of insulation displacement elements, piercing an insulated cable associated with one of the data handling systems with the displacement elements and electrically contacting the displacement elements with corresponding conductors inside the cable.

22. The method of claim 18, wherein one of said converting steps includes converting serial data into corresponding parallel data, and the other one of said converting steps includes converting parallel data into corresponding serial data.

23. The method of claim 12, including converting by way of the electrical circuitry the voltage level of the data signals transmitted to at least some of the first set of electrical contact elements from a first voltage level into a second voltage level and providing the corresponding data signals at the second voltage level to at least some of the second set of electrical contact elements through the conductors inside the connector housing, and converting by way of the electrical circuitry the voltage level of the data signals transmitted to at least some of the second set of electrical contact elements from the second voltage level into the first voltage level and providing the corresponding data signals at the first voltage level to at least some of the first set of electrical contact elements through the conductors inside the connector housing.

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(54) **CONNECTOR INTERFACE**

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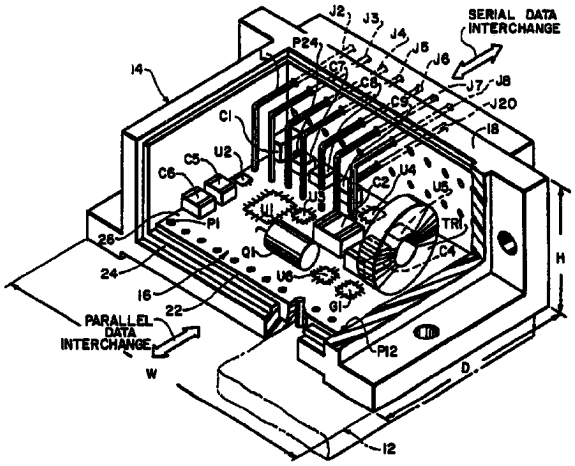
(57) **ABSTRACT**

A connector interface for enabling communications between first and second data handling systems wherein the data in the first system is arranged in a first type of format and the data in the second system is arranged in a second type of format, includes a connector housing with first and second sets of electrical contact elements exposed at different portions of the housing. Circuitry contained entirely within the housing operates to convert data transmitted to the first set of contact elements from the first data handling system into corresponding data in the second type of format for transmission to the second data handling system through the second set of contact elements, and to convert data transmitted to the second set of contact elements from the second data handling system into corresponding data in the first format for transmission to the first data handling system. One set of electrical contact elements may, for example, be arranged to extend out from the connector housing in two parallel rows to allow the elements to be directly connected to corresponding terminals arranged in a dual in line configuration on an outside printed circuit board. The connector arrangement greatly simplifies the design and construction of data processing systems requiring specific interfaces between certain parts of the systems, such as between data terminal equipment and data communication equipment employing serial binary data interchange.



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EX PARTE REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

NO AMENDMENTS HAVE BEEN MADE TO THE PATENT

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

The patentability of claims **1–23** is confirmed.

* * * * *

United States Patent [19]

Brandt

[11] **Patent Number: 4,543,450**

[45] **Date of Patent: Sep. 24, 1985**

[54] **INTEGRATED CONNECTOR AND MODEM**

[76] Inventor: **Randy Brandt**, 1607 Dressage, Orange, Calif. 92669

[21] Appl. No.: **571,867**

[22] Filed: **Jan. 18, 1984**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 433,817, Jan. 3, 1983, abandoned.

[51] **Int. Cl.**[4] **H04M 11/00**
[52] **U.S. Cl.** ..... **179/2 C**
[58] **Field of Search** ..... 179/2 C, 2 DP, 184, 179/186; 375/8, 9

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Primary Examiner—Gene Z. Rubinson
Assistant Examiner—W. J. Brady
Attorney, Agent, or Firm—K. H. Boswell; Edward D. O'Brian

[57] **ABSTRACT**

A data communication device which includes a terminal housing having a terminal connector forming a part thereof, with a modem located in the housing so as to be physically and electrically connected to a data terminal or computer when the terminal connector is connected to the data terminal or computer. A telephone cable having a plug means at one end so as to connect to a modular telephone is connected via its other end to the housing so as to be electrically connected to the modem.

8 Claims, 5 Drawing Figures

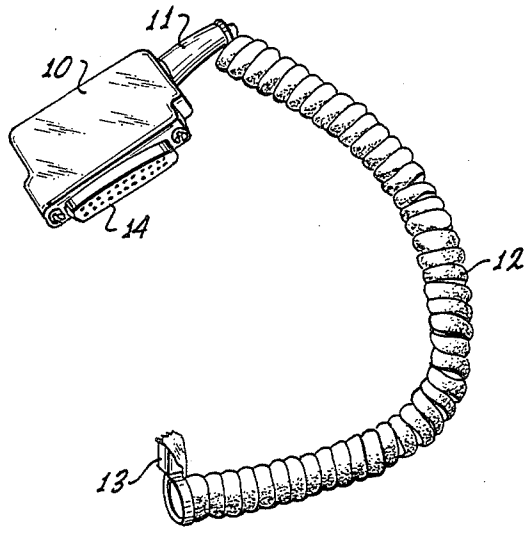

EXHIBIT B

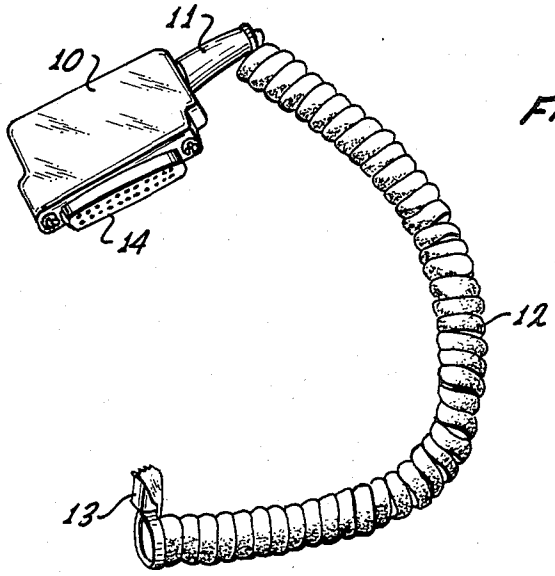

Fig. 1

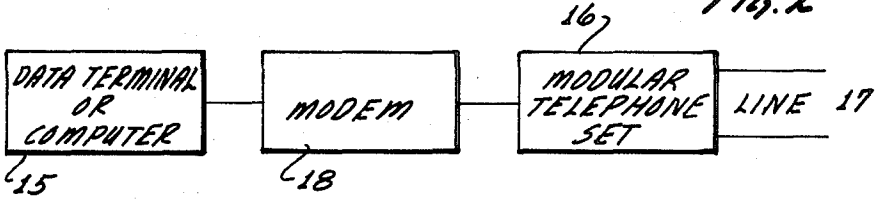

Fig. 2

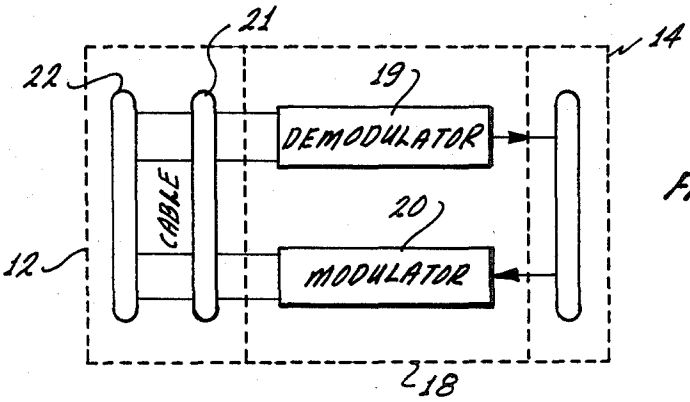

Fig. 3

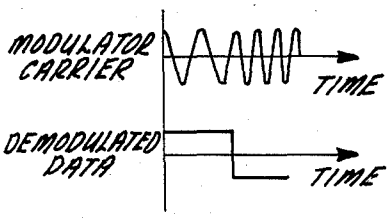

Fig. 4A

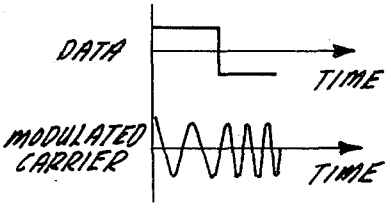

Fig. 4B

INTEGRATED CONNECTOR AND MODEM

CROSS REFERENCE TO RELATED APPLICATION

This application is a continuation in part of my application Ser. No. 433,817, abandoned filed Jan. 3, 1983, and entitled, "Instacom Modem Cable", the entire disclosure of which is herein incorporated by reference.

BACKGROUND OF THE INVENTION

This invention relates to a data communication device which includes a terminal housing having a terminal connector forming a part thereof, with a modem located in the housing so as to be physically and electrically connected to a data terminal or computer when the terminal connector is connected to the data terminal or computer. Further, a telephone cable having a plug means at one end so as to connect to a modular telephone is connected via its other end to the housing so as to be electrically connected to the modem.

Data communication modems (hereinafter referred to as modems) are well known. These devices are utilized to transfer digital information between separated data terminals or computers by transferring the digital information over a phone line or the like. This is done by utilizing digital modulated analog carrier frequencies to carry the digital signals. Modem transmission techniques are described for example, in Bennett et al, "Data Transmission", McGraw Hill, 1975.

One commonly used modem utilizes acoustic coupling between the modem and the hand set of the telephone to acoustically exchange modulated carrier signals between the modem and the telephone hand set.

A further modem utilizes a housing which is located near a data terminal or computer and couples with the data terminal and computer via a ribbon cable having an appropriate connector on the end. A further connection then is made between the modem housing and a telephone. This modem requires an external power source which normally entails the use of a transformer to step down the voltage from a common electrical line to the voltage which is utilized to drive the modem.

As data communication systems become more complex, it has become desirable and necessary to reduce the physical size of the same, to reduce the power consumption of the same, and to reduce the number of components so as to reduce the cost and complexity of the device.

BRIEF DESCRIPTION OF THE INVENTION

In view of the above, it is a broad object of this invention to provide a data communication modem having a reduction in the number of components thus reducing size, costs and power consumption. It is a further object of this invention to provide a modem which is directly attachable to a data terminal or computer so as to eliminate the necessity of having a separate component box which must be physically located close to but separate from the data terminal or computer, taking up valuable shelf space, desk space or the like. Further it is an object of this invention to provide a modem which can be powered directly utilizing the power supply of the data terminal or computer or of a telephone set.

These and other objects, as will become evident from the remainder of this specification are achieved in a data communication device which comprises: a connector housing; a terminal connector located on said connector housing for physically and electrically connecting said connector housing to an input/output interface port of a data terminal or a computer; said connector housing sized and shaped so as to be supportable on said interface port by said terminal connector; modem means located in said connector housing in direct electrical association with said terminal connector; a phone cable having ends, one of said ends attachable to said connector housing in electrical association with said modem means, the other of said ends including a phone connector plug means for electrically connecting said cable to a modular telephone set.

In the preferred embodiment of the invention, a data communication modem is provided which is miniaturized, utilizes low voltage power and is directly formed as a part of a 25 pin "D" connector such that it can be connected directly to a data terminal or computer. Further, the phone cable can utilize a USOC plug for direct connection to the hand set port of a standard modular telephone set. This allows direct connection to the telephone set, eliminating distortion effects caused by acoustics and also eliminates interferences caused by ambient noise and the like.

DETAILED DESCRIPTION OF THE DRAWINGS

This invention will be better understood when taken in conjunction with the drawings wherein:

FIG. **1** is a plan view of the modem of this invention;

FIG. **2** is a diagrammatic view showing a functional data communication systems utilizing the modem of FIG. **1**;

FIG. **3** is an electrical schematic of the modem of FIG. **1**; and

FIG. **4** shows the relationship between input/output data and carrier components utilized by the modem of FIG. **1** for transferring data.

The invention described in this specification and shown in the drawings utilizes certain principles and/or concepts as are set forth in the claims appended to this specification. Those skilled in the electronic arts will realize that these principles and/or concepts are capable of being utilized in a variety of embodiments which may differ from the embodiment utilized for illustrative purposes herein. For this reason, this invention is not to be construed as being limited to only the illustrative embodiment, but is only to be construed as being limited by the claims.

DETAILED DESCRIPTION OF THE INVENTION

In FIG. **1**, an embodiment of the invention is shown which utilizes low power electronic modem circuits packaged as a microcircuit so as to be directly connectable to a data terminal or computer. The modem of the embodiment of FIG. **1** utilizes a housing **10** which accepts a jack **11** attached to one end of a phone cable **12** which has a USOC plug **13** at its other end. Located on the housing **10** is common 25 pin (D) connector, such as an RS-232-C connector. This embodiment is such that the RS-232-C connector **14** can be directly attached to an input/output interface port of a data terminal or computer with the housing **10** then physically connected to the interface port by the connector **14**.

Located within the interior of the housing **10** is a modem **18**. Because the connector **14** and the housing **10** are assembled as a single unit with the modem **18**

located in the housing **10**, when the connector **14** is attached to the data terminal or computer, this directly physically and electrically attaches the modem **18** to the data terminal or computer. This eliminates the necessity of having a separate independent structure to house the modem **18** thus decreasing the complexity of a communications system.

The jack **11** makes an appropriate electrical connection between the cable **12** and the modem **18**. The USOC plug **13** can then be connected to the hand set plug of a modular telephone set.

The cable **12** is shown as a common stretch cable which allows for linkage of the housing **10** after it is connected via the connector **14** to an input/output connecting port of a data terminal or computer with an appropriate telephone set. By utilizing the embodiment of FIG. **1**, the cable **12** is the only hardware necessary to connect the data terminal or computer to the telephone set. This is in contrast to commonly utilized modems wherein, in addition to a cable connecting to the telephone set, a further flat ribbon cable must be utilized to connect to the data terminal or computer and a power cord must be connected to the modem for supplying power thereto.

For the embodiment of FIG. **1**, one of the pins on the connector **14** is matched to an appropriate socket in the interface port of the data terminal or computer which is connected to an appropriate power supply within the data terminal or computer so as to supply electrical power to the modem **18**. This eliminates the need of having an external power cord to supply power to the modem **18**. Alternatively, power could be fed to the modem **18** via cable **12** from the transmitter (microphone) side of the telephone set **16**. It is preferred however, to supply power via the connector **14**.

In FIGS. **2** and **3**, a communications system is shown in FIG. **2** which utilizes the modem of FIG. **1** with the schematic of the modem of FIG. **1** then shown in FIG. **3**. A common telephone line **17** feeds a modular telephone set **16** which is connected to the modem **18**, with the modem **18** then being connected to the data terminal or computer. The lines **21** and **22** within the cable **10** are appropriately connected to a demodulator **19** and a modulator **20** located within the modem **18**. These are then connected to appropriate pins or the like, designated by the numeral **23**, within the connector **14**.

Incoming and outgoing data modulated carrier signals terminate and originate, respectively, at the modem **18**. The information bearing modulated carrier signals are either detected for incoming transmission from the telephone **16** or generated for outgoing transmissions from a data source such as a computer or data terminal **15**.

To transfer data using the system of this invention, the modulated carrier signals enter and exit the modem through the telephone set **16** utilizing the cord and plug assembly **12** and **13**, respectively.

An inbound modulated carrier (similar to FIG. **4A**) would enter the system from the telephone or communications network **17** through the telephone set **16** which projects the modem from line hazards, and provides the necessary coupling and impedance matching. The carrier signal is then transmitted to the USOC plug **13** and cable **12** into the demodulator **19** of the modem **18** which is inside the connector housing **10**. The demodulator **19** interrogates the carrier signal and reconstructs an exact replica of the data being sent over the telephone network **17** by the modulated carrier signal which originated at another location. This data (FIG. **4A**) presents itself on a single output pin on connector **14** which is connected to the receiving computer or data terminal **15**.

When the data transmission is to be generated at the computer or data terminal **15**, the data from the computer or data terminal **15** is presented to a single pin on modem connector **14** different from the receive data pin. The data is then transmitted to the modulator **20** also located inside of the connector housing **10**. The modulator **20** generates a suitable carrier signal (FIG. **4B**) for transmission. The data modulated carrier signal is then transmitted to the telephone set **16** through cable **12** and plug **13**. This signal is then coupled by the telephone set **16** to the telephone network **17**.

I claim:

1. A data communication device which comprises:
a connector housing;
a portion of said connector housing forming a terminal connector for physically and electrically connecting said connector housing to an input/output interface port of a data terminal or a computer;
together said connector housing and said terminal connector sized and shaped so as to be supportable on said interface port by said terminal connector;
a modem means sized and shaped so as to be located in the interior of said connector housing in direct electrical association with said terminal connector;
a phone cable having ends, one of said ends attachable to said connector housing in electrical association with said modem means, the other of said ends including a phone connector plug means for electrically connecting said cable to a modular telephone set.

2. The device of claim **1** wherein:
said device further includes a power supply connecting means for supplying electrical power to said modem means.

3. The device of claim **2** wherein:
said power supply connecting means comprises said terminal connector including a power connector means located on said terminal connector so as to be connectable to said data terminal or computer to receive electrical power from said data terminal or computer.

4. The device of claim **1** wherein:
said terminal connector comprises a 25 pin "D" connector.

5. The device of claim **4** wherein:
said 25 pin "D" connector comprises an RS-232-C connector.

6. The device of claim **5** wherein:
at least one of said pins of said RS-232-C connector is electrically coupled between said data terminal or computer and said modem means when said terminal connector is connected to said interface port of said data terminal or computer so as to supply electrical power from said data terminal or compute to said modem means.

7. The device of claim **1** wherein:
said phone connector plug means comprises a USOC modular plug.

8. The device of claim **5** wherein:
said phone connector plug means comprises a USOC modular plug.

* * * * *

United States Patent [19]

Farago

[11] **Patent Number: 4,972,470**

[45] **Date of Patent: Nov. 20, 1990**

[54] **PROGRAMMABLE CONNECTOR**

[76] Inventor: **Steven Farago**, 171 Forest Dr., Mount Kisco, N.Y. 10549

[21] Appl. No.: **83,258**

[22] Filed: **Aug. 6, 1987**

[51] **Int. Cl.**[5] **H04L 9/00**

[52] **U.S. Cl.** **380/3**; 380/52; 310/71; 439/189; 364/240.8

[58] **Field of Search** 380/3, 52; 310/71; 439/189; 364/240.8

[56] **References Cited**

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4,691,355	9/1987	Wirstrom et al.	380/23
4,694,492	9/1987	Wirstrom et al.	380/23

Primary Examiner—Thomas H. Tarcza
Assistant Examiner—David Cain
Attorney, Agent, or Firm—Israel Nissenbaum

[57] **ABSTRACT**

A configurable connector between two or more devices with at least one of the devices being capable of programming the connector through an interface therewith. The connector contains programmable electronic circuitry capable of being instructed by the device whereby the connector assumes a desired connecting configuration and/or function. In one embodiment the connector is programmed to inquire and determine the configuration of the device to which it is connected. With the results of its analysis the connector adapts the necessary timing, pin-outs, voltages, and other parameters to assure proper communication between the connected devices. In other embodiments the connector contains electronic components to add specific functions for data exchange, such as data buffering, data encryption and the like. In addition, the connector is programmable with interchangeable pin designations thereby obviating the need for rewiring for different applications and physical connections.

13 Claims, 4 Drawing Sheets

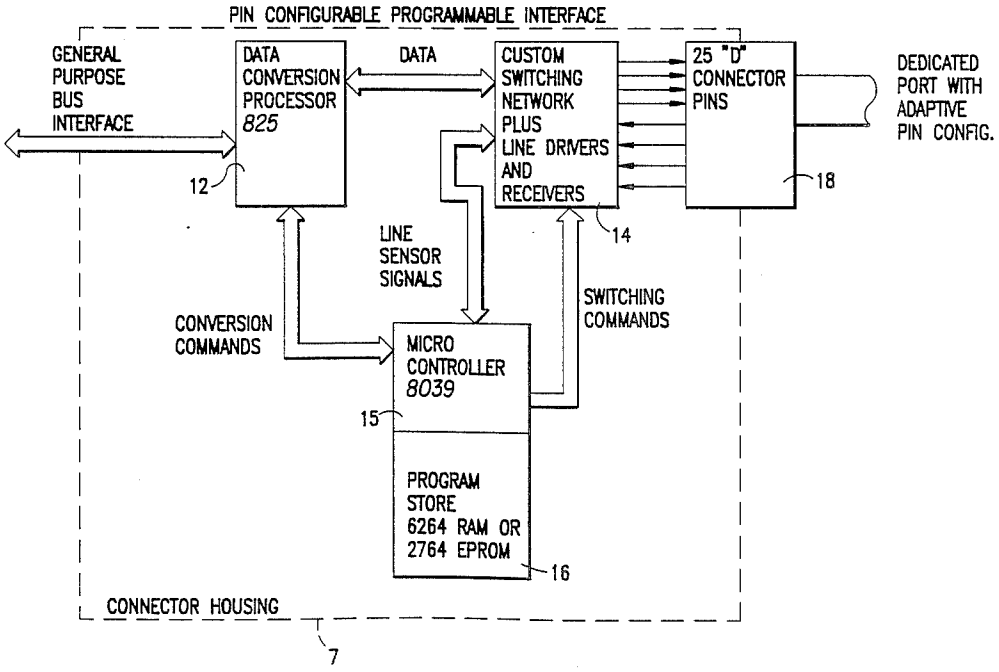

EXHIBIT C

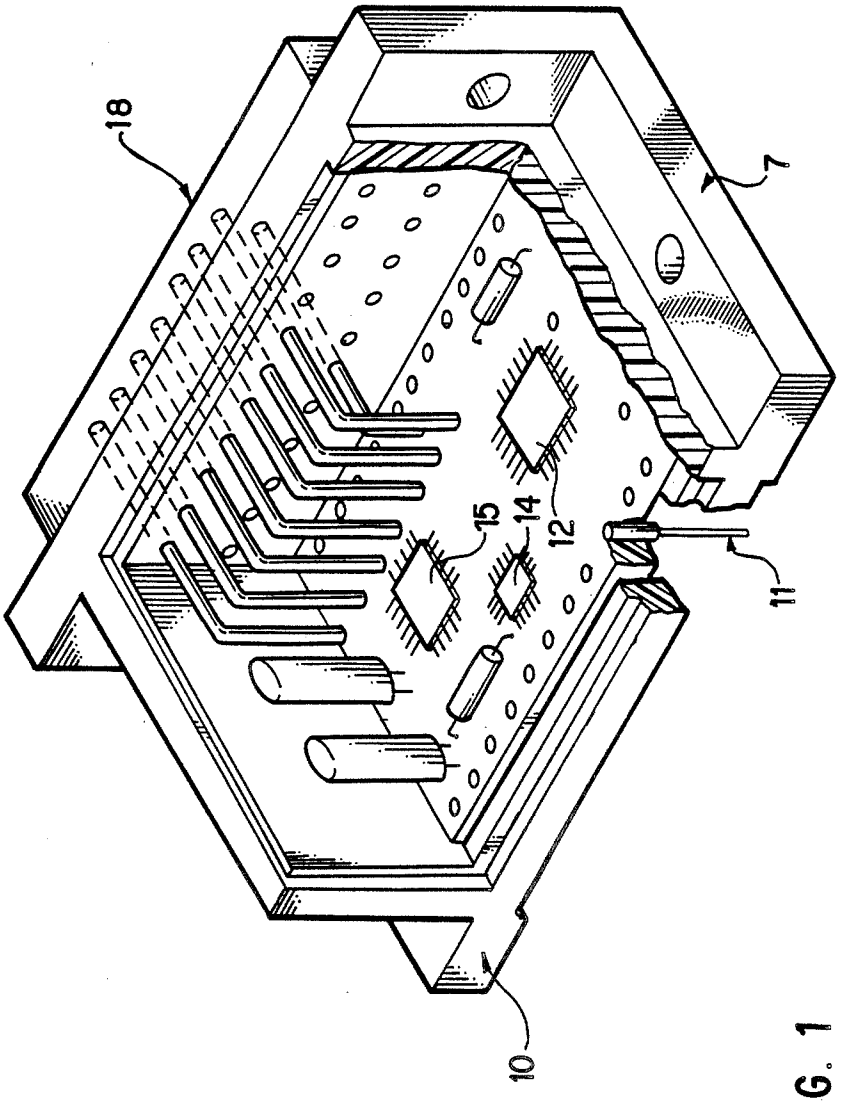

FIG. 1

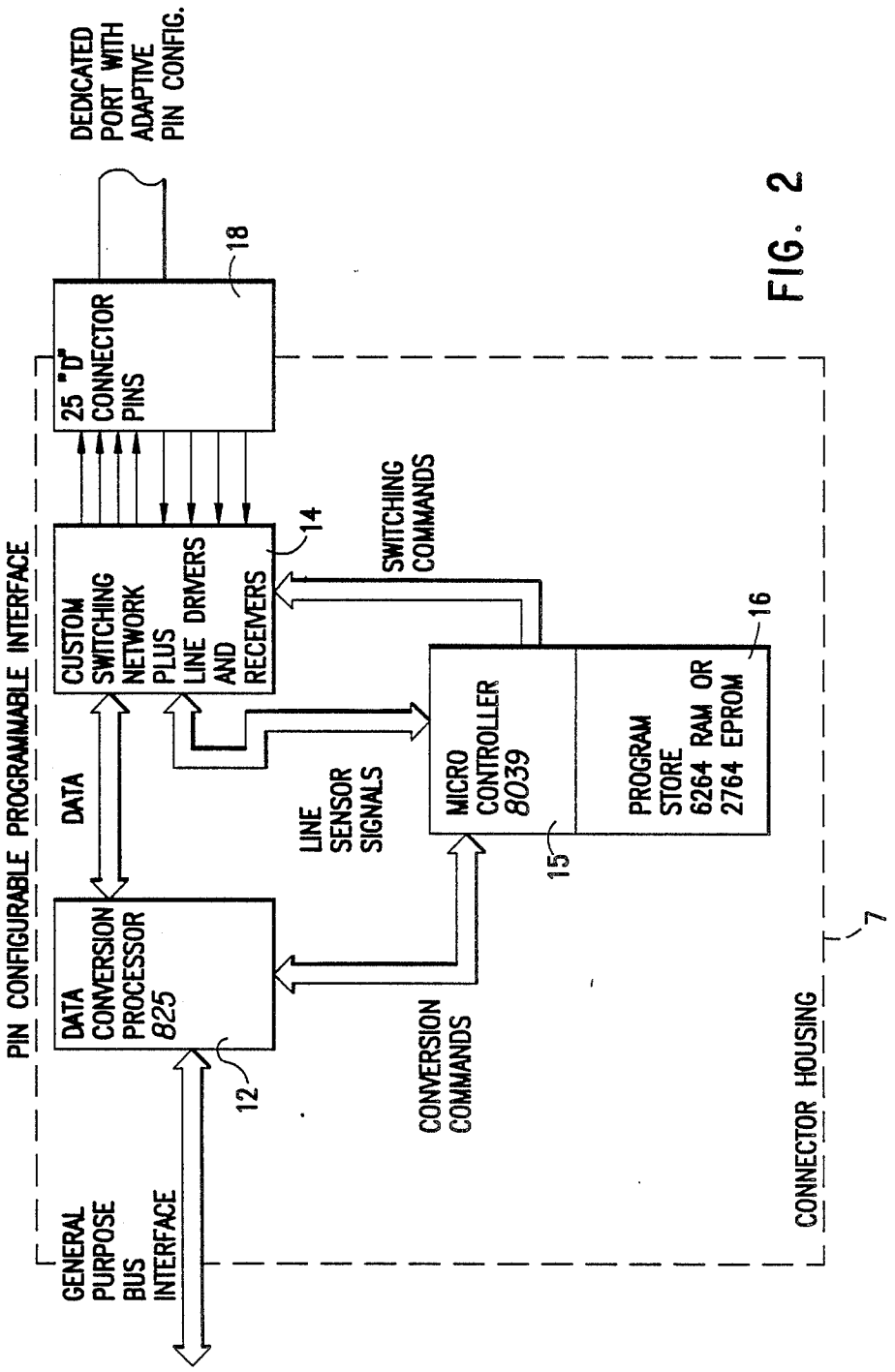
DEDICATED PORT WITH ADAPTIVE PIN CONFIG.
18
25 "D" CONNECTOR PINS
14
CUSTOM SWITCHING NETWORK PLUS LINE DRIVERS AND RECEIVERS
SWITCHING COMMANDS
16
MICRO CONTROLLER 8039
PROGRAM STORE 6264 RAM OR 2764 EPROM
15
DATA
LINE SENSOR SIGNALS
DATA CONVERSION PROCESSOR 825
12
CONVERSION COMMANDS
GENERAL PURPOSE BUS INTERFACE
PIN CONFIGURABLE PROGRAMMABLE INTERFACE
CONNECTOR HOUSING
7

FIG. 2

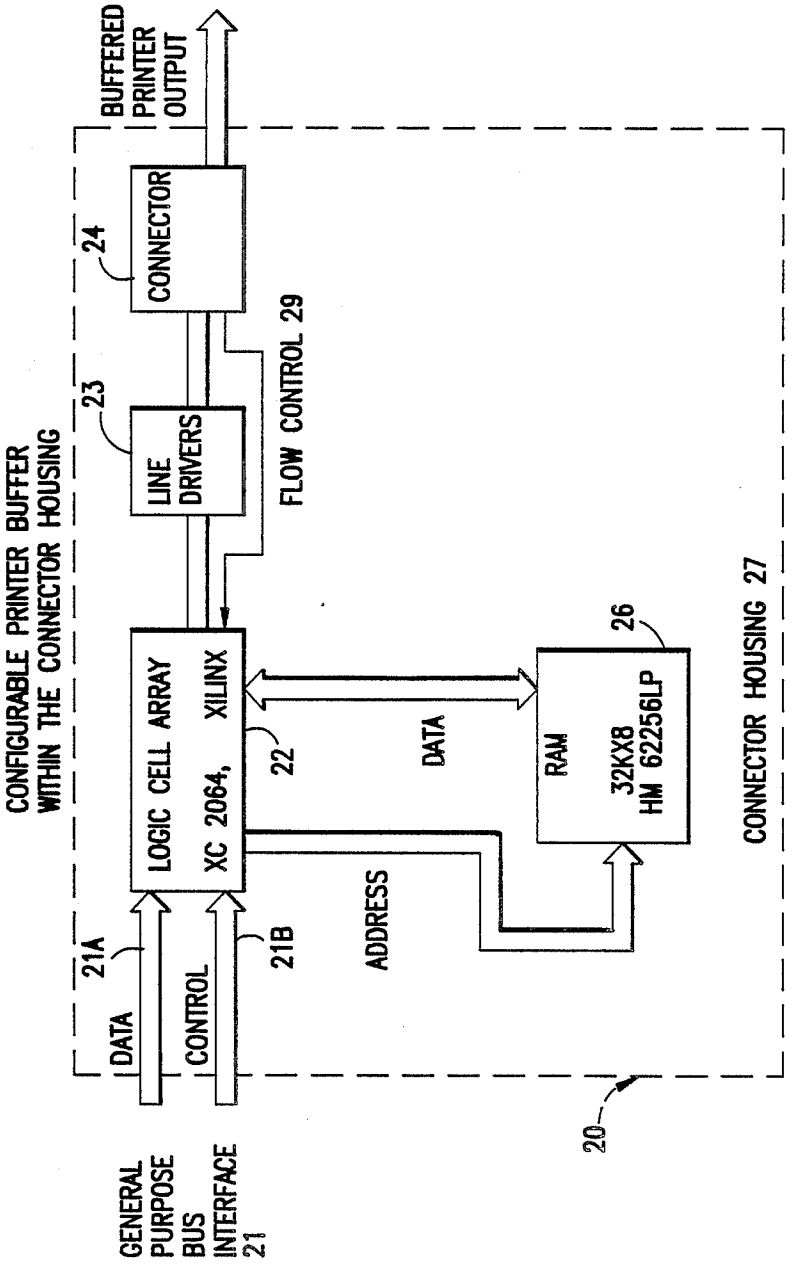
BUFFERED PRINTER OUTPUT
24
CONNECTOR
23
LINE DRIVERS
FLOW CONTROL 29
CONFIGURABLE PRINTER BUFFER WITHIN THE CONNECTOR HOUSING
LOGIC CELL ARRAY XILINX XC 2064,
22
DATA
26
RAM 32KX8 HM 62256LP
CONNECTOR HOUSING 27
21A
DATA
CONTROL
21B
ADDRESS
GENERAL PURPOSE BUS INTERFACE 21
20

FIG. 3a

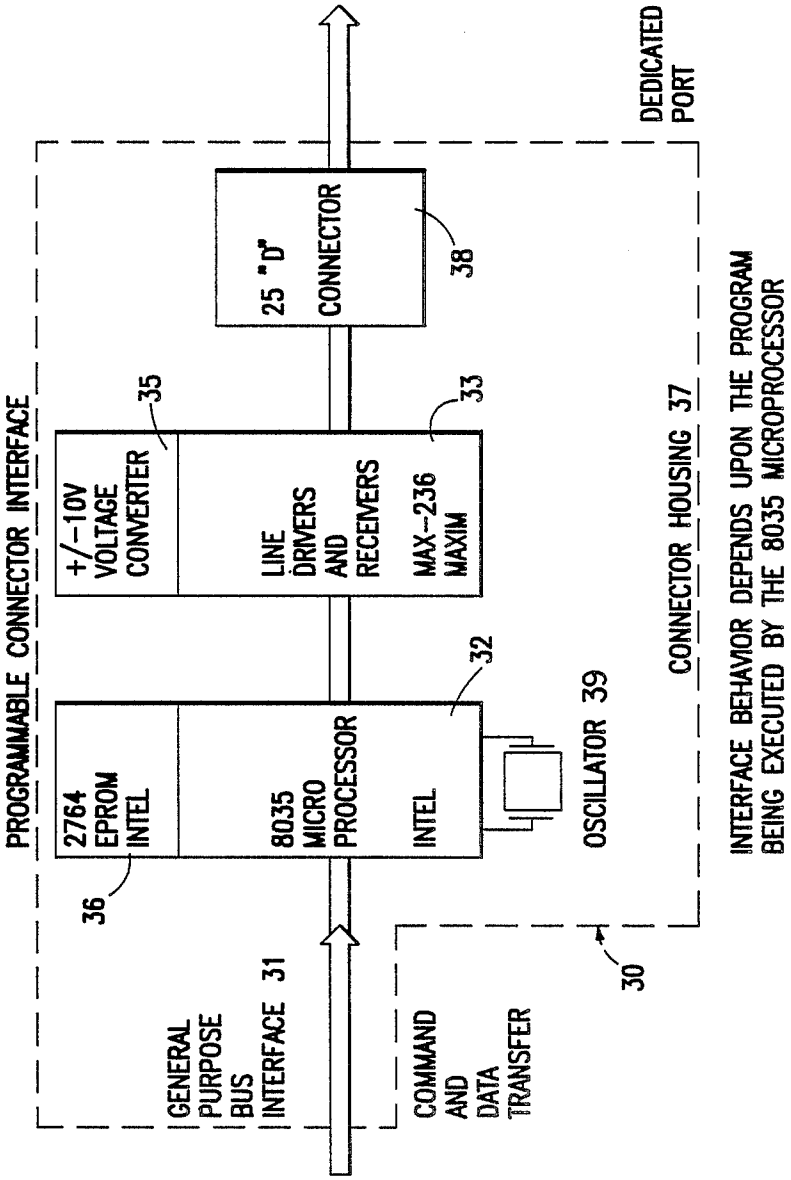
DEDICATED PORT
25 "D" CONNECTOR
38
CONNECTOR HOUSING 37
PROGRAMMABLE CONNECTOR INTERFACE
+/-10V VOLTAGE CONVERTER
35
LINE DRIVERS AND RECEIVERS
MAX-236 MAXIM
33
2764 EPROM INTEL
36
8035 MICRO PROCESSOR
INTEL
32
OSCILLATOR 39
INTERFACE BEHAVIOR DEPENDS UPON THE PROGRAM BEING EXECUTED BY THE 8035 MICROPROCESSOR
GENERAL PURPOSE BUS INTERFACE 31
COMMAND AND DATA TRANSFER
30

FIG. 3b

PROGRAMMABLE CONNECTOR

This invention relates to connectors between devices for the transfer of information therebetween and in particular to the interconnection of computer devices to peripheral devices.

In U.S. Pat. No. 4,603,320, issued on July 29, 1986 and copending application no. 891,190, filed July 28, 1986, a "smart" connector was disclosed wherein the connector contained, within the housing thereof, the requisite electronic circuitry for providing a data conversion between two or more interfaced devices. Such conversions included a conversion between parallel and serial and between analog and digital data formats. These connectors were however limited to a single hard wired-in conversion application. Thus, while they provided an improvement over the common simple electrical current connectors, they were nevertheless limited to a single operative function.

It is an object of the present invention to provide a connector between devices which is capable of being externally programmed or instructed to adapt itself into a desired connecting configuration and/or function between the devices.

It is a further object of the present invention to provide a connector which, when externally activated, is programmed to inquire and determine the requisite connecting function and to reconfigure itself accordingly.

These and other objects, features and advantages of the present invention will become more evident from the following discussion and drawings in which:

FIG. 1 schematically depicts the internal components of a programmable connector in accordance with the present invention;

FIG. 2 is a block diagram showing the program/configuration supplied to the device of FIG. 1; and

FIGS. 3*a–b* are block diagrams showing specific programmable connector functions.

Generally the present invention comprises a connector having a housing which contains at least two physical interface connection elements such as electrical pins and socket connections, through the walls thereof, for connection to at least two external devices. The connector further contains, within the housing thereof, programmable means remotely accessible by at least one of said devices whereby instructions are sent to the programmable means whereby the function or configuration of the connector is changed thereby as desired. The programmable means is preferably a general purpose electrical circuitry with or without the ability to erase and reprogram it. The loaded program determines the specific function of the connector and the programming can be performed in several ways. For example, the connector may be one-time programmed. In another embodiment the connector is electrically programmed and later erased for reconfiguration. If desired, the program is either downloaded at every power-on cycle, or reconfigured "on the fly".

A significant feature is the ability of the programmable connector of the present invention to inquire and determine the characteristics of the interfaced devices whereby intelligent firmware can find the right connection without cable swapping or rewiring. In addition, the connector automatically adapts the necessary timing, voltages etc. to ensure a proper connection. A suitable algorithm is incorporated or downloaded and

stored in a non-volatile manner such as an EPROM or by battery backed RAM. In such embodiments a microprocessor with EPROM is located within the connector housing with the EPROM (or factory programmed mask prom/rom) containing the program that performs the desired interface function. Different programs in the EPROM result in different interface functions. Alternatively, there is a programmable logic array inside the connector housing which is for example, one time programmed (PLA) or is RAM based. The RAM based method results in flexibility with the connector being capable of being configured and reconfigured by a simple instruction for changing protocol, parameters or pin-outs. In some embodiments, the external device such as a computer provides for an input means such as a keyboard or a downloading from a storage device which accesses the connector and instructs it to assume the requisite interface function and/or configuration. In other embodiments the connector is programmed to conduct its own inquiries regarding the nature of the connection interface and adapt itself accordingly. In such embodiments the simple act of powering on is considered herein to be an initiation instruction.

Examples of interfaced devices through which interface instructions may be transmitted to the connector include the aforementioned computer with peripheral input devices. Other commonly interfaced devices include modems, printers and the like to which a transmission of data is required. Data input peripherals for such devices as well as hard wired controls can be utilized in properly instructing the connector to assume the requisite interface function and/or configuration.

It is understood that while the functions of pins of a specific interface can be programmed, according to the present invention, to assume a desired electrical connection configuration, the physical characteristics remain unchanged.

In accordance with the present invention several features are embodied within the connector. A programmable and/or configurable device is contained within the housing of the connector. The configurable device is supplied with a program and/or configuration, with the device and the supplied program and/or configuration, performing a specific predetermined function inside the connector. Different programs and/or configurations result in different functions being performed or executed by the connector.

Programmable and/or configurable electronic devices suitable for use within the connector of the present invention include microprocessor chips with program storage memory. Examples of such chips include the Intel 8035, 8049 and 8031 designated chips. The Intel 2764 Eprom is an example of the program storage memory.

A further example of such programmable and/or configurable electronic devices is a microcontroller with downloadable code storage e.g. the Intel 8031 with an 8k x 8 static RAM memory and the Hitachi HM 2-62256. Other examples include programmable array logic (e.g. MMI LCA ZPAL20L8), custom gate array, programmable logic cell array (e.g. XILINK XC-2064 or 2018, MMI LCA M-2064) and erasable programmable logic device (e.g. ALTERA EP-1210 and 1280, and INTEL 5C180).

Various means may be utilized to supply the program or configuration to the programmable or configurable devices. For example, a custom mask is programmed at the manufacturing site and configured into silicon dur-

ing wafer fabrication (ROM principle). Alternatively, the programmable and/or configurable electronic device is one time programmable at the user level by utilizing the fusible link programming method. EPROM technology, as embodied in the 2764 Eprom or Altera EP-1210 parts, is utilizable for electrically programmable and u.v. light erasable devices. A further example is a RAM based configuration storage with downloadable feature, such as the XILINX XC-2064 and the 8031 micro plus 6264 Static RAM. In order to maintain a non-volatile program/configuration an alternative battery backup storage device such as is available from Dallas Semiconductor may be utilized.

Various specific, predetermined programmable functions of the programmable connector of the present invention include:

(a) a user programmable port interface, e.g. serial, parallel, etc;

(b) adaptive pin arrangement via software algorithm and hardware switching network of an input-output structure with the connected device and an algorithm to configure the connector to match the network;

(c) a buffered port interface with the connector providing temporary storage of data to accommodate devices operating at different speeds; and

(d) a data encryption device incorporated in the connector to provide higher levels of security during data transfer.

In accordance with the present invention, different programs installed in the connector can result in different functions of the connector. For example the connector may function as a reconfigurable port whereby one physical hardware interface can change configuration with the same port becoming an RS-232, RS-422, RS-485 protocol or it can even become a Centronic interface. Such configurations and reconfigurations are accomplished by downloading the proper configuration into the programmable connector as desired.

With specific reference to the drawings, FIG. **1** depicts a pin configurable programmable interface connector **10** with housing **7** in which are contained a general purpose bus interface **11** extending through one wall of housing **7** and a second dedicated port **18** with an adaptive pin configuration. As schematically depicted in FIG. **2**, connector housing **7** further contains a data conversion processor **12** having a data interface with custom switching network **14** with line drivers and receivers which, in turn, are interfaced with the connector pins **18**. Microcontroller **15** provides switching commands to the switching network **14** and conversion commands to the data conversion processor **12** and receives line sensor signals from the switching network. Microchip **16** contains an EPROM (e.g. 2764 Eprom) or (6264 Static RAM) RAM to provide the requisite programmed and programmable commands.

FIG. **3***a* schematically depicts the electronic configuration of a printer buffer **20** within a connector housing **27**. A logic cell array **22** (XILINX XC-2064) receives data and control commands from a connected device such as a computer with an input device such as a keyboard or storage element such as a disk drive (not shown), through connections **21***a* and **21***b* respectively of the general purpose bus interface **21**. The logic cell array is in turn linked with a 32k x 8 RAM chip **26** (Hitachi HM-62256 type) which it addresses and sends to and receives data from. The logic cell array sends signals to a buffered printer output **24**, via line drivers **23**, which is in turn connected to the printer for the desired output. A flow control **29** is interfaced between the connector output **24** and the logic cell array **22**. In such embodiment the connector may similarly function as a buffer element between a printer and a data transmitting modem. The logic cell array **22** is configured at every "power-up" sequence via the general purpose bus interface **21** to perform the printer buffer function. The configuration accomplishes a hardware data-control path which is responsible for the desired buffering feature.

FIG. **3***b* further schematically depicts a pin configurable programmable connector interface device **30**. A connector housing **37** contains a general purpose bus interface **31** and a **25** pin "D" connector **38** with a dedicated port for connection to external devices. A microprocessor **32** (Intel 8035) sends and receives commands through bus interface **31** and is in turn electrically connected to line drivers and receivers **33**. EPROM **36** (2764 Eprom) provides the requisite program for the microprocessor **32** to execute. Voltage converter (+10 V) **35** provides power for line drivers and receivers **33** and oscillator **38** povides the timing for the microprocessor **32**. The interface behavior of the connector **30** is dependent upon the program being executed by microprocessor **32**. Thus, EPROM **36** can provide a protocol selection program whereby different connection protocols may be selected for a single connector such as serial, and various serial interface standards such as RS-232, RS-422, RS-485, or even a Centronics parallel interface, etc. for a completely compatible connection between interfaced devices. In a particularly useful embodiment, as data is transmitted through the connector, generally from a computer to a modem for retransmission over communication lines, the program causes the data to be encrypted for secured transmission. With a similarly programmed connector at the receiving end, the data is translated into usable form.

It is understood that the above description and drawings are illustrative of the present invention and details contained therein are not to be construed as limitations on the present invention. Variations in programs, components and structural configurations and the like may be made without departing from the scope of the present invention as defined in the following claims.

What is claimed is:

1. An electronically configurable connector, for connecting at least two discrete external electronic devices, said devices having individual housings and said connector having its own housing which contains at least two physical interface connection elements through the walls thereof, wherein, with the connection of one of the physical interface connection elements with a first one of said devices, at least one other of the physical interface connection elements is exposed externally to said first one of said devices for physical electrical connection with another of said devices; characterized in that said devices, when initially physically connected by said connector, do not electronically communicate with each other as desired; and wherein the connector further comprises electrically programmable means, comprising electronic circuitry with a loaded program, said electronic circuitry being remotely accessible by at least one of said connected devices whereby electrical instructions are sent thereto for interpretation by the loaded program, with operational instructions being generated, whereby the electronic circuitry causes modification of the connection between the connected devices to provide the function or configuration of the

connector for communication between the connected devices as desired.

2. The connector of claim **1** wherein said programmable electrically means, after receiving said electrical instructions, causes said connector to function as a printer buffer between a printer, which comprises one of said external devices, and a data transmission device which comprises another of said external devices.

3. The connector of claim **2** wherein said data transmission device comprises a computer.

4. The connector of claim **2** wherein said data transmission device comprises a modem.

5. The connector of claim **1** wherein said electrically programmable means, after receiving said electrical instructions, causes said connector to function as an encryption device for data transmitted between said external devices.

6. The connector of claim **1** wherein at least one of said physical interface connection elements comprises multiple pin outputs and wherein said electrically programmable means, after receiving said electrical instructions, causes said connector to electrically reconfigure itself between said physical interface connection elements whereby the configuration of said multiple pin outputs is reconfigured as desired.

7. The connector of claim **1** wherein said electrically programmable means comprises a microprocessor with program storage memory.

8. The connector of claim **1** wherein said electrically programmable means comprises a microcontroller with downloadable code storage.

9. The connector of claim **1** wherein said electrically programmable means comprises a programmable array logic.

10. The connector of claim **1** wherein said electrically programmable means comprises a custom gate array.

11. The connector of claim **1** wherein said electrically programmable means comprises a programmable logic cell array.

12. The connector of claim **1** wherein said electrically programmable means comprises an erasable programmable logic device.

13. The connector of claim **1** wherein the connector and its housing are external to all of the connected devices.

* * * * *

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(12) EX PARTE REEXAMINATION CERTIFICATE (5028th)

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Farago

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(54) **PROGRAMMABLE CONNECTOR**

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(58) **Field of Search** 710/2, 8, 11, 14, 710/62, 63, 70, 71; 380/52, 266; 439/189, 955; 341/100, 101; 370/366; 713/192

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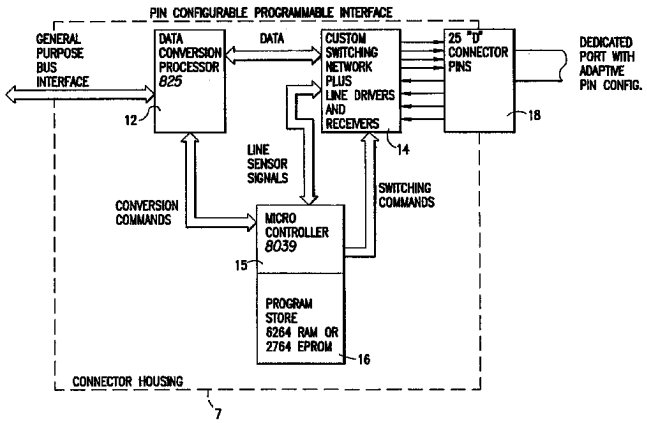
Primary Examiner—Fritz M. Fleming

(57) **ABSTRACT**

A configurable connector between two or more devices with at least one of the devices being capable of programming the connector through an interface therewith. The connector contains programmable electronic circuitry capable of being instructed by the device whereby the connector assumes a desired connecting configuration and/or function. In one embodiment the connector is programmed to inquire and determine the configuration of the device to which it is connected. With the results of its analysis the connector adapts the necessary timing, pin-outs, voltages, and other parameters to assure proper communication between the connected devices. In other embodiments the connector contains electronic components to add specific functions for data exchange, such as data buffering, data encryption and the like. In addition, the connector is programmable with interchangeable pin designations thereby obviating the need for rewiring for different applications and physical connections.



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EX PARTE REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

NO AMENDMENTS HAVE BEEN MADE TO THE PATENT

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

The patentability of claims **1–13** is confirmed.

* * * * *

United States Patent [19]

Farago

[11] **Patent Number: 4,686,506**

[45] **Date of Patent: Aug. 11, 1987**

[54] **MULTIPLE CONNECTOR INTERFACE**

[75] Inventor: **Steven Farago**, Mount Kisco, N.Y.

[73] Assignees: **Anico Research, Ltd. Inc.**, Mount Kisco; **Rapitech Systems Inc.**, Suffern, both of N.Y. ; a part interest to each

[21] Appl. No.: **891,190**

[22] Filed: **Jul. 28, 1986**

Related U.S. Application Data

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[51] **Int. Cl.**[4] **H03K 13/24**

[52] **U.S. Cl.** ..... **340/347 DD**; 361/394; 439/620

[58] **Field of Search** ..... 340/347 DD; 339/17 R, 339/17 C, 17 F, 14 R, 17 M, 17 LC, 17 N, 176 R, 176 M, 176 MP; 361/392–395, 412, 415; 364/705, 771; 179/20 P

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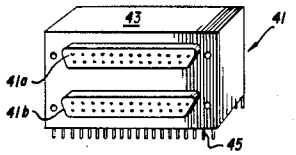
Primary Examiner—Vit W. Miska

Attorney, Agent, or Firm—Israel Nissenbaum

[57] **ABSTRACT**

A connector interface for enabling multiple conversions between first and second data handling systems wherein the data in the first system is arranged in a first type of format and the data in the second system is arranged in a second type of format, includes a connector housing with first and second sets of electrical contact elements exposed at different portions of the housing. Circuitry contained entirely within the housing operates to convert data transmitted to the first set of contact elements from the first data handling system into corresponding data in the second type of format for transmission to the second data handling system through the second set of contact elements, and to convert data transmitted to the second set of contact elements from the second data handling system into corresponding data in the first format for transmission to the first data handling system. One set of electrical contact elements may, for example, be arranged to extend out from the connector housing in two parallel rows to allow the elements to be directly connected to corresponding terminals arranged in a dual in line configuration on an outside printed circuit board. The other set of electrical contact elements may be arranged for multiple simultaneous or selective output connections for applications such as multiple communication, digital to analog and analog to digital conversions, and a multiple floppy disk controller.

13 Claims, 16 Drawing Figures



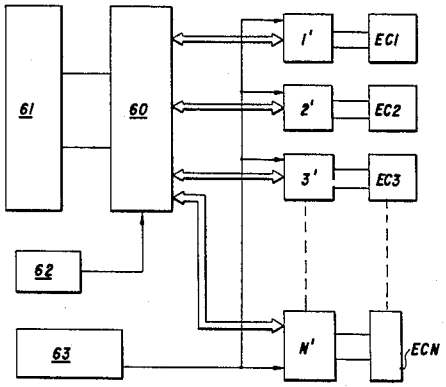


EXHIBIT D

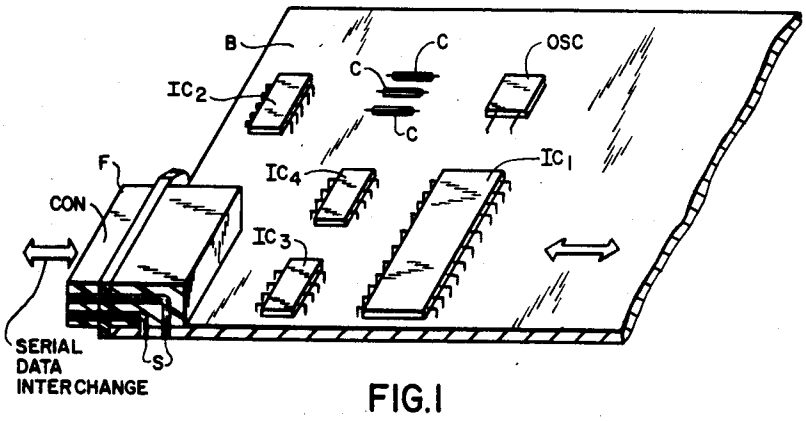
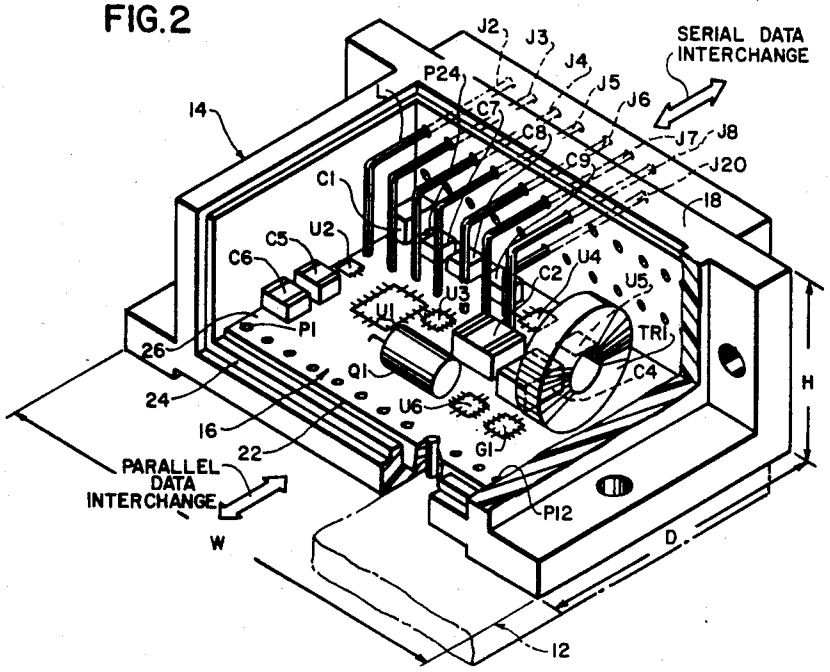
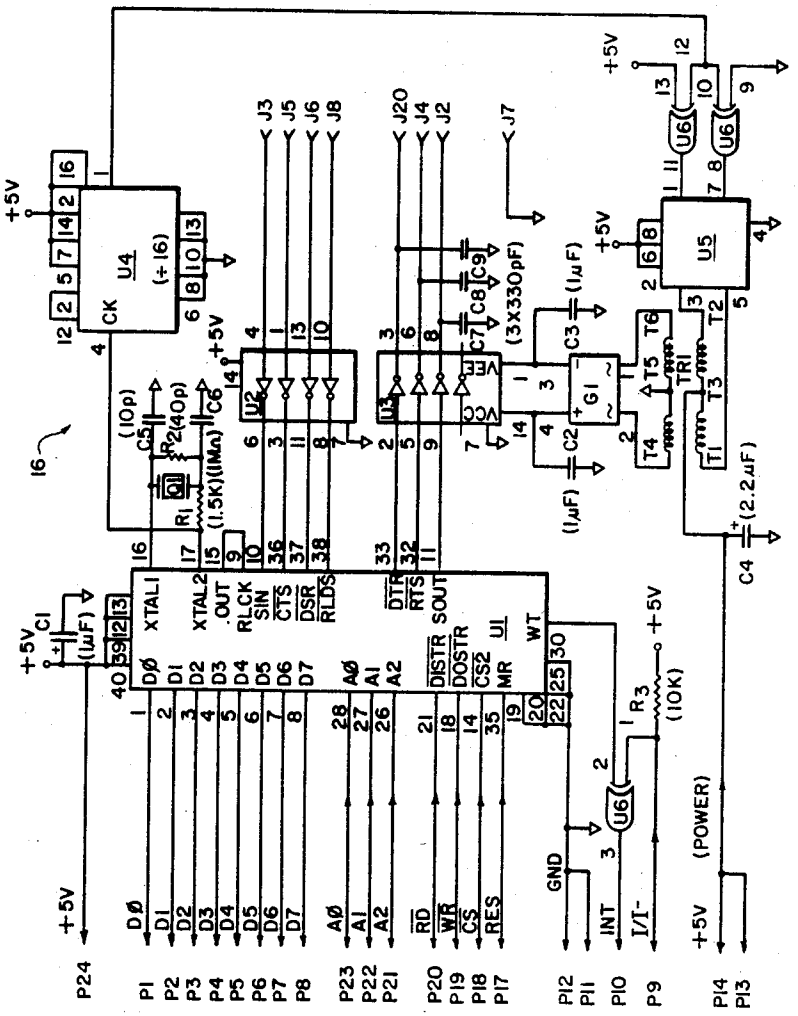


FIG.1
PRIOR ART

FIG.2




+5V
U4
(÷16)
CK
U5
U6
U1
U2
U3
G1
J3
J5
J6
J8
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J4
J2
J7
C1
C2
C3
C4
C5
C6
C7
C8
C9
R1
R2
R3
(10K)
(3X330pF)
(1μF)
(2.2μF)
(10p)
(40p)
(1.5K)
(1MΩ)
XTAL1
XTAL2
RLCK
SIN
CTS
DSR
RLDS
DTR
RTS
SOUT
DISTR
DOSTR
CS2
MR
WT
RD
WR
CS
RES
INT
GND
(POWER)
I/T-
TRI
T1
T2
T3
T4
T5
T6
P24
P1
P2
P3
P4
P5
P6
P7
P8
P23
P22
P21
P20
P19
P18
P17
P12
P11
P10
P9
P14
P13

FIG.3

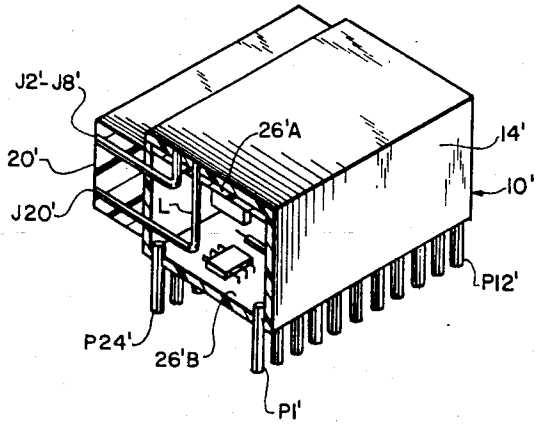


FIG.4

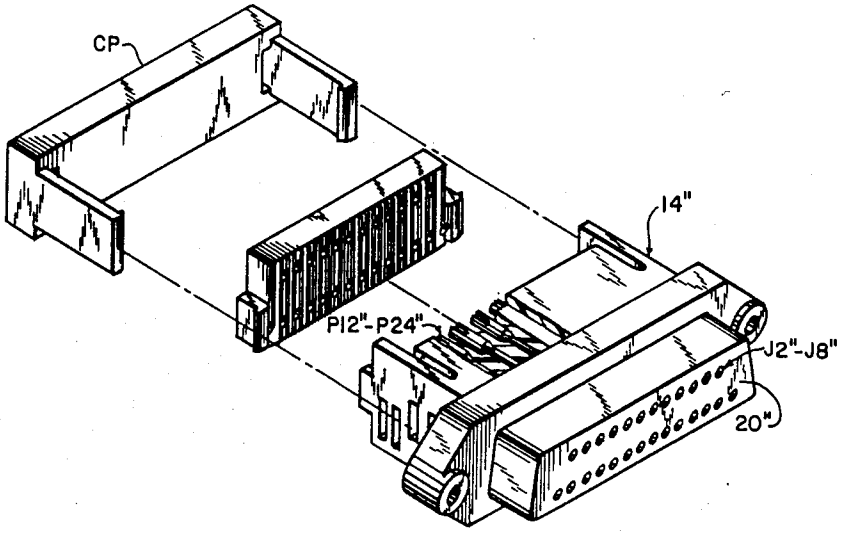
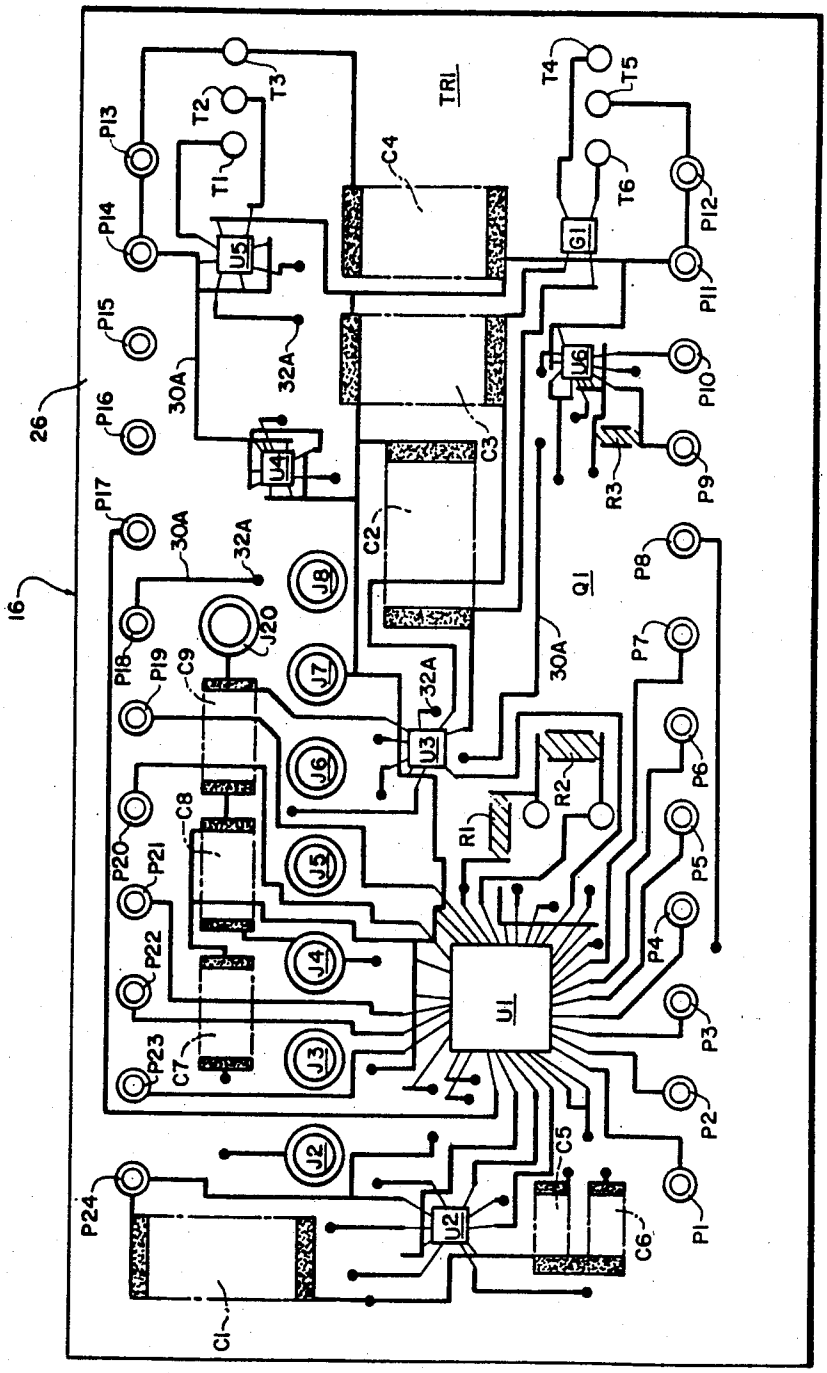


FIG.5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T2
T3
T4
T5
T6
TR1
C4
P13
P14
P15
P16
P17
P18
P19
P20
P21
P22
P23
P24
P12
P11
P10
P9
P8
P7
P6
P5
P4
P3
P2
P1
U5
U4
U6
G1
U3
U2
U1
Q1
J8
J20
J7
J6
J5
J4
J3
J2
C1
C2
C3
C5
C6
C7
C8
C9
R1
R2
R3
30A
32A
26
16

FIG.6A

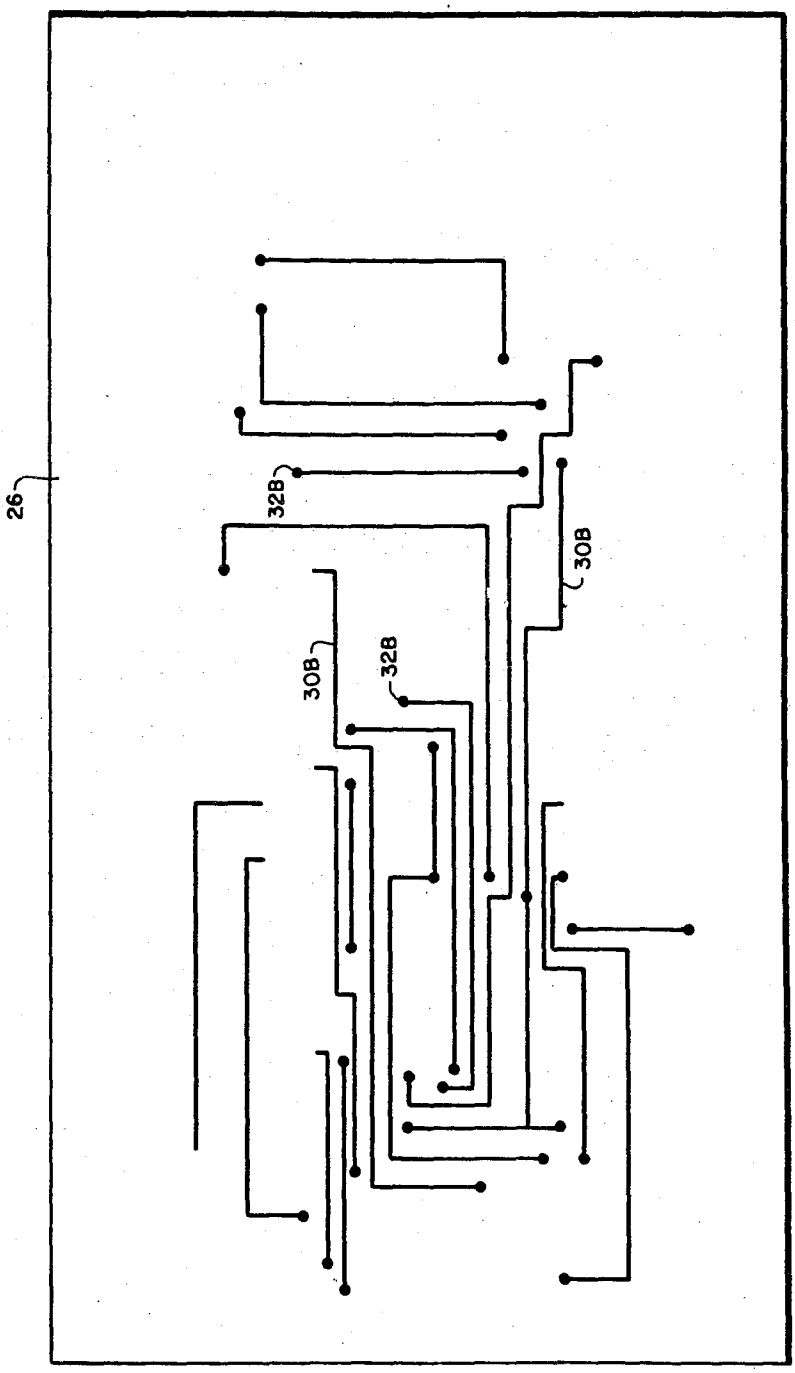
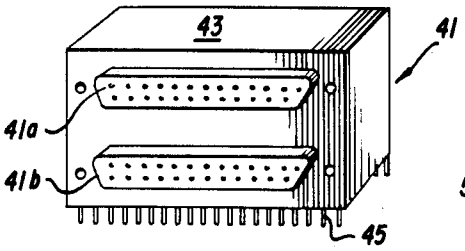


FIG.6B

FIG. 7A



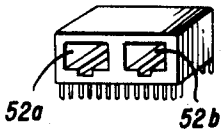


FIG. 8A

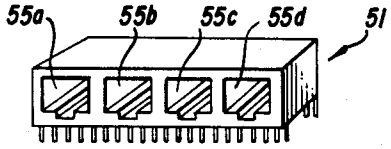


FIG. 8B

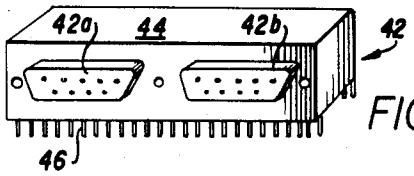


FIG. 7B

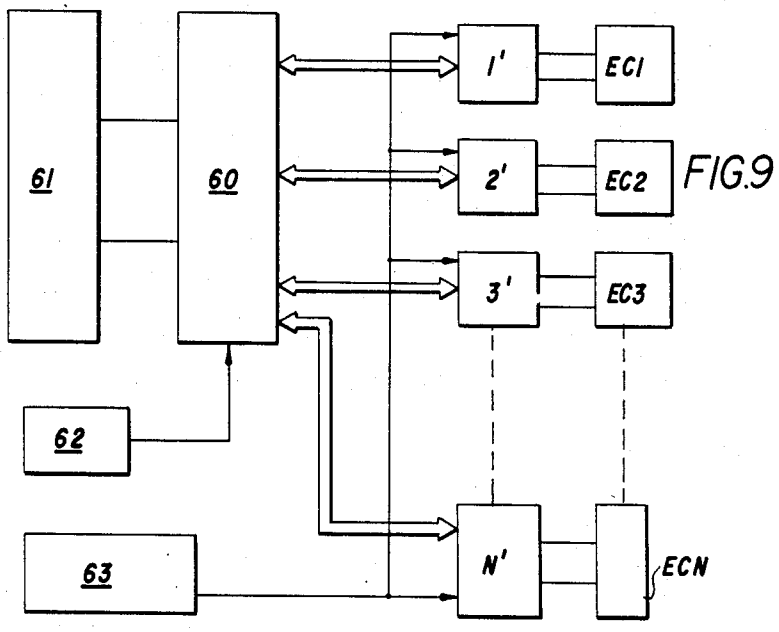


FIG. 9

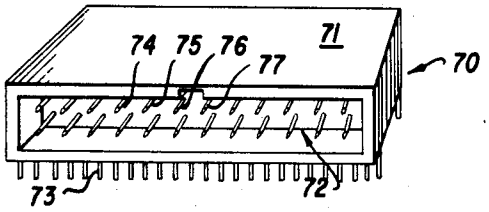


FIG. 10A

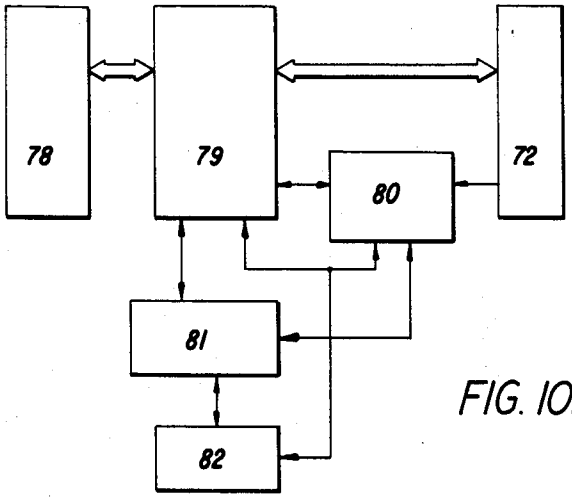


FIG. 10B

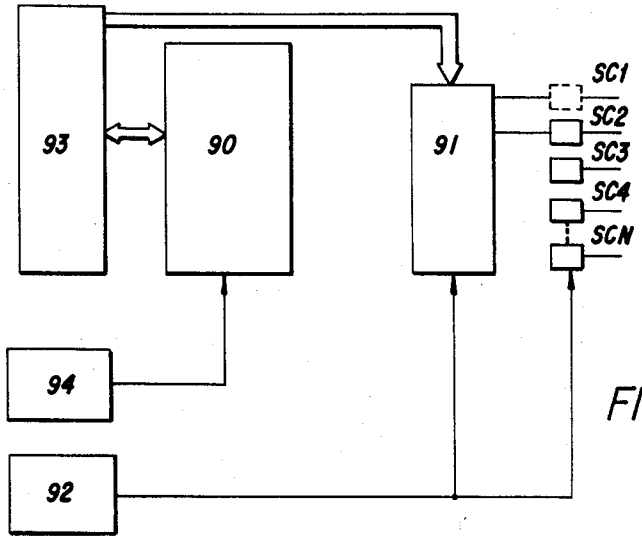


FIG. 11

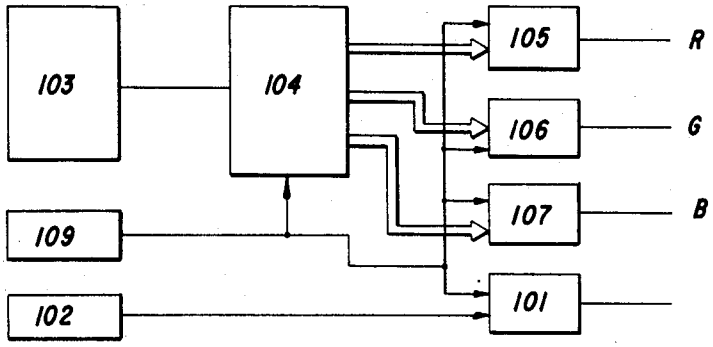


FIG. 12

MULTIPLE CONNECTOR INTERFACE

This is a continuation-in-part of application Ser. No. 484,823 filed April 13, 1983, U.S. Pat. No. 4,603,320.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to electrical connectors, and particularly to a connector having internal circuitry capable of providing a specified electrical interface between various types of data handling equipment.

2. Description of the Prior Art

The proliferation of digital data processing equipment, first in business and now into the home, has created an ongoing demand for such equipment with ever increased capabilities but at an affordable price. The modern trend to integrate numerous discrete electrical components within single semiconductor integrated circuits or "chips", has provided for greater economies in the manufacture of digital electronic equipment. Not only is the overall physical size and weight of the equipment reduced through use of integrated circuit technology, but manufacturing costs also are alleviated in that the price of each integrated circuit used is but a fraction of the total cost represented by all the components it contains.

Digital data processing systems which are in common use today include portions arranged to allow the user to communicate with the system by way of, for example, a terminal or a printer. The user "talks" or provides information to the system through the terminal, and this information is converted into digital data which the system is capable of understanding. After the data is processed by the system which may include some form of computer, a suitable response is transmitted back to the user in digital form and then properly converted into visibly recognizable words or symbols on the screen of the terminal or on a sheet generated by a printer.

Accordingly, it is often necessary to provide cable interconnections between differently located units of a data processing system to allow the units to transmit and receive digital data to and from one another.

Certain types of digital equipment, e.g. a terminal or a printer, transmit or receive digital data in serial bit format. That is, each character (i.e., letter or numeral) of the data is sent or received one bit at a time. It will be appreciated that in a typical system where each character occupies multiple bits, communicating the characters as serial bits between separately located pieces of equipment reduces significantly the number of separate conductors which must be provided in the connecting cables, allows for the communicating equipments to operate in time synchronism with one another with regard to the data exchanged between them, as well as for the use of parity bits and other common error detecting techniques to be applied for each data character communicated. Other kinds of equipment in data handling systems operate in a parallel bit format. For example, computers operate on data which is loaded in internal registers one full character (i.e., eight bits) at a time, and likewise provide output information a character at a time to internal output registers.

In order to insure compatability between terminals, printers and other input/output data handling equipment which operate in a serial bit format, and computer

mainframes and related equipment, the Electronic Industries Association promulgated in 1969 a now widely accepted interface standard known as EIA RS-232-C, the provisions of which are incorporated by reference herein. The RS-232-C Standard, entitled "Interface Between Data Terminal Equipment and Data Communication Equipment Employing Serial Binary Data Interchange", ensures that serial bit format equipment produced by one manufacturer will operate properly with serial bit format equipment of another manufacturer. The RS-232-C Standard applies not only to the interchange of information data signals between data handling equipment, but also to the interchange of timing and control data signals between such equipment (Sec. 1.4 of the Standard).

In order to ensure satisfactory noise immunity of the data signals to be communicated over connecting cables, the RS-232-C Standard provides that the data signals transmitted over the cables have magnitudes of at least ±6 volts (See Sec. 2.3 of the Standard). Since most data handling equipment today operate at five-volt levels, the Standard makes necessary additional power supplies for enabling a voltage level conversion of the data signals to be interchanged over the connecting cable.

With regard to mechanical characteristics of the interface, the RS-232-C Standard states that the interface is "located at a pluggable connector signal interface point between the two equipments. The female connector . . . should be mounted in a fixed position near the data terminal equipment". (Sec. 3.1). FIG. 3.1 within the RS-232-C Standard assigns certain circuit functions to each of 25 connector pins associated with the pluggable connector at the signal interface point. While the Standard does not specify a particular type of multiple pin connector (See Appendix I to the Standard), the "D-type" 25 pin connector (for example, AMP type 206584–1) has essentially become an industry standard.

A printed circuit board together with circuit components and software necessary to achieve an RS-232-C interface between a computer terminal on one side, and modems or serial line printers on the other side, is available from a variety of manufacturers. Such boards are mountable inside the computer, and separate cable is provided. These boards are compatible from the RS-232-C side but they differ on the computer side from computer to computer.

The known RS-232-C interfaces which include a printed circuit board are arranged physically as shown in FIG. 1. The board B can be a "stand alone card" and be connected via a card cage connector (not shown) to various parallel signal bus lines associated with a microprocessor in a computer or other terminal equipment (also not shown). Alternatively, it can be a part of a more complex board. The RS-232-C Standard 25-pin connector CON may be mounted along one edge of the board B as shown, and the pins directly connected electrically to printed conductors on the board by soldering as at points S on the underside of the board B. This leaves a female connector part F fixedly mounted near the data terminal equipment as required by the Standard. The various conductors to which the pins of the connector CON are connected lead to electrical circuitry arranged over other portions of the board B, including, for example, a main logic element chip IC 1, line driver IC 3, line receiver IC 4, crystal oscillator OSC, frequency divider IC 2, and a number of discrete components C.

It will be appreciated that the known RS-232-C interface board arrangements require that a certain amount of space be allocated in existing equipment for their insertion, such space often being at a premium in units intended to be portable and of small overall dimensions. As far as is known, there has been no attempt to integrate any electrical interface circuitry, including those components required to implement the RS-232-C interface as shown in FIG. 1, within the prescribed interface connector itself such as the 25-pin connector CON.

A connector is known from U.S. Pat. No. 3,790,858 to Brancaleone et al within which RF filter elements are connected to a number of parallel pin-like contact elements which are supported inside and extend axially through a cylindrical shell. The filter elements are connected internally between the contact elements and a common cylindrical metal ground plate.

SUMMARY OF THE INVENTION

A primary object of the present invention is to provide a connector which exhibits simultaneously both the electrical characteristics and the connector requirements of a specified interface between two different data handling systems or equipments.

Another object of the invention is to provide a method wherein electrical circuitry for carrying out a specified function between two different data handling systems is integrated within a connector housing so as to reduce significantly spatial requirements within equipment associated with the systems.

It is a still further object of the present invention to provide a connector which provides a conversion interface between two data handling systems with a single input from a first data handling system and either identical and simultaneous multiple outputs to the second data handling system or different multiple outputs with selection between the multiple output interfaces.

Another object of the present invention is to provide said connector with multiple conversions between the two data handling systems.

These and other objects, features and advantages of the present invention will become more evident from the following discussion and the drawings.

According to one aspect of the invention, a connector includes a housing having a first set and a second set of terminals extending at least partly through wall parts of the housing to engage corresponding terminals of first and second outside connection means associated with first and second data handling systems, respectively. With an output signal the output set of terminals may be physically separated into multiple interfaces for simultaneous connection to multiple output devices with each device receiving an identical output. Alternatively, multiple conversions between the first and second data handling system is possible with selective switching for the desired interfacing between the first and second set of terminals. Logic interface circuit means is arranged within the connector housing and coupled between the first and second set of terminals. The circuit means operates to convert data signals transmitted to the first set of terminals from the first data handling system in a first type of format into corresponding data signals in a second type of format, and to provide the corresponding data signals in the second type of format to the second set of terminals for transmission to the second data handling system. The circuit means also operates to convert data signals transmitted to the second set of terminals from the second data handling system in a second type of format into corresponding data signals in a first type of format, and to provide the corresponding data signals in the first type of format to the first set of terminals for transmission to the first data handling system. For some applications the conversion of the data signals, as described, is in one direction to an output device.

According to another aspect of the invention, a method of implementing a logical interface to enable communications between a first data handling system in which data signals are arranged in a first type of format, and a second data handling system in which data signals are arranged in a second type of format, includes the steps of providing a connector housing; supporting first and second sets of electrical contact elements on the housing; containing electrical circuitry within the connector housing and connecting the circuitry with the first and the second sets of contact elements by arranging conductors inside the housing; converting by way of the electrical circuitry data signals transmitted to the first set of electrical contact elements in a first type of format from a first data handling system outside the connector housing into corresponding data signals in a second type of format and providing same to the second set of electrical contact elements through the conductors inside the connector housing; and converting by way of the electrical circuitry data signals transmitted to the second set of electrical contact elements in the second type of format from a second data handling system outside the connector housing into corresponding data signals in the first type of format and providing same to the first set of electrical contact elements through the conductors inside the connector housing. With an output only type of application the conversion between formats is in one direction to an output device and can embody a multiple output set of electrical contact elements for simultaneous identical output. Alternatively, either or both of multiple first and second set of electrical contact elements can be selectively switched as required. In this context, the term "multiple" refers also to contact elements which are electronically converted to different interface elements.

The invention will be more clearly understood upon reading the following detailed description of preferred embodiments thereof in conjunction with the accompanying drawing.

BRIEF DESCRIPTION OF THE DRAWING

In the drawing:

FIG. 1 is a perspective view of a conventional serial interface arranged on a portion of a printed circuit board;

FIG. 2 is a perspective view, with parts broken away, showing a first embodiment of a connector according to the present invention mounted on a printed circuit board;

FIG. 3 is a schematic diagram representing electrical circuitry contained in the housing of the connector in FIG. 2;

FIG. 4 is a perspective view of a second embodiment of a connector according to the present invention;

FIG. 5 is a perspective view of a third embodiment of a connector according to the present invention;

FIG. 6A is a top plan view of a printed circuit layout, and the phantom outline of the components, of the electrical circuitry seen in the schematic diagram of FIG. 3; and

FIG. 6B is a bottom plan view of the printed circuit board illustrating the interconnection among the various components.

FIGS. 7A and 7B are perspective views of alternative multiple RS-232C type connectors in accordance with the present invention.

FIGS. 8A and 8B are perspective views of alternative multiple serial communication connectors using RJ-11 type modular jacks.

FIG. 9 is an electrical block diagram schematically showing the logic interface for the connectors of FIGS. 7A, 7B, 8A and 8B.

FIG. 10A is a perspective view of a connector in accordance with the present invention which provides a multiple daisy-chained floppy drive controller interface.

FIG. 10B is an electrical block diagram schematically depicting operation of the connector of FIG. 10A.

FIG. 11 is an electrical block diagram schematically depicting a multiple channel analog to digital converter within a connector of the present invention.

FIG. 12 is an electrical block diagram schematically depicting a multiple channel digital to analog converter within a connector of the present invention with an RGB output.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 2 shows a first embodiment of a connector 10 according to the invention, the connector 10 being mounted on a printed circuit board 12 associated with a data handling system or equipment (not shown) in which data is interchanged in a parallel format. The connector 10 includes a connector housing 14, portions of which are omitted in FIG. 2 for the purpose of illustrating electrical circuitry 16 mounted in the interior space of the housing 14. It is preferable that walls of the housing 14 substantially enclose the interior space so as to protect the circuitry 16 contained therein.

As shown in FIG. 2, the housing 14 is in the form of a generally rectangular hollow block and includes a front wall 18, a part of which projects outwardly to define a first outside connection surface 20 parallel to the inside surface of wall 18. Housing 14 also includes a bottom wall 22 the outside surface of which defines a second outside connection surface 24. The outside dimensions of the housing 14, particularly those of the front wall 18 together with the first outside connection surface 20, preferably conform to those of a standard socket connector, thereby being adapted to mate with a standard plug connector or corresponding or complementary configuration. For applications in the RS-232-C interface, the housing 14 should conform to the dimensions of the known 25-pin "D type" subminiature connector mentioned earlier. Typical dimensions for the housing 14 thus may be a height H of about 0.5 inches (12.70 mm.), a depth D of about 1.2 inches (30.48 mm.) and a width W of about 2.0 inches (50.80 mm.).

The electrical circuitry 16 includes, in the embodiment of FIG. 2, a carrier in the form of a single printed circuit board or substrate 26 mounted closely adjacent and parallel to the inside surface of the bottom wall 22. Various integrated circuits and discrete components are mounted on the board 26, and are electrically connected by soldering, or by other technology, to conductors on one or both sides of the board 26.

The various "chips" and components shown in FIG. 2 as contained within the connector housing 14 on the board 26, and represented schematically in FIG. 3, include integrated circuits U1–U6; four tantalum chip capacitors C1–C4; a set of five chip capacitors C5–C9; a quartz crystal Q1; a toroid core transformer TR1 having bifilar wound primary and secondary windings T1–T2 and T4–T6; and a Graetz diode bridge G1. Each of eight conductors L extends from a different one of eight connection points on the printed circuit board 26 (FIG. 2), to corresponding female electrical contact elements or terminals J2–J8 and J20 which extend partly through and are supported in openings in the wall 18. The outside ends of the female contact elements are exposed at the first outside connection surface 20 to engage corresponding pins of an outside plug connector (not shown). The numbers assigned to the female contact elements J2–J8 and J20 correspond to the pin number-circuit function assignments prescribed in the RS-232-C Standard, mentioned earlier. Further, 24 male electrical contact elements or pins P1–P24 extend in two parallel rows of 12 pins each, downwardly from connection points near the long edges of the board 26 (FIG. 2), to engage openings in printed conductors or a conventional dual in line socket on the outside printed circuit board 12, at the second outside connection surface 24.

In accordance with a preferred technique of manufacture, the housing 14, except for the bottom wall 22, is molded in one piece; the elements or terminals J2–J8 and J20, as well as the conductors L, being included in the molding operation. Then, the bottom wall 22 and abutting printed circuit board 26 are snapped into position in the housing. By means of localized heating, the bottom wall is fused to the housing so that a completely unitary structure is achieved.

FIG. 3 shows the interconnections between the chips and other electrical components on the printed circuit board 26 contained within the connector housing 14, together with the female and the male contact elements arranged on the first and the second outside connection surfaces 20, 24 of the connector 10, respectively. The circuitry of FIG. 3 is one example of circuitry which functions to provide the electrical characteristics of an RS-232-C interface, but it will be appreciated that different circuitry may be integrated within the connector housing 14 to carry out the same function or other commonly used interfaces including 8-bit Parallel, GPIB (general purpose interface bus- IEEE 488), and Ethernet.

The integrated circuit U1 may be, for example, National Semiconductor type INS 8250A. The circuit U1 serves as a main logic element which handles all data signal interchanges between, e.g., a microprocessor (not shown) which handles data in a parallel bit format and communications equipment (not shown) which sends and receives serial bit data. Circuit U1 contains several programmable registers which determine the communications format and all the necessary information data to perform successfully a two-way data interchange between two data systems of different data formats. Specifically, before sending or receiving any data via an RS-232-C line, a controlling microprocessor (not shown) must load the internal registers with the required commands. The system software contains the following load functions which, when programmed within circuit U1, enable the latter to be used for data communications. The preprogrammed functions are:

1. Baud rate and baud rate factor;
2. Character length;

3. Number of stop bits;
4. Parity enable/disable and parity polarity;
5. Modem control functions; and
6. Additional operational conditions.

Instructions representing the above load functions are transmitted to the circuit U1 from an outside microprocessor (not shown) over data bus lines DO–D7 corresponding to the male contact elements or pins P1–P8 on the second outside connection surface 24 of the connector housing 14 (FIG. 2). The appropriate registers within circuit U1 are selected by the address bus lines A, A1 and A2 (pins P23, P22 and P21), and a write signal ($\overline{WR}$, pin P19) validates the register loadings.

When data characters are transmitted by the outside microprocessor after the foregoing initialization procedure, the circuit U1 performs a parallel-to-serial data conversion. First, the eight-bit parallel data is placed into a transmitter register within circuit U1 which then automatically adds a start bit, followed by the data character bits themselves (least significant first) and the programmed number of stop bits for each character. Also, an even or odd parity bit is inserted prior to the stop bit(s) as defined previously by the system program. The character is then transmitted as a serial data stream on a data output line S_{out} at terminal 11 of the circuit U1. The rate at which the data is shifted out is determined by another previously programmed register within circuit U1. The quartz crystal Q1 coupled to the circuit U1 operates together with a programmable divider within circuit U1 to generate a signal of the appropriate frequency for shifting out the data bits.

The strength or voltage levels of the data bits or signals shifted out from the circuit U1, typically TTL compatible (zero to +5 volts). As mentioned earlier, the RS-232-C Standard requires a stronger signal level so that data can be transmitted over a long cable with the capacity of noise suppression. Accordingly, a line driver circuit U3, e.g., Motorola type MC 1488, is coupled to data output S_{out} and supplementary handshake signals as $\overline{RTS}$ (Request to Send) and $\overline{DTR}$ (Data Terminal Ready) of the circuit U1. When powered by an appropriate power supply, the line driver circuit U3 converts the TTL compatible level (zero to +5 volt) of the serial output from the circuit U1, to a ±12 volt level sufficient to satisfy the RS-232-C Standard. The integral power supply is constructed of a push-pull mode switching scheme, performed by high frequency oscillator derived from U4 (e.g. 4516 B RCA), 74C86 exclusive OR gates (U6 e.g. Nat. Semiconductor), high current power transistors within U5 (75951 e.g. Texas Instruments) Tr1 transformer, G1 diode bridge and C2,C3 tantalum capacitors.

When a serial data bit stream is transmitted to the connector 10 from an outside data handling system, specifically to the female contact elements J3 at the first outside connection surface 20 of the housing 14, the higher voltage level of the bit streams is converted to a TTL compatible (0 to 5 volt) logic level by way of buffer-inverters within circuit U2 (e.g., Motorola type MC 1489 A). Also, high level complementary signals (J5, J6 and J8 are converted down). The serial data is then shifted into a receiver register within the main logic element circuit U1 where the data is converted into a parallel format; however, the start and stop bits and the parity bit are subtracted. Thus, the data is then ready to be sent to the microprocessor or other outside parallel format data system over the data bus lines DO–D7.

The circuit U1 is selected for operation by the microprocessor or other outside parallel data system connected to the pins P2–P24 of the connector 10 by way of a chip select signal ($\overline{CS}$, pin P18). The receiver register within the circuit U1 is selected by a preset combination of the address bus lines (AO, A1, A2; pins P23, P22, P21), and the parallel data is placed on the data bus lines (DO–D7; pins P1–P8) for transmission to the outside microprocessor. A read signal ($\overline{RD}$, pin P20) activates the data reading from the circuit U1 to the microprocessor. Likewise, status information reading procedure can be performed similarly.

There are several control signals, and control and status registers in circuit U1 that determine the bidirectional serial communication procedure. All the necessary signals, including "handshaking", status and command bits, and modem control are included in communications following the preprogrammed functions from the outside microprocessor software.

Those components on the board 16 (FIG.2) which have not been discussed above in detail but appear in the circuitry of FIG. 3 will be recognized and understood by those skilled in the art. A preferred quartz crystal Q1 is Seiko type DS-MGQ, 1.8432 MHz, series resonant. The chip capacitors C1–C4 may be Arco type ACT, tantalum, and the chip capacitors C5–C9 may be Murata type GR40 Y5V. Chip resistors R1–R3 can be Panasonic type ERJ-86CSJ, or alternatively can be thick film resistors deposited on the board 16.

The toroid transformer TR1 preferably is made from a Ferroxcube core type 266CT125, material 4C4. The primary winding is 2×10 turns and the secondary is 2×25 turns, both bifilar.

FIG. 4 shows a second embodiment of a connector 10' according to the invention. The outside dimensions and overall appearance of the connector 10' are generally similar to those of the connector 10 of FIG. 2. Two printed circuit boards or substrates 26'A and 26'B are, however, provided in housing 14' instead of the single board 26 in FIG. 2. Board 26' A extends at the top of the housing 14' parallel to the board 26'B which extends across the bottom of housing 14'. Board 26' B carries 24 pins P1'–P24' on its bottom outside surface 24' for connection directly to an outside circuit board or into a dual-in-line socket. The board 26' A is coupled by leads L' to female contact elements J2'–J8' and J20' which engage an outside plug connector at connection surface 20' of the connector 10'

FIG. 5 shows a third embodiment of a connector 10'' according to the invention. A single, flexible printed circuit board 26'' is contained within the connector housing 14''. Conductors at one end of the board 26'' are directly to the inside ends of female contact elements J2''–J8'' and J20'' which are arranged to engage an outside plug connector at contact surface 20''. Conductors at an opposite end of the flexible board 26'' are connected directly to the inside ends of insulation displacement type pins P1''–P24''. A cap CP is constructed and arranged to clamp a flat insulated cable (not shown) over pointed ends of pins P1''–P24'' so that the pins pierce through the cable insulation to electrically contact corresponding conductors of the flat cable.

It will be appreciated that the connector of the present invention provides a completely self-contained interface unit which eliminates all the inconveniences of designing and realizing a data interface such as the RS-232-C Standard. Particular components no longer need be selected to meet the requirements of the Stan-

dard, voltage level conversions are provided for, and time consuming test procedures and debugging are eliminated. The present connector thus saves engineering effort, development and production time as well as labor costs. Importantly, a considerable space savings is achieved in terminal equipment which would otherwise require means to accommodate a separate interface board.

In order to enable the man skilled in the art to practice this invention in some detail, a complete printed circuit layout is shown in FIG. **6**. This layout conforms with the circuitry previously illustrated in schematic form in FIG. **3**. The contact areas **J2–J8** and **J20**, which correspond with the respective female contact elements so designated, will be seen in FIG. **6A**. Likewise, contact areas **P1–P12** (at the near longitudinal edge) and **P13–P24** (at the far edge), which correspond with the respective male contact elements bearing the same designation. Capacitors **C1–C9**, oscillator **Q1**, and transformer **TR1**, are seen in phantom outline while resistors **R1**, **R2** and **R3** are represented by means of hatch lines. All the other principal elements are shown by means of rectangles suitably labeled. Appropriate wire bonding from the several integrated circuits **U1–U6**, as well as from the Graetz bridge **G1**, is shown in FIG. **6A** connected to the conductors **30A** on the printed circuit board.

It will be noted by the skilled worker that suitably correlated conductors **30B** are provided on the lower surface of the printed circuit board **26** (FIG. **6B**) so as to make the requisite interconnections among components. The dots **32** sent so-called "vias" between the upper and lower surfaces of board **26**.

It will be appreciated that, for the sake of clarity, the depiction of a printed circuit layout for a circuit board **26** to be housed in connector **10** of FIG. **2** is greatly enlarged (approximately 7 times).

In FIGS. 7A and 7B, dual RS-232-C connectors **41** and **42** are shown with each having the data conversion cicuitry contained within the respective housings **43** and **44**. In FIG. 7A the connector **41** embodies two standard **25** pin "D" connectors **41***a* and **41***b* in stacked configuration with pins **45** extending for connection to a microprocessor. In a different spatial configuration FIG. 7B depicts connector **42** having a side by side configuration of **9** pin "D" connectors **42***a* and **42***b* and pins **46** for connection to a microprocessor.

The connector embodiment **52** in FIG. **8A** is similar to the side by side configuration of connector elements shown in FIG. 7B but with modular RJ-11 type jacks **52***a* and **52***b* in place of the "D" connectors. Connector **51** shown in FIG. **8B** is a further modification of the connector shown in FIG. **8A** wherein four jacks **55***a–d* are provided for a connection interface.

As schematically shown in FIG. **9**, external connector elements ECl-n, corresponding to the "D" connectors or RJ-11 jacks, are individually connected to a multiple channel LSI logic element **60** through corresponding line driver/receivers 1′—n′. Logic element **60** is in turn connected to bus interface **61** for interfacing with the microprocessor. In order to minimize size requirements whereby the conversion circuitry may be readily contained within the connector housing there is sharing of components. To wit, there is a single multichannel LSI logic element **60**, bus interface **61**, oscillator **62**, and power conversion unit **63**. The size and output of the power conversion unit is determined by the number of output devices since it must be sufficient to drive "n" number of line driver/receivers. Generally, this requires a maximum power output of about 2 watts for every 4 channels. With the state of current technology, multi-channel LSI logic elements have up to 8 channels and accordingly "n" presently ranges up to 8. However it is understood that the present invention is similarly applicable to connectors having LSI elements with multi-channels in excess thereof.

In the connector embodiments of FIGS. 7A, 7B, 8A, 8B and **9**, there is a virtual simultaneous operation of multiple channels and accordingly the connector can provide a simultaneous communications linkage between, for example, one processing computer and multiple data destinations.

The connector of the present invention provides a data conversion interface for applications other than communication such as depicted in **10A**, **10B**, **11** and **12**. These latter embodiments exemplify usage of connectors having various contained conversion elements therewithin.

In FIG. **10A** connector **70** provides a floppy drive controller interface. Housing **71** contains floppy interface elements **72** and bus interface pins **73**. As schematically shown in FIG. **10B** four floppy disk drives are daisy chained and connected to the floppy drive controller **70**. Dedicated pins SEL **74–77** select one out of the four drives to be active at a time in the multiplexed series. The connector contains the bus interface **78**, floppy controller LSI **79**, data separator element **80**, phase locked loop **81** and quartz oscillator **82**. Again the number of floppy drives capable of being controlled by a single connector element is determined by the current state of the art with regard to the capability of the floppy controller LSI and the number of channels it embodies for driving multiple drives.

FIG. **11** schematically shows the internal circuitry for a multiple channel analog to digital converter for use with, for example different signal conditioning elements, for containment within the connector of the present invention. In FIG. **11** various analog signals from signal conditioning elements SC **1**—n are individually connected to analog channel selector **91** and power supply **92**. Examples of analog signals include temperature, voltage, amperage etc. Microprocessor bus interface **93** is interfaced with both the analog to digital converter **90** and analog channel selector **91** with the latter connection providing requisite direct channel selection as required. Analog conditioned signals pass from the analog channel selector **91** to the analog to digital converter **90** for conversion and transmission to the microprocessor. Oscillator **94** provides the timing for the converter **90** and power supply **92** provides power for the analog channel selector **91**. With the multiplexed arrangement, as shown, only one channel at a time is selected for analog to digital conversion.

As shown in FIG. **12** a multiple channel digital to analog converter within a connector of the present invention provides a multiple simultaneous conversion for an analog output to an RGB monitor. FIG. **12** schematically depicts a multiple channel digital to analog convertor for use with, for example an RGB monitor, for containment within the connector of the present invention. Microprocessor bus interface **103** interfaces, with look up tables **104** and digital to analog converters **105–107** for providing an R G B output respectively at the connector output interface for an attached RGB monitor. Sychronizing generator **101**, clock **109**, and power supply **102** provide the required timing and

power for the multiple simultaneously processed digital to analog signals.

While specific embodiments of the invention have been shown and described in detail to illustrate the application of the inventive principles, it will be understood that the invention may be embodied otherwise without departing from such principles.

I claim:

1. A connector for implementing a direct predetermined logical interface between a first data handling system wherein data signals are arranged in a first type of format, and a second data handling system wherein data signals are arranged in a second type of format, comprising:

a connector housing including a first wall part forming a first outside connection surface and a second wall part forming a second outside connection surface;

a first set of terminals arranged to extend at least partly through said first wall part from inside said connector housing in a given configuration for engaging in contact with corresponding terminals of first outside connection means associated with the first data handling system, with said first set of terminals forming an interface member for matingly engaging a corresponding interface member formed by said corresponding terminals associated with the first data handling system;

a second set of terminals arranged to extend at least partly through said second wall part from inside said connector housing in a given configuration for engaging in contact with multiple corresponding terminals of second outside connection means associated with the second data handling system, with said second set of terminals forming multiple interface members for matingly engaging corresponding interface members formed by said corresponding terminals associated with the second data handling system; and

interface circuit means arranged within said connector housing and coupled between said first set of terminals and said second set of terminals for converting data signals transmitted to at least some of said first set of terminals from the first data handling system in the first type of format into corresponding data signals in the second type of format and providing said corresponding data signals in the second type of format to at least some of said second set of terminals for subsequent transmission to the second data handling system.

2. A connector according to claim 1 wherein data signals transmitted to at least some of said second set of terminals from the second data handling system in the second type of format are converted by conversion means, within said connector, into corresponding data signals in the first type of format and said corresponding data signals in the first type of format are provided to at least some of said first set of terminals for subsequent transmission to the first data handling system.

3. A connector according to claim 2, wherein said interface circuit means comprises means for converting data signals transmitted to at least some of said first set of terminals in a serial format into corresponding data signals in a parallel format and providing the corresponding parallel data signals to at least some of said second set of terminals for multiple simultaneous output, and for converting data signals transmitted to at least some of said second set of terminals in a parallel format into corresponding data signals in a serial format and providing the corresponding serial data signals to at least some of said first set of terminals.

4. A connector according to claim 1, wherein said interface circuit means comprises means for selectively converting multiple analog data signals into corresponding data signals in a digital format.

5. A connector according to claim 1, wherein said interface circuit means comprises means for converting multiple digital data signals into corresponding analog data signals.

6. A connector according to claim 1, wherein said connector provides a multiple daisy chained floppy drive controller interface.

7. A connector according to claim 1 wherein said connector housing has structural dimensions of a height of no more than about 0.5 inches (12.70 mm), a depth of no more than about 1.2 inches (30.48 mm), and a width of no more than about 2.0 inches (50.80 mm).

8. A connector according to claim 1 wherein said connector housing comprises walls forming an enclosure member and wherein said interface circuit means are completely enclosed within the walls of said connector housing.

9. The connector of claim 1 wherein said first set of terminals comprises a number of male contact elements adapted for direct integrated electrical mating with a printed circuit board member which handles data in said first type of format and wherein said housing is adapted to be physically supported by said printed circuit board.

10. The connector of claim 1 wherein said first set of terminals comprises a number of male contact pins adapted for direct integrated electrical mating with an insulated ribbon cable connector member, with said pins being adapted to pierce the insulation of said cable to electrically contact conductors of said cable whereby said electrical mating is effected, said cable connector member being adapted to be electrically connected to a printed circuit board which handles data in a first format and wherein said connector comprises means to physically enclose a portion, of said ribbon cable connector

11. The connector of claim 1 wherein said interface circuit means further comprises a power supply, with said power supply being contained within said walls of said connector housing.

12. A multiple "D-type" RS-232-C connector having a male connection interface adapted for direct integrated electrical mating with a printed circuit board member which handles data in a parallel format, said connecter further having multiple female connection interfaces for mating connection with corresponding external male connection interface members from one or more external devices which handle data in a serial format, characterized in that means for converting data from said parallel format to said serial format and means for converting data from said serial format to said parallel format are electrically positioned between said male connection interface and said female connection interfaces within said connector, and wherein said connector is adapted to be physically supported by said printed circuit board.

13. A multiple "RJ-11" connector having a male connection interface adapted for direct integrated electrical mating with a printed circuit board member which handles data in a parallel format, said connecter further having multiple female connection interfaces for

mating connection with corresponding external male connection interface members from one or more external devices which handle data in a serial format, characterized in that means for converting data from said parallel format to said serial format and means for converting data from said serial format to said parallel format are electrically positioned between said male connection interface and said female connection interfaces within said connector, and wherein said connector is adapted to be physically supported by said printed circuit board.

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(54) **MULTIPLE CONNECTOR INTERFACE**

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(52) **U.S. Cl.** **341/100**; 361/394; 439/620

(58) **Field of Search** 341/100, 101; 439/389, 391, 393, 620, 621, 622

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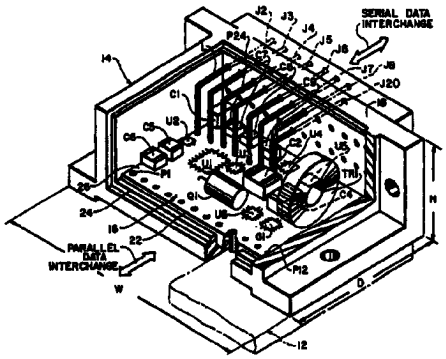
(57) **ABSTRACT**

A connector interface for enabling multiple conversions between first and second data handling systems wherein the data in the first system is arranged in a first type of format and the data in the second system is arranged in a second type of format, includes a connector housing with first and second sets of electrical contact elements exposed at different portions of the housing. Circuitry contained entirely within the housing operates to convert data transmitted to the first set of contact elements from the first data handling system into corresponding data in the second type of format for transmission to the second data handling system through the second set of contact elements, and to convert data transmitted to the second set of contact elements from the second data handling system into corresponding data in the first format for transmission to the first data handling system. One set of electrical contact elements may, for example, be arranged to extend out from the connector housing in two parallel rows to allow the elements to be directly connected to corresponding terminals arranged in a dual in line configuration on an outside printed circuit board. The other set of electrical contact elements may be arranged for multiple simultaneous or selective output connections for applications such as multiple communication, digital to analog and analog to digital conversions, and a multiple floppy disk controller.



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* cited by examiner

EX PARTE REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

NO AMENDMENTS HAVE BEEN MADE TO THE PATENT

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

The patentability of claims **1–13** is confirmed.

* * * * *

PRETEC ELECTRONICS CORPORATION
Attn: Tommy Ho, Operation Manager
46791 Fremont Blvd.
Fremont, CA 94538
Telephone: 510-440-0535

Attorneys for Defendant PRETEC ELECTRONICS CORPORATION, Pro Per

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACTICON TECHNOLOGIES, LLC

Plaintiff,

v.

PRETEC ELECTRONICS CORPORATION, a California corporation; and C-ONE TECHNOLOGY CORPORATION, a Taiwan corporation,

Defendants.

AND RELATED CROSS ACTIONS

Case No. C-06-4679 JF (HRL)

DEFENDANT PRETEC ELECTRONICS CORPORATION AND C-ONE TECHNOLOGY CORPORATION'S MOTION TO CHANGE TIME

PRETEC ELECTRONICS CORPORATION and C-ONE TECHNOLOGY CORPORATION move for an order extending the deadline for the INITIAL CASE MANAGEMENT CONFERENCE (CMC) on 11/29/2006. Pretec and C-One have other litigations pending in the United States. The attorneys of Pretec and C-One have just filed a motion to withdraw as counsel and that motion was granted by the court. The court further ordered Pretec and C-One to assign replacement counsel. Pretec and C-One have not yet obtained new counsel and are seeking new attorney aggressively. Accordingly, to avoid prejudice to Pretec and C-One and to allow Pretec and C-One sufficient opportunity to retain a counsel, Pretec and

EXHIBIT E

C-One respectfully request a 60 days extension of the current initial case management conference. If this request is denied, Pretec and C-One will lose the opportunity to obtain a proper counsel and will not be represented in this case.

For all of the aforementioned reasons, Pretec and C-One respectfully request a 60 days extension of the current initial case management conference deadline.

Respectfully submitted,

Dated: Oct 19, 2006

PRETEC ELECTRONICS CORPORATION

By: _____
Tommy Ho, Operation Manager of Pretec

C-ONE TECHNOLOGY CORP.

By: _____
Gordon Yu, President of C-One

PROOF OF SERVICE

ACTICON v. PRETEC,C-ONE et al.
United States District Court Northern District of California (San Jose Division) –
Case No.:C 06 4679 JF(HRL)

I declare that I am over the age of eighteen (18) and not a party to this action. My business address is 46791 Fremont Blvd., Fremont, CA 94538.

On October 19, 2006, I served the following document(s):

MOTION OF DEFENDANT C-ONE TECHNOLOGY CORPORATION AND PRETEC ELECTRONICS CORPORATION TO CHANGE TIME

on the interested parties in this action by placing a true and correct copy of document(s) in a sealed envelope addressed as follows:

ROBERT J. YORIO
COLBY B. SPRINGER
CHRISTINE S. WATSON
CARR & FERRELL LLP
2200 Geng Road
Palo Alto, CA 94303

( ) **[U.S. MAIL]** I am readily familiar with the business practice for collection and processing of correspondence for mailing with the United States Postal Service. I know that the correspondence is deposited with the United States Postal Service on the same day this declaration was executed in the ordinary course of business. I know that the envelope was sealed and, with postage thereon fully prepaid, placed for collection and mailing on this date, following ordinary business practices in the United States mailed in Fremont, California.

(x) **[OVERNIGHT DELIVERY]** Via Federal Express or similar overnight courier service, by depositing in a box or other facility regularly maintained by such overnight delivery service, or delivering such envelope to a courier or driver authorized by said overnight delivery service to receive documents, in an envelope designated by said overnight delivery service with delivery fees paid or provided for, addressed to the above-named persons on whom it is to be served.

( ) **[PERSONAL SERVICE]** I caused to be delivered by hand the above-referenced document(s) to the above-named person(s).

( ) **[FACSIMILE]** Via facsimile machine, I caused the above-referenced document(s) to be transmitted to the person(s) and facsimile number(s) shown above.

Executed on June ____, 2006, in Fremont, California.

( ) **(STATE)** I declare under penalty of perjury under the laws of the State of California that the above is true and correct.

(X) **(FEDERAL)** I declare that I was retained by the office of a member of the bar of this court at whose direction the service was made.

Tommy Ho

Tommy Ho

State of California
Secretary of State

I, DEBRA BOWEN, Secretary of State of the State of California, hereby certify:

That the attached transcript of 2 page(s) was prepared by and in this office from the record on file, of which it purports to be a copy, and that it is full, true and correct.

IN WITNESS WHEREOF, I execute this certificate and affix the Great Seal of the State of California this day of

APR 20 2007

Debra Bowen

DEBRA BOWEN
Secretary of State

EXHIBIT F

D0830959

FILED JK
In the office of the Secretary of State
of the State of California
NOV 2 8 2006

1828248

CERTIFICATE OF DISSOLUTION

CORPORATION NUMBER: D-1828248

CHIU FENG CHEN CERTIFIES THAT:

1. SHE IS THE DIRECTOR NOW IN OFFICE OF PRETEC ELECTRONICS CORP, A CALIFORNIA CORPORATION.

2. THE CORPORATION HAS BEEN COMPLETELY WOUND UP.

3. THE CORPORATION'S KNOWN DEBTS AND LIABILITIES HAVE BEEN ACTUALLY PAID.

4. THE CORPORATION'S KNOWN ASSETS HAVE BEEN DISTRIBUTED TO THE PERSONS ENTITLED THERETO.

5. A FINAL FRANCHISE TAX RETURN, AS DESCRIBED BY SECTION 23332 OF THE REVENUE AND TAXATION CODE, HAS BEEN OR WILL BE FILED WITH THE FRANCHISE TAX BOARD AS REQUIRED UNDER PART 10.2 (COMMENCING WITH SECTION 18401) OF DIVISION 2 OF THE REVENUE AND TAXATION CODE.

6. THE ELECTION TO DISSOLVE WAS MADE BY THE VOTE OF ALL THE OUTSTANDING SHARES.

7. THE CORPORATION IS DISSOLVED.

I FURTHER DECLARE UNDER PENALTY OF PERJURY UNDER THE LAWS OF THE STATE OF CALIFORNIA THAT THE MATTERS SET FORTH IN THIS CERTIFICATE ARE TRUE AND CORRECT OF MY OWN KNOWLEDGE.

DATE: 11/22/06

CHIU FENG CHEN, DIRECTOR

OFFICE OF THE SECRETARY OF STATE

PRETEC

News Release

Pretec Announces the World's Fastest and most Rugged Industrial CompactFlash™ Card

San Jose, California, April 3rd, 2007 –– **Pretec**, the pioneer of the highest capacity flash memory cards of CF card (64GB) and USB Flash Drive, will demonstrate the worlds world's fastest and most rugged industrial CompactFlash Card (266X) today at ESC booth 1348.

With transfer rates of up to 40MB/sec (UDMA mode 5) and rugged metal construction, Pretec ruggedized Industrial CompactFlash™ card provides the highest performance and most reliable industrial grade storage solution in CompactFlash™ form factor. In addition to high performance, Pretec Ruggedized Industrial CompactFlash™ card also offers ultra low power consumption allowing for extended battery life in mobile or remote applications without an external power source.

Fully compliant with CompactFlash™ Specification, Pretec Ruggedized Industrial CompactFlash™ utilizes a rugged metal housing which is a standard feature allowing for greater resistance to shock and vibration and is also available in extended and high operating temperature rated versions allowing for operation in harsh environmental conditions from −20°C to 85°C and −40°C to 85°C.

In addition to high performance and ruggedized features, Pretec Ruggedized Industrial CompactFlash™ card is also available with the implementation of ATAPI-5 Security features allowing for device specific or operator specific security parameters to secure data from unauthorized use and or with mainbord BIOS integration, prevent the installation of an un secured CompactFlash™ Card making it the ideal storage solution for data sensitive applications.

EXHIBIT G

PRETEC News Release

About Pretec

Pretec™ (http://www.pretec.com) offers a complete spectrum of small form factor memory cards and card readers such as CF, SD MMC, and USB Flash Drive for digital imaging, mobile communication, and industrial flash markets. Pretec has consistently demonstrated the highest capacity cards first available in the world: such as CF card 80MB, 128MB, 160MB, 320MB, 640MB, 1.5GB, 3GB, 6GB, 12GB and 16GB CF card; the first 1GB and 4GB MMC card; the largest size 8GB and 16GB USB Flash Drive; and the highest capacity SD cards in 4GB and 8GB (SDHC). With more than 100 patents granted or filed, Pretec has also been offering the highest speed cards in the world such as CF 80X (2004), MMC 4.0 150X (2004), USB 166X/266X (2005), SD 133X (2005), MMC*plus*™ 266X (2005); and smallest size USB Flash drive in the world such as i-Disk Tiny ("Best Gear of 2003" by *TIME Magazine*), i-Disk Diamond (also known as Cu-Flash) (2005).

*For more information, please visit www.pretec.com

*Note: i-Disk, i-Disk Tiny, or i-Disk Diamond are trademarks of Pretec Electronics Corporation. All other trademarks mentioned herein are recognized as the property of their respective holders.

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