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JEFFREY E. OSTROW (213118)
SIMPSON THACHER & BARTLETT LLP
2550 Hanover Street
Palo Alto, California 94304
Phone: (650) 251-5000
Facsimile: (650) 251-5002
Email: jostrow@stblaw.com

Attorneys for Plaintiff
CSR plc

UNITED STATES DISTRICT COURT

CENTRAL DISTRICT OF CALIFORNIA

SOUTHERN DIVISION

CSR plc,

Plaintiff,

v.

BROADCOM CORPORATION,

Defendant

Case No. **SACV10-01281 AG (FFMx)**

COMPLAINT FOR PATENT INFRINGEMENT

DEMAND FOR JURY TRIAL

Plaintiff CSR plc ("CSR") by its attorneys, alleges as follows:

NATURE OF THE CASE

1. CSR is one of the world's leading providers of connectivity and location-enabled semiconductor products. Since 1995, SiRF Technology, Inc. ("SiRF"), now a subsidiary of CSR, has been a pioneer in the field of designing and developing semiconductors to provide Global Positioning System ("GPS") technology solutions. The innovative nature of this technology has been recognized by the United States Patent Office, which has issued more than 200 patents to SiRF alone.

2. Defendant Broadcom Corporation ("Broadcom") is one of the largest "fabless" or non-manufacturing semiconductor companies in the world, with more than $4.4 billion in annual revenues. Its sales of semiconductor products providing GPS capability, which compete

directly with those sold by the much smaller CSR, have grown substantially and steadily since it entered the field of GPS semiconductors by acquiring a competitor of SiRF's in 2007. As a result of the infringing products, Broadcom has been able to achieve double-digit sequential revenue growth within its mobile and wireless business, as stated in Defendant's Q2 Earnings Call of July 27, 2010. Broadcom has publicly stated that it expects this growth to continue; its President and CEO told investors that Broadcom's "GPS business will be one of our largest percentage growth drivers in 2010." He attributed this growth to "definite strength in our GPS business in terms of just performance of the technology." Increasingly, Broadcom has sold its GPS products and solutions together with its baseband processor products designed for use in cellular phones and other wireless handset devices.

3. Broadcom's growth has, however, been achieved unlawfully. By this complaint, CSR charges Broadcom with comprehensive and systematic infringement of CSR's valuable intellectual property rights in the field of GPS and related wireless communications technology, including infringement of the nine United States patents identified below. Upon information and belief, a reasonable opportunity for discovery will show that more than 50 Broadcom wireless semiconductor products infringe one or more of the CSR patents identified below.

4. In addition to substantial damages for Broadcom's past and willful infringement, CSR seeks an injunction to restrain Broadcom from further sales of its infringing products, including the BCM4750, BCM4751, BCM 4760, BCM2075, BCM29751, and Hammerhead II GPS products, the BCM4325 and BCM4329 wireless connectivity products, the BCM 21331, BCM 2153, BCM 2091 and BCM 21553 baseband processors, Broadcom's Long Term Orbits ("LTO") with Assisted GPS ("AGPS") technology, and Broadcom's CellAirity Mobile Platform, and to restore fair competition in the market for semiconductor products providing GPS and wireless capability.

JURISDICTION AND VENUE

5. This is an action for patent infringement arising under the patent laws of the United States, Title 35, United States Code.

6. This Court has subject matter jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and 1338(a).

7. This Court has personal jurisdiction over Broadcom because Broadcom has constitutionally sufficient contacts with California to make personal jurisdiction proper in this Court. In particular, Broadcom has purposefully directed activities to this judicial district, including utilizing a distributor in this judicial district to offer to sell and to sell products which infringe the patents asserted in this Complaint. Moreover, on information and belief, Broadcom solicits business within this district and elsewhere in California, and derives revenue from the sale of its products and/or services within this district and elsewhere in California, which gives this Court general jurisdiction over Broadcom.

8. Venue is proper in this district pursuant to 28 U.S.C. §§ 1391(b), 1391(c) and 1400(b) because a substantial part of the events giving rise to the claims occurred in this district and Defendant Broadcom maintains an office in the Southern Division of this district.

THE PARTIES

9. Plaintiff CSR is a corporation registered in the United Kingdom with its principal place of business at Churchill House, Cambridge Business Park, Cowley Road, Cambridge, CB4 0WZ United Kingdom, and with its U.S. headquarters in California.

10. Defendant Broadcom is a corporation organized and existing under the laws of California, with its principal place of business at 5300 California Avenue, Irvine, California 92617.

BACKGROUND

11. Plaintiff CSR is a leading provider of multifunction connectivity and location-enabled silicon platforms. CSR devotes a substantial portion of its resources to developing new products and strengthening its technological expertise in the location market. As of January 2010, CSR had approximately 582 patents granted worldwide – approximately 250 patents granted in the United States and 332 patents granted in other territories. As of July 2010, SiRF had approximately 397 patents granted worldwide – approximately 246 patents granted in the United States and 151 granted in other territories.

12. Founded in 1995, SiRF began selling semiconductors providing GPS capability in 1996. SiRF merged with a subsidiary of CSR on June 26, 2009. While SiRF was still an independent company, it also invested hundreds of millions of dollars in research and development, spending more than $340 million between 2004 and 2007 alone. These efforts resulted in the introduction of numerous commercially successful products, including the breakthrough SiRFStarIII and SiRFStarIV product lines, and led to the issuance of more than 200 United States patents between 1996 and 2008. The combination of SiRF's pioneering innovations in the GPS and assisted GPS ("AGPS") field with CSR's broad technology portfolio, which includes Bluetooth, GPS, FM, Wi-Fi (IEEE802.11), UWB, NFC and other technologies, enables CSR to provide customers with solutions that incorporate GPS capabilities with fully integrated radio, baseband and microcontroller elements.

13. CSR's technology has been adopted by market leaders into a wide range of mobile consumer devices such as mobile phones, automobile navigation and telematics systems, portable navigation devices ("PNDs"), wireless headsets, mobile computers, mobile internet devices, GPS recreational devices, digital cameras, and mobile gaming, as well as a wide range of personal and commercial tracking applications.

14. Defendant Broadcom sells numerous semiconductor products providing GPS, AGPS, mobile, and wireless capabilities that compete with CSR's products. For example, Broadcom's BCM4750, BCM4751, BCM4760, BCM2075, BCM20751, Hammerhead II, BCM4325 and BCM4329 semiconductor products are key components of the GPS, AGPS, mobile and wireless connectivity business driving Broadcom's growth.

15. The BCM4750, and its successor, the BCM4751, are single-chip GPS receivers that interface with mobile phones, personal data assistants ("PDAs"), PNDs, and MP3 players. For some time, the BCM4750 has been and remains Broadcom's main offering in the market for discrete GPS semiconductor products. As alleged below, the BCM4750 and BCM4751 infringe CSR's patents.

16. The BCM2075 and BCM20751 are Bluetooth FM and GPS combo devices for use in mobile handsets, media players, and PNDs that require GPS receiver functionality.

Broadcom recently introduced these products to the market with considerable fanfare. However, as alleged below, the BCM2075 and BCM20751 infringe CSR's patents.

17. The BCM4760 is a System-on-Chip device combining a GPS receiver and application processor designed for personal navigation devices and other low-power electronics products. As alleged below, the BCM4760 infringes CSR's patents.

18. The Hammerhead II is a single-chip GPS receiver that interfaces with mobile phones, PDAs, PNDs, and MP3 players. Prior to the BCM4750, the Hammerhead II was Broadcom's main offering in the market for discrete GPS semiconductor products. As alleged below, the Hammerhead II infringes CSR's patents.

19. The BCM4325 and its successor, the BCM4329, are single-chip devices that include auto-calibration technology for use in mobile or handheld wireless products. On April 27, 2010, in connection with Broadcom's announcement of its earnings for the first quarter of 2010, Broadcom's Chief Financial Officer told investors that "the 4325 chip, which is our Bluetooth FM wireless LAN chip[,] was our number one seller, highest volume shipped in Q1, and it's [sic] successor the 4329 will be our highest volume chip probably in this quarter." In Broadcom's Q2 Earnings Call of July 27, 2010, Broadcom's CEO stated that this "Bluetooth GPS combo" is "very attractive right now." As alleged below, the BCM4325 and its successor, the BCM4329, also infringe CSR's patents.

20. The BCM 21331, BCM 2153, BCM 2091 and BCM 21553 are baseband processors that include GPS frequency aiding technology for use in mobile or handheld wireless devices. Broadcom touts its baseband products as providing "best-in-class solutions for all of the critical components required for today's advanced mobile devices, including feature-rich functionality, 2G and 3G cellular connectivity, multimedia acceleration and support for both Bluetooth® and Wi-Fi® protocols." As alleged below, the BCM 21331, BCM 2153, BCM2091 and BCM 21553 infringe CSR's patents.

21. Broadcom's LTO technology, according to Broadcom, "brings GPS assistance data to mobile device users who do not have the benefit of Assisted-GPS (AGPS) infrastructure in their wireless networks." Since 2005, the LTO product has been incorporated in mobile

devices. Broadcom's AGPS technology, according to Broadcom, "served approximately 10 million subscribers worldwide" in 2005 and was "the core of the first US nationwide AGPS enabled mobile network in 2002." As alleged below, Broadcom's AGPS technology infringes at least one of CSR's patents. As alleged below, Broadcom's LTO technology infringes at least one of CSR's patents.

22. Broadcom's CellAirity Mobile Platform is a mobile handset hardware and software platform that incorporates frequency-aiding technology. As alleged below, Broadcom's CellAirity Mobile Platform infringes CSR's patents.

PATENTS IN SUIT

23. On September 2, 1997, the United States Patent and Trademark Office (the "Patent Office") duly and legally issued United States Letters Patent No. 5,663,735 ("the '735 patent"), entitled "GPS Receiver Using A Radio Signal For Improving Time To First Fix." CSR is the assignee of all rights, title, and interest in and to the '735 patent and possesses all rights of recovery under the '735 Patent, including the right to recover damages for past infringement. A true and correct copy of the '735 patent is attached hereto as Exhibit A.

24. On November 12, 2002, the Patent Office duly and legally issued United States Letters Patent No. 6,480,150 ("the '150 patent"), entitled "Autonomous Hardwired Tracking Loop Coprocessor For GPS and WAAS Receiver." CSR is the assignee of all rights, title, and interest in and to the '150 patent and possesses all rights of recovery under the '150 Patent, including the right to recover damages for past infringement. A true and correct copy of the '150 patent is attached hereto as Exhibit B.

25. On February 11, 2003, the Patent Office duly and legally issued United States Letters Patent No. 6,519,466 ("the '466 patent"), entitled "Multi-Mode Global Positioning System For Use With Wireless Networks." CSR is the assignee of all rights, title, and interest in and to the '466 patent and possesses all rights of recovery under the '466 patent, including the right to recover damages for past infringement. Broadcom requested *ex parte* reexamination of the '466 patent on August 6, 2008, and the Patent Office issued an *Ex Parte*

Reexamination Certificate, confirming the patentability of the '466 patent, on May 18, 2010. A true and correct copy of the '466 patent is attached hereto as Exhibit C.

26. On November 18, 2003, the Patent Office duly and legally issued United States Letters Patent No. 6,650,879 ("the '879 patent"), entitled "Personal Communications Device with GPS Receiver and Common Clock Source." CSR is the assignee of all rights, title, and interest in and to the '879 patent and possesses all rights of recovery under the '879 patent, including the right to recover damages for past infringement. Broadcom requested *ex parte* reexamination of the '879 patent on September 19, 2008, and the Patent Office issued an *Ex Parte* Reexamination Certificate, confirming the patentability of the '879 patent, on October 20, 2009. A true and correct copy of the '879 patent is attached hereto as Exhibit D.

27. On April 19, 2005, the Patent Office duly and legally issued United States Letters Patent No. 6,882,827 ("the '827 patent"), entitled "Testing Response of a Radio Tranceiver." CSR is the assignee of all rights, title, and interest in and to the '827 patent and possesses all rights of recovery under the '827 patent, including the right to recover damages for past infringement. A true and correct copy of the '827 patent is attached hereto as Exhibit E.

28. On August 23, 2005, the Patent Office duly and legally issued United States Letters Patent No. 6,934,322 ("the '322 patent"), entitled "Data Message Bit Synchronization and Local Time Correction Methods and Architectures." CSR is the assignee of all rights, title, and interest in and to the '322 patent and possesses all rights of recovery under the '322 patent, including the right to recover damages for past infringement. A true and correct copy of the '322 patent is attached hereto as Exhibit F.

29. On November 28, 2006, the Patent Office duly and legally issued United States Letters Patent No. 7,142,157 ("the '157 patent"), entitled "Determining Position Without Use of Broadcast Ephemeris Information." CSR is the assignee of all rights, title, and interest in and to the '157 patent and possesses all rights of recovery under the '157 patent, including the right to recover damages for past infringement. Broadcom requested *ex parte* reexamination of the '157 patent on August 27, 2008, and the Patent Office issued an *Ex Parte*

Reexamination Certificate, confirming the patentability of the '157 patent, on December 22, 2009. A true and correct copy of the '157 patent is attached hereto as Exhibit G.

30. On June 26, 2007, the Patent Office duly and legally issued United States Letters Patent No. 7,236,883 ("the '883 patent"), entitled "Aiding In A Satellite Positioning System." CSR is the assignee of all rights, title, and interest in and to the '883 patent and possesses all rights of recovery under the '883 patent, including the right to recover damages for past infringement. A true and correct copy of the '883 patent is attached hereto as Exhibit H.

31. On August 11, 2009, the Patent Office duly and legally issued United States Letters Patent No. 7,573,422 ("the '422 patent"), entitled "Advanced Power Management for Satellite Positioning System." CSR is the assignee of all rights, title, and interest in and to the '422 patent and possesses all rights of recovery under the '422 patent, including the right to recover damages for past infringement. A true and correct copy of the '422 patent is attached hereto as Exhibit I.

FIRST CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 5,663,735

32. Plaintiff incorporates the allegations of paragraphs 1-31 as though fully set forth herein.

33. Upon information and belief, Broadcom has infringed and continues to infringe, directly and/or indirectly by way of inducement and/or contributory infringement, literally and/or under the doctrine of equivalents, in violation of 35 U.S.C. § 271, one or more claims of the '735 patent by making, having made, using, importing, selling and/or offering for sale in the United States one or more semiconductor products that embody the invention claimed in the '735 patent, or that use and/or incorporate the claimed invention, including, by way of example and without limitation, the BCM4750, BCM4751, BCM2075, BCM20751, and Hammerhead II GPS semiconductor products, the BCM 21331, BCM 2153, BCM 2091 and BCM 21553 baseband processors, and Broadcom's CellAirity Mobile Platform.

34. By infringing the '735 patent, Broadcom has caused and will continue to cause Plaintiff to suffer damages in an amount to be determined at trial.

35. Plaintiff has no adequate remedy at law against Broadcom's act of infringement, and unless Broadcom is preliminarily and permanently enjoined from infringing the '735 patent, CSR will suffer irreparable harm.

36. Upon information and belief, Broadcom's infringement of the '735 patent is willful and CSR should be awarded increased damages pursuant to 35 U.S.C. § 284 and attorneys fees pursuant to 35 U.S.C. § 285.

SECOND CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 6,480,150

37. Plaintiff incorporates the allegations of paragraphs 1-31 as though fully set forth herein.

38. Upon information and belief, Broadcom has infringed and continues to infringe, directly and/or indirectly by way of inducement and/or contributory infringement, literally and/or under the doctrine of equivalents, in violation of 35 U.S.C. § 271, one or more claims of the '150 patent by making, having made, using, importing, selling and/or offering for sale in the United States one or more GPS semiconductor products that embody the invention claimed in the '150 patent, or that use and/or incorporate the claimed invention, including, by way of example and without limitation, the BCM4750, BCM4751, BCM4760, BCM2075, BCM20751, and Hammerhead II GPS semiconductor products.

39. By infringing the '150 patent, Broadcom has caused and will continue to cause Plaintiff to suffer damages in an amount to be determined at trial.

40. Plaintiff has no adequate remedy at law against Broadcom's act of infringement, and unless Broadcom is preliminarily and permanently enjoined from infringing the '150 patent, CSR will suffer irreparable harm.

41. Upon information and belief, Broadcom's infringement of the '150 patent is willful and CSR should be awarded increased damages pursuant to 35 U.S.C. § 284 and attorneys fees pursuant to 35 U.S.C. § 285.

THIRD CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 6,519,466

42. Plaintiff incorporates the allegations of paragraphs 1-31 as though fully set forth herein.

43. Upon information and belief, Broadcom has infringed and continues to infringe, directly and/or indirectly by way of inducement and/or contributory infringement, literally and/or under the doctrine of equivalents, in violation of 35 U.S.C. § 271, one or more claims of the '466 patent by making, having made, using, importing, selling and/or offering for sale in the United States one or more semiconductor products that embody the invention claimed in the '466 patent, or that use and/or incorporate the claimed invention, including, by way of example and without limitation, the BCM4750, BCM4751, BCM2075, BCM20751, and Hammerhead II GPS semiconductor products, Broadcom's LTO and AGPS server technology, and Broadcom's CellAirity Mobile Platform.

44. By infringing the '466 patent, Broadcom has caused and will continue to cause Plaintiff to suffer damages in an amount to be determined at trial.

45. Plaintiff has no adequate remedy at law against Broadcom's act of infringement, and unless Broadcom is preliminarily and permanently enjoined from infringing the '466 patent, CSR will suffer irreparable harm.

46. On August 6, 2008, according to the records of the Patent Office, Broadcom requested *ex parte* reexamination of the '466 patent, seeking to have the '466 patent invalidated. On May 18, 2010, the Patent Office confirmed the patentability of the '466 patent.

47. Broadcom was aware of the '466 patent at least as early as August 6, 2008, when it requested reexamination of that patent.

48. Upon information and belief, Broadcom's infringement of the '466 patent is willful and CSR should be awarded increased damages pursuant to 35 U.S.C. § 284 and attorneys fees pursuant to 35 U.S.C. § 285

FOURTH CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 6,650,879

49. Plaintiff incorporates the allegations of paragraphs 1-31 as though fully set forth herein.

50. Upon information and belief, Broadcom has infringed and continues to infringe, directly and/or indirectly by way of inducement and/or contributory infringement, literally and/or under the doctrine of equivalents, in violation of 35 U.S.C. § 271, one or more claims of the '879 patent by making, having made, using, importing, selling and/or offering for sale in the United States one or more GPS semiconductor products that embody the invention claimed in the '879 patent, or that use and/or incorporate the claimed invention, including, by way of example and without limitation, the BCM4750, BCM4751, BCM2075, BCM20751, and Hammerhead II GPS semiconductor products.

51. By infringing the '879 patent, Broadcom has caused and will continue to cause Plaintiff to suffer damages in an amount to be determined at trial.

52. Plaintiff has no adequate remedy at law against Broadcom's act of infringement, and unless Broadcom is preliminarily and permanently enjoined from infringing the '879 patent, CSR will suffer irreparable harm.

53. On September 19, 2008, according to the records of the Patent Office, Broadcom requested *ex parte* reexamination of the '879 patent, seeking to have the '879 patent invalidated. On October 20, 2009, the Patent Office confirmed the patentability of the '879 patent.

54. Broadcom was aware of the '879 patent at least as early as September 19, 2008, when it requested reexamination of that patent.

55. Upon information and belief, Broadcom's infringement of the '879 patent is willful and CSR should be awarded increased damages pursuant to 35 U.S.C. § 284 and attorneys fees pursuant to 35 U.S.C. § 285.

FIFTH CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 6,882,827

56. Plaintiff incorporates the allegations of paragraphs 1-31 as though fully set forth herein.

57. Upon information and belief, Broadcom has infringed and continues to infringe, directly and/or indirectly by way of inducement and/or contributory infringement, literally and/or under the doctrine of equivalents, in violation of 35 U.S.C. § 271, one or more claims of the '827 patent by making, having made, using, importing, selling and/or offering for sale in the United States one or more GPS semiconductor products that embody the invention claimed in the '827 patent, or that use and/or incorporate the claimed invention, including, by way of example and without limitation, the BCM2075, BCM20751, BCM4325 and BCM4329 wireless communication semiconductor products.

58. By infringing the '827 patent, Broadcom has caused and will continue to cause Plaintiff to suffer damages in an amount to be determined at trial.

59. Plaintiff has no adequate remedy at law against Broadcom's act of infringement, and unless Broadcom is preliminarily and permanently enjoined from infringing the '827 patent, CSR will suffer irreparable harm.

60. Upon information and belief, Broadcom's infringement of the '827 patent is willful and CSR should be awarded increased damages pursuant to 35 U.S.C. § 284 and attorneys fees pursuant to 35 U.S.C. § 285.

SIXTH CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 6,934,322

61. Plaintiff incorporates the allegations of paragraphs 1-31 as though fully set forth herein.

62. Upon information and belief, Broadcom has infringed and continues to infringe, directly and/or indirectly by way of inducement and/or contributory infringement, literally and/or under the doctrine of equivalents, in violation of 35 U.S.C. § 271, one or more claims of the '322 patent by making, having made, using, importing, selling and/or offering for sale in the United States one or more GPS semiconductor products that embody the invention claimed in the '322 patent, or that use and/or incorporate the claimed invention, including, by way of example and without limitation, the BCM4750, BCM4751, BCM4760, BCM2075, BCM20751, and Hammerhead II GPS semiconductor products.

63. By infringing the '322 patent, Broadcom has caused and will continue to cause Plaintiff to suffer damages in an amount to be determined at trial.

64. Plaintiff has no adequate remedy at law against Broadcom's act of infringement, and unless Broadcom is preliminarily and permanently enjoined from infringing the '322 patent, CSR will suffer irreparable harm.

65. Upon information and belief, Broadcom's infringement of the '322 patent is willful and CSR should be awarded increased damages pursuant to 35 U.S.C. § 284 and attorneys fees pursuant to 35 U.S.C. § 285.

SEVENTH CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 7,142,157

66. Plaintiff incorporates the allegations of paragraphs 1-31 as though fully set forth herein.

67. Upon information and belief, Broadcom has infringed and continues to infringe, directly and/or indirectly by way of inducement and/or contributory infringement, literally and/or under the doctrine of equivalents, in violation of 35 U.S.C. § 271, one or more claims of the '157 patent by making, having made, using, importing, selling and/or offering for sale in the United States one or more GPS semiconductor products that embody the invention claimed in the '157 patent, or that use and/or incorporate the claimed invention, including, by way of example and

without limitation, the BCM4750, BCM4751, BCM4760, BCM2075, BCM20751 and Hammerhead II GPS semiconductor products.

68. By infringing the '157 patent, Broadcom has caused and will continue to cause Plaintiff to suffer damages in an amount to be determined at trial.

69. Plaintiff has no adequate remedy at law against Broadcom's act of infringement, and unless Broadcom is preliminarily and permanently enjoined from infringing the '157 patent, CSR will suffer irreparable harm.

70. On August 27, 2008, according to the records of the Patent Office, Broadcom requested *ex parte* reexamination of the '157 patent, seeking to have the '157 patent invalidated. On December 22, 2009, the Patent Office confirmed the patentability of the '157 patent.

71. Broadcom was aware of the '157 patent at least as early as August 27, 2008, when it requested reexamination of that patent.

72. Upon information and belief, Broadcom's infringement of the '157 patent is willful and CSR should be awarded increased damages pursuant to 35 U.S.C. § 284 and attorneys fees pursuant to 35 U.S.C. § 285.

EIGHTH CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 7,236,883

73. Plaintiff incorporates the allegations of paragraphs 1-31 as though fully set forth herein.

74. Upon information and belief, Broadcom has infringed and continues to infringe, directly and/or indirectly by way of inducement and/or contributory infringement, literally and/or under the doctrine of equivalents, in violation of 35 U.S.C. § 271, one or more claims of the '883 patent by making, having made, using, importing, selling and/or offering for sale in the United States one or more semiconductor products that embody the invention claimed in the '883 patent, or that use and/or incorporate the claimed invention, including, by way of example and without limitation, the BCM4750, BCM4751, BCM2075, BCM20751, and Hammerhead

II GPS semiconductor products, the BCM 21331, BCM 2153, BCM 2091 and BCM 21553 baseband processors, and Broadcom's CellAirity Mobile Platform.

75. By infringing the '883 patent, Broadcom has caused and will continue to cause Plaintiff to suffer damages in an amount to be determined at trial.

76. Plaintiff has no adequate remedy at law against Broadcom's act of infringement, and unless Broadcom is preliminarily and permanently enjoined from infringing the '883 patent, CSR will suffer irreparable harm.

77. Upon information and belief, Broadcom's infringement of the '883 patent is willful and CSR should be awarded increased damages pursuant to 35 U.S.C. § 284 and attorneys fees pursuant to 35 U.S.C. § 285.

NINTH CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 7,573,422

78. Plaintiff incorporates the allegations of paragraphs 1-31 as though fully set forth herein.

79. Upon information and belief, Broadcom has infringed and continues to infringe, directly and/or indirectly by way of inducement and/or contributory infringement, literally and/or under the doctrine of equivalents, in violation of 35 U.S.C. § 271, one or more claims of the '422 patent by making, having made, using, importing, selling and/or offering for sale in the United States one or more GPS semiconductor products that embody the invention claimed in the '422 patent, or that use and/or incorporate the claimed invention, including, by way of example and without limitation, the BCM4750, BCM4751, BCM2075, and BCM20751 GPS semiconductor products.

80. By infringing the '422 patent, Broadcom has caused and will continue to cause Plaintiff to suffer damages in an amount to be determined at trial.

81. Plaintiff has no adequate remedy at law against Broadcom's act of infringement, and unless Broadcom is preliminarily and permanently enjoined from infringing the '422 patent, CSR will suffer irreparable harm.

82. Upon information and belief, Broadcom's infringement of the '422 patent is willful and CSR should be awarded increased damages pursuant to 35 U.S.C. § 284 and attorneys fees pursuant to 35 U.S.C. § 285.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff prays for judgment on the complaint as follows:

a. Judgment in favor of Plaintiff and against Defendant for infringement of the '735, '150, '466, '879, '827, '322, '157, '883 and '422 patents;

b. Entry of a preliminary and permanent injunction enjoining Defendant, its affiliated entities, its officers, agents, servants, employees, and those persons in active concert or participation with them who receive actual notice thereof, from directly or indirectly infringing, inducing the infringement of, or contributing to the infringement of the '735, '150, '466, '879, '827, '322, '157, '883 and '422 patents;

c. An award to Plaintiff for compensatory damages caused by Defendant's infringement, together with pre-judgment and post-judgment interest thereon;

d. An award to Plaintiff of increased damages for Defendant's willful infringement;

e. An award to Plaintiff for costs, interest, and reasonable attorneys' fees incurred herein;

f. An accounting for future sales; and

g. Such other and further relief as the Court may deem just and appropriate.

DEMAND FOR JURY TRIAL

In accordance with Fed. R. Civ. P. 38(b) and Local Rule 38-1, Plaintiff CSR demands a trial by jury on all issues so triable.

Dated: August 20, 2010

SIMPSON THACHER & BARTLETT LLP

By: _____
JEFFREY E. OSTROW
Attorneys for Plaintiff CSR plc

Jeffrey E. Ostrow
SIMPSON THACHER & BARTLETT LLP
2550 Hanover Street
Palo Alto, CA 94304
Tel: (650) 251-5000
Fax: (650) 251-5002

Exhibit A

US005663735A

United States Patent [19]

Eshenbach

[11] Patent Number: 5,663,735

[45] Date of Patent: Sep. 2, 1997

[54] **GPS RECEIVER USING A RADIO SIGNAL FOR IMPROVING TIME TO FIRST FIX**

[75] Inventor: **Ralph F. Eshenbach**, Woodside, Calif.

[73] Assignee: **Trimble Navigation Limited**, Sunnyvale, Calif.

[21] Appl. No.: **650,482**

[22] Filed: **May 20, 1996**

[51] **Int. Cl.**[6] **H04B 7/185**; G01S 5/02

[52] **U.S. Cl.** **342/357**

[58] **Field of Search** 342/357; 455/67.6

[56] **References Cited**

U.S. PATENT DOCUMENTS

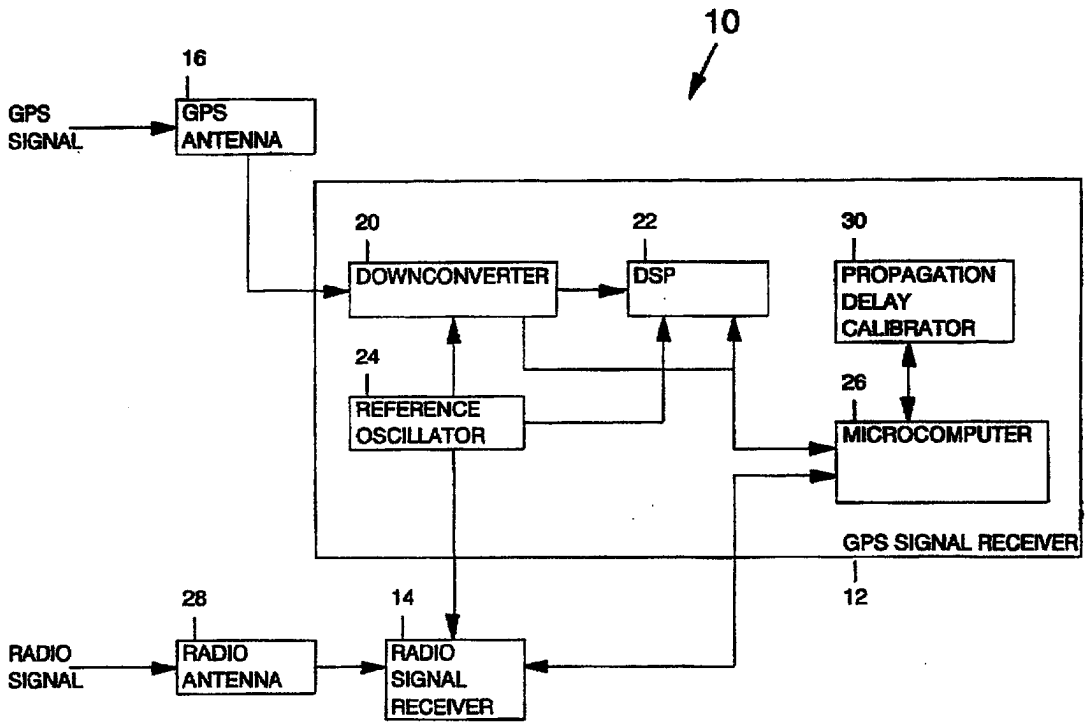
5,477,228	12/1995	Tiwari et al.	342/357
5,499,032	3/1996	Kelley et al.	342/357
5,523,761	6/1996	Gildea	342/357

Primary Examiner—Theodore M. Blum
Attorney, Agent, or Firm—David R. Gildea

[57] **ABSTRACT**

A global positioning system (GPS) receiver apparatus using time and frequency information derived from a radio signal other than the GPS satellite signal for improving the time to first fix (TTFF). The GPS receiver apparatus includes a GPS signal receiver for receiving a GPS satellite signal modulated with data bits and a radio signal receiver for receiving a radio signal having a standard time and/or a standard frequency. The radio signal receiver provides standard time information to the GPS signal receiver. The GPS signal receiver uses the standard time information to resolve a GPS time for a time of arrival of a data bit. The GPS signal receiver includes a propagation delay calibrator for correcting the standard time for the travel time due to the path length for the radio signal. The radio signal receiver uses a reference clock signal provided by the GPS signal receiver for determining a frequency error between a frequency of the reference clock signal and the standard frequency. The GPS signal receiver uses the frequency error for pre-tuning to the carrier frequency of the GPS satellite signal.

17 Claims, 5 Drawing Sheets



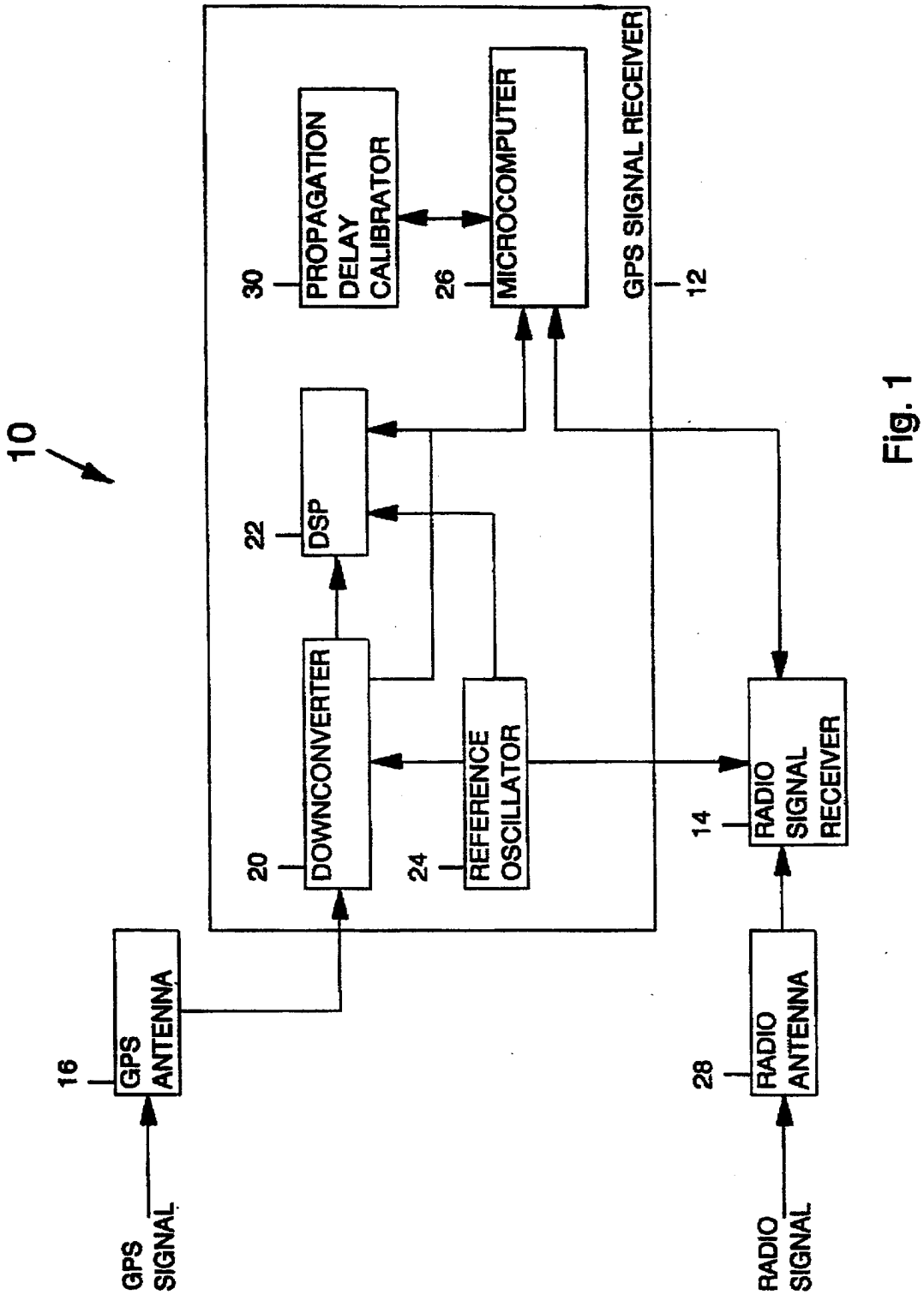

10
GPS SIGNAL RECEIVER
12
PROPAGATION DELAY CALIBRATOR
30
MICROCOMPUTER
26
DSP
22
DOWNCONVERTER
20
REFERENCE OSCILLATOR
24
RADIO SIGNAL RECEIVER
14
GPS ANTENNA
16
RADIO ANTENNA
28
GPS SIGNAL
RADIO SIGNAL

Fig. 1

HF STANDARD FREQUENCY AND TIME SIGNAL BROADCASTS					
Name	Country	Carrier Power (kW)	Broadcast Frequency (MHz)	Days/ Week	Hours/ Day
ATA	India	8	5, 10, 15	7	24
BPM	China	10-20	2.5, 5, 10, 15	7	24
CHU	Canada	3-10	3.330, 7.335, and 14.670	7	24
HLA	Republic of Korea	2	5	5	7
IAM	Italy	1	5	6	2
IBF	Italy	5	5	7	2.75
JJY	Japan	2	2.5, 5, 8, 10, 15	7	24
LOL	Argentina	2	5, 10, 15	7	5
OMA	Czecho-slovakia	1	2.5	7	24
RCH	USSR	1	2.5, 5, 10	7	21
RID	USSR	1	5.004, 10.004, 15.004	7	24
RIM	USSR	1	5, 10	7	20.5
RTA	USSR	5	10, 15	7	20.5
RWM	USSR	5-8	4.996, 9.996, 14.996	7	24
VNG	Australia	10	5, 10, 15	7	24
WWV	United States	2.5-10	2.5, 5, 10, 15, 20	7	24
WWVH	United States	5-10	2.5, 5, 10, 15	7	24
ZLFS	New Zealand	0.3	2.5	1	3
ZUO	South Africa	4	2.5, 5	7	24

Fig. 2a

LF and VLF Time and Frequency Stations					
Call Sign	Location	Power (kW)	Carrier (kHz)	Days/ Week	Hours/ Day
DCF77	Mainflingen, Germany	20	77.50	7	24
GBR	Rugby, United Kingdom	60	15.95 16.00	7	22
HBG	Prangins, Switzerland	20	75.00	7	24
JJF-2 JG2AS	Sanwa, Sashima, Ibaraki, Japan	10	40.00	7	24
MSF	Rugby, United Kingdom	25	60.00	7	24
NAA	Cutler, Maine United States	1000	24.00	7	24
NCA	Aguada, Puerto Rico	100	28.50	7	24
NTD	Yoshima, Japan	50	17.40	7	24
NLK	Jim Creek, Washington, United States	125	24.80	7	24
NPM	Lualualei, Hawaii, United States	600	23.40	7	24
NSS	Annapolis, Maryland, United States	400	21.40	7	24

Fig. 2b

LF and VLF Time and Frequency Stations					
Call Sign	Location	Power (kW)	Carrier (kHz)	Days/ Week	Hours/ Day
NWC	NW Cape, Australia	1000	22.30	7	24
OMA	Liblice, Czechoslovakia	5	50.00	7	24
RBU	Moskva, USSR	10	66.67	7	24
RTZ	Irkutsk, USSR	10	50.00	7	23
RW-166	Irkutsk, USSR	40	200.00	7	23
RW-76	Novosibirsk, USSR	150	272.00	7	22
UNW3	Molodechno, USSR	---	25.50, 25.10 25.00, 23.00 20.50	7	2
UPD8	Arkhangelsk, USSR	---	25.50, 25.10 25.00, 23.00 20.50	7	2
UQC3	Khabarovsk, USSR	300	25.50, 25.10 25.00, 23.00 20.50	7	2
USB2	Frunze, USSR	---	25.50, 25.10 25.00, 23.00 20.50	7	3
UTR3	Gorky, USSR	300	25.50, 25.10 25.00, 23.00 20.50	7	2

Fig. 2c

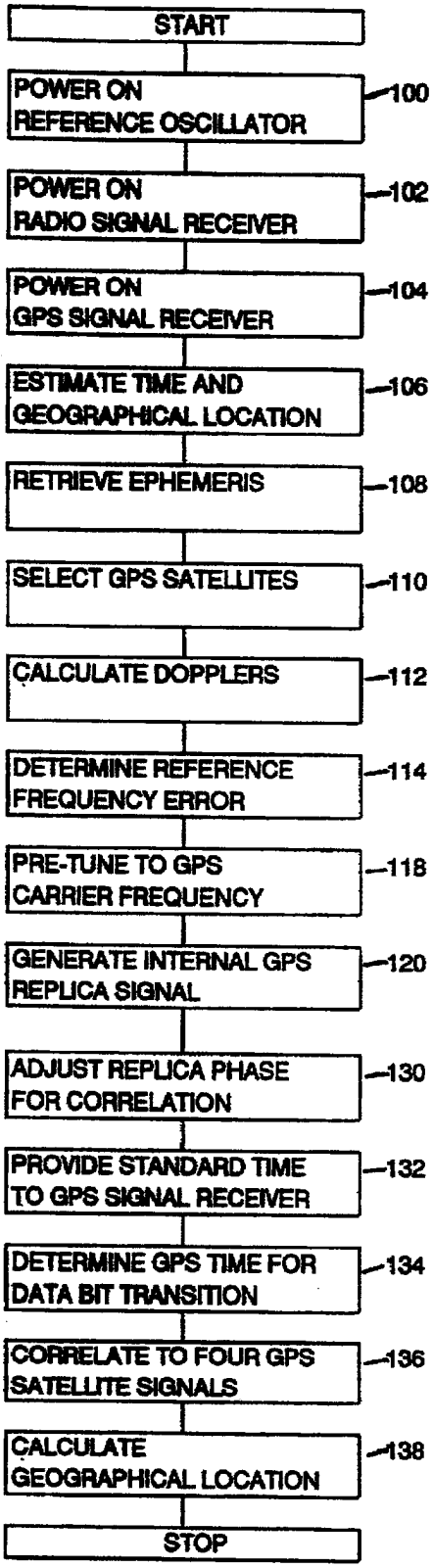

START
POWER ON REFERENCE OSCILLATOR
100
POWER ON RADIO SIGNAL RECEIVER
102
POWER ON GPS SIGNAL RECEIVER
104
ESTIMATE TIME AND GEOGRAPHICAL LOCATION
106
RETRIEVE EPHEMERIS
108
SELECT GPS SATELLITES
110
CALCULATE DOPPLERS
112
DETERMINE REFERENCE FREQUENCY ERROR
114
PRE-TUNE TO GPS CARRIER FREQUENCY
118
GENERATE INTERNAL GPS REPLICA SIGNAL
120
ADJUST REPLICA PHASE FOR CORRELATION
130
PROVIDE STANDARD TIME TO GPS SIGNAL RECEIVER
132
DETERMINE GPS TIME FOR DATA BIT TRANSITION
134
CORRELATE TO FOUR GPS SATELLITE SIGNALS
136
CALCULATE GEOGRAPHICAL LOCATION
138
STOP

Fig. 3

GPS RECEIVER USING A RADIO SIGNAL FOR IMPROVING TIME TO FIRST FIX

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates generally to global positioning system (GPS) receivers and more particularly to a GPS receiver apparatus having an improved time to first fix by using standard time and frequency information available from a radio signal.

2. Description of the Prior Art

Global positioning system (GPS) receivers are used in many applications where accurate time and geographical location are required. In several applications, it is important to minimize the time delay between when the GPS receiver is turned on and when it determines a GPS-based time and/or geographical location. This time delay, known as the time to first fix (TTFF) includes (i) time to tune the frequency of the GPS receiver to a carrier frequency of a GPS signal from a GPS satellite, (ii) time to align a phase of an internally generated pseudo-random noise (PRN) code to a PRN code in the GPS signal, (iii) time to receive data bits in the GPS signal to determine a GPS-based time, (iv) time to tune frequency and align phase to acquire a GPS signal from a second, a third, and a fourth GPS satellite, and (v) time to calculate a GPS-based geographical location. Fewer than four GPS satellites may be sufficient if the GPS receiver has other information such as altitude. The TTFF may include additional time delay if the GPS receiver does not already have an approximate time, its approximate geographical location, and ephemeris information for the locations in space of the GPS satellites. Existing GPS receivers have TTFFs in the range of a few tens of seconds to a few minutes.

The GPS signal is modulated with data bits at a fifty bits per second (BPS) rate (twenty milliseconds per bit) that are modulated by a coarse/acquisition (C/A) PRN code sequence at a 1.023 megahertz rate (one microsecond per chip) that is 1023 chips long (one millisecond). Each of the GPS satellites has a distinct PRN code that enables the GPS receiver to distinguish the GPS signal of one GPS satellite from the GPS signal of another GPS satellite. The data bits are organized into sub-frames that are six seconds in length. Each sub-frame includes a hand over word (HOW) that includes information for the GPS time of emission for a data bit. In existing GPS receivers, the time to receive the data bits to determine the GPS-based time includes up to six seconds to receive the GPS time in the HOW. Under some conditions the GPS receiver must receive more than one HOW, thereby adding more than one six second time increment to the TTFF.

The time to tune the frequency of the GPS receiver to the carrier frequency of the GPS signal depends upon the accuracy of an internal reference frequency. Some existing GPS receivers have eliminated or minimized this time by using a highly accurate internal reference oscillator such as an oven stabilized crystal oscillator or an atomic clock. However, such oscillators typically have a high power consumption and are expensive. Instead, most existing GPS receivers tune to the carrier frequency using a frequency search where first one frequency and then another is tried until a correct carrier frequency is found. Unfortunately, the time to do the frequency search increases the TTFF.

There is a need for a GPS receiver apparatus that determines GPS time without waiting for the HOW in the GPS signal and/or tunes to the GPS signal without using a highly accurate oscillator or frequency searching in order to have a fast time to first fix (TTFF).

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a global positioning system (GPS) receiver apparatus that uses standard time information derived from a radio signal other than the GPS satellite signal for determining a time of a transition between two data bits of the GPS satellite for providing a GPS-based time.

Another object is to provide a GPS receiver apparatus that uses standard frequency information of a radio signal other than the GPS satellite signal for pre-tuning the frequency of a GPS receiver apparatus for acquiring a GPS satellite signal.

Briefly, in a preferred embodiment, a global position system (GPS) receiver apparatus includes a GPS signal receiver for receiving a GPS signal having GPS time and geographical location determination data bits and a radio signal receiver for receiving a radio signal having a standard time and/or standard frequency information. The radio signal receiver provides the standard time information to the GPS signal receiver. The GPS signal receiver includes a downconverter for downconverting the GPS signal to a GPS intermediate frequency (IF) signal; a digital signal processor (DSP) for correlating the GPS IF signal to an internally generated GPS replica signal and providing correlation data; a reference oscillator for providing the reference clock signal to the DSP for generating the GPS replica signal; and a microcomputer for using the standard time information and the correlation data to resolve the GPS time for a time of arrival of a data bit and providing a GPS-based time and geographical location. The GPS signal receiver further includes a propagation delay calibrator for correcting the standard time information for a travel time due to a path length for the radio signal. Optionally, the radio signal receiver uses the reference clock signal for providing frequency error information for a difference between a multiple of a frequency of the reference clock signal and the standard frequency. The GPS signal receiver uses the frequency error information for pre-tuning the GPS signal receiver to the frequency of the GPS satellite signal.

An advantage of the GPS receiver apparatus of the present invention is that it uses standard time information in a radio signal for determining a GPS time, thereby improving a time to first fix (TTFF).

Another advantage of the GPS receiver apparatus of the present invention is that it uses standard frequency information in a radio signal for pre-tuning to the frequency of the GPS satellite signal, thereby improving a time to first fix (TTFF).

These and other objects and advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiments which are illustrated in the various figures.

IN THE DRAWINGS

FIG. 1 is a block diagram of a GPS receiver apparatus of the present invention providing a fast time to first fix (TTFF);

FIG. 2*a* is a table of stations broadcasting high frequency (HF) radio signals having a standard time and a standard frequency for reception by the radio signal receiver of FIG. 1;

FIGS. 2*b* and 2*c* are tables of stations broadcasting low or very low frequency (LF/VLF) radio signals having a standard time and a standard frequency for reception by the radio signal receiver of FIG. **1**; and

FIG. **3** is a flow chart of a method using the GPS receiver apparatus of FIG. **1** for a fast TTFF.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. **1** illustrates a block diagram of a global positioning system (GPS) receiver apparatus of the present invention referred to by the general reference number **10**. The GPS receiver apparatus **10** includes a GPS signal receiver **12** for receiving a GPS signal from GPS satellites and a radio signal receiver **14** for receiving a radio signal having standard time and/or frequency information. The GPS signal includes a carrier signal that is modulated by data bits at a fifty BPS rate (twenty milliseconds per data bit). The data bits include information for determining a GPS-based time and geographical location. A pseudo-random noise (PRN) code sequence of 1023 chips that is distinct for each of the GPS satellites spreads the GPS signal by modulating the data bits at a chip rate of 1.023 megahertz (approximately one microsecond per chip) and a sequence rate of one kilohertz (one millisecond per sequence). A more complete description of the GPS signal is available in an "Interface Control Document ICD-GPS-200", revised in 1991, published by Rockwell International Corporation and incorporated herein by reference. The radio signal includes modulation for a standard time known to better than about ten milliseconds and optionally a standard carrier frequency that is known to better than about 1×10^{6} and preferable better than 3.3×10^{7}. Several stations, such as WWV, WWVH, WWVB, CHU, and GOES broadcast radio signals having such standard time and frequency. A more complete list and description of such stations is given in FIGS. 2*a*, 2*b*, and 2*c*.

A GPS antenna **16** receives the GPS signal from an airwave that is broadcast by the GPS satellite and converts it into a conducted GPS signal for processing by the GPS signal receiver **12**. The GPS signal receiver **12** includes a downconverter **20** connected to the antenna **16** for downconverting the frequency of the GPS signal to a GPS intermediate frequency (IF) signal; a digital signal processor (DSP) **22** connected to the downconverter **20** for generating a GPS replica signal, correlating the GPS replica signal to the GPS signal, and providing correlation data; a reference oscillator **24** connected for providing a reference clock signal for the downconverter **20** and the DSP **22**; and a microcomputer **26** connected to the radio signal receiver **14** for receiving the standard time and/or frequency information and the DSP **22** for receiving the correlation data and providing application information including the GPS-based time and the geographical location. Preferably the center frequency of the GPS IF signal is twenty-five megahertz or less, however, any frequency including baseband that is suitable for digital processing can be used. The microcomputer **26** includes a microprocessor such as a 68HC030 available from Motorola Corporation, one or more memory devices for storing executable program code and variable data, clocking circuitry, a real time clock, and associated signal conditioning and input/output hardware. The microprocessor operates in a conventional manner for receiving digital signal inputs, processing information in the inputs according to the program code, and issuing digital signal outputs for controlling the elements of the GPS receiver apparatus **10** and providing the application information. Optionally, the DSP **22** and the microcomputer **26** may be combined into a single circuit element or single integrated circuit.

The GPS replica signal includes a selected frequency and a selected PRN code sequence having a selected phase matching an expected frequency and expected PRN code sequence of the GPS signal having a phase, respectively. The selected frequency and selected phase are based upon a frequency and phase of the reference clock signal and a frequency and a phase adjustment provided by the microcomputer **26** based upon the correlation data. The process of adjusting the frequency and phase of the GPS replica signal to match or correlate to the actual frequency and phase of the GPS IF signal is known as "acquiring" the GPS signal. When the frequency and phase adjustments are such that the GPS replica signal has the approximately the same phase and frequency as the GPS IF signal, the GPS signal receiver **12** is said to be "tracking" and the correlation data indicates the senses of the data bits in the GPS signal. More complete explanations of the known techniques for GPS signal receivers are available in U.S. Pat. No. 4,754,465 by Charlie R. Trimble and U.S. Pat. No. 4,847,862 by Paul E. Braisted and Ralph F. Eschenbach for GLOBAL POSITIONING SYSTEM COURSE ACQUISITION CODE RECEIVERs incorporated herein by reference.

A radio antenna **28** receives the radio signal from an airwave that is broadcast by a station and converts it into a conducted radio signal for processing by the radio signal receiver **14**. The radio signal receiver **14** demodulates and decodes the radio signal and provides the information for the standard time to the microcomputer **26**. The radio signal receiver **14** may be designed and constructed as a high frequency (HF) radio receiver for receiving a radio signal in a frequency range of 2.5 to 30 megahertz, a low frequency (LF) radio receiver for receiving a radio signal in a 30 to 300 kilohertz range, or a very low frequency (VLF) radio receiver for receiving a radio signal in a 3 to 30 kilohertz range. Such radio receivers are well-known in the field of signal receivers. Optionally, the radio signal receiver **14** receives the reference clock signal and provides the microcomputer **26** with information for a frequency error of a difference between a selected multiple of the frequency of the reference clock signal and the standard frequency of the radio signal. The multiple may be an integer or a ratio of two integers either greater than or less than one depending upon the desired clocking rate for the DSP **22** and the type of construction used in the radio signal receiver **14**. Alternatively, the frequency error may be used to tune the frequency of the reference oscillator using a phase lock loop. In a preferred embodiment for acquiring the GPS signal, microprocessor **26** pre-tunes the frequency of the GPS signal receiver **12** by selecting an initial frequency adjustment based upon the frequency error information. Then, the microcomputer **26** and the DSP **22** cooperate to match the phase of the selected PRN code in the GPS replica signal to the phase of the PRN code in the GPS IF signal by trying PRN codes and phases until correlation is found indicating that the GPS signal has been acquired and the GPS signal receiver **12** is tracking.

As soon as the GPS signal receiver **12** is tracking the GPS signal, the microcomputer **26** uses the standard time, known to be accurate to within ten milliseconds, to determine the GPS time of a next sense transition of a data bit, having a twenty millisecond period, in the correlation data; thereby eliminating a requirement to wait up to six seconds or more until one or more HOWs are decoded. Optionally, when the GPS signal receiver **12** is tracking the GPS signal from more than one GPS satellite, the microcomputer **26** observes more than one stream of correlation data to minimize the likelihood that a sense transition is delayed by a long string of 1's

or 0's. Executable program code for a propagation delay calibrator **30** is stored in the memory in the microcomputer **26** for enabling the microcomputer **26** to calibrate the standard time for a time delay due to the path length between a stored geographical location of the station transmitting the radio signal and a stored, last known or estimated geographical location of the GPS antenna **16**.

FIGS. **2***a*, **2***b*, and **2***c* are tables of high frequency (HF) and low frequency and very low frequency (LF/VLF) standard frequency and time signal broadcasts, for use as the radio signal. The tables list names or call signs, countries or locations, powers in kilowatts, frequencies in megahertz or kilohertz, numbers of days of the week of broadcasting, and hours of the day of broadcasting.

FIG. **3** illustrates flow chart of activities of the GPS receiver apparatus **10** leading up to a first fix of the GPS-based time and geographical location by the GPS signal receiver **12**. At the start, the GPS receiver apparatus **10** is powered off or in a standby mode where at least one of the downconverter **20**, DSP **22**, and the microcomputer **26** are inhibited from using full operational power. In a step **100** the reference oscillator is powered on. For some applications, the power to the reference oscillator **24** remains on continuously. In a step **102** the radio signal receiver **14** is powered on and receives the reference clock signal and the radio signal. In a step **104** the GPS signal receiver **12** is powered on or is switched from a standby mode to a normal operational mode. In a step **106** the GPS signal receiver **12** estimates an approximate time based upon time information from the real time clock and an estimated geographical location for the GPS antenna **16** based upon a last known location and last known velocity. In a step **108** the GPS signal receiver **12** retrieves ephemeris information for the locations in space of the GPS satellites. In a step **110** the GPS signal receiver **12** uses the approximate time, estimated geographical location, and ephemeris information to select one or more GPS satellites for acquisition of the GPS signal. In a step **112** the GPS signal receiver **12** calculates Doppler shifts for the carrier frequencies of the GPS signal for the GPS satellites that were selected. In a step **114** the radio signal receiver **14** determines the frequency error for the difference between the selected multiple of the frequency of the reference clock signal and the standard frequency of the radio signal and provides the frequency error information to the GPS signal receiver **12**. In a step **118** the GPS signal receiver uses the Doppler shift and the frequency error information to pre-tune to the expected carrier frequency of the GPS signal from the selected GPS satellite. In a step **120** the GPS signal receiver **12** generates the GPS replica signal having the PRN code for the selected GPS satellite. The GPS signal receiver **12** is now ready to acquire the GPS signal.

In a step **130** the GPS signal receiver **12** adjusts the GPS replica signal PRN code phase until the GPS replica signal correlates to the GPS IF signal. The GPS signal receiver **12** is now tracking and receiving data bits from at least one GPS satellite. In a preferred embodiment, the GPS signal receiver **12** operates to pre-tune to the carrier frequencies from several GPS satellites and correlate with several PRN codes in parallel. In a step **132** the radio signal receiver **14** provides the standard time information to the GPS signal receiver **12**. In a step **134** the GPS signal receiver **12** applies the standard time information to determine the GPS-based time for the time of arrival of the transition of the sense between two data bits. When the GPS signal from more than one GPS satellite is being tracked, the GPS signal receiver **12** uses the data bit streams from any one of the GPS satellites in order to insure an timely transition will occur. In a step **136** the GPS signal receiver **12** correlates to the GPS signal from four GPS satellites. In a step **138** the GPS signal receiver **12** uses the GPS time, the ephemeris information, and the phases of the GPS replica PRN code sequence to calculate the GPS-based geographical location for the GPS antenna **16**.

Although the present invention has been described in terms of the presently preferred embodiments, it is to be understood that such disclosure is not to be interpreted as limiting. Various alterations and modifications will no doubt become apparent to those skilled in the art after having read the above disclosure. Accordingly, it is intended that the appended claims be interpreted as covering all alterations and modifications as fall within the true spirit and scope of the invention.

What is claimed is:

1. A global positioning system (GPS) receiver apparatus, comprising:

a radio signal receiver for receiving a radio signal having a standard time, decoding said standard time from said radio signal, and providing information for said standard time in a radio receiver output signal; and

a GPS signal receiver for receiving a GPS signal having data bits and coupled to the radio signal receiver for using said standard time information for resolving a GPS-based time for a time of arrival of one of said data bits.

2. The GPS receiver apparatus of claim **1**, wherein:

the GPS signal receiver includes a propagation delay calibrator for calibrating said standard time information for a path length of said radio signal.

3. The GPS receiver apparatus of claim **1**, wherein:

the radio signal receiver includes a low frequency (LF) radio signal receiver for receiving said radio signal from at least one of (i) WWVB, (ii) DCF77, (iii) HBG, (iv) IJF-2, (v) JG2AS, (vi) MSF, (vii) OMA, (viii) RBU, (ix) RTZ, (x) RW-166, and (xi) RW-76.

4. The GPS receiver apparatus of claim **1**, wherein:

the radio signal receiver includes a high frequency (HF) radio signal receiver for receiving said radio signal from at least one of (i) WWV, (ii) WWVH, (iii) CHU, (iv) ATA, (v) BPM, (vi) HLA, (vii) IAM, (viii) IBF, (ix) JJY, (x) LOL, (xi) OMA, (xii) RCH, (xiii) RID, (xiv) RIM, (xv) RTA, (xvi) RWM, (xvii) VNG, (xviii) ZLFS, and (xix) ZUO.

5. The GPS receiver apparatus of claim **1**, wherein:

the radio signal receiver includes a very low frequency (VLF) radio signal receiver for receiving said radio signal from at least one of (i) GBR, (ii) NAA, (iii) NCA, (iv) NTD, (v) NLK, (vi) NPM, (vii) NSS, (viii) NWC, (ix) UNW3, (x) UPD8, (xi) UQC3, (xii) USB2, and (xiii) UTR3.

6. The GPS receiver apparatus of claim **1**, wherein:

the radio signal receiver includes a GOES satellite signal receiver for receiving said radio signal from a GOES satellite.

7. The GPS receiver apparatus of claim **1**, further including:

a reference oscillator for providing a reference clock signal;

a microcomputer for receiving frequency error information for a difference between a frequency of said radio signal and a multiple of a frequency of said reference clock signal, and providing a responsive frequency adjustment; and

a digital signal processor for using said frequency adjustment for pre-tuning to a frequency of said GPS signal; and

wherein the radio signal receiver is further for receiving said reference clock signal and providing said frequency error information.

8. The GPS receiver apparatus of claim **1**, wherein:

the GPS receiver includes a digital signal processor for receiving a GPS intermediate frequency signal and providing said one of said data bits having said time of arrival; and a microcomputer for receiving said one of said data bits and resolving said GPS-based time for said time of arrival.

9. A global positioning system (GPS) receiver apparatus, comprising:

a radio signal receiver for receiving a radio signal having an accurate carrier frequency and for providing frequency error information for a difference between said carrier frequency and a multiple of a frequency of a reference clock signal; and

a GPS signal receiver coupled to the radio signal receiver, including:

a) a reference oscillator for providing said reference clock signal;

b) a microcomputer for using said frequency error information for providing a frequency adjustment; and

c) a digital signal processor for using said frequency adjustment for pre-tuning to a frequency for acquiring a GPS signal.

10. The GPS receiver apparatus of claim **8**, wherein:

the radio signal receiver includes a low frequency (LF) radio signal receiver for receiving said radio signal from at least one of (i) WWVB, (ii) DCF77, (iii) HBG, (iv) JJF-2, (v) JG2AS, (vi) MSF, (vii) OMA, (viii) RBU, (ix) RTZ, (x) RW-166, and (xi) RW-76.

11. The GPS receiver apparatus of claim **9**, wherein:

the radio signal receiver includes a high frequency (HF) radio signal receiver for receiving said radio signal from at least one of (i) WWV, (ii) WWVH, (iii) CHU, (iv) ATA, (v) BPM, (vi) HLA, (vii) IAM, (viii) IBF, (ix) JJY, (x) LOL, (xi) OMA, (xii) RCH, (xiii) RID, (xiv) RIM, (xv) RTA, (xvi) RWM, (xvii) VNG, (xviii) ZLFS, and (xix) ZUO.

12. The GPS receiver apparatus of claim **9**, wherein:

the radio signal receiver includes a very low frequency (VLF) radio signal receiver for receiving said radio signal from at least one of (i) GBR, (ii) NAA, (iii) NCA, (iv) NTD, (v) NLK, (vi) NPM, (vii) NSS, (viii) NWC, (ix) UNW3, (x) UPD8, (xi) UQC3, (xii) USB2, and (xiii) UTR3.

13. The GPS receiver apparatus of claim **9**, wherein:

the radio signal receiver includes a GOES satellite signal receiver for receiving said radio signal from a GOES satellite.

14. The GPS receiver apparatus of claim **9**, wherein:

said carrier frequency has an accuracy of at least 1×10^{-6}.

15. A method for improving time to first fix in a global positioning system (GPS) receiver apparatus for receiving a GPS signal, comprising steps of:

receiving a radio signal having a standard time;

decoding said standard time from said radio signal;

receiving said GPS signal having data bits; and

using said standard time for resolving a GPS-based time for a time of arrival of one of said data bits.

16. A method for improving time to first fix in a global positioning system (GPS) receiver apparatus for receiving a GPS signal, comprising steps of:

receiving a radio signal having an accurate carrier frequency;

providing a reference clock signal;

determining a frequency error for a difference between said carrier frequency and a multiple of a frequency of said reference clock signal;

using said frequency error for computing a frequency adjustment; and

using said frequency adjustment in a digital signal processor in said GPS receiver for pre-tuning to a frequency for acquiring said GPS signal.

17. The method of claim **16**, wherein:

said carrier frequency has an accuracy of at least 1×10^{-6}.

* * * * *

Exhibit B

US006480150B2

(12) **United States Patent**
Falk et al.

(10) **Patent No.: US 6,480,150 B2**
(45) **Date of Patent: *Nov. 12, 2002**

(54) **AUTONOMOUS HARDWIRED TRACKING LOOP COPROCESSOR FOR GPS AND WAAS RECEIVER**

(75) Inventors: **Henry D. Falk**, Long Beach; **Leon Kuo-Liang Peng**, Mountain View; **Wesley F. Marumo**, Cypress, all of CA (US)

(73) Assignee: **SiRF Technology, Inc.**, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **09/871,394**

(22) Filed: **May 31, 2001**

(65) **Prior Publication Data**

US 2001/0048388 A1 Dec. 6, 2001

Related U.S. Application Data

(63) Continuation of application No. 09/397,438, filed on Sep. 17, 1999.

(51) **Int. Cl.**[7] **G01S 5/02**; H04B 7/185; G06G 7/78; H04L 27/06

(52) **U.S. Cl.** **342/357.12**; 375/344; 701/213

(58) **Field of Search** 342/357.12; 375/316, 375/344; 701/213

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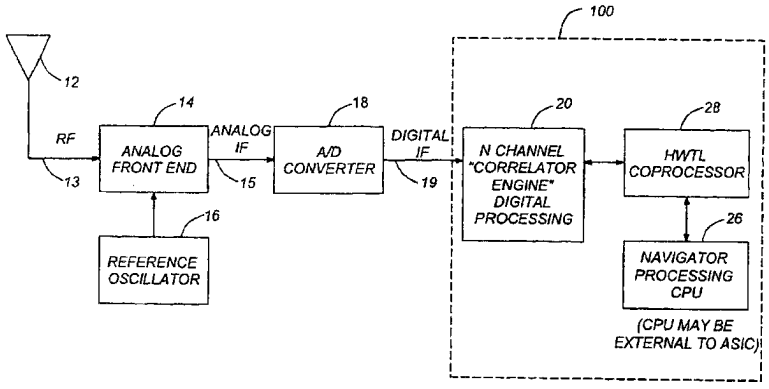
Primary Examiner—Thomas H. Tarcza
Assistant Examiner—Fred H Mull
(74) *Attorney, Agent, or Firm*—Thomas, Kayden, Horstemeyer & Risley, L.L.P.

(57) **ABSTRACT**

An autonomous Hardwired Tracking Loop (HWTL) ASIC comprising a HWTL coprocessor provided for implementing most of the receiver processing function for data acquisition and tracking functions of a radio receiver system in dedicated hardware. With the expanded functionality provided by an HWTL coprocessor in the autonomous HWTL ASIC, the interruption of CPU performing the navigation processing is significantly reduced to thereby maximize throughput and minimize power burden on the microprocessor. In the preferred embodiment, the HWTL ASIC also comprises the CPU and a correlator, wherein the correlator provides the high rate greater than approximately 1 KHz signal processing operations, the HWTL coprocessor providing the data acquisition and tracking (medium frequency signal processing) operations, and the CPU thereby freed to provide more bandwidth for lower frequency processing, i.e., navigation and non-radio receiver operations, such as user applications, processing requiring CPU intervention at approximately 10 Hz or less CPU processing rate.

36 Claims, 9 Drawing Sheets



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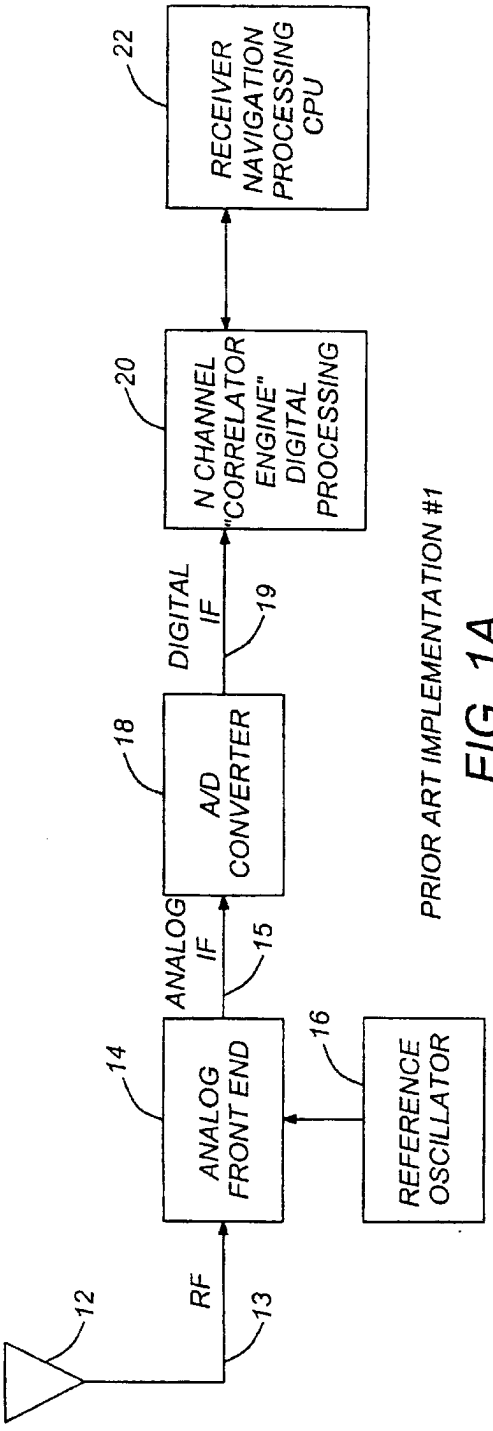
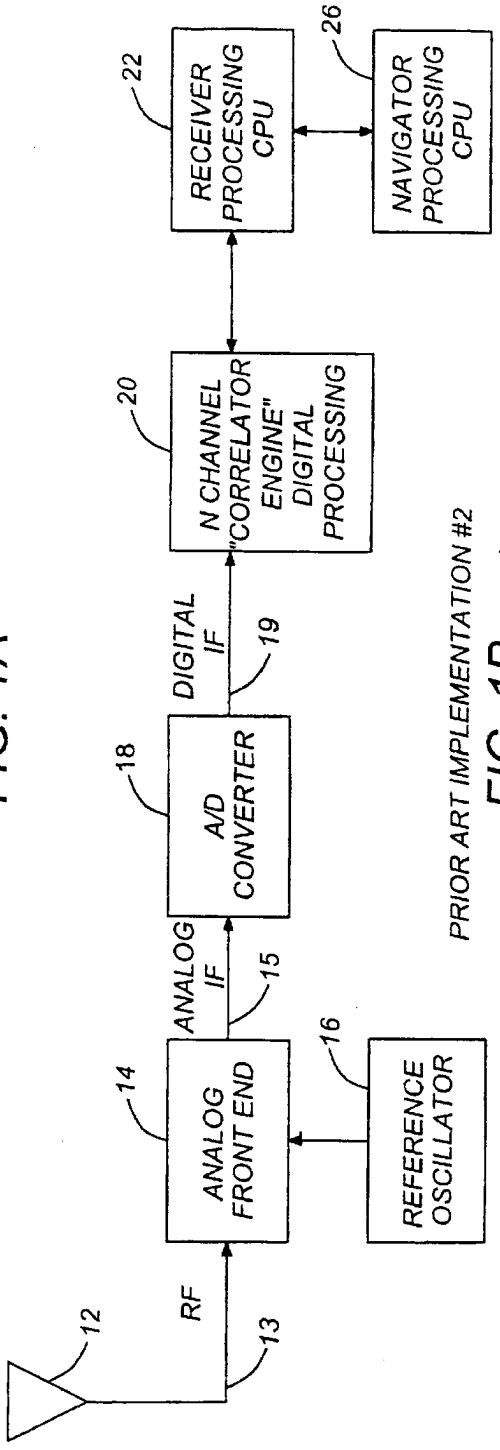


PRIOR ART IMPLEMENTATION #1

FIG. 1A



PRIOR ART IMPLEMENTATION #2

FIG. 1B

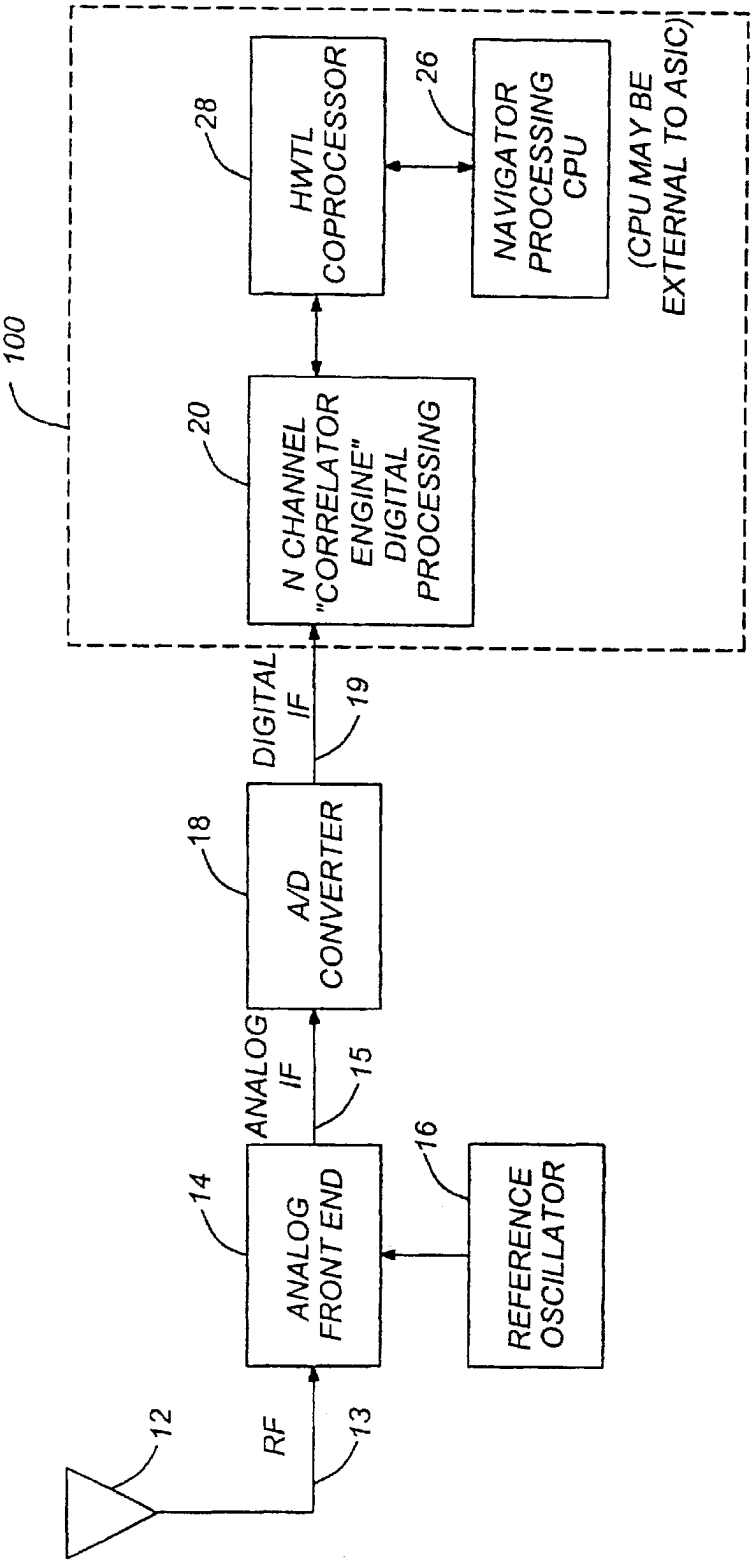

100
(CPU MAY BE EXTERNAL TO ASIC)
28
HWTL COPROCESSOR
26
NAVIGATOR PROCESSING CPU
20
N CHANNEL "CORRELATOR ENGINE" DIGITAL PROCESSING
DIGITAL IF
19
18
A/D CONVERTER
ANALOG IF
15
16
14
ANALOG FRONT END
REFERENCE OSCILLATOR
12
RF
13

FIG. 2

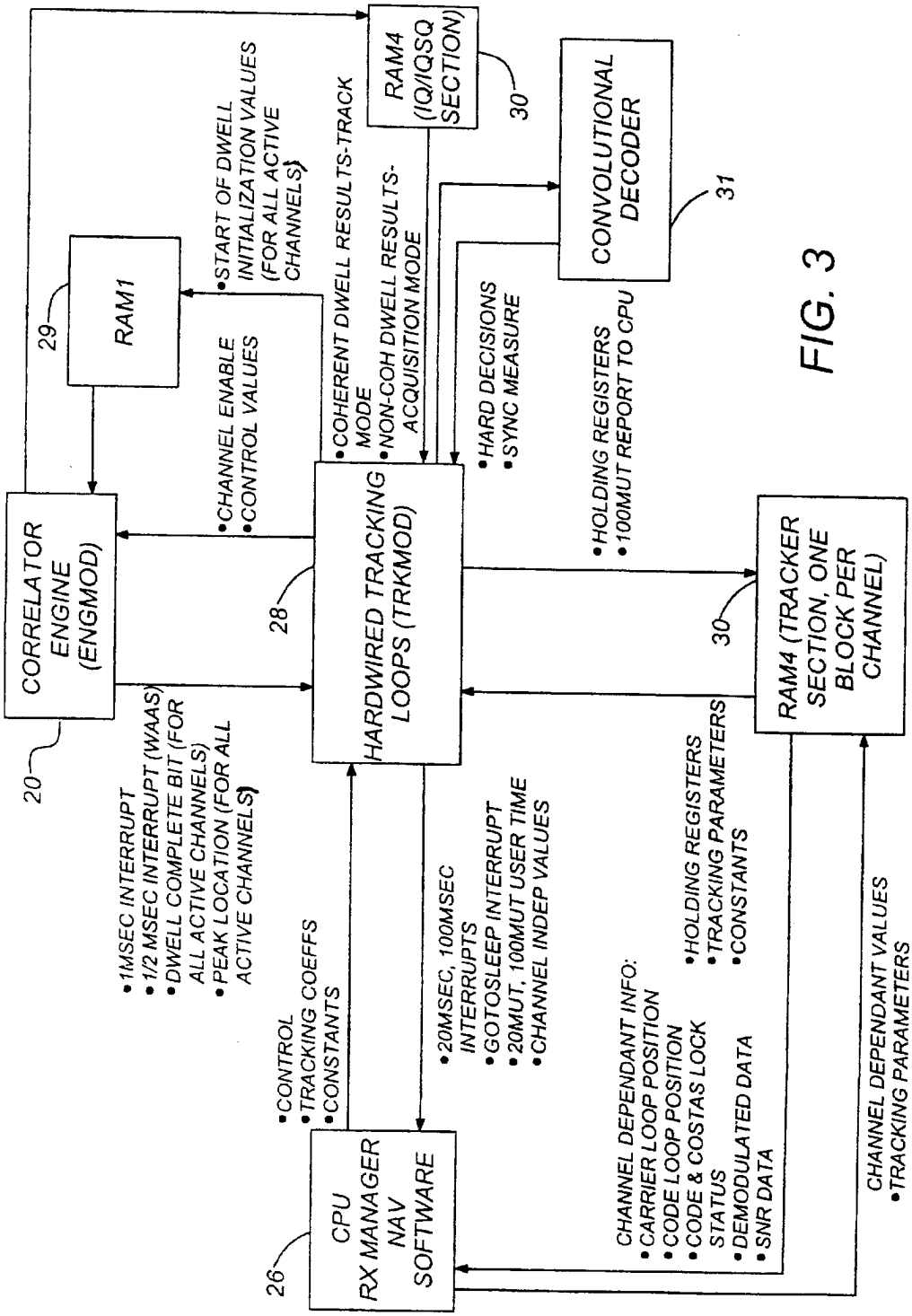

RAM4 (IQ/IQSQ SECTION)
30
CONVOLUTIONAL DECODER
31
RAM1
29
•START OF DWELL INITIALIZATION VALUES (FOR ALL ACTIVE CHANNELS)
•CHANNEL ENABLE •CONTROL VALUES
•COHERENT DWELL RESULTS-TRACK MODE
•NON-COH DWELL RESULTS-ACQUISITION MODE
•HARD DECISIONS •SYNC MEASURE
•HOLDING REGISTERS •100MUT REPORT TO CPU
CORRELATOR ENGINE (ENGMOD)
20
HARDWIRED TRACKING LOOPS (TRKMOD)
28
RAM4 (TRACKER SECTION, ONE BLOCK PER CHANNEL)
30
•1MSEC INTERRUPT •1/2 MSEC INTERRUPT (WAAS) •DWELL COMPLETE BIT (FOR ALL ACTIVE CHANNELS) •PEAK LOCATION (FOR ALL ACTIVE CHANNELS)
•CONTROL •TRACKING COEFFS •CONSTANTS
•20MSEC, 100MSEC INTERRUPTS •GOTOSLEEP INTERRUPT •20MUT, 100MUT USER TIME •CHANNEL INDEP VALUES
•HOLDING REGISTERS •TRACKING PARAMETERS •CONSTANTS
CHANNEL DEPENDANT INFO: •CARRIER LOOP POSITION •CODE LOOP POSITION •CODE & COSTAS LOCK STATUS •DEMODULATED DATA •SNR DATA
CHANNEL DEPENDANT VALUES •TRACKING PARAMETERS •CONSTANTS
CPU RX MANAGER NAV SOFTWARE
26

FIG. 3

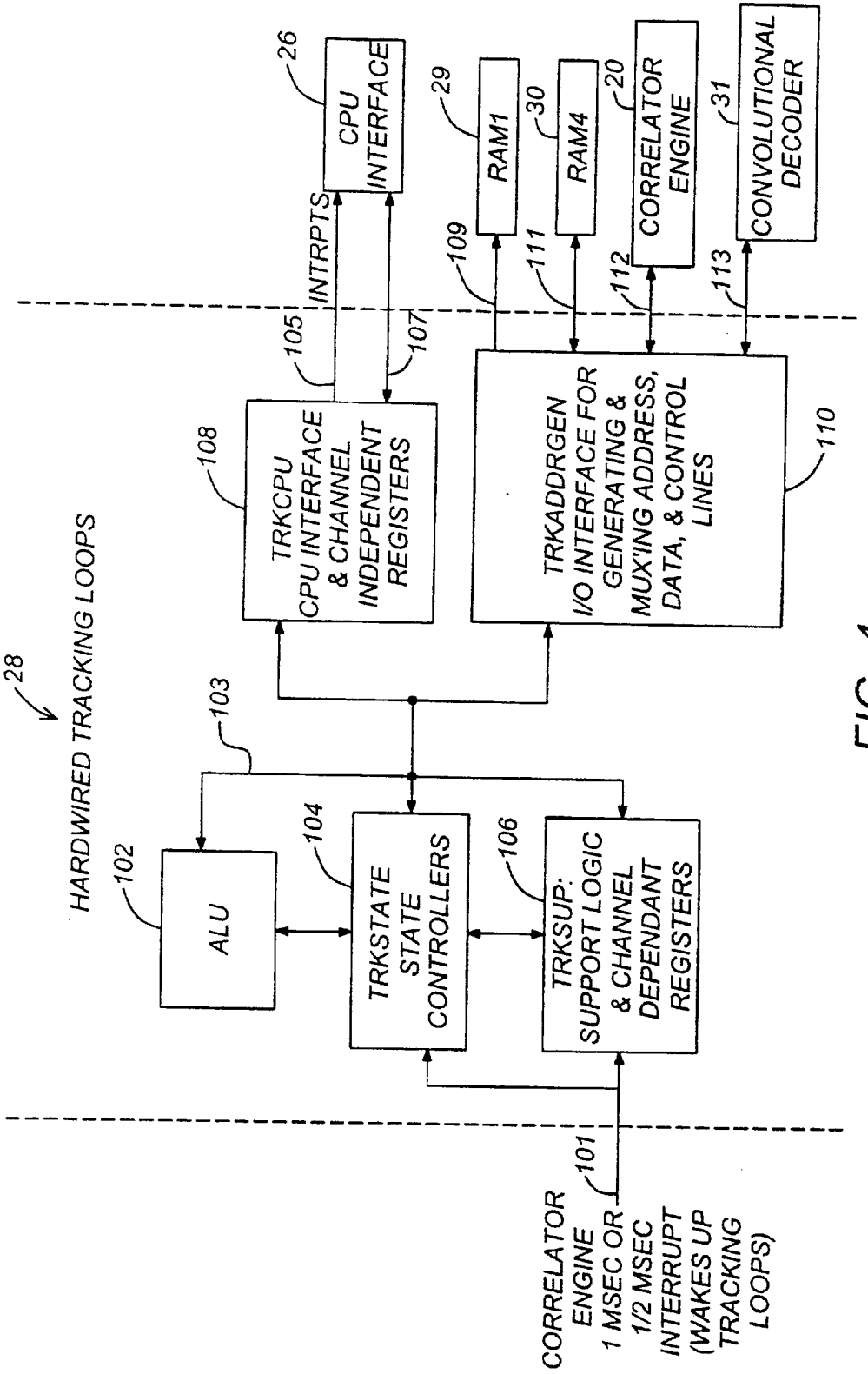

HARDWIRED TRACKING LOOPS
28
ALU
102
TRKSTATE STATE CONTROLLERS
104
TRKSUP: SUPPORT LOGIC & CHANNEL DEPENDANT REGISTERS
106
103
TRKCPU CPU INTERFACE & CHANNEL INDEPENDENT REGISTERS
108
TRKADDRGEN I/O INTERFACE FOR GENERATING & MUX'ING ADDRESS, DATA, & CONTROL LINES
110
CPU INTERFACE
26
INTRPTS
105
107
RAM1
29
RAM4
30
CORRELATOR ENGINE
20
CONVOLUTIONAL DECODER
31
109
111
112
113
CORRELATOR ENGINE 1 MSEC OR 1/2 MSEC INTERRUPT (WAKES UP TRACKING LOOPS)
101

FIG. 4

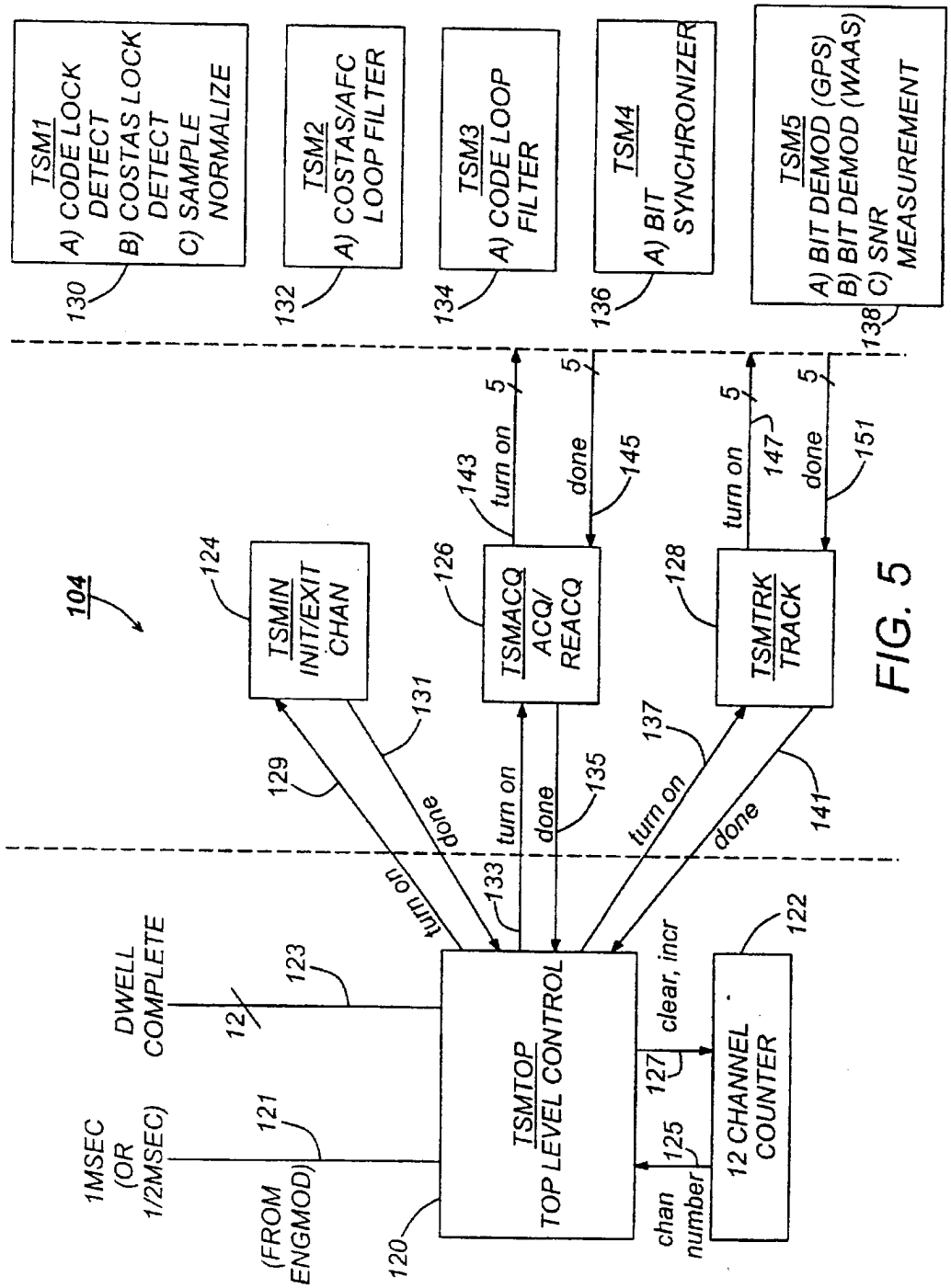

TSM1
A) CODE LOCK DETECT
B) COSTAS LOCK DETECT
C) SAMPLE NORMALIZE
130
TSM2
A) COSTAS/AFC LOOP FILTER
132
TSM3
A) CODE LOOP FILTER
134
TSM4
A) BIT SYNCHRONIZER
136
TSM5
A) BIT DEMOD (GPS)
B) BIT DEMOD (WAAS)
C) SNR MEASUREMENT
138
104
TSMIN
INIT/EXIT CHAN
124
TSMACQ
ACQ/ REACQ
126
TSMTRK
TRACK
128
TSMTOP
TOP LEVEL CONTROL
120
12 CHANNEL COUNTER
122
DWELL COMPLETE
123
12
1MSEC (OR 1/2MSEC)
121
(FROM ENGMOD)
chan number
125
clear, incr
127
turn on
done
129
131
133
135
137
141
143
145
147
151
5

FIG. 5

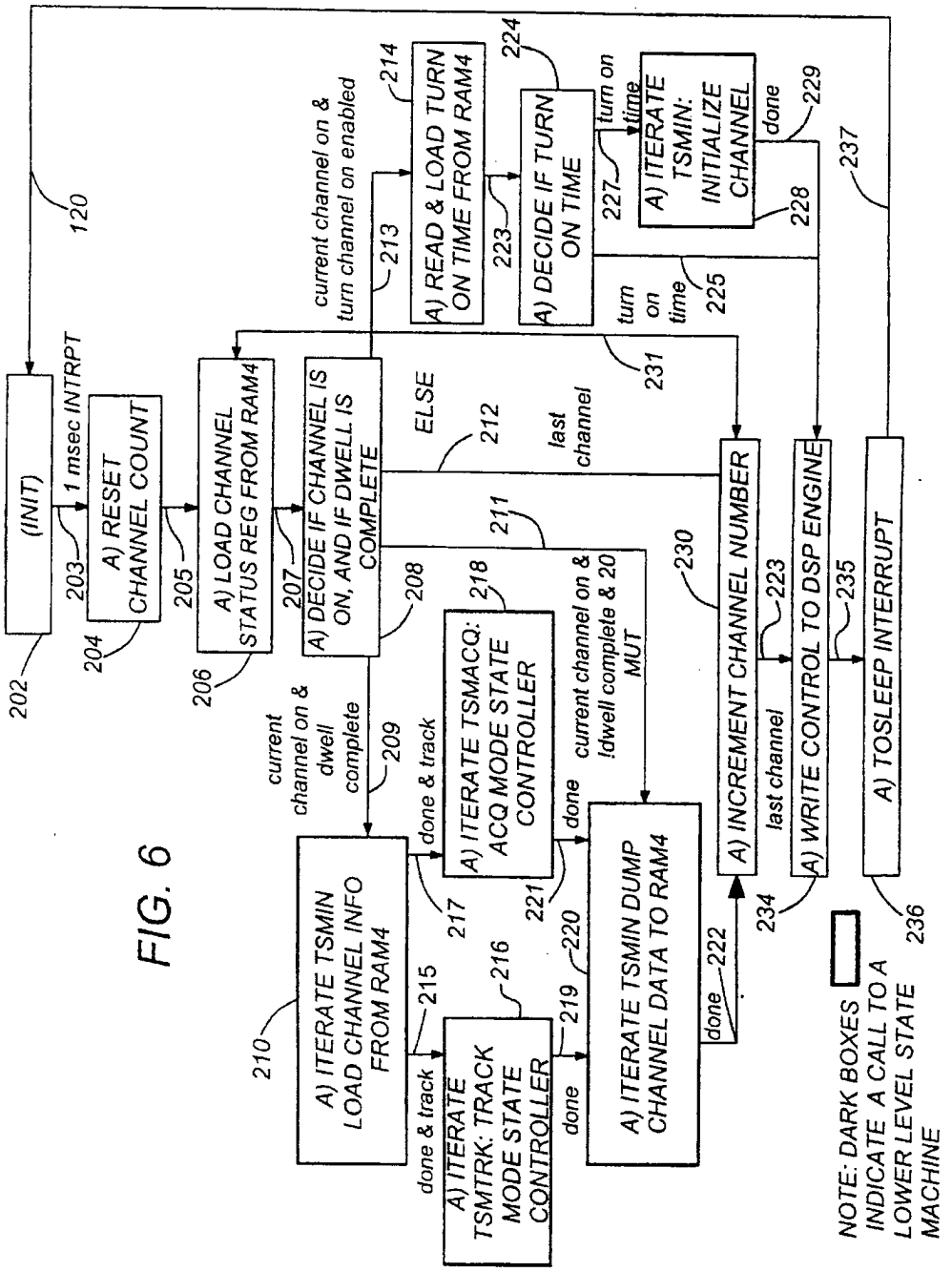

(INIT)
1 msec INTRPT
A) RESET CHANNEL COUNT
A) LOAD CHANNEL STATUS REG FROM RAM4
A) DECIDE IF CHANNEL IS ON, AND IF DWELL IS COMPLETE
ELSE
current channel on & turn channel on enabled
A) READ & LOAD TURN ON TIME FROM RAM4
A) DECIDE IF TURN ON TIME
turn on time
A) ITERATE TSMIN: INITIALIZE CHANNEL
done
last channel
A) INCREMENT CHANNEL NUMBER
A) WRITE CONTROL TO DSP ENGINE
A) TOSLEEP INTERRUPT
current channel on & dwell complete
done & track
A) ITERATE TSMIN LOAD CHANNEL INFO FROM RAM4
A) ITERATE TSMACQ: ACQ MODE STATE CONTROLLER
current channel on & !dwell complete & 20 MUT
A) ITERATE TSMTRK: TRACK MODE STATE CONTROLLER
A) ITERATE TSMIN DUMP CHANNEL DATA TO RAM4
NOTE: DARK BOXES INDICATE A CALL TO A LOWER LEVEL STATE MACHINE
120
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
222
223
224
225
227
228
229
230
231
234
235
236
237

FIG. 6

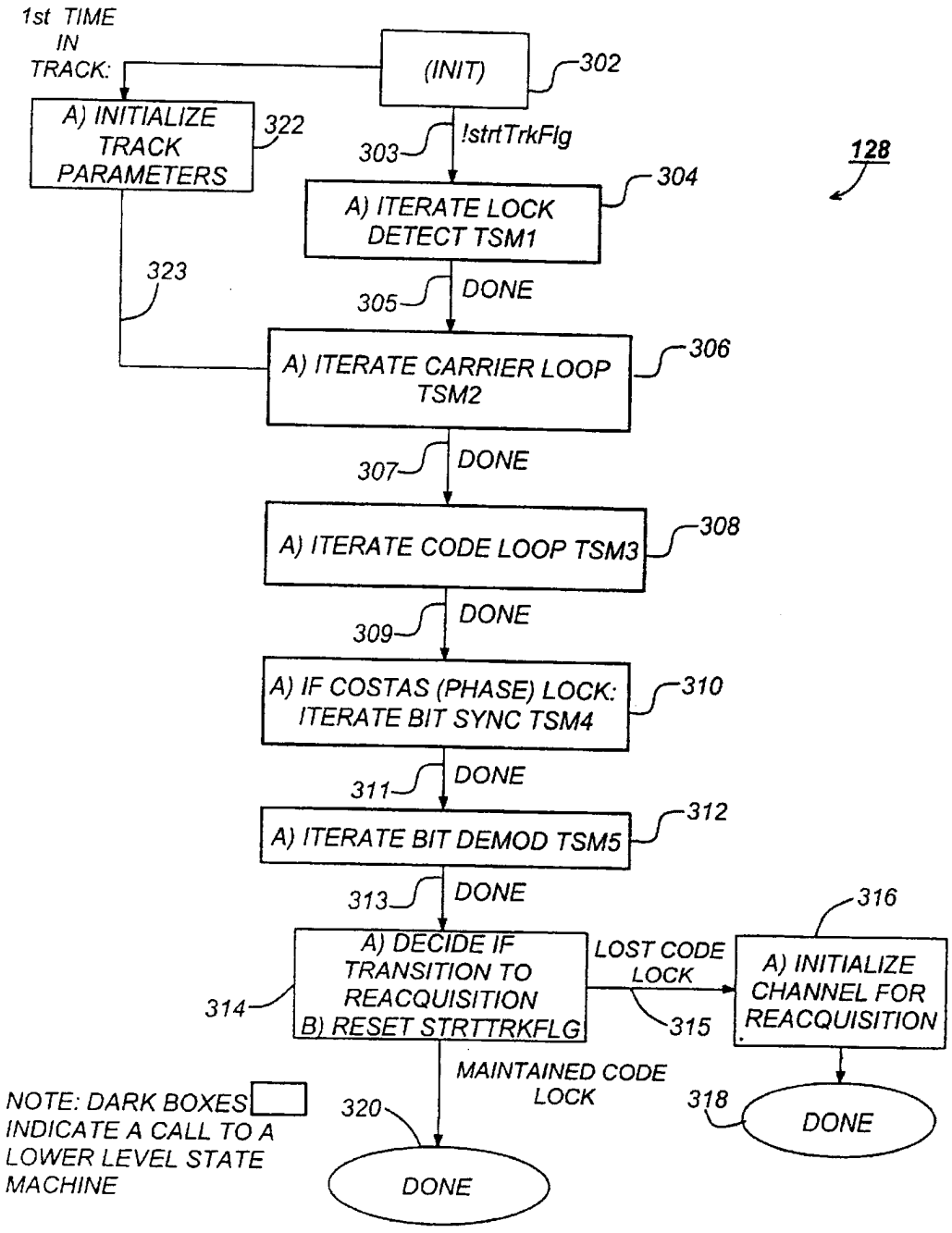

1st TIME IN TRACK:
(INIT)
302
A) INITIALIZE TRACK PARAMETERS
322
303
!strtTrkFlg
128
304
A) ITERATE LOCK DETECT TSM1
323
305
DONE
A) ITERATE CARRIER LOOP TSM2
306
307
DONE
A) ITERATE CODE LOOP TSM3
308
309
DONE
A) IF COSTAS (PHASE) LOCK: ITERATE BIT SYNC TSM4
310
311
DONE
A) ITERATE BIT DEMOD TSM5
312
313
DONE
316
A) DECIDE IF TRANSITION TO REACQUISITION
B) RESET STRTTRKFLG
314
LOST CODE LOCK
315
A) INITIALIZE CHANNEL FOR REACQUISITION
MAINTAINED CODE LOCK
318
DONE
320
DONE
NOTE: DARK BOXES INDICATE A CALL TO A LOWER LEVEL STATE MACHINE

FIG. 7

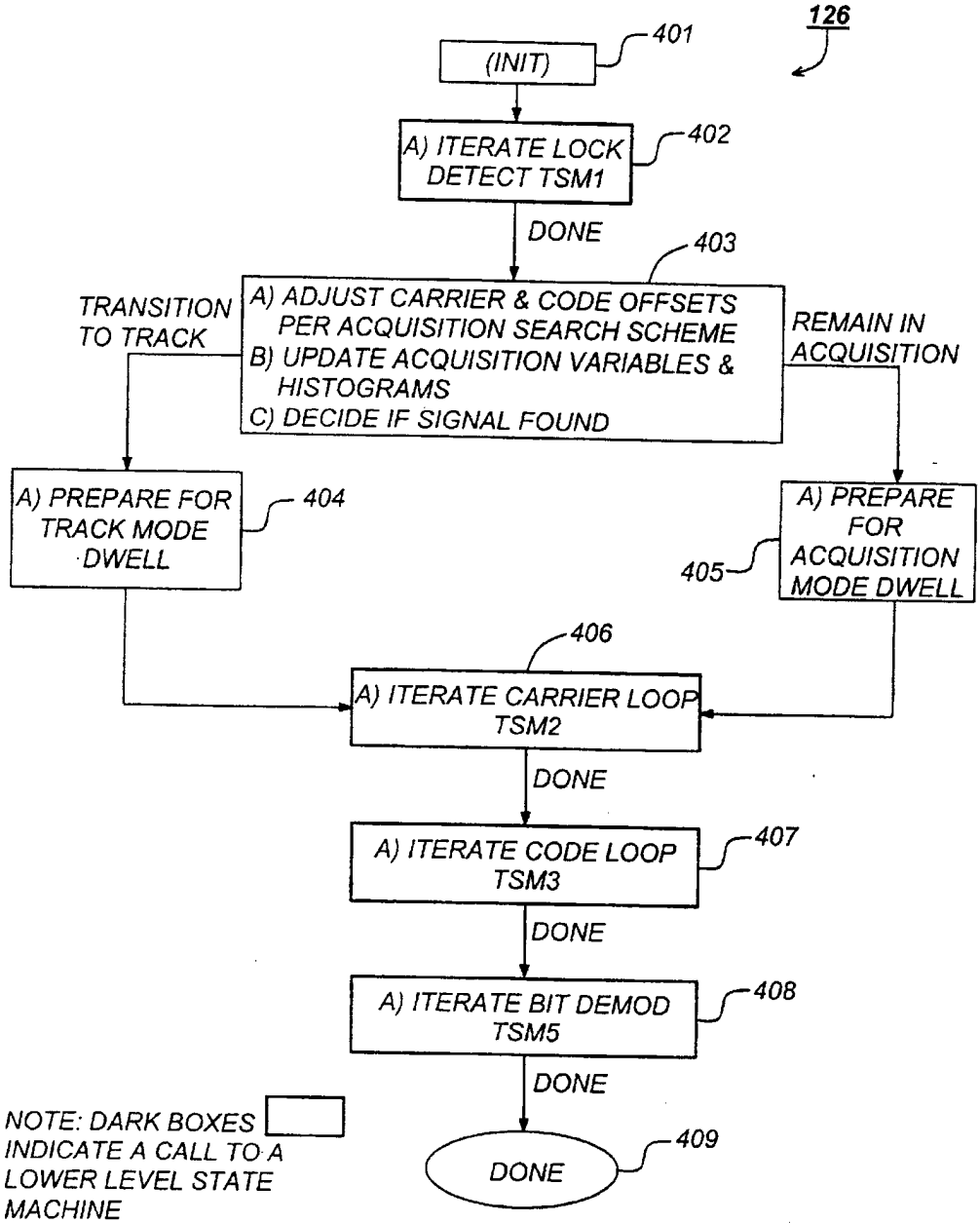

126
(INIT)
401
A) ITERATE LOCK DETECT TSM1
402
DONE
403
A) ADJUST CARRIER & CODE OFFSETS PER ACQUISITION SEARCH SCHEME
B) UPDATE ACQUISITION VARIABLES & HISTOGRAMS
C) DECIDE IF SIGNAL FOUND
TRANSITION TO TRACK
REMAIN IN ACQUISITION
A) PREPARE FOR TRACK MODE DWELL
404
A) PREPARE FOR ACQUISITION MODE DWELL
405
406
A) ITERATE CARRIER LOOP TSM2
DONE
A) ITERATE CODE LOOP TSM3
407
DONE
A) ITERATE BIT DEMOD TSM5
408
DONE
DONE
409
NOTE: DARK BOXES INDICATE A CALL TO A LOWER LEVEL STATE MACHINE

FIG. 8

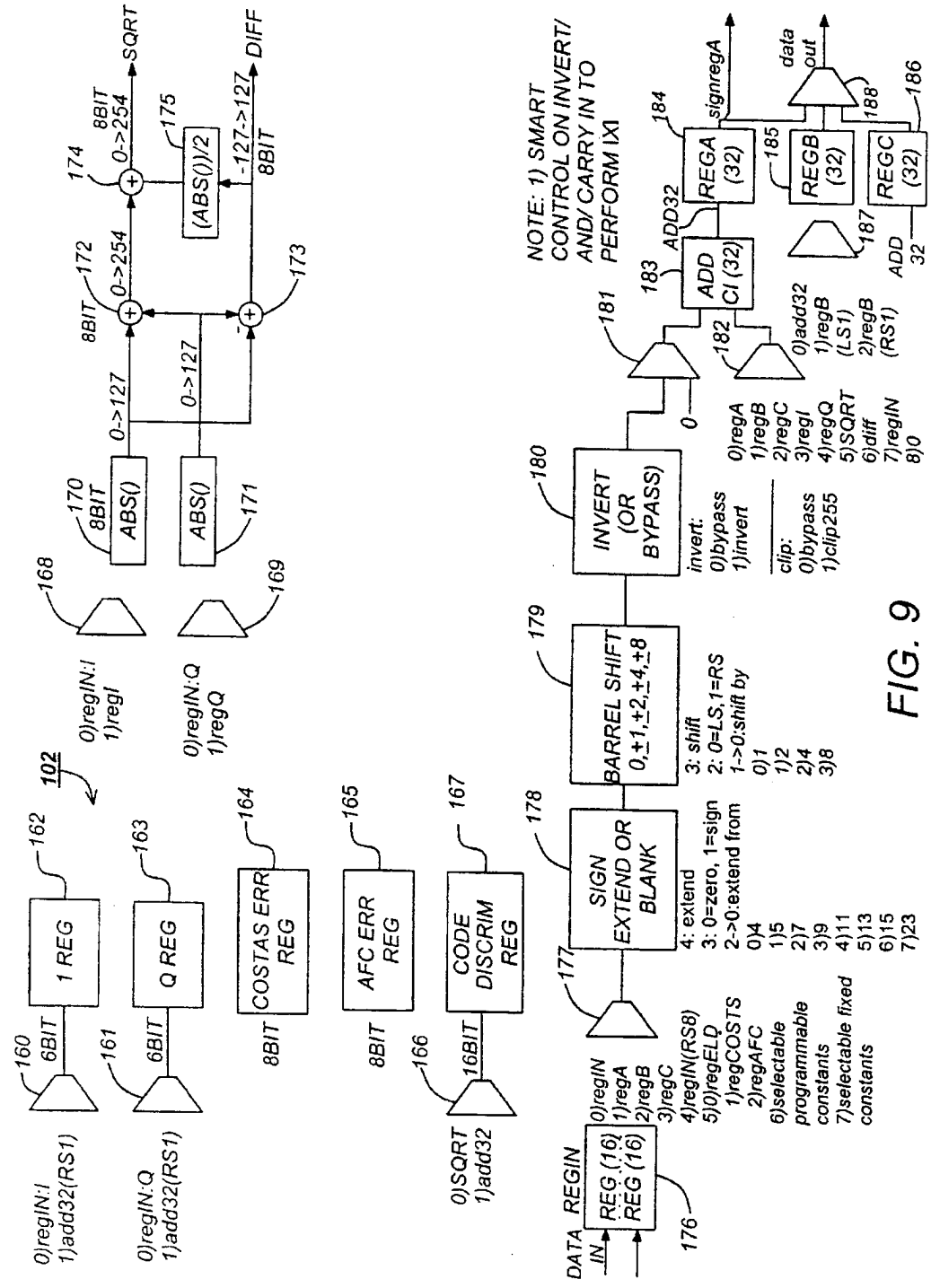

NOTE: 1) SMART CONTROL ON INVERT/ AND/ CARRY IN TO PERFORM IX1
DATA IN
REGIN
REG (16)
REG (16)
176
0)regIN
1)regA
2)regB
3)regC
4)regIN(RS8)
5)0)regELD
1)regCOSTS
2)regAFC
6)selectable programmable constants
7)selectable fixed constants
SIGN EXTEND OR BLANK
177
4: extend
3: 0=zero, 1=sign
2->0:extend from
0)4
1)5
2)7
3)9
4)11
5)13
6)15
7)23
178
BARREL SHIFT
0,+1,+2,+4,+8
179
3: shift
2: 0=LS,1=RS
1->0:shift by
0)1
1)2
2)4
3)8
INVERT (OR BYPASS)
180
invert:
0)bypass
1)invert
clip:
0)bypass
1)clip255
181
0
182
0)regA
1)regB
2)regC
3)regI
4)regQ
5)SQRT
6)diff
7)regIN
8)0
183
ADD CI (32)
ADD32
184
REGA (32)
signregA
185
REGB (32)
data out
187
0)add32
1)regB (LS1)
2)regB (RS1)
ADD 32
REGC (32)
188
186
168
169
170
8BIT
ABS()
171
0->127
0->254
172
8BIT
0->254
174
175
(ABS())/2
-127->127
8BIT
DIFF
SQRT
173
0->127
0)regIN:I
1)regI
0)regIN:Q
1)regQ
102
160
6BIT
1 REG
161
6BIT
Q REG
162
163
0)regIN:I
1)add32(RS1)
0)regIN:Q
1)add32(RS1)
164
COSTAS ERR REG
8BIT
165
AFC ERR REG
8BIT
166
16BIT
167
CODE DISCRIM REG
0)SQRT
1)add32

FIG. 9

AUTONOMOUS HARDWIRED TRACKING LOOP COPROCESSOR FOR GPS AND WAAS RECEIVER

CROSS REFERENCE TO RELATED APPLICATIONS

This is a continuation of application Ser. No. 09/397,438, filed Sep. 17, 1999, entitled "AUTONOMOUS HARDWIRED TRACKING LOOP COPROCESSOR FOR GPS AND WAAS RECEIVER", which application is incorporated herein by reference.

FIELD OF INVENTION

This invention relates to the field of GPS receivers.

BACKGROUND OF INVENTION

The Global Positioning System is a navigation system that can be used to provide a user with accurate position and time. It consists of a constellation of GPS satellites that broadcast the GPS signal, ground stations to control those satellites, and radio receivers such as shown in FIGS. **1A** and **1B** to capture the GPS signals and extract navigation information from them. Encoded on the transmissions of each satellite are messages that indicate the location of the satellite and time of transmission of the signal. By acquiring the signal of four satellites, and by performing calculations to determine the difference between the time of transmission and time of reception by the user equipment, a user can triangulate and determine latitude, longitude, elevation, and time. As illustrated in both prior art radio receiver implementations of FIGS. **1A** and **1B**, a typical GPS radio receiver comprises an antenna **12** up front to capture a GPS signal **13** broadcasted from a satellite. A RF front end **14** uses a reference oscillator **16** to down convert input RF signal **13** to an analog IF signal **15**. An analog to digital converter (A/D) 18 samples analog IF signal **15** and converts it into a digital IF output **19**. IF signal **19** then undergoes digital signal processing comprising essentially three levels of signal processing illustrated in Table 1 below.

TABLE 1

Receiver Functionality vs. Processing Rate Frequency

	FUNCTIONALITY		
	Signal Sampling & Correlation (i.e., correlation, replicating P or C/A code)	Receiver Processing (i.e., Tracking Loops, Bit Synchronization, Data Demod, etc.)	Navigation & Other Processing (i.e., Calculations of Position & Time, User Applications)
Processing Frequency	High rates (i.e., 50 MHz to 1 KHz)	Medium rates (i.e., 1 KHz to 10 Hz)	Low rates (i.e., 10 Hz and slower)
FIG. 1A Prior Art Scheme	ASIC (i.e., Correlator 20) performs process	CPU #1 (i.e., CPU 22) performs receiver processing, navigation & other processing (interrupted at medium rate)	
FIG. 1B Prior Art Scheme	ASIC (i.e., Correlator 20) performs process	CPU #1 (i.e., CPU 22) performs receiver processing (interrupt at medium rate)	CPU #2 (i.e., CPU 26) navigation & other processing (interrupt at low rate)

The three levels of signal processing can be quantified according to the functions and processing frequency expected at each stage of processing. A first stage consists of signal sampling and correlation processing that is (CPU) intensive and operates at very high frequency processing rate such as typically between 1 KHz to 50 MHz processing rate. This correlation processing stage comprises processing various steps that compare (or correlate) digitized signal **19** with a locally generated code that attempts to replicate the P or C/A code generated by a satellite. The replica code searches a "space" that consists of the unique codes generated by the different satellites, the temporal portion of the code being sent at any given time, and the Doppler frequency offset caused by the relative motion of the satellite and user. Generally, the Correlator Engine (such as) Correlator **20** of FIGS. **1A** and **1B**) performs parallel correlations with multiple code position/Doppler value combinations simultaneously in a multiple channel fashion, usually up to 12.

A second stage shown in Table 1, referred to as the receiver processing, typically comprises performing tracking loop function, bit synchronization, data demodulation, and other such typical signal processes running at a medium rate of 1 KHz to 10 Hz signal processing rate requirement. Finally, a third stage of signal processing illustrated in Table 1 comprises low frequency rate signal processing of 10 Hz or slower processes typically found in navigation processing, such as calculation of position and time.

As summarized in Table 1, typical prior art implementation of FIG. **1A** provides that the high rate signal sampling and correlation functions are performed by a Correlator ASIC **20**, while all other remaining medium to low level processing is performed by a receiver CPU **22**. This implementation presents a substantial drawback in that the receiver CPU **22** is overly burden with the still intensive processing requirements expected of the typical receiver processing function (i.e., 1 KHz to 10 Hz rate processing) that competes with the navigation processing and other non-GPS applications, including user applications. Moreover, as also summarized in Table 1, prior art implementation of FIG. **1B** of providing two CPUs (a receiver CPU **22** and a navigation process CPU **26**) to segregate and offload the medium frequency rate processes from the navigation CPU thus provides more time for that CPU to allocate to other non-GPS processing. However, prior art scheme of having a second CPU results in substantial increase to cost and silicon.

Accordingly, for typical radio receiver applications, either a more powerful CPU (with increased power consumption) needs to be used, or user desired software applications suffer from the microprocessor limited bandwidth to service both the correlator engine operations as well as the typical GPS receiver and navigational processing. There is therefore a dire need to off load the functions of the microprocessor in a GPS receiver system, while still servicing the needs of correlator engine operations and maintain the GPS receiver system performance.

SUMMARY OF INVENTION

An autonomous Hardwired Tracking Loop (HWTL) radio receiver comprising a CPU, a Correlator Engine (a "Correlator") and a Hardwired Tracking Loop ("HWTL") coprocessor is provided in accordance with the principles of this invention. The HWTL coprocessor provided in a HWTL integrated circuit executes acquisition and tracking procedures in radio receivers, such as a GPS and WAAS receiver that have traditionally been executed in software by the CPU. Accordingly, providing a HWTL coprocessor frees up the CPU to perform various other critical navigational and user desired applications, while minimizing the cost and real estate required. In the preferred embodiment, the Correlator

Engine, the HWTL coprocessor, and the CPU are all integrated on a single integrated circuit to minimize power consumption and lowers cost and also to relax the GPS receiver system's CPU requirements to allow the CPU more bandwidth to address user applications and lower CPU frequency intensive signal processing that are 10 Hz or less.

The receiver processing functions performed by the HWTL coprocessor include typical acquisition and tracking functions such as, for example, carrier loops, code loops, code lock detect, costas lock detect, bit synchronization, data demodulation, and SNR data gathering. The HWTL coprocessor implements the search processing for initial acquisition or reacquisition to track as well as controlling exit processing of track to reacquisition, as determined by CPU programmable parameters. The HWTL coprocessor can operate on a single channel in initial acquisition or on up to twelve channels in reacquisition or track. If the HWTL coprocessor is operating in reacquisition/track mode, then one of the channels may be a WAAS channel.

BRIEF DESCRIPTION OF DRAWINGS

FIG. **1A** is a block diagram illustrates a typical prior art GPS receiver.

FIG. **1B** is a block diagram illustrating another typical prior art GPS receiver.

FIG. **2** is a block diagram illustrating a radio receiver comprising an autonomous HWTL chip provided in accordance with the principles of this invention.

FIG. **3** is a block diagram describing a functional signal flow of the HWTL coprocessor of FIGS. **2** and **3**.

FIG. **4** is a more detailed block diagram describing the HWTL coprocessor of FIG. **2**.

FIG. **5** is a more detailed block diagram describing the HWTL State Controller (TRKSTATE) of FIG. **4**.

FIG. **6** is a more detailed block diagram describing the HWTL Top Level State Controller (TSMTOP) of FIG. **5**.

FIG. **7** is a more detailed block diagram describing the HWTL Track State Controller (TSMTRK) of FIG. **5**.

FIG. **8** is a more detailed block diagram describing the HWTL Acquisition Controller (TSMACQ) of FIG. **5**.

FIG. **9** is a more detailed block diagram describing the HWTL ALU of FIG. **4**.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT(S)

Structural Implementation

FIG. **2** illustrates an autonomous advanced digital signal processing chip ("HWTL chip") **100** provided in accordance with the principles of this invention. The term "HWTL chip" may also be referred to herein interchangeably with "HWTL ASIC" or "HWTL integrated circuit") HWTL chip **100** comprises in the preferred embodiment a digital Correlator Engine ("Correlator") **20**, a CPU **26**, and a HWTL coprocessor **28** operating under the direction of the on-board CPU **26**. Correlator Engine **20** receives an IF signal **19** and performs GPS signal processing including, such as: C/A code capture, Doppler rotation, correlation with a replica C/A code, coherent & noncoherent integration and an 8 bin frequency correlation. Table 2 illustrates one functional objective of the HWTL chip **100** provided in accordance with the principles of this invention

TABLE 2

Receiver Functionality vs. Processing Rate Frequency

	FUNCTIONALITY		
	Signal Sampling & Correlation (i.e., correlation, replicating P or C/A code)	Receiver Processing (i.e., Tracking Loops, Bit Synchronization, Data Demod, etc.)	Navigation & Other Processing (i.e., Calculations of Position & Time, User Applications)
Processing Frequency	High rates (i.e., 50 MHz to 1 KHz)	Medium rates (i.e., 1 KHz to 10 Hz)	Low rates (i.e., 10 Hz and slower)
HWTL ASIC 100 (FIG. 2)	HWTL Chip on-board Correlator Engine 20 (alternatively, external to HWTL ASIC)	HWTL chip on-board HWTL Coprocessor 28 (performs receiver processing)	HWTL chip on-board CPU 26 (performs navigation & other processing-alternatively, external to HWTL ASIC)

FIG. **3** illustrates the HWTL functional signal flow. Data is passed both directly and indirectly between navigation processing CPU **26**, HWTL coprocessor **28** and Correlator Engine **20**. Data is passed indirectly through the use of two on board storage devices, such as SRAM **29** and **30** (or RAM1 and RAM4, respectively.) RAM1 is used by Correlator Engine **20** as the first buffer of a double buffer scheme for track and acquisition dwell initialization parameters. RAM4 is a multipurpose RAM. Coherent and noncoherent accumulations are dumped to RAM4 by Correlator Engine **20**. HWTL coprocessor **28** uses RAM4 as a scratchpad to store channel specific registers and coefficients. This section of RAM4 is partitioned into channel address spaces of 128 words deep per channel.

Generally, CPU **26** directly programs HWTL coprocessor **28** with coefficients and values that are applicable to all channels (channel independent). Values that are specific to a channel (channel dependant) are programmed by CPU **26** into that channel's address space in RAM4.

HWTL Coprocessor 28 Top Level Block Diagram

FIG. **4** illustrates a top-level functional block diagram of HWTL coprocessor **28** of FIG. **2**. FIG. **5** illustrates a more detailed block diagram of HWTL coprocessor **28** which comprises five submodules: ALU **102**, TRKSTATE **104**, TRKSUP **106**, TRKCPU **108**, and TRKADDRGEN **110**.

Functional control of HWTL coprocessor **28** resides in the HWTL state controllers provided in TRKSTATE module **104**. Select and enable lines from TRKSTATE **104** allow registers in all remaining modules of HWTL coprocessor **28** to be updated, while controlling data flow between HWTL coprocessor **28**, Correlator engine **20**, RAM1 and RAM4.

TRKSTATE Module Operation

FIG. **5** illustrates a more detail block diagram of TRKSTATE **104** that provides all the control state machines of HWTL coprocessor **28**. As shown in FIG. **5**, the control state machines of HWTL coprocessor **28** are organized into three levels. The first and top level comprises TSMTOP **120**, which provides primary control and calls and passes control as needed to a second level of HWTL coprocessor state machines. The second level comprises TSMIN **124**, TSMACQ126, and TSMTRK128. These second level state machines call state machines from a third level, comprising TSM1 **130**, TSM2 **132**, TSM3 **134**, TSM4 **136**, and TSM5 **138**.

FIG. **6** illustrates a flow chart of the top-level state controller TSMTOP **120**. State machine TSMTOP **120** is activated every millisecond (or every ½ msec for a WAAS receiver application) via an interrupt signal from Correlator engine **20**. As detailed in the flow chart illustration of FIG. **6**, once initiated, state machine TSMTOP **120** then proceeds to cycle through twelve channels to determine if each channel is active or needs to be turned active (i.e.—has already been turned on, or needs to be turned on for the first time). Although twelve channels are used herein as an illustration, it is envisioned that in alternative embodiments, variation in the number of channel chosen is contemplated as within the scope of this invention. In cycling through the channels during execution of TSMTOP **120**, TSMTOP **120** state machine checks one by one whether each channel is already turned on or needs to be turned on. In order to turn on a channel the CPU programs in RAM4 a modulo 100 msec user time for TSMTOP **120** to turn on that channel. If that time matches the current 100 mut time (as determined by a modulo 100 millisecond user time counter in the TRKSUP**106** module), then the TSMIN state machine **124** is activated by TSMTOP **120** in an initialize channel mode to initialize that channel for the first time. On the other hand, if the channel has already been turned on and needs to be processed (because of a dwell completed from the Correlator Engine **20**), then TSMTOP **120** instead executes TSMIN **124** in setup HWTL channel mode to set up the HWTL coprocessor **28** to process that channel. This comprises primarily of loading channel specific values from RAM4 into HWTL coprocessor **28**. TSMTOP **120** then executes either TSMACQ **126** (if the channel is in initial acquisition or reacquisition mode) or TSMTRK **128** (if the channel is in track mode). After TSMACQ **126** or TSMTRK **128** completes its processing, TSMTOP**120** turns on TSMIN **124** once more, but this time in an exit sequence (or cleanup mode), to provide any needed clean up (including saving the 100 mut report in RAM4 if necessary) before proceeding to the next channel.

Thus, the TSMIN **124** state machine can be activated by TSMTOP **120** in one of three modes: initialize channel mode, set up HWTL hardware mode, or cleanup HWTL hardware mode. The initialize channel mode is used only when a channel is turned on for the first time. The set up HWTL hardware mode and cleanup HWTL hardware modes are used every time a channel is processed following a dwell complete from the Correlator engine for that channel, to load data from RAM4 into hardware at the start of channel processing and to store data back to RAM4 upon completing channel processing, respectively.

FIG. **7** shows the basic flow of the TSMTRK**128** track mode controller state machine, including the activation of third level state machines: TSM1 **130**, TSM2 **132**, TSM3 **134**, TSM4 **136**, and TSM5 **138**. These third level state machines perform much of the actual signal processing to acquire a signal, such as to lock on to it and extract data from it. TSM1 **130** is activated to perform a code lock detect. This operation analyzes the correlator outputs to determine if a signal level is present large enough relative to noise to indicate a true code being present. TSM1 **130** also performs a costas lock (phase lock) detect to determine if most of the signal power is consistently present mainly in the I (in phase) vs. Q (quadrature) component of the sampled signal. TSM2 **132** is activated to perform costas and AFC carrier loop functions. These are methods of using the sampled I and Q to dynamically track the "motion" of the carrier (L1) signal by matching to its phase and frequency variations. TSM3 **134** is activated to perform code loop functions. The code loop tracks the "motion" of the code modulated onto the carrier by determining and following the positions where the code transitions from high to low or low to high. TSM4 **136** is activated to perform bit synchronization. This is the process of determining where the 20 millisecond modulated data bits begin and end on the signal. This 20 millisecond data contains the satellite information for the CPU software to determine where the satellites are transmitting from. Finally TSM5 **138** is activated to perform data demodulation. This is the process of accumulating the sampled I signal for 20 milliseconds to determine if each 20 millisecond modulated data bit has a value of zero or one. TSM5 **138** also collects data for signal to noise ratio calculations.

FIG. **8** shows the basic flow of the TSMACQ **126** acquisition mode controller state machine used to perform initial acquisition and reacquisition. As described above for TSMTRK **128**, TSM1 **130** is turned on to perform the code lock detect. TSM2 **132** performs the carrier loops operations. TSM3 **134** performs the code loops operations. TSM5 **136** performs data demodulation and collects data for signal to noise ratio calculations. Actually, in acquisition TSM5 does not perform a true data demodulation since this is not possible until the signal has been locked on to in track, but it does collect information useful to software and maintains placeholders.

In addition to these basic third level state machine functions, the TSMACQ **126** state controller controls and steps the Correlator engine **20** through the code (time) and doppler (frequency) space to search for the presence of a GPS satellite signal. TSMACQ **126** is programmed by CPU **26** with parameters that determine the strategy of how to search for the signal and the criteria for determining that the signal is truly there. This includes repeating correlation in a particular code/doppler position once lock threshold is exceeded and comparing the peak value to neighboring peaks to decide which truly contains the signal. It also includes the strategy of how to proceed if a code/doppler position is rejected.

ALU Module Operations

FIG. **9** illustrates in more detail the ALU module **102** of FIG. **4** that performs much of the word wide (16 or 32 bit) data path calculations for the HWTL coprocessor's functions. ALU **102** is directed by control signals from TRKSTATE module **104** of FIG. **4** that selects data paths and enable registers. In this example, ALU **102** receives a 16-bit wide data from RAM4 and stores that data in a 32 bit wide input register REGIN **176**. ALU **102** then outputs results back to RAM4 **30** of FIG. **3**, which is also provided to state controller TRKSUP **106**, and to TRKADDRGEN **110** of FIG. **5**. In the preferred embodiment, the ALU **102** comprises three primary 32-bit storage registers: REGA **184**, REGB **185**, and REGC **186**. In addition, for convenience of operation, several smaller registers, i.e., I REG **162** and Q REG **163**, COSTAS ERR REG **164**, AFC ERR REG **165**, and CODE DISCRIM REG **167**, are provided to store values such as I & Q, costas error, AFC error and code discriminator to avoid shifting these values too many times back and forth from RAM4. ALU **102** accommodates input data in several forms and can sign or zero extended from several bit positions (as required to implement the signal processing). The data can right or left barrel shifted by 1, 2, 4 or 8 places. It can also be 1's or 2's complement inverted. Finally, selected data is then fed into a 32-bit adder **183** before being stored in REGA **184**, REGB **185**, or REGC **186**.

TRKSUP Module Operations

TRKSUP module **106** comprises of assorted circuit logic provided to support the signal processing, and acquisition

scheme, and maintain flags and mode registers (mostly channel specific that are accessed from RAM4, updated, and stored back in RAM4). TRKSUP **106** provides the following functionality for example and can be implemented in a number of various well known circuit designs that provide such functions:

1) User time counters to maintain 20 mut & 100 mut (one for all channels)
2) Channel time counter to maintain 20 mct (channel specific)
3) Code tap and frequency bin counters
4) Integrate and dump counter for code and costas lock
5) Jsync & Ksync flags (code & costas lock indicators)
6) Bit sync flag
7) Track mode flag
8) Shift register & counter to support shift & add multiplies
9) G1/G2 lookup support logic (The G1/G2 values are used to properly initialize the CA coders that generate the pseudo random code employed by GPS)
10) Sample normalizer up/down counter
11) Data demodulator shift register
12) Acquisition algorithm support logic (histogram bins, code & doppler step counters)

All these functions can be provided with discrete logic in the form of up counters, up/down counters, single bit register flags, multiple bit wide registers and shift registers. All of their functionality could have been performed by the ALU **102**, but they are used to provide storage on a channel by channel basis to mitigate the need of repeatedly reading and storing data in RAM4 while a single channel is being processed. They also provide more specialized capability since they are implemented with discrete logic rather than software.

TRKCPU Module Operations

The primary function of TRKCPU module **108** (see FIG. **4**) is to handle the interface between HWTL coprocessor **28** to CPU **26**. The functionality provided includes:

1) CPU interface
2) CPU programmable parameter storage registers (generally values that are non-channel specific, i.e.—one value applies to all twelve channels, so that is not necessary to take up twelve locations in RAM4)
3) Channel enabled registers—indicates which of the 12 available channels has been turned on. It provides the capability for a channel to be turned on at any time modulo 100 mut or turned off immediately
4) Override control—allows the CPU of override the autonomous algorithm of the tracker and force things such as: transition from track to reacquisition, the type of track to reacquisition transition, clearing and redetermination of bit sync, and transition to multipath.
5) Multiplexes from stored parameter values as determined by mode. This allows the CPU to provide a set of parameters up front and then the HWTL can decide which values to use.
6) Latches the data ready (dwell complete) interrupts from the Correlator engine.

TRKADDRGEN Module Operations

The primary operations of TRKADDRGEN module **110** (FIG. **4**) comprises generating control signals and addressing to access RAM1, RAM4, and Correlator engine **20**. TRKADDRGEN module **110**'s operations comprises:

1) Address and write strobe generation for RAM1—selects region of RAM1 to access as dictated by channel counter value.
2) Address and read/write request generation for RAM4—selects region of RAM4 to access as dictated by channel counter value and whether access is to the Correlator Engine **20** dumps, tracker channel scratchpad area, or G1/G2 lookup table area.
3) Address and write strobe generation for Correlator engine—selects region of Correlator engine address space to access as dictated by channel counter value.
4) Data out mux—multiplexes data from various sources (ALU, TRKSUP, etc) to send out to RAM1, RAM4, and the Correlator engine.
5) Channel counter—used by TSMTOP to cycle through the 12 channels to process successively any active channels.
6) Enable generator—produces a divide by 2 enable of the master clock to allow multiple cycles for long data path processing (primarily in the ALU). Most data paths and enabling of registers is gated with this enable, creating an effective data path time of approximately 40 nsec. In addition, accesses to RAM4 are controlled by a handshake acknowledge from RAM4 in response to a TRKMOD read/write request. If RAM4 does not immediately acknowledge, then wait states are implemented by delaying this enable signal.

Thus, in the preferred embodiment of HWTL coprocessor **28**, except for restricting Initial Acquisition to channel **0**, HWTL coprocessor **28** provides 12 independent tracking/reacquisition channels with the following capabilities:

(1) Initial Acquisition,
(2) Reacquisition,
(3) Carrier and Code loop tracking,
(4) Bit sync algorithm,
(5) Data demodulation, and
(6) 100 ms Status buffering

After a channel has been initialized, HWTL chip **100** autonomously searches for the programmed satellite, acquires carrier and code synchronization, performs bit synchronization, demodulates GPS data, and provides range data, SNR data, and lock/operational status at a 10 Hz interrupt rate. If the signal is lost, the Tracker automatically enters the Reacquisition State, repeatedly searching a programmed time/frequency uncertainty window until the signal is recovered or until software disables the channel and reprograms the search parameters and SVID.

Systems Level Description of HWTL Functionality

Typical tracking and acquisition operations of HWTL coprocessor are next described from a "systems" perspective, rather than the more "mechanical" implementation point of view utilized to this point.

Initial Acquisition Function Overview

As illustrated in FIG. **8**, in Initial Acquisition, Channel **0** searches the estimated time uncertainty at a fixed rate of 118 chips/non-coherent dwell and searches Doppler at ⅞ths of the 8 bin frequency window. The following search parameters are programmable:

1. Coherent dwell and non-coherent dwell,
2. Time search and type (swept or expanding),

3. Doppler search (swept or expanding),
4. False Alarm rate (sync threshold setting),
5. Start time delay (1 to 99 ms)
6. Number of searches before 'Acquisition Fail' status flag is set.

Initial Acquisition Search Algorithm

Initial Acquisition uses a histogram approach to synchronize Doppler and time to within ¼ of the frequency filter bandwidth and ¼ of a C/A code chip, respectively. After a non-coherent dwell, the Tracker reads the peak magnitude from the engine and compares it to a sync threshold. If the signal level does not break threshold, the Tracker waits for the next dwell that will cover the next 118-chip time slice. However, if the threshold is exceeded, the algorithm clears an 8-filter by 3-tap histogram centered in time at the peak tap, and initializes the peak tap/filter bin to a value of one. At subsequent dwells, if the peak exceeds threshold and lies within the histogram's 3×8 time-frequency window, the respective histogram bin is incremented while all others are decremented (minimum of zero). If the peak does not exceed threshold or exceeds threshold but is not in one of the 24 bins, all bins are decremented. When a bin reaches a programmable count of nominally 4 (except for any tap in frequency filter bin number **4**, which is automatically dismissed at a programmable count of nominally 4), the search algorithm proceeds to the verify cycle, whose purpose is to mitigate aliasing caused by high SNR signals. In the verify cycle, the carrier Doppler is slewed so that Bin **0**, or the DC bin, is centered on the signal. If the signal is an alias, bin **0** will be centered near a sin(x)/x sampling null, and will not be verified. The Tracker switches to track-mode if the signal is verified a programmable number of times. If after searching the time/frequency window the programmed SVID is not detected, the search algorithm sets the 'Acquisition Fail' status flag.

Reacquisition Overview

There are two reacquisition modes: (1) 'normal' and (2) 'resume'. In a 'normal' reacquisition, the Tracker always begins its search relative to its current carrier loop Doppler estimate and code loop phase estimate. The Tracker selects the normal mode only if bit sync has been completed; otherwise, the 'resume' mode is selected. The 'resume' mode is implemented to mitigate false detects. Thus, when a channel falls out of track mode because it has locked to a frequency or code sidelobe, it will use as its reference point the Doppler and code phase saved from the last reacquisition search step, i.e., it will resume its search as if it had just dismissed the last dwell position.

The core reacquisition algorithm is the same for both modes. The Tracker searches time in fixed 10 chip steps, and although the carrier Doppler step size is programmable, 750 Hz is the baseline step size. As with initial acquisition, the number of Doppler and code steps, the false alarm rate, dwell period, and search type (expanding or swept) are programmable. Except for reducing the histogram from 24 tap/filter bins to 3 taps, the reacquisition algorithm is identical to the initial acquisition histogram search. On the first detection, the histogram is centered and the center bin is set to 1 and the neighboring tap bins are zeroed. Subsequent sync detects increment the respective bin and decrement the other two until the peak bin reaches the programmed threshold count (baseline is 4 for P_{FA}=0.1) or all three bins decrement to zero. If the peak reaches the threshold count, the coder is slewed to move the peak tap over to the punctual pull-in tap, tap **0**, and the Tracker switches to track mode. If all three bins decrement to zero, the code phase is stepped 10 chips and the procedure continues.

Tracking Function Overview

FIG. **7** illustrates an example of the tracking process of HWTL coprocessor function of track mode provided by Track State Controller (TSMTRK) **128**. While in the track mode, TSMTRK **128** (or also referred herein as "the Tracker") uses a composite AFC/Costas carrier tracking loop to acquire and maintain carrier phase synchronization, and a first order code loop with frequency aiding from the carrier loop to maintain code phase or time synchronization. The coherent dwell or iteration period is fixed at 1 ms, but the following parameters are programmable:

1. AFC loop bandwidth, either 1^{st} or 2^{nd} order, and can be disabled if Costas locked,
2. Costas loop bandwidth and either 2^{nd} or 3^{rd} order, Code loop bandwidth, and either conventional ½ chip Early-Late (E–L), narrow E–L, or multipath discriminators.

Support Functions

In addition to the AFC/Costas Carrier loop and Code loop, the hardwired tracker performs several functions in order to determine when to transition between acquisition and track, determine bit sync, and extract demodulated data. These include the Code and Costas Lock Detectors, Bit Synchronizer, and Data Demodulator.

Code and Costas Lock Detectors

Code lock and Costas lock detectors with 100 ms update intervals are provided. At the end of a 100 ms integrate and dump period, the code lock (or signal lock detector) compares to a sync threshold the quotient of the mean signal envelope divided by the mean signal plus noise envelope, and if the quotient exceeds threshold, the 'Code Lock' status bit is set in the 100 ms status report and an 'unlocked' status counter is cleared. If the quotient is less than the threshold, the 'unlocked' status counter is incremented. If the counter ever reaches its programmed threshold, the Tracker will exit to reacquisition mode. This 'unlock' status counter is incorporated to delay entry into the reacquisition cycle until there is a very high probability that the signal has been lost. The Costas lock detector compares the mean $|I|-|Q|$ value to a sync threshold. The averaging (integration) time is 100 ms.

Bit Synchronization

After achieving Costas lock, 1 ms I samples are filtered by a 20-tap moving-window filter and the absolute value of the filter is applied to one of 20 bins of a histogram. The bin address to which the filter is added is equal to the state of the modulo-20 20 ms user time counter. After approximately 40 bits, the magnitude of the peak histogram bin and its two neighboring bins are used to compute the location of the bit edge relative to the state of the modulo-20 20 ms user time counter. For example, if the neighboring bin that is later in time than the peak bin is larger than the early bin, the edge resides somewhere in the late bin's 1 ms coherent integration interval. Conversely, if the early bin is larger than the late bin, the edge resides in the peak bin's 1 ms coherent integration interval. When the early and late bin magnitudes are comparable to each other, noise can introduce a 1 ms error because the bit edge is either very late in the peak bin's 1 ms integration period or very early in the late bin's 1 ms period. For these cases, the code chip number is used to decide the correct bin: if the chip number is very small, the bit edge occurs late in a 1 ms period, so the edge must reside in the peak bin; if the chip number is very large, the bit edge occurs early in a 1 ms period, and therefore, the edge must reside in the late bin.

Data Demodulation

After bit sync, de-normalized I and Q samples are accumulated over 20 ms. At 20 ms channel time, (1) the absolute

values of the accumulators are accumulated, (2) the sign bit of the I accumulator is shifted into the channel's data buffer, (3) the 20 ms 'badlock' and 'badphase' status bits are shifted into their respective status buffer, (4) the No (noise-floor) 20 ms accumulator is absolute-valued and accumulated, and (5) the I, Q, and No accumulators are then dumped.

100 ms Status Reports

At every 100 ms interrupt, each channel writes the following data items to a RAM4 buffer as a 100 ms CPU report:

(1) 4, 5, or 6 GPS hard decision data bits (5 nominal), (this is the 20 millisecond demodulated data)

(2) Modulo-20 20 ms channel time at 100 ms user time epoch,

(3) Modulo-1023 PN chip number at 100 ms user time epoch,

(4) 16-bit Code phase at 100 ms user time epoch,

(5) 32-bit Carrier delta-phase over last 100 ms,

(6) 32-bit Carrier Doppler estimate (2.046 MHz/2^{32}),

(7) |I| and |Q| Accumulation (for 4, 5, or 6 bits),

(8) |No| Accumulation (for 4, 5, or 6 bits),

(9) 'Badlock' status, 1 per 20 ms bit,

(10) 'Badphase' status, 1 per 20 ms bit,

(11) Track/Acq status, Code lock status, Costas lock status, Bitsync status

WAAS Processing

One channel of the hardwired tracking loop can act as WAAS receiver channel. Processing of the WAAS channel is similar to processing of GPS channels with the following differences. The WAAS channel is iterated at a ½ msec rate so that carrier and code loops and the code and costas lock detectors are iterated every ½ msec. The ½ msec coherent dwell resolution allows the 2 millisecond WAAS soft symbols to be divided into four bins for bit synchronization and data demodulation. Further, two symbol pair soft decisions are fed into a convolutional decoder to obtain hard decision data bits at a 4 msec rate. First, one pairing of soft symbols into the convolutional decoder is attempted and if the resultant sync measure is too large, then the other pairing is tried until hard decision bit sync is obtained.

The 100 mut status report for the WAAS channel will contain 24, 25 or 26 hard decision bits saved up from the past 100 milliseconds, as well as a corresponding number of I, Q and noise accumulations. If the WAAS channel is enables then the entire hardwired tracking loop and engine operates in ½ millisecond mode. This means that all coherent dwells (except for initial acquisition) can be programmed in increments of ½ milliseconds. This results in performance advantages for reacquisition.

CPU Oversight

The CPU is required to program the HWTL with initial values as to the search and tracking parameters for desired satellite channels. Thereafter, the CPU collects GPS data and phase information at a 100 millisecond rate to perform navigation functions. The CPU can also disable (ignore) the 100 millisecond interrupts from the HWTL for extensive periods of time (on the order of several seconds) while the HWTL continues its acquisition and tracking functions without CPU supervision. Thus, when the CPU re-enables the HWTL coprocessor's 100 millisecond interrupt it returns to channels that have been continuously tracking and can make position estimates almost immediately from code position.

Thus, the HWTL integrated circuit comprising a HWTL coprocessor provided in accordance with the principles of this invention provides a lower cost, lower real estate implementation of a radio receiver. Providing a HWTL coprocessor allows the CPU in the radio receiver to allocate more processing bandwidth for lower frequency rate operations such as navigation and user applications that are in the range of lower than 10 Hz, while offloading the higher frequency signal processing to the HWTL coprocessor and the Correlator engine. The radio receiver architecture in accordance with the principles of this invention thus addresses the need to minimize power consumption in the typical radio receivers to thereby better accommodate the industry trend to embed radio receivers in small, portable consumer devices.

Although in the preferred embodiment, Correlator **20**, CPU **26** and HWTL coprocessor **28** are integrated on a single ASIC, it is contemplated that either or both CPU **26** and Correlator **20** can conceivably be implemented external to HWTL chip **100**. Moreover it is understood that although, in this described example, we often referred to the implementation of the HWTL coprocessor as for either a GPS or WAAS radio receiver, it is contemplated as within the scope of this invention that the principle of a HWTL coprocessor in a radio receiver is applicable to a variety of radio receiver applications in addition to GPS and WAAS applications.

Foregoing described embodiments of the invention are provided as illustrations and descriptions. They are not intended to limit the invention to precise form described. In particular, Applicant(s) contemplate that functional implementation of invention described herein may be implemented equivalently in hardware, software, firmware, and/or other available functional components or building blocks. Other variations and embodiments are possible in light of above teachings, and it is thus intended that the scope of invention not be limited by this Detailed Description, but rather by claims following.

What is claimed is:

1. An autonomous hardwired tracking loop (HWTL) integrated circuit comprising:

a HWTL coprocessor coupled to receive an IF signal from a correlator engine, the HWTL coprocessor providing radio signal processing comprising data tracking or acquisition processing on the IF signal to generate HWTL processed data for further radio receiver processing operations by a CPU.

2. The HWTL integrated circuit of claim **1**, wherein the HWTL integrated circuit is coupled to the CPU to provide the HWTL processed data to the CPU, wherein the CPU provides navigation and other non-radio receiver processing.

3. The HWTL integrated circuit of claim **1**, wherein the HWTL coprocessor provides signal processing operations in a range from approximately 10 Hz to 1 KHz processing rate.

4. The HWTL integrated circuit of claim **1**, wherein the HWTL coprocessor comprises:

a track state module (TRKSTATE) that initiates a set of state machine operations, and also provides a plurality of functional control signals of the HWTL coprocessor comprising one or more select and enable lines; and

an ALU coupled to the TRKSTATE module to receive the one or more select and enable signal to provide a plurality of data path calculations for tracking, the ALU is also coupled to the one or more on-board memory components for retrieving and storing a set of processed data;

a track support module (TRKSUP) comprising a set of assorted logic for supporting signal processing and acquisition operations;

a track CPU module (TRKCPU) for handling interface to the CPU via a bus; and

a track address generator (TRKADDRGEN) for generating one or more control lines and addresses for accessing the one or more on-board memory components and the Correlator engine.

5. The HWTL integrated circuit of claim **1**, wherein the HWTL coprocessor acquires, tracks and demodulates WAAS data.

6. The HWTL integrated circuit of claim **1**, wherein the HWTL coprocessor provides a half millisecond mode operation of the hardwired tracking loop to support WAAS bitsync and data demodulation and to support reacquisition ½ millisecond coherent dwells.

7. An autonomous hardwired tracking loop (HWTL) radio receiver system comprising:

a correlator engine, the correlator engine receives an IF signal and provides correlation operations to generate a correlated data output;

a CPU; and

a HWTL coprocessor coupled between the correlator engine and the CPU to direct passage of data via one or more on-board memory components to the correlator engine or the CPU, wherein the one or more on-board memory components comprises storing a set of parameters associated with data tracking and acquisition operations.

8. The HWTL radio receiver of claim **7**, wherein the HWTL coprocessor is integrated on an integrated circuit.

9. The HWTL radio receiver of claim **7**, wherein the HWTL coprocessor and the CPU is integrated on a single integrated circuit.

10. The HWTL radio receiver of claim **7**, wherein the HWTL coprocessor, the CPU and the correlator comprises an integrated circuit.

11. The HWTL integrated circuit of claim **7**, wherein the HWTL coprocessor comprises:

a track state module (TRKSTATE) that initiates a set of state machine operations, and also provides a plurality of functional control signals of the HWTL coprocessor comprising one or more select and enable lines; and

an ALU coupled to the TRKSTATE module to receive the one or more select and enable signal to provide a plurality of data path calculations for tracking, the ALU is also coupled to the one or more on-board memory components for retrieving and storing a set of processed data;

a track support module (TRKSUP) comprising a set of assorted logic for supporting signal processing and acquisition operations;

a track CPU module (TRKCPU) for handling interface to the CPU via a bus; and a track address generator (TRKADDRGEN) for generating one or more control lines and addresses for accessing the one or more on-board memory components and the Correlator engine.

12. The HWTL radio receiver of claim **7**, wherein the HWTL coprocessor acquires, tracks and demodulates WAAS data.

13. The HWTL radio receiver of claim **7**, wherein the HWTL coprocessor is coupled to the CPU to provide the HWTL processed data to the CPU, wherein the CPU provides navigation and other non-radio receiver processing.

14. The HWTL radio receiver of claim **7**, wherein the HWTL coprocessor provides signal processing operations in a range from approximately 10 Hz to 1 KHz processing rate.

15. An autonomous hardwired tracking loop method (HWTL method) for a radio receiver system having a correlator, a CPU, and a HWTL coprocessor, wherein the HWTL method comprises:

providing signal processing functions requiring greater than 1 KHz frequency rate by the correlator;

providing receiver processing comprising data acquisition and tracking function processing by the HWTL coprocessor; and

providing navigation and non-radio receiver operations by the CPU.

16. The HWTL method of claim **15** wherein the receiver processing comprises signal processing operations at a frequency in a range between approximately 1 KHz to 10 Hz.

17. The HWTL method of claim **15** wherein the CPU navigation and non-radio receiver operations comprises signal processing operations at a less than approximately 10 Hz processing requirements.

18. An apparatus for acquiring and tracking signals received from a plurality of GPS transmitters, comprising:

an engine for correlating the signals received from the plurality of GPS transmitters; and

a subsystem communicatively coupled to the engine, the subsystem configured to acquired and track the correlated signals, the subsystem including:

a subsystem processor, implementing at least one software module that acquires and track the correlated signals according to instructions stored in a memory communicatively coupled to the processor, wherein the instructions include at least one operation implemented in a circuit module.

19. The apparatus of claim **18**, wherein the engine correlates the signals received from the plurality of GPS transmitters according to a code position and a doppler value.

20. The apparatus of claim **18**, wherein the subsystem is disposed on a single integrated circuit chip.

21. The apparatus of claim **18**, wherein the subsystem and the engine are disposed on a single integrated circuit chip.

22. The apparatus of claim **18**, wherein the circuit module comprises discreet logic implementing the operations supporting the software modules.

23. The apparatus of claim **18**, wherein the circuit module includes memory storage independent of the memory communicatively coupled to the subsystem processor.

24. The apparatus of claim **18**, wherein the operations include at least one operation for accessing, updating, and storing data in a counter selected from the group comprising:

a time counter shared by all of a plurality of channels;

a channel specific time counter for each of the plurality of channels;

a code tap counter;

a frequency bin counter;

an integrated counter;

a dump counter;

a shift register and counter;

an up/down counter;

a code step counter; and

a doppler step counter.

25. The apparatus of claim **18**, wherein the operations include at least one operation for accessing, updating, or storing data in stored in a data demodulator shift register.

26. The apparatus of claim **18**, wherein the operations include at least one operation for accessing, updating, or storing data in stored in a plurality of histogram bins.

27. The apparatus of claim **18**, wherein the operations include at least one operation for setting and resetting a flag selected from the group comprising:

a bit synchronization flag; and

a track mode flag.

28. The apparatus of claim **18**, wherein the operations include at least one operation for accessing an indicator selected from the group comprising:

a code lock indicator; and

a costas lock indicator.

29. The apparatus of claim **18**, further comprising a navigation processor.

30. The apparatus of claim **29**, wherein the navigation processor and the engine are implemented in the same integrated circuit.

31. The apparatus of claim **30**, wherein the navigation processor, the subsystem processor and the engine are implemented in the same integrated circuit.

32. The apparatus of claim **18**, wherein the subsystem processor implements a plurality of hierarchically organized software modules, including:

a first software module, communicatively coupled to the engine;

a first set of software modules, each of the software modules operating under control of the first software module.

33. The apparatus of claim **32**, wherein the first software module is activated by the engine.

34. The apparatus of claim **33**, wherein the first software module is activated by an interrupt signal from the engine.

35. The apparatus of claim **32**, wherein the first set of software modules includes:

an acquisition software module for acquiring and reacquiring the signals received from the plurality of GPS transmitters;

a tracking software module for tracking the signals received from the plurality of GPS transmitters.

36. The apparatus of claim **35**, wherein the first set of software modules further comprises an initialization software module for initializing the first software module and the second software module.

* * * * *

Exhibit C

US006519466B2

(12) **United States Patent**
Pande et al.

(10) **Patent No.: US 6,519,466 B2**
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(54) **MULTI-MODE GLOBAL POSITIONING SYSTEM FOR USE WITH WIRELESS NETWORKS**

(75) Inventors: **Ashutosh Pande**, Milpitas, CA (US); **Lionel Jacques Garin**, Palo Alto, CA (US); **Kanwar Chadha**, Los Gatos, CA (US); **Gregory Bret Turetzky**, San Jose, CA (US)

(73) Assignee: **Sirf Technology, Inc.**, San Jose, CA (US)

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Primary Examiner—Edward F. Urban
Assistant Examiner—Erika A Gary
(74) *Attorney, Agent, or Firm*—Hogan & Hartson, LLP

(57) **ABSTRACT**

The present invention discloses a GPS system that can operate in different modes depending on the network facilities and bandwidth available, the GPS information that can be acquired, or user or system requirements. The modes comprise standalone mode, where a mobile communications device computes the position of the device, an autonomous mode, where the mobile communications device transmits the computed position to a server, application, or PSAP in a communications network, a network aided mode, where the network aides the mobile communications device in determining the position of the device, a network based mode, and other modes.

20 Claims, 6 Drawing Sheets