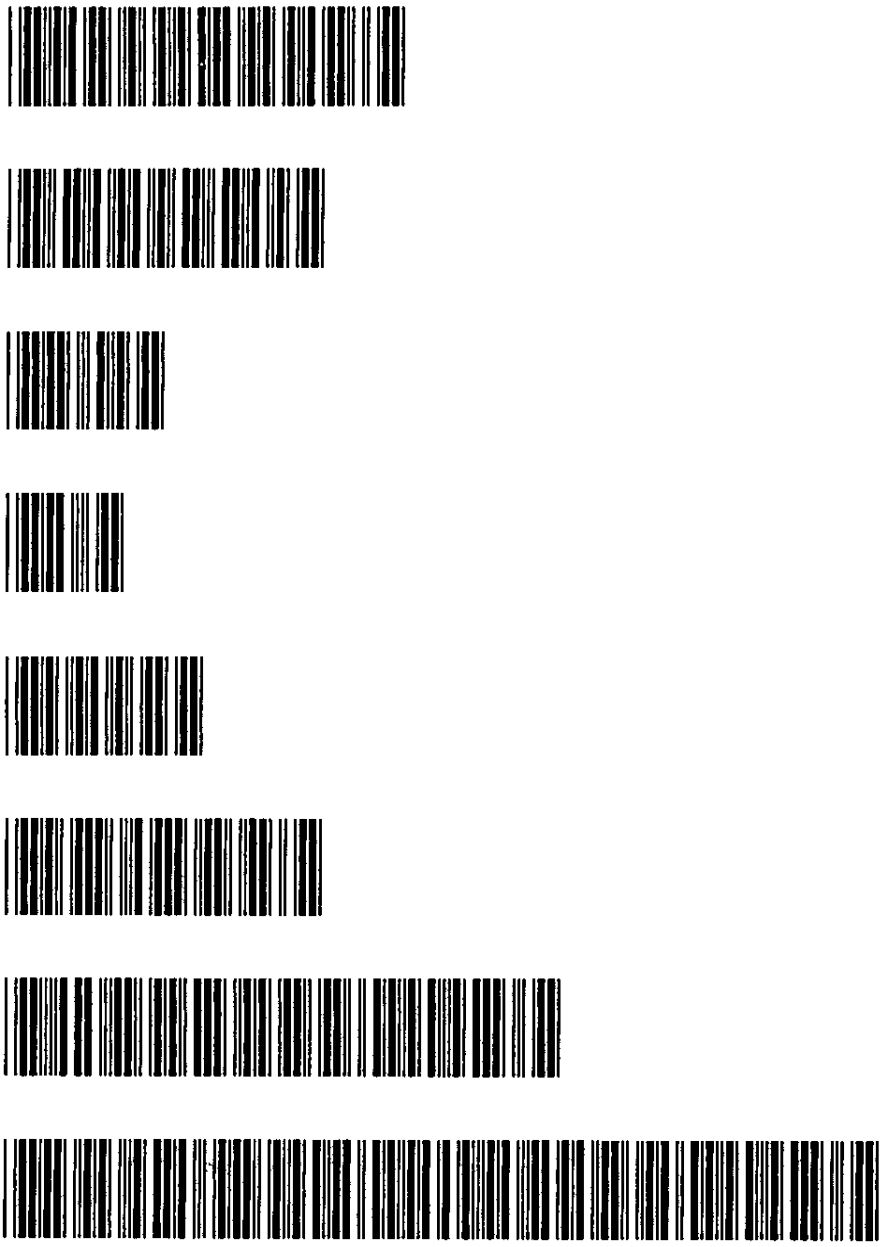

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UNITED STATES DISTRICT COURT

SOUTHERN DISTRICT OF CALIFORNIA

QUALCOMM INCORPORATED, Plaintiff, v. CONEXANT SYSTEMS, INC. and SKYWORKS SOLUTIONS, INC., Defendants.	02 CV 2002 B (JFS) **SECOND AMENDED COMPLAINT FOR PATENT INFRINGEMENT, MISAPPROPRIATION OF TRADE SECRETS, AND BREACH OF CONTRACT** **DEMAND FOR JURY TRIAL**
CONEXANT SYSTEMS, INC. and SKYWORKS SOLUTIONS, INC., Counterclaimants, v. QUALCOMM INCORPORATED, Counterdefendant.	

ORIGINAL

1. Plaintiff QUALCOMM Incorporated ("QUALCOMM"), for its complaint against defendants Conexant Systems, Inc. and Skyworks Solutions, Inc. ("Defendants"), alleges as follows:

THE PARTIES

QUALCOMM is a Delaware corporation that maintains its principal place of business at 5775 Morehouse Drive, San Diego, California, 92121. QUALCOMM develops, manufactures, markets, licenses and operates advanced communications systems based on proprietary technology.

2. On information and belief, defendant Conexant Systems, Inc. ("Conexant") is a Delaware corporation having its principal place of business at 4311 Jamboree Road, Newport Beach, California, 92660-3095.

3. On information and belief, defendant Skyworks Solutions, Inc. ("Skyworks") is a Delaware corporation having its principal place of business at 20 Sylvan Road, Woburn, Massachusetts, 01801. On information and belief, Skyworks was formed in June 2002 as a result of a merger between Conexant's wireless business and Alpha Industries, Inc.

JURISDICTION AND VENUE

4. This Court has jurisdiction over QUALCOMM's patent infringement claim pursuant to the patent laws of the United States, 35 U.S.C. §§ 1 et seq., and pursuant to 28 U.S.C. § 1338. This Court has supplemental jurisdiction over QUALCOMM's related misappropriation of trade secrets and breach of contract claims pursuant to 28 U.S.C. § 1367.

5. Venue is proper in this judicial district pursuant to 28 U.S.C. §§ 1391(b), 1391(c) and 1400(b) because Defendants have regularly conducted business in this judicial district, and certain of the acts complained of herein occurred in this judicial district.

FACTS

6. This action arises out of Defendants' infringement of eight patents assigned to QUALCOMM, Defendants' misappropriation of certain trade secrets owned by QUALCOMM, and defendant Conexant's breach of a nondisclosure agreement with QUALCOMM.

PATENT INFRINGEMENT

7. On March 12, 1996, U.S. Patent No. 5,499,280, entitled "CLOCK SIGNAL GENERATION," ("the '280 patent") was duly and legally issued to inventors Nathaniel B. Wilson

and Gene H. McAllister. A copy of the '280 patent is attached hereto as Exhibit A.

8. On April 1, 1997, U.S. Patent No. 5,617,060, entitled "METHOD AND APPARATUS FOR AUTOMATIC GAIN CONTROL AND DC OFFSET CANCELLATION IN QUADRATURE RECEIVER," ("the '060 patent") was duly and legally issued to inventors Nathaniel B. Wilson, Peter J. Black, and Paul E. Peterzell. A copy of the '060 patent is attached hereto as Exhibit B.

9. On March 24, 1998, U.S. Patent No. 5,732,341, entitled "METHOD AND APPARATUS FOR INCREASING RECEIVER IMMUNITY TO INTERFERENCE," ("the '341 patent") was duly and legally issued to inventor Charles E. Wheatley, III. A copy of the '341 patent is attached hereto as Exhibit C.

10. On February 16, 1999, U.S. Patent No. 5,872,481, entitled "EFFICIENT PARALLEL-STAGE POWER AMPLIFIER," ("the '481 patent") was duly and legally issued to inventors John F. Sevic and Richard J. Camarillo. A copy of the '481 patent is attached hereto as Exhibit D.

11. On September 19, 1995, U.S. Patent No. 5,452,473, entitled "REVERSE LINK, TRANSMIT POWER CORRECTION AND LIMITATION IN A RADIOTELEPHONE SYSTEM," ("the '473 patent") was duly and legally issued to inventors Ana L. Weiland, Richard K. Kornfield, Richard J. Kerr, John E. Maloney, and Nathaniel B. Wilson. A copy of the '473 patent is attached hereto as Exhibit E.

12. On December 31, 1996, U.S. Patent No. 5,590,408, entitled "REVERSE LINK, TRANSMIT POWER CORRECTION AND LIMITATION IN A RADIOTELEPHONE SYSTEM," ("the '408 patent") was duly and legally issued to inventors Ana L. Weiland, Richard K. Kornfield, and John E. Maloney. A copy of the '408 patent is attached hereto as Exhibit F.

13. On August 5, 1997, U.S. Patent No. 5,655,220, entitled "REVERSE LINK, TRANSMIT POWER CORRECTION AND LIMITATION IN A RADIOTELEPHONE SYSTEM," ("the '220 patent") was duly and legally issued to inventors Ana L. Weiland, Richard K. Kornfield, and John E. Maloney. A copy of the '220 patent is attached hereto as Exhibit G.

14. On September 2, 2003, U.S. Patent No. 6,615,027, entitled "METHOD AND

CIRCUIT FOR PROVIDING INTERFACE SIGNALS BETWEEN INTEGRATED CIRCUITS," ("the '027 patent") was duly and legally issued to inventors Gurkanwal Sahota, Mehdi H. Sani, and Sassan Shahrokhinia. A copy of the '027 patent is attached hereto as Exhibit H.

15. QUALCOMM is the owner of the '280, '060, '341, '481, '473, '408, '220, and '027 patents by assignment, with full and exclusive right to bring suit to enforce these patents.

16. The '280, '060, '341, '481, '473, '408, '220, and '027 patents relate generally to the transmission, reception and processing of radio signals by wireless telephones.

17. On information and belief, Defendants have been and are still infringing, contributing to infringement, and/or inducing others to infringe the '280, '060, '341, '481, '473, '408, '220, and '027 patents by making, using, offering for sale, selling, or importing integrated circuits and modules for use in wireless telephones. Defendants' acts of infringement have occurred within this district and elsewhere throughout the United States.

18. On information and belief, Defendants have willfully infringed the '280, '060, '341, '481, '473, '408, '220, and '027 patents by continuing in their acts of infringement after learning of these patents and of their infringement of these patents.

MISAPPROPRIATION OF TRADE SECRETS AND BREACH OF CONTRACT

19. In early 2000, QUALCOMM began discussions with Conexant regarding a possible joint business relationship between the two companies. As part of these discussions, QUALCOMM and Conexant entered into a written nondisclosure agreement ("the NDA") in July 2000. Under the NDA, QUALCOMM and Conexant agreed that any confidential information disclosed by a party in the course of the discussions would be used by the other party only for the purpose of evaluating the potential joint business relationship. A copy of the NDA is attached hereto as Exhibit I.

20. QUALCOMM has at all times complied with its material duties under the terms of the NDA.

21. On or about September 6, 2000, representatives from QUALCOMM and Conexant met to discuss the parties' potential joint business relationship. During the course of the meeting, QUALCOMM disclosed certain confidential, proprietary information regarding the design of certain interfaces for certain of its integrated circuits. In particular, QUALCOMM described a new,

optimized interface between the most recent generation of QUALCOMM's Mobile Station Modem ("MSM") and the transmit chain. At the meeting, QUALCOMM identified this information as confidential and proprietary and therefore subject to the terms of the NDA.

22. The information regarding the design of the interfaces for QUALCOMM's integrated circuits was not publicly known at that time. QUALCOMM maintained the confidentiality of its integrated circuit interface design by preventing the disclosure of this information to third parties other than disclosure covered by a nondisclosure agreement or disclosure at a later point in time through a published patent application or issued patent.

23. QUALCOMM invested substantial amounts of money and resources into the design of its integrated circuit interfaces. The interface design was inventive, and of great commercial importance to QUALCOMM as a trade secret pending any publication of a patent application or issued patent. If competitors learned of the information maintained by QUALCOMM as a trade secret, they could undermine the competitive advantages rightfully belonging to QUALCOMM and unfairly undermine QUALCOMM's position in the market.

24. By the end of 2000, QUALCOMM and Conexant decided not to pursue a joint business relationship.

25. Around May 2001, QUALCOMM discovered that Conexant was manufacturing and selling integrated circuits based on the interface design information obtained from QUALCOMM in September 2000.

26. By using QUALCOMM's design information in this manner, Conexant violated the NDA's requirement that this information be used solely for the purposes of evaluating the parties' potential joint business relationship. QUALCOMM subsequently informed Conexant that it was using QUALCOMM's proprietary and trade secret information in violation of the NDA, and demanded that Conexant cease its unauthorized activities.

27. Despite being on notice that it was in violation of the NDA, Conexant continued to manufacture and sell integrated circuits based on QUALCOMM's proprietary interface design.

28. On information and belief, Skyworks manufactures and sells integrated circuits based on QUALCOMM's proprietary interface design, and has acquired this design information through

Conexant. As a successor corporation to Conexant, Skyworks knew or reasonably should have known that this design information was proprietary and trade secret information owned by QUALCOMM that should not have been used for commercial purposes under the NDA.

COUNT ONE

(PATENT INFRINGEMENT)

29. QUALCOMM repeats and re-alleges the allegations of paragraphs 1 through 28 above as if fully set forth herein.

30. In violation of 35 U.S.C. § 271, Defendants have infringed and are continuing to infringe, literally and/or under the doctrine of equivalents, the '280, '060, '341, '481, '473, '408, '220, and '027 patents by practicing one or more claims of each of the '280, '060, '341, '481, '473, '408, '220, and '027 patents in their manufacture, use, offering for sale, sale, and/or importation of integrated circuits and modules for use in wireless telephones, and/or by inducing or contributing to the infringement of the '280, '060, '341, '481, '473, '408, '220, and '027 patents by others.

31. QUALCOMM has been damaged by Defendants' infringement and, unless Defendants secure a license to the '280, '060, '341, '481, '473, '408, '220, and '027 patents from QUALCOMM or are enjoined by this Court, Defendants will continue their infringing activity and QUALCOMM will continue to be damaged.

COUNT TWO

(MISAPPROPRIATION OF TRADE SECRETS)

32. QUALCOMM repeats and re-alleges the allegations of paragraphs 1 through 28 above as if fully set forth herein.

33. QUALCOMM adopted reasonable measures as described herein to maintain the secrecy of the interface design at issue.

34. QUALCOMM has invested substantial amounts of money and resources in the development of the interface design for its integrated circuits. The interface design is of great commercial importance to QUALCOMM.

35. Defendants knew or should have known when they manufactured and sold products incorporating QUALCOMM's proprietary interface design that they were misusing confidential,

proprietary trade secret information belonging to QUALCOMM.

36. Defendants' manufacture and sale of products incorporating QUALCOMM's proprietary interface design with full knowledge of their duty not to make commercial use of that information constitutes misappropriation of QUALCOMM's trade secrets under California Civil Code § 3426 et seq.

37. Defendants' misappropriation of QUALCOMM's trade secrets was willful and malicious.

38. QUALCOMM has been damaged by Defendants' misappropriation of its trade secrets and, unless Defendants are enjoined by this Court, Defendants will continue their misappropriation of QUALCOMM's trade secrets by continuing to manufacture and sell products incorporating QUALCOMM's proprietary interface design.

COUNT THREE

(BREACH OF CONTRACT)

39. QUALCOMM repeats and re-alleges the allegations of paragraphs 1 through 28 and 32 through 38 above as if fully set forth herein.

40. In default of its obligations under the NDA, defendant Conexant has used confidential, proprietary trade secret information belonging to QUALCOMM and covered by the NDA for purposes other than evaluating the possibility of a joint business relationship between QUALCOMM and Conexant.

41. QUALCOMM has performed all of its material obligations under the NDA.

42. QUALCOMM has been damaged as a result of Conexant's breach of the NDA and, unless Conexant is enjoined by this Court, Conexant will continue to breach the NDA by continuing to manufacture and sell products incorporating QUALCOMM's proprietary interface design.

PRAYER FOR RELIEF

WHEREFORE, plaintiff QUALCOMM prays for the following relief against Defendants:

(a) A preliminary and permanent injunction against Defendants, their officers, agents, servants, employees, attorneys, all parent and subsidiary corporations, all assignees and successors in interest, and those persons in active concert or participation with Defendants, including distributors

and customers, enjoining them from continuing acts of infringement of QUALCOMM's '280, '060, '341, '481, '473, '408, '220, and '027 patents;

(b) An award of damages under 35 U.S.C. § 284 for Defendants' infringement of QUALCOMM's '280, '060, '341, '481, '473, '408, '220, and '027 patents, including damages based on lost profits, lost royalties, and price erosion, together with pre-judgment and post-judgment interest;

(c) A trebling of said damages pursuant to 35 U.S.C. § 284;

(d) An award of attorneys' fees pursuant to 35 U.S.C. § 285;

(e) An injunction against Defendants, their officers, agents, servants, employees, attorneys, all parent and subsidiary corporations, all assignees and successors in interest, and those persons in active concert or participation with Defendants, enjoining them from manufacturing or selling products incorporating QUALCOMM's proprietary integrated circuit interface design;

(f) An award of damages for Defendants' misappropriation of QUALCOMM's trade secrets, together with pre-judgment and post-judgment interest;

(g) A doubling of such damages pursuant to Cal. Civ. Code § 3426.3(c);

(h) An award of recovery of Defendants' unjust enrichment pursuant to Cal. Civ. Code § 3426.3(a);

(i) An award of attorneys' fees for Defendants' misappropriation of QUALCOMM's trade secrets pursuant to Cal. Civ. Code § 3426.4;

(j) An award of damages for defendant Conexant's breach of the NDA, together with pre-judgment and post-judgment interest;

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(k) An award of attorneys' fees for defendant Conexant's breach of the NDA, pursuant to section 12 of the NDA;

(l) Any such other relief that this Court deems just and proper.

Dated: June 9, 2004

DAY CASEBEER
MADRID & BATCHELDER LLP

By: _____
James R. Batchelder

Attorneys for Plaintiff and Counterdefendant
QUALCOMM Incorporated

DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Federal Rules of Civil Procedure, QUALCOMM demands a trial by jury on all issues triable of right by a jury.

Dated: June 1, 2004

DAY CASEBEER
MADRID & BATCHELDER LLP

By: _____
James R. Batchelder

Attorneys for Plaintiff and Counterdefendant
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US005499280A

United States Patent [19]

Wilson et al.

[11] Patent Number: 5,499,280

[45] Date of Patent: Mar. 12, 1996

[54] CLOCK SIGNAL GENERATION

[75] Inventors: Nathaniel B. Wilson, San Diego; Gene H. McAllister, La Mesa, both of Calif.

[73] Assignee: QUALCOMM Incorporated, San Diego, Calif.

[21] Appl. No.: 382,770

[22] Filed: Feb. 2, 1995

[51] Int. Cl.[6] H03K 23/48

[52] U.S. Cl. 377/108; 377/48; 327/115

[58] Field of Search 377/48, 108; 327/115, 327/160

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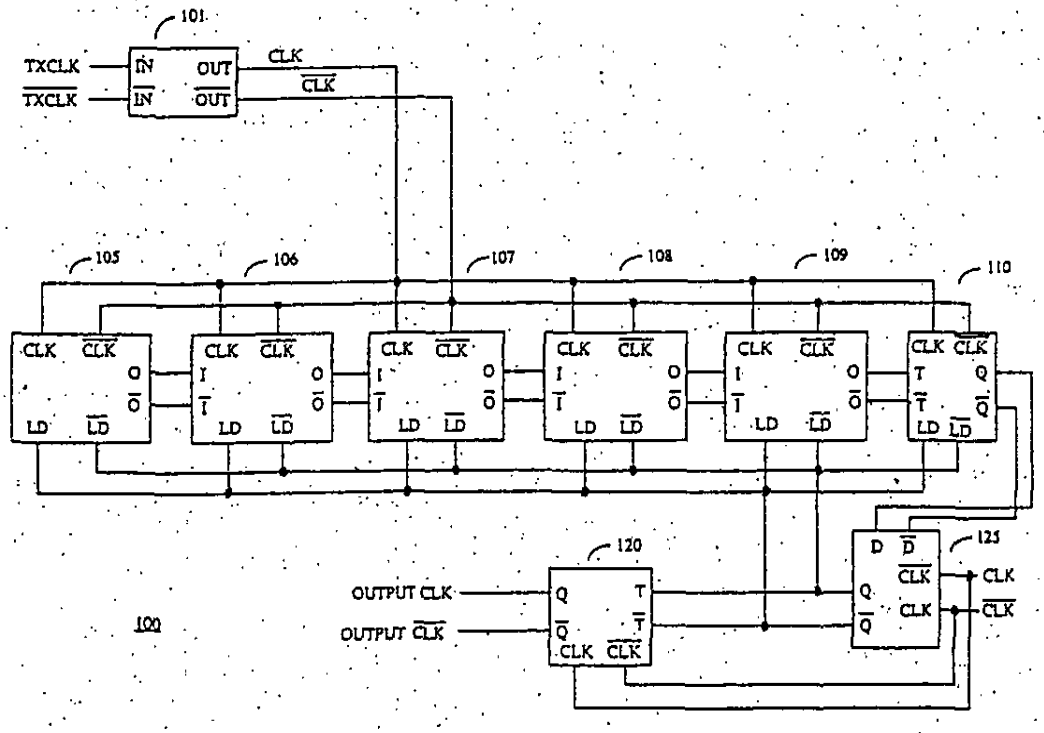
Primary Examiner—John S. Heyman

Attorney, Agent, or Firm—Russell B. Miller; Roger W. Martin

[57] ABSTRACT

The clock signal generator of the present invention divides a higher frequency clock down to a frequency that is an uneven sub-multiple of the higher frequency. The input clock to be divided down clocks an 11-bit counter (105–110) that outputs an overflow signal to a D flip-flop (125). The D flip-flop generates a load signal that resets the counter after 1025 clock periods. The load signal also suppresses, after 1025 clock periods, the toggling of another toggle flip-flop (120) that provides a divide by two clock. By suppressing a clock pulse in the divide by two clock, every 1025 clock pulses of the higher frequency clock, the average clock frequency of the divide by two clock is reduced to an uneven sub-multiple of the higher clock frequency.

12 Claims, 3 Drawing Sheets



Ex. A-1

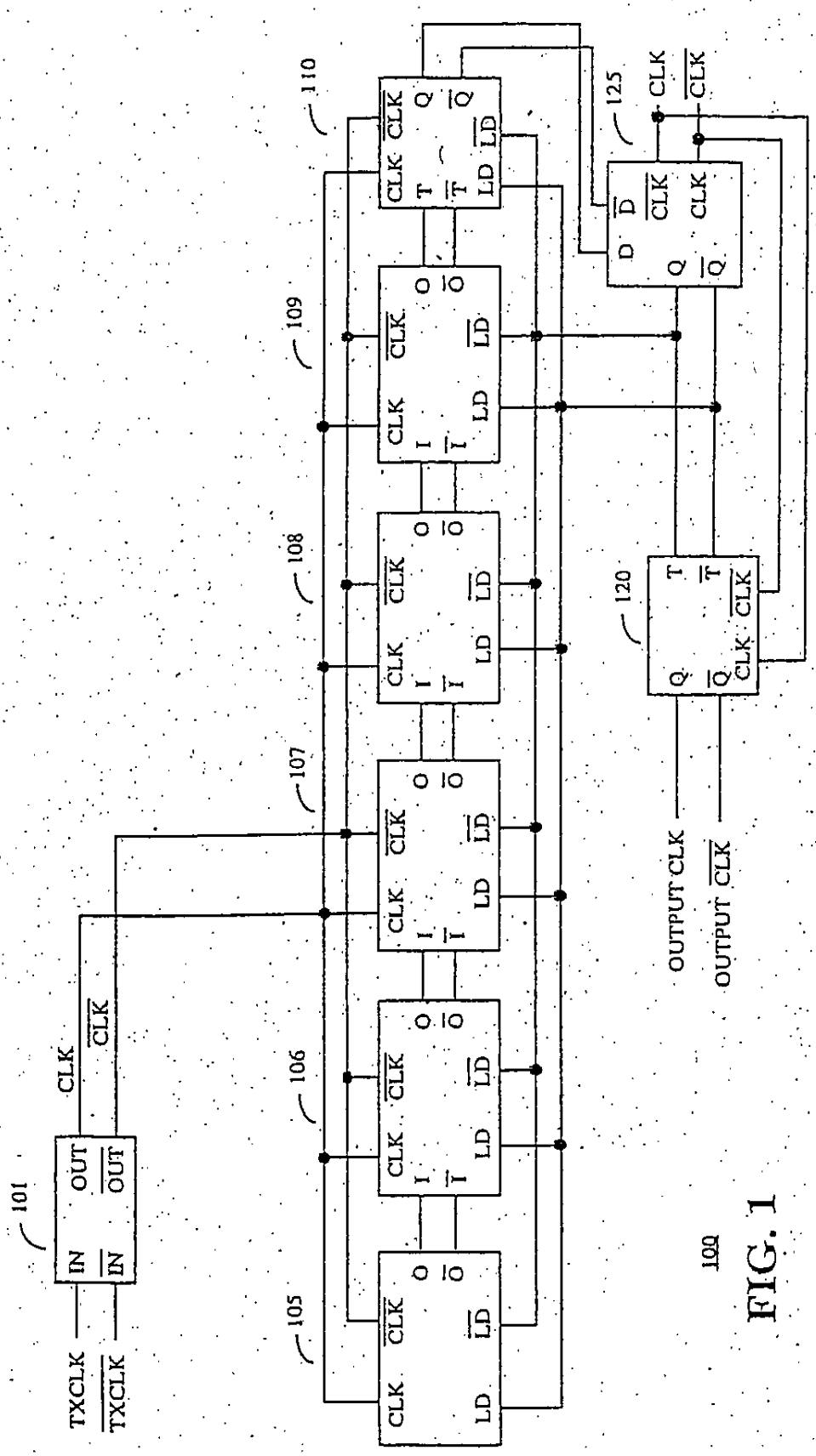


FIG. 1

Ex. A-2

Ex. A-2

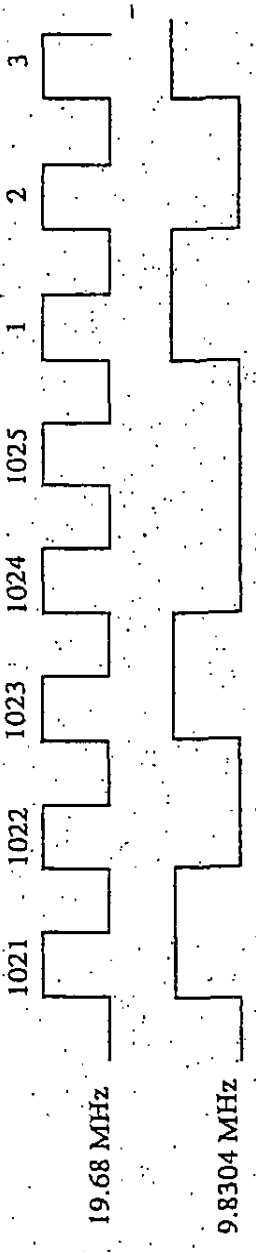


FIG. 2

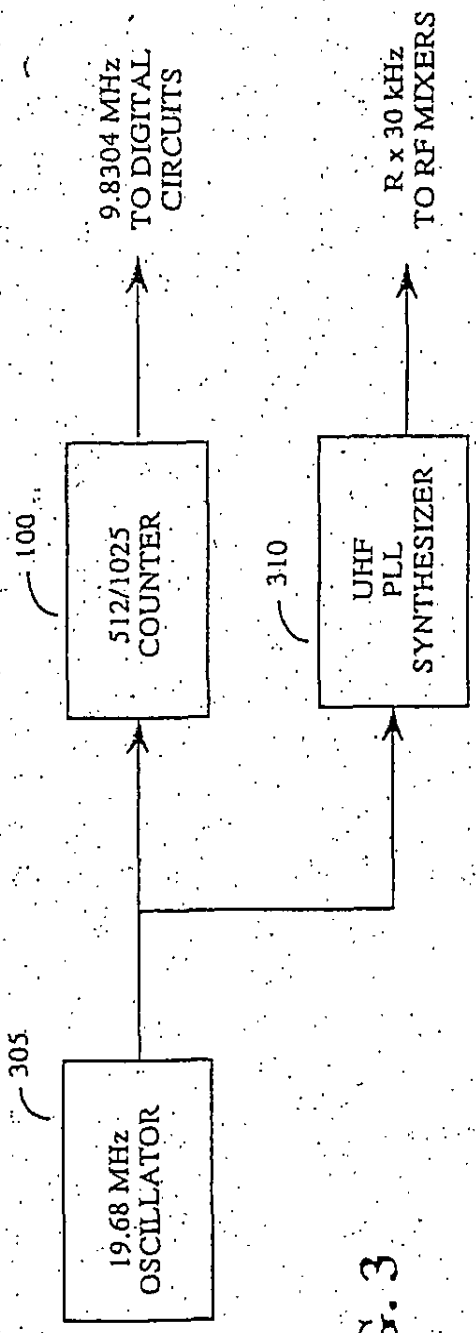


FIG. 3

Ex. A-3

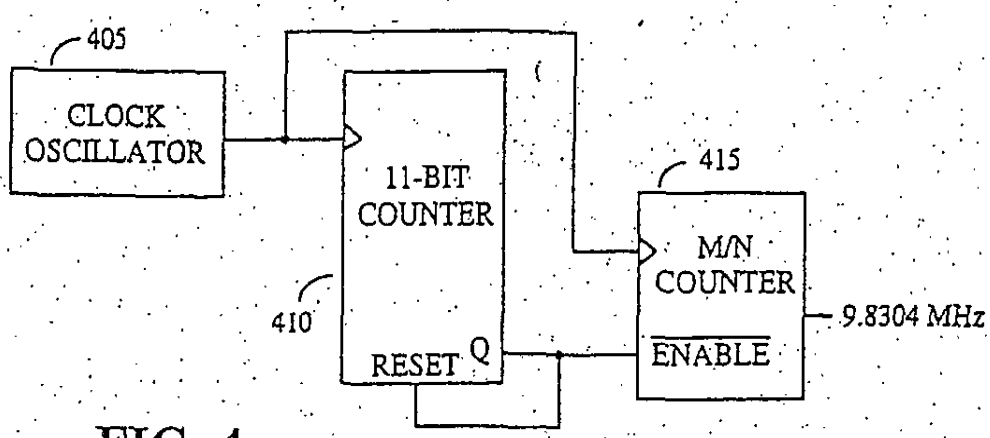


FIG. 4

CLOCK OSCILLATOR FREQ.	M/N FOR 9.8304 MHz
9.84 MHz (2 x 4.92 MHz)	1/1
14.76 MHz (3 x 4.92 MHz)	2/3
19.68 MHz (4 x 4.92 MHz)	1/2
24.6 MHz (5 x 4.92 MHz)	2/5
29.52 MHz (6 x 4.92 MHz)	1/3

FIG. 5

Ex. A-4

CLOCK SIGNAL GENERATION

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to clock signals. More particularly, the present invention relates to the generation of a clock signal.

2. Description of the Related Art

Cellular radiotelephones are rapidly decreasing in size and cost. In order to accomplish these reductions, the number of parts contained in a radiotelephone are reduced. This reduces the cost of the total number of radiotelephone parts, the manufacturing costs and also reduces the weight of the unit. In order to continue these reductions in cost and weight, the radiotelephone parts count must be reduced further.

Radiotelephones require multiple clock frequencies to operate due to the different requirements of circuits within the radiotelephone. For example, a microprocessor may use a different clock than the RF circuits. Some of these clock frequencies are obtained by dividing one clock signal into sub-multiples of that frequency. This technique reduces the number of oscillators needed to generate the various clock signals.

In a code division multiple access radiotelephone, a master clock frequency of eight times the chip rate of 1.2288 MHz is used for various digital circuits. For cellular use, this frequency, 9.8304 MHz, or its double of 19.6608 MHz, are not suitable master frequencies for the RF components of the radiotelephone since neither is an even multiple of the 30 kHz RF channel spacing required for cellular radio in the United States.

In this case, multiple oscillators are needed to generate the different clock signals required by both the digital hardware and the RF circuitry. There is a resulting need for a clock generator that can produce a clock frequency that is an uneven multiple of another frequency, thus reducing the number of clock synthesizers required.

SUMMARY OF THE INVENTION

The clock generator of the present invention generates a clock signal having a frequency that is an uneven sub-multiple of a higher frequency input clock signal. The clock generator is comprised of a counter that is clocked by the input clock signal. The counter generates a count overflow indication in response to a predetermined number of input clock signal pulses. A data latch is coupled to the count overflow indication. The input clock signal latches the count overflow indication into the data latch, thus generating a load signal. A toggle flip-flop is coupled to the input clock signal and the load signal. The toggle flip-flop divides down the input clock signal to a lower frequency while the load signal adjusts this lower frequency to the frequency that is an uneven submultiple of the frequency of the input clock signal.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a circuit diagram of the preferred embodiment of the clock generator of the present invention.

FIG. 2 shows a timing diagram in accordance with the clock generator of FIG. 1.

FIG. 3 shows a block diagram of a clock generation circuit incorporating the clock generator of FIG. 1.

FIG. 4 shows a block diagram of the clock generator of the present invention.

FIG. 5 shows a table of clock oscillator frequencies and divide ratios in accordance with the block diagram of FIG. 4.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The clock generator of the present invention divides a higher frequency clock signal down to an uneven multiple, lower frequency clock signal. In the preferred embodiment, the clock generator provides an output to input ratio of $^{313}/_{1025}$. The clock generator thus eliminates the need for an analog synthesizer to generate the lower clock frequency.

The clock generator of the present invention is illustrated in FIG. 4. The clock generator is comprised of a clock oscillator (405) that generates an input clock signal for an 11-bit counter (410) and an $^{M}/_{N}$ counter (415). The divide ratio of the $^{M}/_{N}$ counter (415) is different for alternate embodiments to accommodate different input clock signal frequencies. The divide ratio is changed by implementing the $^{M}/_{N}$ counter (415) in different ways. The 11-bit counter (410) enables and disables the M/N counter (415), thus altering the average frequency of the clock signal output from the $^{M}/_{N}$ counter.

In the preferred embodiment, the input clock is a multiple of 4.92 MHz. 19.68 MHz (4×4.92 MHz=656×30 kHz) and 24.6 MHz (5×4.92 MHz =820×25 kHz) are particularly convenient values. In CDMA cellular telephones with a spread spectrum chip rate of 1.2288 MHz, this selection of the input clock is especially advantageous.

An input clock that is an even multiple of 30 kHz is required for the RF phase locked loop synthesizer in phones for U.S. cellular (or a multiple of 25 kHz for some countries). 4.92 MHz is the closest multiple of 30 kHz that is greater than 4×1.2288 MHz. For this reason, the telephone can use analog to digital converters (ADC) and digital to analog converters (DAC) that are clocked by the generator of the present invention, without a significant performance penalty due to the resulting clock jitter.

For example, for the case of an input clock of 19.68 MHz and a signal bandwidth of 614 kHz being clocked out of a DAC, the clock jitter results in about −25dBc of in-band noise being added to the DAC's output spectrum. However, the out of band noise (at greater than 750 kHz) is down below −40 dBc. Both the in-band and out of band noise is acceptable for spread spectrum cellular. If an input clock such as 19.8 MHz, which is farther from a multiple of 4.92 MHz, was selected to drive the $^{M}/_{N}$ counter for the DAC's, the out of band noise that results from the clock jitter would be unacceptably large.

The table of FIG. 5 illustrates some possible clock oscillator frequencies and the respective dividing ratios for the $^{M}/_{N}$ counter to generate the desired 9.8304 MHz signal. The preferred embodiment of the clock generator uses a 19.68 MHz clock frequency with a dividing ratio of ½.

The preferred embodiment of the clock generator of the present invention is illustrated in FIG. 1. This embodiment is comprised of five 2-bit counters (105–109) and a 1-bit counter (110) connected in a 6 stage configuration. These counters taken together form the 11-bit counter (410) of FIG. 4. In the preferred embodiment, the 1-bit counter (110) is a toggle flip-flop.

The counters each have count overflow outputs that become true when the counter overflows from the logical

Ex. A-5

"11" state. In the preferred embodiment, each counter has both a count overflow output and an inverse count overflow output.

The count overflow output and the inverse count overflow output of one stage (105) are coupled to the count input and inverse count input, respectively, of the next counter stage (106). These outputs cause the clock pulse count to ripple through the 5 counters. The count overflow output and inverse count overflow output of the last 2-bit counter stage (109) is input to the toggle and inverse toggle inputs of the flip-flop (110) configured to operate as a 1-bit counter.

The input clock signal, from the clock oscillator, is input to a clock driver (101) that increases the drive current of the clock. The clock driver (101) increases the number of gates that the clock signal can drive. In the preferred embodiment, the clock signal is comprised of a clock and an inverse clock.

The counters (105–110) are clocked by the clock signal from the clock driver (101). The clock and the inverse clock are input to the counters respective clock and inverse clock inputs. In the preferred embodiment, the counters (105–110) increment on the rising edge of the clock pulse and the falling edge of the inverse clock pulse.

The most significant bit from the final stage of the counter (110) goes true on the 1024^{th} input clock cycle. This bit is output to a D flip-flop (125) where it is latched in by the inverse input clock signal to generate a latched load signal.

The latched load signal is used to load logical 0's into the counter. This effectively resets the counter to zero so that the count begins from there. The load occurs on the 1025^{th} input clock cycle. In the preferred embodiment, the load signal is comprised of a load and inverse load signal.

The output clock signal, 9.8304 MHz in the preferred embodiment, is generated by a divide-by-two toggle flip-flop (120) that serves as the $^{M}/_{N}$ counter (415) from FIG. 4. The latched load and inverse load signals are input to the toggle inputs of the flip-flop (120). The clock and inverse clock signals are input to the respective clock inputs of the flip-flop (120). When the latched load signals are false, the toggle flip-flop (120) changes state on the rising edge of the clock signal pulses. This toggling divides the clock signal by 2.

The divide-by-two state exists for 1024 input clock periods, producing 512 output clock pulses. During the 1025^{th} input clock period, the load signal disables the toggle input, forcing the flop-flop (120) to hold its current state. The toggle flip-flop (120), therefore, produces 512 clock periods for each 1025 input clock periods.

The output clock does not have a constant cycle time. The long term average frequency (or the average over 512 cycles) is 9.8304 MHz. The resulting jitter is within tolerable limits for the preferred embodiment of a cellular radiotelephone. The divided down clock also benefits from low spectral noise.

FIG. 2 illustrates a timing diagram of the higher frequency input clock signal in comparison to the output clock signal. It can be seen that the output clock toggles on the leading edge of each input clock pulse. This continues until the 1025^{th} clock pulse where the divide-by-two toggle flip-flop is disabled by the load signal.

FIG. 3 illustrates a typical cellular radiotelephone application for the clock generator of the present invention. This clock generation circuit uses a 19.68 MHz oscillator (305) to generate the input clock signal. The clock generator (100) of the present invention then produces the 9.8304 MHz clock. A phase locked loop synthesizer (310) generates another clock having a higher frequency that is an integer multiple, R, of 30 kHz. This clock, in the preferred embodiment, is used by the RF mixers of the radio.

As is evident from FIG. 5, additional embodiments of the clock generator of the present invention can use different input clock signals to generate the 9.8304 MHz output clock. These alternate embodiments implement the $^{M}/_{N}$ counter in different ways to generate the output clock.

A first alternate embodiment generates the output clock signal using an input clock signal of 9.84 MHz (2×4.92 MHz). In this embodiment, the $^{M}/_{N}$ counter is an asynchronous clock gating circuit.

A second embodiment generates the output clock signal using an input clock signal having a frequency of 14.76 MHz (3×4.92 MHz). In this embodiment, a 2-bit state machine with asynchronous clock gating is used as the $^{M}/_{N}$ counter.

A third embodiment generates the output clock signal using an input clock signal having a frequency of 24.6 MHz (5×4.92 MHz). This embodiment uses a 3-bit state machine as the $^{M}/_{N}$ counter.

A fourth embodiment generates the output clock signal using an input clock signal having a frequency of 29.52 MHz (6×4.92 MHz). This embodiment uses a 2-bit state machine as the $^{M}/_{N}$ counter.

Other embodiments of the clock generator of the present invention can be implemented using other types of $^{M}/_{N}$ counters. The embodiments presented above are only a narrow sampling of such embodiments.

The preferred embodiment of the present invention also uses both a signal and an inverse of the signal. Alternate embodiments may use only the signal, and not the inverse signal, depending on the technology in which the present invention is implemented; i.e., CMOS, bipolar, etc.

As can be seen above, the clock generator of the present invention generates an uneven multiple clock frequency without additional analog frequency synthesizers, thus saving cost and weight in an electronic device. Without the clock generator of the present invention, additional phase locked loop synthesizers would be required.

We claim:

1. A clock generator for generating an output clock signal having a first frequency from an input clock signal having a second frequency, the first frequency being an uneven sub-multiple of the second frequency, the clock generator comprising:

a counter having a clock input coupled to the input clock signal and a reset input coupled to a latched load signal, the counter generating a count overflow indication in response to a predetermined number of input clock signal pulses and resetting in response to the latched load signal;

a data latch having an input coupled to the count overflow indication, the data latch generating the latched load signal in response to the input clock signal and the count overflow indication; and

a toggle flip-flop having a first input coupled to the input clock signal and a second input coupled to the latched load signal, the toggle flip-flop generating the output clock signal in response to the latched load signal and the input clock signal.

2. The clock generator of claim 1 wherein said counter further comprises:

a plurality of 2-bit counters each having an input coupled to the input clock signal, the plurality of 2-bit counters

Ex. A-6

each generating a 2-bit count overflow indication, each 2-bit count overflow indication being coupled to a next stage 2-bit counter of the plurality of 2-bit counters, a final stage 2-bit counter of the plurality of 2-bit counters generating a final stage 2-bit count overflow indication; and

a 1-bit counter having a first input coupled to the final stage 2-bit count overflow indication and a second input coupled to the input clock signal.

3. The clock generator of claim 2 wherein said data latch is a D flip-flop.

4. A clock generator for generating an output clock signal having a first frequency from an input clock signal having a second frequency, the first frequency being an uneven sub-multiple of the second frequency, the clock generator comprising:

a plurality of counters each having a clock input coupled to the input clock signal and each having a reset input coupled to a latched load signal, the plurality of counters each generating a count overflow indication and each resetting in response to the latched load signal, each count overflow indication being coupled to a next stage counter of the plurality of counters, a final stage counter of the plurality of counters generating a predetermined maximum count indication;

a D flip-flop having a first input coupled to the predetermined maximum count indication and a second input coupled to the input clock signal, the D flip-flop generating the latched load signal in response to the predetermined maximum count indication and the input clock signal; and

a toggle flip-flop having a first input coupled to the input clock signal and a second input coupled to the latched load signal, the toggle flip-flop generating the output clock signal in response to the latched load signal and the input clock signal.

5. A clock generator for generating an output clock signal having a first frequency from an input clock signal having a second frequency, the first frequency being an uneven sub-multiple of the second frequency, the clock generator comprising:

a plurality of 2-bit counters each having an input coupled to the input clock signal, the plurality of 2-bit counters each generating a count overflow indication, each count overflow indication being coupled to a next stage counter of the plurality of 2-bit counters, a final stage 2-bit counter of the plurality of counters generating a 2-bit count overflow indication;

h first toggle flip-flop having a first input coupled to the 2-bit count overflow indication and a second input coupled to the input clock signal, the first toggle flip-flop generating a predetermined maximum count indication;

a D flip-flop having a first input coupled to the predetermined maximum count indication and a second input coupled to the input clock signal, the D flip-flop generating a latched load signal in response to the predetermined maximum count indication and the input clock signal; and

a second toggle flip-flop having a first input coupled to the input clock signal and a second input coupled to the latched load signal, the second toggle flip-flop generating the output clock signal in response to the latched load signal and the input clock signal.

6. A method for generating an output clock signal having a first frequency from an input clock signal having a second frequency in a circuit having a counter, the first frequency being an uneven sub-multiple of the second frequency, the method comprising the steps of:

generating by the counter a maximum count indication after a predetermined number of clock pulses of the input clock signal;

generating a latched load signal in response to the maximum count indication and the input clock signal;

generating the output clock signal, when the latched load signal is false, in response to the input clock signal;

disabling the output clock signal when the latched load signal is true; and

resetting the counter when the latched load signal is true.

7. A clock generation circuit for generating a first clock signal having a first frequency and a second clock signal having a second frequency both from an input clock signal having a third frequency, the first frequency being an uneven sub-multiple of the third frequency, the clock generator comprising:

an oscillator for generating the input clock signal having the third frequency of N×4.92 MHz;

a clock generator for generating the first clock signal, the clock generator having an output to input ratio of $(^{1024}/_{1025})\times(^{2}/_{N})$, the clock generator comprising:

a counter having a clock input coupled to the input clock signal

and a reset input coupled to a latched load signal, the counter generating a count overflow indication in response to a predetermined number of input clock signal pulses and resetting in response to the latched load signal;

a data latch having an input coupled to the count overflow indication, the data latch generating the latched load signal in response to the input clock signal and the count overflow indication; and

a toggle flip-flop having a first input coupled to the input clock signal and a second input coupled to the latched load signal, the toggle flip-flop generating the output clock signal in response to the latched load signal and the input clock signal; and a phase locked loop synthesizer for generating the second clock signal.

8. The clock generation circuit of claim 7 wherein N is an integer and N≧2.

9. The clock generator of claim 7 wherein said counter further comprises:

a plurality of 2-bit counters each having an input coupled to the input clock signal, the plurality of 2-bit counters each generating a 2-bit count overflow indication, each 2-bit count overflow indication being coupled to a next stage 2-bit counter of the plurality of 2-bit counters, a final stage 2-bit counter of the plurality of 2-bit counters generating a final stage 2-bit count overflow indication; and

a 1-bit counter having a first input coupled to the final stage 2-bit count overflow indication and a second input coupled to the input clock signal.

10. The clock generator of claim 9 wherein said data latch is a D flip-flop.

11. A clock generator for generating an output clock signal having a first frequency from an input clock signal having a second frequency, the first frequency being an uneven sub-multiple of the second frequency, the clock generator comprising:

Ex. A-7

Ex. A-7

a first counter having a clock input coupled to the input clock signal and a reset input coupled to a count overflow indication, the counter generating the count overflow indication in response to a predetermined number of input clock signal pulses, the first counter being reset by the count overflow indication; and

a second counter having a first input coupled to the input clock signal and a second input coupled to the count overflow indication, the second counter generating the output clock signal from the input clock signal and modifying the output clock signal in response to the count overflow indication.

12. The clock generator of claim 11 wherein said first counter further comprises:

a plurality of 2-bit counters each having an input coupled to the input clock signal, the plurality of 2-bit counters each generating a 2-bit count overflow indication, each 2-bit count overflow indication being coupled to a next stage 2-bit counter of the plurality of 2-bit counters, a final stage 2-bit counter of the plurality of 2-bit counters generating a final stage 2-bit count overflow indication; and

a 1-bit counter having a first input coupled to the final stage 2-bit count overflow indication and a second input coupled to the input clock signal.

Ex. A-8

US005617060A

United States Patent [19]

Wilson et al.

[11] Patent Number: 5,617,060

[45] Date of Patent: Apr. 1, 1997

[54] METHOD AND APPARATUS FOR AUTOMATIC GAIN CONTROL AND DC OFFSET CANCELLATION IN QUADRATURE RECEIVER

[75] Inventors: Nathaniel B. Wilson, San Diego, Calif.; Peter J. Black, St. Lucia, Australia; Paul E. Peterzell, San Diego, Calif.

[73] Assignee: QUALCOMM Incorporated, San Diego, Calif.

[21] Appl. No.: 423,332

[22] Filed: Apr. 13, 1995

Related U.S. Application Data

[63] Continuation of Ser. No. 235,812, Apr. 28, 1994, abandoned.

[51] Int. Cl.[6] H03G 3/20

[52] U.S. Cl. 330/129; 455/239.1; 330/141

[58] Field of Search 330/129, 141, 330/279, 281; 332/123, 124, 125; 455/239.1, 240.1, 245.1, 250.1

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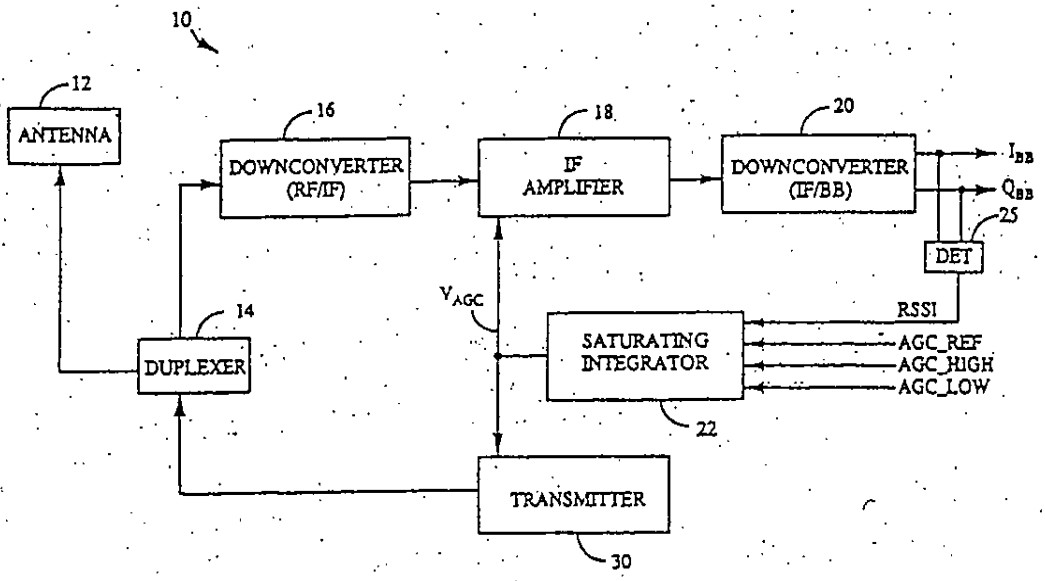
Primary Examiner—Steven Mottola

Attorney, Agent, or Firm—Russell B. Miller; Roger W. Martin

[57] ABSTRACT

An automatic gain control (AGC) and D.C. offset correction method and apparatus for controlling signal power of a received RF signal within a dual mode quadrature receiver is disclosed herein. In a preferred implementation the automatic gain control apparatus may be adjusted to provide a desired control response to various fading characteristics of a received FM, FSK, GMSK, QPSK, or BPSK signal. The AGC apparatus includes an adjustable gain amplifier having an input port for receiving an input signal, a control port for receiving a gain control signal, and an output port for providing an output signal. A quadrature downconverter coupled to the output port serves to translate the frequency of the output signal to a baseband frequency, thereby producing baseband signals. In a preferred implementation the downconverter is operative to map the carrier frequency of the output signal to a baseband frequency offset by a predetermined margin from D.C. Two high gain active lowpass filters provide out-of-band signal rejection for the baseband signals. A D.C. feedthrough suppression loop, disposed to receive said baseband signal, suppresses D.C. offsets produced by the downconverter and lowpass filters, hence providing a compensated baseband signal. The AGC apparatus is further disposed to generate a received power signal based on the power of the output signal. A saturating integrator compares the received power signal to a reference signal and produces the gain control signal by integrating or by refraining from integration based on values of the reference, received power signal, and gain control signals, thereby extending the usable dynamic range of the receiver for FM mode.

21 Claims, 10 Drawing Sheets



Ex. B-1

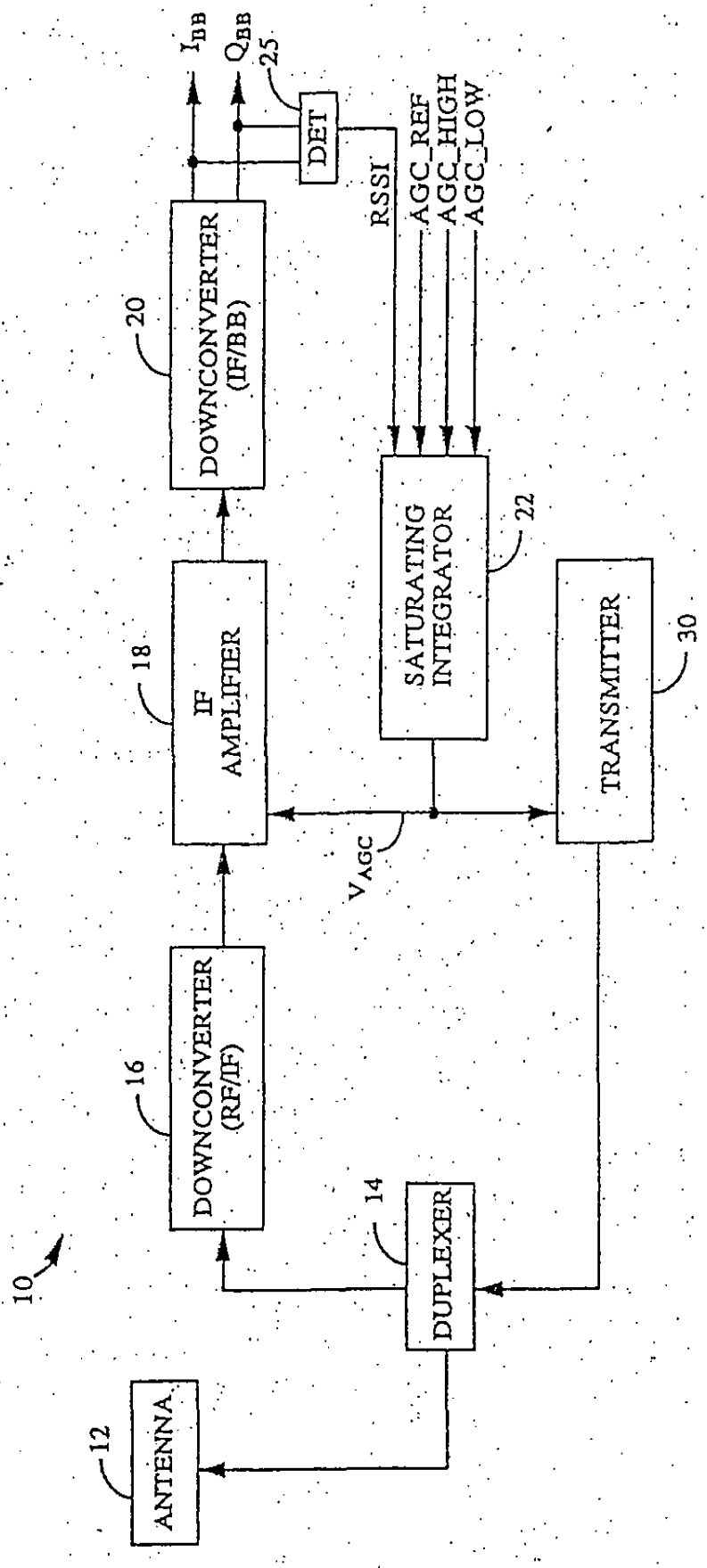


FIG. 1

Ex. B-2

Ex. B-2

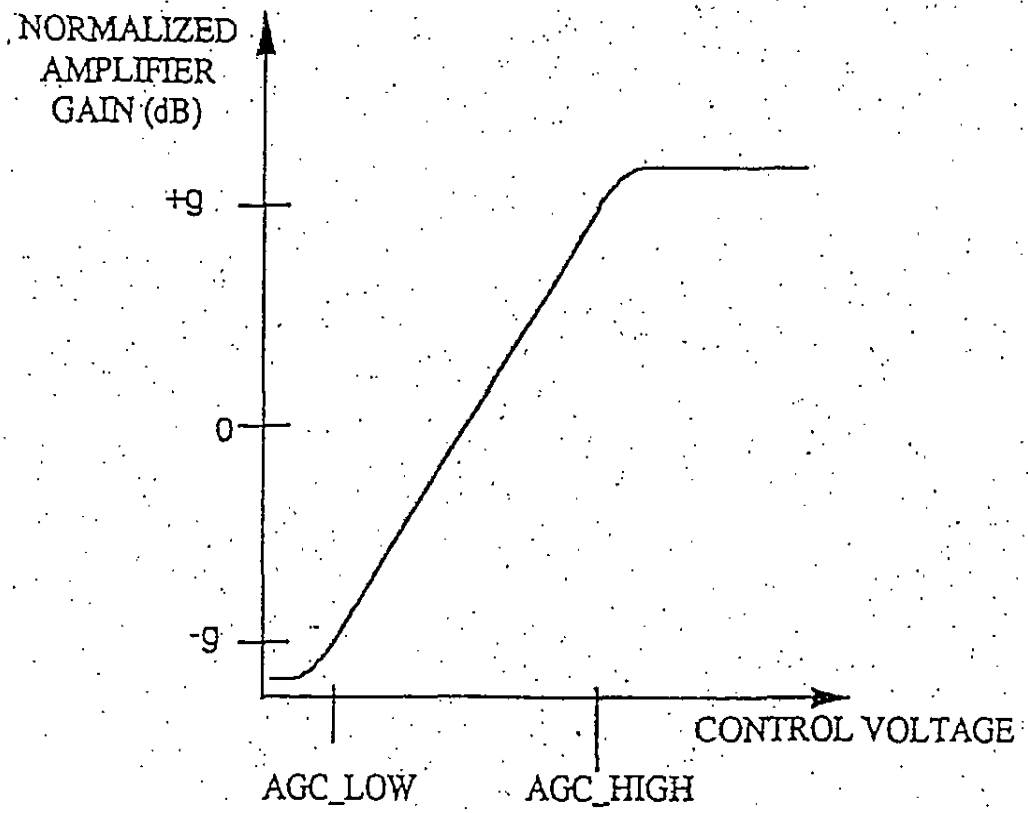

NORMALIZED
AMPLIFIER
GAIN (dB)
+g
0
-g
CONTROL VOLTAGE
AGC_LOW
AGC_HIGH

FIG. 2

Ex. B-3

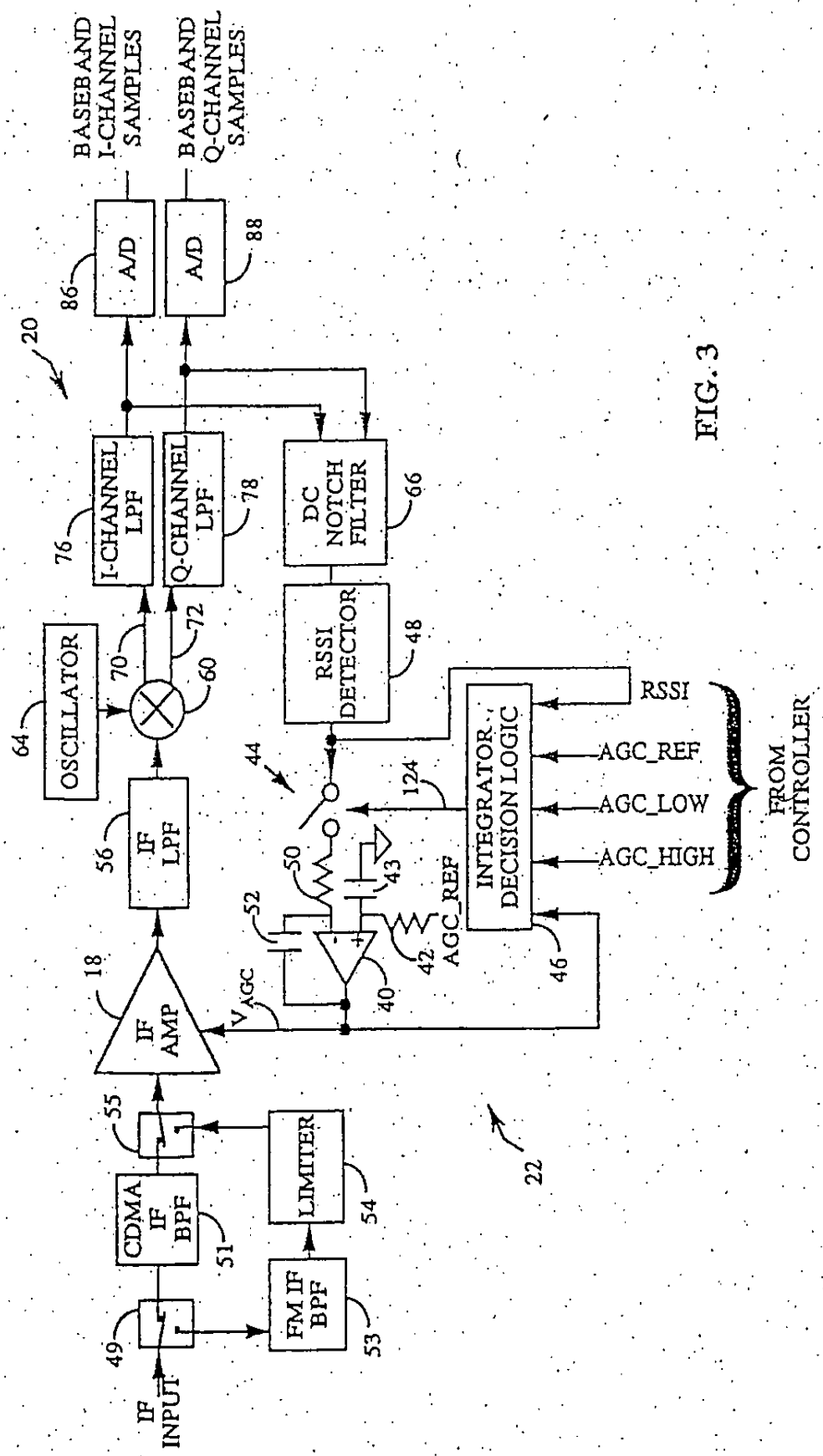

BASEBAND I-CHANNEL SAMPLES
BASEBAND Q-CHANNEL SAMPLES
A/D
A/D
86
88
20
I-CHANNEL LPF
Q-CHANNEL LPF
76
78
DC NOTCH FILTER
66
RSSI DETECTOR
48
OSCILLATOR
64
70
72
60
IF LPF
56
44
124
RSSI
AGC_REF
AGC_LOW
AGC_HIGH
FROM CONTROLLER
INTEGRATOR DECISION LOGIC
50
43
52
42
AGC_REF
46
18
IF AMP
V_AGC
40
55
CDMA IF BPF
51
LIMITER
54
22
49
FM IF BPF
53
IF INPUT

FIG. 3

Ex. B-4

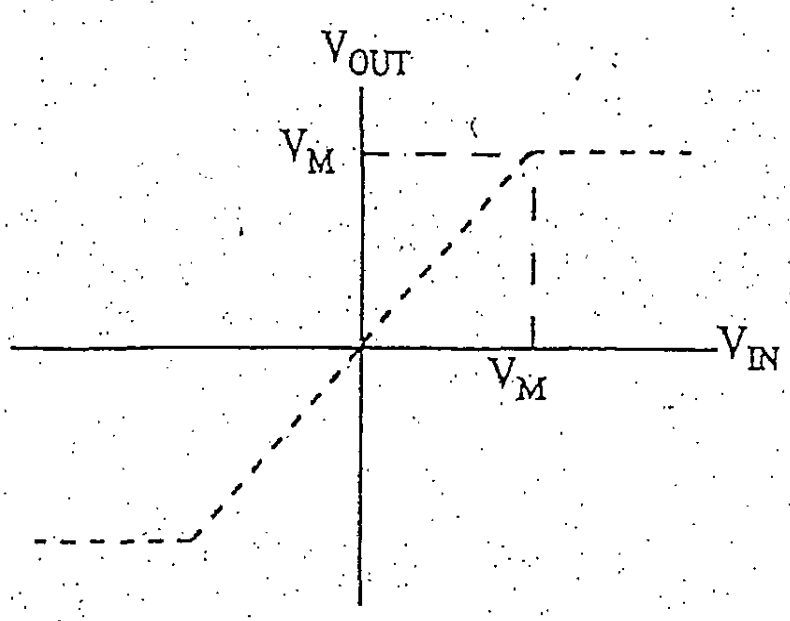


FIG. 4A

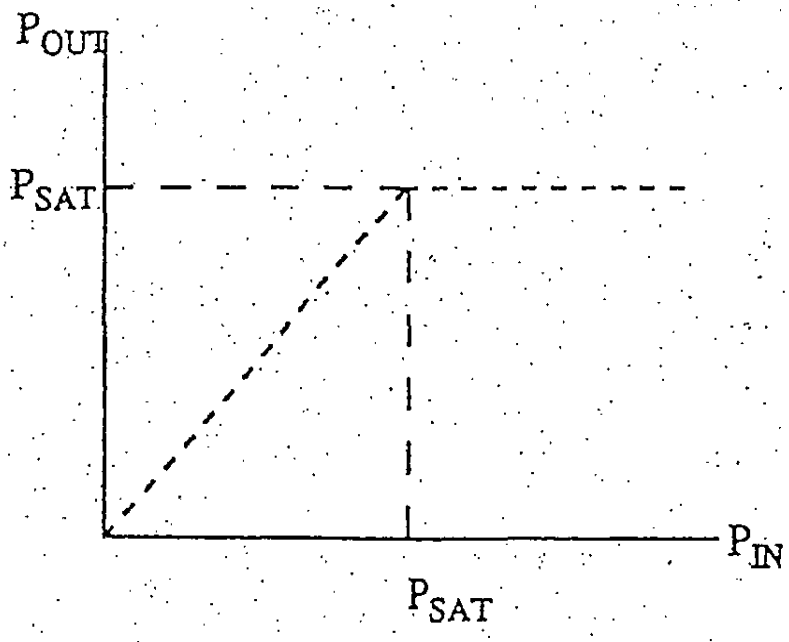


FIG. 4B

Ex. B-5

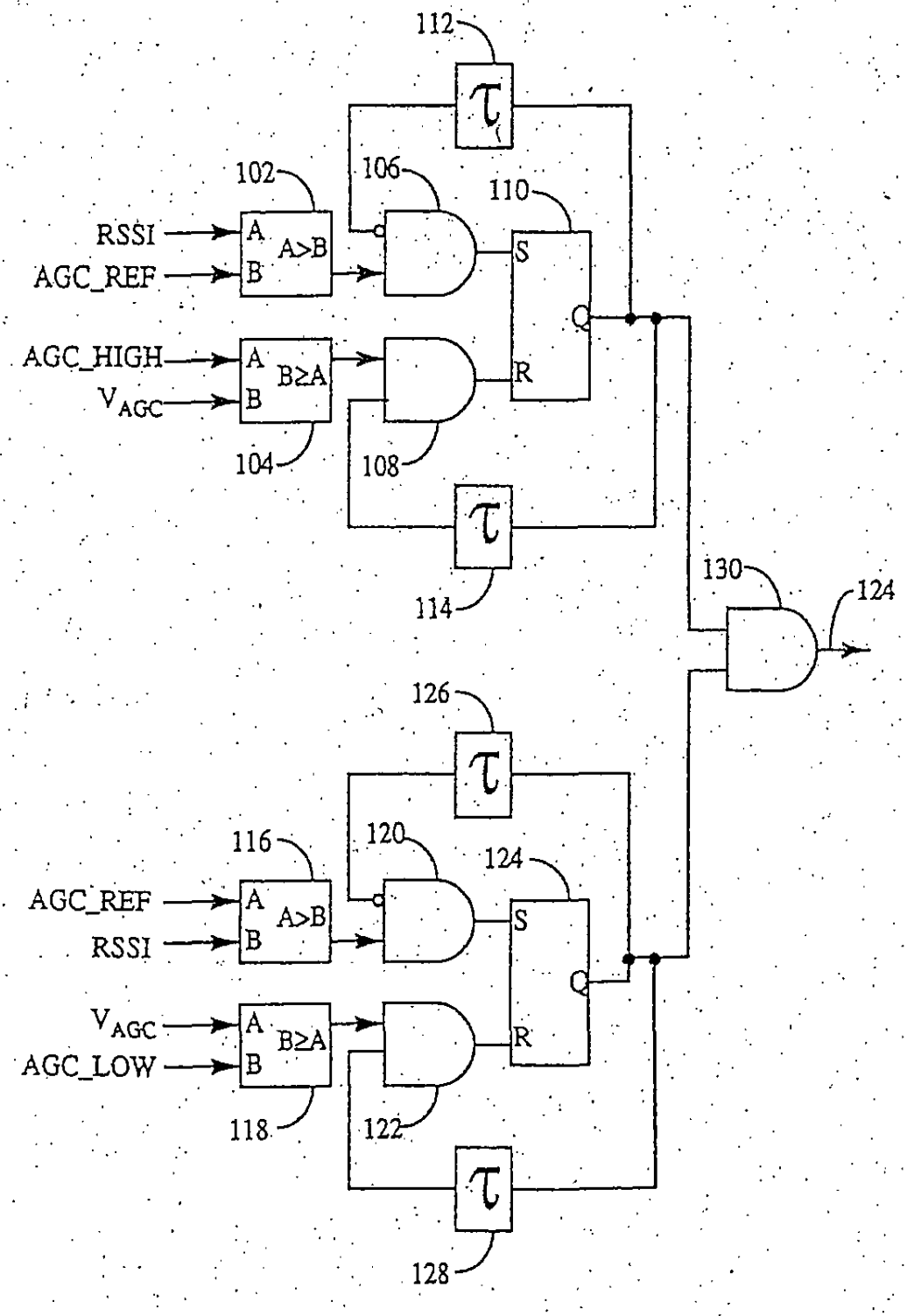

112
τ
102
106
110
RSSI
AGC_REF
A
B
A>B
S
R
AGC_HIGH
V_AGC
B≥A
104
108
τ
114
130
124
126
τ
116
120
124
AGC_REF
RSSI
A>B
S
R
V_AGC
AGC_LOW
B≥A
118
122
τ
128

FIG. 5

Ex. B-6

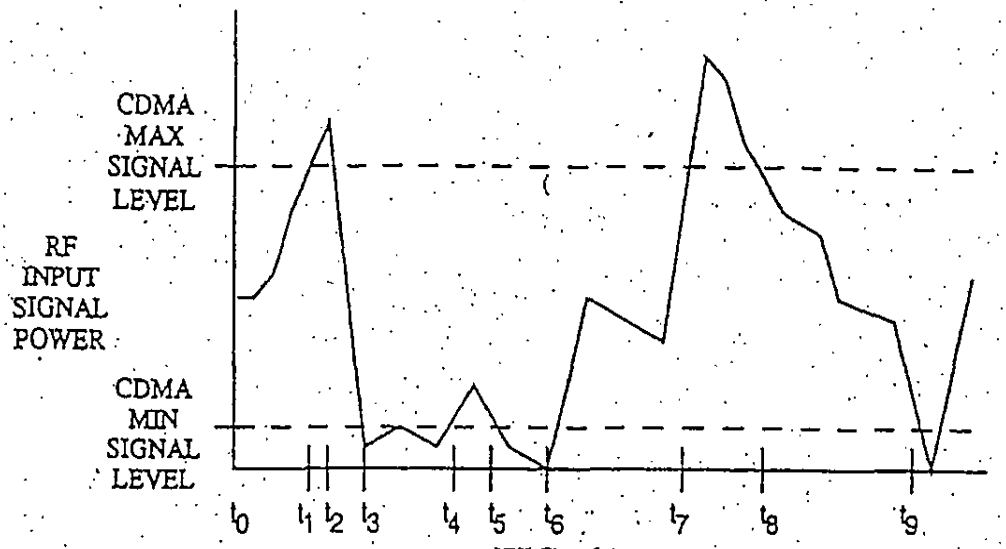


FIG. 6A

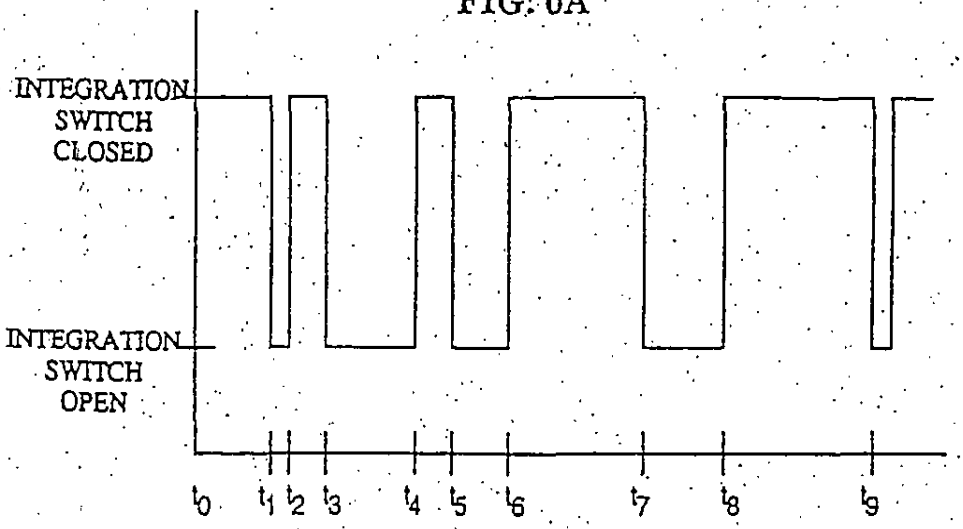


FIG. 6B

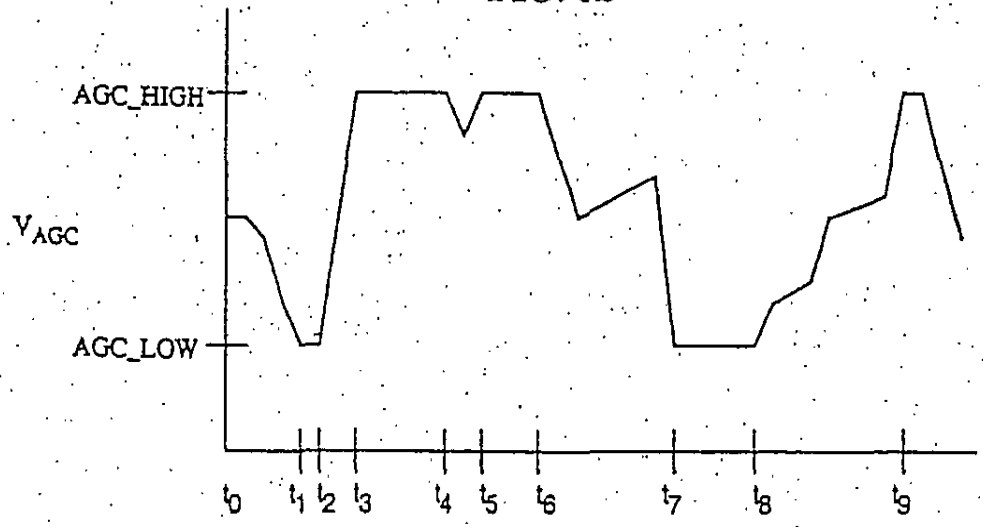


FIG. 6C

Ex. B-7

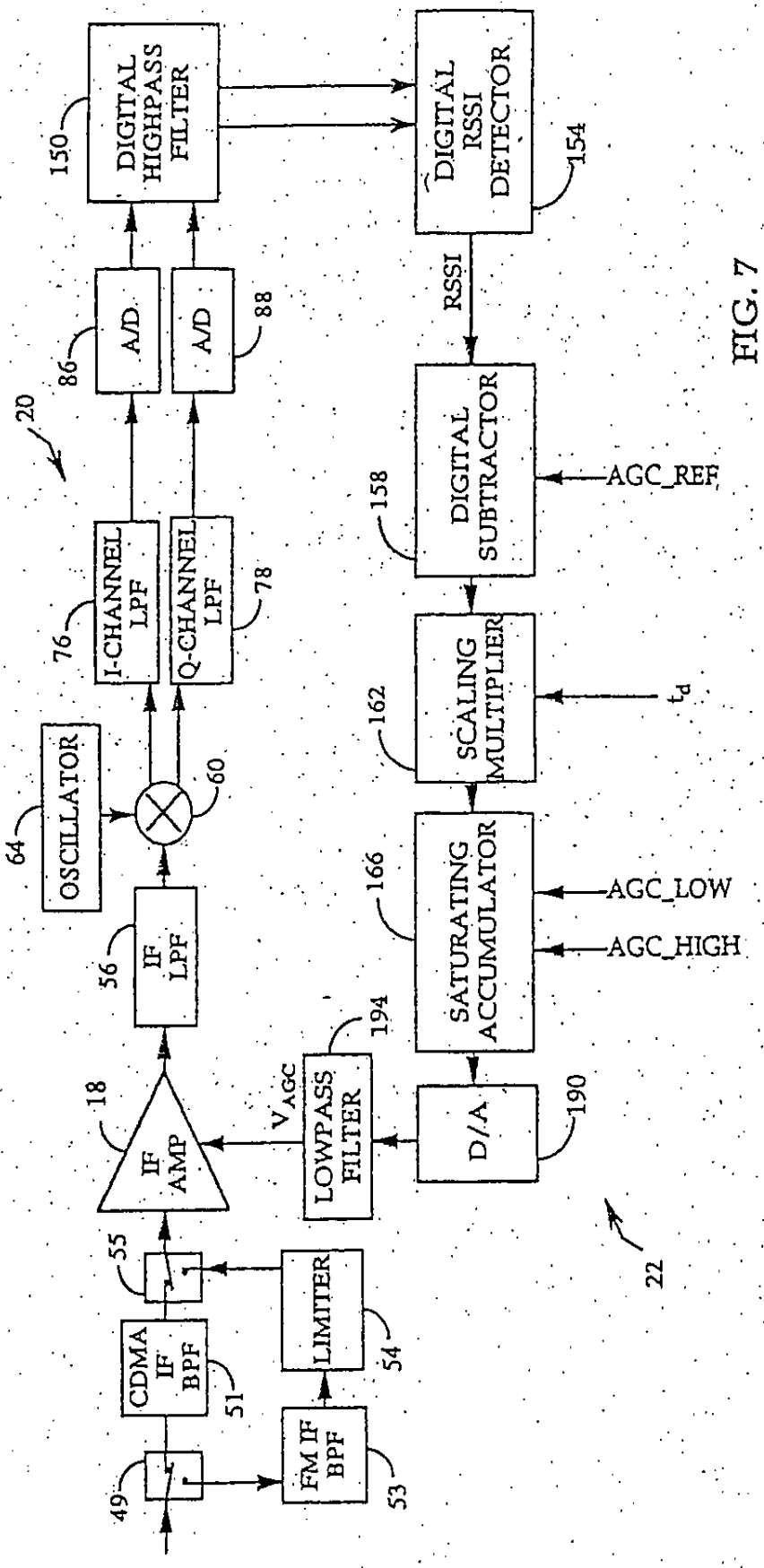

DIGITAL HIGHPASS FILTER
150
DIGITAL RSSI DETECTOR
154
RSSI
A/D
86
A/D
88
20
DIGITAL SUBTRACTOR
158
AGC_REF
I-CHANNEL LPF
76
Q-CHANNEL LPF
78
SCALING MULTIPLIER
162
t_d
OSCILLATOR
64
60
SATURATING ACCUMULATOR
166
AGC_LOW
AGC_HIGH
IF LPF
56
LOWPASS FILTER
194
V_{AGC}
D/A
190
IF AMP
18
22
55
LIMITER
54
CDMA IF BPF
51
FM IF BPF
53
49

FIG. 7

Ex. B-8

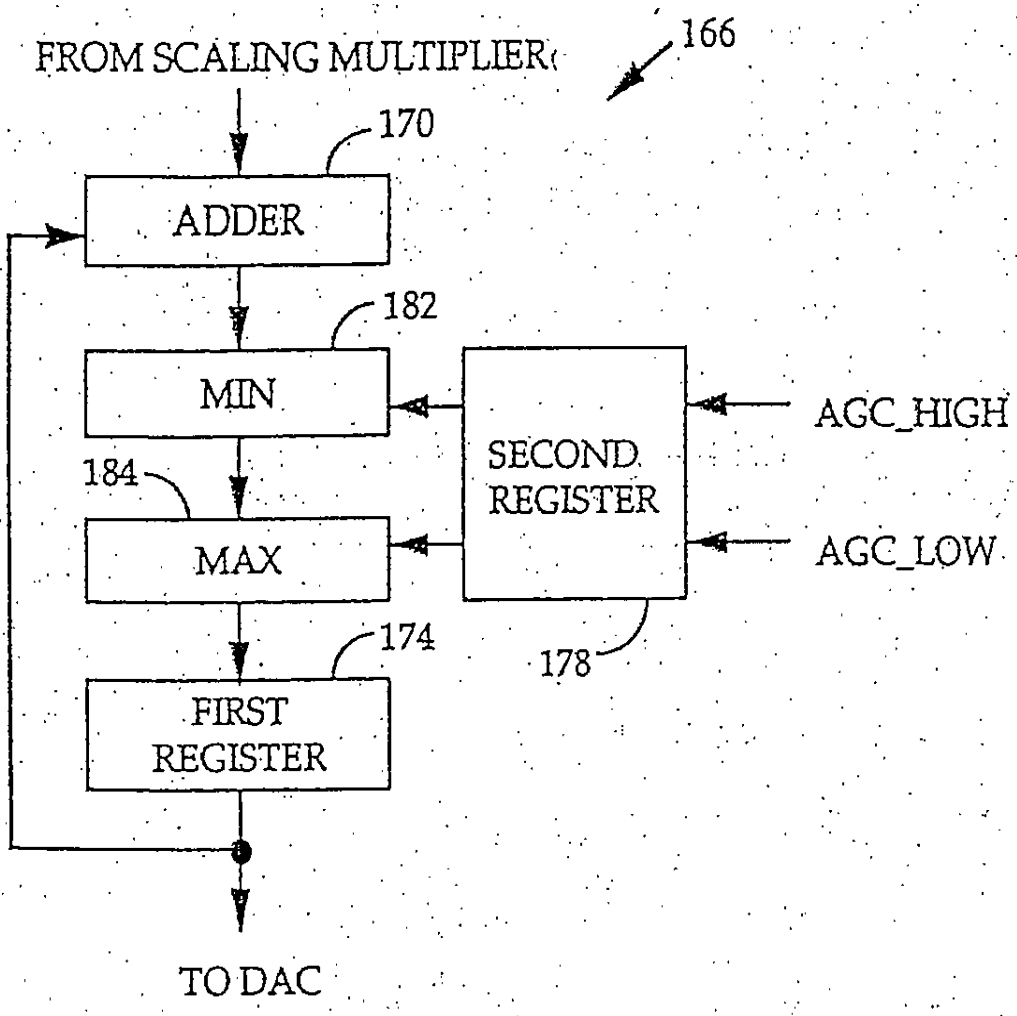

FROM SCALING MULTIPLIER
166
170
ADDER
182
MIN
184
MAX
174
FIRST REGISTER
SECOND REGISTER
178
AGC_HIGH
AGC_LOW
TO DAC

FIG. 8

Ex. B-9

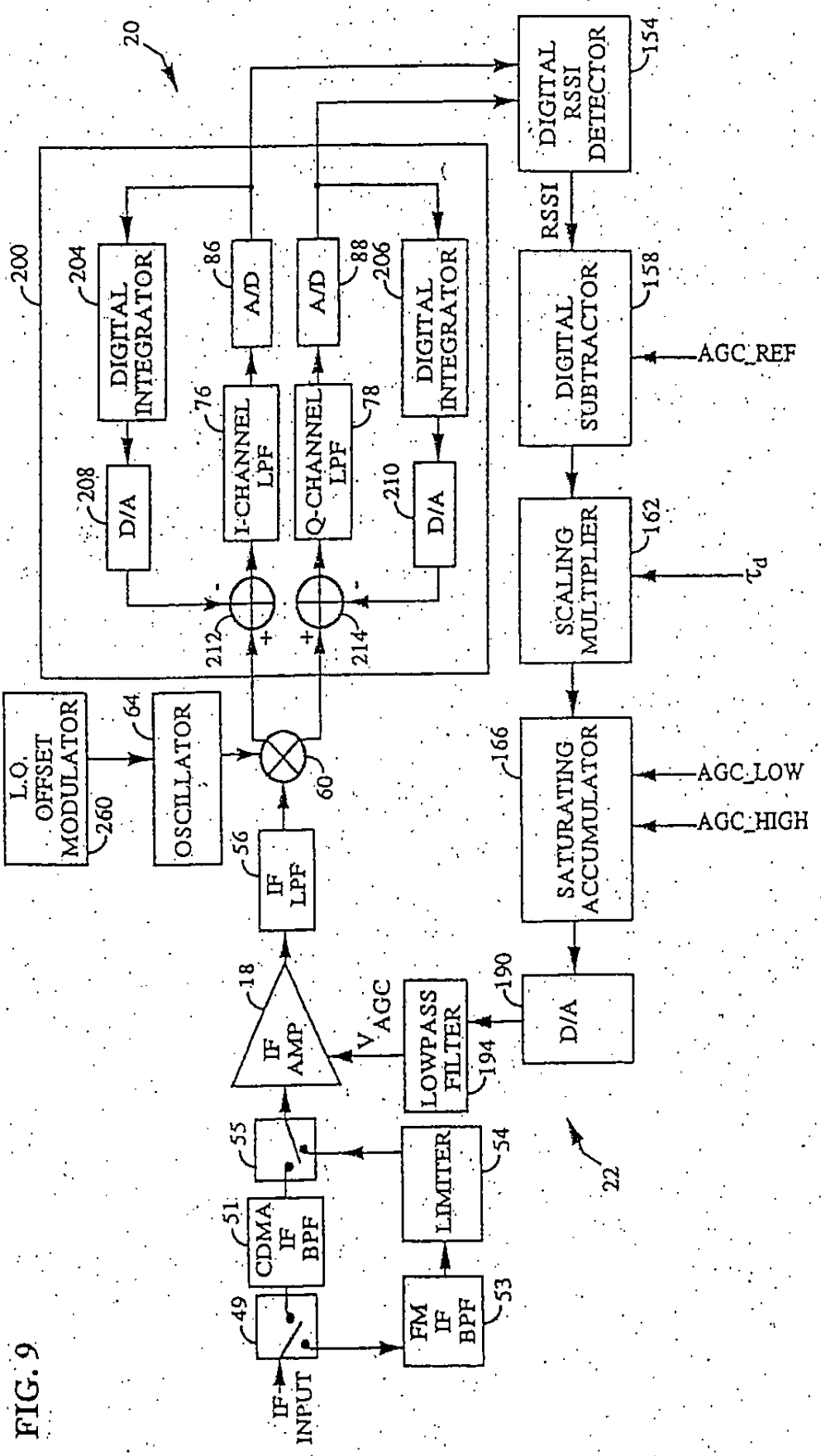

20
DIGITAL RSSI DETECTOR
154
RSSI
200
204
DIGITAL INTEGRATOR
86
A/D
88
A/D
206
DIGITAL INTEGRATOR
DIGITAL SUBTRACTOR
158
AGC_REF
208
D/A
76
I-CHANNEL LPF
78
Q-CHANNEL LPF
210
D/A
212
214
SCALING MULTIPLIER
162
τ_d
L.O. OFFSET MODULATOR
260
64
OSCILLATOR
60
166
SATURATING ACCUMULATOR
AGC_LOW
AGC_HIGH
56
IF LPF
18
IF AMP
V_{AGC}
LOWPASS FILTER
194
190
D/A
55
LIMITER
54
22
51
CDMA IF BPF
49
FM IF BPF
53
IF INPUT

FIG. 9

Ex. B-10

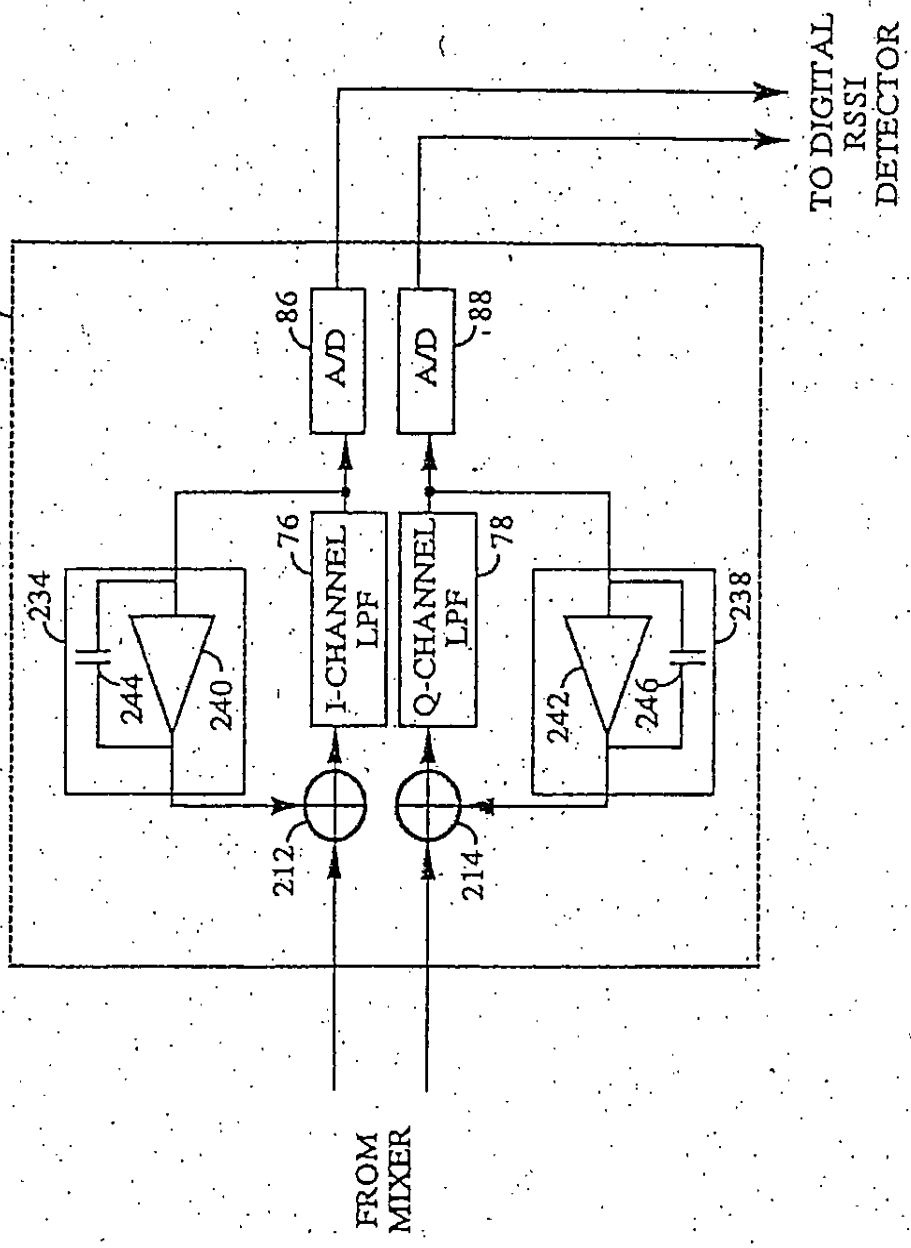

TO DIGITAL RSSI DETECTOR
230
86
A/D
88
A/D
76
I-CHANNEL LPF
78
Q-CHANNEL LPF
234
244
240
242
246
238
212
214
FROM MIXER

FIG. 10

Ex. B-11

METHOD AND APPARATUS FOR AUTOMATIC GAIN CONTROL AND DC OFFSET CANCELLATION IN QUADRATURE RECEIVER

This is a Continuation of application Ser. No. 08/235,812, filed Apr. 28, 1994 now abandoned.

BACKGROUND OF THE INVENTION

I. Field of the Invention

The present invention relates generally to RF receivers using quadrature demodulation. More particularly, the present invention relates to a novel method and apparatus for providing automatic gain control, out-of-band signal rejection, and D.C. offset cancellation within a digital receiver.

II. Description of the Related Art

In analog receivers, such as are used in narrowband FM cellular communication systems, FM demodulators are employed to extract information encoded in the phase of an incident waveform. Existing FM demodulators often include an analog frequency discriminator preceded by an analog limiter, with the limiter serving to constrain the input signal power to a constant level. In this way maximum signal to noise ratio is maintained at the input to the frequency discriminator over the full dynamic range of the FM input signal. However, such an analog signal processing technique generally involves extensive signal filtering, and frequently is implemented using a large number of discrete components. Moreover, it has been demonstrated that improved performance may be achieved using linear digital waveform demodulation rather than analog demodulation. Unfortunately, conventional demodulation techniques are often not applicable to digital receivers, since clipping of the received signal would result in corruption of the data derived therefrom.

A digital receiver for receiving a digitally modulated information signal will generally include a variable gain amplifier with a gain adjusted by a control signal. The process of adjusting the gain of a received signal using a control signal is called Automatic Gain Control (AGC). Typically in digital receivers, the AGC process involves measurement of an output signal power of the variable gain amplifier. The measured value is compared with a value representing the desired signal power and an control signal for the variable gain amplifier is generated. The error value is then used to control amplifier gain so as to adjust the signal strength to coincide with the desired signal power. To effect digital demodulation with an optimal signal to noise ratio, automatic gain control is used to hold the magnitude of the baseband waveforms dose to the full dynamic range of the baseband analog to digital converters. This generally requires, however, that automatic gain control be provided over the full dynamic range of the received signal power.

In the cellular environment, a digital receiver may receive a signal which experiences rapid and wide variations in signal power. In digital receivers such as are used in a code division multiple access (CDMA) and Time Division Multiple Access (TDMA) mobile cellular telephone, it is necessary to control the power of the demodulated signal for proper signal processing. However, in digital receivers to be both CDMA or TDMA compatible and conventional FM compatible, i.e., dual-mode digital/FM receivers, it is necessary to provide power control of both wideband CDMA (or TDMA) signals and narrowband FM signals. The control process is complicated by the differing dynamic ranges

associated with the received FM and CDMA signal power. That is, the magnitude of received FM signals may vary over a dynamic range greater than 100 dB, whereas CDMA systems typically result in a more limited dynamic range, i.e., approximately 80 dB.

The provision of separate AGC circuitry for each mode increases the hardware complexity and expense of such receivers. Accordingly, it would be desirable to provide AGC circuitry capable of operating both upon narrowband, wide-dynamic range FM signals, as well as upon wideband CDMA signals of more limited dynamic range.

It would also be desirable to provide digital AGC in inexpensive receivers utilizing analog to digital (A/D) converters with limited dynamic range. Again, because FM signals within cellular systems may vary more than 100 dB and relatively inexpensive 8-bit A/D's are limited to a dynamic range of approximately 48 dB, a cost effective AGC implementation should be capable of controlling the gain of the portion of the receiver preceding the A/D converters so as to control the signal's dynamic range at the A/D converter. The alternative is to employ expensive A/D converters having greater dynamic range, thereby increasing the cost of the receiver or to increase the AGC range of the analog portion of the radio which is very difficult and costly.

It is therefore an object of the present invention to provide a novel and improved AGC circuit which incorporates the desirable features mentioned above, and which, as is described hereinafter, also realizes certain other advantages relative to conventional AGC techniques.

In standard FM cellular telephones, the AGC function is performed by a circuit called a limiter. When a limiter is used, out-of-band signal rejection can only be done using intermediate frequency (IF) filters. Although the requisite signal rejection capability may be achieved through the use of ceramic IF filters, these tend to be relatively large and expensive. Smaller and less expensive IF filters are generally incapable of being realized so as to possess the desired signal rejection characteristics, and hence are generally not employed in FM cellular telephone receivers.

As is well known, recent advances in integrated circuit (IC) technology have made possible the realization of active baseband filters which are quite small and inexpensive compared to IF filters. It follows that it would be desirable to employ active IC baseband filters to effect significant out-of-band signal suppression, thereby allowing smaller and less expensive IF filters to be used to provide any additional required signal rejection. In an active filter, the higher the gain—the better rejection that is possible. But the higher the gain, the more susceptible the system to unwanted D.C. offsets. Suppression of such D.C. offsets is desirable to maximize the available signal dynamic range, minimize offset induced distortion in the baseband demodulated signal and minimize offset induced errors in baseband signal strength estimates.

In standard digital communications systems such as quadrature phase shift keying (QPSK), used in standard CDMA communication systems (and some TDMA systems), or binary phase shift keying (BPSK), information from the waveform is recovered by downconversion of the signal to baseband frequency centered about D.C. In this case D.C. offsets are easily removed, since for QPSK and BPSK, the carrier is generally suppressed by the transmitter anyway. Hence at baseband, a D.C. notch can be used.

However, for constant amplitude modulations such as FM and continuous phase FSK (which are used in FM cellular telephone systems such as AMPS) and Gaussian Minimum

Ex. B-12

Shift Keying (GMSK) (used in some TDMA systems), the carrier must be preserved in order to demodulate the received signal.

The employment of active baseband IC filters leads to the necessity of providing some mechanism for suppression of undesired D.C. offsets. The IF processing chain of conventional digital cellular telephone receivers typically includes a local oscillator (L.O.) having a frequency selected such that the carrier frequency is downconverted to D.C., and a simple D.C. notch filter is used to remove unwanted D.C. offsets. If an FM, FSK, or GMSK signal is processed by such an IF processing chain, then the D.C. offset suppression will not only remove unwanted D.C. components, but also critical phase and amplitude information at the carrier frequency. That is, in FM cellular telephone systems significant amplitude and phase information is present at the carrier frequency, and performance will be adversely affected if such information is destroyed.

However, there are two narrow bands of frequencies in between the carrier frequency F_c and F_c+F_1 and between F_c and F_c-F_1 (where F_1 is the lowest frequency expected in the demodulated spectrum, typically F_1=300 Hz for FM cellular) which can be suppressed without adversely affecting the demodulated signal. Although minimal voice information is carried at intermodulation products at frequencies close to the carrier frequency, such products are uncommon and of relatively short duration. Accordingly, the suppression of only the low-frequency intermodulation products after baseband downconversion does not usually result in the loss of appreciable voice information. Similarly, in FSK and GMSK systems, very little signal power is present below F_1=(symbol rate)/100, so again the frequency band between F_c and F_c+F_1 may be suppressed without degradation of the digital data.

It is therefore a further object of the present invention to provide quadrature receiver in which high-gain/highly selective active baseband filters may be employed without causing the loss of carrier frequency information.

SUMMARY OF THE INVENTION

The present invention is a novel automatic gain control method and apparatus for controlling signal power of a received RF signal over a wide dynamic range. In a preferred implementation the automatic gain control apparatus may be adjusted to provide a desired control response to various fading characteristics of the received RF signal. In applications where the signal of interest is a suppressed carrier digital format such as BPSK or QPSK (for CDMA Digital Cellular) or a constant envelope continuous-phase format such as GMSK, FSK, or FM (used in AMPS cellular phase system), the apparatus of the present invention is capable of providing the necessary gain control, out-of-band signal rejection, and downconversion to baseband, with no D.C. offset.

In accordance with the present invention an automatic gain control (AGC) apparatus for a dual mode receiver is disclosed. The AGC apparatus includes an adjustable gain amplifier having an input port for receiving an input signal, a control port for receiving a gain control signal, and an output port for providing an output signal. A downconverter coupled to the output port serves to translate the frequency of the output signal to a baseband frequency, thereby producing a baseband signal. In a preferred implementation the downconverter is operative to map the carrier frequency of the received signal of the output signal to a baseband frequency offset by a predetermined margin from D.C. A D.C. feedthrough suppression loop, disposed to receive said baseband signal, suppresses D.C. feedthrough signals produced by the downconverter, hence providing a compensated baseband signal.

The AGC apparatus further comprises means for generating a received power signal based on the power of the output signal. A saturating integrator compares the received power signal to a reference signal and produces the gain control signal by integrating or by refraining from integration based on values of the reference, received power signal, and gain control signals.

BRIEF DESCRIPTION OF THE DRAWINGS

The features, objects, and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters identify correspondingly throughout and wherein:

FIG. 1 illustrates in block diagram form an exemplary application of the automatic gain control apparatus (AGC) of the present invention;

FIG. 2 illustratively represents the gain of an AGC amplifier as a function of the gain control voltage;

FIG. 3 shows an exemplary embodiment of the automatic gain control apparatus of the invention which includes a control loop implemented in analog form;

FIGS. 4A and 4B illustratively represent the voltage and power transfer characteristics, respectively, associated with an exemplary implementation of a signal limiter included within the inventive gain control apparatus;

FIG. 5 depicts an exemplary implementation of decision logic used to govern operation of an integration control switch;

FIGS. 6A–6C are timing diagrams illustrative of the operation of the AGC apparatus of the invention;

FIG. 7 shows a preferred embodiment of the AGC apparatus of the invention including a digital realization of the control loop;

FIG. 8 depicts an exemplary implementation of a digital saturating accumulator included within the integrator of FIG. 7;

FIG. 9 shows an alternately preferred embodiment of the AGC loop of invention which includes a D.C. feedthrough suppression loop; and

FIG. 10 provides a block diagram representation of an analog D.C. feedthrough suppression loop.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In a digital receiver, such as used in a code division multiple access (CDMA) portable cellular communications device, it is necessary to set the power of the processed signal to a constant level. In the cellular environment, a receiver may receive a signal which experiences rapid and wide variations in signal power. In order to properly process the digital data contained within the received signal the signal power must be controlled within the receiver. In a dual-mode digital receiver, e.g., a digital receiver capable of processing both CDMA (or TDMA) and standard FM signals, the received signal dynamic range will vary as a function of the selected operative mode. Accordingly, an automatic gain control apparatus for a digital receiver is

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disclosed which is capable, in each of its operative modes, of compensating for variation in received signal power in either environment.

FIG. 1 illustrates in block diagram form an exemplary application of the automatic gain control apparatus of the present invention. In FIG. 1, the automatic gain control apparatus is implemented in the transceiver of a CDMA portable cellular telephone 10. Telephone 10 may be a dual mode, i.e. CDMA (or TDMA) and conventional FM compatible. The automatic gain control apparatus of the present invention is capable of providing power control of both wideband CDMA (or TDMA) signals and narrowband FM signals. The compatibility of such circuitry to operate on both wideband and narrowband signals provides cost, component and power savings for the receiver.

Telephone 10 includes antenna 12 for receiving RF signals, including CDMA or FM communication signals, transmitted from a base station. Antenna 12 couples the received signals to duplexer 14 which provides the received signals to the receiver portion of telephone 10. Duplexer 14 also receives CDMA or FM communication signals from a transmitter portion of telephone 10 for coupling to antenna 12 and transmission to a base station.

The received signals are output from duplexer 14 to downconverter 16 where the RF signals are converted to a lower frequency range and are provided as corresponding intermediate frequency (IF) signals. The IF signals from downconverter 16 are provided to automatic gain controlled IF amplifier 18. The IF signals are amplified at a gain level determined by an AGC signal (V_{AGC}) which is also provided to amplifier 18. Amplifier 18 is capable of providing linear control of gain over a high dynamic range, such as in excess of 80 dB, on the basis of V_{AGC}. Amplifier 18 may be of a design described in, for example, U.S. Pat. No. 5,099,204, entitled "LINEAR GAIN CONTROL AMPLIFIER", and assigned to the Assignee of the present invention.

In the above-referenced U.S. Pat. No. 5,099,204, a compensation circuit is employed to achieve a desired dynamic range of linear control. In particular implementations such control may be provided by the amplification circuit in the absence of assistance from a compensation circuit. Included among such implementations are those, for example, in which several amplification stages are arranged in cascade. Similarly, the availability of a high-voltage power supply may eliminate the need for a compensation circuit.

The gain controlled IF signals are output from amplifier 18 to a second frequency downconverter, downconverter 20, where the IF signals are converted to a lower frequency range and are provided as corresponding in-phase and quadrature-phase baseband signals I_{BB} and Q_{BB}. In the embodiment shown in FIG. 1, the baseband signals in the CDMA mode of operation are I and Q samples of encoded digital data which are output for further phase demodulation and correlation. In a dual mode receiver, downconverter 20 also frequency downconverts FM signals so as to provide baseband FM in-phase and quadrature-phase signals, which are further phase/frequency demodulated into an audio output signal.

Detector 25 measures the strength of the signals output by downconverter 20 and generates a corresponding received signal strength indication (RSSI) signal. The RSSI signal, along with an AGC reference signal (AGC_REF) supplied by a controller (not shown), are provided to a saturating integrator 22. The AGC_REF signal corresponds to a desired signal strength level for the baseband signals. The controller also provides AGC limit low (AGC_LOW) and AGC limit high (AGC_HIGH) reference signals to saturating integrator 22. The AGC_HIGH and AGC_LOW signals correspond to limits on the magnitude of a gain control signal (V_{AGC}) provided to a control port of amplifier 18 by saturating integrator 22.

FIG. 2 illustratively represents the gain of amplifier 18 as a function of the gain control voltage. Referring to FIG. 2, the gain of amplifier 18 is seen to nonlinearly taper to relatively constant values for control voltages exceeding AGC_HIGH and less than AGC_LOW. In general, it will be desired to constrain the value of V_{AGC} to within the linear range between AGC_HIGH and AGC_LOW in order that the corresponding time constant of the control loop remain within an acceptable range. Deviation of the loop time constant from the acceptable range could result in significant loop control errors. In accordance with the invention, amplifier 18 is constrained to operate within a region of linear gain by saturating integrator 22 in order to prevent the performance degradation introduced by such loop control errors.

As is described below, saturating integrator 22 is operative to integrate the difference between the RSSI and AGC_REF signals when V_{AGC} is between AGC_HIGH and AGC_LOW. When presented with an input which would cause V_{AGC} to exceed AGC_HIGH or fall below AGC_LOW integrator 22 stops integrating and the gain control signal V_{AGC} is held constant at either AGC_HIGH or AGC_LOW, thereby improving control loop response as described above.

Referring again to FIG. 1, saturating integrator 22 receives the RSSI signal from detector 25, along with the AGC_REF signal from the controller. In order to provide accurate power control, in general it is necessary for the difference between the RSSI signal and the AGC_REF signal to be minimized. Saturating integrator 22 is used to provide this function in the AGC loop by forcing the difference to zero. For example, if the gain of the signal is too high, the RSSI signal will also be high as compared to AGC_REF. Until these signals are of equivalent magnitude, the integrator output signal V_{AGC} will continue to decrease the gain of amplifier 18.

It should be understood that the RSSI measurement can be made at various points in the processing of the received signal. Although FIG. 1 illustrates that the measurement is made after frequency downconversion by downconverter 20, the measurement can be made at any point in the signal processing chain following IF amplifier 18. The RSSI measurement will preferably be made subsequent to completion of signal filtering, thereby minimizing the measured spurious interference power. In using analog power control techniques for both the wideband and narrowband signals, the same power control circuitry can be used for both modes of operation.

With respect to a transmitter portion 30 of the portable telephone of FIG. 1, transmit power is also controlled. The V_{AGC} signal is again used to provide instantaneous control of transmit power in CDMA mode. The V_{AGC} signal is provided to the transmitter portion 30, along with various other control signals from the controller (not shown).

Referring now to FIG. 3, there is shown an exemplary embodiment of the automatic gain control apparatus of the invention which includes a partially analog implementation of saturating integrator 22. In FIG. 3, the saturating integrator includes operational amplifier (op amp) integrator 40 having a capacitive feedback network. In particular, integrator 40 receives the AGC_REF signal through resistor 42 at its non-inverting input, to which is also connected capaci-

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tor 43. When switch 44 is closed in response to control information provided by integrator decision logic 46, an RSSI signal output by RSSI detector 48 is received by integrator 40 through resistor 50. When switch 44 is held in an open position in response to control information from integrator decision logic 46, a capacitor 52 serves to hold the output (V_{AGC}) of integrator 40 constant at either AGC_HIGH or AGC_LOW. This prevents saturation of amplifier 18 when the magnitude of the IF input signal departs from a predefined dynamic range.

Again referring to FIG. 3, an embodiment of a switching arrangement is shown using RF switches 49 and 55. RF switches 49 and 55 couple CDMA IF bandpass filter 51 to IF amplifier 18 during CDMA mode as shown by the setting of the switches in FIG. 3. In FM mode, the position of RF switches 49 and 55 changes to couple FM IF bandpass filter 53 and limiter 54 to IF amplifier 18. FM IF bandpass filter 53 for rejecting out-of-channel interference defines the bandwidth of the FM signals provided through limiter 54 to amplifier 18. For example, in FM mode operation the FM IF filter 53 is designed to have a passband spanning approximately one cellular channel (e.g., 30 kHz), and a stopband extending significantly beyond (e.g., ±60 kHz) the IF center frequency. During CDMA mode operation the CDMA IF filter 51 is designed to reject out-of-channel interference and defines the bandwidth of the CDMA signals provided to amplifier 18. For example during CDMA mode, CDMA IF bandpass filter 51 may provide a passband commensurate with the chip rate of the baseband portion of the receiver (e.g. 1.26 MHz), and provide a predefined rejection bandwidth (e.g. 1.8 MHz). In an alternative embodiment, limiter 54 could be in the common path before IF amplifier 18.

Limiter 54 attenuates high power RF signals, which are principally received during FM mode operation. FM signals may exceed the maximum power of signals encountered during CDMA mode operation. In a preferred embodiment limiter 54 limits the input power to amplifier 18 to within the dynamic range, e.g., 80 dB, characteristic of CDMA operation. Limiter 54 allows the control range of the automatic gain control (AGC) loop of FIG. 3 to be designed on the basis of the expected CDMA dynamic range, thereby eliminating the need to provide separately calibrated AGC control loops for FM and CDMA mode operation.

FIG. 4A and 4B illustratively represent the voltage and power transfer characteristic, respectively, associated with an exemplary implementation of limiter 54. Referring to FIG. 4A and 4B, limiter 54 does not attenuate signals having voltage magnitudes less then a predefined maximum voltage Vm. The saturated power may be quantified as $P_{SAT}=Vm^2/2R_L$, where R_L denotes the input load impedance of amplifier 18. For input power in excess of P_{SAT}, the output signals power produced by limiter 54 is made to remain constant at approximately P_{SAT} by clipping the peak signal voltage to the voltage Vm. The value of P_{SAT} will be selected based on the maximum expected CDMA input power level. Accordingly, for example, high-power sinusoidal IF input signals ($Pin>P_{SAT}$), the output waveform produced by limiter 54 is truncated to a fixed amplitude but the fundamental frequency and phase information is not lost. The limiter induced harmonic distortion is removed by lowpass filter 56.

Low-pass filter 56, included within the downconverter 20, is designed to have a cut-off frequency larger than the frequency of the IF signal output by amplifier 18 in either CDMA mode or FM mode. As noted above, low-pass filter 56 is designed to attenuate harmonics of the IF signal output by amplifier 18 prior to downconversion to baseband in-phase (I) and quadrature phase (Q) components. High-power waveforms clipped by limiter 54 create unwanted harmonics. IF lowpass filter 56 removes the unwanted harmonics so that they are not converted to baseband along with the desired IF signal information. In an exemplary embodiment the type, order, and passband edge of filter 56 are selected to attenuate in the amplified IF signal produced by amplifier 18.

The filtered IF signal is provided to a first input of a mixer 60, while the other input of mixer 60 receives a locally generated reference signal from oscillator 64. Mixer 60 mixes the filtered IF signal with the reference signal to produce the I and Q baseband (quadrature) components on output lines 70 and 72, respectively. The mixer 60 is designed to map a frequency which is offset from the IF center frequency by a predefined margin, e.g. from 3 to 300 Hz, to the baseband D.C. frequency. Such a D.C. offset margin allows the automatic gain control loop of FIG. 3 to distinguish between an unmodulated FM signal (i.e., a continuous wave (CW) signal) from an input D.C. offset error. Specifically, mixer 60 will preferably be operative to produce an output frequency of approximately 100 Hz in response to an input CW signal at the mid-band IF frequency. In this way input D.C. offset errors tending to corrupt RSSI power measurements are removed by a D.C. notch filter 66 without attenuating CW signal information.

Referring again to FIG. 3, output lines 70 and 72 are respectively connected to baseband I and Q-channel lowpass filters (LPFs) 76 and 78. I and Q-channel LPFs 76 and 78 will preferably each be implemented so as to provide lowpass transfer functions exhibiting cutoff frequencies of 13 kHz and 630 kHz, respectively, during FM and CDMA mode operation. In an exemplary embodiment filters 76 and 78 each include a pair of I and Q-channel, one of which is employed during CDMA mode operation and the other during FM mode operation. The individual filters included within I and Q-channel LPFs 76 and 78 are switched into the baseband I and Q signal paths, respectively, in accordance with the selected mode of operation. In the preferred embodiment the system controller includes means for switching the filters included within the filter networks in accordance with the operative mode selected.

In addition to performing an anti-aliasing function for A/D converters 86 and 88, I and Q-channel LPFs 76 and 78 also provide out-of-band signal rejection. In the preferred embodiment, filters 76 and 78 have high gain, and high stop-band rejection. As a result, IF bandpass filter 51 and 53 can have less stop-band rejection, and therefore can be less expensive.

After filtering by the I and Q-channel LPFs 76, 78 and by D.C. notch filter 66, the resulting baseband I and Q signals are provided to RSSI detector 48. RSSI detector 48 provides an output RSSI signal indicative of measured signal power (in dB). The difference between the RSSI signal output by RSSI detector 48 and AGC_REF is integrated within saturating integrator 22 so as to produce the control voltage V_{AGC}.

Again referring to FIG. 3, the I and Q outputs of the I and Q-channel LPFs 76 and 78 are also provided to I and Q analog to digital (A/D) converters 86 and 88, respectively. A/D converters 86 and 88 operate to quantize the baseband I and Q signals for digital demodulation in the selected operative mode, i.e., either CDMA or FM. In the preferred embodiment the dynamic range of A/D converters 86 and 88 is selected to be sufficient to accommodate signals that exceed the control range of the AGC apparatus of IF amplifier 18. As was noted above with reference to FIGS. 2

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and 3, decision logic 46 within saturating integrator 22 constrains the control voltage V_{AGC} to within the range $AGC\_LOW<V_{AGC}<AGC\_HIGH$. This prevents amplifier 18 from saturating in a nonlinear operating region.

Accordingly, A/D converters 86 and 88 are designed to quantize input signals, without excessive distortion, whether or not integrator 40 is saturated. In the preferred embodiment, each of A/D converters 86 and 88 provides 6 to 8 bits of dynamic range. This dynamic range is sufficient to prevent degradation in the signal to noise ratio of the input to A/D converters 86 and 88 as compared to the signal to noise ratio of the quantized digital output of A/D converters 86 and 88 for any RF input level. For example, when V_{AGC} reaches AGC_LOW, limiter 54 constrains the amplitude of the IF signal. In this way, the signal level at the input of A/D converters 86 and 88 may exceed the level indicated by AGC_REF by only some fixed amount. Therefore, A/D converters 86 and 88 will continue to accurately quantize the baseband signals at the increased level.

Likewise the dynamic range of A/D converters 86 and 88 is sufficient to prevent degradation of the signal to noise ratio at low RF input signal levels. For example when V_{AGC} reaches AGC_HIGH and switch 44 opens, if the input RF signal continues to fall, the baseband signal level at the input of A/D converters 86 and 88 falls below the level indicated by AGC_REF. The decreased level of the signal input to A/D converters 86 and 88 results in less than full utilization of the device, i.e., some of the bits of the output of the A/D converters 86 and 88 are not used. For larger RF input signals, the entire dynamic range of the A/D converters 86 and 88 is utilized during the conversion process. Hence, the AGC apparatus of the invention enables a limited range AGC control loop to be used in demodulating signals spanning a substantially larger dynamic range than the control range of the IF amplifier 18.

FIG. 5 depicts an exemplary implementation of decision logic 46 operative to control the position of the switch 44. As shown in FIG. 5, the AGC_HIGH and V_{AGC} signals are presented to logical comparator 104. When V_{AGC} exceeds the level of AGC_HIGH, the output of comparator 104 becomes a logic level one (1). The output of comparator 104 is logically AND'ed with the output of flip-flop 110, which is at a logic level 1 due to the closed position of switch 44. The output of flip-flop 110 is delayed through delay element 114 to prevent excessive, spurious toggling of the position of switch 44. AND gate 108 and delay element 114 operate to prevent switch 44 from being opened until after a fixed period of time following its closure. The output of AND gate 108 transitions from low to high thus resetting the output of flip-flop 110 to a logic level 0 and producing a logic level 0 at the output of AND gate 130 and opening switch 44. When switch 44 is opened, the RSSI signal and AGC_REF signal are no longer forced by the loop to be equivalent. In the case when AGC_HIGH has been exceeded and the loop is opened, the RSSI signal indicates a smaller signal than AGC_REF and the output of logical comparator 102 becomes a logic level 0. When the RSSI signal exceeds the level of AGC_REF, the output of comparator 102 transitions high and the output of AND gate 106 also transitions high, thus setting the output of flip-flop 110 to logic level 1 and closing switch 44. Delay element 112 and AND gate 106 function similarly to delay 114 and AND gate 108, and prevent closure of switch 44 until it has been open for a predefined time period.

An analogous sequence of logical operations is executed when the level of the RF input signal exceeds the AGC range. When V_{AGC} falls below the level of AGC_LOW, the output of comparator 118 becomes a logic level 1. The output of comparator 118 is logically AND'ed with the output of flip-flop 124, which is at a logic level 1 when switch 44 is closed. The output of AND gate 122 then transitions from low to high, thus resetting the output of flip-flop 124 to a logic level 0. This causes a logic level 0 to appear at the output of AND gate 130, which results in the opening of switch 44. When switch 44 is opened, the RSSI signal is no longer forced by the loop to be equal to AGC_REF. Upon the loop being opened in this manner the RSSI signal will be larger than AGC_REF and the output of logical comparator 116 will be at logical level 0. When the RSSI signal becomes smaller than AGC_REF, the outputs of comparator 116 and AND gate 120 transition high. The transition sets the output of flip-flop 124 to logic level 1 and closes switch 44. Delay elements 126 and 128 and AND gates 120 and 122 function similarly to delay 114 and AND gate 108, and serve to prevent rapid toggling of switch 44 between open and closed positions.

The logical output of AND gate 130 can be considered an integration enable signal and is impressed upon a switch control line 124 connected to switch 44. In the preferred embodiment switch 44 is closed in response to the impression of a logical 1 upon control line 124, and is opened when a logical 0 is impressed thereupon. Integrator decision logic 46 thus controls when the difference between the RSSI and AGC_REF signals is integrated by integrator 40. In this way integrator decision logic 46 and integrator 40 cooperate to provide the V_{AGC}. The operation of the AGC apparatus of FIG. 3 may be described in greater detail with reference to the timing diagrams of FIGS. 6A–6C. In particular, FIGS. 6A and 6B respectively depict the time variation in the power of an exemplary RF signal and the corresponding state (open or closed) of switch 44 within saturating integrator 22. FIG. 6C shows the corresponding value of the gain control voltage (V_{AGC}) generated by integrator 40 in response to the RF input signal of FIG. 6A.

As is indicated by FIGS. 6A and 6C, over a first integration interval ($t_0<t<t_1$) the power of the RF input signal is confined to the AGC control range of the AGC loop, and accordingly $AGC\_LOW<V_{AGC}<AGC\_HIGH$ (FIG. 6C). At time $t=t_1$, integrator decision logic 46 determines that V_{AGC} has reached AGC_LOW, and consequently opens switch 44. Switch 44 remains open over the time interval $t_1<t<t_2$, during which time integrator 40 is prevented from integrating the difference between RSSI and AGC_REF. During this time the input of A/D converters 86 and 88 is constrained by limiter 54. At time $t=t_2$ the RF input signal power has again become less than the upper bound of the loop control range, which results in switch 44 being closed by integrator decision logic 46 and V_{AGC} exceeding AGC_LOW. Switch 44 then remains closed over a second integration interval ($t_2<t<t_3$) until the control voltage V_{AGC} reaches AGC_HIGH, at which time switch 44 is again opened by integrator decision logic 46. During this time the input of A/D converters 86 and 88 varies in response to changes in RF input signal level. In a similar manner switch 44 is closed by integrator decision logic 46 at times t_4, t_6 and t_8 in order to initiate third, fourth and fifth integration intervals.

Referring now to FIG. 7, there is shown a preferred embodiment of the AGC loop of the invention in which is included a digital realization of saturating integrator 22. In the embodiment of FIG. 7 digital highpass filter 150, rather than analog D.C. notch filter 66, is employed to remove the D.C. offset inherent in the baseband I and Q samples produced by A/D converters 86 and 88. The cutoff frequency

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of the digital highpass filter 150 is selected to be substantially less than the frequency offset introduced within mixer 60. In an alternate implementation of removal of the D.C. offset may be achieved by:

(i) separately determining averages of the baseband I and Q signal samples, and

(ii) subtracting the resultant D.C. component from each I and Q component prior to further processing.

Digital RSSI detector 154 will typically include a look-up table containing values of log power indexed as a function of the magnitudes of the baseband I and Q samples. Digital PSI detector 154 approximates log power, i.e., 10 LOG (I^2+Q^2), by determining the value of LOG(MAX{ABS(I), ABS(Q)}) and the value of a correction term. The operation MAX{ABS(I),ABS(Q)} produces an output value equivalent to the magnitude of the largest component of a given I/Q sample pair. In a particular implementation this output value serves as an index into a look-up table of log power. The output derived from the look-up table is then added to a correction term approximately equivalent to the difference between LOG (I^2+Q^2) and LOG(MAX{ABS(I),ABS(Q)}).

The received power estimate, i.e., the RSSI signal, produced by digital RSSI detector 154 is supplied to digital subtractor 158 along with the AGC_REF signal. The resulting error signal is then scaled in accordance with a desired loop time constant t_d by digital scaling multiplier 162. The loop time constant t_d is chosen in accordance with the expected fading characteristics of the RF input signal. Relatively short loop time constants (faster loop response) will generally be selected to enable tracking of signals exhibiting abrupt fading characteristics while slowing the loop response to a level that does not cause excessive overshoot or ringing given the delays introduced in the loop by filters and other elements.

In a preferred embodiment scaling multiplier 162 may be programmed to multiply the error signal from digital subtractor 158 by a first loop time constant in response to decaying RSSI signals, and to multiply by a second loop time constant when the value of the RSSI signal is increasing. This allows for further flexibility in tailoring the AGC loop response on the basis of the fading characteristics of the operational environment and minimizes loop overshoot.

Referring again to FIG. 7, scaled error signal generated by scaling multiplier 162 is provided to saturating accumulator 166. Saturating accumulator 166 operates to accumulate values of the scaled error signal into an aggregate error signal until the aggregate error signal reaches either AGC_HIGH or AGC_LOW. The value of the aggregate error signal is then held at either AGC_HIGH or AGC_LOW until a scaled error signal is received which, after combination with the existing aggregate error signal, results in an aggregate error signal within the range defined by AGC_HIGH and AGC_LOW.

FIG. 8 depicts an exemplary discrete time implementation of saturating accumulator 166, As is indicated by FIG. 8, the scaled error signal is provided to a first input of a digital adder 170. The scaled error signal is added within digital adder 170 to the aggregate error signal produced in the previous time step by saturating accumulator 166, where the aggregate error signal is stored in register 174. The values of AGC_HIGH and AGC_LOW provided by a system controller (not shown) are stored within second register 178. Minimum and maximum signal clippers 182 and 184, coupled to second register 178, constrain the value of the digital signal provided to first register 174 to within the range defined by AGC_HIGH and AGC_LOW.

The digital implementation of highpass filter 150, RSSI detector 154 and saturating integrator 22 depicted in FIGS. 7 and 8 offers several advantages relative to corresponding analog realizations. For example, the digital components utilized therein are not susceptible to temperature drift, and allow the integration time constant to be adjusted in accordance with expected signal fading conditions so as to expedite loop signal acquisition. In addition, a filter and integrator implemented in digital form occupy significantly less volume than a corresponding arrangement of discrete resistive and capacitive components.

It is also anticipated that the utilization of a digital RSSI detector and a digital saturating integrator will result in improved accuracy. In particular, during the period when the value of V_{AGC} is required to be maintained at either AGC_HIGH or AGC_LOW, capacitive discharge and the like associated with analog components will generally result in the value of V_{AGC} "drooping" from the desired level over a period of time. The digital implementation of the saturating integrator shown in FIGS. 7 and 8 does not exhibit the signal "droop" characteristic of analog implementations.

Referring again to FIGS. 7 and 8, the control signal stored within the first register 174 of saturating accumulator 166 is provided to digital to analog converter (DAC) 190. In a preferred embodiment the resolution of DAC 190 will be sufficient to provide an output analog AGC step size of less than 1 dB. Alternatively, a pulse width modulated (PWM) or pulse density modulated (PDM) output pulse sequence of 0,1 logic levels is produced in response to the control signal. PDM signaling is explained in U.S. Pat. No. 5,337,338, titled Pulse Density Modulation Circuit (Parallel to Serial) Comparing in a Nonsequential Bit Order assigned to the Assignee of the present invention. The average value of the output pulse sequence corresponds to the desired analog output voltage.

The analog output provided by DAC 190 is passed through lowpass filter 194 prior to being applied to the gain control port of IF amplifier 18. Lowpass filter 194 is designed to attenuate any spurious output produced by DAC 190.

Referring now to FIG. 9, there is shown an alternate preferred embodiment of the AGC loop of invention operative to advantageously suppress undesired D.C. offset signal components without simultaneously destroying carrier frequency signal information. The AGC loop of FIG. 9 bears substantial similarity to the AGC loop of FIG. 7, and hence like reference numerals are used in the representation of like circuit elements. As noted in the Background of the Invention, in receivers for digital modulation such as QPSK or BPSK, it is common for the frequency of the local oscillator (L.O.) within the IF processing chain to be selected such that the received carrier frequency is downconverted (i.e., mapped) to D.C. Again, however, subsequent baseband processing designed to suppress undesired D.C. feedthrough passed by mixer 60 also tends to destroy signal information centered about the received carrier which occurs for modulation schemes such as FM, and continuous-phase FSK.

In accordance with one aspect of the invention, the L.O. frequency of the oscillator 64 is selected such that the received carrier is mapped to a baseband frequency offset from D.C. by a predetermined margin. A D.C. feedthrough suppression loop 200 (FIG. 9) enables cancellation of undesired D.C. feedthrough while simultaneously preserving signal information at the received carrier frequency. In a preferred implementation the L.O. frequency is chosen to be offset by a small amount (e.g., 100 Hz) from the carrier frequency nominally resulting in downconversion of the received spectrum to baseband. It follows that the I and Q channel signal energy output by the mixer 60 at the prede-

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termined offset frequency (e.g., 100 Hz) corresponds to the information impressed upon the received carrier frequency. The downconverted spectrum, including carrier information, is passed to A/D converters 86 and 88 while undesired D.C. feedthrough from mixer 60 is suppressed. Although this process results in the attenuation of energy at the frequency spaced from the received carrier by the predetermined offset, in many applications (e.g., voice communication) the suppressed low frequency energy carries minimal usable signal information. Accordingly, the D.C. suppression loop 200 advantageously allows cancellation of extraneous D.C. feedthrough without destruction of information present at the received carrier frequency.

As is indicated by FIG. 9, the D.C. feedthrough suppression loop 200 includes I and Q channel digital integrators 204 and 206 having input ports operatively coupled to the outputs of I and Q-channel LPFs 76 and 78 through A/D converters 86 and 88, respectively. In the embodiment of FIG. 9 the integrators 204 and 206 are respectively disposed to integrate the digital outputs of A/D converters 86 and 88. The results of each integration are converted to analog signals by I and Q channel digital to analog converters (D/A) 208 and 210, which are seen to be respectively interposed between the digital integrators 204 and 206 and analog subtractors 212 and 214. The gain constants of digital integrators 204 and 206 may be selected such that integrators 204 and 206 are unresponsive to signal power at frequencies at 100 Hz and above. The resultant D.C. cancellation signals produced by integrators 204 and 206 are nominally equal to the undesired D.C. errors introduced in the signal path by mixer 60, I and Q-channels LPFs 76 and 78, and A/D converters 86 and 88. In this way it is ensured that the power level provided to A/D converters 86 and 88, and hence also to the RSSI circuit 154, is indicative of the power level actually received by saturating integrator 22. Hence, the D.C. feedthrough suppression loop 200 functions to maintain the integrity of the received power level even during elimination of undesired D.C. feedthrough.

Turning now to FIG. 10, there is shown an analog implementation of a D.C. feedthrough suppression loop 230 (which can be substituted in FIG. 9 in place of feedthrough suppression loop 200) operative to eliminate undesired D.C. feedthrough while simultaneously preserving the level of signal power supplied to digital RSSI detector 154. The L.O. frequency of the oscillator 64 (FIG. 9) is again selected such that the carrier frequency is mapped to a baseband frequency offset from D.C. by a predetermined margin. The D.C. feedthrough suppression loop 230, in a manner substantially similar to that described above with reference to the feedthrough suppression loop 200, enables cancellation of undesired D.C. feedthrough while simultaneously preserving signal information at the received carrier frequency. Specifically, by appropriately selecting the gains at integrators 234 and 238, the downconverted carrier information mapped to the offset frequency is passed to A/D converters 86 and 88. As discussed above, undesired D.C. feedthrough from mixer 60 is then suppressed by subtractors 212 and 214.

The D.C. feedthrough suppression loop 230 also operates to ensure that the baseband signal power provided to A/D converters 86 and 88, and hence to RSSI detector 154, is indicative of the signal power actually received, and is uncorrupted by extraneous D.C. signals.

In an exemplary embodiment it may be desired to modify the D.C. feedthrough suppression technique described above in order to accommodate the reception of received FM signals corresponding to "multi-tone" analog signals. More particularly, in certain applications the received FM signal may be representative of a "multi-tone" waveform comprised of a set of stationary, i.e., fixed-frequency, signal components, where each stationary component corresponds to the magnitude or pitch of a particular analog tone. This may require that the low-frequency intermodulation products created by interaction of the multiple FM signal components be preserved. Accordingly, if a static frequency offset is introduced by the L.O. oscillator 64, it is possible that particular intermodulation products will be mapped by mixer 60 to baseband D.C. (i.e., to the same baseband frequency at which may be present D.C. feedthrough). In this case it may prove difficult to distinguish between undesired D.C. feedthrough and useful signal information mapped by mixer 60 to baseband D.C. Since the D.C. feedthrough suppression loops 200 and 230 will generally be designed to cancel substantially all D.C. signal energy produced by mixer 60, it is conceivable that useful intermodulation information could be eliminated along with the undesired D.C. feedthrough.

Referring again to FIG. 9, in accordance with another aspect of the invention this difficulty is addressed by providing an L.O. offset modulator 260 operative to introduce time varying variation into the D.C. offset applied to the nominal L.O. frequency. The term "nominal" L.O. frequency refers to that frequency at which the received center carrier frequency is mapped to baseband D.C. by mixer 60. Because in this case the L.O. offset frequency supplied to mixer 60 is not static, but instead varies over a predefined range, received stationary components will not be continuously mapped to baseband D.C. but will instead be mapped to baseband frequencies based on variation in the L.O. offset. Hence, useful low-frequency intermodulation products may be distinguished from undesired D.C. feedthrough, because D.C. feedthrough remains at baseband D.C. notwithstanding variation in the frequency offset applied to the L.O. oscillator signal. Accordingly, the offset modulator 260 allows the D.C. feedthrough suppression loop to eliminate undesired D.C. feedthrough while simultaneously preserving certain stationary signal information.

The modulated frequency offset introduced to the nominal L.O. frequency may be characterized in terms of a mean offset frequency, a minimum and a maximum offset frequency, and an offset modulation frequency (i.e., the rate at which the offset is varied between the minimum and maximum offset frequencies). For example, in a particular embodiment the mean frequency offset is selected to be 100 Hz, the minimum and maximum offsets are respectively chosen to be 50 Hz and 150 Hz, and the offset modulation frequency is set at 10 Hz.

If the described embodiment is used to build an FM FSK, or GMSK receiver, then the output of A/D converters 86 and 88 is fed to an FM demodulator (not shown). The modulation signal introduced by L.O. offset modulator 260 (10 Hz in preferred embodiment) can be easily removed after the FM demodulation by a digital high pass filter with a cutoff frequency somewhat higher than L.O. offset modulators 260's maximum offset frequency without affecting audio quality.

The previous description of the preferred embodiments is provided to enable any person skilled in the art to make or use the present invention. The various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without the use of the inventive faculty. Thus, the present invention is not intended to be limited to the embodiments shown herein but is to be

Ex. B-18

accorded the widest scope consistent with the principles and novel features disclosed herein.

We claim:

1. An automatic gain control apparatus including an adjustable gain amplifier, the adjustable gain amplifier having an input port for receiving an input signal, a control port for receiving a gain control signal, and an output port for providing an output signal, the automatic gain control apparatus comprising:

a downconverter coupled to said output port for downconverting frequency of said output signal to a baseband frequency so as to produce a baseband signal, said downconverter being operative to map a carrier frequency of said output signal to a baseband frequency offset by a predetermined margin from D.C.;

a D.C. feedthrough suppression loop, disposed to receive said baseband signal, for suppressing D.C. feedthrough signals produced by said frequency downconverter and for providing a compensated baseband signal;

means for generating a received power signal based on power of said compensated baseband signal; and

saturating integrator means for comparing said received power signal to a reference signal and for generating an error signal in response to a result of the comparison, said saturating integrator means including means for providing said gain control signal by selectively integrating said error signal based on values of said error and gain control signals.

2. The automatic gain control apparatus of claim 1 wherein said D.C. feedthrough suppression loop further includes:

a subtractor having a first input for receiving said baseband signal; and an output port operatively coupled to an input of a low-pass filter; and

an integrator having an integrator input port operatively coupled to an output port of said low-pass filter, and having an integrator output port operatively coupled to a second input of said subtractor.

3. The automatic gain control apparatus of claim 2 wherein said D.C. feedthrough suppression loop further includes:

an analog to digital converter coupled to said output port of said low-pass filter; and

a digital to analog converter interposed between said integrator output port and said second input of said subtractor.

4. The automatic gain control apparatus of claim 1 wherein said saturating integrator means includes first means for selectively enabling said error signal to be integrated only while magnitude of said gain control signal is less than a first predefined threshold, and second means for selectively enabling said error signal to be integrated only while magnitude of said gain control signal exceeds a second predefined threshold.

5. The automatic gain control apparatus of claim 1 wherein said downconverter includes:

a mixer having a first input port for receiving said output signal; and

a local oscillator connected to a second input port of said mixer wherein frequency of said local oscillator is selected such that said center frequency of said output signal mapped to said baseband frequency offset by said predetermined margin from D.C.

6. The automatic gain control apparatus of claim 5 wherein said downconverter includes an offset modulator circuit for varying said frequency of said oscillator circuit so as to vary said predetermined margin by which said center frequency of said output signal is mapped relative to D.C.

7. The automatic gain control apparatus of claim 6 wherein said downconverter includes a mixer coupled to said output port of said adjustable gain amplifier, said mixer being operative to downconvert said output signal to I and Q baseband signal components of said baseband signal.

8. The automatic gain control apparatus of claim 7 wherein said D.C. feedthrough suppression loop includes first and second low-pass filters for filtering said I and Q baseband signal components, respectively.

9. A method for automatic gain control using an adjustable gain amplifier, the adjustable gain amplifier having an input port for receiving an input signal, a control port for receiving a gain control signal, and an output port for providing an output signal, the method comprising the steps of:

downconverting frequency of said output signal to a baseband frequency so as to produce a baseband signal wherein a carrier frequency of said output signal is mapped to a baseband frequency offset by a predetermined margin from D.C.;

suppressing D.C. feedthrough signals accompanying said baseband signal so as to provide a compensated baseband signal;

generating a received power signal based on power of said compensated baseband signal; and

integrating selectively a difference between said received power signal and a reference signal based on values of said error and gain control signals.

10. An automatic gain control apparatus for compensating for variations in received signal power, the automatic gain control apparatus comprising:

an adjustable gain amplifier having an input port coupled to a received signal, an output port for generating an output signal having a frequency, and a control port for receiving a gain control signal;

a downconverter coupled to the output port for downconverting the frequency of the output signal to produce a baseband signal having a baseband frequency, the downconverter mapping a carrier frequency of the output signal to a baseband frequency offset by a predetermined margin from D.C.;

a filter, coupled to the downconverter, for removing D.C. offset errors and signal in the baseband signal to generate a filtered signal;

a power detector, coupled to the filter, for generating a power level signal in response to a power of the filtered signal; and

an integrator having a first input coupled to the power detector and a second input coupled to a reference signal, the integrator generating the gain control signal by selectively integrating a difference between the reference signal and the power level signal.

11. The automatic gain control apparatus of claim 10 and further including control logic for selectively enabling the difference to be integrated while a magnitude of the gain control signal is less than a first predetermined threshold and greater than a second predetermined threshold.

12. The automatic gain control apparatus of claim 10 wherein the downconverter is comprised of:

an intermediate frequency filter coupled to the output port of the adjustable gain amplifier;

an oscillator for generating a frequency reference signal;

a mixer, coupled to the oscillator and the intermediate frequency filter, for generating at least one baseband

Ex. B-19

component in response to the frequency reference signal and the output signal; and

at least one low pass filter, coupled to the mixer, for generating at least one lowpass transfer function from the at least one baseband component.

13. The automatic gain control apparatus of claim 12 wherein the apparatus operates in either a code division multiple access mode (CDMA) or a frequency modulated (FM) mode and the at least one low pass filter is comprised of a first filter for operation in the CDMA mode and a second filter for operation in the FM mode.

14. The automatic gain control apparatus of claim 11 wherein the integrator includes a switch controlled by the control logic, in a closed position the switch coupling the power level signal to an input of the integrator and, in an open position, a capacitor holding the integrator input at one of a plurality of predetermined voltage levels.

15. An automatic gain control apparatus for compensating for variations in received signal power, the automatic gain control apparatus comprising:

an adjustable gain amplifier having an input port coupled to a received signal, an output port for generating an output signal having a frequency, and a control port for receiving an analog gain control signal;

a downconverter, coupled to the output port, for downconverting the frequency of the output signal to produce at least one baseband signal having a baseband frequency, the downconverter mapping a carrier frequency of the output signal to a baseband frequency offset by a predetermined margin from D.C.;

at least one analog to digital converter, each coupled to a different baseband signal of the at least one baseband signal, each analog to digital converter generating a digital representation of the respective baseband signal;

a filter, coupled to the at least one analog to digital converter, for generating at least one filtered signal;

a power detector coupled to the filter, the power detector generating a power level signal in response to the at least one filtered signal;

an integrator, coupled to the power detector, for comparing the power level signal to a predetermined reference signal to generate an error signal, the integrator generating a digital gain control signal by selectively integrating the error signal in response to values of the error signal and the digital gain control signal; and

a digital to analog converter coupled between the integrator and the adjustable gain amplifier, the digital to analog converter generating the analog gain control signal from the digital gain control signal.

16. The apparatus of claim 15 wherein the integrator comprises:

a subtractor coupled to the power detector, the subtractor generating the error signal in response to a difference between the power level signal and the predetermined reference signal;

a scaling multiplier, coupled to the subtractor, that generates a scaled error signal by multiplying the error signal by a first constant when the power level signal is decreasing in value and multiplying by a second constant when the power level signal is increasing in value; and

an accumulator, coupled to the scaling multiplier, that generates the digital gain control signal by accumulating the scaled error signal, the accumulator holding the digital gain control signal at a minimum predetermined threshold when the accumulated scaled error signal decreases to the minimum predetermined threshold and the accumulator holding the digital gain control signal at a maximum predetermined threshold when the accumulated scaled error signal increases to the maximum predetermined threshold.

17. The apparatus of claim 15 and further including a lowpass filter coupling the digital to analog converter to the adjustable gain amplifier.

18. A method for compensating for variations in received signal power in an automatic gain control apparatus having an adjustable gain amplifier, the adjustable gain amplifier having an input port coupled to a received signal, an output port for generating an output signal having a frequency, and a control port for receiving a gain control signal, the method comprising the steps of:

downconverting the frequency of the output signal to produce a baseband signal having a baseband frequency;

generating a filtered signal by removing D.C. offset errors and signal in the baseband signal;

generating a power level signal in response to a power of the filtered signal; and

generating a gain control signal by selectively integrating a difference between the power level signal and a reference signal.

19. The method of claim 18 wherein the step of generating a gain control signal further includes integrating the difference only when the value of the gain control signal is greater than a minimum predetermined threshold and less than a maximum predetermined threshold.

20. A method for compensating for variations in received signal power in an automatic gain control apparatus having an adjustable gain amplifier, the adjustable gain amplifier having an input port coupled to a received signal, an output port for generating an output signal having a frequency, and a control port for receiving an analog gain control signal, the method comprising the steps of:

downconverting the frequency of the output signal to produce at least one baseband signal having a baseband frequency;

generating a digital representation of each respective baseband signal;

generating at least one filtered signal by filtering the digital representations of the at least one baseband signal;

generating a power level signal in response to the at least one filtered signal;

comparing the power level signal to a reference signal to generate an error signal;

generating a digital gain control signal by selectively integrating the error signal in response to values of the error signal and the digital gain control signal; and

converting the digital gain control signal to the analog gain control signal.

21. The method of claim 20 wherein the step of generating a digital gain control signal further includes integrating the error signal only when the value of the digital gain control signal is greater than a minimum predetermined threshold and less than a maximum predetermine threshold.

* * * * *

Ex. B-20

US005732341A

United States Patent [19]

Wheatley, III

[11] Patent Number: 5,732,341

[45] Date of Patent: Mar. 24, 1998

[54] METHOD AND APPARATUS FOR INCREASING RECEIVER IMMUNITY TO INTERFERENCE

[75] Inventor: Charles E. Wheatley, III, Del Mar, Calif.

[73] Assignee: QUALCOMM Incorporated, San Diego, Calif.

[21] Appl. No.: 522,467

[22] Filed: Aug. 31, 1995

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 357,951, Dec. 16, 1994, Pat. No. 5,722,063.

[51] Int. Cl.[6] H04B 1/10; H04G 3/20

[52] U.S. Cl. 455/234.1; 455/219; 455/232.1

[58] Field of Search 455/13.4, 63, 67.1, 455/219, 226.1, 226.2, 232.1, 240.1, 234.1, 245.1, 245.2, 250.1, 254, 268

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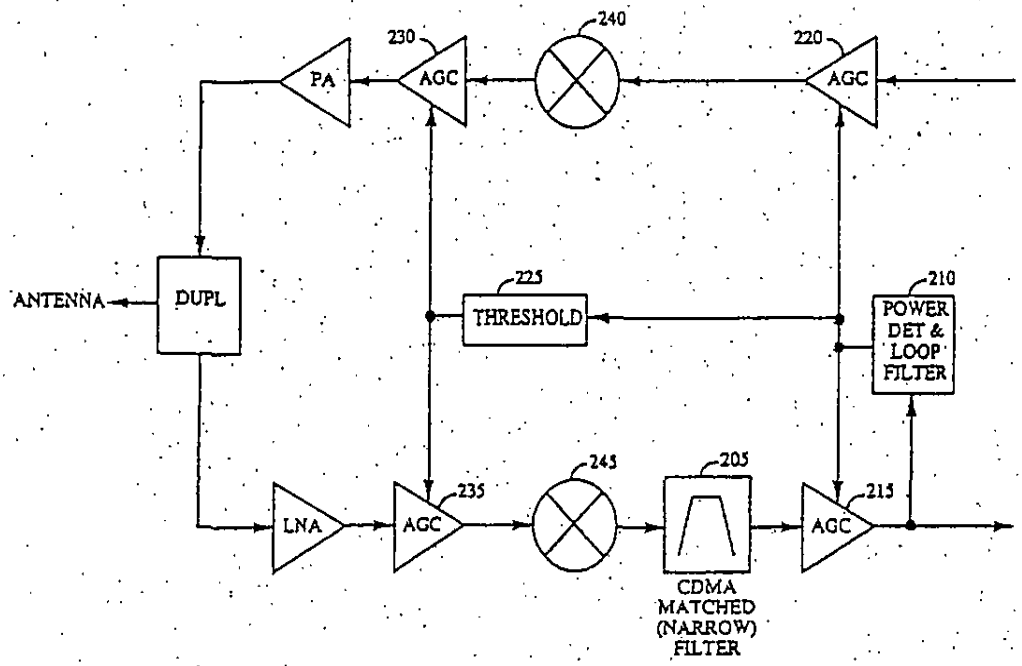
Primary Examiner—Leslie Pascal

Attorney, Agent, or Firm—Russell B. Miller; Roger W. Martin

[57] ABSTRACT

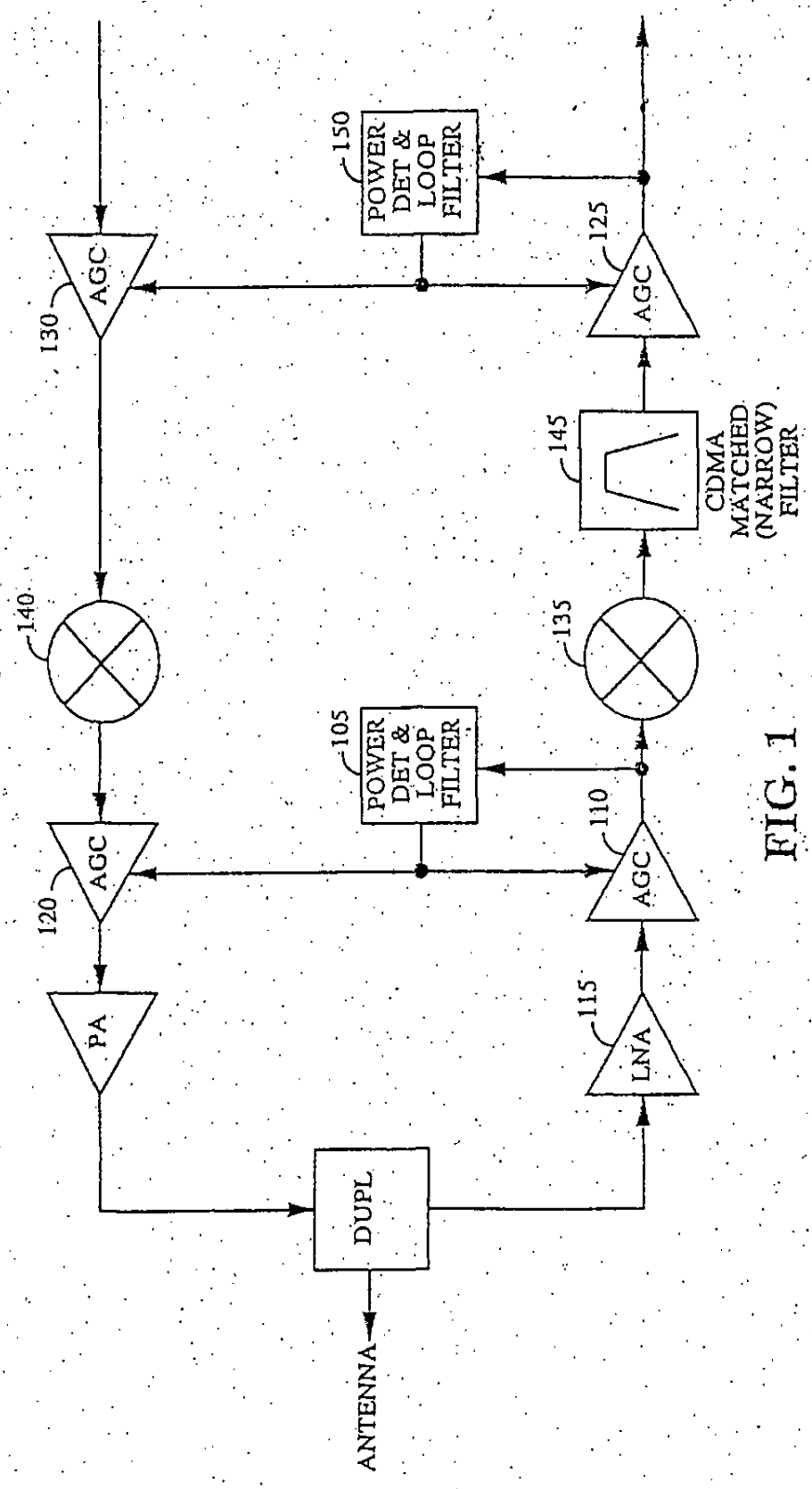
The process of the present invention adjusts the input gain by a predetermined amount. The receiver processing measures the gain change in the IF sisal power. If the change is less than the predetermined amount, the CDMA signal and jammers are below the noise floor and, therefore, the gain is increased. If the IF signal power change is equal to the predetermined amount, the CDMA signal is above the noise floor and the interference is minimal. Therefore, in this case, gain adjustment is not necessary, but increasing gain will improve sensitivity. If the IF signal power change is greater than the predetermined amount, the interference is evident and the gain is reduced to reduce the intermodulation products. This process is used until the receiver is operating at the best compromise between interference and noise figure.

20 Claims, 14 Drawing Sheets



Ex. D-1

Ex. C-1


150
POWER DET & LOOP FILTER
125
AGC
130
AGC
145
CDMA MATCHED (NARROW) FILTER
140
135
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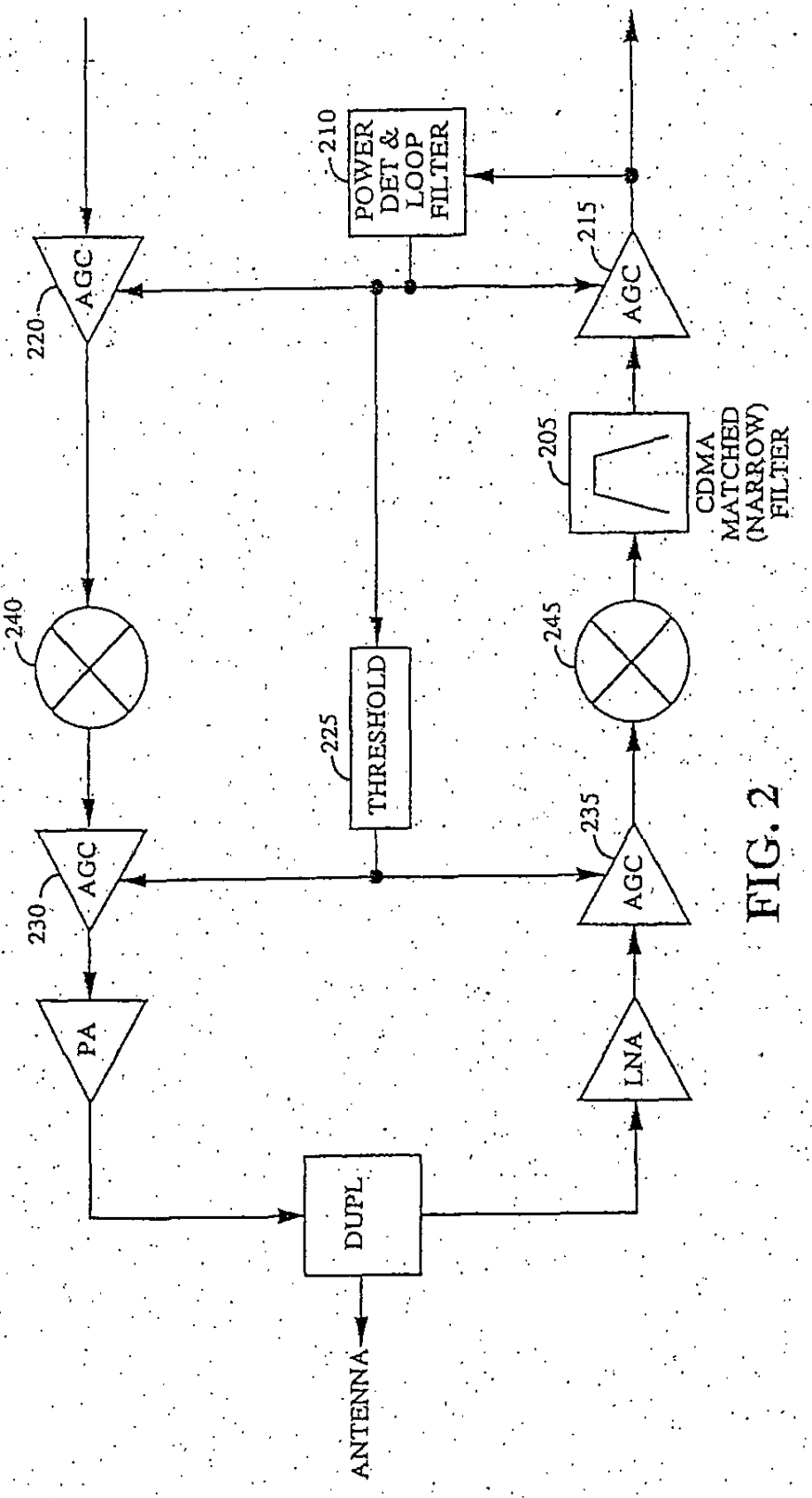
POWER DET & LOOP FILTER
110
AGC
120
AGC
PA
115
LNA
DUPL
ANTENNA

FIG. 1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POWER DET & LOOP FILTER
215
AGC
220
AGC
205
CDMA MATCHED (NARROW) FILTER
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225
THRESHOLD
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AGC
230
AGC
PA
LNA
DUPL
ANTENNA

FIG. 2

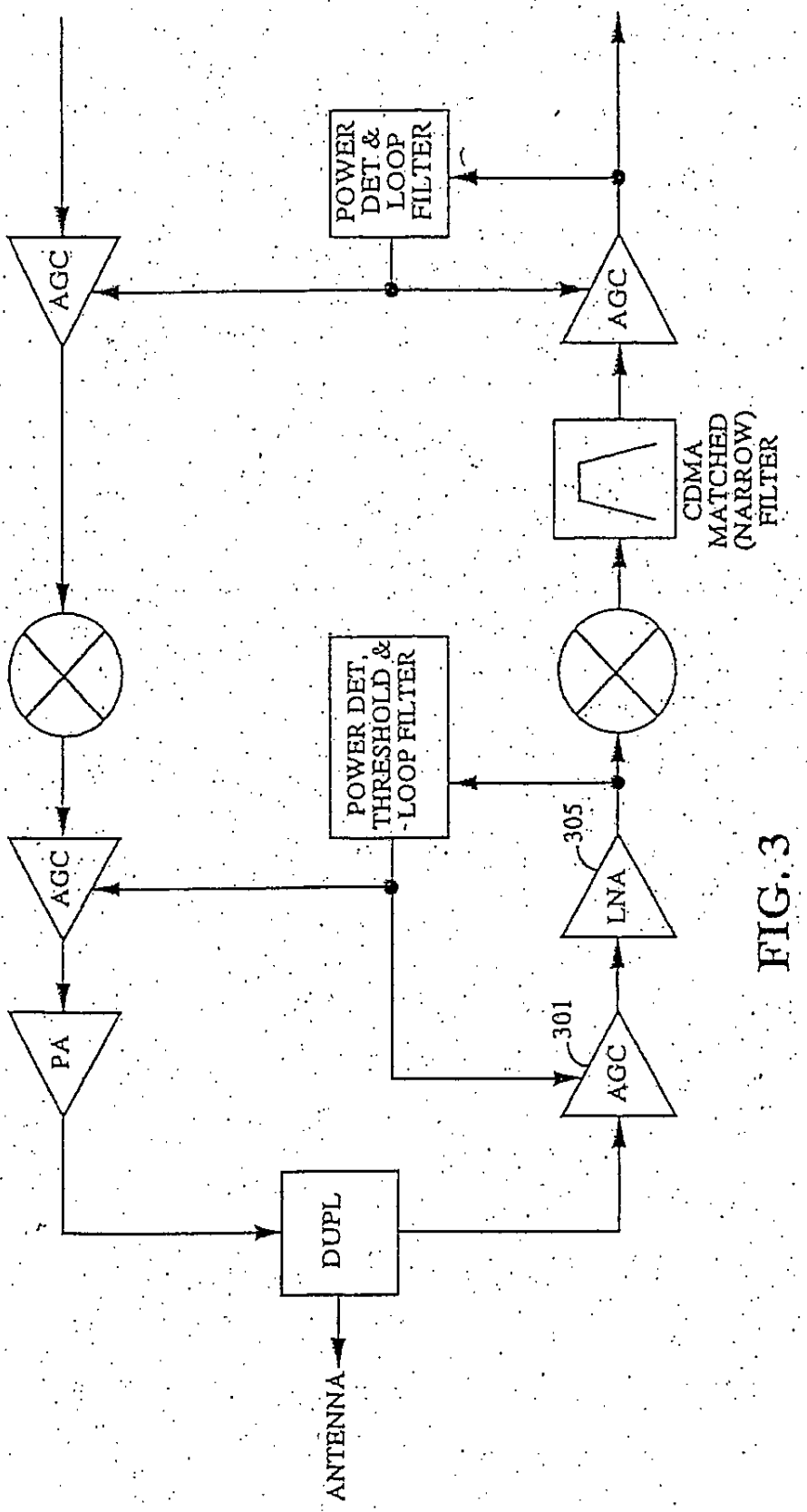

POWER DET & LOOP FILTER
AGC
AGC
CDMA MATCHED (NARROW) FILTER
POWER DET, THRESHOLD & LOOP FILTER
305
LNA
AGC
PA
301
AGC
DUPL
ANTENNA

FIG. 3

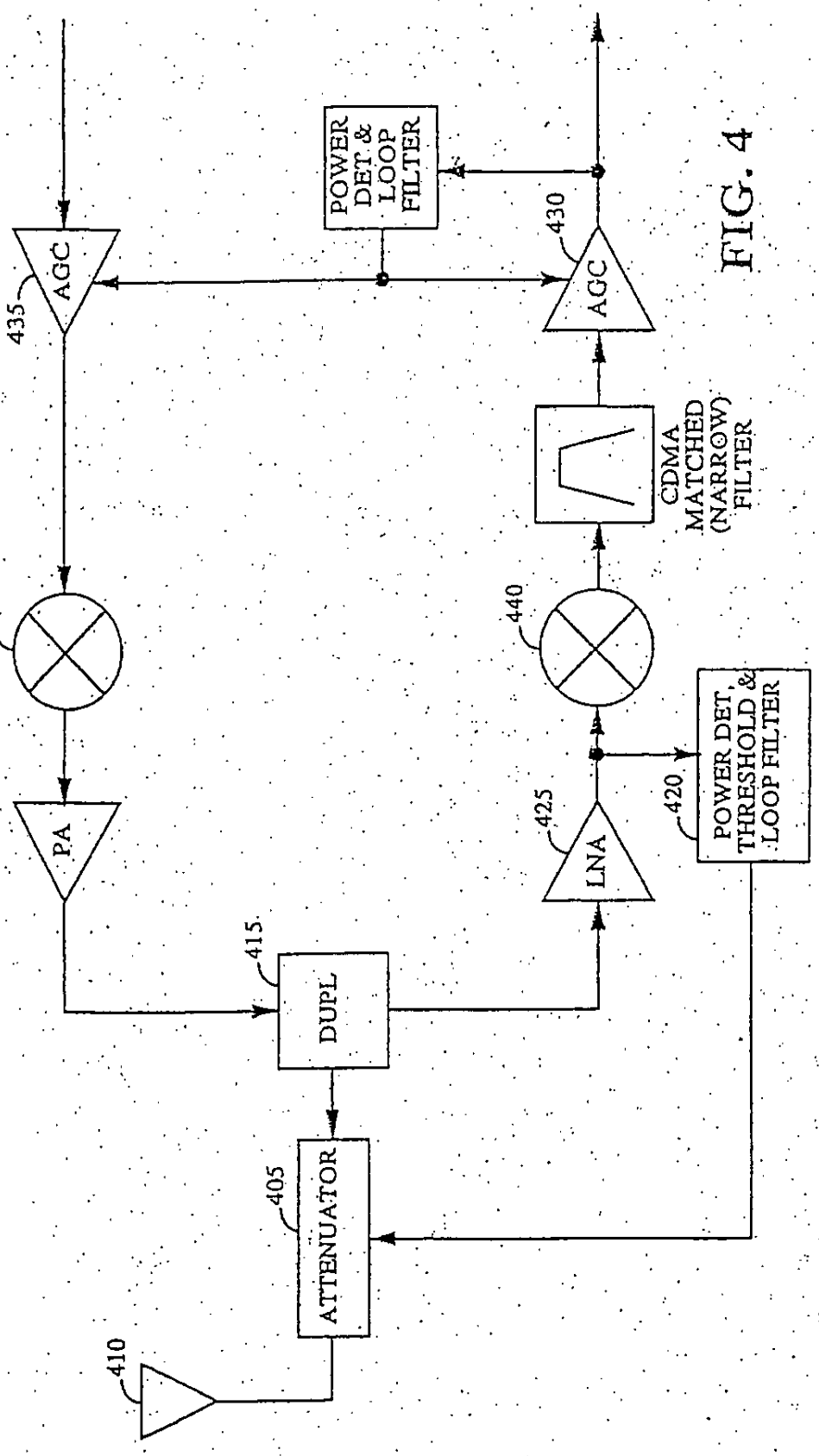


FIG. 4

Ex. D-5

Ex. C-5

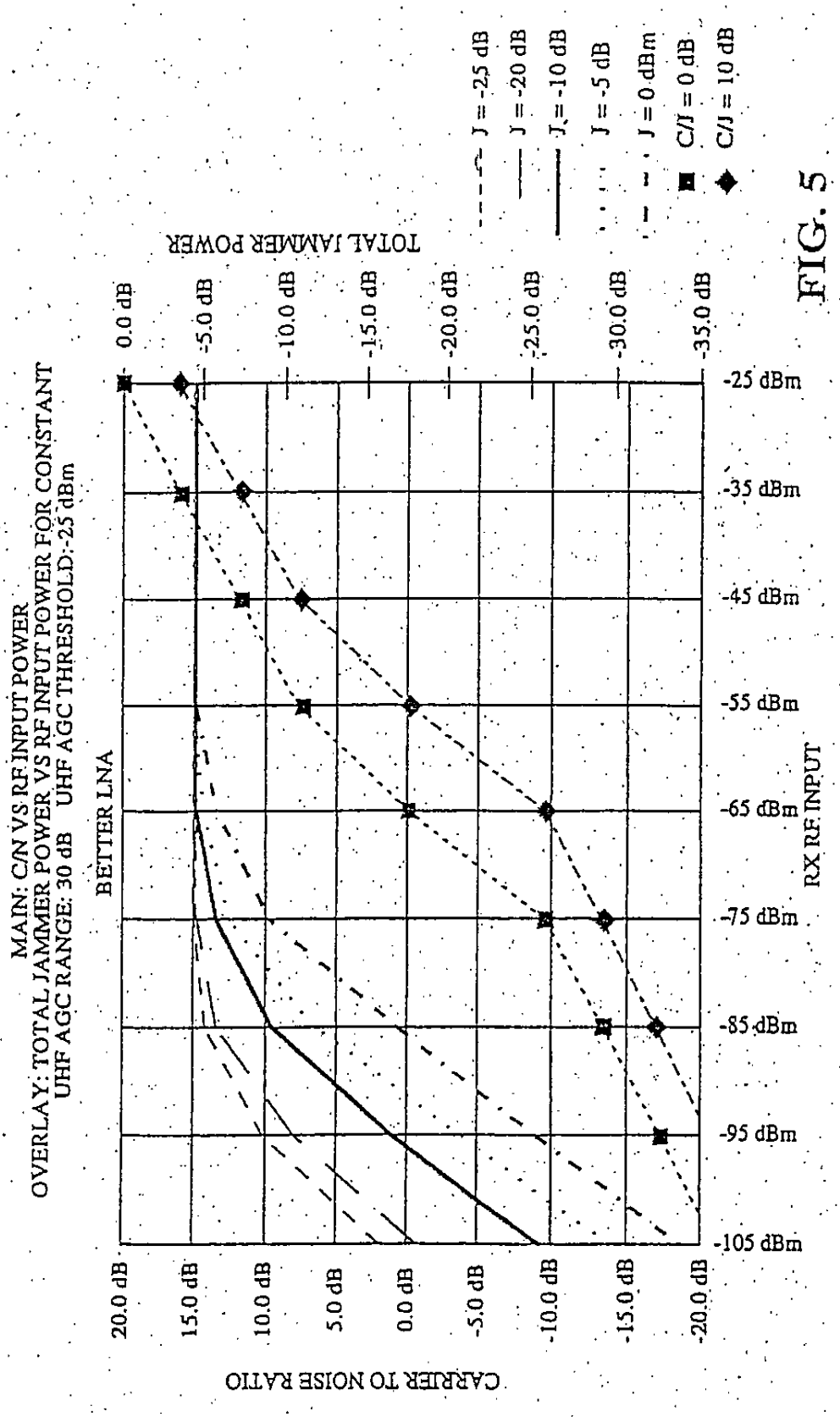


FIG. 5

Ex. D-6

Ex. C-6

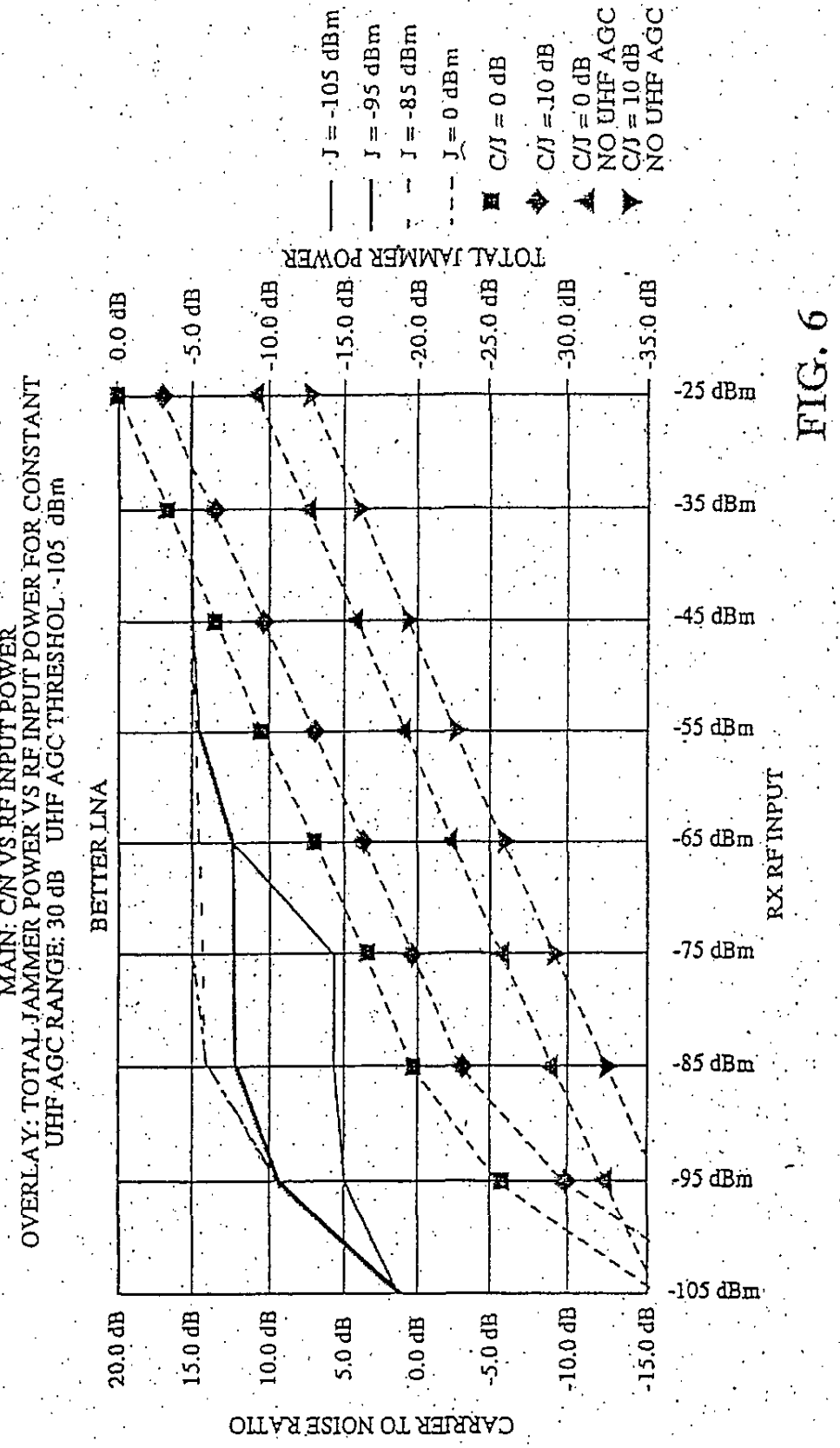
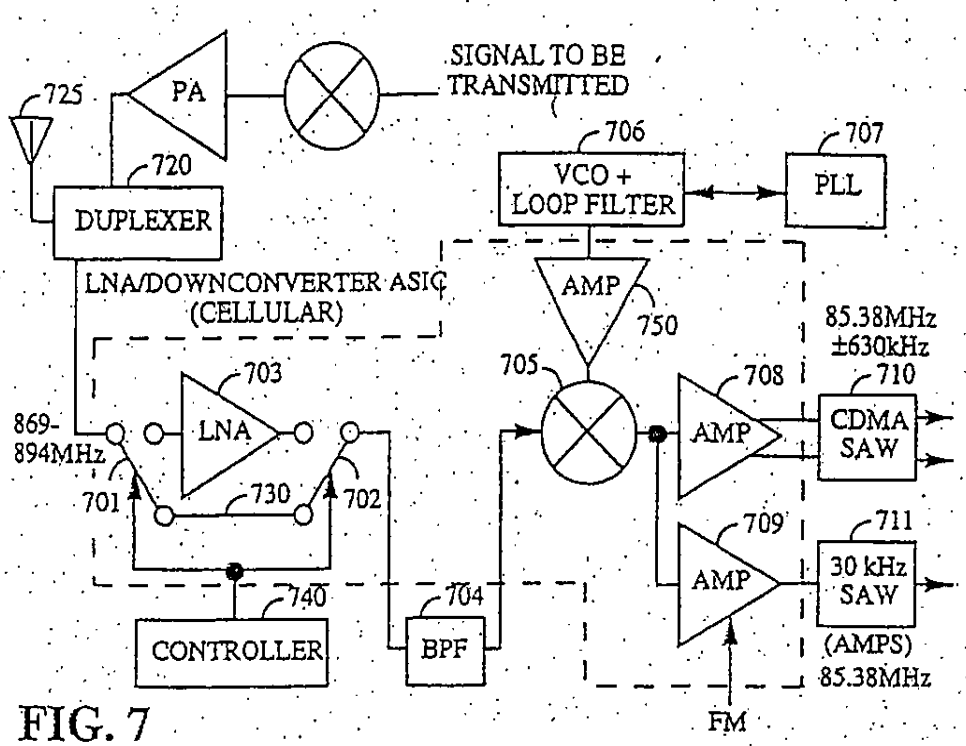


FIG. 6

Ex. D-7

Ex. C-7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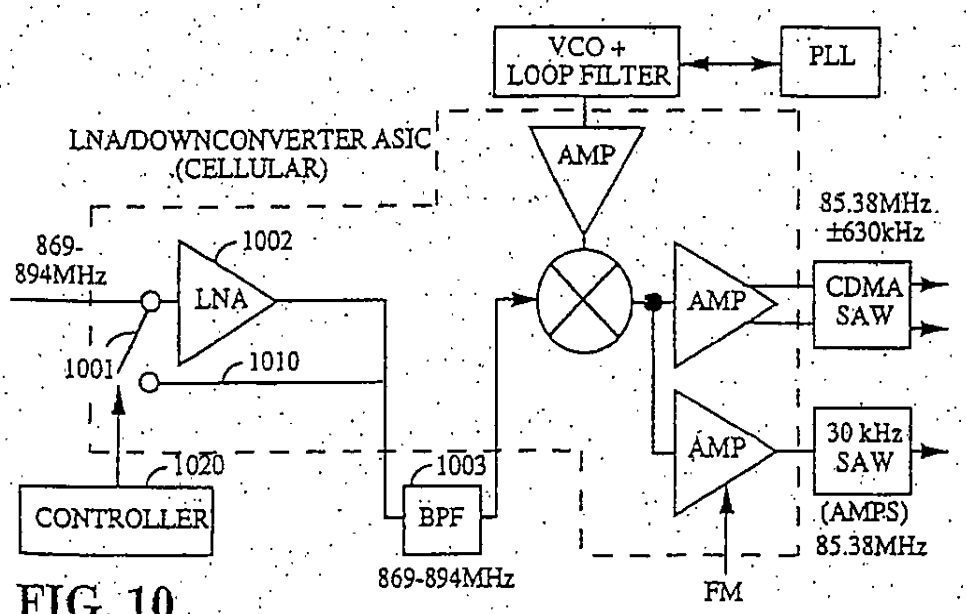
PA
SIGNAL TO BE TRANSMITTED
706
VCO + LOOP FILTER
707
PLL
720
DUPLEXER
LNA/DOWNCONVERTER ASIC (CELLULAR)
AMP
750
85.38MHz ±630kHz
705
703
708
710
869-894MHz
LNA
AMP
CDMA SAW
701
730
702
709
711
AMP
30 kHz SAW
740
704
CONTROLLER
BPF
(AMPS) 85.38MHz
FM

FIG. 7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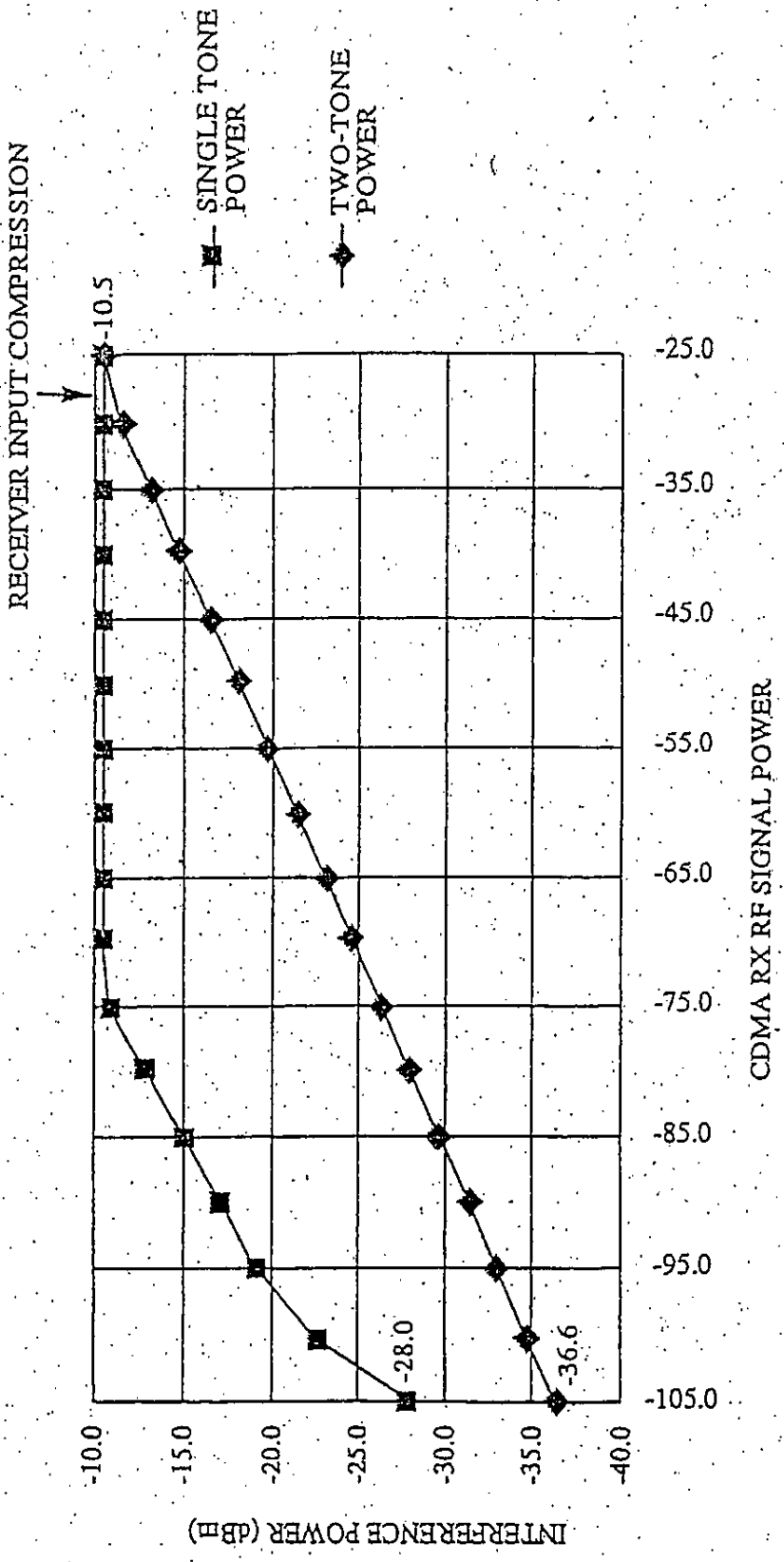
LNA/DOWNCONVERTER ASIC (CELLULAR)
AMP
85.38MHz. ±630kHz
869-894MHz
1002
LNA
AMP
CDMA SAW
1001
1010
AMP
30 kHz SAW
1020
1003
CONTROLLER
BPF
(AMPS) 85.38MHz
869-894MHz
FM

FIG. 10

FIG. 8



Ex. D-9

Ex. C-9

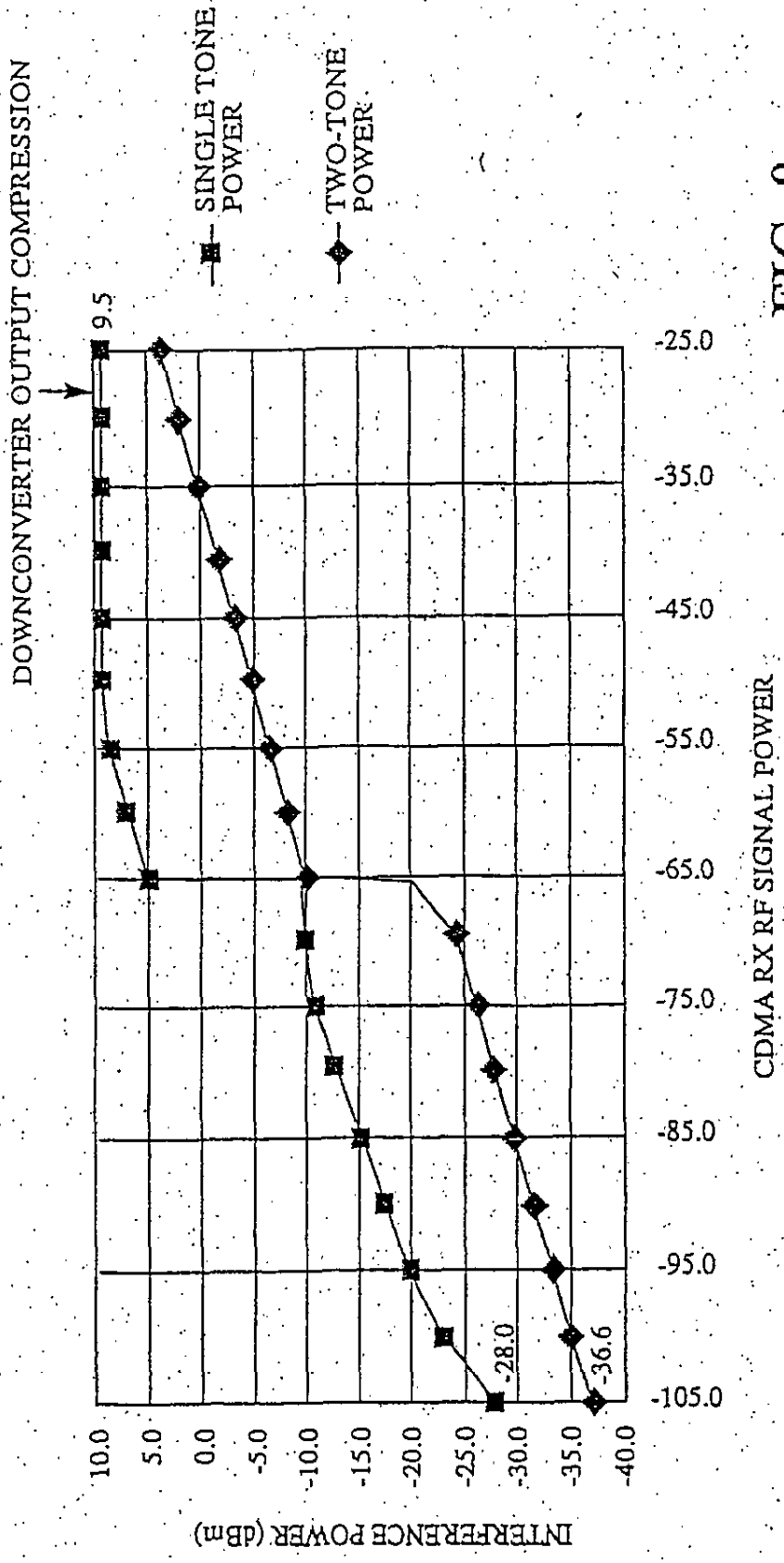


FIG. 9

Ex. D-10

Ex. C-10

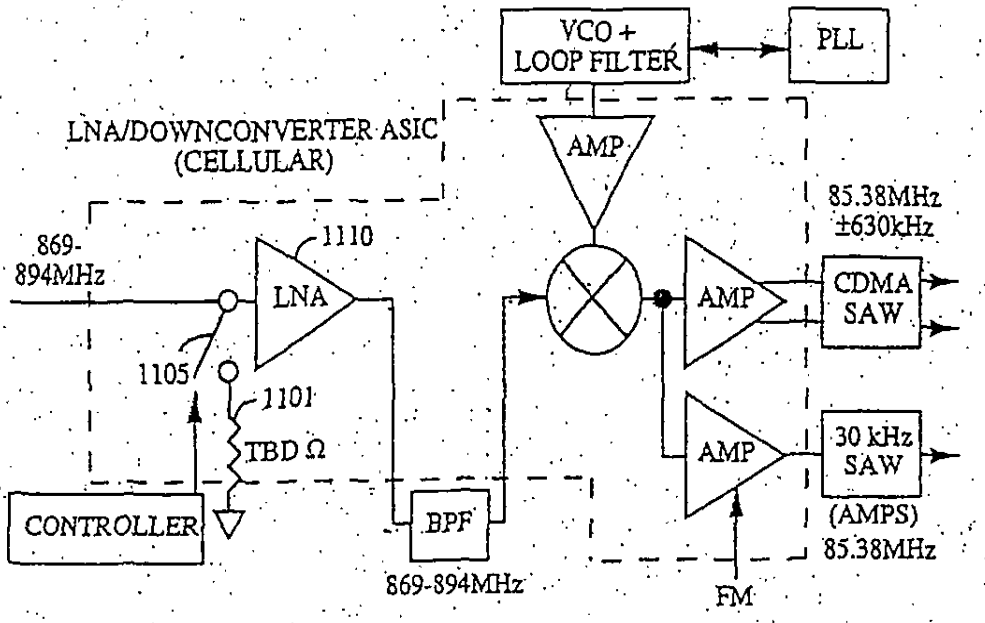
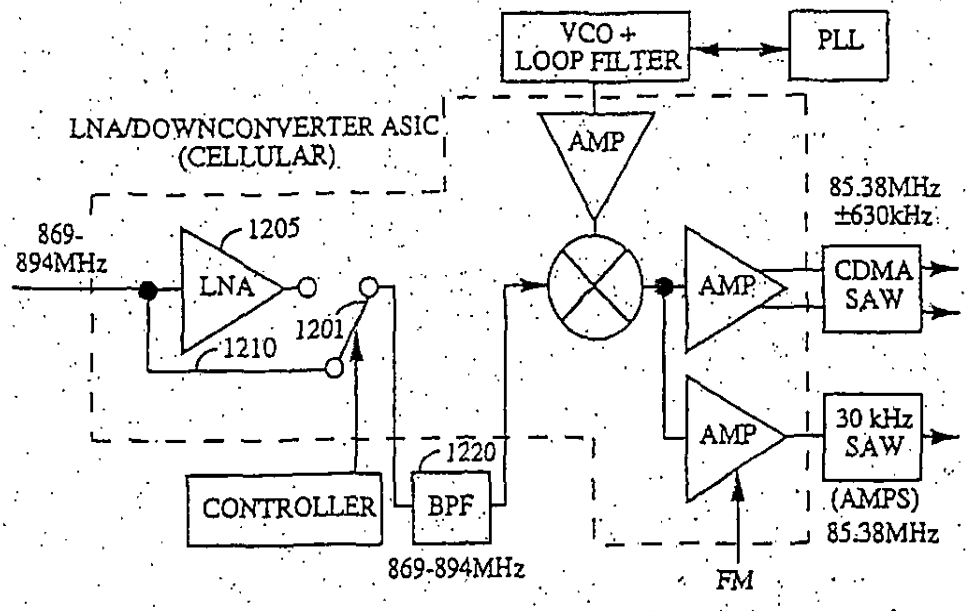

VCO + LOOP FILTER
PLL
LNA/DOWNCONVERTER ASIC (CELLULAR)
AMP
85.38MHz ±630kHz
869-894MHz
1110
LNA
AMP
CDMA SAW
1105
1101
TBD Ω
AMP
30 kHz SAW
CONTROLLER
BPF
(AMPS) 85.38MHz
869-894MHz
FM

FIG. 11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PLL
LNA/DOWNCONVERTER ASIC (CELLULAR)
AMP
85.38MHz ±630kHz
869-894MHz
1205
LNA
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1220
CONTROLLER
BPF
(AMPS) 85.38MHz
869-894MHz
FM

FIG. 12

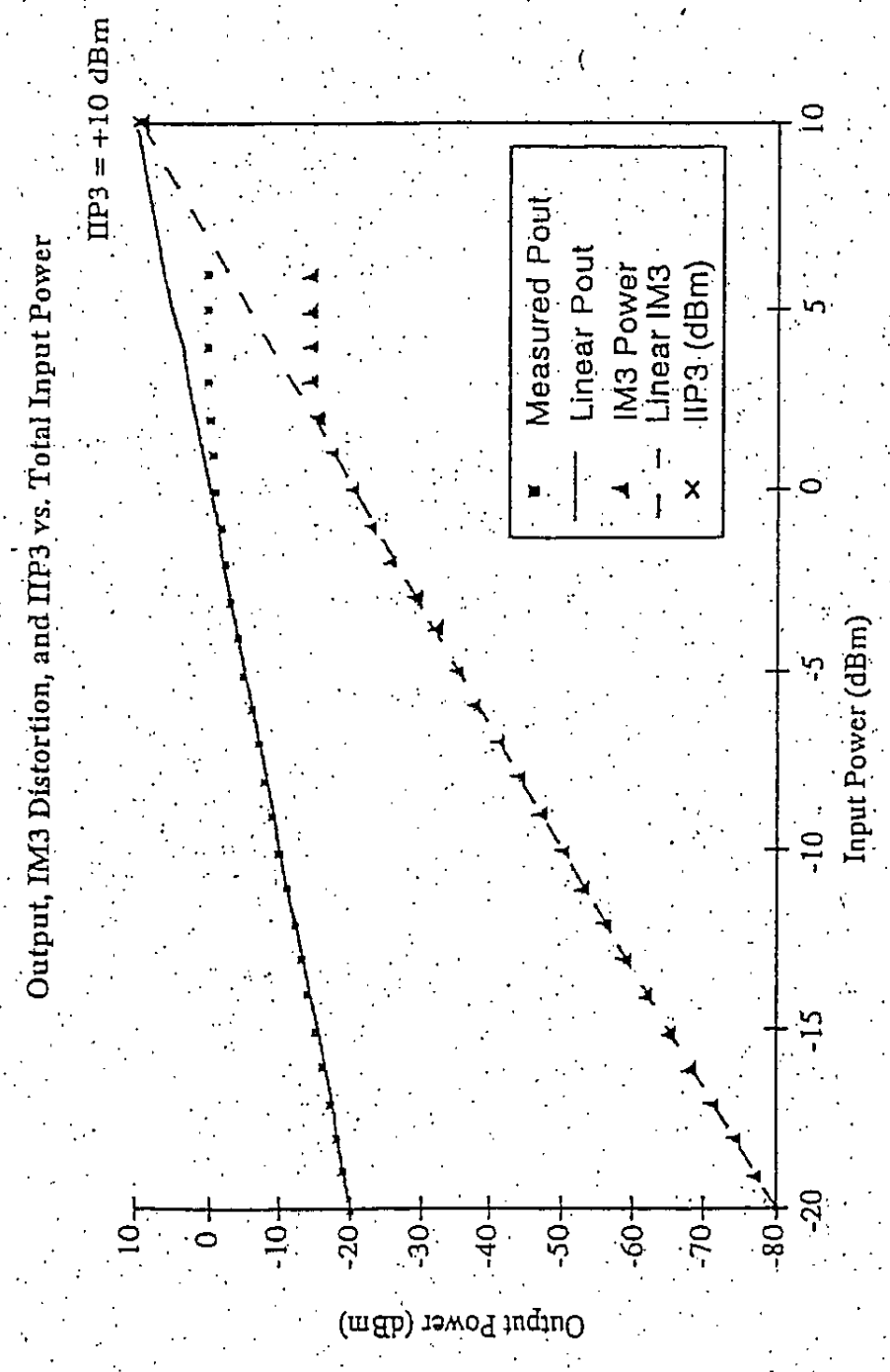

FIG. 13

Ex. D-12

Ex. C-12

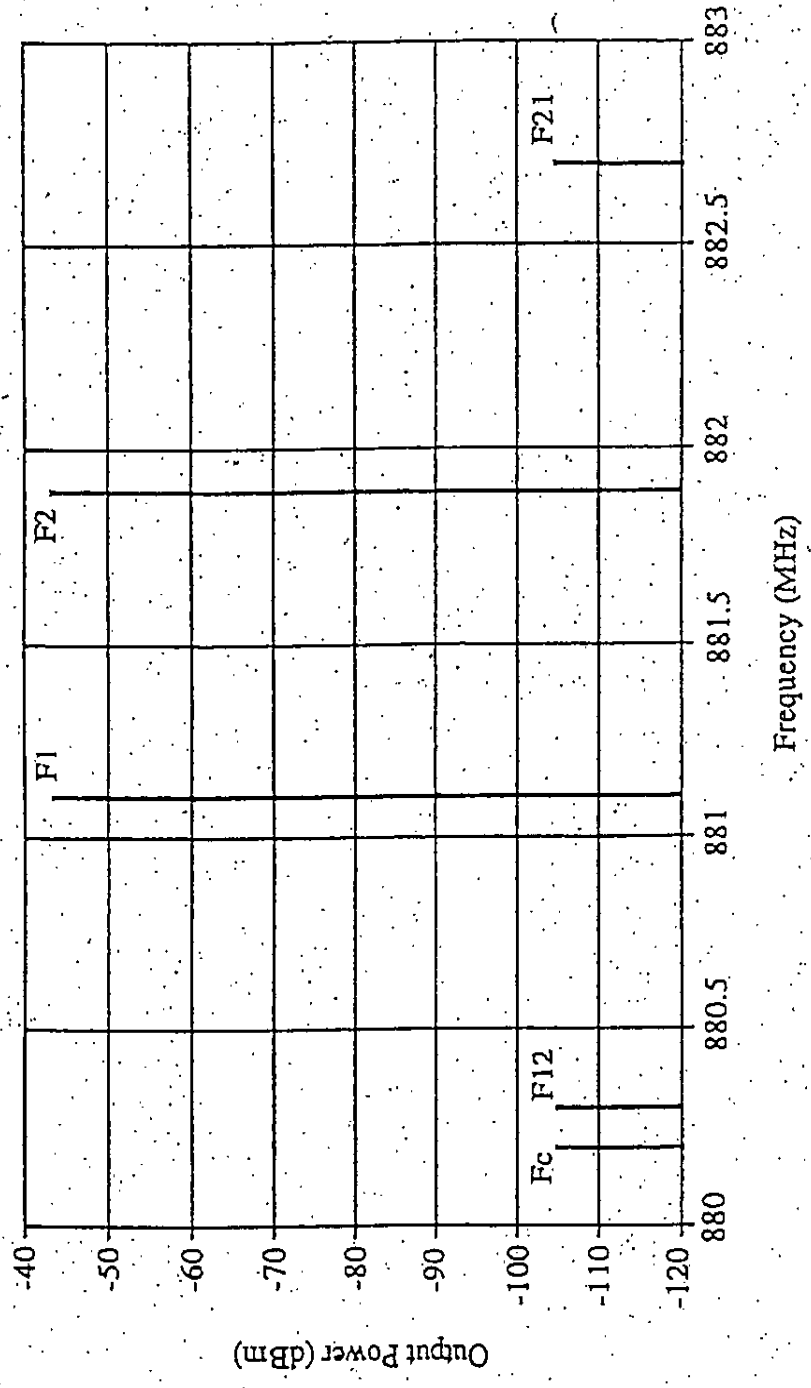

FIG. 14

Ex. D-13

Ex. C-13

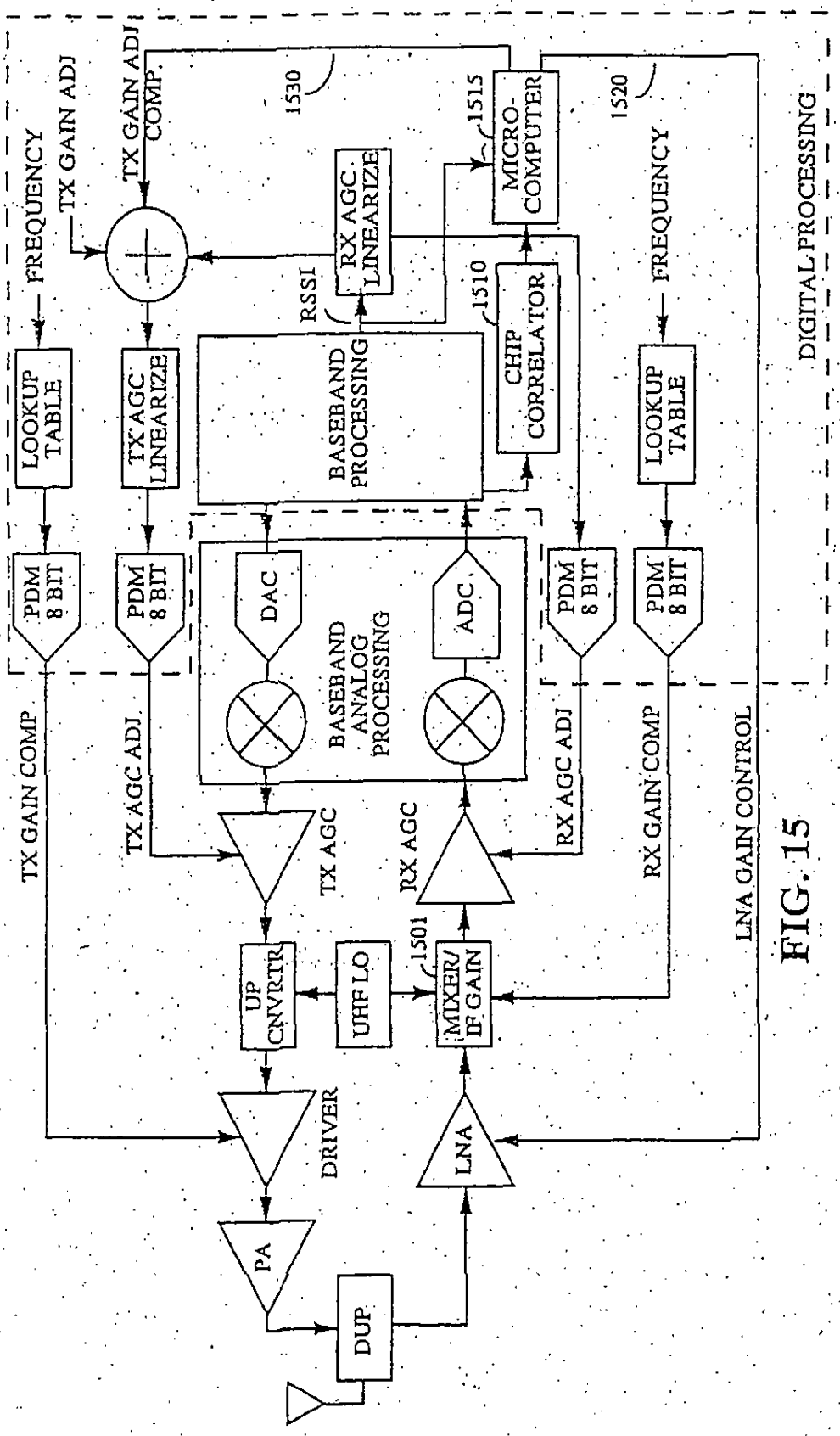

FIG. 15

Ex. D-14

Ex. C-14

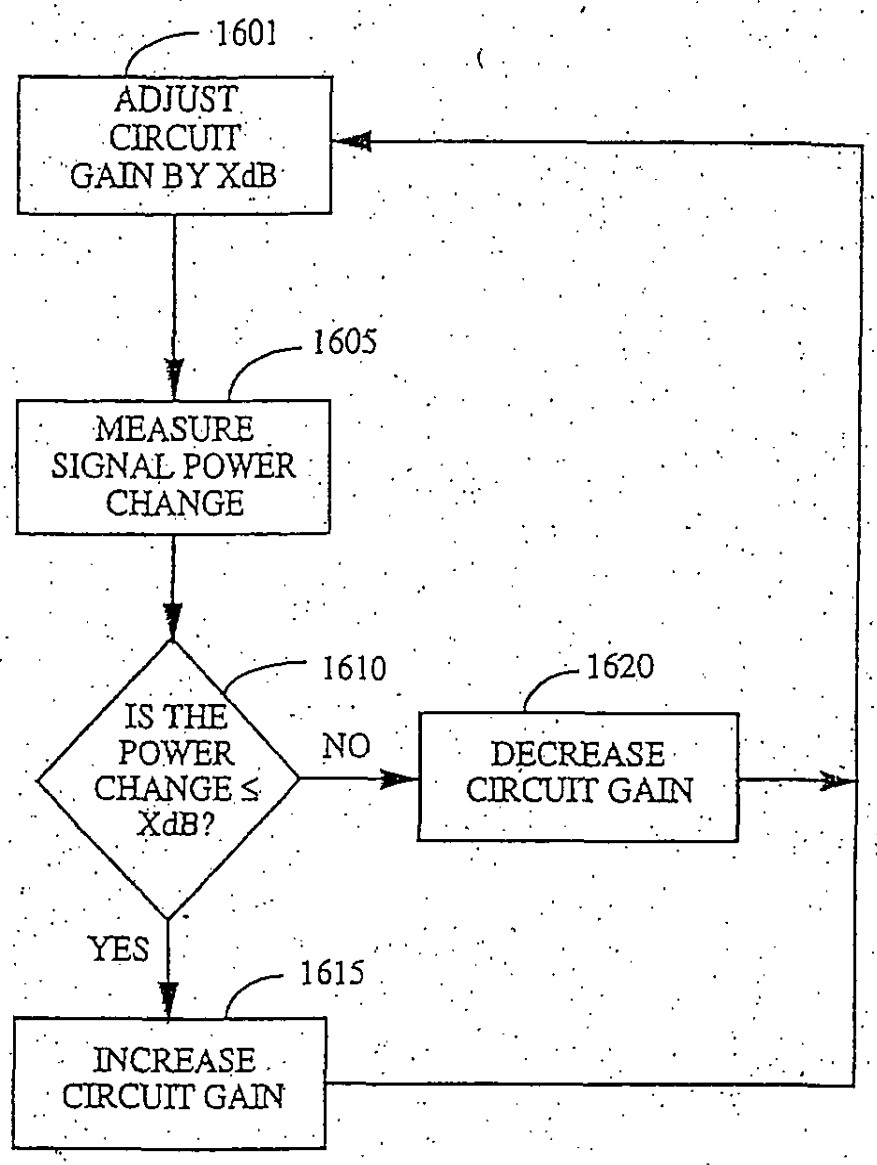
1601
ADJUST CIRCUIT GAIN BY XdB
1605
MEASURE SIGNAL POWER CHANGE
1610
IS THE POWER CHANGE ≤ XdB?
NO
1620
DECREASE CIRCUIT GAIN
YES
1615
INCREASE CIRCUIT GAIN

FIG. 16

METHOD AND APPARATUS FOR INCREASING RECEIVER IMMUNITY TO INTERFERENCE

This application is a CIP of U.S. application Ser. No. 08/357,951 filed Dec. 16, 1994 which is now U.S. Pat. No. 5,722,063.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to radio communications. More particularly, the present invention relates to improving a communication receiver's immunity to interference.

2. Description of the Related Art

There are presently multiple types of cellular radiotelephone systems operating. These systems include the advanced mobile phone system (AMPS) and the two digital cellular systems: time division multiple access (TDMA) and code division multiple access (CDMA). The digital cellular systems are being implemented to handle capacity problems that AMPS is experiencing.

All the cellular radiotelephone systems operate by having multiple antennas covering a geographic area. The antennas radiate into an area referred to in the art as a cell. The AMPS cells are separate and distinct from the CDMA cells. This makes it likely that the antenna for one system's cell may be located in a cell of another system. Likewise, within a particular system (AMPS, CDMA, and TDMA), there are two service providers within a given area. These providers often choose to place cells in different geographical locations from their competitor, hence there are situations where a radiotelephone on system 'A' might be far away from the nearest system 'A' cell while close to a system 'B' cell. This situation means that the desired receive signal will be weak in the presence of strong multi-tone interference.

This intermixing of system antennas can cause problems for a mobile radiotelephone that is registered in one system, such as the CDMA system, and travels near another system's antenna, such as an AMPS antenna. In this case, the signals from the AMPS antenna can interfere with the CDMA signals being received by the radiotelephone due to the proximity of the radiotelephone with the AMPS cell or the higher power of the AMPS forward link signal.

The multi-tone interference encountered by the radiotelephone from the AMPS signals creates distortion products or spurs. If these spurs fall in the CDMA band used by the radiotelephone, they can degrade receiver and demodulator performance.

It is frequently the case in an AMPS system for the carriers (A and B bands) to 'jam' the competitor system unintentionally. The goal of the cellular carrier is to provide a high signal to noise ratio for all the users of their system by placing cells close to the ground, or near their users, and radiating the FCC power limit for each AMPS channel. Unfortunately, this technique provides for better signal quality for the carrier's system at the expense of interfering with the competitor's system.

Intermodulation distortion, such as that caused by the above situations, is defined in terms of the peak spurious level generated by two or more tones injected into a receiver. Most frequently, the third-order distortion level is defined for a receiver in terms of a third-order input intercept point or IIP3. IIP3 is defined as the input power (in the form of two tones) required to create third order distortion products equal to the input two tone power. As shown in FIG. 13, IIP3 can

only be linearly extrapolated when a non-linear element, such as an amplifier, is below saturation.

As shown in FIG. 14, third-order distortion products occur when two tones are injected in a receiver. Tone #1 is at frequency f1 at power level P1 in dBm. Tone #2 is at frequency f2 at power level P2 in dBm. Typically P2 is set to equal P1. Third-order distortion products will be created at frequencies 2×f1 - f2 and 2×f2 - f1 at power levels P12 and P21 respectively. If P2 is set to equal P1, then spurious products should be equal, or P12 and P21 should be equal. Signal fc is injected at power level Pc to show that the added distortion is equal to a low level signal in this case. If there is a filter that filters out f1, f2 and f21 after the distortion is created, the power at f12 will still interfere with the signal power at fc. In example FIG. 14, for a CDMA application, the goal is that the intermod P12 should be equal to the signal power of −105 dBm for a total two tone power of −43 dBm, so the IIP3 must be >−9 dBm.

As is well known in the art, IIP3 for a single non-linear element is defined as the following:

$$IIP3 = \frac{IM3}{2} + P_{in}\ (\text{dBm})$$

If $P_1=P_2$, then $P_{in}=P_1+3$ dB or P_2+3 dB (dBm) and

$IM3=P_1-P_{12}=P_2-P_{21}=P_2-P_{12}=P_1-P_{21}$ (dB)

For cascaded IIP3, where more non-linear elements are used, the equation is as follows:

$$IIP3 = -10*\log 10\left(10^{(\text{Gain element } 2/3)/10} + 10^{(-IIP3 \text{ of previous stage})/10}\right)$$

where:

Gain=gain to element input.

Therefore, one way to improve the cascaded IIP3 of a receiver is to lower the gain before the first non-linear element. In this case, the LNA and mixer limit IIP3. However, another quantity needs to be defined that sets the sensitivity or lowest receive signal level without interference. This quantity is referred to in the art as the noise figure, (NF). If the gain of the receiver is reduced to improve IIP3 (and interference immunity), the NF (and sensitivity to small desired signals) is degraded.

The Element NF is defined as the following:

$$\text{Element } NF = \frac{S_i}{N_i} - \frac{S_o}{N_o}\ (\text{dB}),$$

where:

Si/Ni is the input signal to noise ratio in dB, and

S_o/N_o is the output signal to noise ratio in dB.

For elements in cascade in a receiver, the equation is as follows:

$$\text{Cascaded } NF = 10*\log 10\left[10^{(NFe/10)} + \frac{10^{(NFi/10)} - 1}{10^{(Gain/10)}}\right],$$

where:

NFe equals the noise figure of the element,

NFi equals the cascaded noise figure up to the element, and

Gain equals the running gain up to the element.

The 'best' cascaded NF can be achieved if the gain up to the element is maximized, this equation is in contradiction to the requirement for the 'best' cascaded IIP3. For a given element by element and receiver NF and IIP3, there are a limited set of gain values for each element that meet all of the requirements.

Typically, a receiver is designed with NF and IIP3 as predefined constants, as both of these quantities set the receiver's dynamic range of operation with and without interference. The gain, NF, & IIP3 of each device are optimized based on size, cost, thermal, quiescent and active element current consumption. In the case of a dual-mode CDMA/FM portable cellular receiver, the CDMA standard requires a 9 dB NF at minimum signal. In other words, for CDMA mode, the sensitivity requirement is a 0 dB S/N ratio at −104 dBm. For FM mode, the requirement is a 4 dB S/N ratio at −116 dBm. In both cases, the requirements can be translated to a NF as follows:

$$NF = S(\text{dBm}) - \frac{S}{N}\ (\text{dB}) - N_{therm}(\text{dBm/Hz}) - \text{Signal } BW\ (\text{dB/Hz}),$$

where

S is the minimum signal power,

S/N is the minimum signal to noise ratio.

N_{therm} is the thermal noise floor (−174 dBm/Hz@290° K.),

and Signal BW (dB/Hz) is the bandwidth of the signal.

Therefore,

CDMA NF=−104 dBm−0 dB−(−174 dBm/Hz)−61 dB/Hz=9 dB,

FM NF=−116 dBm−4 dB−(−174 dBm/Hz)−45 dB/Hz=9 dB,

where

−61 dBm/Hz is the noise bandwidth for a CDMA channel

−45 dBm/Hz is the noise bandwidth for a FM channel

However, the receiver's NF is only required when the signal is near the minimum level and the IIP3 is only required in the presence of interference or strong CDMA signals.

There are only two ways to provide coverage in the areas where the carrier is creating strong interference. One solution is to employ the same technique; i.e., co-locate their cells along with the competition's. Another solution is to improve the immunity of a receiver to interference. One way to improve the immunity is to increase the receiver current. This is not a practical solution, however, for a portable radio that relies on battery power. Increasing the current would drain the battery more rapidly, thereby decreasing the talk and standby time of the radiotelephone. There is a resulting need to minimize multi-tone interference in a radiotelephone without impacting the current consumption.

SUMMARY OF THE INVENTION

The process of the present invention adjusts attenuation in a circuit, thereby improving a receiver's immunity to interference. The circuit has an attenuator with attenuation and automatic gain control (AGC) with a variable gain. The process varies the attenuation by a predetermined amount. The gain of the circuit is then detected. If the detected gain change is greater than a predetermined threshold, intermodulation products have been detected and the front end attenuation is increased to reduce the intermodulation product power.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a block diagram of the apparatus of the present invention for increasing receiver immunity.

FIG. 2 shows a block diagram of another alternate embodiment of the present invention.

FIG. 3 shows a block diagram of another alternate embodiment of the present invention.

FIG. 4 shows a block diagram of another alternate embodiment of the present invention.

FIG. 5 shows a another plot of received RF input power versus carrier to noise ratio in accordance with the embodiment of FIG. 7.

FIG. 6 shows a plot of receive RF input power versus carrier to noise ratio in accordance with the embodiment of FIG. 8.

FIG. 7 shows a block diagram of another alternate embodiment of the present invention.

FIG. 8 shows a plot of interference power vs. signal power without using the apparatus of the present invention.

FIG. 9 shows a plot of interference power vs. signal power in accordance with the alternate embodiments of the apparatus of the present invention.

FIG. 10 shows a block diagram of an alternate embodiment of the present invention.

FIG. 11 shows a block diagram of another alternate embodiment of the present invention.

FIG. 12 shows a block diagram of another alternate embodiment of the present invention.

FIG. 13 shows a plot of non-linear transfer characteristics and distortion measurement.

FIG. 14 shows a spectral description of distortion products.

FIG. 15 shows a block diagram of a method for detecting the power of a received signal in accordance with the present invention.

FIG. 16 shows a flow chart of the attenuation control process of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

It is an objective of the present invention to vary the receiver NF and IIP3 for enhancing the IIP3 (or interference immunity) without compromising NF when necessary. This performance 'enhancement' is accomplished by varying the gain of the first active element in the receiver. The gain can be varied by varying the gain of the LNA over a continuous range or switching out the low noise amplifier with bypass switches.

A block diagram of the preferred embodiment of the present invention is illustrated in FIG. 1. This embodiment involves adjusting the LNA 115 gain on a continuous basis using adjustable gain control (AGC) 110 at the receiver front end. The continuous AGC 110 at the front end also provides a linearity benefit at a minimum RF input level while the AGC 120 on the transmit side may reduce the IF AGC 125 and 130 requirements.

This embodiment detects the power output from the LNA 115. The power detector 105 measures both the signal power and the jammer power together at RF. Using this embodiment, the power detector 105 can continuously decrease the LNA 115 gain at a lower received power than the −65 dBm of the subsequent "switched gain" embodiments of FIGS. 7, 10, 11 and 12.

The preferred embodiment operates by the power detector 105 detecting the received signal and jammer power at RF. This detected power goes through a loop filter and is used to adjust the receive AGC 110, thereby adjusting the intercept point of the receive components. The gain is decreased as the measured power increases and the gain is increased as the measured power decreases. This embodiment could also combine the LNA 115 and the AGC 110 to form a variable

gain LNA, thus eliminating the need for the separate AGC 110 block. The power of the transmit AGC 120, located before the power amplifier 150, is adjusted in the same way as the receive AGC 110 in order to maintain the overall TX power level.

AGC amplifiers 125 and 130 are also located after the mixers 135 and 140 in order to adjust the gain after the jammers have been filtered out by the bandpass filter 145. These AGC amplifiers 125 and 130 perform the normal CDMA AGC function of open loop power control, closed loop power control, and compensation. These IF AGCs 125 and 130 are required due to the wide dynamic range requirements for CDMA. Typically, these AGCs 125 and 130 have greater than 80 dB of gain range. The receive and transmit AGC 125 and 130 after the mixers are adjusted by another power detector 150 that measures the total power after the received signal is downconverted. The power detector 150 adjusts the AGCs 125 and 130 gain downward as the downconverted signal's power increases and adjusts the AGCs 125 and 130 gain upward as the downconverted signal's power decreases.

In the preferred embodiment, the received signals are in the frequency band of 869–894 MHz. The transmitted signals are in the frequency band of 824–849 MHz. Alternate embodiments use different frequencies.

The plot illustrated in FIG. 5 shows the benefit of this AGC approach. The left hand y-axis shows the carrier over noise ratio versus receive input power parameterized by the jammer level. The right hand y-axis shows the total jammer power required for a constant C/J as a function of received input power. When the jammer is not present (–100 dBm), the radio operates as though there is no RF AGC. As the jammer is increased, the C/N is decreased, but the effective linearity is also increased. In this example, the RF dynamic range is 30 dB and the threshold, where the RF AGC becomes active, is at the point the jammer power is greater than –25 dBm.

An alternate embodiment of the continuous gain adjustment is illustrated in FIG. 2. This embodiment first filters out the jammers with the bandpass filter 205 before the power detector 210 determines the power level of the downconverted signal. A threshold detector 225 determines when the signal power level reaches a certain point, –105 dBm in this embodiment, and then adjusts the AGCs 230 and 235 gain down when the signal power exceeds that power level. The AGCs 230 and 235 gain is adjusted upward when the signal power level goes below this threshold. The gain of AGCs 215 and 220 after the mixers 240 and 245 is adjusted continuously without checking for a predetermined threshold of power, performing the normal CDMA AGC power control.

The plot of this embodiment is illustrated in FIG. 6. When the threshold is set at –105 dBm, the minimum receive RF level, the C/N does not increase as quickly as the case where there is no RF AGC. The advantage of this embodiment is that the linearity benefit begins at a very low RF input power, no receive RF power detector is needed, and the AGC loop detects signal power only. Hence, the AGC loop is a simpler design than detecting at RF power.

Still another embodiment of the present invention is illustrated in FIG. 3. This embodiment operates similarly to the embodiment of FIG. 1. The only difference being the placement of the AGC 301 prior to the LNA 305 in the receive path.

Yet another embodiment of the present invention is illustrated in FIG. 4. This embodiment uses an attenuator 405 between the antenna 410 and the duplexer 415. The attenuation is controlled by the power detector 420 after the LNA 425. The power detector 420 measures the received signal and jammer power, filters it, and compares it to a predetermined threshold. In this embodiment, the threshold is –25 dBm. When the combined signal and jammer power reaches this threshold, the attenuation caused by the attenuator 405 is increased. This adjustment can be either in digital fixed steps or continuously adjusted. The AGC 430 and 435 after the mixers 440 and 445 are adjusted in the same manner as the FIG. 1 preferred embodiment.

An alternate embodiment of the apparatus of the present invention is illustrated in FIG. 7. This embodiment uses switches 701 and 702 to alter the front end gain. The actual switching level depends on the signal to noise requirements as a function of the signal level, or noise figure, for a particular CDMA radiotelephone design. The present invention can be used in an AMPS radiotelephone, however the switching characteristics will be changed to accommodate a different operating point.

This embodiment is comprised of an antenna 725 that receives and transmits radio signals. Receive and transmit paths in the radio are coupled to the antenna 725 through a duplexer 720 that separates the received signals from the transmitted signals.

A received signal is input to an LNA 703 that is coupled between two switches 701 and 702. One switch 701 couples the LNA 702 to the duplexer 720 and the second switch 702 couples the LNA 703 to a band-pass filter 704. In the preferred embodiment, the switches 701 and 702 are single-pole double-throw gallium arsenide switches.

The LNA 703 is coupled to one pole of each switch such that when both switches 701 and 702 are switched to those poles, the received signal is coupled to the LNA 703 and the amplified signal from the LNA 703 is output to the band-pass filter 704. The band-pass filter 704 in this embodiment has a frequency band of 869–894 MHz. Alternate embodiments use different bands depending on the frequencies of the signals being received.

A bypass path 730 is coupled to the other pole of each switch. When the switches 701 and 702 are switched to their other poles, the received signal from the duplexer 720 bypasses the LNA 703 and is conducted directly to the band-pass filter 704. In this embodiment, these switches 701 and 702 are controlled by the radiotelephone's microcontroller 740. In an alternate embodiment, a separate controller is used to control the positions of these switches.

After the band-pass filter 704 has filtered the received signal, the filtered signal is downconverted to a lower intermediate frequency (IF) for use by the rest of the radio. The down-conversion is done by mixing 705 the received signal with another signal having a frequency set by a phase locked loop 707 driving a voltage controlled oscillator 706. This signal is amplified 750 before being input to the mixer 705.

The downconverted signal from the mixer 705 is input to the back end AGCs 708 and 709. These AGCs 708 and 709 are used by the radiotelephone for closed loop power control, as is already well known in the art.

In the process of the present invention, the microcontroller 740 monitors the power of the received signal. When the power exceeds –65 dBm, the microcontroller 740 instructs the switches 701 and 702 to switch to the bypass position, thus coupling the received signal directly to the bandpass filter 704. By bypassing the LNA 703 gain, the intercept point for the receiver is increased proportionally by the

reduction in gain in dB. Alternate embodiments use other circuitry and methods to monitor the power of the received signal.

An alternate embodiment of the process of the present invention continuously adjusts the front end gain. This embodiment uses a lower power threshold such as −25 dBm.

The plots of FIGS. 8 and 9 illustrate the benefits of the switchable gain embodiments of the present invention illustrated in FIGS. 7, 10, 11 and 12. FIG. 8 illustrates a plot of interference power versus radio frequency (RF) signal power for a typical radio that is not using the switchable gain apparatus. This plot shows that the maximum interference level is limited to the receiver input compression point at −10.5 dBm. Both the single and dual tone power curves are shown.

The plot of FIG. 9 shows the interference power received by the radio versus the radio frequency signal power received by the radio using the switchable gain method and apparatus of the present invention. It can be seen that at the −65 dBm point of the graph, the switches are switched to bypass the LNA gain thus allowing a greater interference power to be tolerated without affecting the RF signal power. Both the single tone and two tone power curves are shown.

Another alternate embodiment of the apparatus of the present invention is illustrated in FIG. 10. This embodiment uses a single-pole single-throw switch 1001. In this embodiment, the switch 1001 is switched to the bypass path 1010 by the controller 1020 when the received signal power reaches −65 dBm. This effectively shorts out the LNA 1002 gain, thus coupling the received signal directly to the band-pass filter 1003.

Yet another alternate embodiment of the apparatus of the present invention is illustrated in FIG. 11. This embodiment uses a single-pole single-throw switch 1105 that, when closed, shorts the input of the LNA 1110 to ground through a resistor 1101. This creates an impedance mismatch at the input causing the signal to attenuate, thus reducing the gain caused by the LNA 1110. As in the above embodiments, the switch 1105 is closed when the input signal power reaches −65 dBm. The resistance required for the resistor 1101 is dependent on the amount of attenuation desired. This resistance will be different for different LNA's in alternate embodiments.

Still another embodiment of the apparatus of the present invention is illustrated in FIG. 12. This embodiment uses a single-pole double-throw switch 1201 at the output of the LNA 1205. The LNA 1205 is connected to one pole of the switch 1201 and a bypass path 1210 is connected to the other pole. The input to the bypass path 1210 is connected to the input of the LNA 1205. When the power level of the received RF signal reaches −65 dBm, the switch 1201 is thrown from the position coupling the LNA 1205 to the bandpass filter 1220 to the bypass path 1210. This couples the signal directly to the band-pass filter 1220, bypassing the gain of the LNA 1205.

In all of the above embodiments, the LNA can be powered down at the same time that it is bypassed by the switch or switches. This can be accomplished by connecting the LNA's power pin to a switch that is also controlled by the controller. Once the LNA is bypassed and is no longer used, power can be removed. This reduces the power consumption of the radio, thus increasing the talk and standby time for which the battery can be used.

In another embodiment of the present invention, E_c/I_o detection is used to determine when to adjust the front end gain. Additional embodiments use other quality measurements, such as E_b/I_o.

These ratios are quality measurements for digital communications system performance. The E_b/I_o ratio expresses the energy per bit to the total interference spectral density of the channel while the E_c/I_o ratio expresses the energy per CDMA chip relative to the total interference spectral density. E_b/I_o can be considered a metric that characterizes the performance of one communication system over another; the smaller the required E_b/I_o the more efficient is the system modulation and detection process for a given probability of error. Given that E_c/I_o and received signal strength are readily available, the microcontroller can detect the presence of strong interference as a drop in E_c/I_o while the AGC detector detects the increased interference. The microcontroller can lower the front end gain to improve interference immunity which would improve E_c/I_o and lower the distortion products falling within the signal bandwidth.

When the signal quality goes above the E_b/I_o or E_c/I_o threshold, the front end gain is reduced. The gain adjustment can be accomplished using either the continuous adjustment method or the amplifier switching method, both described above.

Still another embodiment, illustrated in FIG. 15, would be to detect the signal power at IF or baseband instead of the combination of the signal and jammer power at RF. This approach is simpler in that there is only one power detector and AGC control loop.

FIG. 15 illustrates a block diagram of the alternate method of detecting the power of the received signal. The signal is first downconverted to baseband frequency 1501. This analog signal is then converted to a digital signal 1505 for further baseband processing including determining the received signal strength. The chip correlator 1510 determines the energy per chip with respect to the energy of all the non-coherent components. This information, along with the received signal strength indicator (RSSI) is used by the processor 1515 to determine the amount of gain adjustment for both the receive 1520 and transmit 1530 power.

Since the received signal power measurement includes both the signal and jammer power, the receive gain is increased only when both the signal level and the energy per chip drops. Since the RSSI is being changed, the transmit power must also be changed to compensate, thus enabling the open loop power control to operate properly. Thus, the processor adjusts the transmit gain whenever the receive gain is adjusted.

Other embodiments use erasures or signal power to control the variable gain AGC. Additional embodiments, instead of controlling both transmit and receive power, only control receiver power.

A process for controlling the gain of the above embodiments is illustrated in FIG. 16. This process is based on the relationship illustrated in the graph of FIG. 13. In FIG. 13, one can see that as the interference input power increases along the X axis, the intermodulation products (the lower curve) increase faster than the interference power. Therefore, X dB of attenuation applied at the input will result in a decrease of the IM3 intermodulation products by 3*X dB if interference is present at the receiver input.

Typically, intermodulation products don't fall into the IF section of the radio due to their low power. Intermodulation products outside of the IF section oft he radio do not cause receiver performance problems. Thus, adjustment of the receiver gain is only necessary if the intermodulation products are of sufficient power to affect the IF signal.

Referring to FIG. 16, the process of the present invention first adjusts the input gain 1601. In the preferred

embodiment, this gain adjustment is 3 dB. However, other embodiments can use other values of gain adjustment, such as the range of 1 dB–6 dB. The receiver processing is then used to measure the change in the power of the received signal 1605. In the preferred embodiment, the automatic gain control processing detects the IF signal power change. It is understood that measurement of the change in received signal power may be accomplished at the RF or baseband stages of the receiver as well.

If the signal power changes by approximately 3 dB, the CDMA signal is greater than the noise floor and there are no intermodulation products that might cause problems. Additional gain adjustment is not needed in this case, but increasing the gain will improve receiver sensitivity. IF signal power changes of approximately (3±0.5) dB are still considered to be 3 dB.

If the IF signal power changes by less than 3 dB 1610, the CDMA signal is less than the noise floor or there are no intermodulation products that might cause problems. In this case, the AGC is only seeing a small CDMA signal and noise. Therefore, it is necessary to increase the receiver circuit gain 1615 and thus increase the sensitivity of the receiver.

If the IF signal power changes by more than 3 dB, the intermodulation products are causing enough of a problem that additional gain adjustment is necessary 1620. In the preferred embodiment, if the input gain was changed by 3 dB the intermodulation products will change by 9 dB when large interference is present. In this case, the average gain may be decreased by a small amount (e.g., 3 dB) until the process of the present invention determines that the intermodulation products are reduced to an acceptable level.

The process of the present invention can be used continuously, checking for intermodulation products at a low rate. This rate is ten times per second in the preferred embodiment. Other embodiments use the process once per frame cycle. Still other embodiments use the process at other rates, such as upon detection of a significant error on the forward link.

In summary, the method of the present invention enables a mobile radio to travel near antennas of different systems while increasing the radio's resistance to radio frequency interference from the other system. By decreasing the front end gain, the intercept point of the radio's receive circuitry increases so that the spurs from the other system's signals will not cause performance degradation of the receiver and demodulator.

I claim:

1. A method for circuit gain adjustment, the circuit having a signal with power, the method comprising the steps of:

varying the circuit gain a predetermined amount;

determining a magnitude of a change in the power of the signal in response to the varying of the circuit gain; and

adjusting the circuit gain in response to the magnitude of the change in the power of the signal, the step of adjusting comprising the steps of:

decreasing the circuit gain when the magnitude of the change in the power of the signal is greater than a predetermined threshold; and

increasing the circuit gain when the magnitude of the change in the power of the signal is less than or equal to the predetermined threshold.

2. The method of claim 1 wherein the predetermined amount is about 3 dB and the predetermined threshold is about 9 dB.

3. A method for adjusting the power of a received signal having a plurality of frames in a circuit having a variable gain, the method comprising the steps of:

receiving the received signal at a radio frequency;

converting the received signal from the radio frequency to an intermediate frequency;

filtering the received signal;

varying the gain of the circuit by a predetermined amount;

determining a magnitude of a change in the power of the received signal in response to varying the gain; and

adjusting the gain of the circuit in response to the magnitude of the change in the power of the received signal, said step of adjusting comprising the steps of:

decreasing the gain of the circuit when the magnitude of the change in the power of the received signal is greater than a predetermined threshold; and

increasing the gain of the circuit when the magnitude of the change in the power of the received signal is less than or equal to the predetermined threshold.

4. The method of claim 3 wherein the predetermined amount is about 3 dB and the predetermined threshold is about 9 dB.

5. The method of claim 3 wherein said step of determining magnitude of a change in the power of the received signal is performed before said step of converting the received signal from the radio frequency to an intermediate frequency.

6. The method of claim 3 wherein said step of determining a magnitude of a change in the power of the received signal is performed after said step of converting the received signal from the radio frequency to an intermediate frequency.

7. The method of claim 3 wherein said step of determining a magnitude of a change in the power of the received signal is performed after said step of filtering the received signal.

8. The method of claim 3 further comprising the step of repeating said varying, determining, and adjusting steps at a predetermined rate.

9. The method of claim 8 wherein said predetermined rate is about 10 times per second.

10. The method of claim 8 wherein said predetermined rate is once per frame.

11. A method for increasing immunity of a radiotelephone to radio frequency interference, said radiotelephone having an antenna for receiving radio signals having a received power level, an attenuator, a variable gain receive amplifier, a gain controller, and a receive power detector, the method comprising the steps of:

said gain controller varying said received power level of said received radio signals by a predetermined amount;

said receive power detector detecting a magnitude of a change in said received power level of said received radio signals in response to said gain controller varying said received power level; and

said gain controller adjusting a gain of said variable gain receive amplifier in response to said magnitude of said detected received power level change, said adjusting comprising the steps of:

said gain controller decreasing said gain of said variable gain receive amplifier when said detected received power level change is greater than a predetermined threshold; and

said gain controller increasing said gain of said variable gain receive amplifier when said detected received power level change is less than or equal to a predetermined threshold.

12. The method of claim 11 wherein said varying step comprises attenuating said received radio signals with said variable attenuator.

13. The method of claim 11 wherein said varying step comprises adjusting said gain of said variable gain receive amplifier.

14. A system for adjusting the power of a received signal having a plurality of frames in a circuit having a variable gain, the system comprising:

means for receiving the received signal at a radio frequency;

means for converting the received signal from the radio frequency to an intermediate frequency;

means for filtering the received signal;

means for varying the gain of the circuit by a predetermined amount;

means for determining a magnitude of a change in the power of the received signal in response to the varied gain; and

means for adjusting the gain of the circuit in response to the magnitude of the change in the power of the received signal, the means for adjusting including:

means for decreasing the gain of the circuit when the magnitude of the change in the power of the received signal is greater than a predetermined threshold; and

means for increasing the gain of the circuit when the magnitude of the change in the power of the received signal is less than or equal to the predetermined threshold.

15. The system of claim 14, wherein the predetermined amount is about 3 dB and the predetermined threshold is about 9 dB.

16. The system of claim 14, wherein the means for determining a magnitude of a change in the power of the received signal determines the magnitude of the change before the means for converting converts the received signal from the radio frequency to an intermediate frequency.

17. The system of claim 14, wherein the means for determining a magnitude of a change in the power of the received signal determines the magnitude of the change after the means for converting converts the received signal from the radio frequency to an intermediate frequency.

18. The system of claim 14, wherein the means for determining a magnitude of a change in the power of the received signal determines the magnitude of the change after the means for filtering filters the received signal.

19. An apparatus for increasing immunity of a radiotelephone to radio frequency interference, comprising:

an antenna for receiving radio signals;

a variable gain receive amplifier for amplifying said received signals;

a gain controller for varying a received power level of said received signals by a predetermined amount by adjusting a gain of said variable gain receive amplifier; and

a receive power detector for detecting a magnitude of a change in said received power level of said received signals in response to said gain adjustment;

wherein said gain controller adjusts said gain of said variable gain receive amplifier in response to said magnitude of said change in said received power level, said gain controller decreasing said gain of said variable gain receive amplifier when said change in said received power level is greater than a predetermined threshold, and said gain controller increasing said gain of said variable gain receive amplifier when said change in said received power level is less than or equal to said predetermined threshold.

20. An apparatus for increasing immunity of a radiotelephone to radio frequency interference, comprising:

an antenna for receiving radio signals;

a variable attenuator for attenuating said received signals;

a gain controller for varying a received power level of said received signals by a predetermined amount by adjusting an attenuation of said variable attenuator; and

a receive power detector for detecting a magnitude of a change in said received power level of said received signals in response to said attenuation adjustment,

wherein said gain controller adjusts said attenuation of said variable attenuator in response to said magnitude of said change in said received power level, said gain controller increasing said attenuation of said variable attenuator when said change in said received power level is greater than a predetermined threshold, and said gain controller decreasing said attenuation of said variable attenuator when said change in said received power level is less than or equal to said predetermined threshold.

* * * * *

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United States Patent [19]

Sevic et al.

[11] Patent Number: 5,872,481

[45] Date of Patent: Feb. 16, 1999

[54] EFFICIENT PARALLEL-STAGE POWER AMPLIFIER

[75] Inventors: John F. Sevic; Richard J. Camarillo, both of San Diego, Calif.

[73] Assignee: QUALCOMM Incorporated, San Diego, Calif.

[21] Appl. No.: 767,124

[22] Filed: Dec. 9, 1996

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 579,169, Dec. 27, 1995.

[51] Int. Cl.[6] H03F 3/68

[52] U.S. Cl. ..... 330/51; 330/124 R; 330/295

[58] Field of Search ..... 330/51, 124 R, 330/133, 134, 285, 295

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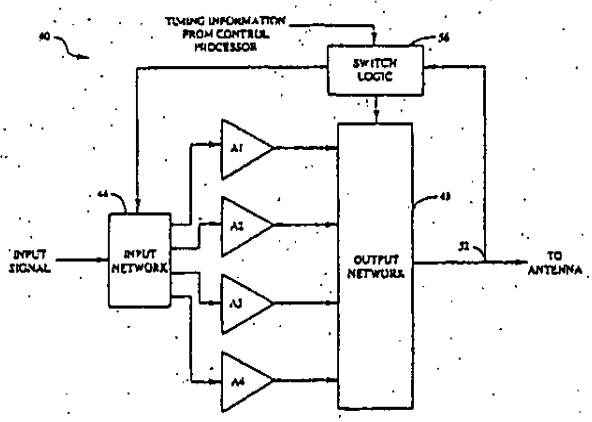
Primary Examiner—Steven Mottola.

Attorney, Agent, or Firm—Russell B. Miller; Brian S. Edmonston; Roger W. Martin

[57] ABSTRACT

An amplifier circuit for providing an amplified signal in response to an input signal. The amplifier circuit includes an input network for applying the input signal to a selected at least one of a plurality of amplifier stages. An output network is provided for coupling the amplified signal from the selected at least one amplifier stage. The appropriate amplifier stage is selected by a control circuit in response to a desired power value of the amplified signal. By selectively activating only the amplifier stage(s) that are necessary to provide the desired level of output power, increased DC efficiency can be accomplished in applications that require an amplifier which operates linearly over a wide dynamic range.

8 Claims, 12 Drawing Sheets



Ex. E-1

Ex. D-1

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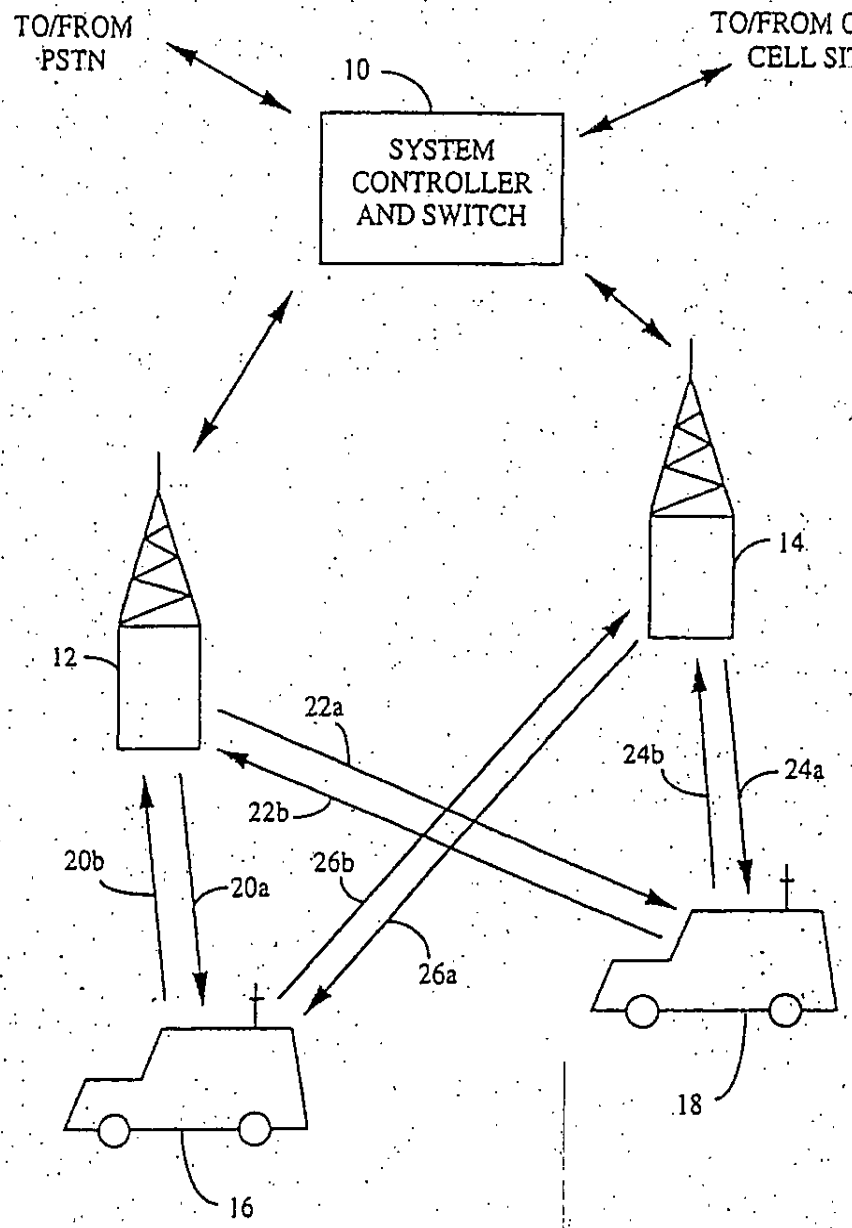

TO/FROM PSTN
10
SYSTEM CONTROLLER AND SWITCH
TO/FROM OTHER CELL SITES
12
14
22a
22b
24b
24a
20b
20a
26b
26a
16
18

FIG. 1

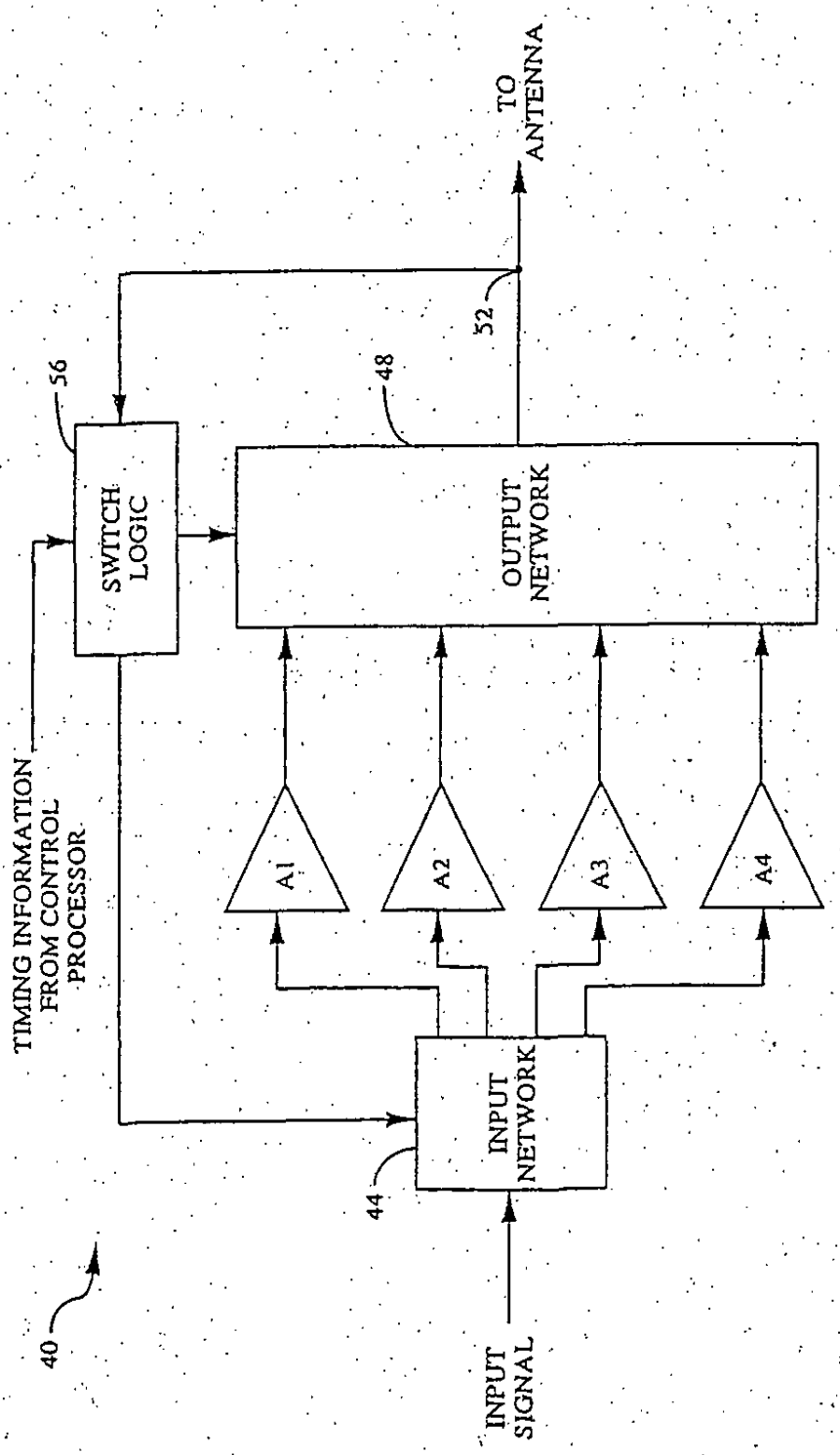
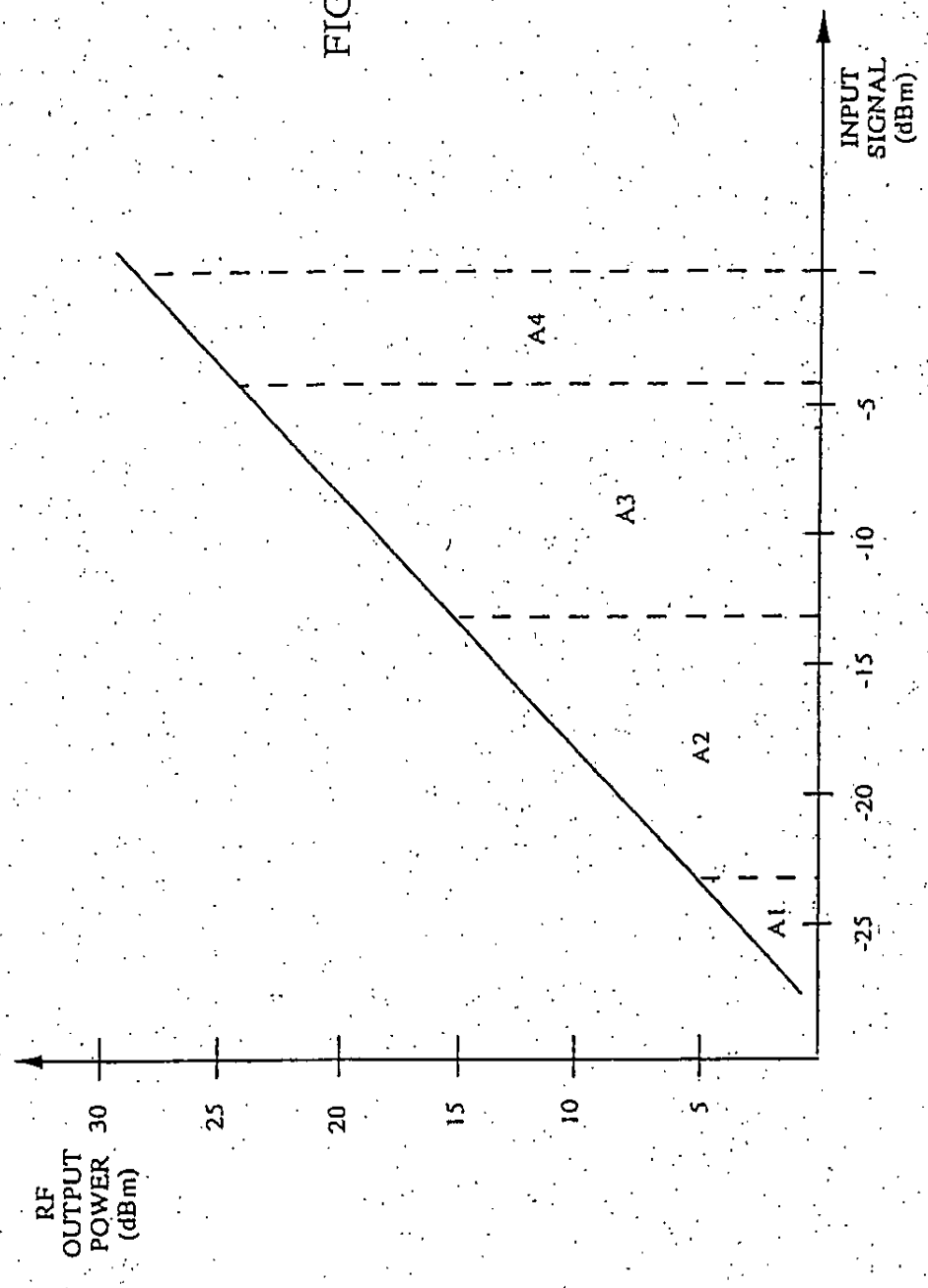

TO ANTENNA
52
48
56
SWITCH LOGIC
OUTPUT NETWORK
A1
A2
A3
A4
TIMING INFORMATION FROM CONTROL PROCESSOR
INPUT NETWORK
44
40
INPUT SIGNAL

FIG. 2

FIG. 3



Ex. E-5

Ex. D-5

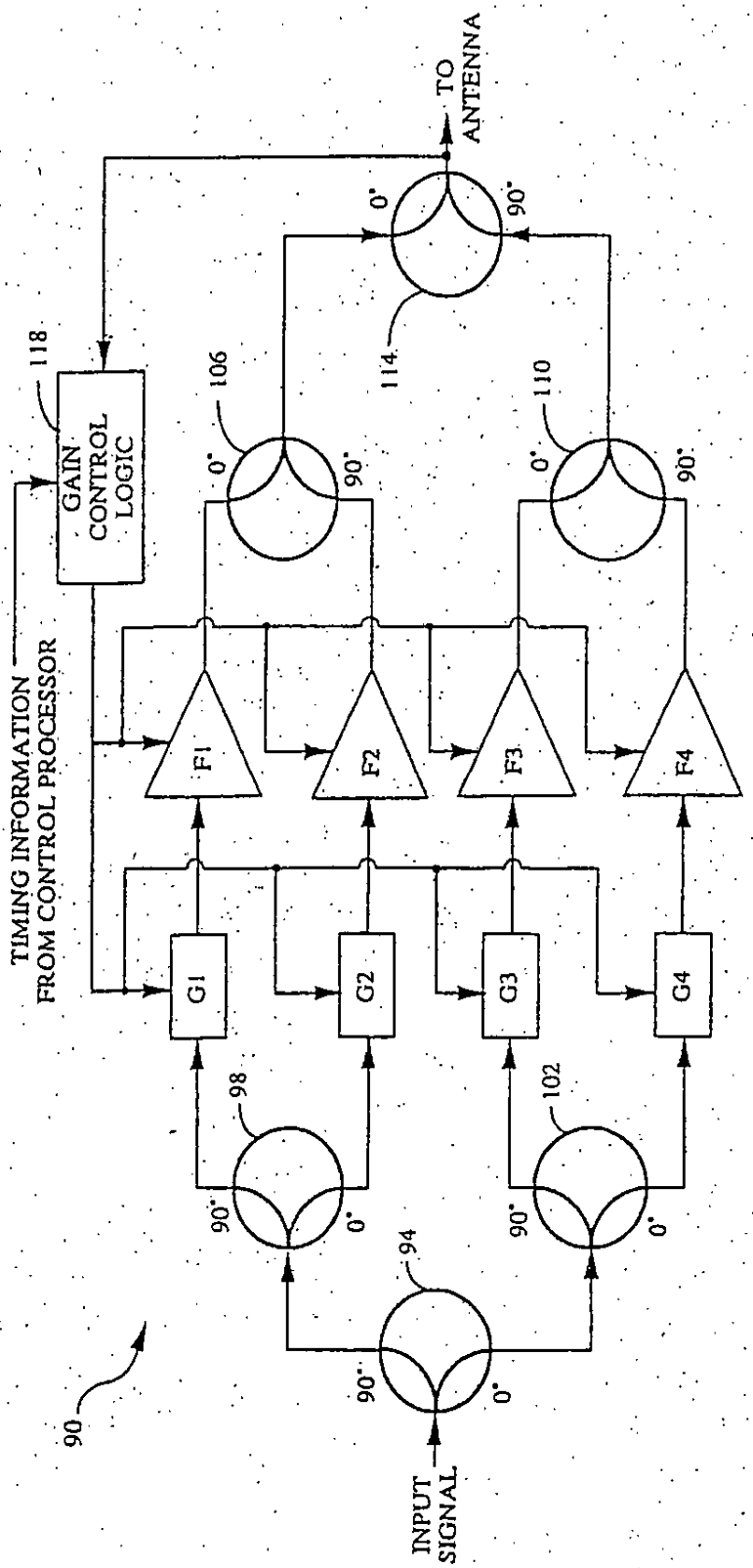

TO ANTENNA
0°
90°
114
118
GAIN CONTROL LOGIC
106
110
TIMING INFORMATION FROM CONTROL PROCESSOR
F1
F2
F3
F4
G1
G2
G3
G4
98
102
94
90
INPUT SIGNAL

FIG. 4

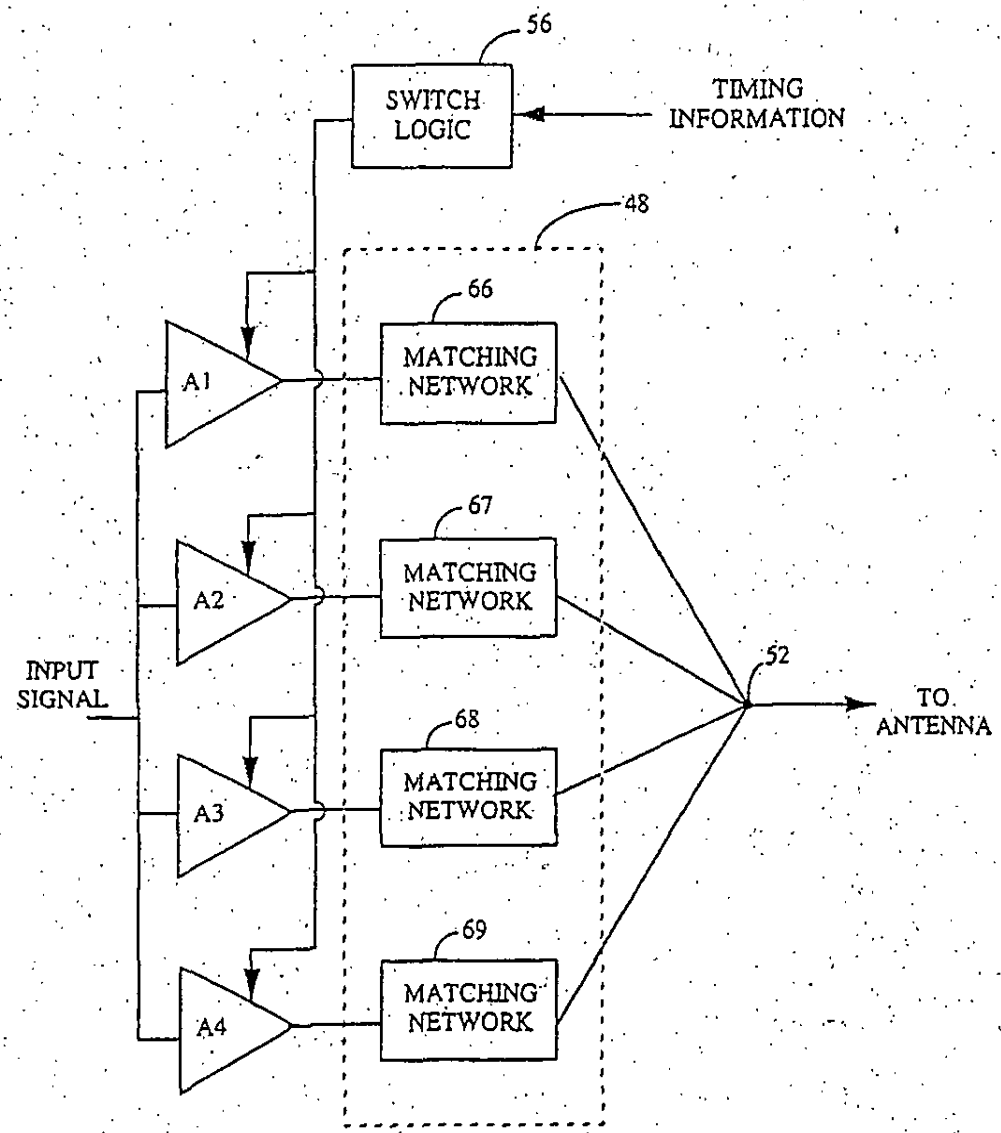

56
SWITCH LOGIC
TIMING INFORMATION
48
66
MATCHING NETWORK
67
MATCHING NETWORK
68
MATCHING NETWORK
69
MATCHING NETWORK
A1
A2
A3
A4
INPUT SIGNAL
52
TO ANTENNA

FIG. 5A

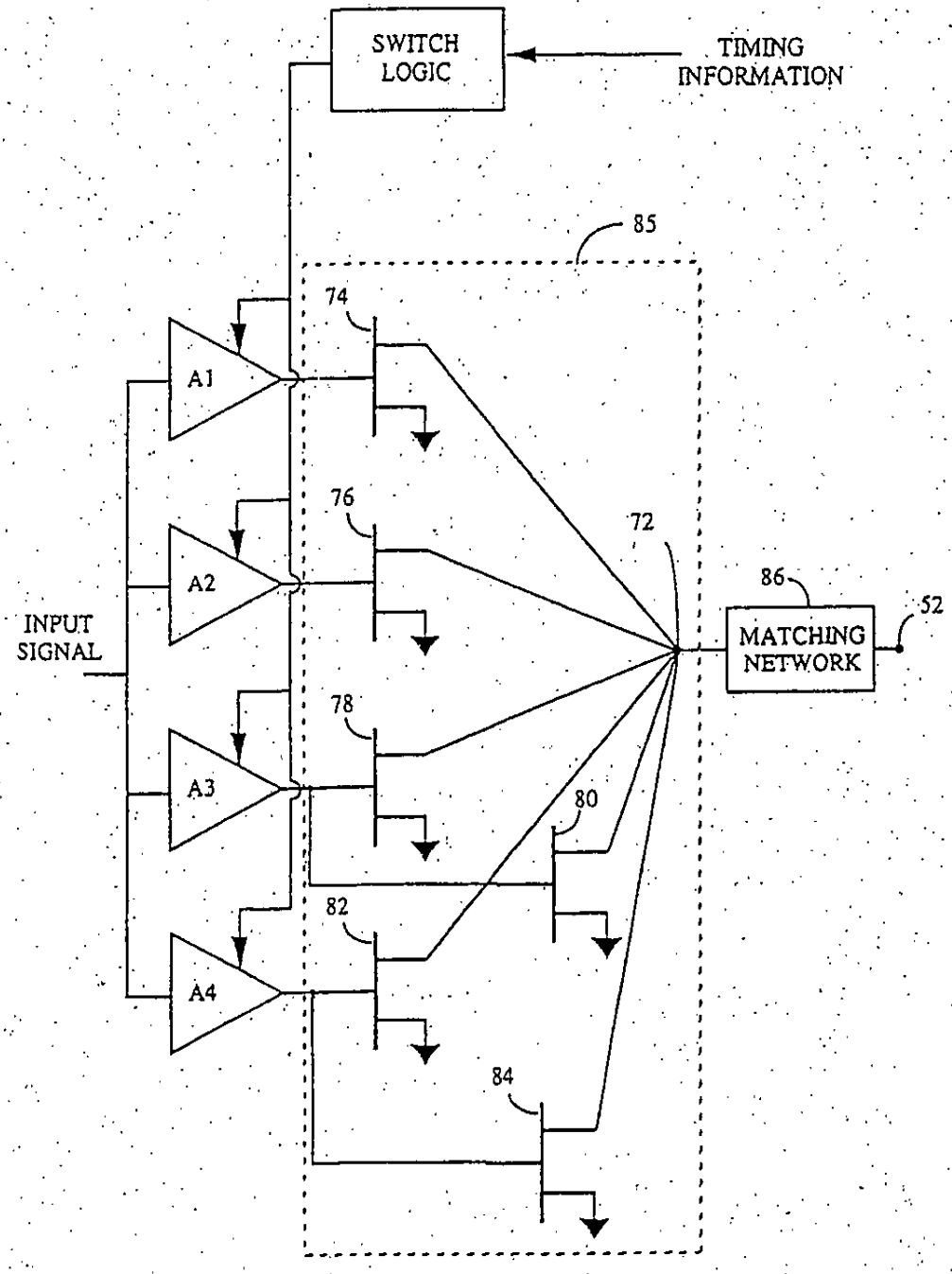

SWITCH LOGIC
TIMING INFORMATION
85
74
A1
76
A2
72
86
52
INPUT SIGNAL
MATCHING NETWORK
78
A3
80
82
A4
84

FIG. 5B

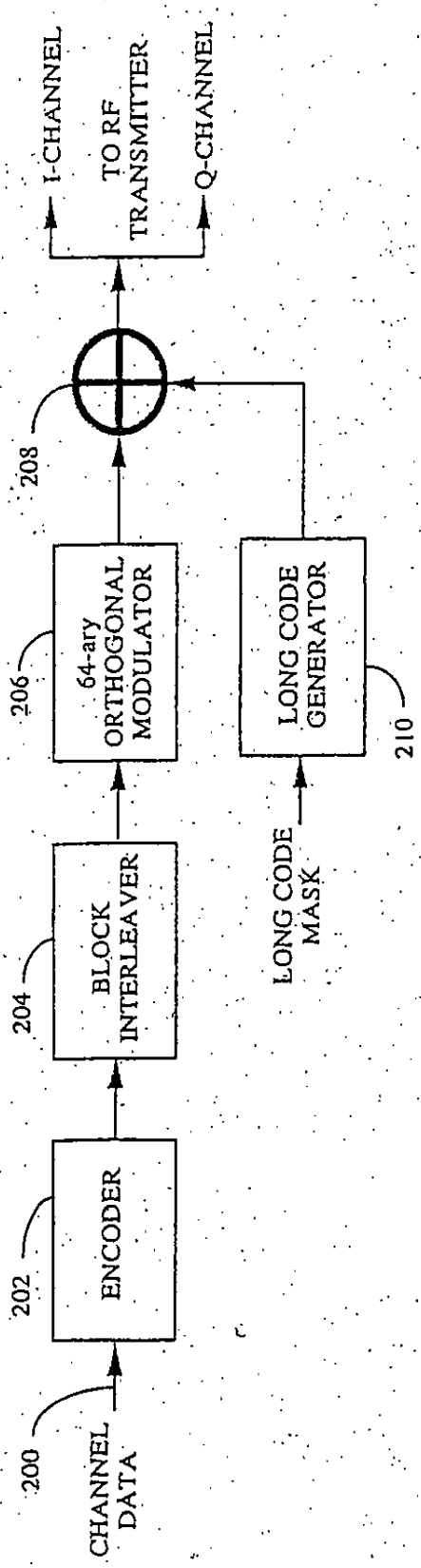

I-CHANNEL
TO RF TRANSMITTER
Q-CHANNEL
208
206
64-ary ORTHOGONAL MODULATOR
LONG CODE GENERATOR
210
LONG CODE MASK
204
BLOCK INTERLEAVER
202
ENCODER
200
CHANNEL DATA

FIG. 6

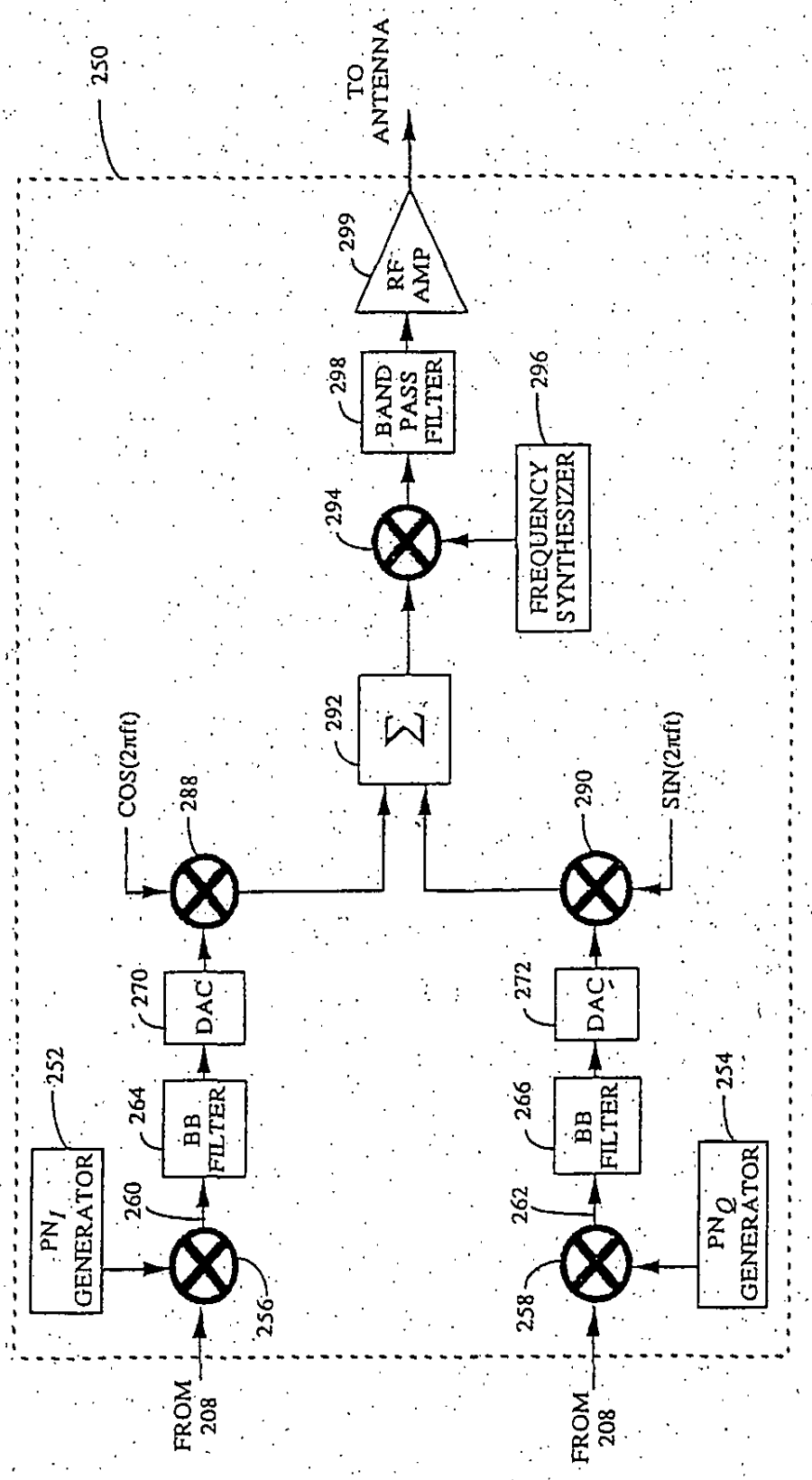

250
TO ANTENNA
299
RF AMP
298
BAND PASS FILTER
296
FREQUENCY SYNTHESIZER
294
292
COS(2πft)
288
290
SIN(2πft)
270
DAC
272
DAC
252
PN$_I$ GENERATOR
264
BB FILTER
266
BB FILTER
254
PN$_Q$ GENERATOR
260
262
256
258
FROM 208
FROM 208

FIG. 7

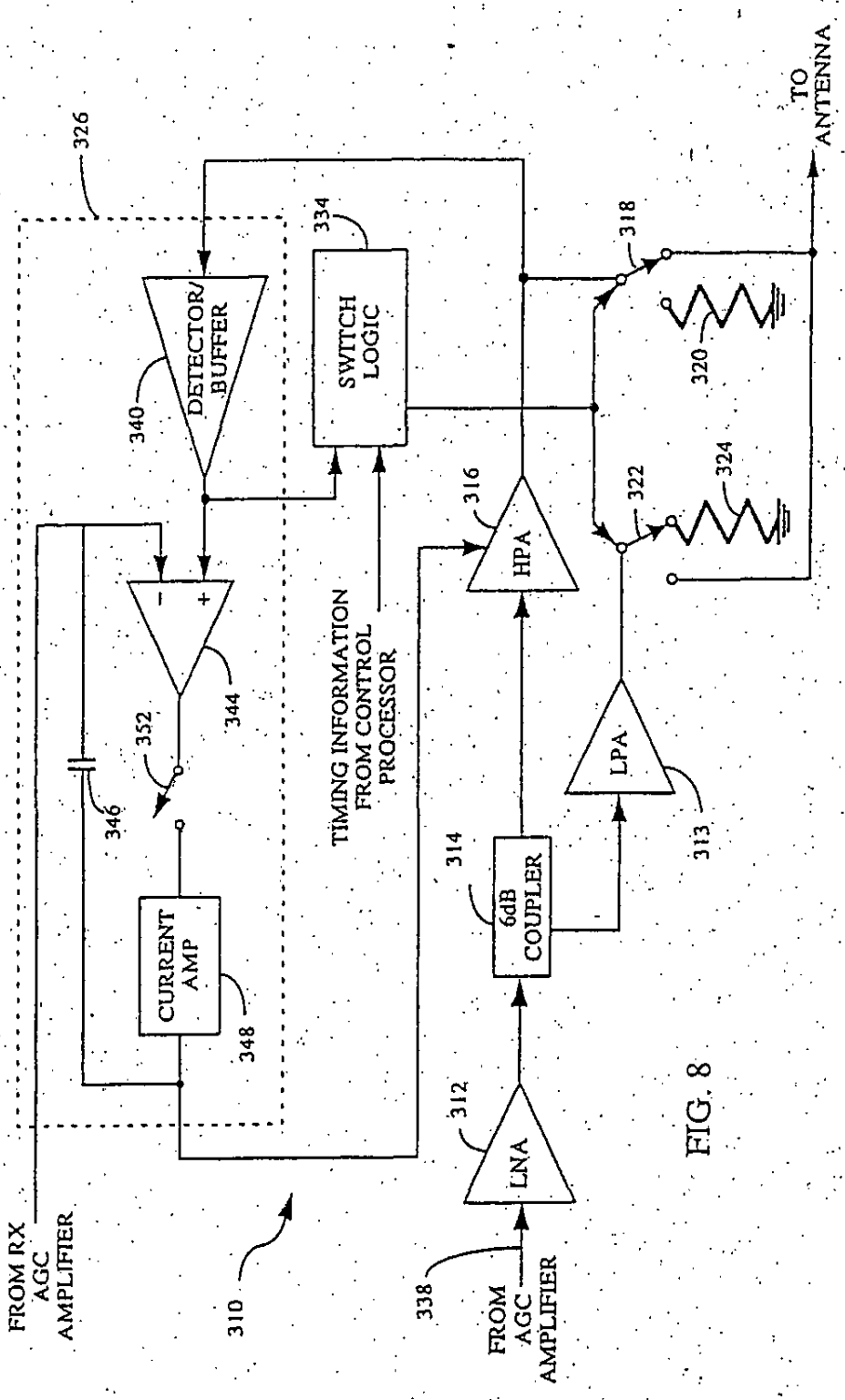

326
TO ANTENNA
334
318
DETECTOR/ BUFFER
SWITCH LOGIC
340
320
324
322
316
HPA
TIMING INFORMATION FROM CONTROL PROCESSOR
344
352
LPA
313
346
314
6dB COUPLER
CURRENT AMP
348
312
LNA
FROM RX AGC AMPLIFIER
310
338
FROM AGC AMPLIFIER

FIG. 8

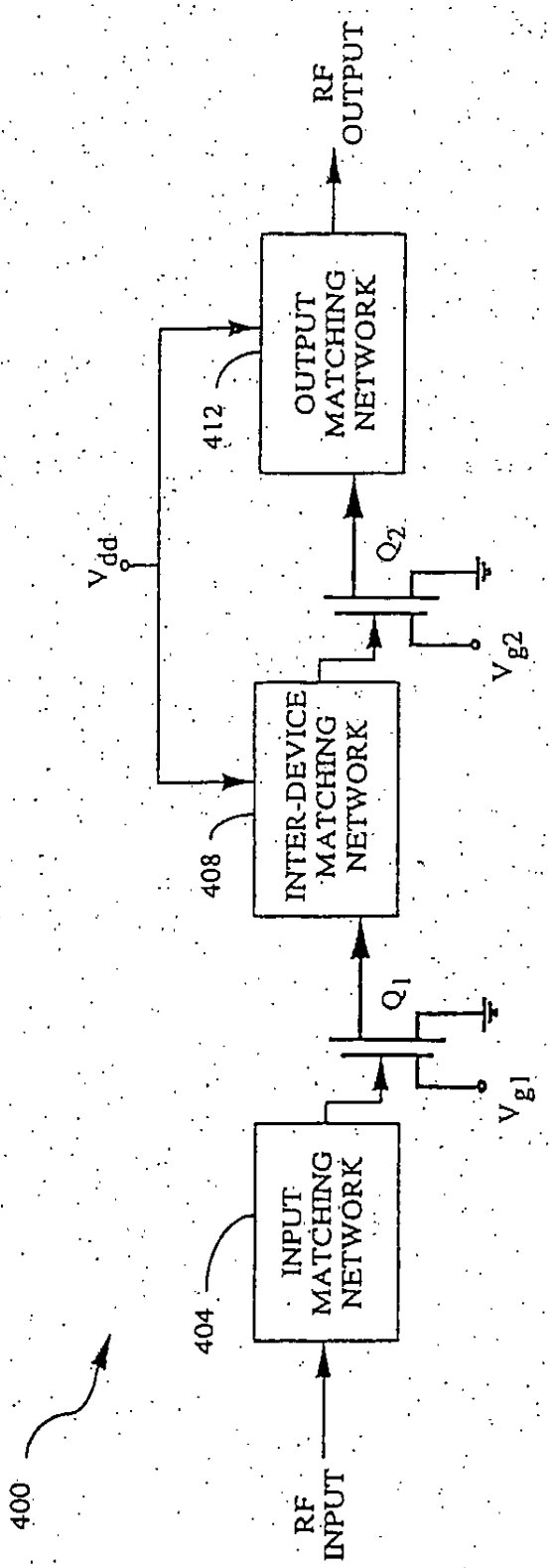

RF OUTPUT
OUTPUT MATCHING NETWORK
412
V_{dd}
Q_2
V_{g2}
INTER-DEVICE MATCHING NETWORK
408
Q_1
V_{g1}
INPUT MATCHING NETWORK
404
400
RF INPUT

FIG. 9

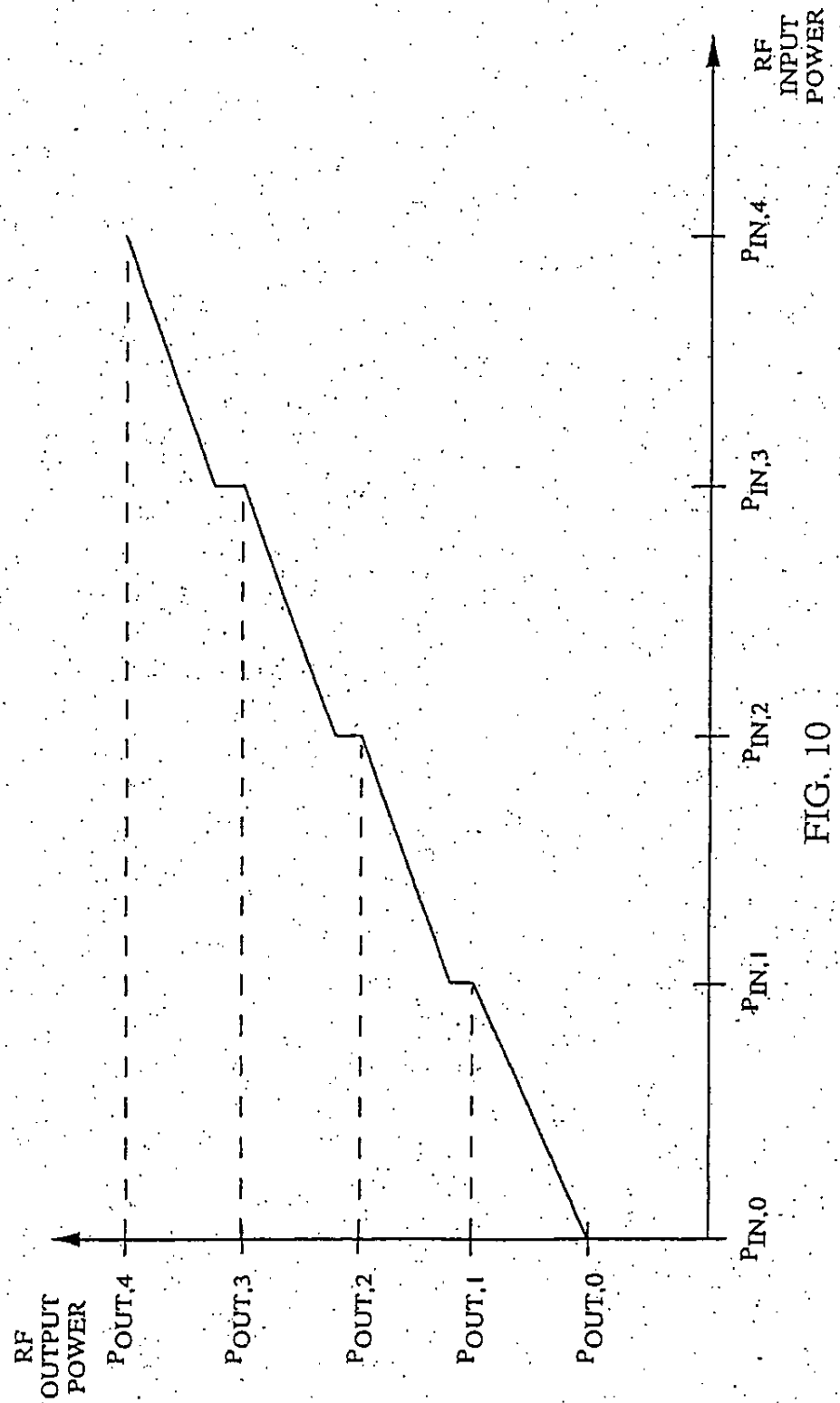


FIG. 10

Ex. E-13

Ex. D-13

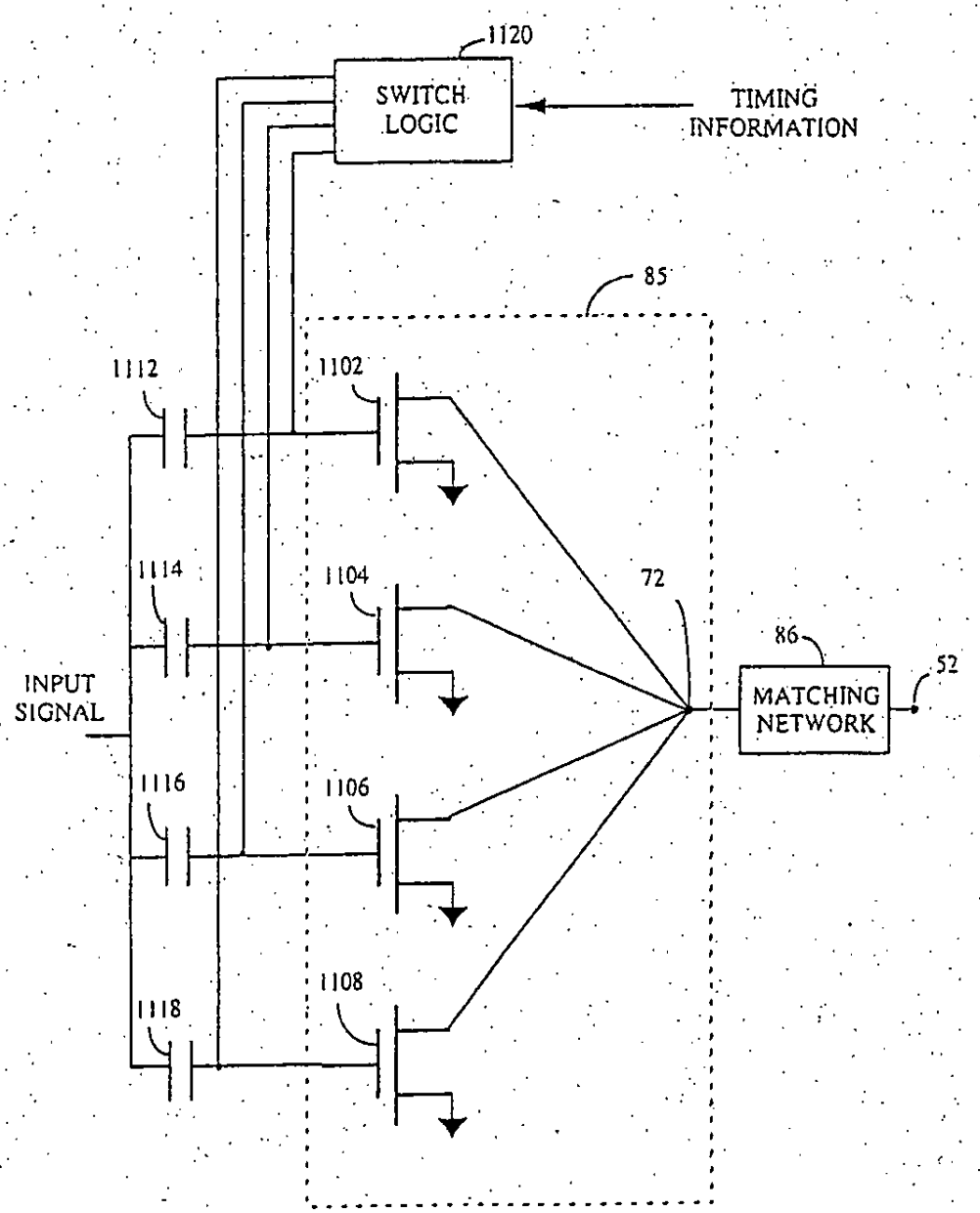

1120
SWITCH LOGIC
TIMING INFORMATION
85
1112
1102
1114
1104
72
86
52
INPUT SIGNAL
MATCHING NETWORK
1116
1106
1108
1118

FIG. 11

EFFICIENT PARALLEL-STAGE POWER AMPLIFIER

BACKGROUND OF THE INVENTION

I. Related Applications

This application is a Continuation-In-Part of U.S. patent application Ser. No. 08/579,169, filed Dec. 27, 1995, which is currently pending.

II. Field of the Invention

The present invention relates to signal amplifiers. More specifically, the present invention relates to methods and circuit arrangements for providing highly efficient, linear signal amplification over a wide dynamic range by employing multiple parallel amplifying devices.

III. Description of the Related Art

The use of code division multiple access (CDMA) modulation techniques is one of several techniques for facilitating communications in which a large number of system users are present. Although other techniques such as time division multiple access (TDMA), frequency division multiple access (FDMA), and amplitude modulation (AM) modulation schemes such as amplitude companded single sideband (ACSSB) are known, CDMA has significant advantages over these other techniques. The use of CDMA techniques in a multiple access communication system is disclosed in U.S. Pat. No. 4,901,307 entitled "SPREAD SPECTRUM MULTIPLE ACCESS COMMUNICATION SYSTEM USING SATELLITE OR TERRESTRIAL REPEATERS", assigned to the assignee of the present invention, the disclosure thereof incorporated by reference.

In the just mentioned patent, a multiple access technique is disclosed where a large number of mobile telephone system users each having a transceiver communicate through satellite repeaters or terrestrial base stations (also known as cell-site stations, or for short cell-sites) using CDMA spread spectrum communication signals. In using CDMA communications, the frequency spectrum can be reused multiple times thus permitting an increase in system user capacity. The use of CDMA results in a much higher spectral efficiency than can be achieved using other multiple access techniques. In a CDMA system, increases in system capacity may be realized by controlling the transmitter power of the portable units associated with each user so as to reduce interference to other system users.

In a terrestrial CDMA cellular communication system it is extremely desirable to maximize the capacity in terms of the number of simultaneous communication links capable of being supported by a given system bandwidth. System capacity can be maximized if the transmitter power of each portable unit is controlled such that the transmitted signal arrives at the cell-site receiver with the minimal signal to noise interference ratio which allows acceptable data recovery. If a signal transmitted by a portable unit arrives at the cell-site receiver at a power level that is too low, the bit-error-rate may be too high to permit high quality communications. If, on the other hand, acceptable communication is established by setting the mobile unit transmitted signal at a power level that is too high when received at the cell site receiver, interference will occur with other mobile unit transmitted signals that are sharing the same channel, i.e. bandwidth. This interference may adversely affect communications with other portable units unless the total number of communicating portable units is reduced.

The signals received from each portable unit at the cell-site station are measured, and the measurement results

compared with a desired power level. Based on this comparison the cell-site determines the deviation in the received power level from that which is necessary to maintain the desired communications. Preferably the desired power level is a minimum power level necessary to maintain quality communications so as to result in a reduction in system interference.

The cell-site station then transmits a power control command signal to each system user so as to adjust or "fine tune" the transmit power of the portable unit. This command signal is used by the portable unit to change the transmit power level closer to a level required to sustain communication on the reverse link between the portable unit and the cell-site. As channel conditions change, typically due to motion of the portable unit, both the portable unit receiver power measurement and the power control feedback from the cell-site station continually readjust the transmit power level so as to maintain a proper power level.

The utilization of these types of power control techniques requires that the portable unit transmitter be capable of linear operation over a relatively wide dynamic range. Since existing portable units operate on battery power, it is also necessary that the transmitter power amplifier be capable of efficient, linear operation over the dynamic range typical of CDMA communication systems. Since conventional power amplifier designs, both variable gain and fixed gain, have been found to lack the requisite efficiency and linearity over a wide dynamic range, there exists a need for a power amplifier capable of providing this type of performance.

SUMMARY OF THE INVENTION

Broadly, the invention takes the form of an amplifier circuit for providing an amplified signal in response to an input signal in a manner which improves efficiency while maintaining linearity. The amplifier circuit includes an input switch for applying the input signal to a selected one of first and second parallel-connected amplifier stages, where the first amplifier stage is biased to provide constant gain over a first input signal dynamic range and the second amplifier stage is biased to provide constant gain over a second input signal dynamic range. An output network is provided for coupling the amplified signal from the selected amplifier stage.

In a preferred embodiment the output network includes an output switch for connection to an output node of the selected amplifier stage, and further includes a power measurement circuit for measuring power of the amplified signal. A switch control circuit may be provided for controlling the connection of the input switch and the output switch to the other one of the amplifier stages when measured power of the amplified output signal departs from a predetermined output range. In a particular implementation of the invention within a digital transmitter, the switch control circuit only allows the input switch matrix and the output network to select a different one of the amplifier stages during transitions between the digital words or symbols within the input signal.

In one embodiment the input signal is provided directly to a plurality of different final stage transistor devices. The respective gates of the devices are isolated at DC by blocking capacitors, but are tied together at the RF frequency of the input signal. Switch logic selectively provides a DC bias current only to the devices which are required for amplification of the input signal. Thus, by biasing on only the devices that are required for the present amplifition of the input signal, DC efficiency is improved significantly.

BRIEF DESCRIPTION OF THE DRAWINGS

The features and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters correspond throughout and wherein:

FIG. 1 is a schematic overview of an exemplary cellular telephone system which includes at least one cell-site and a plurality of portable units;

FIG. 2 shows a simplified block diagram of a parallel stage amplifier of the present invention;

FIG. 3 illustratively represents an exemplary scheme for biasing the amplifier stages A1–A4 within the parallel stage amplifier of FIG. 2;

FIG. 4 is a block diagram of an alternate embodiment of a parallel-stage amplifier of the present invention.

FIG. 5A depicts an alternate embodiment of the present invention wherein the input and output switching functions are inherent to the amplifier stages themselves.

FIG. 5B depicts yet another embodiment of the present invention wherein the input and output switching functions are inherent to the amplifier stages themselves.

FIG. 6 provides a block diagrammatic representation of a portable unit spread spectrum transmitter in which may be incorporated an efficient parallel stage amplifier of the present invention.

FIG. 7 shows an exemplary implementation of an RF transmitter included within the spread spectrum transmitter of FIG. 6.

FIG. 8 is a block diagram of an embodiment of the inventive parallel-stage amplifier designed for low-noise signal amplification.

FIG. 9 is a schematic representation of a dual-transistor amplifier suitable for use as a single stage of the parallel stage amplifier of the invention.

FIG. 10 illustratively represents the transfer characteristic of a parallel stage amplifier of the invention in which the constituent amplifier stages are offset in gain.

FIG. 11 depicts yet another embodiment of the present invention wherein the input and output switching functions are inherent to the amplifier stages themselves.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

I. Introduction to CDMA Cellular Communications

An exemplary terrestrial cellular telephone communication system is illustrated in FIG. 1. The system illustrated in FIG. 1 utilizes CDMA modulation techniques in communications between the system portable user, and the cell-sites. Each portable user communicates with one or more cell-sites by way of a portable transceiver (e.g., portable telephones), each of which includes a transmitter in which may be incorporated an efficient parallel power amplifier of the present invention. In this discussion the term "portable unit" is used to refer generally to the remote subscriber station for the purposes of this description. Note, however, that the portable unit may be fixed in location. The portable unit may be part of a multiple user concentrated subscriber system. The portable unit may be used to carry voice, data, or a combination of signal types. The term "portable unit" is a term of art and is not meant to limit the scope or function of the unit.

In FIG. 1, system controller and switch 10 typically includes appropriate interface and processing hardware for providing system control information to the cell-sites. Controller 10 controls the routing of telephone calls from the public switched telephone network (PSTN) to the appropriate cell-site for transmission to the appropriate portable unit. Controller 10 also controls the routing of calls from the portable units via at least one cell-site to the PSTN. Controller 10 may direct calls between portable users via the appropriate cell-site stations since the portable units do not typically communicate directly with one another.

Controller 10 may be coupled to the cell-sites by various means such as dedicated telephone lines, optical fiber links or by radio frequency communications. In FIG. 1, two exemplary cell-sites, 12 and 14, are shown along with two exemplary portable units 16 and 18. Arrows 20*a*–20*b* and 22*a*–22*b* respectively define the possible communication links between cell-site 12 and portable units 16 and 18. Similarly, arrows 24*a*–24*b* and arrows 26*a*–26*b* respectively define the possible communication links between cell-site 14 and portable units 18 and 16. Cell-sites 12 and 14 normally transmit using equal power.

Portable unit 16 measures the total power received from cell-sites 12 and 14 upon paths 20*a* and 26*a*. Similarly, portable unit 18 measures the power received from cell-sites 12 and 14 upon paths 22*a* and 24*a*. In each of portable units 16 and 18, signal power is measured in the receiver where the signal is a wideband signal. Accordingly, this power measurement is made prior to correlation of the received signal with a pseudo-noise (PN) spectrum spreading signal.

When portable unit 16 is closer to cell-site 12, the received signal power typically will be dominated by the signal traveling path 20*a*. When portable unit 16 is nearer to cell-site 14, the received power typically will be dominated by the signal traveling on path 26*a*. Similarly, when portable unit 18 is closer to cell-site 14, the received power typically will be dominated by the signal on path 24*a*. When portable unit 18 is closer to cell-site 12, the received power typically will be dominated by the signal traveling on path 22*a*.

Each of portable units 16 and 18 uses the resultant measurement to estimate the path loss to the closest cell-site. The estimated path loss, together with knowledge of the portable antenna gain and the cell-site G/T is used to determine the nominal transmitter power required to obtain the desired carrier-to-noise ratio in the cell-site receiver. The knowledge by the portable units of the cell-site parameters may be either fixed in memory or transmitted in cell-site information broadcast signals, setup channel, to indicate other than nominal conditions for a particular cell-site.

As the portable units 16 and 18 move throughout the cell-sites, it becomes necessary to regulate the transmit power of each over a wide dynamic range. Although power amplifiers exist which are capable of signal amplification over a wide dynamic range, the associated gain variation tends to complicate the design of the remainder of the portable unit transmitter. In addition to exhibiting constant gain, it is also desired that the portable unit transmit amplifier conserve battery power by operating efficiently over the entire dynamic range of interest. In accordance with the invention, a highly efficient, linear gain power amplifier is provided which meets these and other objectives.

II. Overview of Efficient Parallel Power Amplifier

Turning now to FIG. 2, there is shown a simplified block diagram of a parallel-stage amplifier 40 of the present invention. An input signal, typically a digitally-modulated RF communication signal, is received by an input network 44 from an RF transmit modulator (not shown). The input network 44 relays the input signal to at least one of an exemplary set of four parallel amplifier stages A1–A4. In the simplest embodiment, input network 44 is a switch matrix

which selectively provides the input signal to one of the parallel amplifier stages A1–A4. However, other implementations of the input network 44 (see FIG. 4) may effect input switching in a manner which minimizes distortion and signal loss. In a preferred implementation the amplifier stages A1–A4 each include a high-frequency field-effect transistor (FET) or bipolar junction transistor (BJT) power amplifier.

The outputs from the amplifier stages A1–A4 are provided to an output network 48, which couples the amplified RF output signal from the selected amplifier stage, or stages, A1–A4 to an amplifier output node 52. Although the output network 48 may be realized using a switch matrix or the like, other implementations of the output network 48 described below (see FIG. 4) effect output switching in a manner which minimizes distortion and signal loss. The amplified RF signal is provided to a transmit antenna (not shown), as well as to switch logic 56. The switch logic 56 monitors the level of the amplified RF signal at output node 52, and instructs the input network 44 and output network 48 to select the amplifier stage A1–A4 designed to provide output power over a range in which is included the monitored output signal level. In an alternate embodiment, switch logic 56 may monitor a received power level or power control commands from an associated base station.

In a preferred embodiment illustrated in FIG. 3, the amplifier stages A1–A4 are each biased to provide identical gain over a different output signal range. In an exemplary embodiment, the amplifier stage A1 is biased so as to provide approximately 28 dB of linear gain for output power of up to 5 dBm in response to input signals of up to −23 dBm. Similarly, the amplifier stages A2, A3 and A4 are each biased to produce the same linear gain as stage A1 over different output signal ranges. Specifically, in the exemplary embodiment of FIG. 3 the amplifier stage A2 produces output signal energy over the range of 5–15 dBm in response to input signals between −23 to −13 dBm, while amplifier stages A3 and A4 provide output signal energy of between 15–24 dBm and 24–28 dBm for input signals between −13 to −4 dBm and −4 to +1 dBm, respectively. When the amplifier stages are implemented as FET or BJT devices, a bias network (not shown) may be employed to supply the level of bias current to each amplifier stage required for operation over the specified output range. It should be noted that the gain values and ranges of FIG. 3 are intended to serve as a specific example, and that quite different input and output power ranges may be associated with alternate implementations.

Considering again the specific case of FIG. 3, assume that the input signal level is increasing and is approaching −23 dBm. In this instance the input signal will continue to be applied to the amplifier stage A1 until switch logic 56 senses that the level of the RF output signal has risen to approximately 5 dBm. At this juncture switch logic 56 commands the input network 44 to apply the input signal to amplifier stage A2, and instructs the output network 48 to begin coupling the resultant amplified RF output signal from A2 to output node 52. A similar transition between amplifier stages A2 and A3, and between stages A3 and A4, is controlled by switch logic 56 upon the RF output signal level approaching 15 and 24 dBm, respectively. Optionally, switch logic 56 may provide for hysteresis to prevent excessive switching between adjacent amplifier stages A1–A4 when the input signal level varies while near a transitional boundary. Since each of the amplifier stages A1–A4 is realized to exhibit an identical gain over a specified RF output signal range, the parallel amplifier 40 appears to surrounding circuit elements as a unitary amplifier having constant gain over the entire output range. This characteristic of the invention advantageously simplifies the design associated RF transmit circuitry, since it obviates the need to accommodate gain variation over the output signal range. It should be noted that although preferably only one of individual amplifier stages A1–A4 described by FIG. 3 may be turned ON at one time, other embodiments, described below, may turn ON/OFF varying combinations of amplifier stages at one time to obtain the desired RF output.

As is indicated by FIG. 2, timing information relating to boundaries between the digital words or symbols inherent within the digitally-modulated input signal is provided to switch logic 56 from the local control processor. In accordance with another aspect of the invention, the switch logic 56 only instructs the input network 44 and output network 48 to select a different one of the amplifier stages A1–A4 during transitions between the digital words or symbols within the input signal. This ensures that any phase difference between the signal paths through the amplifier stages A1–A4 does not corrupt the integrity of the digital information carried by the amplified RF output signal. For example, in the exemplary CDMA modulation format described below, a digital input data stream is encoded using a set of orthogonal Walsh codes, or "symbols". In this embodiment, switch logic 56 is enabled to instruct the input network 44 and output network 48 to switch between amplifier stages A1–A4 only during transitions between Walsh symbols. Since in an exemplary embodiment the period of each Walsh symbol is very short (e.g., 3.25 ms) relative to the rate of change of the RF output power, a number of opportunities will typically be available for switching between amplifier stages proximate the time of crossing of the RF output signal level into a different output range.

Turning now to FIG. 4, a block diagram is provided of an alternate embodiment of a parallel-stage amplifier 90 of the present invention. An input signal, again typically a digitally-modulated RF communication signal, is received by a first quadrature-phase divider 94. The first quadrature-phase divider 94 divides the input signal into a pair of input signal components of equivalent magnitude and quadrature phase. The quadrature-phase signal components from the first divider 94 are provided to second and third quadrature-phase dividers 98 and 102. The second divider 98 provides quadrature-phase outputs to gain adjustment elements G1 and G2, and the third divider 102 provides quadrature-phase outputs to gain adjustment elements G3 and G4. The gain adjustment elements G1–G4 are each serially connected to a corresponding one of fixed-gain amplifiers F1–F4, with each serial connection of a gain adjustment element and a fixed-gain amplifier forming an adjustable-gain amplifier stage.

The outputs of the adjustable-gain amplifier stages are combined using an arrangement of first, second and third quadrature-phase combiners 106, 110 and 114. The resultant amplified output signal is forwarded to a transmit antenna (not shown), as well as to gain control logic 118. Gain control logic 118 operates to set the overall amplifier gain by selecting various combinations of the adjustable-gain amplifier stages, and by setting the gain of each adjustable-gain stage. In the exemplary embodiment of FIG. 4, each of the fixed gain amplifiers F1–F4 are biased to provide an identical nominal gain of N dB, and each gain-adjustment element G1–G4 may be set at a gain/attenuation of −3 dB, or at 0 dB. This allows a desired level of RF output power to be produced by setting the gain of selected ones of the adjustable-gain amplifier stages as indicated below in TABLE I.

TABLE I

RF Output	Amplifiers	Gain-Adjustment Settings			
Power	Selected	G1	G2	G3	G4
N dB	F1, F2, F3, F4	-3 dB	-3 dB	-3 dB	-3 dB
(N - 3) dB	F1, F2	0 dB	0 dB	—	—
(N - 6) dB	F1	0 dB	—	—	—

Referring to the first row of entries within TABLE I, when each of the amplifiers F1–F4 are actuated, and each of the gain-adjustment elements G1–G4 are set to −3 dB, an RF output power of N dB is produced. If the level of the input signal decreases such that the RF output power approaches (N−3) dB, then fixed-gain amplifiers F3 and F4 are turned-off and gain-adjustment elements G1 and G2 are set to 0 dB. As is indicated by TABLE I, when fixed-gain amplifiers F3 and F4 are turned off the setting of gain-adjustment elements G3 and G4 becomes irrelevant. If it is then subsequently desired to reduce the RF output power level to (N−6) dB, fixed-gain amplifier F2 is turned off and the gain-adjustment elements G1 is returned to a setting of 0 dB. Again, timing information from the control processor allows gain control logic 118 to switch the fixed-gain amplifiers F1–F4 ON/OFF only during transitions between the digital words or symbols inherent within the input signal, and gain control logic 118 may provide for hysteresis to avoid excessive switching of gain-adjustment elements G1–G4 and fixed-gain amplifiers F1–F4 when the output power varies near a switching boundary.

The output impedance of the amplifier stages is unimportant when they are turned OFF due to first, second and third quadrature-phase combiners 106, 110 and 114. However, DC efficiency is maintained by turning on only those amplifier stages F1–F4 which are needed to produce the desired RF output power.

It should be noted that although FIG. 4 represents a preferred embodiment, other embodiments using phase shifting and combining are also possible. For example, the gain-adjustment elements G1–G4 could be replaced by only two gain-adjustment elements, each positioned immediately before quadrature-phase dividers 98 and 102, respectively. Alternatively, a single gain-adjustment element could be positioned immediately before quadrature-phase divider 94. In the extreme, the gain-adjustment elements G1–G4 could be eliminated altogether, with the resulting change in overall gain of the amplifier 90 being compensated for by other circuitry in the system employing the present invention. Furthermore, quadrature-phase dividers 94, 98, and 102, as well as quadrature-phase combiners 106, 110, and 114 could be replaced by any type of phase shifter. It is also noteworthy that the number of quadrature-phase dividers and combiners is driven only by the number of parallel amplification stages.

Referring now to FIG. 5A, yet another embodiment of the present invention is depicted in which selection between amplifier stages is accomplished by turning ON/OFF the transistor amplifier(s) comprising each stage. In the embodiment of FIG. 5A, each amplifier stage A1–A4 is assumed to be comprised of one or more field-effect transistor (FET) devices. However, it is understood that each of these amplifier stages could be a BJT or other active device. A given stage is selected by activating the FET devices comprising the stage, and is deselected by turning OFF the given FET devices and ensuring that the output impedance of the powered-off FETs is high to minimize adverse loading by the powered-off FETs. In this way, additive combination of a desired number of stages is achieved by selectively turning ON/OFF the FET devices for each stage A1–A4. In contrast to the embodiment of FIG. 2, both the input switching function and the output switching function are inherent to the FET devices themselves. Thus, switch logic 56 controls amplifier stages A1–A4 directly.

The output network 48 includes matching elements 66–69 connected respectively between the amplifier stages A1–A4 and the output node 52. The matching elements 66–69 serve to provide an optimum power match between the outputs of the amplifier stages A1–A4 and the antenna (not shown) coupled to output node 52. Each combination of an amplifier stage A1–A4 and an associated matching element 66–69 provides nearly equivalent signal gain, and each such combination is turned ON/OFF by switch logic 56 as necessary to achieve a desired level of output power. Accordingly, only the number of amplifier stages A1–A4 required to produce the desired level of output power are turned ON at any given instant of time, thereby conserving DC power and maintaining nearly constant efficiency. Furthermore, by using the individual stages A1–A4 to accomplish the output switching function, and an output network 48 which comprises matching elements 66–69, one may avoid power loss and signal distortion through a switch.

FIG. 5B shows yet another embodiment of the present invention, in which one or more amplifier gain cells or transistors are interposed between the output of each amplifier stage A1–A4 intermediate node 72. FIG. 5B is similar to FIG. 5A. However, instead of individual matching networks 66–69 for each amplifier device, a final amplifier device 85, comprising multiple gain cells 74–84 within the final amplifier device 85, is coupled to a single matching network 86. In the exemplary embodiment of FIG. 5B, a single gain cell transistor 74 is connected between stage A1 and the intermediate node 72. Similarly, single gain cell transistor 76 is connected between stage A2 and the intermediate node 72. A pair of gain cell transistors 78, 80 are connected between stage A3 and the intermediate node 72, and another pair of gain cell transistors 82, 84 are connected between stage A4 and the intermediate node 72. In contrast to the output network depicted in FIG. 5A, the implementation of FIG. 5B uses a single final amplification device 85 in which each of the individual gain cells 74–84 within the final amplification device 85 may have a separate input. This allows for a reduction in physical size and cost, and permits fabrication of the final amplification device 85 upon a single die. As in the embodiment of FIG. 5A, no output switch is required because if gain cell 74–84 are either BJTs or FETs, biasing them off puts their respective outputs in a high impedance state, with minimal real loading.

Each gain cell 74–84 is turned ON/OFF via a bias current provided by its preceding amplifier stage A1–A4. By turning ON/OFF a particular set of the gain cell transistors, a desired level of output power is accommodated. It is noted in this exemplary embodiment that when stage A3 or A4 is activated, sufficient bias current is produced to turn ON both gain cell transistors (78,80) or (82,84), respectively. It should also be noted that although amplifier stages A3 and A4 each drive two separate cell transistors (78,80) and (82,84), respectively, alternate embodiments may use more or fewer gain cell transistors in each stage.

Consider now an exemplary implementation of the amplifier of FIG. 5B in which each gain cell transistor 74–84 is designed to provide approximately 1 Watt of power when biased ON by its preceding amplifier stage A1–A4. TABLE II lists the different levels of output power produced by this exemplary implementation when various combinations of

gain cell transistors are biased ON by their respective amplifier stages A1–A4. Examining TABLE II, one can see that by turning ON either amplifier stage A1 or A2, the total RF output power may be increased by one watt, while turning on either amplifier stage A3 or A4, the total RF output power may be increased by two watts. Thus, according to the method of TABLE II, the specific embodiment of FIG. 5B can be used to generate varying RF output power levels from one to six watts, using four amplifier stages A1–A4, and maintaining DC efficiency by biasing ON only those stages that are necessary to generate the desired output power. Note that TABLE II represents merely an exemplary implementation, and that gain cell transistors 74–84 each could be designed to provide more or less than one watt. However, selecting each gain cell 74–84 to be the same size simplifies manufacturing of the final amplification device 85.

In the specific implementation of FIG. 5B represented by the first row of TABLE II, if only one amplifier stage and its associated gain cell transistor, for example A1 and transistor 74, is biased ON, with all others A2–A4 biased off, the reactive loading of the off-state transistors (76, 78, 80, 82, 84) may not provide optimum gain matching when using only a single output matching circuit 86. However, improved DC efficiency at the low output level, for example 1 watt as indicated by TABLE II, is achieved. Furthermore, any gain mismatch may be adjusted for in the individual amplifier stages selected, in this case A1, or in the associated system where the invention is employed.

TABLE II

Amplifier Stage and Gain Cell(s)				Total RF Output
A1 (74)	A2 (76)	A3 (78, 80)	A4 (82, 84)	Power (Watts)
ON	OFF	OFF	OFF	1
OFF	OFF	ON	OFF	2
ON	OFF	ON	OFF	3
OFF	OFF	ON	ON	4
ON	OFF	ON	ON	5
ON	ON	ON	ON	6

Yet another embodiment, similar to that of FIG. 5B is shown in FIG. 11. The embodiment of FIG. 11 differs from that of FIG. 5B in that the input signal does not pass through four individually switched driver amplifiers, but rather is provided directly to four different final stage transistor devices, 1102, 1104, 1106, and 1108. It should be noted that any one or all of the devices 1102–1108 may be either single or multiple-gate devices and that the configuration shown is merely exemplary. Additionally, although the devices 1102–1108 are illustrated in FIG. 11 as FET devices sharing a common gate and common drain, as was previously mentioned with respect to the previous Figures, they may also be BJT devices sharing a common emitter and common base, or a combination of different device types as may be permitted to be manufactured on a single die. Additionally, each of the devices 1102–1108 may be of different gain values.

The respective gates of the devices 1102–1108 are isolated at DC by blocking capacitors 1112, 1114, 1116, and 1118, but are tied together at the RF frequency of the input signal. Switch logic 1120 selectively provides a DC bias current only to the devices 1102–1108 which are required for amplification of the input signal. Thus, by biasing on only the devices that are required for the present amplifition of the input signal, DC efficiency is improved significantly. As a result, a final stage amplification scheme similar to that of TABLE II above may be implemented. An input matching network (not shown), preferably optimized for best performance with all devices 1102–1108 active, may also be included.

III. Dual-Transistor Amplifier Stage

FIG. 9 is a schematic representation of a dual-transistor amplifier 400 suitable for use as a single stage (e.g., as one of the stages A1–A4) within the parallel stage amplifier of the invention. The amplifier stage 400 includes an input driver FET (Q1) and an output FET (Q2). Although in FIG. 9 a pair of dual-gate field-effect transistors (Q1, Q2) comprise the amplifier stage 400, it is understood that in alternate embodiments single-gate field effect transistors (FET), or bipolar junction transistors (BJT) or transistors realized using other device technologies may be employed.

The small signal input to the amplifier 400 is applied to the gate of FET Q1 through an input matching network 404, which is designed to optimize power transfer into FET Q1. Similarly, an inter-device matching network 408 serves to maximize power transfer from the output of FET Q1 to the input of FET Q2. In like manner an output matching network 412 provides an optimum power match between the output impedance of FET Q2 and the load (not shown) driven by the amplifier 400.

The quiescent bias currents through FETs Q1 and Q2 are controlled through adjustment of the DC gate potentials V_{g1} and V_{g2}, respectively. Typically, the DC gate potentials V_{g1} and V_{g2} are set such that the amplifier 400 exhibits constant gain over low and high output power levels. In the embodiment of FIG. 9, the dimensions of input FET Q1 are selected to be smaller than the corresponding dimensions of output FET Q2 by an exemplary ratio of approximately 8:1, it being understood that other ratios may be more suitable for alternate implementations. This design leads to enhanced efficiency by enabling the bias current supplied to output FET Q2 to be substantially reduced when only low levels of output power are required from the amplifier 400. When only a low level of output power is required, the bias current through FET Q2 is reduced relative to the bias current required for an intermediate level of output power, and the bias current through FET Q1 is somewhat increased. Since the smaller input FET Q1 is capable of operating more efficiently than the larger output FET Q2 for low output power levels, the efficiency of the amplifier 400 is increased by substantially reducing the bias current through FET Q2 during low-power operation. Changes in bias current may be effected by controlling the DC gate potentials V_{g1} and V_{g2} in an analog fashion, or through adjustment in discrete steps.

IV. Efficient Power Amplifier within a CDMA Portable Unit

Referring to FIG. 6, there is shown a block diagrammatic representation of a portable unit spread spectrum transmitter in which may be incorporated an efficient parallel stage amplifier of the present invention. In an exemplary CDMA system, orthogonal signaling is employed to provide a suitable ratio of signal to noise on the portable unit-to-base station link, i.e., on the "reverse" link.

In the transmitter of FIG. 6, data bits 200 consisting of, for example, voice converted to data by a vocoder, are supplied to an encoder 202 where the bits are convolutionally encoded. When the data bit rate is less than the bit processing rate of the encoder 202, code symbol repetition may be used such that encoder 202 repeats the input data bits 200 in order to create a repetitive data stream at a bit rate which matches the operative rate of encoder 202. In an exemplary embodiment the encoder 202 receives data bits 200 at a nominal bit rate (R_s) of 11.6 kbits/second, and produces

Ex. E-19

Ex. D-19

R_s/r=34.8 symbols/second, where "r" denotes the code rate (e.g. ½) of the encoder 202. The encoded data is then provided to block interleaver 204 where it is block interleaved.

Within the 64-ary orthogonal modulator 206, the symbols are grouped into characters containing $\log_2 64$=6 symbols at a rate of $(1/r)(R_s/\log_2 64)$=5,800 characters/second, with there being 64 possible characters. In a preferred embodiment each character is encoded into a Walsh sequence of length 64. That is, each Walsh sequence includes 64 binary bits or "chips", there being a set of 64 Walsh codes of length 64. The 64 orthogonal codes correspond to Walsh codes from a 64 by 64 Hadamard matrix wherein a Walsh code is a single row or column of the matrix.

The Walsh sequence produced by the modulator 206 is seen to be provided to an exclusive-OR combiner 208, where it is then "covered" or multiplied at a combiner with a PN code specific to a particular portable unit. Such a "long" PN code is generated at rate Rc by a PN long code generator 210 in accordance with a user PN long code mask. In an exemplary embodiment the long code generator 210 operates at an exemplary chip rate, R_c, of 1.2288 Mhz so as to produce four PN chips per Walsh chip. In accordance with the invention, an efficient parallel stage amplifier within the portable unit transmitter is permitted to change state only between those PN chips at the boundary of each Walsh code symbol (i.e, after the last, and prior to the first, PN chip of successive code symbols).

Referring to FIG. 7, there is shown an exemplary implementation of the RF transmitter 250. In code division multiple access (CDMA) spread spectrum applications, a pair of short PN sequences, PN_I and PN_Q, are respectively provided by a PN_I generator 252 and by a PN_Q generator 254 to exclusive-OR combiners 256 and 258. The PN_I and PN_Q sequences relate respectively to in-phase (I) and quadrature phase (Q) communication channels, and are generally of a length (32,768 chips) much shorter than the length of each user long PN code. The resulting I-channel code spread sequence 260 and Q-channel code spread sequence 262 are then passed through baseband filters 264 and 266, respectively.

Digital to analog (D/A) converters 270 and 272 are provided for converting the digital I-channel and Q-channel information, respectively, into analog form. The analog waveforms produced by D/A converters 270 and 272 are provided along with local oscillator (LO) carrier frequency signals $\cos(2\pi ft)$ and $\sin(2\pi ft)$, respectively, to mixers 288 and 290 where they are mixed and provided to summer 292. The quadrature phase carrier signals $\sin(2\pi ft)$ and $\cos(2\pi ft)$ are provided from suitable frequency sources (not shown). These mixed IF signals are summed in summer 292 and provided to mixer 294.

Mixer 294 mixes the summed signal with an RF frequency signal from frequency synthesizer 296 so as to provide frequency upconversion to the RF frequency band. The RF may then be bandpass filtered 298 and provided to an efficient parallel stage RF amplifier 299 of the invention. Again, the portable unit controller ensures proper phase is maintained by allowing the selected combination of amplifier stages within the amplifier 299 to be changed only between the PN chips defining the transitions between each Walsh code symbol.

V. Dual-Stage Parallel Amplifier in a CDMA Portable Unit

FIG. 8 is a block diagram a parallel-stage amplifier 310 designed for signal amplification over a wide dynamic range in a CDMA portable unit such as that described above and illustrated in FIGS. 6 and 7. Amplifier 310 includes parallel amplification stages represented by low-power amplifier (LPA) 313 and high power amplifier (HPA) 316, an output switch matrix represented by first and second switches (318, 322), first and second dummy loads (320, 324), and switch logic 334. Briefly, amplifier 310 yields improved DC efficiency by exclusively utilizing LPA 313, which draws a low level of DC current, when only low levels of output power are required and exclusively utilizing HPA 316 when high levels of output power are required. This efficiency is accomplished by the operation of switch logic 334, alternatively directing the respective outputs of LPA 313 and HPA 316 between first and second dummy loads (320, 324) and an antenna (not shown). During low-power operation, switch logic 334 directs first switch 318 to provide the output of HPA 316 to first dummy load 320, and directs second switch 322 to provide the output of LPA 313 to an antenna (not shown). As more transmit power is required, HPA 316 begins to produce the same power as is being transmitted by LPA 313, the output of HPA 316 being dumped into first dummy load 318. At the proper switching boundary, switch logic 334 directs first switch 318 to provide the output of HPA 316 to an antenna (not shown), and directs second switch 324 to provide the output of LPA 313 to second dummy load 324.

In the preferred embodiment the LPA 313 functions as a class A amplifier during low-power mode operation. That is, the LPA 313 provides a power gain independent of the level of the RF input signal provided thereto while the LPA 313 is not in compression. Furthermore, as a class A amplifier, LPA 313 consumes nearly constant DC power regardless of its RF output power level, again as long as LPA 313 is not in compression. During operation in low-power mode the level of output power provided to the antenna is essentially controlled by adjusting the level of RF input power provided to the LPA 313. Because LPA 313 provides uniform gain during low-power mode operation, linearly tracking the input power with minimum distortion, the RF output power level produced by LPA 313 is effectively controlled by AGC amplifier (not shown) preceding LNA 312.

In accordance with the invention, the output power appearing at the output of the HPA 316 is matched to the output power produced by the LNA 313 during a transition period immediately preceding any switch between low-power and high-power modes of operation. In particular, during the transition period the power produced by HPA 316 is monitored by a gain control loop 326. The gain control loop 326 sets the gain of the HPA 316 during the transition period to be equivalent to the gain of amplifier 313, thereby equalizing the power level at the outputs of the LNA 313 and the HPA 316. In this way a "seamless" transition is effected from low-power to high-power mode, and vice-versa. In an exemplary CDMA implementation, switch logic 334 only permits the switches 318 and 322 to be toggled at Walsh code symbol boundaries.

During high-power mode the HPA 316 operates essentially as a either a class AB or a class B amplifier. That is, the power gain and DC power consumption of the amplifier 316 are a function of the RF input power level. In the preferred embodiment, HPA 316 comprises at least one FET. Since the gate voltage of an FET amplifier affects the amount of current drawn by the FET and the FET gain, higher DC efficiency can be obtained by matching the minimum FET current required for a certain level of operation to the desired RF output power level. Since HPA 316 gain is non-linear over the desired operating range, the level of the RF signal produced by the amplifier 310 may not be controlled exclusively by adjusting the signal level provided

to the HPA 316. Rather, gain control loop 326 operates to set the gain of the HPA 316 in order that a desired level of RF power is delivered to the antenna.

As is indicated by FIG. 8, the gain control loop 326 includes a detector/buffer 340 connected to the output of HPA 316. The detector/buffer 340 drives a loop integrator comprised of operational amplifier 344 and capacitor 346. Since HPA 316 typically includes one or more FET amplifiers, a current amplifier 348 may be included within the control loop 326 for providing the requisite FET amplifier bias current. Power control loop 326 sets the RF output power of HPA 316, as measured by detector/buffer 340, by controlling the gate and drain voltages of HPA 316. In this manner, the non-linearity of HPA 316 can be overcome because the input power to HPA 316, as set by the AGC amplifiers (not shown), may continue to increase as the output requirement increases, but the HPA 316 output power continues to be set by gain control loop 326.

In an exemplary implementation of the amplifier 310 suitable for inclusion within a CDMA transmitter, the gain control loop 326 may also include a switch 352, which is opened for the duration of "blank" frames during which signal power is not provided to the antenna by the amplifier 310. Such blank frames are interposed between active frames of actual data when the overall data transmission rate is less than full-rate. The switch 352 opens the integration loop just prior to commencement of each blank frame, and closes the loop immediately after commencement of the following active frame.

VI. Gain-Offset Parallel Stages

FIG. 10 illustratively represents the transfer characteristic of a parallel stage amplifier of the invention in which the constituent amplifier stages are offset in gain. For convenience, the biasing technique of FIG. 10 will be described with reference to the parallel-stage amplifier shown in FIG. 2. In the biasing approach exemplified by FIG. 10, each of the amplifier stages A1–A4 is realized to be of different gain. Switching between stages occurs in the manner described previously, but the gain offset between stages results in discontinuous variation of the power of the amplified RF output signal. As described previously, the switch logic 56 (FIG. 2) monitors the level of the amplified RF signal at output node 52. Switch logic 52 then instructs the input switch matrix and output network 48 to select the appropriate stage A1–A4 designed for operation at the monitored output signal level.

Referring to FIG. 10, the amplifier stages A1–A4 are each biased to provide linear gain in response to input signals within predefined ranges. In particular, the amplifier stage A1 is biased to produce linear gain over the output signal range $P_{OUT,0}$ to $P_{OUT,1}$ in response to input signals between $P_{IN,0}$ and $P_{IN,1}$. Similarly, the amplifier stages A2, A3, and A4 are biased to provide linear gain over the output signal ranges $P_{OUT,1}$ to $P_{OUT,2}$, $P_{OUT,2}$ to $P_{OUT,3}$, and $P_{OUT,3}$ to $P_{OUT,4}$, respectively. When the amplifier stages are implemented as FET or BJT devices, a bias network (not shown) may be employed to supply the level of bias current to each amplifier stage required for operation over the specified output range.

The gain-offset between stages contemplated by FIG. 10 may be of utility when, for example, it is desired to reduce the dynamic range required of automatic gain control (AGC) circuitry used in conjunction with the parallel stage power amplifier. It may also be of significance that the reduced gain exhibited at low-power levels results in less noise amplification at low input signal levels, where signal to noise ratio is often at a minimum. Accordingly, the gain-offset technique of FIG. 10 may advantageously be employed to improve noise performance at low input signal levels, as well as to improve the overall noise performance of a complete amplifier chain.

The previous description of the preferred embodiments are provided to enable any person skilled in the art to make or use the present invention. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without the use of the inventive faculty. Thus, the present invention is not intended to be limited to the embodiments shown herein, but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

We claim:

1. An amplifier circuit for providing an amplified signal in response to a radio frequency (RF) input signal having successive portions separated by signal boundaries, said amplifier circuit comprising:

a timing information input line receiving timing information representative of the boundaries between the portions of the RF input signal;

a plurality of amplifier stages for amplifying said RF input signal, each of said plurality of amplifier stages having an amplifier stage input for receiving said RF input signal and an amplifier stage output for providing an amplified RF signal, each of said amplifier stages operative to amplify the RF input signal only while a direct current (DC) bias is applied to the respective amplifier stage input thereof;

a control circuit, coupled to each amplifier stage input of said plurality of amplifier stages and to the timing information input line, for selecting particular amplifier stages to be activated and for providing a DC bias to the amplifier input stages of each of the selected amplifier stages, said control circuit operative to vary the selection of particular amplifier stages only during a boundary between portions of the RF input signal; and

means, coupled to each of said amplifier stage inputs, for isolating said DC bias from the amplifier input stages of other ones of said plurality of amplifier stages.

2. The amplifier circuit of claim 1 further comprising an input network, having an input coupled to said input signal and a plurality of outputs, each output coupled to one of said amplifier stage inputs, said input network for providing said input signal to each of said plurality of amplifier stages; and

an output network, coupled to each of said amplifier stage outputs, for providing said amplified signal from a selected at least one of said plurality of amplifier stages at an output network output node.

3. The amplifier circuit of claim 2 wherein said means for isolating comprises a plurality of capacitors, each capacitor having an input coupled to said input signal, and an output coupled to a respective one of said amplifier stage inputs.

4. The amplifier circuit of claim 3 wherein at least one of said plurality of amplifier stages is a field-effect transistor device.

5. The amplifier circuit of claim 3 wherein at least one of said plurality of amplifier stages is a bipolar junction transistor device.

6. A method for providing an amplified signal in response to a radio frequency (RF) input signal having successive portions separated by signal boundaries in an amplifier circuit comprising a plurality of amplifier stages each operative to amplify a signal only while simultaneously receiving a direct current (DC) bias signal, said method comprising the steps of:

receiving timing information representative of the boundaries between the portions of the RF input signal;

applying said input signal to each of said plurality of amplifier stages;

selecting an amplifier stage for use in amplifying the signal;

applying a DC bias signal to the selected amplifier stage, with said DC bias signal being initiated during a boundary between portions of the RF input signal;

isolating said DC bias signal from all but said selected one of said plurality of other amplifier stages;

amplifying said input signal in said selected amplifier stage to generate said amplified signal; and

providing said amplified signal at an output node.

7. The amplifier circuit of claim 1 wherein said portions of the input RF signals are words.

8. The method of claim 6 wherein said portions of the input RF signals are words.

* * * * *

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[54] REVERSE LINK, TRANSMIT POWER CORRECTION AND LIMITATION IN A RADIOTELEPHONE SYSTEM

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[51] Int. Cl.[6] H04B 1/40; H04B 1/04; H04B 1/06

[52] U.S. Cl. 455/88; 455/89; 455/126; 455/127; 455/234.2; 330/129

[58] Field of Search 330/129, 132, 136; 455/73, 74, 67.1, 69, 70, 84, 73, 88, 89, 77, 115, 126, 127, 245.1, 232.1, 234.1, 234.2, 240.1, 246.1, 227, 177.1, 200.1; 375/1, 98

[56] References Cited

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5,056,109	10/1991	Gilhousen	455/69
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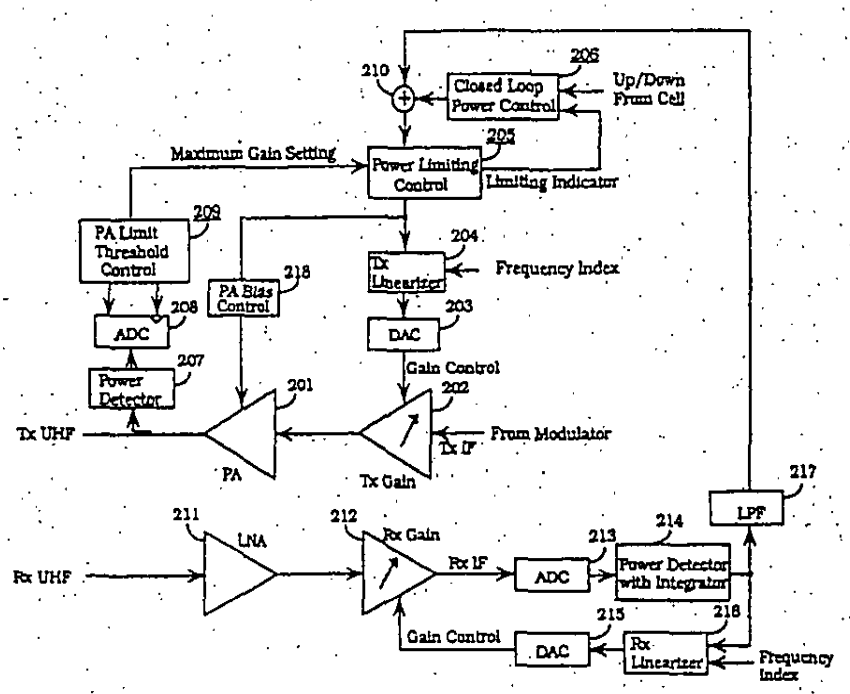
5,267,262	11/1993	Wheatley, III	458/69
5,297,161	3/1994	Ling	455/69

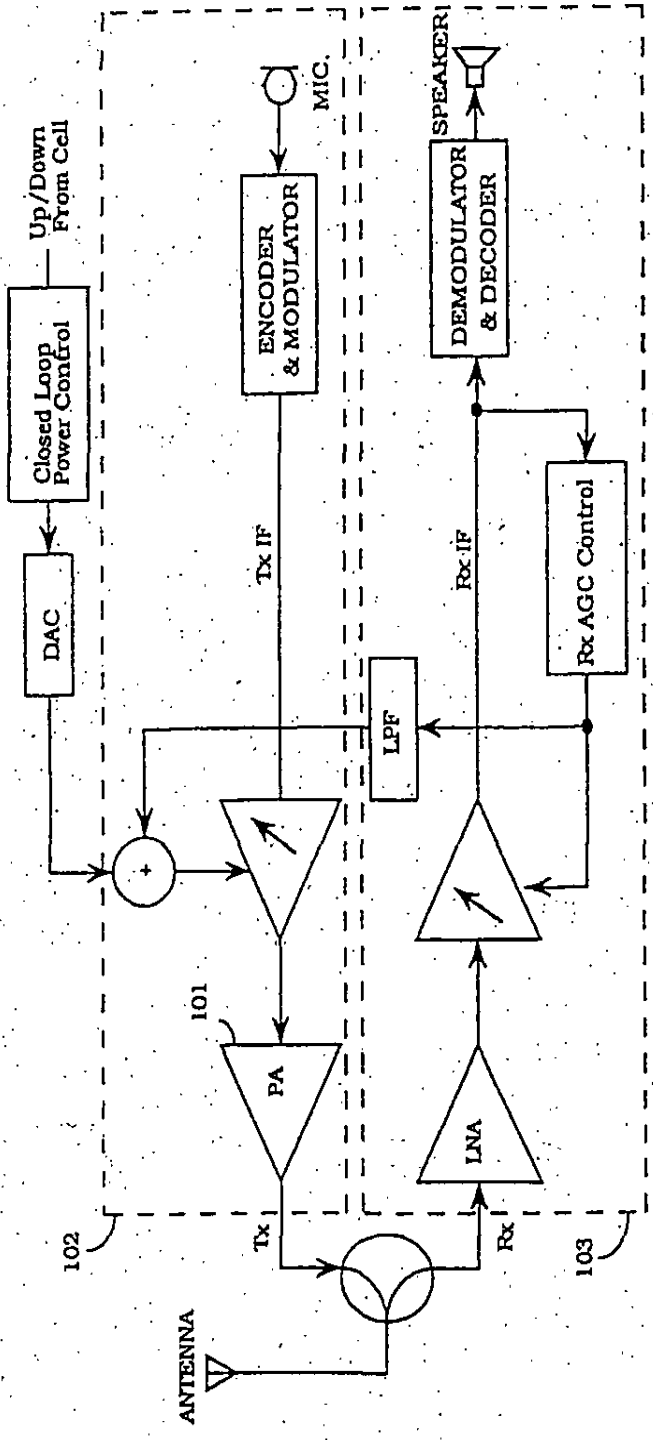
Primary Examiner—Edward F. Urban
Assistant Examiner—Lisa Charouel
Attorney, Agent, or Firm—Kenneth W. Bolvin; Russell B. Miller

[57] ABSTRACT

The process and apparatus of the present invention limits the output power of a radiotelephone, operating in a cellular system in the preferred embodiment. This ensures the transmitted sidebands and synthesizer phase noise remains within a certain specification. This is accomplished by power detection and a correction accumulator that together generate a gain control signal by limiting the gain adjustment to a maximum value, even when the cell site communicating with the radiotelephone is sending power turn-up commands to the radiotelephone. This process includes dynamically correcting the output level of the transmitter due to gain variations in the transmitter stages or gain control elements.

4 Claims, 9 Drawing Sheets





- Prior Art -

FIG. 1

Ex. F-2

Ex. E-2

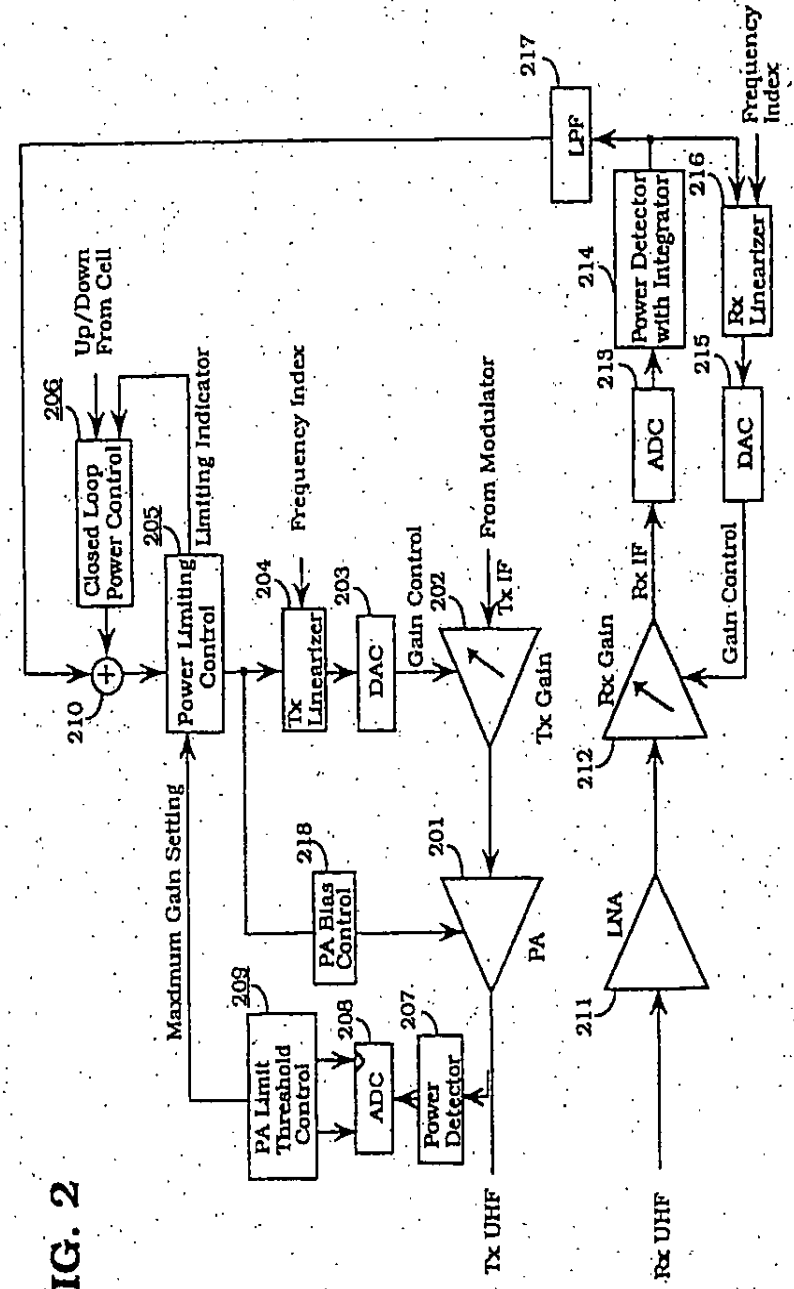
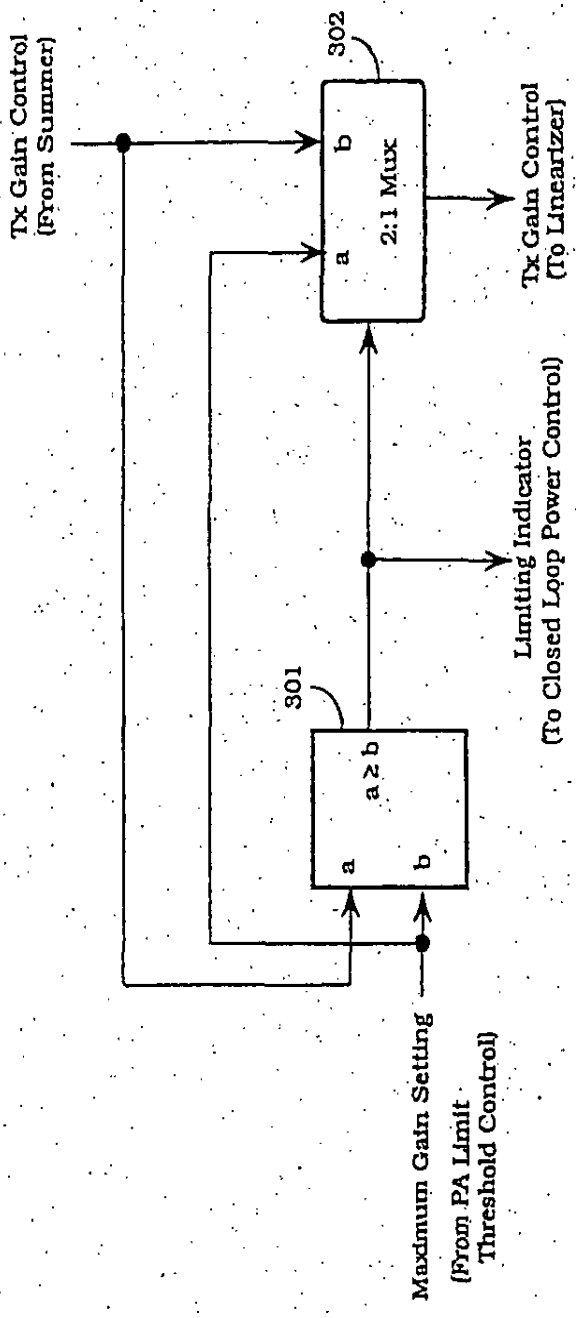


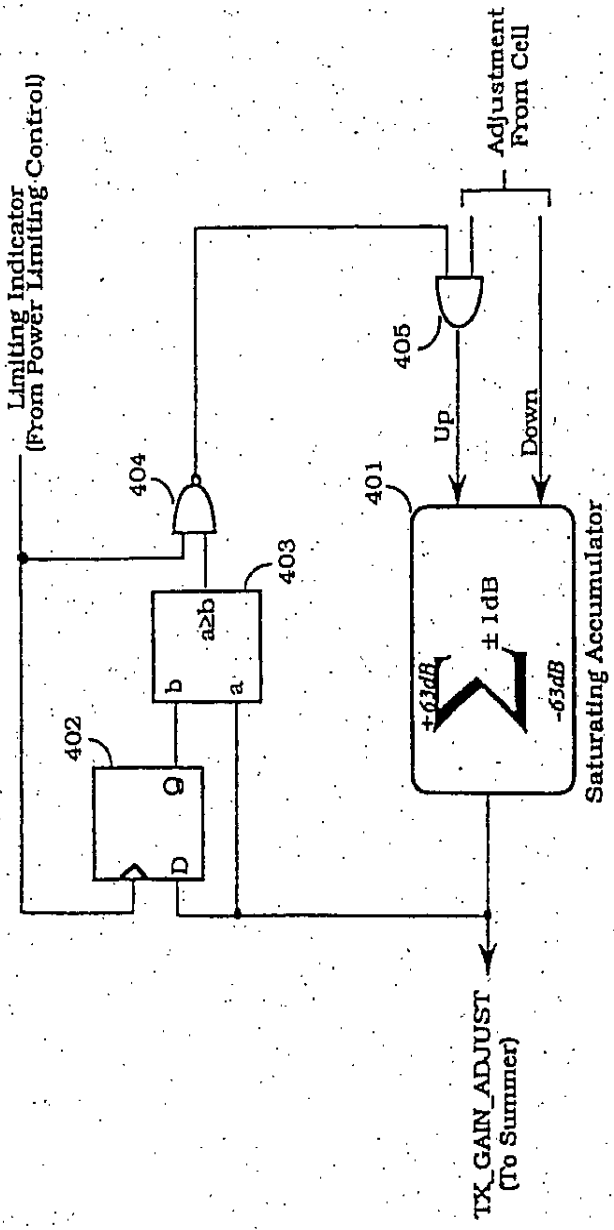
FIG. 2

Ex. F-3 Ex. E-3


Tx Gain Control
(From Summer)
302
b
a
2:1 Mux
Tx Gain Control
(To Linearizer)
Limiting Indicator
(To Closed Loop Power Control)
301
a ≥ b
a
b
Maximum Gain Setting
(From PA Limit
Threshold Control)

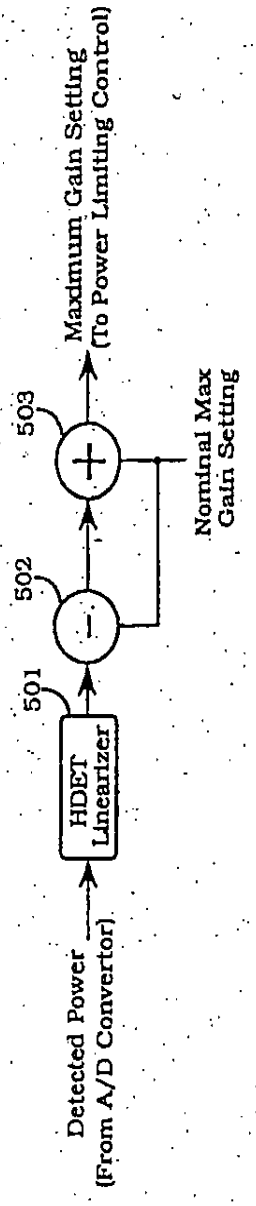
205

FIG. 3


Limiting Indicator
(From Power Limiting Control)
Adjustment
From Cell
405
Up
Down
404
401
403
a≥b
b
a
402
Q
D
±1dB
+63dB
-63dB
Saturating Accumulator
TX_GAIN_ADJUST
(To Summer)

206

FIG. 4


Maximum Gain Setting
(To Power Limiting Control)
503
Nominal Max
Gain Setting
502
501
HDET
Linearizer
Detected Power
(From A/D Convertor)

209

FIG. 5

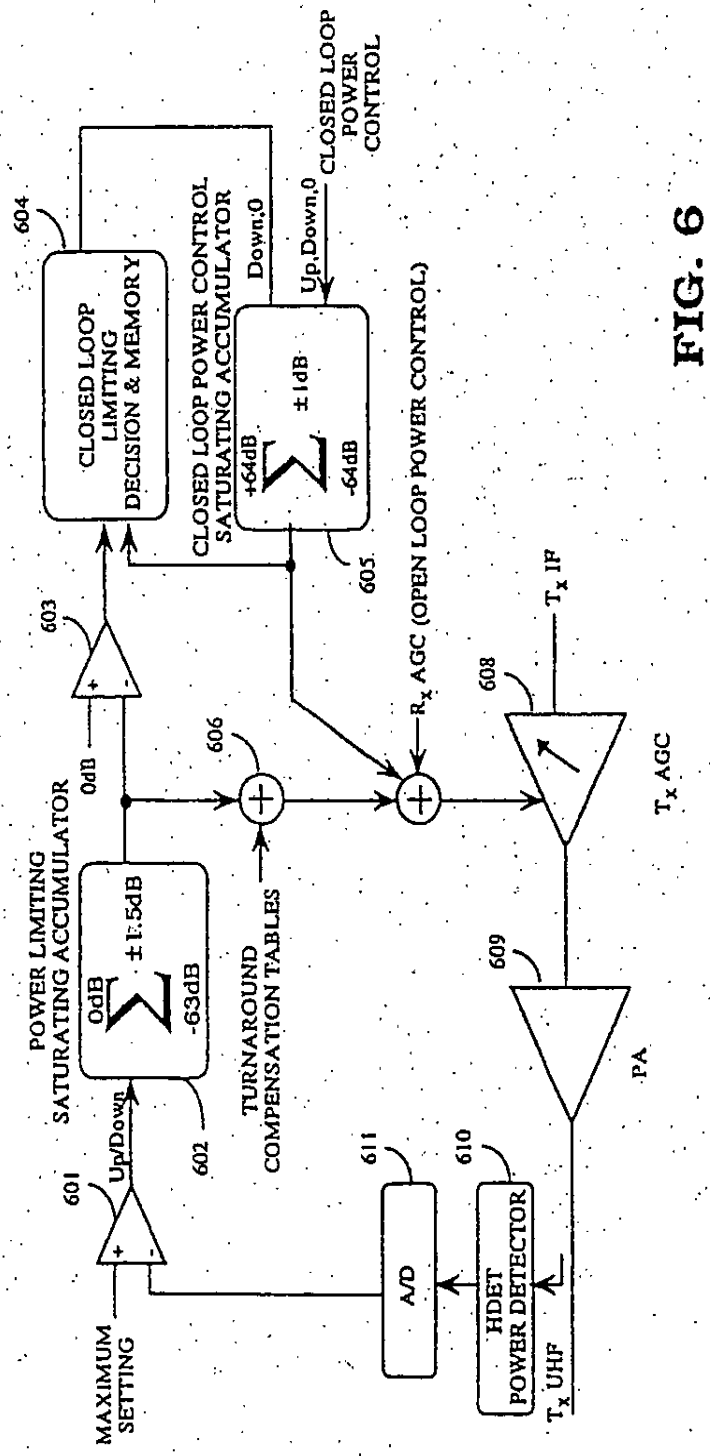

CLOSED LOOP POWER CONTROL
Up,Down,0
CLOSED LOOP POWER CONTROL SATURATING ACCUMULATOR
Down,0
±1dB
+64dB
-64dB
605
CLOSED LOOP LIMITING DECISION & MEMORY
604
603
0dB
606
R_x AGC (OPEN LOOP POWER CONTROL)
T_x IF
608
T_x AGC
POWER LIMITING SATURATING ACCUMULATOR
±1.5dB
0dB
-63dB
602
TURNAROUND COMPENSATION TABLES
609
PA
601
Up/Down
611
610
A/D
HDET POWER DETECTOR
MAXIMUM SETTING
T_x UHF

FIG. 6

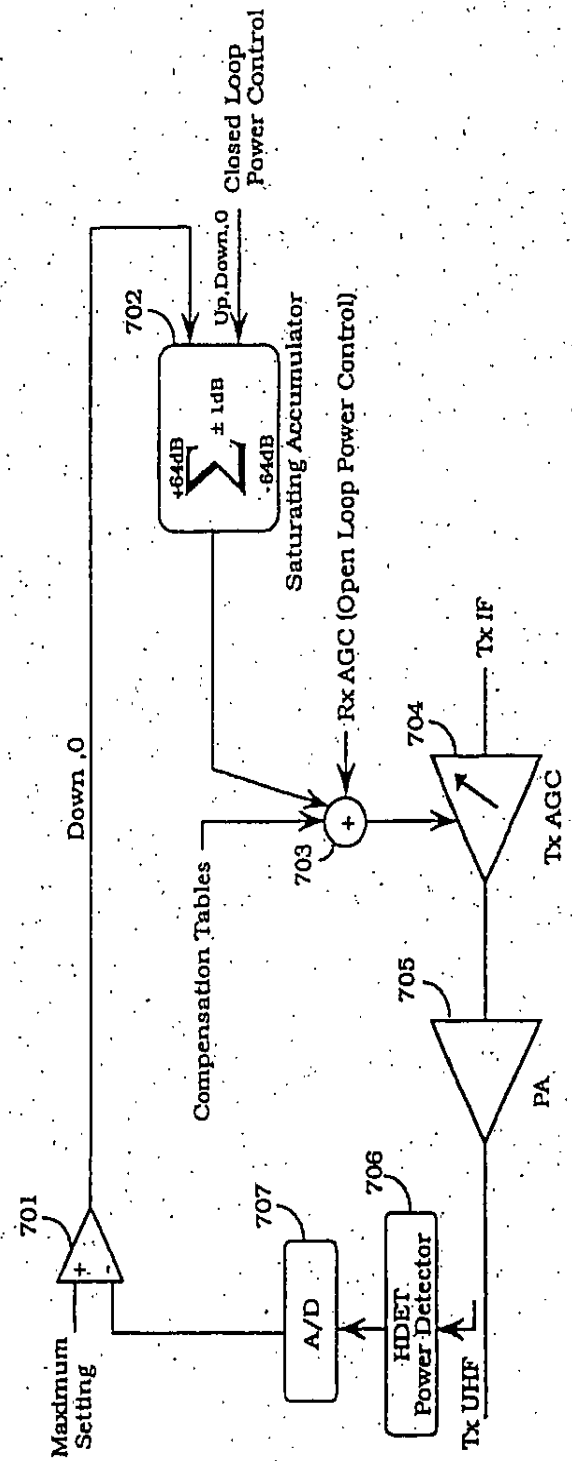

Closed Loop Power Control
Up,Down,0
702
+64dB
± 1dB
-64dB
Saturating Accumulator
Rx AGC (Open Loop Power Control)
Tx IF
704
Tx AGC
Down ,0
703
Compensation Tables
705
PA
701
707
706
A/D
HDET Power Detector
Maximum Setting
Tx UHF

FIG. 7

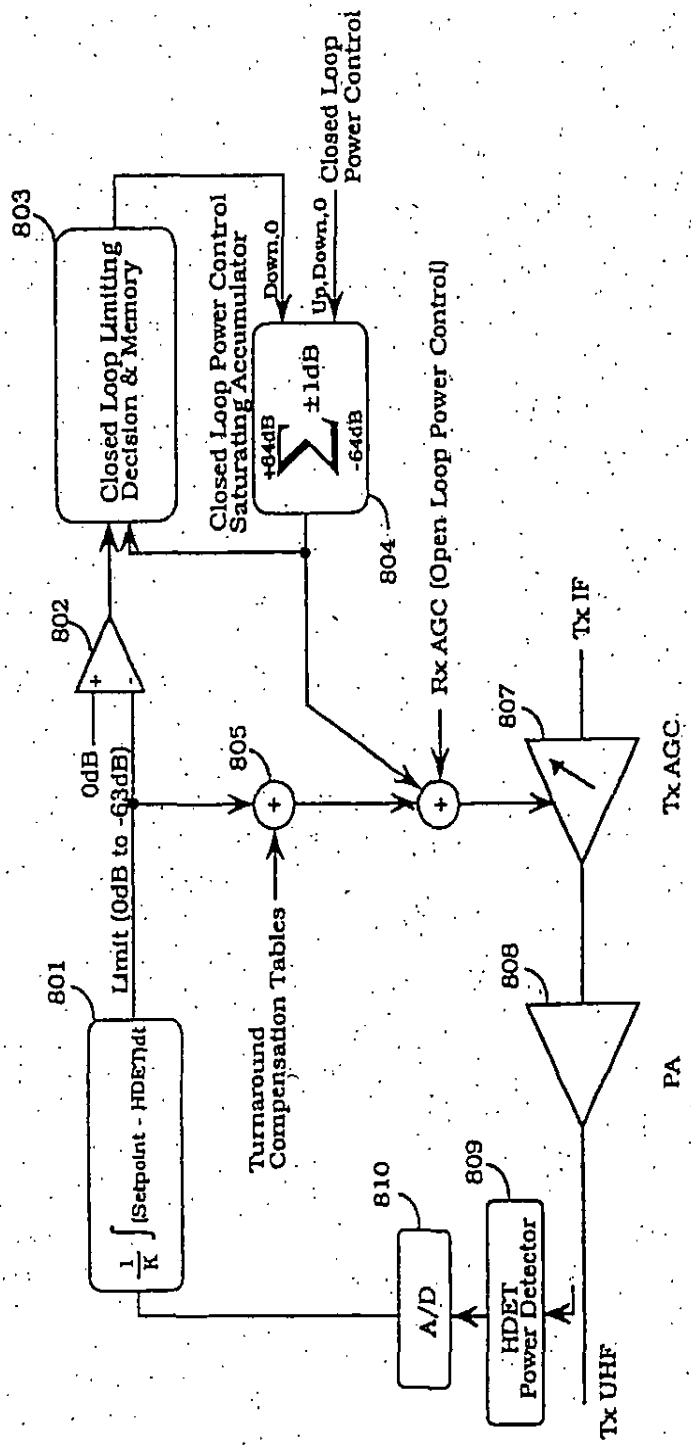

803
Closed Loop Limiting Decision & Memory
Closed Loop Power Control Saturating Accumulator
Down,0
Up,Down,0
Closed Loop Power Control
+84dB
±1dB
-64dB
804
802
0dB
805
Rx AGC (Open Loop Power Control)
Tx IF
807
Tx AGC
Limit (0dB to -63dB)
Turnaround Compensation Tables
801
808
PA
1/K ∫(Setpoint - HDET)dt
810
809
A/D
HDET Power Detector
Tx UHF

FIG. 8

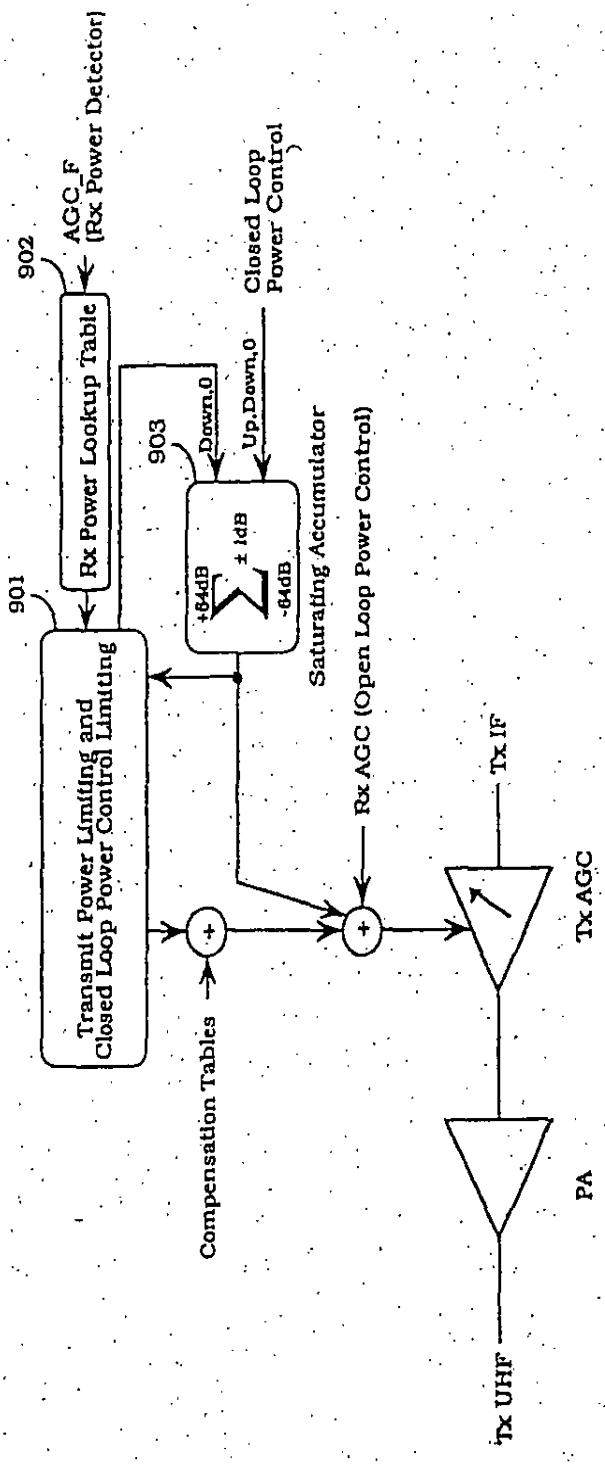

902
AGC_F
(Rx Power Detector)
Rx Power Lookup Table
Closed Loop
Power Control
Up,Down,0
Down,0
903
+64dB
± 1dB
-64dB
Saturating Accumulator
901
Transmit Power Limiting and
Closed Loop Power Control Limiting
Rx AGC (Open Loop Power Control)
Tx IF
Tx AGC
Compensation Tables
PA
Tx UHF

FIG. 9

REVERSE LINK, TRANSMIT POWER CORRECTION AND LIMITATION IN A RADIOTELEPHONE SYSTEM

BACKGROUND OF THE INVENTION

I. Field of the Invention

The present invention relates to radio communications. More particularly, the present invention relates to power control in a radiotelephone system.

II. Description of the Related Art

The Federal Communications Commission (FCC) governs the use of the radio frequency (RF) spectrum. The FCC allocates certain bandwidths within the RF spectrum for specific uses. A user of an allocated bandwidth of the RF spectrum must take measures to ensure that the radiated emissions inside and outside of that bandwidth are maintained within acceptable levels to avoid interfering with other users operating in the same and or other bandwidths. These levels are governed by both the FCC and the particular user groups of said bandwidth.

The 800 MHz cellular telephone system operates its forward link, the cell to radiotelephone transmission, in the bandwidth of 869.01 MHz to 893.97 MHz and the reverse link, the radiotelephone to cell transmission, in the bandwidth of 824.01 MHz to 848.97 MHz. The forward and reverse link bandwidths are split up into channels each of which occupies a 30 kHz bandwidth. A particular user of the cellular system may operate on one or several of these channels at a time. All users of the system must ensure that they are compliant with the level of radiated emissions allowable inside and outside of the channel or channels that they have been assigned.

There are several different techniques of modulation that can be used in the cellular telephone system. Two examples of modulation techniques are frequency division multiple access (FDMA) and code division multiple access (CDMA).

The FDMA modulation technique generates signals that occupy one channel at a time while the CDMA modulation technique generates signals that occupy several channels. Both of these techniques must control their return link radiated emissions to within acceptable limits inside and outside of the assigned channel or channels. For maximum system performance, users of the CDMA technique must carefully control the level of radiated power inside the channels in which they are operating.

FIG. 1 shows a typical prior cellular radiotelephone. In both an FDMA and a CDMA based radiotelephone, there exists the possibility of driving the power amplifier (101) in the transmitter beyond a point where acceptable out of channel radiated emissions are maintained. This is primarily due to the increased distortion output levels of the power amplifier (101) at high output powers. Also, driving the power amplifier (101) beyond a certain point can cause interference internal to the radio. For example, PA puncturing in CDMA affects synthesizer phase noise due to large current transitions. Both of these issues cause unacceptable radio performance.

Maintaining the proper on-channel output power can be difficult due to several undesirable effects in the radiotelephone hardware. For example, the CDMA based radio must implement a power control system that operates over a very wide dynamic range, 80 dB to 90 dB, such that the transmitted output power is linearly related to the received input power.

Closed loop and open loop power control together determine the return link transmit energy, as disclosed in U.S. Pat. No. 5,056,109 to Gilhousen et al. and assigned to Qualcomm, Incorporated. Therefore, the linear and nonlinear errors produced in both the receiver (103) and transmitter (102) RF sections can cause unacceptable power control performance. Also, both the FDMA and CDMA based radios must operate on different channels while maintaining acceptable output power levels. Variation in output power level and input power detection versus frequency can cause an unacceptable amount of error in the amount of return link transmitted energy.

These issues present significant problems to the designer of both FDMA and CDMA based radiotelephones. There is a resulting need for an effective, cost efficient means of correcting these problems.

SUMMARY OF THE INVENTION

The process of the present invention enables a radiotelephone to operate in a linear fashion over a wide dynamic range while maintaining acceptable transmit output power levels inside and outside of the return link bandwidth. The forward and return link power are measured by power detectors and input to an analog to digital converter accessible by both control hardware and/or software. The closed loop power control setting is also monitored. The radiotelephone uses the detected power levels and closed loop power control setting to index a set of correction tables that indicate the reverse link transmit power error and desired power amplifier biasing for the particular operating point. The radiotelephone also determines if the transmitter is operating above a maximum set point. The transmit gain and power amplifier biasing of the radiotelephone are adjusted to correct the undesired error and maintain the desired output power.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a block diagram of a typical prior art radiotelephone frequency section for use in a radiotelephone system.

FIG. 2 shows a block diagram of the preferred embodiment power control correction implementation.

FIG. 3 shows a block diagram of the power limiting control section as related to FIG. 2.

FIG. 4 shows a block diagram of the closed loop power control section as related to FIG. 2.

FIG. 5 shows a block diagram of the PA limit threshold control section as related to FIG. 2.

FIG. 6 shows an alternate embodiment of the present invention that employs a power limiting control system based on accumulator feedback control.

FIG. 7 shows an alternate embodiment of the present invention that employs a power limiting control system based on the closed loop power control accumulator.

FIG. 8 shows an alternate embodiment of the present invention that employs a power limiting control system based on integral feedback control.

FIG. 9 shows an alternate embodiment of the present invention that employs a power limiting control system based on a measure of receive power and the closed loop power control setting to estimate output power.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The process of the present invention provides power control correction for a mobile radiotelephone as well as maintaining acceptable in and out of band maximum emission levels. This is accomplished by real-time compensation utilizing a set of correction tables that are generated during the production testing of each radiotelephone.

FIG. 2 shows a block diagram of a CDMA radiotelephone with the preferred embodiment power control correction implementation. FIGS. 3, 4, and 5 detail specific blocks of FIG. 2. The radiotelephone is comprised of a receive linearization section, transmit linearization section, power amplifier bias control section, and power limiting control section.

The receive linearization section includes an automatic gain control (AGC) section. The signal input to the AGC section is received on the forward link and amplified by a low noise amplifier (LNA) (211). The output of the LNA (211) is input to a variable gain amplifier (212). The variable gain amplifier (212) produces a signal that is converted to a digital signal using an analog to digital converter (ADC) (213).

The power of the digitized received signal is next computed by a digital power detector (214). The power detector (214) includes an integrator that integrates the detected power with respect to a reference voltage. In the preferred embodiment, this reference voltage is provided by the radio's demodulator to indicate the nominal value at which the demodulator requires the loop to lock in order to hold the power level constant. The demodulator requires this value for optimum performance since a power level too far out of the optimum range will degrade the performance of the demodulator. The power detector (214) performs the integration, thus generating an AGC setpoint. The setpoint and a receive frequency index are input to a receiver linearizing table (216).

The AGC setpoint and the frequency index are used to address the linearizer (216), thus accessing the proper calibration value. This calibration value is then output to a digital to analog converter (215) that generates the analog representation of the receive AGC setting.

The analog value adjusts the biasing of the variable gain amplifier (212). The control of the variable gain amplifier (212) forces the receive AGC loop to close such that the input to the receiver linearizing table (216) follows a predetermined straight line with respect to RF input power. This linearization removes the undesired linear and non-linear errors in addition to variations versus frequency that would otherwise be apparent at the input to the receiver linearizing table (216) in the receiver. These errors and variations would contribute to errors in the transmitter.

In order to reduce the error in the receive and transmit chains versus frequency, the receive and transmit linearizers utilize the frequency index that specifies the current center frequency on which the receive and transmit chains are operating. During factory calibration of the radiotelephone, the linearizers are loaded with values, in addition to the previously mentioned calibration values, that are indexed by frequency to correct the errors related to operating center frequency.

The AGC setpoint is the open loop power control signal for the radio. In the preferred embodiment, this is the power control performed by the radio by itself without control input from the cells. As the power of the signal received from the cell increases, the radio decreases its transmit power. This output power control is accomplished by the AGC setpoint that is filtered by a low pass filter (217).

The transmit section includes a digital summer (210) that combines the AGC setpoint and a closed loop power control setting (206). The output of the summer (210) is fed into a power control limiting section (205). The operation of the power control limiting section (205) and the closed loop power control section (206), illustrated in FIGS. 3 and 4 respectively, will be discussed subsequently in greater detail.

The output of the power control limiting section (205), along with the transmit frequency index, are used to address values stored in a transmitter linearizing table (204). The transmitter linearizing table (204) contains values determined from production testing of the radiotelephone. The selected value is input to a digital to analog converter (203) whose output, an analog representation of the digital value input, controls a variable gain amplifier (202).

The biasing of the variable gain amplifier (202) is adjusted by the analog calibration value to a point such that the input to the transmitter linearizing table (204) follows a predetermined straight line with respect to transmitted RF output power. This linearization removes the undesired linear and non-linear errors along with variations versus frequency in the transmitter. This, combined with the previously mentioned receive linearization, greatly reduces the open and closed loop power control errors due to RF performance imperfections.

The power amplifier (PA) bias control section (218) controls the bias point of the transmit PA (201) based on the transmit gain setting such that the transmit sidebands for the given gain setting are optimized versus PA (201) current consumption. This allows a battery powered telephone to maximize talk time by reducing PA (201) current consumption at lower output powers while still maintaining acceptable sideband levels at higher output power levels.

The power control limiting section (205) is illustrated in FIG. 3. The power control limiting section (205) controls the closed loop power control and transmit gain settings when the output of the transmit gain summer (210) corresponds to a transmit output power level which is equal to or greater than the intended maximum output power. The maximum gain setting is determined by the PA limit threshold control section (209).

The threshold control section (209) determines the maximum gain setting based on a nominal value that is modified by a real-time measurement of the transmitted output power. The measurement is accomplished by an analog power detector (207) whose output transformed into a digital signal by an analog to digital converter (208). The digitized power value is then input to the threshold control section (209).

The threshold control section, detailed in FIG. 5, operates by the high power detector (HDET) linearizer (501) scaling the input digitized power value in order to match the numerology of the digital transmit gain control section. The scaled output from the linearizer (501) is subtracted (502) from the nominal maximum gain setting. This maximum gain setting can be hard coded into the radio during assembly or input during manufacturing and testing of the radio.

Ex. F-12

Ex. E-12

The difference of the maximum gain setting and the scaled output power is then added, by the adder (503), to the maximum gain setting. The sum of these signals is then used as the corrected maximum gain setting. This real-time modification of the detected power helps mitigate the errors introduced by temperature variations and aging of the transmitter PAs. In other words, if the difference between the maximum gain setting and the real-time measured power value is 0, then no correction is necessary. If there is a difference between the two, the difference is used to correct the maximum gain setting.

Referring to FIG. 3, a digital comparator (301) detects when the output of the transmit gain summer (210) equals or exceeds the maximum gain setting. The comparator (301) controls a 2:1 multiplexer (302) that outputs the maximum allowable setting when the output of the summer (210) exceeds the maximum allowable setting. When the output of the summer (210) is less than the maximum allowable setting, the multiplexer (302) outputs the direct output of the summer (210). This prohibits the transmitter from exceeding its maximum operating point.

The closed loop power control section (206), illustrated in FIG. 4, accumulates the power control commands sent on the forward link by the controlling radiotelephone cell site and outputs a gain adjust signal. The power control commands are collected in an accumulator (401). The operation of the accumulator (401) is controlled by the power control limiting section (205) when the transmit power amplifier (201) is outputting the maximum allowable power.

When the output of the summer (210) changes from being less than to equal or greater than the maximum allowable setting, the output of the closed loop power control accumulator (401) is latched into a flip-flop (402). While the output of the summer (210) is equal to or greater than the maximum allowable setting, as determined by the comparator (403) and NAND gate (404) circuit, an AND gate (405) masks off any closed loop power control up commands that would force the accumulator (401) above the flip-flop's (402) latched value. This prevents the accumulator from saturating during power limiting yet allows the closed loop power control setting to change anywhere below the latched value.

An alternate embodiment of the process of the present invention is illustrated in FIG. 6. In this embodiment, a power limiting control system is employed based on accumulator feedback control. The system operates by first measuring the output power of the power amplifier (609) using a power detector (610). The detected power is then digitized by an ADC (611) and compared to a maximum allowable setting by the comparator (601). If the output power is greater than the maximum setting, the power limiting accumulator (602) begins turning power down by reducing the gain of the variable gain amplifier (608). If the output power is less than the maximum setting the power limiting accumulator (602) returns to a 0 dB correction value.

In this embodiment, a closed loop power control limiting function (604 and 605), similar to the preferred embodiment, is employed. However, the trigger for the closed loop power control limiting function is a comparator (603) that detects when the power limiting accumulator (602) is limiting the output power by comparing the accumulator (602) output to 0 dB with the comparator (603). The linearizing compensation tables, similar to the tables in the preferred embodiment, are added into the transmit gain control using a summer (606).

In another alternate embodiment, illustrated in FIG. 7, a power limiting control system is employed that is based on the closed loop power control accumulator (702). The system operates by first measuring the output power of the power amplifier (705) using a power detector (706). The detected power is digitized (707) and compared to a maximum allowable setting by the comparator (703). If the output power is greater than the maximum setting, the closed loop power control accumulator (702) is modified to turn the amplifier (704) power down by one step each 1.25 ms until the output power is less than the maximum setting. If the output power is less than the maximum setting, the closed loop power control accumulator is not modified. The linearizing compensation tables, similar to the preferred embodiment, are added into the transmit gain control using a summer (703).

In yet another embodiment, illustrated in FIG. 8, a power limiting control system is employed that is based on integral feedback control. The system operates by first measuring the output power of the power amplifier (808) using a power detector (809). The detected power is digitized (810) and input to an integrator (801) that follows the equation:

$$\frac{1}{K}\cdot\int(\text{Setpoint}-\text{Detected})dt$$

The integrator (801), generating a gain control signal, saturates at 0 dB and −63 dB of correction. The gain control signal is thus limited within a range. If the output power is greater than the setpoint, the integrator turns down the output power of the amplifier (807) at a rate based on the integration constant K until the setpoint is reached. The integrator is allowed to turn power down by as much as 63 dB. If the output power is less than the setpoint, the output of the integrator (801) will be forced to zero, thus not adjusting output power.

In this embodiment, a closed loop power control limiting function (803 and 804), similar to the preferred embodiment, is employed. The trigger for the closed loop power control limiting function, however, is a comparator (802) that detects when the power limiting integrator (801) is limiting the output power. The linearizing compensation tables, similar to the preferred embodiment, are added into the transmit gain control using a summer (805).

In still another embodiment, illustrated in FIG. 9, a power limiting control system is employed that is based only on a measure of receive power, as determined by the Rx power lookup table (902), and the closed loop power control setting as opposed to actual output power. The transmit power limiting and closed loop power control limiting function (901) can be implemented with either the preferred embodiment using the saturating accumulator (903) or one of the alternate embodiments. However, only the receive power and closed loop power control setting are used to estimate transmit output power.

In summary, the process of the present invention ensures that the transmitted sidebands and synthesizer phase noise of a radio transmitter remains within a predetermined specification by limiting the maximum output power. This power limitation is accomplished by a

control loop including a calibration look-up table. Therefore, a radiotelephone using the process of the present invention would not exceed it's nominal maximum power level due to the cell issuing too many power turn-up commands. The radiotelephone limits the power output even when the cell erroneously decides the radiotelephone power should be increased.

We claim:

1. A method for correcting transmit power of a radio device having a plurality of predetermined calibration values and a reference voltage signal, the radio device transmitting and receiving on a plurality of frequencies, each frequency having a frequency index, the method comprising the steps of:

receiving a first signal having a first gain, a first frequency of the plurality of frequencies, and the first frequency having a first frequency index;

determining a receive power value of the first signal;

generating an automatic gain control setpoint in response to the receive power value and the reference voltage signal;

selecting a first predetermined calibration value in response to the automatic gain control setpoint and the first frequency index;

adjusting the first gain in response to the first calibration value;

transmitting a second signal having a second gain and a second frequency of the plurality of frequencies, the second frequency having a second frequency index;

determining a transmit power value of the second signal;

generating a second calibration value in response to the automatic gain control setpoint, the second frequency index, and the transmit power value; and

adjusting the second gain in response to the second calibration value.

2. The method of claim 1 and further including the steps of digitizing the receive power value before generating the automatic gain control setpoint and converting the first predetermined calibration value to an analog value before adjusting the first gain.

3. A radio performing transmit power calibration, the radio transmitting and receiving signals having a plurality of frequencies, each frequency having a frequency index, the radio transmitting signals through a variable gain, transmit amplifier having a control input and receiving signals through a variable gain, receive amplifier having a control input, the radio comprising:

a power detector, coupled to the receive amplifier, for generating a first power value from a received signal having a first frequency;

an integrator, coupled to the power detector, for generating an automatic gain control setpoint from the first power value;

a receive linearizer, coupled to the integrator and the receive amplifier, for generating a receive calibration value in response to the automatic gain control setpoint and a first frequency index corresponding to the first frequency, the receive calibration value being coupled to the receive amplifier control input for adjusting the gain of the receive amplifier;

a second power detector, coupled to the transmit amplifier, for generating a second power value from a transmitted signal having a second frequency; and

a transmit linearizer for generating a transmit calibration value in response to the automatic gain control setpoint, the second power value, and a frequency index corresponding to the second frequency, the transmit calibration value being coupled to the control input of the transmit amplifier for adjusting the gain of the transmit amplifier.

4. A radio performing transmit power calibration, the radio transmitting and receiving signals having a plurality of frequencies, each frequency having a frequency index, the radio transmitting a signal, having a first frequency, through a variable gain transmit amplifier having a control input and receiving a signal, having a second frequency, through a variable gain receive amplifier having a control input, the radio comprising:

a first analog to digital converter, coupled to the receive amplifier, for generating a digital signal from the received signal;

a power detector, coupled to the first analog to digital converter, for generating a power value from the digital signal;

an integrator, coupled to the power detector, for generating an automatic gain control setpoint from the power value;

a receive linearizer, coupled to the integrator, for generating a receive calibration value in response to the automatic gain control set point and a first frequency index corresponding to the second frequency;

a first digital to analog converter, coupled to the receive linearizer, for generating an analog receive calibration value from the receive calibration value, the analog calibration value coupled to the receive amplifier control input for varying the gain of the receive amplifier;

a second power detector, coupled to the transmit amplifier, for generating an analog power value from the transmitted signal;

a second analog to digital converter, coupled to the second power detector, for generating a digital power value from the analog power value;

a transmit linearizer, coupled to the integrator, for generating a transmit calibration value in response to the automatic gain control setpoint, the digital power value, and a second frequency index corresponding to the first frequency; and

a second digital to analog converter, coupled to the second control input, for generating an analog transmit calibration value from the transmit calibration value, the analog transmit calibration value adjusting the gain of the transmit amplifier.

* * * * *

US005590408A

United States Patent [19]

Welland et al.

[11] Patent Number: 5,590,408

[45] Date of Patent: Dec. 31, 1996

[54] REVERSE LINK, TRANSMIT POWER CORRECTION AND LIMITATION IN A RADIOTELEPHONE SYSTEM

[75] Inventors: Ana L. Welland, Encinitas; Richard K. Kornfeld; John E. Maloney, both of San Diego, all of Calif.

[73] Assignee: QUALCOMM Incorporated, San Diego, Calif.

[21] Appl. No.: 407,543

[22] Filed: Mar. 20, 1995

Related U.S. Application Data

[62] Division of Ser. No. 203,151, Feb. 28, 1994, Pat. No. 5,452,473.

[51] Int. Cl.[6] H04B 1/04

[52] U.S. Cl. 455/69; 455/115; 455/116; 455/126

[58] Field of Search 455/33.1, 69, 126, 455/127, 115, 117, 116; 330/129, 132, 136; 375/200, 205, 296, 297; 370/95.3

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4,939,786	7/1990	MaCallum et al.	455/117
5,056,109	10/1991	Gilhousen	455/69
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"CDMA Network Engineering Handbook", Nov. 23, 1993, pp. 8-1 -8-8.

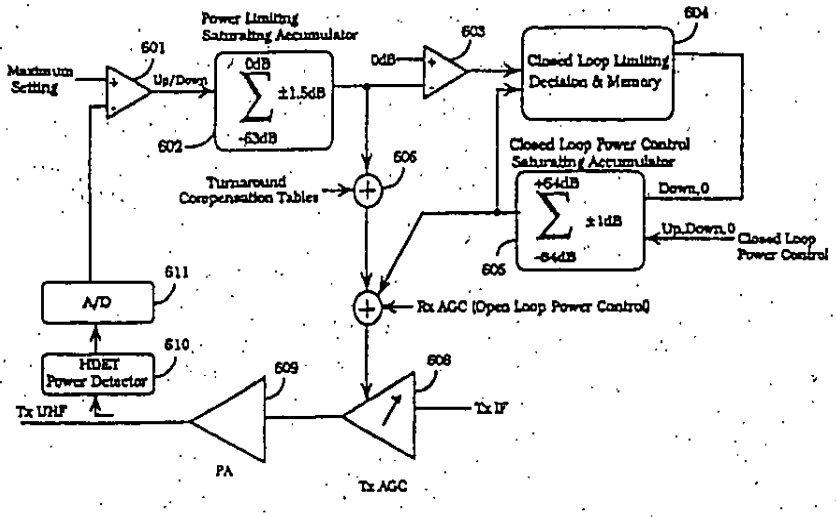
Primary Examiner—Andrew Faile

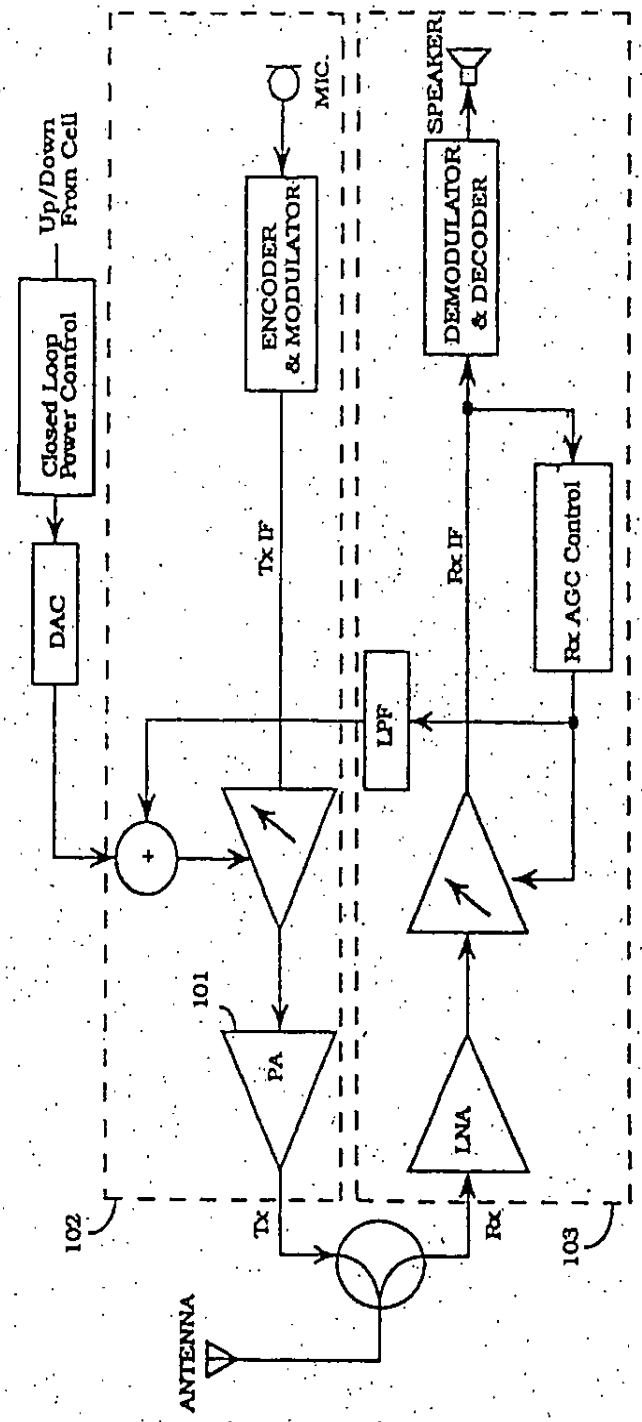
Attorney, Agent, or Firm—Russell B. Miller; Roger W. Martin

[57] ABSTRACT

The process and apparatus of the present invention limits the output power of a radiotelephone, operating in a cellular system in the preferred embodiment. This ensures the transmitted sidebands and synthesizer phase noise remains within a certain specification. This is accomplished by power detection and a correction accumulator that together generate a gain control signal by limiting the gain adjustment to a maximum value, even when the cell site communicating with the radiotelephone is sending power turn-up commands to the radiotelephone. This process includes dynamically correcting the output level of the transmitter due to gain variations in the transmitter stages or gain control elements.

7 Claims, 9 Drawing Sheets





- Prior Art -

FIG. 1

Ex. G-2

Ex. F-2

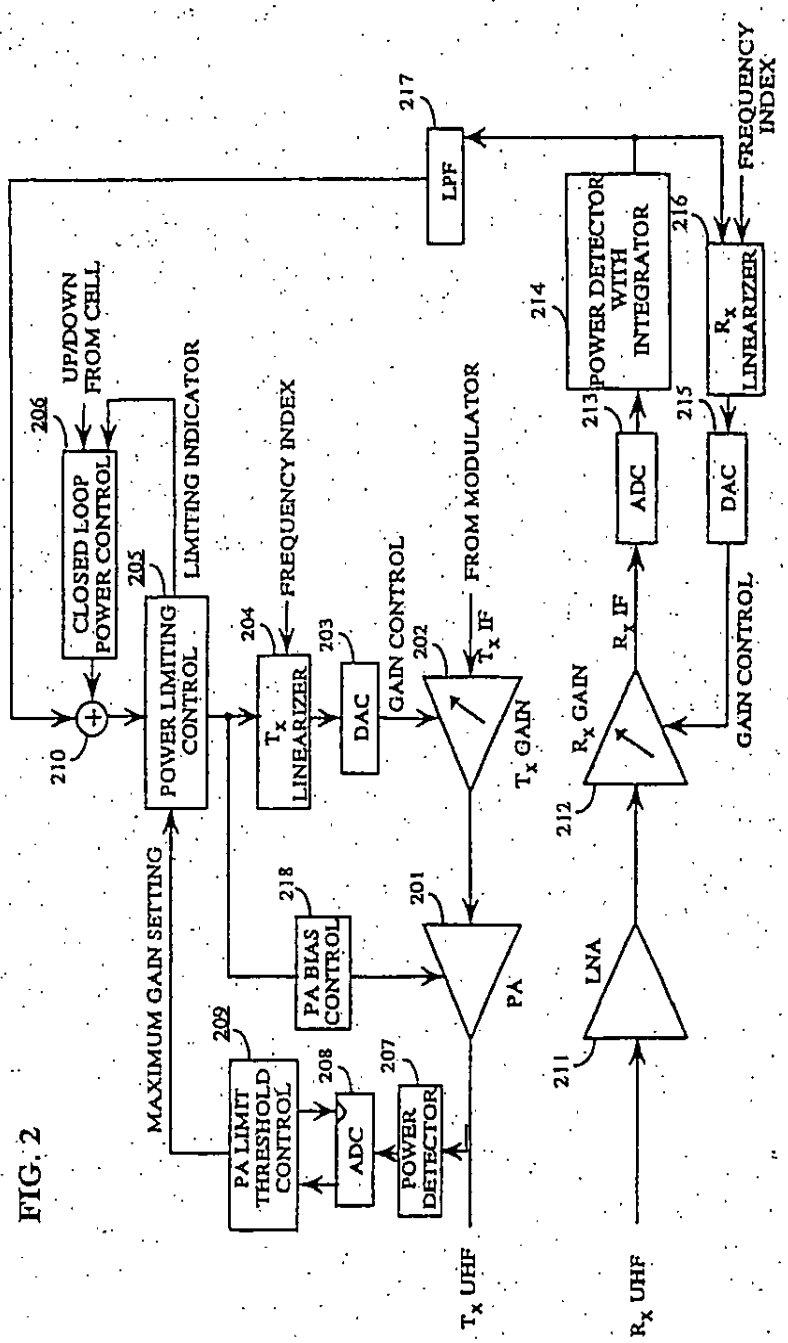
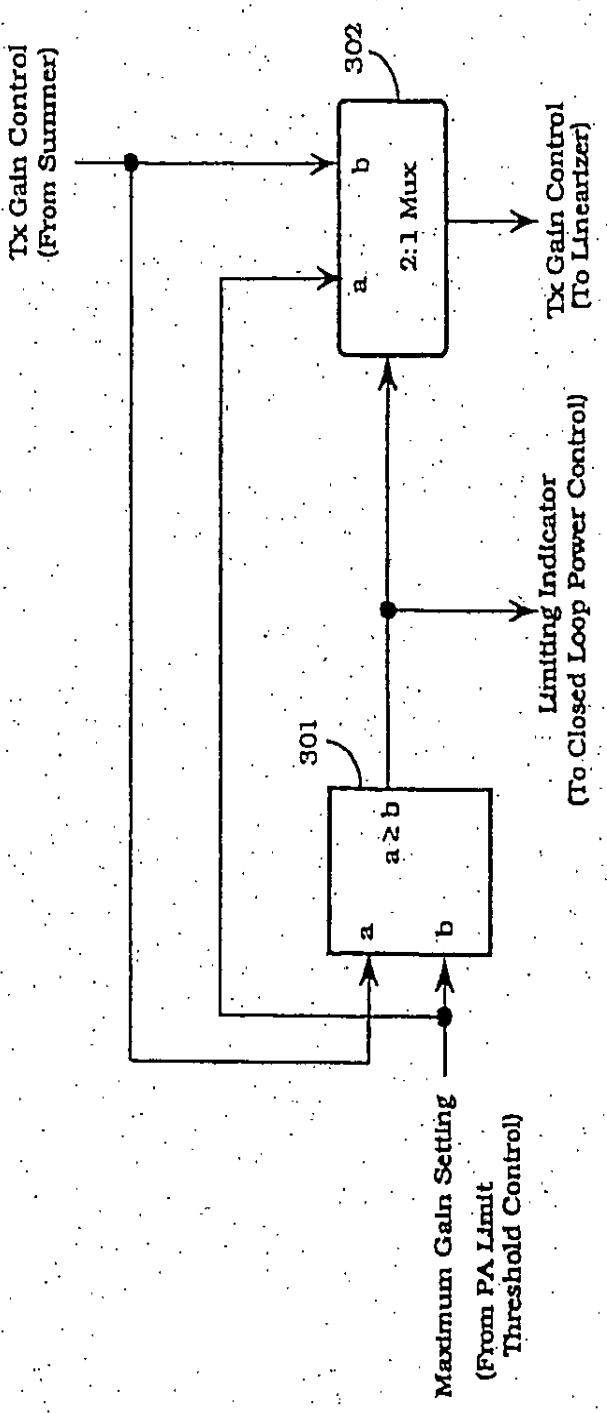


FIG. 2

Ex. G-3

Ex. F-3


Tx Gain Control
(From Summer)
302
b
a
2:1 Mux
Tx Gain Control
(To Linearizer)
Limiting Indicator
(To Closed Loop Power Control)
301
a ≥ b
a
b
Maximum Gain Setting
(From PA Limit
Threshold Control)

205

FIG. 3

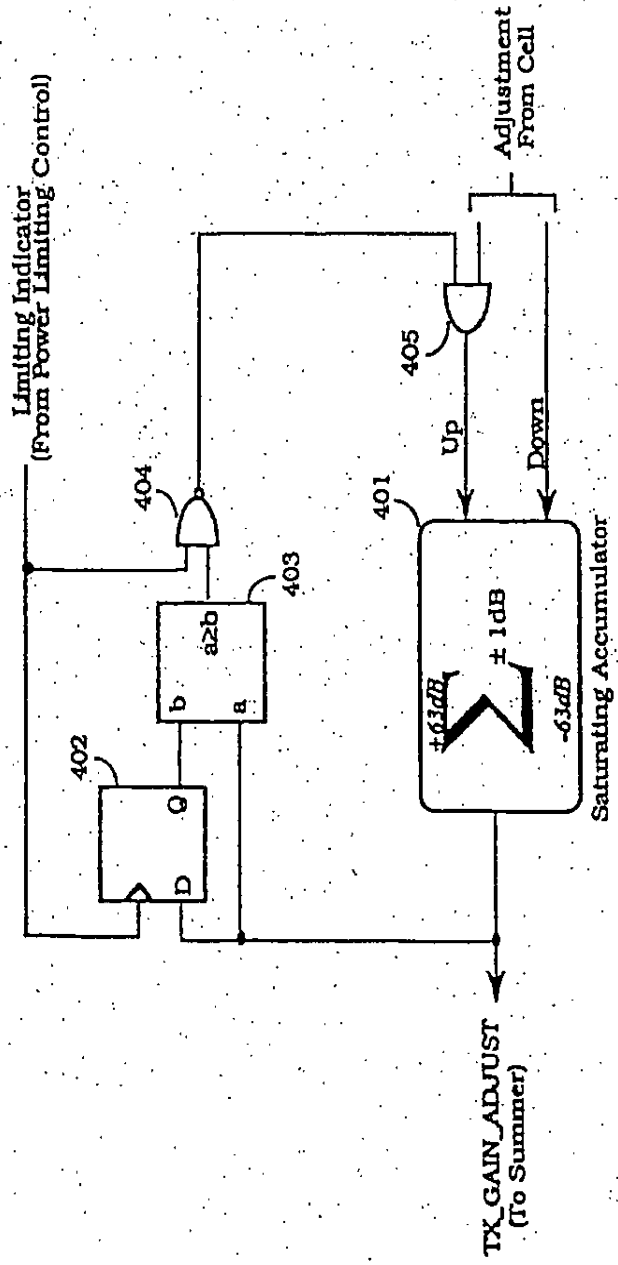
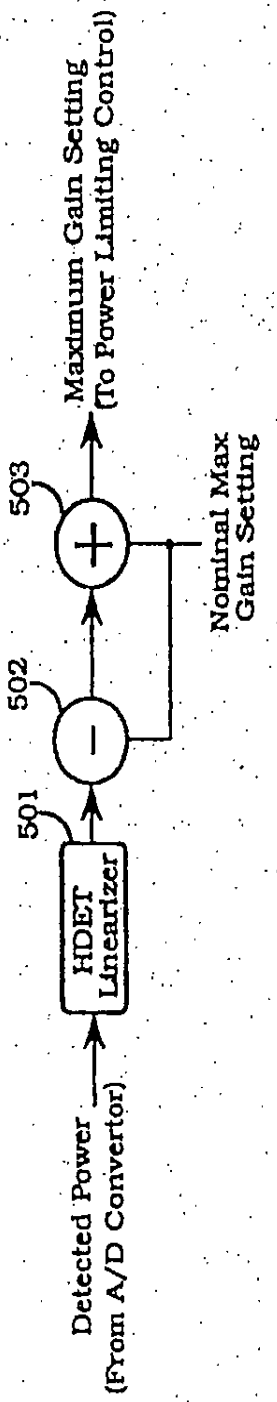

Limiting Indicator
(From Power Limiting Control)
Adjustment
From Cell
405
Up
Down
404
401
403
a≥b
b
a
± 1dB
+63dB
-63dB
Saturating Accumulator
402
Q
D
206
TX_GAIN_ADJUST
(To Summer)

FIG. 4


Maximum Gain Setting
(To Power Limiting Control)
503
Nominal Max
Gain Setting
502
501
HDET
Linearizer
Detected Power
(From A/D Convertor)

209

FIG. 5

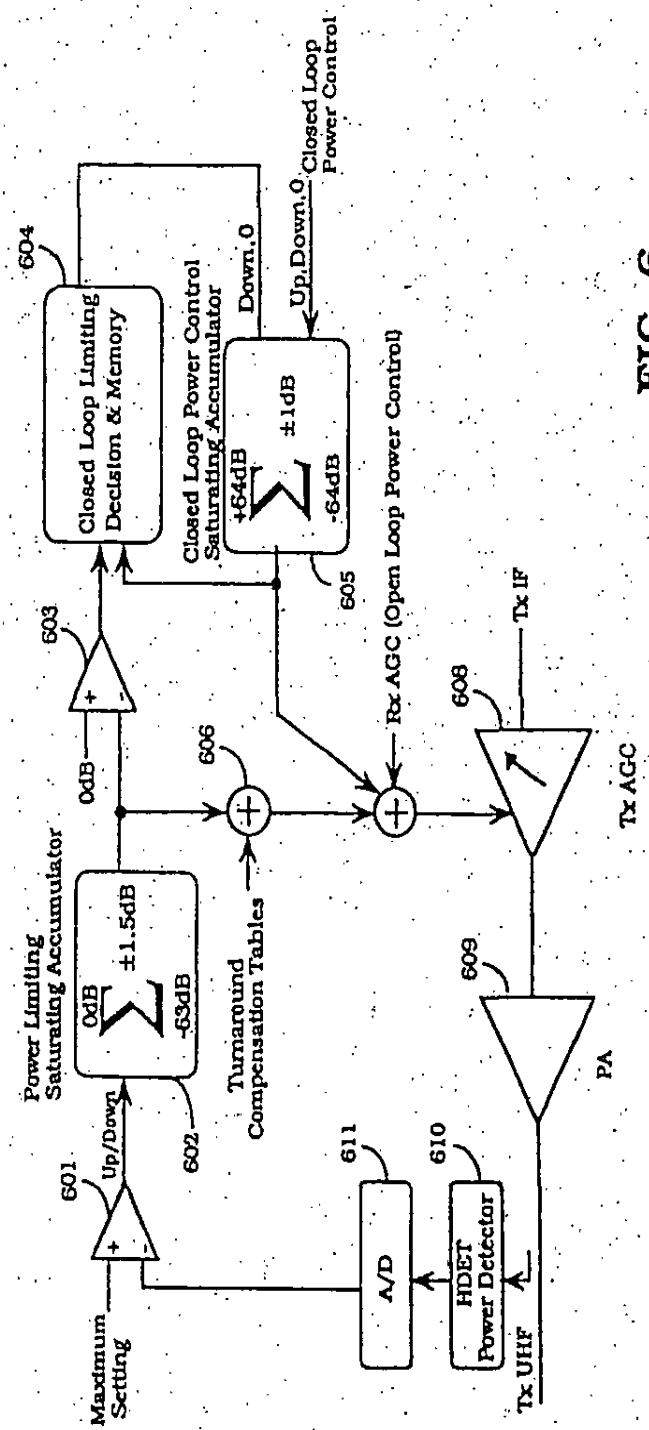

Closed Loop Power Control
Up,Down,0
Down,0
604
Closed Loop Limiting Decision & Memory
Closed Loop Power Control Saturating Accumulator
+64dB
±1dB
-64dB
605
603
0dB
606
Rx AGC (Open Loop Power Control)
Tx IF
608
Tx AGC
Power Limiting Saturating Accumulator
0dB
±1.5dB
-63dB
602
Turnaround Compensation Tables
609
PA
601
Up/Down
611
610
A/D
HDET Power Detector
Maximum Setting
Tx UHF

FIG. 6

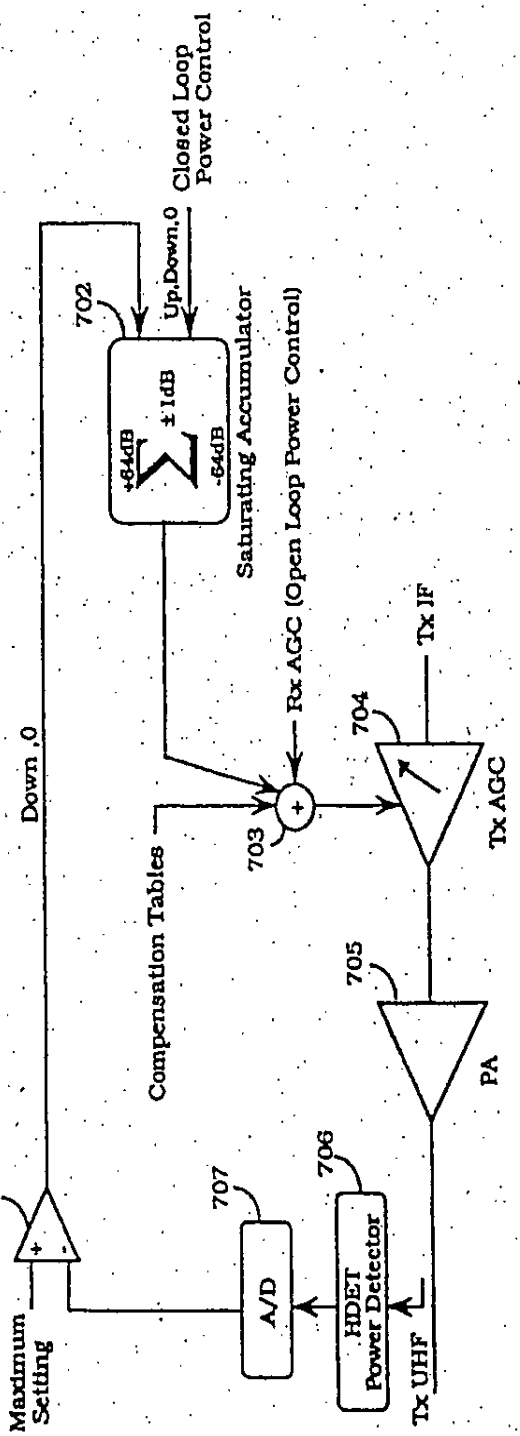

Closed Loop Power Control
Up/Down 0
702
+64dB
±1dB
-64dB
Saturating Accumulator
Rx AGC (Open Loop Power Control)
Tx IF
704
Down 0
703
Tx AGC
Compensation Tables
705
PA
701
707
706
A/D
HDET Power Detector
Maximum Setting
Tx UHF

FIG. 7

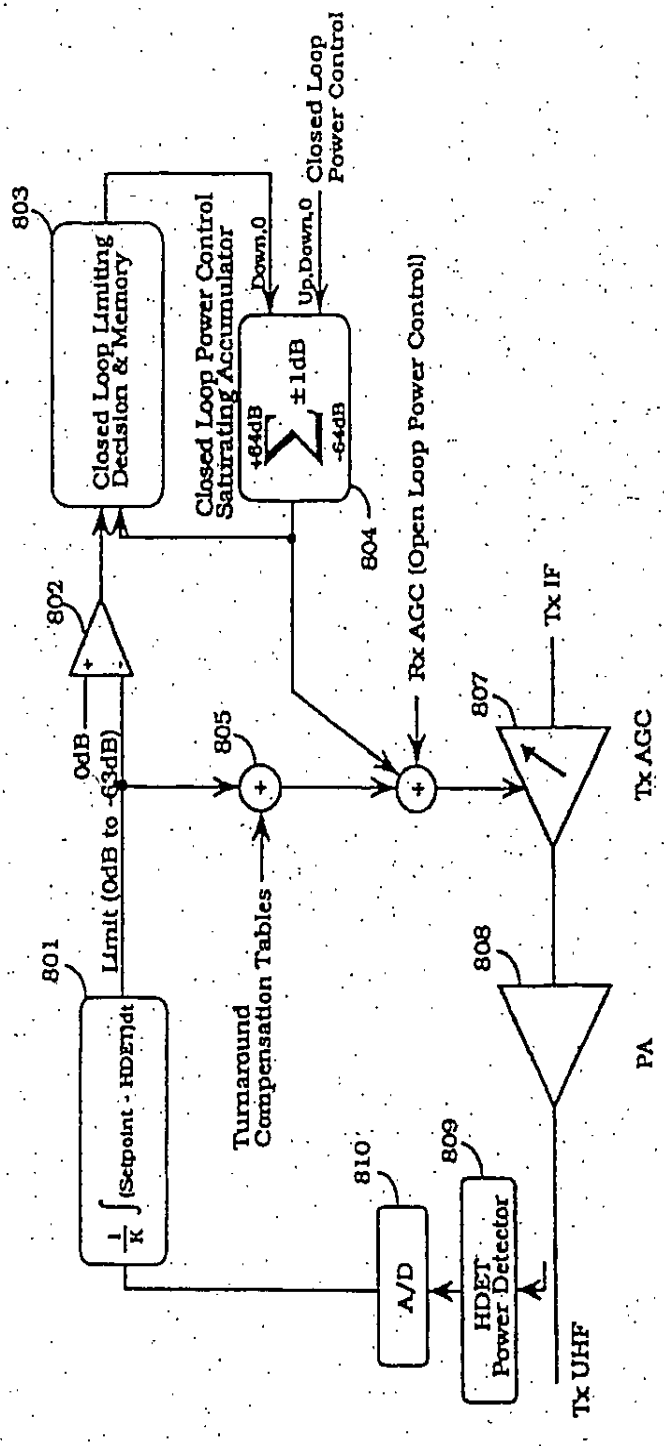

Closed Loop Power Control
Up,Down,0
Down,0
803
Closed Loop Limiting Decision & Memory
Closed Loop Power Control Saturating Accumulator
±1dB
+64dB
-64dB
804
Rx AGC (Open Loop Power Control)
802
0dB
-63dB
805
Limit (0dB to -63dB)
Turnaround Compensation Tables
807
Tx IF
Tx AGC
808
PA
801
$\frac{1}{K}\int$(Setpoint - HDET)dt
810
A/D
809
HDET Power Detector
Tx UHF

FIG. 8

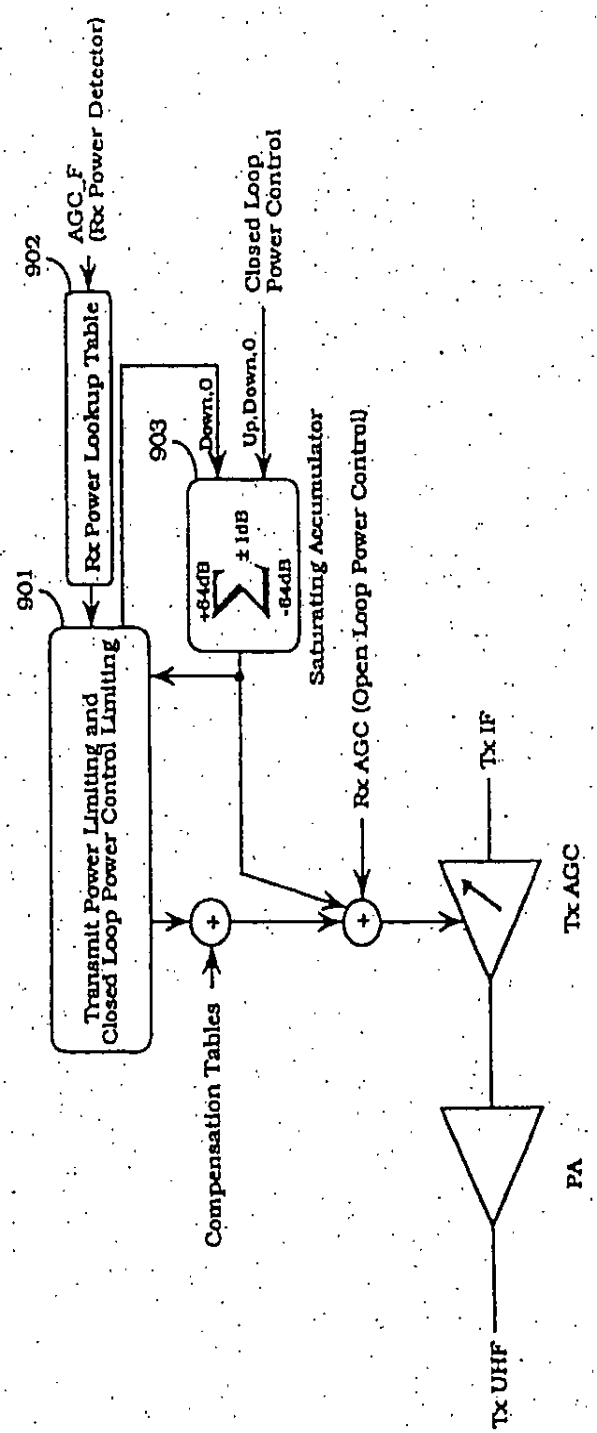

AGC_F (Rx Power Detector)
902
Rx Power Lookup Table
Closed Loop Power Control
Up.Down.0
Down.0
903
+8dB
± 1dB
-8dB
Saturating Accumulator
901
Transmit Power Limiting and Closed Loop Power Control Limiting
Rx AGC (Open Loop Power Control)
Tx IF
Tx AGC
Compensation Tables
PA
Tx UHF

FIG. 9

REVERSE LINK, TRANSMIT POWER CORRECTION AND LIMITATION IN A RADIOTELEPHONE SYSTEM

This is a Divisional of application Ser. No. 08/203,151, filed Feb. 28, 1994, U.S. Pat. No. 5,452,473.

BACKGROUND OF THE INVENTION

I. Field of the Invention

The present invention relates to radio communications. More particularly, the present invention relates to power control in a radio-telephone system.

II. Description of the Related Art

The Federal Communications Commission (FCC) governs the use of the radio frequency (RF) spectrum. The FCC allocates certain band-widths within the RF spectrum for specific uses. A user of an allocated bandwidth of the RF spectrum must take measures to ensure that the radiated emissions inside and outside of that bandwidth are maintained within acceptable levels to avoid interfering with other users operating in the same and or other bandwidths. These levels are governed by both the FCC and the particular user-groups of said bandwidth.

The 800 MHz cellular telephone system operates its forward link, the cell to radiotelephone transmission, in the bandwidth of 869.01 MHz to 893.97 MHz and the reverse link, the radiotelephone to cell transmission, in the bandwidth of 824.01 MHz to 848.97 MHz. The forward and reverse link bandwidths are split up into channels each of which occupies a 30 kHz bandwidth. A particular user of the cellular system may operate on one or several of these channels at a time. All users of the system must ensure that they are compliant with the level of radiated emissions allowable inside and outside of the channel or channels that they have been assigned.

There are several different techniques of modulation that can be used in the cellular telephone system. Two examples of modulation techniques are frequency division multiple access (FDMA) and code division multiple access (CDMA).

The FDMA modulation technique generates signals that occupy one channel at a time while the CDMA modulation technique generates signals that occupy several channels. Both of these techniques must control their return link radiated emissions to within acceptable limits inside and outside of the assigned channel or channels. For maximum system performance, users of the CDMA technique must carefully control the level of radiated power inside the channels in which they are operating.

FIG. 1 shows a typical cellular radiotelephone. In both an FDMA and a CDMA based radiotelephone, there exists the possibility of driving the power amplifier (101) in the transmitter beyond a point where acceptable out of channel radiated emissions are maintained. This is primarily due to the increased distortion output levels of the power amplifier (101) at high output powers. Also, driving the power amplifier (101) beyond a certain point can cause interference internal to the radio. For example, PA puncturing in CDMA affects synthesizer phase noise due to large current transitions. Both of these issues cause unacceptable radio performance.

Maintaining the proper on-channel output power can be difficult due to several undesirable effects in the radiotelephone hardware. For example, the CDMA based radio must implement a power control system that operates over a very wide dynamic range, 80dB to 90dB, such that the transmitted output power is linearly related to the received input power.

Closed loop and open loop power control together determine the return link transmit energy, as disclosed in U.S. Pat. No. 5,056,109 to Gilhousen et al. and assigned to Qualcomm, Incorporated. Therefore, the linear and nonlinear errors produced in both the receiver (103) and transmitter (102) RF sections can cause unacceptable power control performance. Also, both the FDMA and CDMA based radios must operate on different channels while maintaining acceptable output power levels. Variation in output power level and input power detection versus frequency can cause an unacceptable amount of error in the amount of return link transmitted energy.

These issues present significant problems to the designer of both FDMA and CDMA based radiotelephones. There is a resulting need for an effective, cost efficient means of correcting these problems.

SUMMARY OF THE INVENTION

The process of the present invention enables a radiotelephone to operate in a linear fashion over a wide dynamic range while maintaining acceptable transmit output power levels inside and outside of the return link bandwidth. The forward and return link power are measured by power detectors and input to an analog to digital converter accessible by both control hardware and/or software. The closed loop power control setting is also monitored. The radiotelephone uses the detected power levels and closed loop power control setting to index a set of correction tables that indicate the reverse link transmit power error and desired power amplifier biasing for the particular operating point. The radiotelephone also determines if the transmitter is operating above a maximum set point. The transmit gain and power amplifier biasing of the radiotelephone are adjusted to correct the undesired error and maintain the desired output power.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a block diagram of a typical prior art radiotelephone frequency section for use in a radiotelephone system.

FIG. 2 shows a block diagram of the preferred embodiment power control correction implementation.

FIG. 3 shows a block diagram of the power limiting control section as related to FIG. 2.

FIG. 4 shows a block diagram of the closed loop power control section as related to FIG. 2.

FIG. 5 shows a block diagram of the PA limit threshold control section as related to FIG. 2.

FIG. 6 shows an alternate embodiment of the present invention that employs a power limiting control system based on accumulator feedback control.

FIG. 7 shows an alternate embodiment of the present invention that employs a power limiting control system based on the closed loop power control accumulator.

FIG. 8 shows an alternate embodiment of the present invention that employs a power limiting control system based on integral feedback control.

FIG. 9 shows an alternate embodiment of the present invention that employs a power limiting control system based on a measure of receive power and the closed loop power control setting to estimate output power.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The process of the present invention provides power control correction for a mobile radiotelephone as well as maintaining acceptable in and out of band maximum emission levels. This is accomplished by real-time compensation utilizing a set of correction tables that are generated during the production testing of each radiotelephone.

FIG. 2 shows a block diagram of a CDMA radiotelephone with the preferred embodiment power control correction implementation. FIGS. 3, 4, and 5 detail specific blocks of FIG. 2. The radiotelephone is comprised of a receive linearization section, transmit linearization section, power amplifier bias control section, and power limiting control section.

The receive linearization section includes an automatic gain control (AGC) section. The signal input to the AGC section is received on the forward link and amplified by a low noise amplifier (LNA) (211). The output of the LNA (211) is input to a variable gain amplifier (212). The variable gain amplifier (212) produces a signal that is converted to a digital signal using an analog to digital converter (ADC) (213).

The power of the digitized received signal is next computed by a digital power detector (214). The power detector (214) includes an integrator that integrates the detected power with respect to a reference voltage. In the preferred embodiment, this reference voltage is provided by the radio's demodulator to indicate the nominal value at which the demodulator requires the loop to lock in order to hold the power level constant. The demodulator requires this value for optimum performance since a power level too far out of the optimum range will degrade the performance of the demodulator. The power detector (214) performs the integration, thus generating an AGC setpoint. The setpoint and a receive frequency index are input to a receiver linearizing table (216).

The AGC setpoint and the frequency index are used to address the linearizer (216), thus accessing the proper calibration value. This calibration value is then output to a digital to analog converter (215) that generates the analog representation of the receive AGC setting.

The analog value adjusts the biasing of the variable gain amplifier (212). The control of the variable gain amplifier (212) forces the receive AGC loop to close such that the input to the receiver linearizing table (216) follows a predetermined straight line with respect to RF input power. This linearization removes the undesired linear and non-linear errors in addition to variations versus frequency that would otherwise be apparent at the input to the receiver linearizing table (216) in the receiver. These errors and variations would contribute to errors in the transmitter.

In order to reduce the error in the receive and transmit chains versus frequency, the receive and transmit linearizers utilize the frequency index that specifies the current center frequency on which the receive and transmit chains are operating. During factory calibration of the radiotelephone, the linearizers are loaded with values, in addition to the previously mentioned calibration values, that are indexed by frequency to correct the errors related to operating center frequency.

The AGC setpoint is the open loop power control signal for the radio. In the preferred embodiment, this is the power control performed by the radio by itself without control input from the cells. As the power of the signal received from the cell increases, the radio decreases its transmit power. This output power control is accomplished by the AGC setpoint that is filtered by a low pass filter (217).

The transmit section includes a digital summer (210) that combines the AGC setpoint and a closed loop power control setting (206). The output of the summer (210) is fed into a power control limiting section (205). The operation of the power control limiting section (205) and the closed loop power control section (206), illustrated in FIGS. 3 and 4 respectively, will be discussed subsequently in greater detail.

The output of the power control limiting section (205), along with the transmit frequency index, are used to address values stored in a transmitter linearizing table (204). The transmitter linearizing table (204) contains values determined from production testing of the radiotelephone. The selected value is input to a digital to analog converter (203) whose output, an analog representation of the digital value input, controls a variable gain amplifier (202).

The biasing of the variable gain amplifier (202) is adjusted by the analog calibration value to a point such that the input to the transmitter linearizing table (204) follows a predetermined straight line with respect to transmitted RF output power. This linearization removes the undesired linear and non-linear errors along with variations versus frequency in the transmitter. This, combined with the previously mentioned receive linearization, greatly reduces the open and closed loop power control errors due to RF performance imperfections.

The power amplifier (PA) bias control section (218) controls the bias point of the transmit PA (201) based on the transmit gain setting such that the transmit sidebands for the given gain setting are optimized versus PA (201) current consumption. This allows a battery powered telephone to maximize talk time by reducing PA (201) current consumption at lower output powers while still maintaining acceptable sideband levels at higher output power levels.

The power control limiting section (205) is illustrated in FIG. 3. The power control limiting section (205) controls the closed loop power control and transmit gain settings when the output of the transmit gain summer (210) corresponds to a transmit output power level which is equal to or greater than the intended maximum output power. The maximum gain setting is determined by the PA limit threshold control section (209).

The threshold control section (209) determines the maximum gain setting based on a nominal value that is modified by a real-time measurement of the transmitted output power. The measurement is accomplished by an analog power detector (207) whose output transformed into a digital signal by an analog to digital converter (208). The digitized power value is then input to the threshold control section (209).

The threshold control section, detailed in FIG. 5, operates by the high power detector (HDET) linearizer (501) scaling the input digitized power value in order to match the numerology of the digital transmit gain control section. The scaled output from the linearizer (501) is subtracted (502) from the nominal maximum gain setting. This maximum gain setting can be hard coded into the radio during assembly or input during manufacturing and testing of the radio.

The difference of the maximum gain setting and the scaled output power is then added, by the adder (503) to the maximum gain setting. The sum of these signals is then used as the corrected maximum gain setting. This real-time modification of the detected power helps mitigate the errors introduced by temperature variations and aging of the transmitter PAs. In other words, if the difference between the

Ex. G-12

Ex. F-12

maximum gain setting and the real-time measured power value is 0, then no correction is necessary. If there is a difference between the two, the difference is used to correct the maximum gain setting.

Referring to FIG. 3, a digital comparator (301) detects when the output of the transmit gain summer (210) equals or exceeds the maximum gain setting. The comparator (301) controls a 2:1 multiplexer (302) that outputs the maximum allowable setting when the output of the summer (210) exceeds the maximum allowable setting. When the output of the summer (210) is less than the maximum allowable setting, the multiplexer (302) outputs the direct output of the summer (210). This prohibits the transmitter from exceeding its maximum operating point.

The closed loop power control section (206), illustrated in FIG. 4, accumulates the power control commands sent on the forward link by the controlling radiotelephone cell site and outputs a gain adjust signal. The power control commands are collected in an accumulator (401). The operation of the accumulator (401) is controlled by the power control limiting section (205) when the transmit power amplifier (201) is outputting the maximum allowable power.

When the output of the summer (210) changes from being less than to equal or greater than the maximum allowable setting, the output of the closed loop power control accumulator (401) is latched into a flip-flop (402). While the output of the summer (210) is equal to or greater than the maximum allowable setting, as determined by the comparator (403) and NAND gate (404), an AND gate (405) masks off any closed loop power control up commands that would force the accumulator (401) above the flip-flop's (402) latched value. This prevents the accumulator from saturating during power limiting yet allows the closed loop power control setting to change anywhere below the latched value.

An alternate embodiment of the process of the present invention is illustrated in FIG. 6. In this embodiment, a power limiting control system is employed based on accumulator feedback control. The system operates by first measuring the output power of the power amplifier (609) using a power detector (610). The detected power is then digitized by an ADC (611) and compared to a maximum allowable setting by the comparator (601). If the output power is greater than the maximum setting, the power limiting accumulator (602) begins turning power down by reducing the gain of the variable gain amplifier (608). If the output power is less than the maximum setting the power limiting accumulator (602) returns to a 0*dB* correction value.

In this embodiment, a closed loop power control limiting function(604 and 60), similar to the preferred embodiment, is employed. However, the trigger for the closed loop power control limiting function is a comparator (603) that detects when the power limiting accumulator (602) is limiting the output power by comparing the accumulator (602) output to 0*dB* with the comparator (603). The linearizing compensation tables, similar to the tables in the preferred embodiment, are added into the transmit gain control using a summer (606).

In another alternate embodiment, illustrated in FIG. 7, a power limiting control system is employed that is based on the closed loop power control accumulator (702). The system operates by first measuring the output power of the power amplifier (705) using a power detector (706). The detected power is digitized (707) and compared to a maximum allowable setting by the comparator (701). If the output power is greater than the maximum setting, the closed loop power control accumulator (702) is modified to turn the amplifier (704) power down by one step each 1.25 ms until the output power is less than the maximum setting. If the output power is less than the maximum setting, the closed loop power control accumulator is not modified. The linearizing compensation tables, similar to the preferred embodiment, are added into the transmit gain control using a summer (703).

In yet another embodiment, illustrated in FIG. 8, a power limiting control system is employed that is based on integral feedback control. The system operates by first measuring the output power of the power amplifier (808) using a power detector (809). The detected power is digitized (810) and input to an integrator (801) that follows the equation:

$$\frac{1}{T}\cdot\int(\text{Setpoint}-\text{Detected})dt$$

The integrator (801), generating a gain control signal, saturates at 0 dB and −63 dB of correction. The gain control signal is thus limited within a range. If the output power is greater than the setpoint, the integrator turns down the output power of the amplifier (807) at a rate based on the integration constant K until the setpoint is reached. The integrator is allowed to turn power down by as much as 63 dB. If the output power is less than the setpoint, the output of the integrator (801) will be forced to zero, thus not adjusting output power.

In this embodiment, a closed loop power control limiting function (803 and 804), similar to the preferred embodiment, is employed. The trigger for the closed loop power control limiting function, however, is a comparator (802) that detects when the power limiting integrator (801) is limiting the output power. The linearizing compensation tables, similar to the preferred embodiment, are added into the transmit gain control using a summer (805).

In still another embodiment, illustrated in FIG. 9, a power limiting control system is employed that is based only on a measure of receive power as determined by the Rx power lookup table (902), and the closed loop power control setting as opposed to actual output power. The transmit power limiting and closed loop power control limiting function (901) can be implemented with either the preferred embodiment using the saturating accumulator (903), or one of the alternate embodiments. However, only the receive power and closed loop power control setting are used to estimate transmit output power.

In summary, the process of the present invention ensures that the transmitted sidebands and synthesizer phase noise of a radio transmitter remains within a predetermined specification by limiting the maximum output power. This power limitation is accomplished by a control loop including a calibration look-up table. Therefore, a radiotelephone using the process of the present invention would not exceed it's nominal maximum power level due to the cell issuing too many power turn-up commands. The radiotelephone limits the power output even when the cell erroneously decides the radiotelephone power should be increased.

We claim:

1. A method for limiting transmit power of a radio operating in a radio communications system, the radio communications system comprising at least one base station that transmits signals including power control commands to the radio, the radio comprising a variable gain amplifier and a maximum gain setting, the method comprising the steps of:

determining an open loop power control value in response to a signal received from the at least one base station;

determining a gain adjust signal in response to the transmitted power control commands;

combining the open loop power control value and the gain adjust signal to produce a summation signal;

comparing the summation signal to the maximum gain setting;

if the summation signal is greater than or equal to the maximum gain setting, adjusting the variable gain amplifier in response to the maximum gain setting; and

if the summation signal is less than the maximum gain setting, adjusting the variable gain amplifier in response to the summation signal.

2. The method of claim 1 and further including the step of adjusting the maximum gain setting in response to a temperature of the variable gain amplifier.

3. The method of claim 2 wherein the step of adjusting the maximum gain setting further includes the steps of:

the variable gain amplifier transmitting a signal;

detecting a power value of the transmitted signal;

scaling the power value to produce a scaled power signal;

subtracting the maximum gain setting from the scaled power signal to produce a difference signal; and

adding the difference signal to the maximum gain setting.

4. A method for limiting transmit power of a radio operating in a cellular environment, the cellular environment comprising a plurality of cells that transmit power control commands to the radio, the radio comprising a variable gain amplifier and a maximum gain setting, the method comprising the steps of:

determining an open loop power control value in response to a signal received from at least one cell of the plurality of cells;

determining a gain adjust signal in response to the transmitted power control commands;

combining the open loop power control value and the gain adjust signal to produce a summation signal;

adjusting the maximum gain setting in response to a temperature of the variable gain amplifier;

comparing the adjusted maximum gain setting to the summation signal;

if the summation signal is greater than or equal to the adjusted maximum gain setting, prohibiting the gain adjust signal from increasing in response to the transmitted power control commands;

if the summation signal is greater than or equal to the adjusted maximum gain setting, adjusting the variable gain amplifier in response to the adjusted maximum gain setting; and

if the summation signal is less than the adjusted maximum gain setting, adjusting the variable gain amplifier in response to the summation signal.

5. A method for limiting transmit power of a radio operating in a cellular environment, the cellular environment comprising a plurality of cells that transmit power control commands to the radio, the radio comprising a variable gain amplifier, a maximum gain setting, and a power limiting accumulator, the method comprising the steps of:

the variable gain amplifier transmitting a signal;

determining a gain adjust signal in response to the transmitted power control commands;

detecting a power value of the transmitted signal;

digitizing the power value;

comparing the digitized power value to the maximum gain setting;

if the digitized power value is greater than the maximum gain setting, decreasing the gain of the variable gain amplifier; and

if the digitized power value is greater than the maximum gain setting, prohibiting the gain adjust signal from increasing in response to the transmitted power control commands.

6. A method for limiting transmit power of a radio operating in a cellular environment, the cellular environment comprising a plurality of cells that transmit power control commands to the radio, the radio comprising a variable gain amplifier, a maximum gain setting, and a power control command accumulator that generates a gain adjust signal, the method comprising the steps of:

the variable gain amplifier transmitting a signal;

determining the gain adjust signal in response to the transmitted power control commands;

detecting a power value of the transmitted signal;

digitizing the power value;

comparing the digitized power value to the maximum gain setting;

if the digitized power value is greater than the maximum gain setting, decreasing the gain adjust signal by a predetermined amount for every predetermined unit of time until the gain adjust signal is less than the maximum gain setting; and

if the digitized power value is less than or equal to the maximum gain setting, varying the gain of the variable gain amplifier in response to the gain adjust signal.

7. A method for limiting transmit power of a radio operating in a cellular environment, the cellular environment comprising a plurality of cells that transmit power control commands to the radio, the radio comprising a variable gain amplifier, a maximum gain setting, and a power limiting accumulator, the method comprising the steps of:

the variable gain amplifier transmitting a signal;

determining a gain adjust signal in response to the transmitted power control commands;

detecting a power value of the transmitted signal;

digitizing the power value;

determining a difference between the digitized power value and the maximum gain setting;

integrating the difference to generate a gain control signal, the gain control signal being limited to a predetermined range;

adjusting the variable gain amplifier with the gain control signal; and

if the gain control signal is less than a predetermined value, prohibiting the gain adjust signal from increasing the variable gain amplifier in response to the transmitted power control commands.

* * * * *

US005655220A

United States Patent [19]

Weiland et al.

[11] Patent Number: 5,655,220

[45] Date of Patent: Aug. 5, 1997

[54] REVERSE LINK, TRANSMIT POWER CORRECTION AND LIMITATION IN A RADIOTELEPHONE SYSTEM

[75] Inventors: Ana L. Weiland, Encinitas; Richard K. Kornfeld; John E. Maloney, both of San Diego, all of Calif.

[73] Assignee: Qualcomm Incorporated, San Diego, Calif.

[21] Appl. No.: 532,383

[22] Filed: Sep. 22, 1995

Related U.S. Application Data

[60] Continuation of Ser. No. 406,432, Mar. 20, 1995, abandoned, which is a division of Ser. No. 203,151, Feb. 28, 1994, Pat. No. 5,452,473.

[51] Int. Cl.[6] H04B 7/00; H04Q 7/32

[52] U.S. Cl. 455/69; 455/126; 455/115; 375/345; 370/318

[58] Field of Search 455/33.1, 69, 70, 455/126, 127, 115, 117, 116, 54.1, 54.2, 67.1, 63, 67.6, 88; 330/129, 132, 136, 278, 85, 75, 282; 375/200, 205, 296, 297, 345; 370/318, 320, 335, 310

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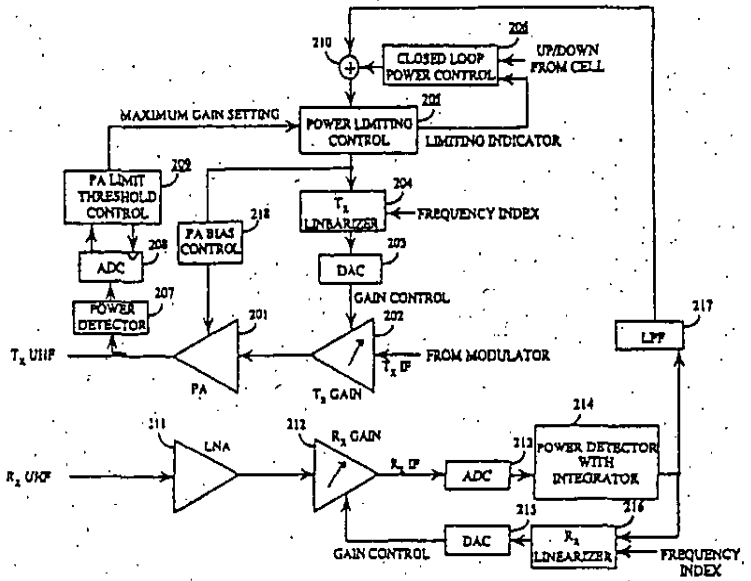
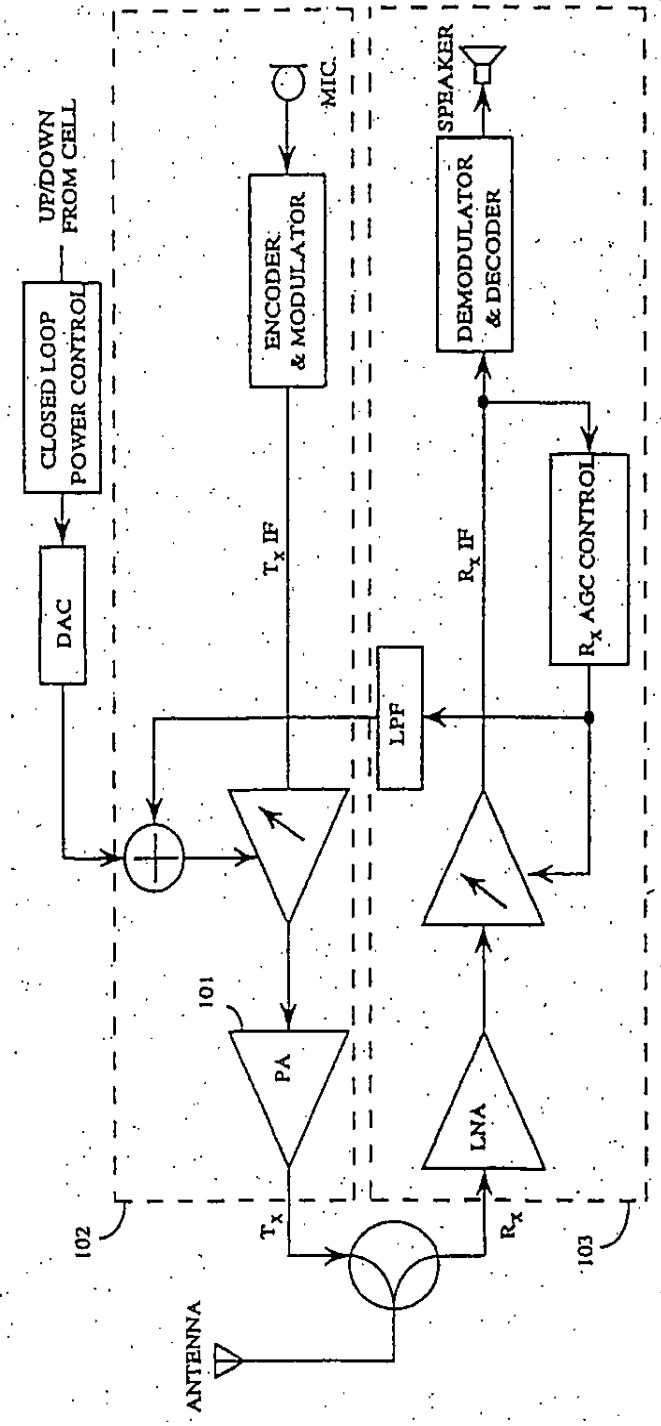
Primary Examiner—Reinhard J. Eisenzopf
Assistant Examiner—Doris To
Attorney, Agent, or Firm—Russell B. Miller; Roger W. Martin

[57] ABSTRACT

The process and apparatus of the present invention limits the output power of a radiotelephone, operating in a cellular system in the preferred embodiment. This ensures the transmitted sidebands and synthesizer phase noise remains within a certain specification. This is accomplished by power detection and a correction accumulator that together generate a gain control signal by limiting the gain adjustment to a maximum value, even when the cell site communicating with the radiotelephone is sending power turn-up commands to the radiotelephone. This process includes dynamically correcting the output level of the transmitter due to gain variations in the transmitter stages or gain control elements.

9 Claims, 9 Drawing Sheets





PRIOR ART

FIG. 1

Ex. H-2

Ex. G-2

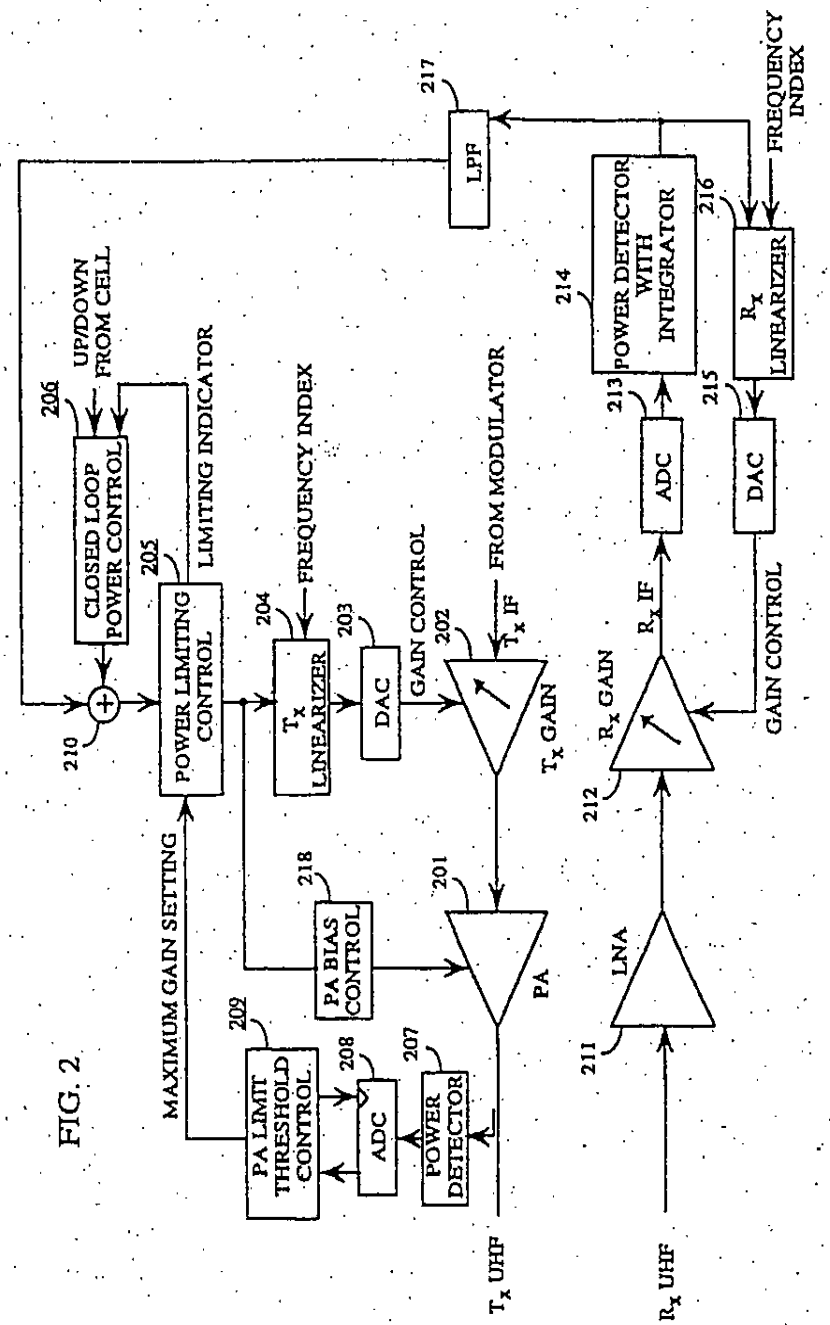
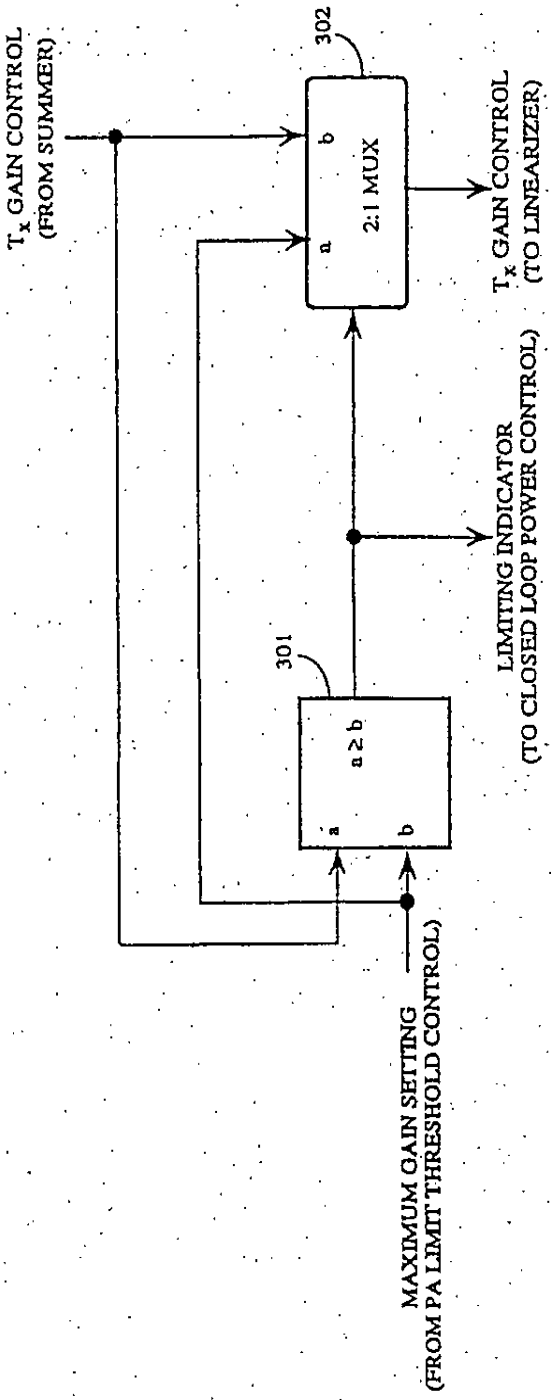


FIG. 2

Ex. H-3

Ex. G-3



205

FIG. 3

Ex. H-4

Ex. G-4

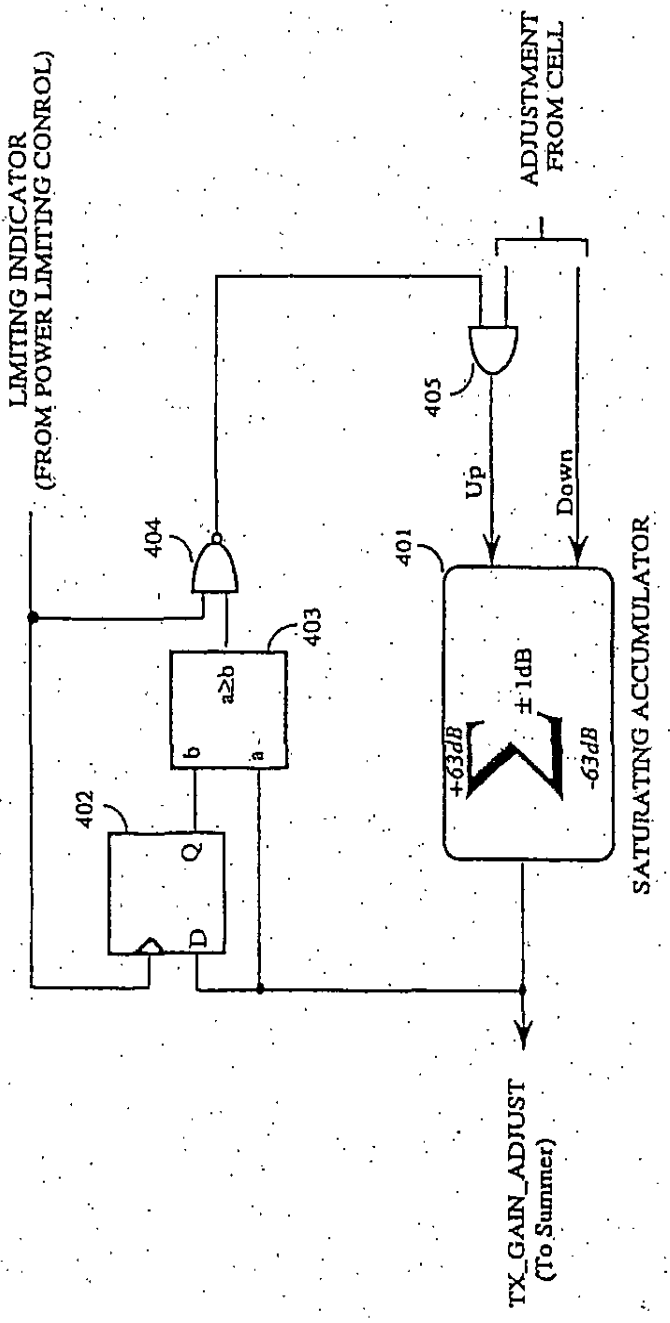
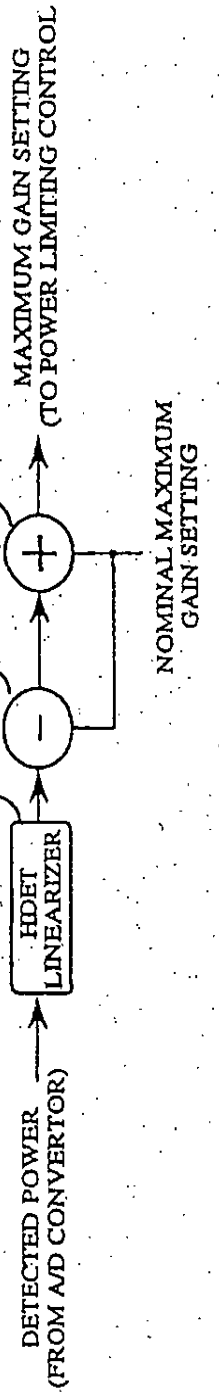


FIG. 4

Ex. H-5

Ex. G-5



209

FIG. 5

Ex. H-6

Ex. G-6

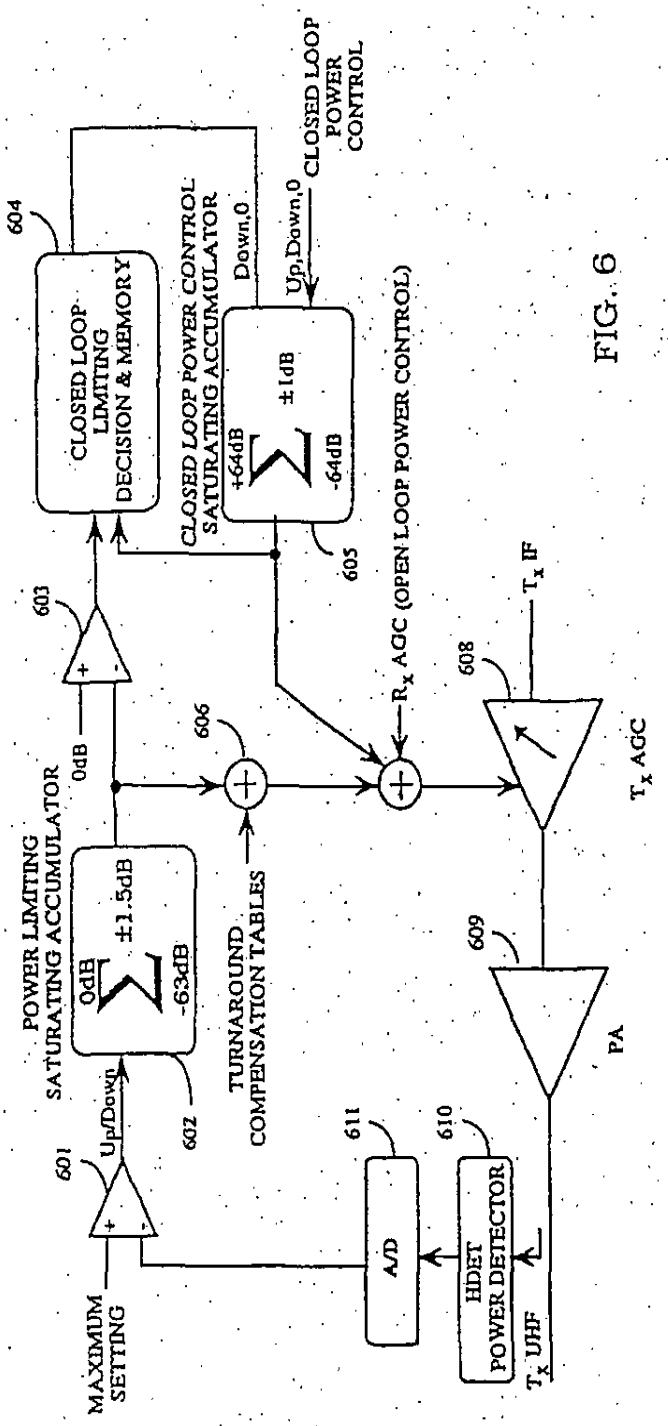


FIG. 6

Ex. H-7

Ex. G-7

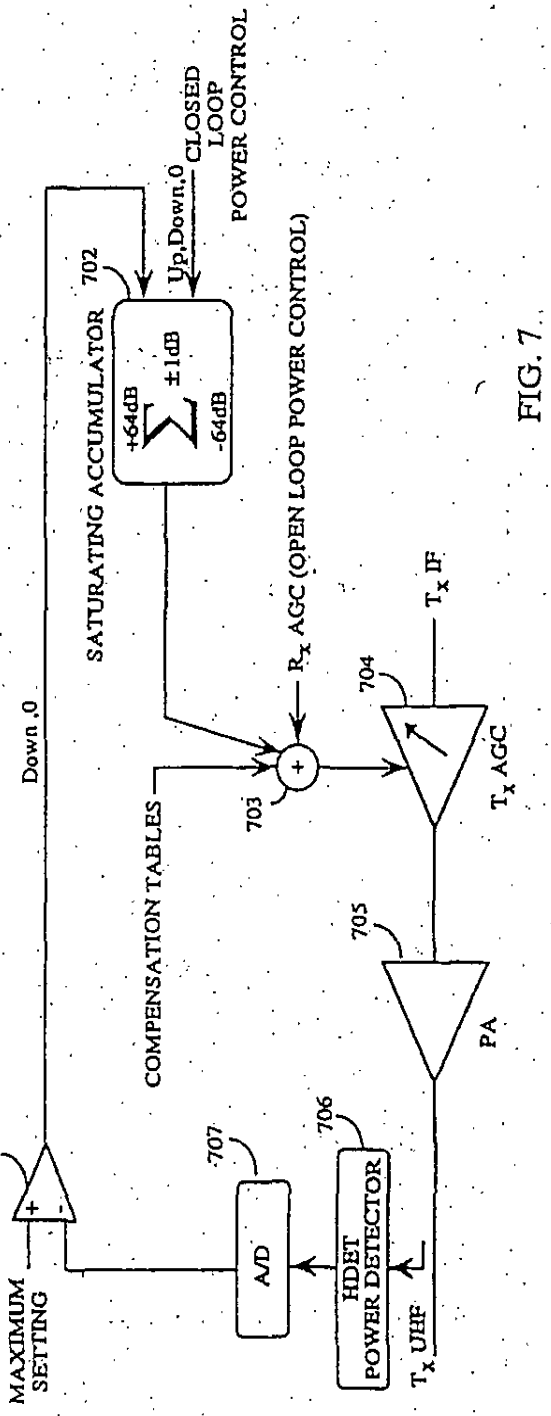


FIG. 7

Ex. H-8

Ex. G-8

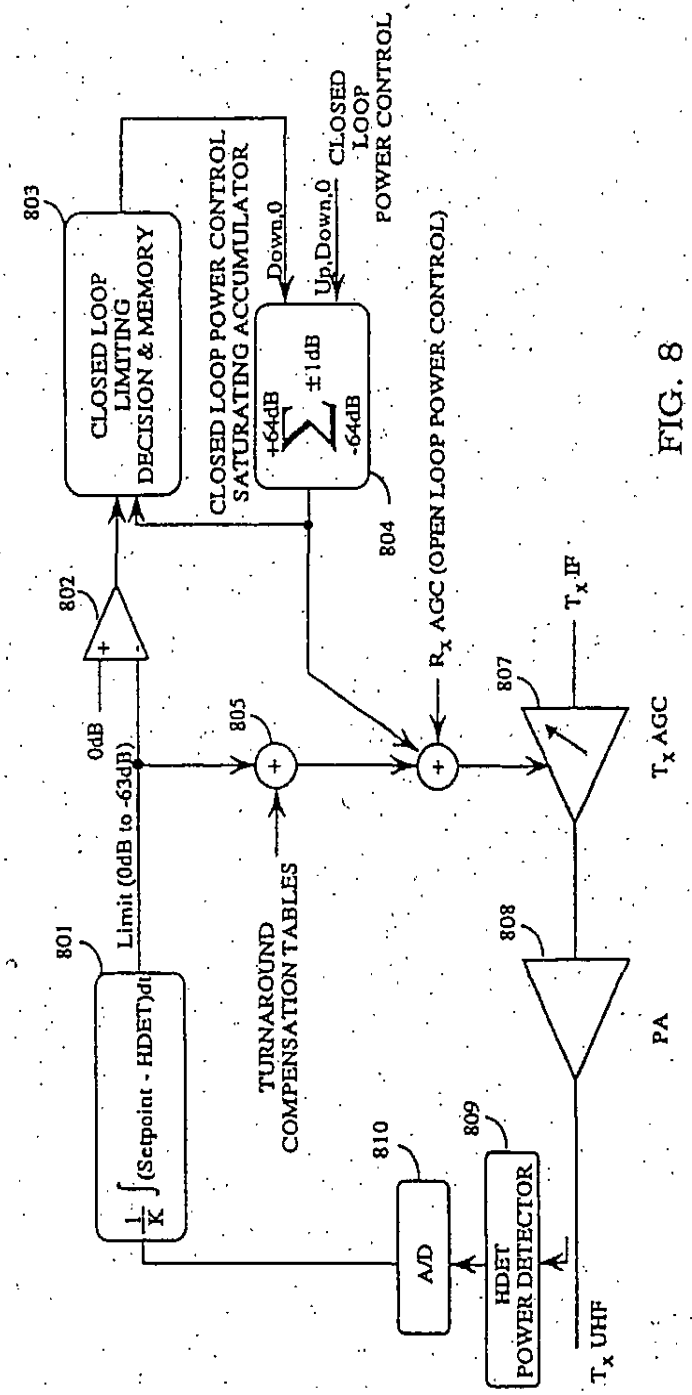


FIG. 8

Ex. H-9

Ex. G-9

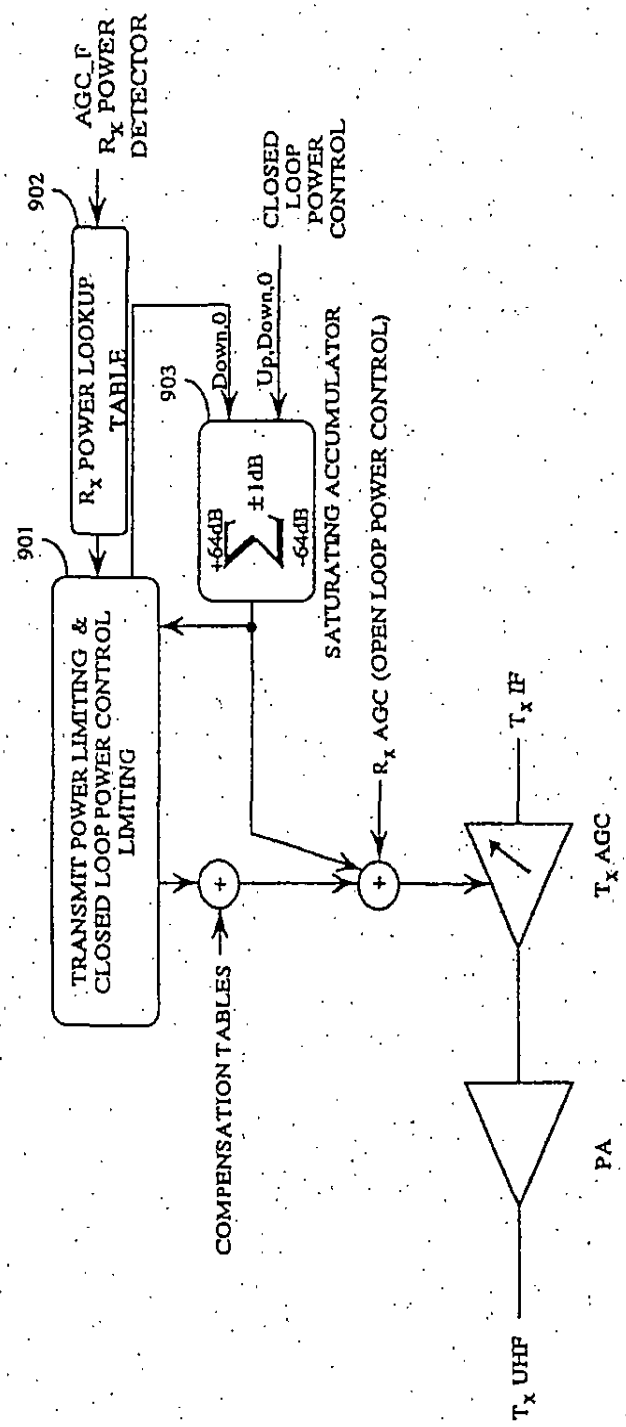


FIG. 9

Ex. H-10

Ex. G-10

REVERSE LINK, TRANSMIT POWER CORRECTION AND LIMITATION IN A RADIOTELEPHONE SYSTEM

This is a continuation of application Ser. No. 08/406,432, filed Mar. 20, 1995 now abandoned, which is a Divisional of application Ser. No. 08/203,151, filed Feb. 28, 1994 now U.S. Pat. No. 5,452,473.

BACKGROUND OF THE INVENTION

I. Field of the Invention

The present invention relates to radio communications. More particularly, the present invention relates to power control in a radiotelephone system.

II. Description of the Related Art

The Federal Communications Commission (FCC) governs the use of the radio frequency (RF) spectrum. The FCC allocates certain bandwidths within the RF spectrum for specific uses. A user of an allocated bandwidth of the RF spectrum must take measures to ensure that the radiated emissions inside and outside of that bandwidth are maintained within acceptable levels to avoid interfering with other users operating in the same and or other bandwidths. These levels are governed by both the FCC and the particular user groups of said bandwidth.

The 800 MHz cellular telephone system operates its forward link, the cell to radiotelephone transmission, in the bandwidth of 869.01 MHz to 893.97 MHz and the reverse link, the radiotelephone to cell transmission, in the bandwidth of 824.01 MHz to 848.97 MHz. The forward and reverse link bandwidths are split up into channels each of which occupies a 30 kHz bandwidth. A particular user of the cellular system may operate on one or several of these channels at a time. All users of the system must ensure that they are compliant with the level of radiated emissions allowable inside and outside of the channel or channels that they have been assigned.

There are several different techniques of modulation that can be used in the cellular telephone system. Two examples of modulation techniques are frequency division multiple access (FDMA) and code division multiple access (CDMA).

The FDMA modulation technique generates signals that occupy one channel at a time while the CDMA modulation technique generates signals that occupy several channels. Both of these techniques must control their return link radiated emissions to within acceptable limits inside and outside of the assigned channel or channels. For maximum system performance, users of the CDMA technique must carefully control the level of radiated power inside the channels in which they are operating.

FIG. 1 shows a typical cellular radiotelephone. In both an FDMA and a CDMA based radiotelephone, there exists the possibility of driving the power amplifier (101) in the transmitter beyond a point where acceptable out of channel radiated emissions are maintained. This is primarily due to the increased distortion output levels of the power amplifier (101) at high output powers. Also, driving the power amplifier (101) beyond a certain point can cause interference internal to the radio. For example, PA puncturing in CDMA affects synthesizer phase noise due to large current transitions. Both of these issues cause unacceptable radio performance.

Maintaining the proper on-channel output power can be difficult due to several undesirable effects in the radiotelephone hardware. For example, the CDMA based radio must

implement a power control system that operates over a very wide dynamic range, 80 dB to 90 dB, such that the transmitted output power is linearly related to the received input power.

Closed loop and open loop power control together determine the return link transmit energy, as disclosed in U.S. Pat. No. 5,056,109 to Gilhousen et al. and assigned to Qualcomm, Incorporated. Therefore, the linear and nonlinear errors produced in both the receiver (103) and transmitter (102) RF sections can cause unacceptable power control performance. Also, both the FDMA and CDMA based radios must operate on different channels while maintaining acceptable output power levels. Variation in output power level and input power detection versus frequency can cause an unacceptable amount of error in the amount of return link transmitted energy.

These issues present significant problems to the designer of both FDMA and CDMA based radiotelephones. There is a resulting need for an effective, cost efficient means of correcting these problems.

SUMMARY OF THE INVENTION

The process of the present invention enables a radiotelephone to operate in a linear fashion over a wide dynamic range while maintaining acceptable transmit output power levels inside and outside of the return link bandwidth. The forward and return link power are measured by power detectors and input to an analog to digital converter accessible by both control hardware and/or software. The closed loop power control setting is also monitored. The radiotelephone uses the detected power levels and closed loop power control setting to index a set of correction tables that indicate the reverse link transmit power error and desired power amplifier biasing for the particular operating point. The radiotelephone also determines if the transmitter is operating above a maximum set point. The transmit gain and power amplifier biasing of the radiotelephone are adjusted to correct the undesired error and maintain the desired output power.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a block diagram of a typical prior art radiotelephone frequency section for use in a radiotelephone system.

FIG. 2 shows a block diagram of the preferred embodiment power control correction implementation.

FIG. 3 shows a block diagram of the power limiting control section as related to FIG.2.

FIG. 4 shows a block diagram of the closed loop power control section as related to FIG.2.

FIG. 5 shows a block diagram of the PA limit threshold control section as related to FIG.2.

FIG. 6 shows an alternate embodiment of the present invention that employs a power limiting control system based on accumulator feedback control.

FIG. 7 shows an alternate embodiment of the present invention that employs a power limiting control system based on the closed loop power control accumulator.

FIG. 8 shows an alternate embodiment of the present invention that employs a power limiting control system based on integral feedback control.

FIG. 9 shows an alternate embodiment of the present invention that employs a power limiting control system based on a measure of receive power and the closed loop power control setting to estimate output power.

Ex. H-11

Ex. G-11

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The process of the present invention provides power control correction for a mobile radiotelephone as well as maintaining acceptable in and out of band maximum emission levels. This is accomplished by realtime compensation utilizing a set of correction tables that are generated during the production testing of each radiotelephone.

FIG. 2 shows a block diagram of a CDMA radiotelephone with the preferred embodiment power control correction implementation. FIGS. 3, 4, and 5 detail specific blocks of FIG. 2. The radiotelephone is comprised of a receive linearization section, transmit linearization section, power amplifier bias control section, and power limiting control section.

The receive linearization section includes an automatic gain control (AGC) section. The signal input to the AGC section is received on the forward link and amplified by a low noise amplifier (LNA) (211). The output of the LNA (211) is input to a variable gain amplifier (212). The variable gain amplifier (212) produces a signal that is converted to a digital signal using an analog to digital converter (ADC) (213).

The power of the digitized received signal is next computed by a digital power detector (214). The power detector (214) includes an integrator that integrates the detected power with respect to a reference voltage. In the preferred embodiment, this reference voltage is provided by the radio's demodulator to indicate the nominal value at which the demodulator requires the loop to lock in order to hold the power level constant. The demodulator requires this value for optimum performance since a power level too far out of the optimum range will degrade the performance of the demodulator. The power detector (214) performs the integration, thus generating an AGC setpoint. The setpoint and a receive frequency index are input to a receiver linearizing table (216).

The AGC setpoint and the frequency index are used to address the linearizer (216), thus accessing the proper calibration value. This calibration value is then output to a digital to analog converter (215) that generates the analog representation of the receive AGC setting.

The analog value adjusts the biasing of the variable gain amplifier (212). The control of the variable gain amplifier (212) forces the receive AGC loop to close such that the input to the receiver linearizing table (216) follows a predetermined straight line with respect to RF input power. This linearization removes the undesired linear and non-linear errors in addition to variations versus frequency that would otherwise be apparent at the input to the receiver linearizing table (216) in the receiver. These errors and variations would contribute to errors in the transmitter.

In order to reduce the error in the receive and transmit chains versus frequency, the receive and transmit linearizers utilize the frequency index that specifies the current center frequency on which the receive and transmit chains are operating. During factory calibration of the radiotelephone, the linearizers are loaded with values, in addition to the previously mentioned calibration values, that are indexed by frequency to correct the errors related to operating center frequency.

The AGC setpoint is the open loop power control signal for the radio. In the preferred embodiment, this is the power control performed by the radio by itself without control input from the cells. As the power of the signal received from the cell increases, the radio decreases its transmit power. This output power control is accomplished by the AGC setpoint that is filtered by a low pass filter (217).

The transmit section includes a digital summer (210) that combines the AGC setpoint and a closed loop power control setting (206). The output of the summer (210) is fed into a power control limiting section (205). The operation of the power control limiting section (205) and the closed loop power control section (206), illustrated in FIGS. 3 and 4 respectively, will be discussed subsequently in greater detail

The output of the power control limiting section (205), along with the transmit frequency index, are used to address values stored in a transmitter linearizing table (204). The transmitter linearizing table (204) contains values determined from production testing of the radiotelephone. The selected value is input to a digital to analog converter (203) whose output, an analog representation of the digital value input, controls a variable gain amplifier (202).

The biasing of the variable gain amplifier (202) is adjusted by the analog calibration value to a point such that the input to the transmitter linearizing table (204) follows a predetermined straight line with respect to transmitted RF output power. This linearization removes the undesired linear and non-linear errors along with variations versus frequency in the transmitter. This, combined with the previously mentioned receive linearization, greatly reduces the open and closed loop power control errors due to RF performance imperfections.

The power amplifier (PA) bias control section (218) controls the bias point of the transmit PA (201) based on the transmit gain setting such that the transmit sidebands for the given gain setting are optimized versus PA (201) current consumption. This allows a battery powered telephone to maximize talk time by reducing PA (201) current consumption at lower output powers while still maintaining acceptable sideband levels at higher output power levels.

The power control limiting section (205) is illustrated in FIG. 3. The power control limiting section (205) controls the closed loop power control and transmit gain settings when the output of the transmit gain summer (210) corresponds to a transmit output power level which is equal to or greater than the intended maximum output power. The maximum gain setting is determined by the PA limit threshold control section (209).

The threshold control section (209) determines the maximum gain setting based on a nominal value that is modified by a real-time measurement of the transmitted output power. The measurement is accomplished by an analog power detector (207) whose output transformed into a digital signal by an analog to digital converter (208). The digitized power value is then input to the threshold control section (209).

The threshold control section, detailed in FIG. 5, operates by the high power detector (HDET) linearizer (501) scaling the input digitized power value in order to match the numerology of the digital transmit gain control section. The scaled output from the linearizer (501) is subtracted (502) from the nominal maximum gain setting. This maximum gain setting can be hard coded into the radio during assembly or input during manufacturing and testing of the radio.

The difference of the maximum gain setting and the scaled output power is then added, by the adder (503), to the maximum gain setting. The sum of these signals is then used as the corrected maximum gain setting. This real-time modification of the detected power helps mitigate the errors introduced by temperature variations and aging of the transmitter PAs. In other words, if the difference between the

Ex. H-12

Ex. G-12

maximum gain setting and the real-time measured power value is 0, then no correction is necessary. If there is a difference between the two, the difference is used to correct the maximum gain setting.

Referring to FIG. 3, a digital comparator (301) detects when the output of the transmit gain summer (210) equals or exceeds the maximum gain setting. The comparator (301) controls a 2:1 multiplexer (302) that outputs the maximum allowable setting when the output of the summer (210) exceeds the maximum allowable setting. When the output of the summer (210) is less than the maximum allowable setting, the multiplexer (302) outputs the direct output of the summer (210). This prohibits the transmitter from exceeding its maximum operating point.

The closed loop power control section (206), illustrated in FIG. 4, accumulates the power control commands sent on the forward link by the controlling radiotelephone cell site and outputs a gain adjust signal. The power control commands are collected in an accumulator (401). The operation of the accumulator (401) is controlled by the power control limiting section (205) when the transmit power amplifier (201) is outputting the maximum allowable power.

When the output of the summer (210) changes from being less than to equal or greater than the maximum allowable setting, the output of the closed loop power control accumulator (401) is latched into a flip-flop (402). While the output of the summer (210) is equal to or greater than the maximum allowable setting as determined by the comparator (403) and NAND gate (404) an AND gate (405) masks off any closed loop power control up commands that would force the accumulator (401) above the flip-flop's (402) latched value. This prevents the accumulator from saturating during power limiting yet allows the closed loop power control setting to change anywhere below the latched value.

An alternate embodiment of the process of the present invention is illustrated in FIG. 6. In this embodiment, a power limiting control system is employed based on accumulator feedback control. The system operates by first measuring the output power of the power amplifier (609) using a power detector (610). The detected power is then digitized by an ADC (611) and compared to a maximum allowable setting by the comparator (601). If the output power is greater than the maximum setting, the power limiting accumulator (602) begins turning power down by reducing the gain of the variable gain amplifier (608). If the output power is less than the maximum setting the power limiting accumulator (602) returns to a 0 dB correction value.

In this embodiment, a closed loop power control limiting function (604 and 605), similar to the preferred embodiment, is employed. However, the trigger for the closed loop power control limiting function is a comparator (603) that detects when the power limiting accumulator (602) is limiting the output power by comparing the accumulator (602) output to 0 dB with the comparator (603). The linearizing compensation tables, similar to the tables in the preferred embodiment, are added into the transmit gain control using a summer (606).

In another alternate embodiment, illustrated in FIG. 7, a power limiting control system is employed that is based on the closed loop power control accumulator (702). The system operates by first measuring the output power of the power amplifier (705) using a power detector (706). The detected power is digitized (707) and compared to a maximum allowable setting by the comparator (701). If the output power is greater than the maximum setting, the closed loop power control accumulator (702) is modified to turn the amplifier (704) power down by one step each 1.25 ms until the output power is less than the maximum setting. If the output power is less than the maximum setting, the closed loop power control accumulator is not modified. The linearizing compensation tables, similar to the preferred embodiment, are added into the transmit gain control using a summer (703).

In yet another embodiment, illustrated in FIG. 8, a power limiting control system is employed that is based on integral feedback control. The system operates by first measuring the output power of the power amplifier (808) using a power detector (809). The detected power is digitized (810) and input to an integrator (801) that follows the equation:

$$1/K\int(\text{Setpoint}-\text{Detected})dt.$$

The integrator (801), generating a gain control signal, saturates at 0 dB and −63 dB of correction. The gain control signal is thus limited within a range. If the output power is greater than the setpoint, the integrator turns down the output power of the amplifier (807) at a rate based on the integration constant K until the setpoint is reached. The integrator is allowed to turn power down by as much as 63 dB. If the output power is less than the setpoint, the output of the integrator (801) will be forced to zero, thus not adjusting output power.

In this embodiment, a closed loop power control limiting function (803 and 804), similar to the preferred embodiment, is employed. The trigger for the closed loop power control limiting function, however, is a comparator (802) that detects when the power limiting integrator (801) is limiting the output power. The linearizing compensation tables, similar to the preferred embodiment, are added into the transmit gain control using a summer (805).

In still another embodiment, illustrated in FIG. 9, a power limiting control system is employed that is based only on a measure of receive power, as determined by the Rx power lookup table (902), and the closed loop power control setting as opposed to actual output power. The transmit power limiting and closed loop power control limiting function (901) can be implemented with either the preferred embodiment using the saturating accumulator (903) or one of the alternate embodiments. However, only the receive power and closed loop power control setting are used to estimate transmit output power.

In summary, the process of the present invention ensures that the transmitted sidebands and synthesizer phase noise of a radio transmitter remains within a predetermined specification by limiting the maximum output power. This power limitation is accomplished by a control loop including a calibration look-up table. Therefore, a radiotelephone using the process of the present invention would not exceed it's nominal maximum power level due to the cell issuing too many power turn-up commands. The radiotelephone limits the power output even when the cell erroneously decides the radiotelephone power should be increased.

We claim:

1. A method for limiting transmit power of a radio operating in a cellular environment, the cellular environment comprising a plurality of cells that transmit power control commands to the radio, the radio comprising a variable gain amplifier and a power limiting accumulator, the method comprising the steps of:

receiving a signal from at least one of the plurality of cells;

determining a power level of the received signal;

determining a closed loop power control value in response to the received signal;

generating a limiting gain control setting in response to the closed loop power control value and the power level, the limiting gain control setting being within a predetermined range;

combining the closed loop power control value, the power level, and the limiting gain control setting to generate a gain control signal and

adjusting the variable gain amplifier in response to the gain control signal.

2. A method for limiting transmit power of a radio operating in a radio communications system, the radio communications system comprising a plurality of base stations that transmit power control commands to the radio, the radio comprising a variable gain amplifier and a maximum gain setting, the method comprising the steps of:

receiving a signal from at least one of the plurality of base stations;

generating a received power level signal in response to the received signal;

generating a closed loop power control signal in response to the received signal;

combining the received power level signal and the closed loop power control signal to produce a summation signal;

comparing the summation signal to the maximum gain setting;

adjusting the variable gain amplifier in response to the maximum gain setting if the summation signal is greater than or equal to the maximum gain setting; and

adjusting the variable gain amplifier in response to the summation signal if the summation signal is less than the maximum gain setting.

3. The method of claim 2 further including the step of adjusting the maximum gain setting in response to a temperature of the variable gain amplifier.

4. A method for limiting transmit power of a radio operating in a cellular environment, the cellular environment comprising a plurality of cells that transmit power control commands to the radio, the radio comprising a variable gain amplifier, a maximum gain setting, and a power limiting accumulator, the method comprising the steps of:

receiving a signal from at least one of the plurality of cells;

generating a received power level signal in response to the received signal;

generating a closed loop power control signal in response to the received signal;

digitizing the received power level signal;

comparing the digitized received power level signal to the maximum gain setting;

decreasing the gain of the variable gain amplifier if the digitized received power level signal is greater than the maximum gain setting; and

prohibiting the closed loop power control signal from changing in response to the power control commands if the digitized received power level signal is greater than the maximum gain setting.

5. A method of limiting transmit power of a radio operating in a cellular environment, the cellular environment comprising a plurality of cells that transmit power control commands to the radio, the radio comprising a variable gain amplifier, a maximum gain setting, and a power control command accumulator, the method comprising the steps of:

receiving a signal from at least one of the plurality of cells;

generating a received power level signal in response to the received signal;

generating a closed loop power control signal in response to the power control commands;

digitizing the received power level signal;

comparing the digitized received power level signal to the maximum gain setting;

decreasing the closed loop power control signal by a predetermined amount for every predetermined unit of time until the closed loop power control signal is less than the maximum gain setting if the digitized received power level signal is greater than the maximum gain setting; and

varying the gain of the variable gain amplifier in response to the closed loop power control signal if the digitized received power level signal is less than or equal to the maximum gain setting.

6. A method for limiting transmit power of a radio operating in a cellular environment, the cellular environment comprising a plurality of cells that transmit power control commands to the radio, the radio comprising a variable gain amplifier, a maximum gain setting, and a power limiting accumulator, the method comprising the steps of:

receiving a signal from at least one of the plurality of cells;

generating a received power level signal in response to the received signal;

generating a closed loop power control signal in response to the power control commands;

digitizing the received power level signal;

determining a difference between the digitized received power level signal and the maximum gain setting;

integrating the difference to generate a gain control signal, the gain control signal being limited to a predetermined range;

adjusting the variable gain amplifier with the gain control signal; and

prohibiting the closed loop power control signal from changing the variable gain amplifier in response to the power control commands if the gain control signal is less than a predetermined value.

7. A radio performing transmit power calibration, operating in a cellular environment comprising a plurality of cells that transmit power control commands to the radio, the radio receiving signals through a variable gain receive amplifier the radio comprising:

a receive power detector, coupled to the receive amplifier, for generating a received power level signal;

a saturating accumulator coupled to the receive amplifier, for generating a closed loop power control signal in response to the power control commands;

a power limiting circuit, coupled to the receive power detector and the saturating accumulator, for generating a limiting gain control setting in response to the closed loop power control signal and the received power level signal, the limiting gain control setting being within a predetermined range;

a signal combiner, coupled to the receive power detector, the saturating accumulator and the power limiting circuit, for combining the received power level signal, the closed loop power control signal, and the limiting gain control setting to generate a transmit gain control signal; and

a transmit amplifier having a variable gain and a control input coupled to the signal combiner, the variable gain

Ex. H-14

Ex. G-14

adjusting in response to the transmit gain control signal.

8. The radio of claim 7 wherein the power limiting circuit further comprises:

a summer for combining the received power level signal and the closed loop power control signal to produce a summation signal; and

a comparator coupled to the summer for comparing the summation signal to a maximum gain setting to generate the limiting gain control setting.

9. The radio of claim 7 wherein the power limiting circuit further comprises:

an analog to digital converter for digitizing the received power level signal; and

an integrator, coupled to the analog to digital converter, for integrating a difference between the received power level signal and a maximum gain setting to generate the limiting gain control setting.

* * * * *

Ex. H-15

Ex. G-15

US006615027B1

(12) United States Patent
Sahota et al.

(10) Patent No.: US 6,615,027 B1
(45) Date of Patent: Sep. 2, 2003

(54) METHOD AND CIRCUIT FOR PROVIDING INTERFACE SIGNALS BETWEEN INTEGRATED CIRCUITS

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(73) Assignee: Qualcomm Incorporated, San Diego, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/489,231

(22) Filed: Jan. 21, 2000

(51) Int. Cl.[7] H04B 1/02

(52) U.S. Cl. 455/91; 455/93; 341/126; 341/135; 341/144

(58) Field of Search 455/91, 93, 95, 455/575; 379/399.01; 341/154, 155, 144, 135, 126

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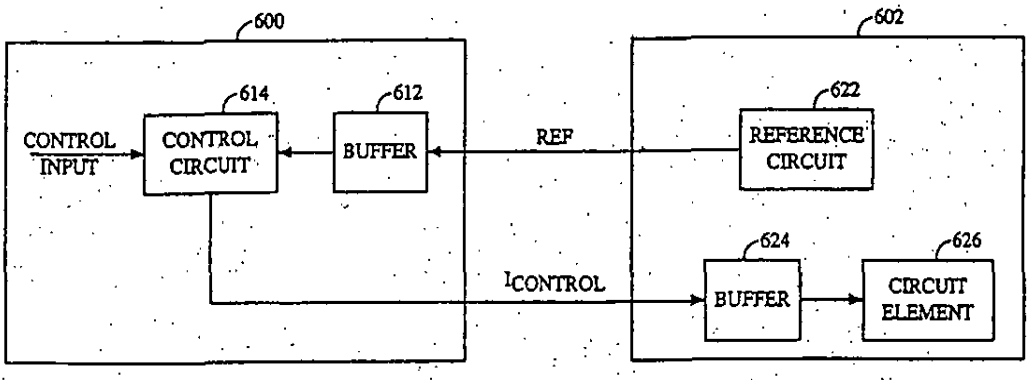
(57) ABSTRACT

Circuitry that generates an interface signal between a first and a second integrated circuit (IC). The circuitry includes a reference circuit that provides a reference signal, an interface circuit, and a circuit element. The interface circuit is implemented on the first IC, operatively couples to the reference circuit, receives the reference signal and a data input, and generates the interface signal. The circuit element is implemented on the second IC, operatively couples to the control circuit, receives the interface signal, and provides an output signal. The reference signal can be a voltage or a current signal, and can be generated in the first or second IC. The interface circuit can be implemented with a current mirror coupled to a switch array, and can be oversampled to ease the filtering requirement. The interface signal can be a differential current signal having multiple (e.g., four, eight, or more) bits of resolution. The circuit element can be, for example, a VGA, a modulator, or other circuits.

85 Claims, 6 Drawing Sheets



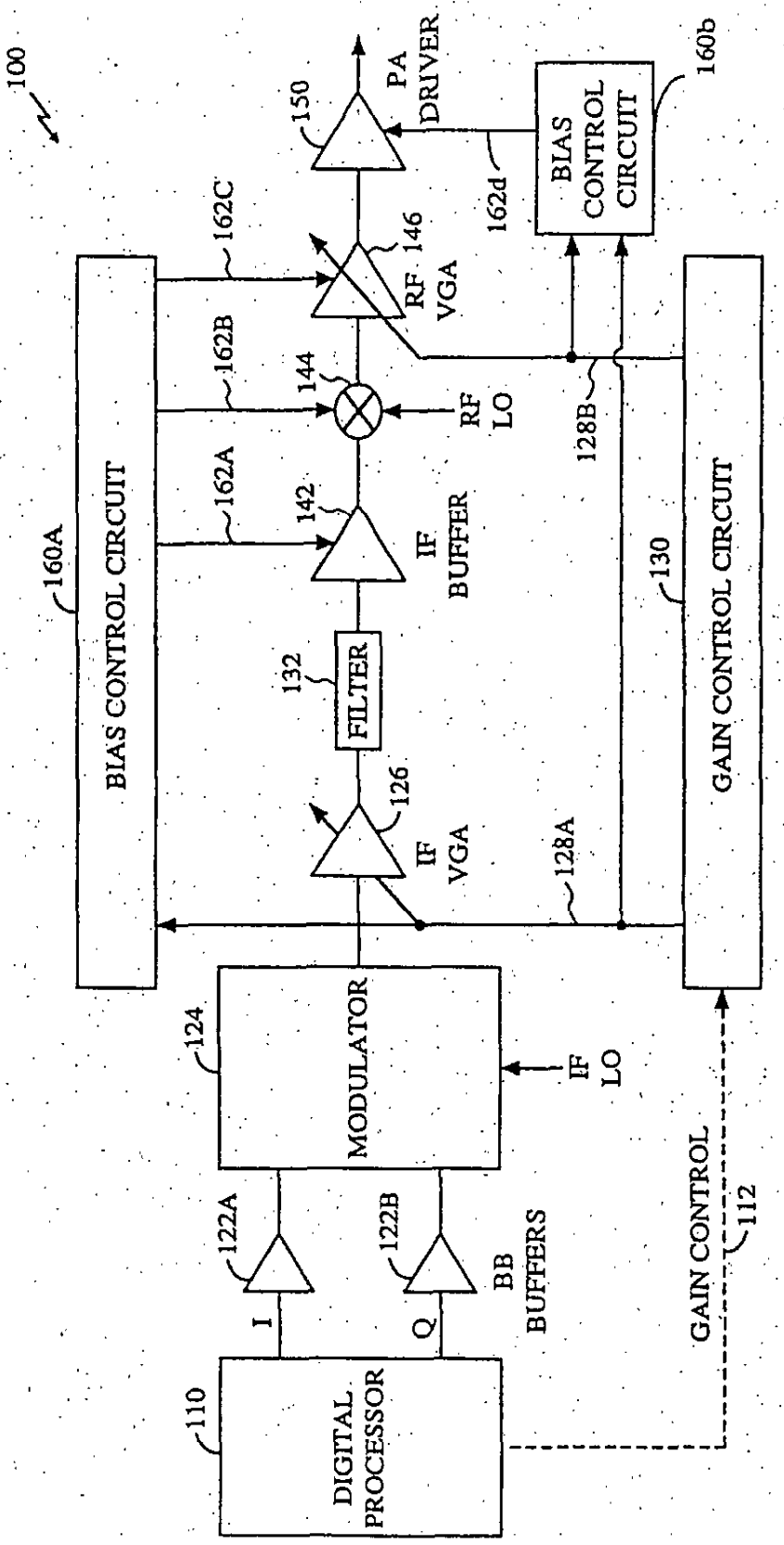

100
PA DRIVER
150
BIAS CONTROL CIRCUIT
160b
162d
162C
RF VGA
146
162B
144
RF LO
128B
BIAS CONTROL CIRCUIT
160A
162A
142
IF BUFFER
130
GAIN CONTROL CIRCUIT
132
FILTER
126
IF VGA
128A
MODULATOR
124
IF LO
122A
122B
BB BUFFERS
I
Q
GAIN CONTROL
112
DIGITAL PROCESSOR
110

FIG. 1

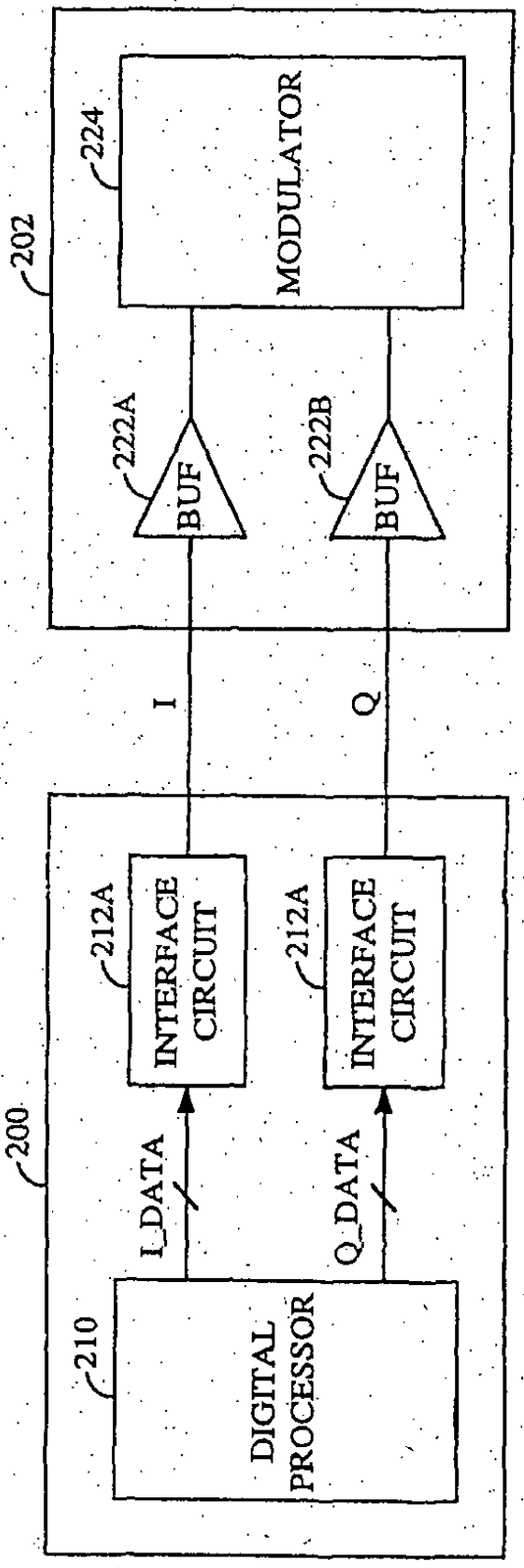

202
224
MODULATOR
222A
BUF
222B
BUF
I
Q
212A
INTERFACE CIRCUIT
212A
INTERFACE CIRCUIT
200
I_DATA
Q_DATA
210
DIGITAL PROCESSOR

FIG. 2

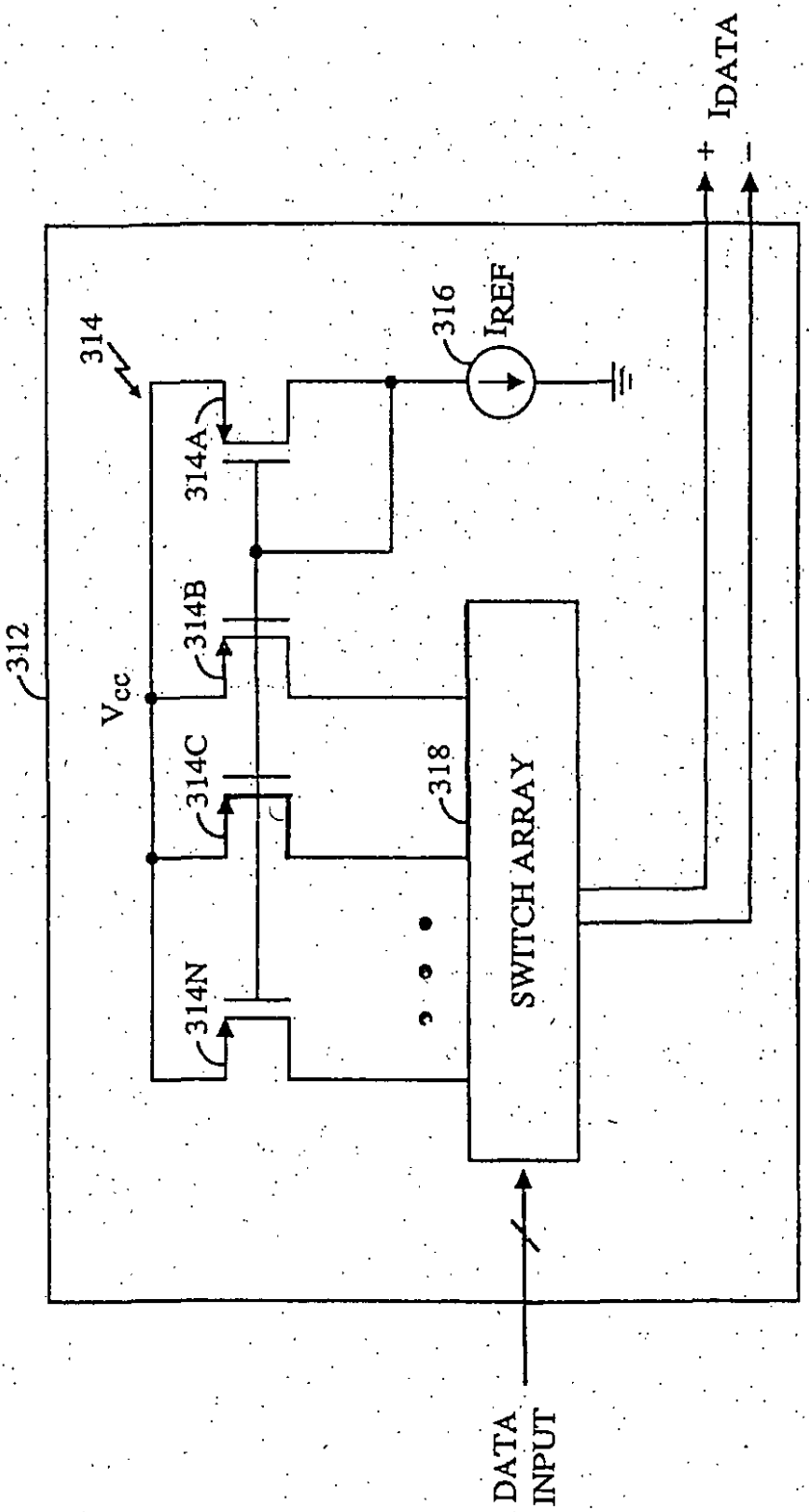

IDATA
+
−
316
IREF
314
314A
314B
312
Vcc
314C
318
SWITCH ARRAY
314N
DATA
INPUT

FIG. 3

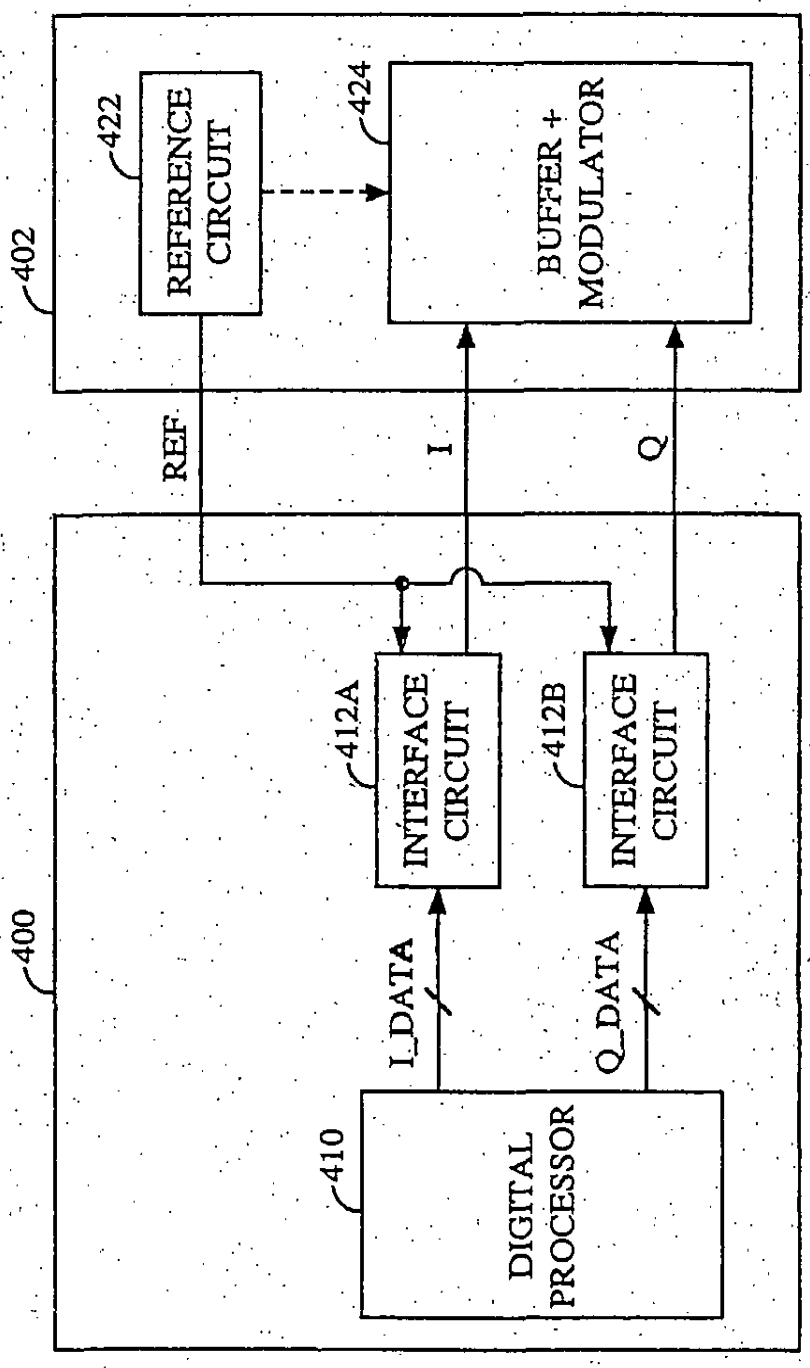

402
422
REFERENCE CIRCUIT
424
BUFFER + MODULATOR
REF
I
Q
400
412A
INTERFACE CIRCUIT
412B
INTERFACE CIRCUIT
I_DATA
Q_DATA
410
DIGITAL PROCESSOR

FIG. 4

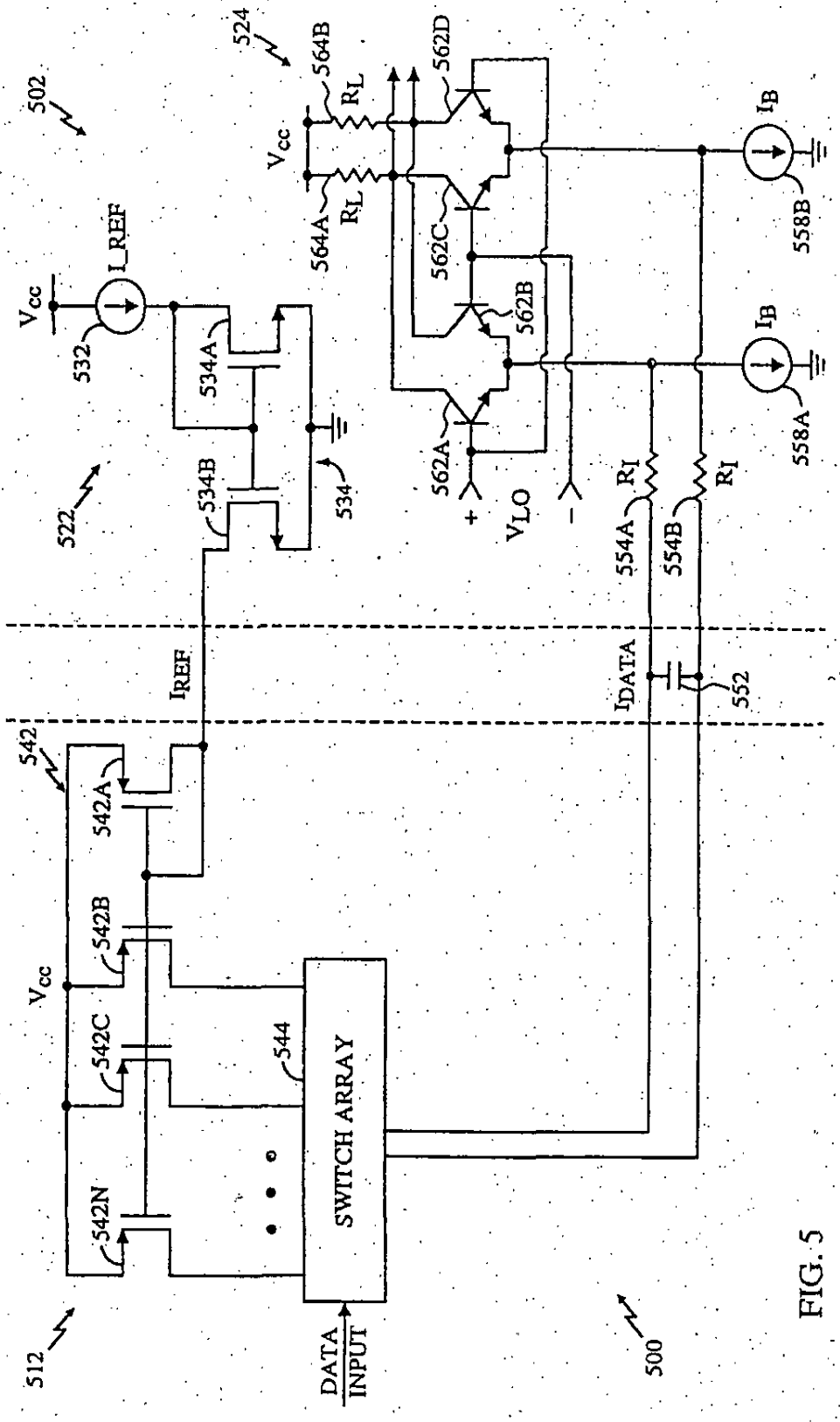

524
564B
R_L
562D
V_{cc}
502
I_B
564A
R_L
562C
558B
V_{cc}
I_REF
562B
I_B
532
534A
558A
562A
534B
534
V_{LO}
554A
R_I
R_I
554B
522
I_{REF}
I_{DATA}
552
542
542A
542B
V_{cc}
542C
544
SWITCH ARRAY
542N
DATA INPUT
512
500

FIG. 5

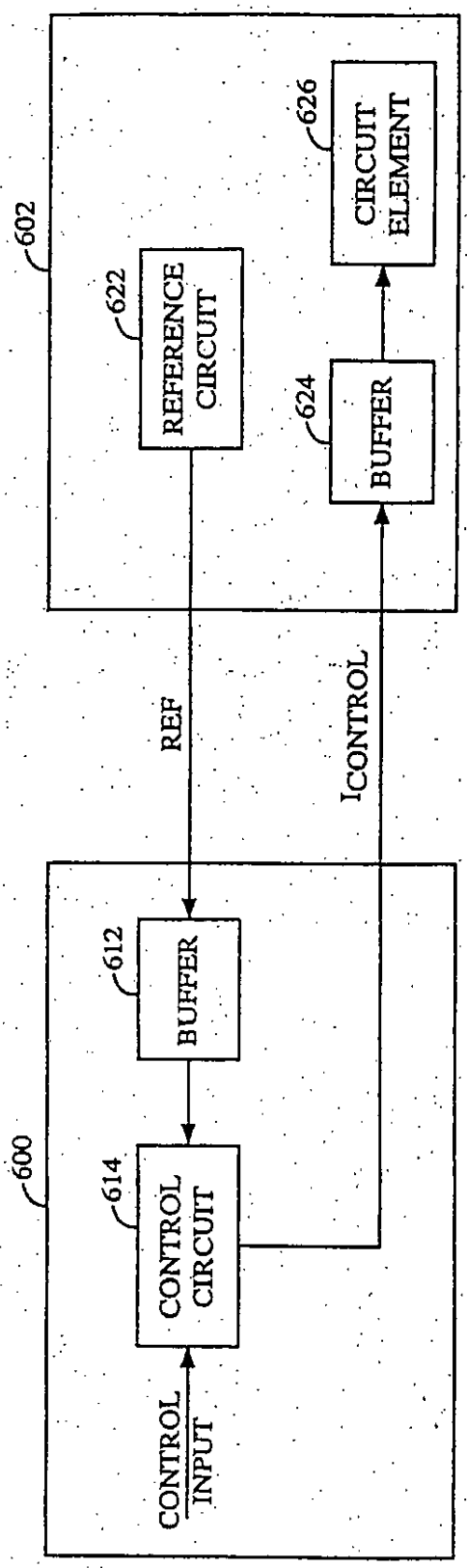

602
626
CIRCUIT ELEMENT
622
REFERENCE CIRCUIT
624
BUFFER
REF
ICONTROL
612
BUFFER
600
614
CONTROL CIRCUIT
CONTROL INPUT

FIG. 6

METHOD AND CIRCUIT FOR PROVIDING INTERFACE SIGNALS BETWEEN INTEGRATED CIRCUITS

BACKGROUND OF THE INVENTION

I. Field of the Invention

The present invention relates to electronics circuits. More particularly, the present invention relates to novel and improved method and circuit for providing interface signals between integrated circuits.

II. Description of the Related Art

Many electronics systems are implemented using multiple integrated circuits (ICs) that interface together to provide the required system functionality. In many instances, circuit interfaces are provided by digital signals having two logic levels (e.g., high and low) to express digital values. Digital signals are popular for interface because of their ease of implementation and robust immunity to noise.

Special challenges arise when interfacing a digital IC with an analog IC. Digital ICs are more efficient and cost effective for implementing digital functions such as digital signal processing and the like. Analog ICs are used to provide linear functions such as signal amplification, buffering, filtering, modulation, mixing, and so on. In many designs, the interface between the digital and analog ICs is implemented using digital signals. Within the analog IC, the digital signals are buffered, converted to analog signal(s) if necessary, and provided to the analog circuit(s).

The use of digital signals to interface digital and analog ICs is undesirable in some applications for several reasons. First, digital signals typically have large signal swing and sharp transition edges, thereby generating large switching noise. This noise can degrade the performance of the analog circuits, which typically operate on smaller signal swing. The amount of noise can be reduced, to an extent, by using separate power supplies and circuit grounds for analog and digital circuits within the analog IC. However, the reduction may not be adequate for some applications. Second, because each digital signal typically provides one bit of data, multiple (e.g., eight) digital signals are necessary to concurrently provide multiple (e.g., eight) bits of data. In addition, one or more clock signals [may also be] are typically provided to latch the data bits at the receiving IC. A large number of signal lines, and a corresponding number of device pins, may thus be required to interface the ICs. Moreover, switching noise typically increases with more digital signal lines.

Accordingly, techniques for providing an improved interface between ICs using fewer signal lines that generate a reduced amount of noise are highly desirable. It is also desirable that the interface does not require complex circuitry to implement.

SUMMARY OF THE INVENTION

The present invention provides techniques to interface a digital IC and an analog IC. In accordance with one aspect of the invention, one or more interface circuits implemented on the digital IC receive data inputs and, in response, provide interface signals that are provided to the analog IC. For some interfaces (e.g., baseband signals), differential current signals having multiple bits of resolution are used. These signals require fewer signal lines to implement and generate a reduced amount of noise, as compared to digital signals. A reference signal can be provided for use in generating the interface signals.

An embodiment of the invention provides circuitry to generate an interface signal between a first and a second integrated circuit. The circuitry includes a reference circuit, an interface circuit, and a circuit element. The reference circuit provides a reference signal. The interface circuit is implemented on the first integrated circuit, operatively couples to the reference circuit, receives the reference signal and a data input, and generates the interface signal. The circuit element is implemented on the second integrated circuit, operatively couples to the control circuit, receives the interface signal, and provides an output signal.

In an embodiment, the interface circuit includes a current mirror coupled to a switch array. The current mirror receives the reference signal and includes two or more mirror paths. The switch array receives and decodes the data input and directs current from a selected set of mirror paths to an output of the switch array.

The reference signal can be a voltage signal or a current signal (i.e., generated based on a voltage reference), and can be generated with a reference circuit implemented on the first or (preferably for some applications) the second integrated circuit. In an embodiment, the interface signal is a differential current signal having multiple (e.g., four, eight, or more) bits of resolution and filtered with a RC network. The interface circuit may be oversampled to ease the filtering requirement. In an exemplary embodiment, the interface signal represents an inphase (I) or a quadrature (Q) baseband signal in a quadrature transmitter, or a control signal. The circuit element can be, for example, a VGA, a modulator, or other circuits.

Another embodiment of the invention provides circuitry in a transmitter that include a first interface circuit (and for some embodiments, a second interface circuit) operatively coupled to a modulator. The first (and second) interface circuit is implemented on a first integrated circuit, receives a first (or second) data input, and provides a first (or second) differential current signal. The modulator is implemented on a second integrated circuit, receives the first (and second) differential current signal and a carrier signal, and generates an output signal in response. Each data input represents a digital baseband signal and can have four, eight, or more bits of resolution. A reference circuit may be implemented on the second (or possibly first) integrated circuit to provide a reference signal. The interface circuits generate the differential current signals based, in part, on the reference signal.

Yet another embodiment of the invention provides a transmitter in a (e.g., CDMA) cellular telephone that includes a digital processor, first and second interface circuits, and a modulator. The digital processor is implemented on a first integrated circuit and provides the digital inphase (I) and quadrature (Q) baseband signals. The first and second interface circuits are implemented on the first integrated circuit and couple to the digital processor. Each interface circuit receives a respective digital baseband signal and provides an analog baseband signal. Each analog baseband signal has at least four bits of resolution and is implemented as a differential current signal. The modulator is implemented on a second integrated circuit, operatively couples to the first and second interface circuits, and receives and modulates the analog baseband signals with a carrier signal to provide a modulated output signal. The transmitter can also include a reference circuit that provides a reference signal. The interface circuits then receive the reference signal and generate the analog baseband signals based, in part, on the reference signal.

Yet another embodiment of the invention provides a method for providing an interface signal from a first to a

second integrated circuit. In accordance with the method, a reference signal is generated at either the first or second integrated circuit and provided to the first integrated circuit. A data input is also received in the first integrated circuit and is used in conjunction with the reference signal to generate the interface signal. The interface signal is then provided from the first to the second integrated circuit. A circuit element in the second integrated circuit receives the interface signal and generates an output signal in response. The circuit element can also receive a signal related to the reference signal, and can generate the output signal based, in part, on this received signal.

BRIEF DESCRIPTION OF THE DRAWINGS

The features, nature, and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters identify correspondingly throughout and wherein:

FIG. 1 shows a simplified block diagram of an embodiment of a quadrature transmitter;

FIG. 2 shows a block diagram of an embodiment of an interface between a digital IC and an analog IC for the I and Q baseband signals;

FIG. 3 shows a schematic diagram of an embodiment of an interface circuit;

FIG. 4 shows a block diagram of an other embodiment of an interface between a digital IC and an analog IC for the I and Q baseband signals;

FIG. 5 shows a schematic diagram of a specific embodiment of the interface and circuitry shown in FIG. 4; and

FIG. 6 shows a block diagram of an embodiment of circuits used to generate a control signal in accordance with the invention.

DETAILED DESCRIPTION OF THE SPECIFIC EMBODIMENTS

The invention can be implemented in various electronics circuits and systems. For clarity, the invention is described for a specific implementation in a transmitter of a cellular communications system.

FIG. 1 shows a simplified block diagram of an embodiment of a quadrature transmitter 100. A digital processor 110 generates data, encodes the data, and converts the digitally processed data into inphase (I) and quadrature (Q) baseband signals. The baseband signals are provided to baseband (BB) buffers 122a and 122b that buffer the signals and provide the buffered signals to a modulator 124. Modulator 124 also receives a signal (e.g., a carrier sinusoid) at an intermediate frequency (IF LO), and modulates the buffered baseband signals with the IF LO to generate an IF modulated signal. Modulator 124 can be a single sideband or a double sideband modulator. For a single sideband modulator, one or more phase shifters may be used to generate IF LOs having the proper phases. The IF signal is provided to an IF variable gain amplifier (IF VGA) 126 that amplifies the signal with a gain determined by a gain control signal 128a from a gain control circuit 130. The amplified IF signal is provided to a filter 132 that filters the IF signal to remove out-of-band noise and undesired signals.

The filtered IF signal is provided to an IF buffer 142 that buffers the signal and provides the buffered IF signal to a mixer 144. Mixer 144 also receives a signal (e.g., a carrier sinusoid) at a radio frequency (RF LO), and upconverts the buffered IF signal with the RF LO to generate a RF signal. Mixer 144 can also be a single sideband or double sideband mixer. The single sideband mixer embodiment may have phase shifters in both the IF and RF LO paths. The RF signal is provided to a RF VGA 146 that amplifies the signal with a gain determined by a gain control signal 128b from gain control circuit 130. The amplified RF signal is provided to a power amplifier (PA) driver 150 that further interfaces with other circuitry such as an external filter (i.e., for filtering out images and spurious signals) and a power amplifier (both elements not shown in FIG. 1). The PA driver provides the required signal drive, and its output couples to an antenna via an isolator and a duplexer (these elements are not shown in FIG. 1).

Various modifications can be made to the transmitter embodiment shown in FIG. 1. For example, fewer or additional filter, buffer, and amplifier stages can be provided in the transmit signal path. Some of the components shown in FIG. may not be used in some embodiments. Moreover, the elements within the signal path can be arranged in different order. In addition, the variable gain in the transmit signal path can be provided by VGAs (as shown in FIG. 1), variable attenuators, multipliers, other variable gain elements, or a combination of the above. Also, a direct upconversion can be used in which the baseband signals are directly upconverted to RF.

Transmitter 100 can be used in many communications applications, such as cellular communications systems. Examples of cellular communications systems include Code Division Multiple Access (CDMA) communications systems, Time Division Multiple Access (TDMA) communications systems, and analog FM communications systems. The use of CDMA techniques in a multiple access communications system is disclosed in U.S. Pat. No. 4,901,307, entitled "Spread Spectrum Multiple Access Communication System Using Satellite or Terrestrial Repeaters," and U.S. Pat. No. 5,103,459, entitled "System and Method for Generating Waveforms in a CDMA Cellular Telephone System," both patents assigned to the assignee of the present invention and incorporated herein by reference. CDMA systems are typically designed to conform to the "TIA/EIA/IS-95-A Mobile Station-Base Station Compatibility Standard for Dual-Mode Wideband Spread Spectrum Cellular System," hereinafter referred to as the IS-95-A standard, which is also incorporated herein by reference.

As shown in FIG. 1, the bias currents for some of the elements in the transmit signal path can be adjusted based on the gain control signals generated by gain control circuit 130. For example, the bias currents of IF buffer 142, mixer 144, and RF VGA 146 can each be adjusted by a bias control circuit 160a via bias control signals 162a, 162b, and 162c, respectively, which are generated based on the value of gain control signal 128a. Similarly, the bias current of PA driver 150 can be adjusted by a bias control circuit 160b via a bias control signal 162d that is generated based on gain control signal 128a or 128b, or both. Gain control signals 128a and 128b may be generated based on a gain control signal 112 that may come from digital processor 110 (as shown by the dashed line in FIG. 1) or another control source.

In an embodiment, the transmit signal path from BB buffers 122 to PA driver 150 (possibly excluding filter 132) is implemented within one or more (e.g., analog) integrated circuits. In an embodiment, the digital processor is implemented on another (e.g., digital) integrated circuit. The gain and bias control circuits can be implemented on the same integrated circuit as the digital processor, on the integrated circuit(s) used to implement the transmit signal path, or on a separate integrated circuit. Thus, interface signals are

Ex. I-9

provided for the baseband signals from the digital processor and the (e.g., gain and bias) control signals from the control circuits.

In FIG. 1, the I and Q baseband signals may each comprise multiple bits of resolution. This can result from, for example, filtering a two-level digital signal with a digital filter. Thus, multiple signal lines may be required to interface the digital processor to the analog circuitry.

In one conventional design, each of the I and Q baseband signals has eight bits of resolution, and the interface comprises eight data lines and two clocks lines. The data lines are time shared between the I and Q signals. The clock lines provide two clock signals that are (e.g., 180 degrees) out-of-phase with respect to each other. The data lines are used to provide the I signal on one phase of the clock and the Q signal on the other phase of the clock. In this design, the data and clock lines generate noise that can degrade the performance of the analog circuits in the transmit signal path. Moreover, the (ten) data and clock lines require a corresponding number of (ten) device pins on both the digital and analog ICs.

FIG. 2 shows a block diagram of an embodiment of an interface between a digital IC 200 and an analog IC 202 for the I and Q baseband signals. As shown in FIG. 2, a digital processor 210 within IC 200 provides the I and Q data to interface circuits 212*a* and 212*b*, respectively. In an embodiment, each of the I and Q data comprises multiple bits of data. Each interface circuit 212 receives the respective data input, converts the data to an analog baseband signal, and provides the analog baseband signal to IC 202. Within IC 202, the I and Q baseband signals are provided to buffers 222*a* and 222*b*, respectively, and the buffered signals are provided to a modulator 224.

FIG. 3 shows a schematic diagram of an embodiment of an interface circuit 312. One interface circuit 312 can be used to implement each of interface circuits 212*a* and 212*b* in FIG. 2. In this embodiment, interface circuit 312 includes a set of P-channel transistors 314*a* through 314*n* configured as a current mirror 314. The gates of transistors 314*a* through 314*n* couple together and the sources also couple together and to a power supply V_{CC}. The drain of transistor 314*a* couples to the gate of transistor 314*a* and to a current source 316 that provides a reference current I_{REF}. Each of transistors 314*b* through 314*n* is configured to provide a particular "mirror" current that is proportional to the reference current I_{REF}. The proportionality (or scaling) factor for a particular mirror path is dependent on the ratio of the size of the transistor in that path to the size of transistor 314*a*. For example, if transistor 314*b* is twice the size of transistor 314*a*, then the amount of current through transistor 314*b* is approximately twice the reference current I_{REF}.

A switch array 318 couples to transistors 314*b* through 314*n*. Switch array 318 also receives and decodes the data input and activates a set of switches within the array that selectively steer the current from transistors 314*b* through 314*n* to the output of the array. The data input can be the I data or the Q data shown in FIG. 2. In an embodiment, switch array 318 includes circuitry that generates a differential current signal I_{DATA} as the output of interface circuit 312.

The use of interface circuits 312 to provide the I and Q baseband signals to the analog IC provides many advantages. Some of these advantages are described below.

First, only two sets of different signal lines (i.e., four lines in all) are required to provide the differential current signals for the I and Q baseband signals. In contrast, eight digital data lines and two clock lines are required by one conventional design. Fewer number of signal lines reduces the number of device pins required to interface the ICs.

Second, the differential current signal I_{DATA} generally has low impedance and limited (or reduced) signal swing. In contrast, the digital signals of the aforementioned conventional design have large signal swing and sharp transition edges. The differential current signals thus generate much less noise than the digital signals.

Third, the differential current signals can reduce circuit complexity at the source and destination ICs. For improved performance (e.g., wide bandwidth, linearity, and so on) many high-speed analog circuits are designed to operate on different current signals. By providing a differential current signal to the analog IC (i.e., as opposed to voltage signals or digital signals), buffering and voltage-to-current conversion circuitry may not be required within the analog IC, thus simplifying its design.

For a CDMA system that conforms to IS-95-A specifications, each of the I and Q data has a bit rate of 1.2288 Mbps. In an embodiment, the I and Q data are oversampled and filtered (e.g., within the digital processor) to provide filtered I and Q data, respectively. It is known that generation of an analog signal from sampled data produces images at the sample rate. By oversampling the I and Q data (e.g., by a factor of 16), the images are pushed higher in frequency by the oversampling factor (which is 16 in this example) and the filtering of the images is simplified. With oversampling, the images can be filtered by a simple RC network, as described below.

For many integrated circuits, variations in the manufacturing process make it difficult to generate accurate component values (e.g., accurate resistor and capacitor values). However, component matching is typically quite good since the entire IC typically experiences similar process conditions. Thus, while it may be challenging to fabricate a resistor having a value that is accurate to within ±30 percent of a targeted value, it is often feasible to match two resistors to within a few percent.

Even with the manufacturing process variations, circuits within the analog IC are required to perform to specifications. To provide consistent performance from IC to IC, the circuits can be designed to operate in conjunction with a reference signal (or a reference value) that can be accurately generated on the IC. For electronic circuits, a bandgap reference circuit can be designed to provide a (relatively) accurate reference voltage (even over process variations). Moreover, the bandgap reference voltage is typically stable over time, power supply, and temperature variations. The bandgap reference voltage can be used to generate other reference voltages and currents used by various circuits within the IC.

FIG. 4 shows a block diagram of another embodiment of an interface between a digital IC 400 and an analog IC 402 for the I and Q baseband signals. As shown in FIG. 4, a digital processor 410 within IC 400 provides the I and Q data to interface circuits 412*a* and 412*b*, respectively. Each interface circuit 412 receives the respective data input and a reference signal REF from a reference circuit 422 within IC 402, converts the data to an analog signal (i.e., using, in part, the reference signal REF), and provides the analog signal to a buffer and modulator 424 within IC 402. A replica of, or a signal related to, the reference signal REF can also be provided from reference circuit 422 to buffer and modulator 424, as indicated by the dashed line.

The reference signal REF can generally be a reference voltage (e.g., a bandgap reference voltage) or a reference

current. By operating the interface circuit and the modulator based on a common reference signal, these circuits can be designed to track each other over process variations on their respective ICs, as described below.

FIG. 5 shows a schematic diagram of a specific embodiment of the interface and circuitry shown in FIG. 4. As shown in FIG. 5, a digital IC 500 includes an interface circuit 512 that couples to a reference circuit 522 and a modulator 524 within an analog IC 502. Reference circuit 522, interface circuit 512, and modulator 524 correspond to reference circuit 422, interface circuit 412, and modulator 424, respectively, in FIG. 4.

In an embodiment, reference circuit 522 includes a current source 532 coupled to a current mirror 534. In an embodiment, current source 532 provides a reference current I_REF generated by providing a bandgap reference voltage across a resistor. The resistor can be an external (i.e., discrete) resistor or an internal resistor fabricated on IC 502, with the choice being dependent on the desired circuit characteristics and functionality, as described below. The reference current I_REF is provided to the reference path (i.e., via a N-channel transistor 534*a*) of current mirror 534. The current through the mirror path (i.e., via a N-channel transistor 534*b*) comprises the reference current I_{REF} that is provided to IC 500. Generally, I_{REF} is proportional to I_REF, with the proportionality factor being determined by the ratio of the size of transistor 534*b* to the size of transistor 534*a*.

Within IC 500, the reference current I_{REF} is provided to interface circuit 512. In an embodiment, interface circuit 512 comprises a current mirror 542 coupled to a switch array 544. Specifically, the reference current I_{REF} is provided to a reference path (i.e., via a P-channel transistor 542*a*) of current mirror 542. Since the gate-source voltage of transistors 542*a* through 542*n* are approximately equal, the current through each mirrored path (i.e., via transistors 542*b* through 542*n*) is related to the current I_{REF} through the reference path (i.e., via transistor 542*a*). The proportionality factor is determined by the ratio of the size of the transistor in the particular mirror path to the size of transistor 542*a*. Transistors 542*b* through 542*n* can be dimensioned to provide approximately equal current through each mirror path (e.g., 1, 1, 1, and so on), exponentially increasing currents (e.g., 1, 2, 4, and so on), or other sets of current values.

Switch array 544 couples to transistors 542*b* through 542*n* and also receives the data input. Switch array 544 decodes the data input and, based on the decoded data, selectively steers current from the mirror paths to the output of the switch array. The current signal I_{DATA} from switch array 544 is provided to IC 502. In an embodiment and as shown in FIG. 5, the current output is provided as a differential current signal for improved noise immunity.

Interface circuit 512 performs in similar manner as a digital-to-analog converter (DAC). Thus, the reconstructed output from interface circuit 512 includes images at $n \cdot f_s$, where f_s is the sample frequency (i.e., the rate of the data input) and $n=1, 2, 3, \ldots$. Interface circuit 512 can be oversampled (e.g., by a factor of 2, 4, 8, 16, or other oversampling ratios) to push the images in the reconstructed signal to higher frequencies for ease of filtering.

As shown in FIG. 5, the current signal I_{DATA} is filtered by a RC network to remove undesired noise and images normally associated with an output from a digital to analog conversion. Specifically, a capacitor 552 is coupled between the differential current signal I that further couples to one end of resistors 554*a* and 554*b*. Capacitor 552 and resistors 554 can be external (i.e., discrete) components or internal components implemented within the ICs (i.e., IC 500 or 502, or both). In an embodiment, capacitor 552 is an external component (i.e., having a value that is larger than that which can be practically implemented within an IC) and resistors 554 are internal components implemented within IC 502.

The other ends of resistors 554*a* and 554*b* couple to current sources 558*a* and 558*b*, respectively, of modulator 524. In an embodiment, each current source 558 provides a bias current I_B that is related to the reference current I_REF, as described below. Modulator 524 further includes a pair of differential amplifiers. The first differential amplifier comprises transistors 562*a* and 562*b* having their emitters coupled together and to current source 558*a*. The second differential amplifier comprises transistors 562*c* and 562*d* having their emitters coupled together and to current source 558*b*. The bases of transistors 562*a* and 562*d* couple together and receive a positive carrier signal $V_{LO}+$, and the bases of transistors 562*b* and 562*c* couple together and receive a negative carrier signal $V_{LO}-$. The collectors of transistors 562*a* and 562*c* couple together and to a resistor 564*a* that further couples to the supply voltage V_{CC}. The collectors of transistors 562*b* and 562*d* couple together and to a resistor 564*b* that also couples to the supply voltage V_{CC}. The differential voltages at resistors 564*a* and 564*b* form the output voltage signal V_{OUT} from modulator 524.

In an embodiment, the reference current I_REF is dependent on a bandgap reference voltage from a bandgap reference circuit (not shown in FIG. 5). In an embodiment, the bandgap voltage reference is provided across an external resistor (i.e., a discrete resistor external to IC 502) to generate the reference current I_REF, which can be expressed as:

$$I\_REF = \frac{V_{REF}}{R_{REF}}, \qquad \text{Eq. (1)}$$

where V_{REF} is the bandgap reference voltage and R_{REF} is the value of the external reference resistor. The use of an external resistor enables the generation of an accurate reference current I_REF, since discrete resistors with 1.0 (or 0.1) percent tolerance are readily available. The reference current I_{REF} is proportional to the reference current I_REF, as determined by the particular design of current mirror 534, and can be expressed as:

$$I_{REF} = \alpha_1 \cdot I\_REF = \alpha_1 \cdot \frac{V_{REF}}{R_{REF}}, \qquad \text{Eq. (2)}$$

where α_1 is the scaling factor associated with current mirror 534.

Interface circuit 512 generates the differential current signal I_{DATA}, which is a scaled version of the reference current I_{REF}. The scaling factor is determined by the data input and the particular design of current mirror 542 (i.e., the sizes of transistors 542*a* through 542*n*). Specifically, the ratio in sizes of each of transistors 542*b* through 542*n* to transistor 542*a* determines the amount of current to be switched for each current path. The data input determines which ones of the switches within switch array 544 are activated and thus the current path(s) to be directed to the switch array output. The current signal I_{DATA} can theoretically be expressed as:

$$I_{DATA}(t) = \frac{\alpha_1 \alpha_2}{2^N} \cdot \frac{V_{REF}}{R_{REF}} \cdot \sum_{n=0}^{\infty} x(n) \cdot h(t - nT) = K \cdot s(t), \quad \text{Eq. (3)}$$

where x[n] is the value of the data input, h(t) is the zero order hold response of the DAC, N is the number of bits for the data input, α_2 is the scaling factor associated with current mirror 542,

$$K = \frac{\alpha_1 \alpha_2}{2^N} \cdot \frac{V_{REF}}{R_{REF}}, \text{ and} \quad \text{Eq. (4)}$$

$$s(t) = \sum_{n=0}^{\infty} x(n) \cdot h(t - nT). \quad \text{Eq. (5)}$$

For an eight bit data input, x[n] ranges from 0 to 255 and 2^N is equal to 256.

Modulator 524 generates the voltage signal V_{OUT} based on the current signal I_{DATA}, the carrier signal V_{LO}, the load resistor R_L, and a modulator gain or conversion factor β. The voltage signal V_{OUT} can be expressed as:

$$V_{OUT}(t) = \beta \cdot 2R_L \cdot I_{DATA}(t) = \beta \cdot 2R_L \cdot K \cdot s(t). \quad \text{Eq. (6)}$$

By lumping the constants together, equation (6) can be expressed as:

$$V_{OUT}(t) = A \cdot R_L \cdot s(t). \quad \text{Eq. (7)}$$

It can be noted from equation (7) that the voltage signal V_{OUT} is a function of the ratio of R_L to R_{REF}, the data input x[n], the bandgap voltage reference V_{REF}, and a scaling factor A that takes into account various factors. The scaling factor A includes the scaling factors α and α associated with current mirrors 534 and 542, respectively. These scaling factors can be accurately set because they are based on the ratios of the sizes of transistors, which can be matched (typically to within a few percents) by exercising good circuit layout techniques. Typically, the bandgap reference voltage V_{REF} and the external reference resistor R_{REF} can also be accurately set.

As noted above, the value of internal resistor R_L cannot typically be set with a high degree of accuracy, and can vary by 30 percents or more from IC to IC due to process variations. Thus, the voltage signal V_{OUT} can vary widely from IC to IC. However, the voltage signal V_{OUT} is typically converted to a current signal I_{OUT} for use by a subsequent circuit, and the V-to-I conversion is achieved by providing V_{OUT} across another internal resistor R_1. The current signal I_{OUT} can be expressed as:

$$I_{OUT}(t) = \frac{V_{out}(t)}{R_1} = A \cdot \frac{R_L}{R_1} \cdot s(t). \quad \text{Eq. (8)}$$

From equation (8), it can be noted that the current signal I_{OUT}, is a function of the ratio of internal resistors R_L to R_1, which can typically be set to an accuracy of within one percent by following good circuit layout guidelines.

For implementations in which the voltage signal V_{OUT} is used directly (i.e., without a V-to-I conversion), an accurate V_{OUT} over process variations can be generated by using an internal reference resistor R_{REF}. Referring to equation (7), the voltage signal V_{OUT} is dependent on the ratio of resistors R_L to R_{REF}, which can be accurately set to within a few percent if both resistors are internally implemented on the same IC.

Thus, the reference resistor R_{REF} can be internal or external, depending on the desired characteristics of the circuit. The voltage signal V_{OUT} or the current signal I_{OUT} can be designed to be dependent mostly on factors that can be accurately set and which is, to a large extent, indifferent to process variations. To generate a voltage signal V_{OUT} that is accurate over process variations an external reference resistor is used, and to generate a current signal I_{OUT} that is accurate over process variations an internal reference resistor is used.

In the specific embodiment of modulator 524 in FIG. 5, current source 558a provides the current "sink" for the differential mixer (comprised of transistors 562a and 562b) and the current signal I_{DATA} via resistor 554a. As noted above, the current signal I_{DATA} is related to the reference current I_{REF}. If the current signal I_{DATA} increases because of an increase in the reference current I_{REF}, then the amount of current through the differential mixer decreases correspondingly if the bias current I_B is fixed, resulting in the mixer cutting off on positive I_{DATA} excursions. The performance (e.g., bandwidth, linearity, and so on) of the differential mixer can degrade due to the smaller bias current.

In an embodiment, to reduce performance degradation due to changes in the reference current I_{REF}, the bias current I_B is designed to be proportional to the reference current I_{REF} (e.g., $I_B = 2I_{REF}$, or some other values). This can be achieved through the use of a current mirror, with the reference current I_{REF} being provided to the reference path of the current mirror and the bias current I_B being provided from the mirror path.

The specific embodiment shown in FIG. 5 provides many advantages. First, only five signal lines are required to provide interface for the I and Q baseband signals (i.e., four lines for the I and Q signals and one for the reference signal). Thus, fewer number of device pins is required to interface the ICs than for the conventional design that uses ten signal lines. Fewer device pins result in a smaller package, thus reducing the size. Second, the differential current signal I_{DATA} drives a low impedance resulting in reduced signal swings at the interface, thus resulting in less noise being generated by this signal. The low impedance also reduces interference. Third, the differential current signal can reduce circuit complexity in the digital and analog ICs. As shown in FIG. 5, interface circuit 512 (by its nature) generates a current signal that can be provided directly, without a signal conversion, to the analog IC. Modulator 524 receives and can directly operate on the differential current signal. Thus, I-to-V and V-to-I conversion circuits are avoided by providing current interfaces. Fourth, the sharing of the reference signal I_{REF} between the digital and analog ICs allows for tracking between the two ICs. As shown in FIG. 5, the current signal I_{DATA} from interface circuit 512 is dependent on the reference current I_{REF}. The bias current I_B can also be designed to track the reference current I_{REF}, as described above, thus allowing the modulator to track the interface circuit. This interface can also allow the current to be shared between the DAC and the mixer, if I_{DATA} is generated from an (NMOS) current source.

Various modifications can be made to the specific embodiment shown in FIG. 5. For example, reference circuit 522 can be implemented in digital IC 500, in which case the reference signal I_{REF} is provided from IC 500 to IC 502. Implementation of the reference circuit in a digital IC is typically more challenging because of the large amounts of switching noise on the digital IC, although this is feasible and may be advantageous for some applications.

Reference circuit 522 can also be designed as a programmable reference source. For example, current source 532 can

comprise a DAC that provides different reference currents depending on the value of a control input. The use of a programmable reference source is particularly advantageous, for example, to allow for adjustment of circuit characteristics (e.g., output signal level, to account for process variations), or to vary the input signal level to provide variable gain.

The invention has been described for the interface of the I and Q baseband signals from the digital IC to the analog IC. The invention can also be used for control signals such as the bias and gain control signals shown in FIG. 1. The bias current and gain of the circuit elements in the transmit signal path are typically controlled, if at all, in increments. For example, the IS-95-A standard requires adjustment of the transmitter output power level in 0.5 dB increments. A multi-level control signal is typically used to provide gain adjustment in 0.5 dB increments, as required by IS-95-A specifications.

As with the baseband signals, a multi-level control signal can be provided by using multiple digital signal lines. However, this is generally not desired because of the large number of required device pins, large amounts of generated noise, and other reasons. An analog control signal generates less noise and can provide multiple levels of control using fewer device pins.

The gain of a gain element (e.g., a VGA) is dependent on various factors such as the design of the gain element, the component values, the characteristics of the active devices, and others. Many of these factors are dependent on the process used to manufacture the IC, and process variations typically cause component values to differ widely. For example, resistor values can vary by 30 percent or more from IC to IC. Similarly, the beta of transistors can vary by a factor of two from one IC to the next. To provide a level of tracking between the control circuit and the element to be controlled, a reference signal can be provided and shared by the circuits.

FIG. 6 shows a block diagram of an embodiment of circuits used to generate a control signal in accordance with the invention. The control circuit is implemented on an IC 600 and the circuit element to be controlled is implemented on an IC 602. IC 602 includes a reference circuit 622 that generates a reference signal REF. The reference signal can be a bandgap voltage reference or a reference current based on, for example, a bandgap voltage. The reference signal REF is provided from IC 602 to IC 600.

Within IC 600, the reference signal REF is buffered by a buffer 612 and provided to a control circuit 614. Control circuit 614 also receives a control input and generates a control signal based on the buffered reference signal and the control input. In an embodiment, the control signal is a current signal $I_{CONTROL}$. The control signal is provided from IC 600 to IC 602.

Within IC 602, the control signal is buffered by a buffer 624 and provided to a circuit element 626. Buffer 624 can, if necessary, generate a control voltage from a received current signal by passing the current signal through a resistor. This resistor can be an external resistor or an internal resistor fabricated on IC 602.

In a specific embodiment, reference circuit 622 generates a reference current I_{REF} based on a bandgap reference voltage and a resistor. Interface circuit 614 then generates the control signal $I_{CONTROL}$ that is a scaled version of the reference current. The scaling is determined, in part, by the control input., The control current signal can be expressed as:

$$I_{CONTROL}=K\cdot I_{REF}y[n] \qquad \text{Eq. (9)}$$

wherein y[n] is the control input and K is the overall scaling factor that takes into account the scaling factors for the reference and control circuits (e.g., the current mirrors within the reference and control circuits). The control current signal is buffered by buffer 624, and the buffered signal is provided to circuit element 626. Circuit element 626 can be, for example, a VGA, a mixer, a PA driver, or other circuit elements.

FIG. 6 shows a specific embodiment for the interface of a control signal between ICs. The invention can be applied to the generation of control signals for cellular telephone transmitter and receivers, and for other circuits. For example, analog control signals can be generated in accordance with the present invention to control, for example, attenuators, mixers, power amplifiers, oscillators in phase lock loops, adjustable filters, and other circuits. The invention is particular advantageous when the circuit to be controlled is fabricated on a first integrated circuit having a first set of characteristics and the control circuit is fabricated on a second integrated circuit having a second set of characteristics that can vary independently with respect to those of the first integrated circuit.

Some embodiments of the invention have been described with circuitry implemented using BJTs and MOSFETs. The invention can also be implemented with other circuits including FETs, MESFETs, HBTs, P-HEMTs, and others. Also, P-MOS and N-MOS can be used to implement the invention. As used herein, "transistor" generically refers to any active circuit, and is not limited to a BJT or MOSFET.

The foregoing description of the preferred embodiments is provided to enable any person skilled in the art to make or use the present invention. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without the use of the inventive faculty. Thus, the present invention is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

What is claimed is:

1. Circuitry to generate an interface signal between a first integrated circuit and a second integrated circuit comprising:

a reference circuit configured to provide a reference signal;

an interface circuit implemented on the first integrated circuit and operatively coupled to the reference circuit, the interface circuit configured to receive the reference signal and a data input and to generate the interface signal in response thereto; and

a circuit element implemented on the second integrated circuit and operatively coupled to the interface circuit, the circuit element configured to receive the interface signal and provide an output signal in response,

wherein the interface signal is a differential current signal.

2. The circuitry of claim 1, wherein the reference circuit is implemented on the second integrated circuit.

3. The circuitry of claim 1, further comprising:

at least one capacitor coupled between the differential current signal.

4. The circuitry of claim 1, wherein the interface signal represents an analog inphase (I) or quadrature (Q) baseband signal in a quadrature transmitter.

5. The circuitry of claim 1, wherein the reference signal is a voltage related to a bandgap voltage.

6. The circuitry of claim 1, wherein the reference signal is a current generated from a reference voltage and a resistor.

7. The circuitry of claim 6, wherein the output signal is a voltage signal, and wherein the resistor is external to the first and second integrated circuits.

8. The circuitry of claim 6, wherein the output signal is a current signal, and wherein the resistor is implemented on the second integrated circuit.

9. The circuitry of claim 6, wherein the interface circuit includes

a current mirror configured to receive the reference signal and to provide two or more mirror paths, and

a switch array coupled to the current mirror, the switching array configured to receive and decode the data input and to direct current from a set of selected mirror paths to an output of the switch array.

10. The circuitry of claim 1, wherein the data input comprises at least four bits of resolution.

11. The circuitry of claim 10, wherein the data input comprises at least eight bits of resolution.

12. The circuitry of claim 1, wherein the interface circuit is oversampled by an oversampling ratio of two or greater.

13. The circuitry of claim 12, wherein the oversampling ratio is 16 or greater.

14. The circuitry of claim 1, wherein the circuit element is a variable gain amplifier (VGA).

15. The circuitry of claim 1, wherein the circuit element is a modulator.

16. The circuitry of claim 15, wherein the modulator includes

a pair of current sources coupled to the interface signal, and

a pair of cross-coupled differential amplifiers, each differential amplifier coupled to a respective current source, the differential amplifiers configured to receive a carrier signal and to generate the output signal based, in part, on the carrier signal and the interface signal.

17. The circuitry of claim 16, wherein each current source in the modulator provides a bias current that is related to the reference signal.

18. A transmitter comprising the circuitry of claim 1.

19. A transmitter in a CDMA cellular telephone comprising the circuitry of claim 1.

20. Circuitry in a transmitter comprising:

a first interface circuit implemented on a first integrated circuit, the first interface circuit configured to receive a first data input and provide a first differential current signal; and

a modulator implemented on a second integrated circuit and operatively coupled to the first interface circuit, the modulator configured to receive the first differential current signal and a carrier signal and to generate an output signal in response thereto.

21. The circuitry of claim 20, further comprising:

a second interface circuit implemented on the first integrated circuit, the second interface circuit configured to receive a second data input and provide a second differential current signal,

wherein the modulator is further configured to receive the second differential current signal and to generate the output signal in response to the second differential current signal.

22. The circuitry of claim 21, wherein the first and second data inputs correspond to inphase (I) and quadrature (Q) baseband signals in a quadrature transmitter.

23. The circuitry of claim 21, further comprising:

a capacitor coupled between each of the first and second differential current signals.

24. The circuitry of claim 21, wherein each of the first and second data inputs has eight or more bits of resolution.

25. The circuitry of claim 21, wherein the first and second interface circuits are operated at an oversampled rate relative to a rate of the first and second data inputs.

26. The circuitry of claim 25, wherein the oversampled rate is sixteen or greater.

27. The circuitry of claim 20, further comprising:

a reference circuit implemented on the second integrated circuit and configured to provide a reference signal,

wherein the first interface circuit couples to the reference circuit and is further configured to receive the reference signal and to generate the first differential current signal based, in part, on the reference signal.

28. The circuitry of claim 27, wherein the reference signal is a current generated based on a reference voltage.

29. A transmitter in a cellular telephone comprising:

a digital processor implemented on a first integrated circuit and configured to provide digital inphase (I) and quadrature (Q) baseband signals;

first and second interface circuits implemented on the first integrated circuit and coupled to the digital processor, each interface circuit configured to receive a respective digital baseband signal and provide an analog baseband signal, wherein each quantized analog baseband signal comprises at least four bits of resolution and is implemented as a differential current signal; and

a modulator implemented on a second integrated circuit and operatively coupled to the first and second interface circuits, the modulator configured to receive and modulate the analog baseband signals with a carrier signal to provide a modulated output signal.

30. The transmitter of claim 29, further comprising:

a reference circuit implemented on the second integrated circuit and configured to provide a reference signal,

wherein each interface circuit couples to the reference circuit and is further configured to receive the reference signal, and wherein the analog baseband signals are further generated based, in part, on the reference signal.

31. A device comprising:

an interface circuit formed on a first integrated circuit (IC) for generating a differential current signal responsive to a reference signal and to a digital data input; and

a circuit element formed on a second IC for generating an output signal on the basis of the differential current signal.

32. The device of claim 31, wherein the device is a transmitter.

33. The device of claim 32, wherein the transmitter is a quadrature transmitter.

34. The device of claim 31, wherein the device is a CDMA telephone.

35. The device of claims 31, 32, or 34, wherein the reference signal is generated by a reference circuit on the second IC.

36. The device of claims 31, 32, or 34, further comprising a reference circuit for generating the reference signal.

37. The device of claims 31, 32, or 34, further comprising at least one capacitor coupled between the differential current signal.

38. The device of claims 31, 32, or 34, wherein the digital data input is at least one of an analog inphase (I) and a quadrature (Q) baseband signal.

39. The device of claims 31, 32, or 34, wherein the reference signal is a voltage reference signal.

40. The device of claim 39, wherein the voltage reference signal is generated on the bas of a bandgap reference voltage.

41. The device of claims 31, 32, or 34, wherein the reference signal is a current generated from a reference voltage and a resistor.

42. The device of claim 41, wherein the output signal is a voltage signal and the resistor is external to the first and second ICs.

43. The device of claim 41, wherein the output signal is a current signal and the resistor is implemented on the second IC.

44. The device of claims 31, 32, or 34, wherein the interface circuit includes a current mirror for generating at least two mirror paths using the reference signal and a switch array for decoding the digital data input and for directing current from selected ones of the mirror paths to generate the differential current signal.

45. The device of claims 31, 32, or 34, wherein the digital data input is at least a four bit digital data input.

46. The device of claims 31, 32, or 34, wherein the digital data input is an oversampled digital data signal.

47. The device of claims 31, 32, or 34, wherein the circuit element is any of a variable gain amplifier (VGA), mixer, and power amplifier (PA) driver.

48. The device of claims 31, 32, or 34, wherein the circuit element is a modulator.

49. The device of claim 48, wherein the modulator includes a pair of current sources coupled to the differential current signal, and a pair of cross-coupled differential amplifiers, each differential amplifier coupled to a respective current source, the differential amplifiers operating to receive a carrier signal and to generate the output signal based, in part, on the carrier signal and the differential current signal.

50. The device of claim 49, wherein each current source in the modulator provides a bias current that is related to the reference signal.

51. The device of claim 48, wherein the modulator performs direct up conversion.

52. A device comprising:

an interface circuit for generating a differential current signal, responsive to a reference signal and to a digital data input and adapted for external capacitive filtering between the differential current signal; and

a circuit element for generating an output signal on the basis of the differential current signal.

53. The device of claim 52, wherein the device is a transmitter.

54. The device of claim 53, wherein the transmitter is a quadrature transmitter.

55. The device of claim 52, wherein the device is a CDMA telephone.

56. The device of claims 52, 53, or 55, wherein the digital data input is at least one of an analog inphase (I) and a quadrature (Q) baseband signal.

57. The device of claims 52, 53, or 55, wherein the interface circuit includes a cement mirror for generating at least two mirror paths using the reference signal and a switch array for decoding the digital data input and for directing current from selected ones of the mirror paths to generate the differential current signal.

58. The device of claims 52, 53, or 55, wherein the circuit element is any of a variable gain amplifier (VGA), mixer, and power amplifier (PA) driver.

59. The device of claims 52, 53, or 55, wherein the circuit element is a modulator.

60. The device of claim 54, wherein the modulator includes a pair of current sources coupled to the differential current signal, and a pair of cross-coupled differential amplifiers, each differential amplifier coupled to a respective current source, the differential amplifiers operating to receive a carrier signal and to generate the output signal based, in part, on the carrier signal and the differential current signal.

61. The device of claim 60, wherein each current source in the modulator provides a bias current that is related to the reference signal.

62. The device of claim 60, wherein the modulator performs direct up conversion.

63. An analog integrated circuit (IC) adapted for use in a transmit signal path of a communication device, and responsive to an input differential current signal generated externally as a function of a reference signal and a digital data input, the analog IC comprising: a reference circuit for generating the reference signal; and a circuit element for generating an output signal on the basis of the differential current signal.

64. The analog integrated circuit of claim 63, wherein the reference signal is a voltage reference signal.

65. The analog integrated circuit of claim 64, wherein the voltage reference signal is generated on the basis of a bandgap reference voltage.

66. The analog integrated circuit of claim 63, wherein the reference signal is a current generated from a reference voltage and a resistor.

67. The analog integrated circuit of claim 66, wherein the output signal is a voltage signal and the resistor is external to the analog integrated circuit.

68. The analog integrated circuit of claim 66, wherein the output signal is a current signal and the resistor is implemented on the analog integrated circuit.

69. The analog integrated circuit of claim 63, wherein the circuit element is any of a variable gain amplifier (VGA), mixer, and power amplifier (PA) driver.

70. The analog integrated circuit of claim 63, wherein the circuit element is a modulator.

71. The analog integrated circuit of claim 70, wherein the modulator includes a pair of current sources coupled to the differential current signal, and a pair of cross-coupled differential amplifiers, each differential amplifier coupled to a respective current source, the differential amplifiers operating to receive a carrier signal and to generate the output signal based, in part, on the carrier signal and the differential current signal.

72. The analog integrated circuit of claim 71, wherein each current source in the modulator provides a bias current that is related to the reference signal.

73. The analog integrated circuit of claim 70, wherein the modulator performs direct up conversion.

74. An integrated circuit (IC) comprising:

a digital processor generating a digital data input; and

at least one interface circuit responsive to a reference signal for generating a differential current signal responsive to a reference signal and to the digital data input.

75. The integrated circuit of claim 74, wherein the at least one interface circuit includes a current mirror for generating at least two mirror paths using the reference signal and a switch array for decoding the digital data input and for directing current from selected ones of the mirror paths to generate the differential current signal.

76. The integrated circuit of claim 75, wherein the digital data input is at least a four bit digital data input.

77. The integrated circuit of claim 76, wherein the digital data input is an oversampled digital data signal.

78. A method comprising:

generating a reference signal;

providing the reference signal to a first circuit;

receiving a digital data input at the first circuit;

generating a differential current signal in the first circuit based, in part, on the digital data input and the reference signal;

providing the differential current signal from the first circuit to a second circuit;

receiving the differential current signal at the second circuit; and

generating an output signal from a circuit element in the second circuit, the output signal being based at least in part on the differential current signal.

79. The method of claim 78, wherein the reference signal is a current generated from a reference voltage.

80. The method of claim 78, further comprising filtering the differential current signal.

81. The method of claim 78, further comprising providing a signal related to the reference signal to the circuit element, wherein the output signal is further generated based, in part, on the signal related to the reference signal.

82. A system comprising:

means, formed on a first integrated circuit (IC), for generating a differential current signal responsive to a reference signal and to a digital data input; and

means, formed on a second IC, for generating an output signal on the basis of the differential current signal.

83. A system comprising:

means for generating a differential current signal, responsive to a reference signal and to a digital data input and adapted for external capacitive filtering between the differential current signal; and

means for generating an output signal on the basis of the differential current signal.

84. An analog integrated circuit (IC) adapted for use in a transmit signal path of a communication device, and responsive to an input differential current signal generated externally as a function of a reference signal and a digital data input, the analog IC comprising:

means for generating the reference signal; and

means for generating an output signal on the basis of the differential signal.

85. An integrated circuit (IC) comprising:

means for generating a digital data input; and

at least one interface circuit means responsive to a reference signal for generating a differential current signal responsive to a reference signal and to the digital data input.

* * * * *

MUTUAL
NON-DISCLOSURE AGREEMENT

This Mutual Non-Disclosure Agreement (the "Agreement") is made and entered into effective July 14, 2000, by and between QUALCOMM Incorporated, a Delaware corporation, with offices located at 5775 Morehouse Drive, San Diego, California 92121, and Conexant Systems, Inc., a Delaware corporation, with offices located at 4311 Jamboree Road, Newport Beach, California 92660, with regard to the following facts:

WHEREAS, each party to this Agreement possesses confidential and/or proprietary information related to technology and business activities, including, but not limited to, process technologies and capacities, wireless communications systems, business outlooks, revenue, pricing, product cost models and historical cost structures related thereto, trade secrets, computer programs and software (including, but not limited to, code, software output, screen displays, file hierarchies, graphics and user interfaces), formulas, data, inventions, techniques, product designs, tool kits, marketing roadmaps, strategies and third party confidential information (the "INFORMATION"); and

WHEREAS, each party in possession of INFORMATION (the "Disclosing Party") desires to disclose some of its INFORMATION to the other party (the "Receiving Party") subject to the terms and conditions of this Agreement;

NOW, THEREFORE, in consideration of the promises made herein, the receipt of certain INFORMATION and good and other valuable consideration, the receipt of which is hereby acknowledged, the parties hereto agree as follows:

1. Permitted Use. The Receiving Party shall handle, use, treat and utilize such INFORMATION as follows: (a) hold all INFORMATION received from the Disclosing Party in strict confidence using the same standard of care it uses to protect its own highly sensitive information, but in no event less than a reasonable degree of care; (b) use such INFORMATION only for the purpose of (i) evaluating the possibility of forming a joint business relationship or other commercial arrangement between the parties concerning such INFORMATION, and (ii) if and when such relationship is formed by a written agreement, furthering the purpose and intent expressly stated in such written agreement; (c) reproduce such INFORMATION only to the extent necessary for such purpose; (d) restrict disclosure of such INFORMATION to its employees with a need to know (and advise such employees of the obligations assumed herein) and to affiliates and independent contractors as set forth in Section 3 herein; and (e) not disclose such INFORMATION to any third party, including, but not limited to, any manufacturer (including, but not limited to, RF Micro Devices, Inc.) without prior written approval of such Disclosing Party. In addition, with respect to any equipment, component, software, or other items delivered to the Receiving Party by the Disclosing Party, the Receiving Party shall not reverse engineer, disassemble, decompile, or otherwise analyze the physical construction of, any such items.

The restrictions on the Receiving Party's use and disclosure of INFORMATION as set forth above shall not apply to any INFORMATION which the Receiving Party can demonstrate:

i. is wholly and independently developed by the Receiving Party without the use of INFORMATION of the Disclosing Party; or

ii. is or has become generally available to the public without breach of this Agreement by the Receiving Party; or

iii. at the time of disclosure to the Receiving Party, was known to such Receiving Party free of restriction and evidenced by documentation in the Receiving Party's possession; or

iv. is approved for release by written authorization of the Disclosing Party, but only to the extent of and subject to such conditions as may be imposed in such written authorization; or

v. is disclosed in response to a valid order of a court or other governmental body in the United States or any political subdivision thereof, but only to the extent of and for the purposes of such order; provided, however, that the Receiving Party shall first notify the Disclosing Party in writing of the order and permit the Disclosing Party a reasonable opportunity to seek an appropriate protective order.

2. Designation. INFORMATION shall be subject to the restrictions of Section 1 if it is in writing or other tangible form and clearly marked as proprietary or confidential when disclosed to the Receiving Party or, if not disclosed in tangible form, if clearly identified as confidential or proprietary at the time of disclosure. The parties agree to use reasonable efforts to summarize the content of oral disclosures which are proprietary or confidential but failure to provide such summary shall not affect the nature of the INFORMATION disclosed if such INFORMATION was identified as confidential or proprietary when orally disclosed.

3. Disclosure to Affiliates and Third Parties. This Agreement does not permit either party to disclose INFORMATION to any third party, except the Receiving Party may disclose INFORMATION to its affiliates and independent contractors provided that (i) INFORMATION shall be disclosed to any such affiliates and independent contractors on a need-to-know basis only and (ii) said affiliates and independent contractors are under contractual duty to hold INFORMATION disclosed by the Receiving Party to them confidential, at least to the same extent as the Receiving Party is obligated to keep INFORMATION confidential under this Agreement. The Receiving Party shall be responsible for any improper disclosure of INFORMATION made by any such affiliates and independent contractors to the same extent as if the Receiving Party itself had made such improper disclosure. Furthermore, the Receiving Party agrees, at its sole expense, to take all reasonable measures (including but not limited to court proceedings) to restrain such affiliates and independent contractors from prohibited or unauthorized disclosure or use of the INFORMATION..

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5. No Obligation. Neither this Agreement nor the disclosure or receipt of INFORMATION shall be construed as creating any obligation of a party to furnish INFORMATION to the other party or to enter into any agreement or relationship with the other party with respect to mutual business.

6. Return of Information. All INFORMATION shall remain the sole property of the Disclosing Party which originally disclosed such INFORMATION, and all materials containing any such INFORMATION (including all copies made by the Receiving Party) shall, within thirty (30) days of written request receipt, be returned to the Disclosing Party. Upon request of the Disclosing Party, the Receiving Party shall certify in writing that all materials containing such INFORMATION (including all copies thereof) have been returned to the Disclosing Party.

7. Written Assurance. To enable the Disclosing Party to disclose restricted technology and/or computer software to the Receiving Party in compliance with the requirements of the U.S. Department of Commerce Export Administration Regulations, the Receiving Party hereby gives its assurance to the Disclosing Party that the Receiving Party will not knowingly, unless prior written authorization is obtained from the Disclosing Party and the appropriate governmental body, reexport, directly or indirectly, restricted technology and/or computer software which is not otherwise available to the general public, nor allow the direct product thereof to be shipped directly or indirectly, to any of the

following countries or any successor thereof (as this list of countries may be amended from time to time by the U.S. Department of Commerce/and or U.S. Treasury Department):

Afghanistan	Georgia	North Korea
Albania	Iran	People's Republic of China
Armenia	Iraq	Romania
Azerbaijan	Kazakhstan	Russia
Belarus	Kyrgystan	Sudan
Bulgaria	Laos	Syria
Cambodia	Latvia	Tajikistan
Cuba	Libya	Turkmenistan
Estonia	Lithuania	Ukraine
Fed Rep of Yugoslavia (Serbia but not Montenegro or Kosovo)	Macau	Uzbekistan
	Moldova	Vietnam
	Mongolia	

Notwithstanding any other provision of this Agreement, this Section 7 shall survive any termination or expiration of this Agreement.

8. Term and Termination. This Agreement shall become effective on the date first set forth above and shall terminate upon the happening of the earlier of:

(a) The written notice of either party to the other of its election, with or without cause, to terminate this Agreement; or

(b) The expiration of twelve (12) months from the date first set forth above.

9. Notice. Any notice or other communication made or given by either party in connection with this Agreement shall be sent via facsimile (with confirmation) or by registered or certified mail, postage prepaid, return-receipt requested, or by courier service addressed to the other party at its address set forth below:

QUALCOMM Incorporated 5775 Morehouse Drive San Diego, California 92121	Conexant Systems, Inc. 4311 Jamboree Road Newport Beach, California 92660
Attn: Legal Department Fax: (858) 845-1250	Attn: Stewart Davis Fax: (949) 483-4176

10. Survivability. Each party agrees that all of its obligations undertaken herein as a Receiving Party shall survive and continue for a period of five (5) years after any termination or expiration of this Agreement.

11. Injunctive Relief. The parties agree that any unauthorized use of any of the INFORMATION in violation of this Agreement disclosed by a Disclosing Party will cause such Disclosing Party irreparable injury for which it would have no adequate remedy at law. Accordingly, the Disclosing Party shall be entitled to immediate injunctive relief prohibiting any violation of this Agreement, in addition to any other rights and remedies available to such Disclosing Party.

12. Attorneys' Fees. In the event either party shall bring any action to enforce or protect any of its rights under this Agreement, the prevailing party shall be entitled to recover, in addition to its damages, its reasonable attorneys' fees and costs incurred in connection therewith.

13. Governing Law and Forum. This Agreement shall be governed in all respects solely and exclusively by the laws of the State of California, U.S.A. without regard to conflict of laws principles.

14. Miscellaneous. This Agreement constitutes the entire understanding among the parties hereto as to the INFORMATION and supersedes (i) all prior discussions between them relating thereto and, (ii) that certain Non Disclosure Agreement between the parties entered into effective July 13, 2000. No amendment or modification of this Agreement shall be valid or binding on the parties unless made in writing and signed on behalf of each of the parties by its authorized officer or representative. No party may assign or transfer, in whole or in part, any of its rights, obligations or duties under this Agreement. The failure or delay of any party to enforce at any time any provision of this Agreement shall not constitute a waiver of such party's right thereafter to enforce each and every provision of this Agreement. In the event that any of the terms, conditions or provisions of this Agreement are held to be illegal, unenforceable or invalid by any court of competent jurisdiction, the remaining terms, conditions or provisions hereof shall remain in full force and effect.

15. Counterparts and Facsimile Delivery. This Agreement may be executed in two or more identical counterparts, each of which shall be deemed to be an original and all of which taken together shall be deemed to constitute the Agreement when a duly authorized representative of each party has signed a counterpart. The parties intend to sign and deliver this Agreement by facsimile transmission. Each party agrees that the delivery of the Agreement by facsimile shall have the same force and effect as delivery of original signatures and that each party may use such facsimile signatures as evidence of the execution and delivery of the Agreement by all parties to the same extent that an original signature could be used.

IN WITNESS WHEREOF, the parties have executed this Agreement on the date set forth above.

Conexant Systems, Inc., a Delaware corporation	QUALCOMM Incorporated, a Delaware corporation
By: Mohy F. Abdelgany	By:
Print Name: Mohe F. Abdelgany	Print Name: Jonathan Weiser
Title: V.P. – Wireless Communications Div.	Title: V.P. – Division Counsel