MILBANK, TWEED, HADLEY & McCLOY LLP
James Pooley (CA Bar No. 058041)
L. Scott Oliver (CA Bar No. 174824)
Marc David Peters (CA Bar No. 211725)
Anupam Sharma (CA Bar No. 229545)
3000 El Camino Real
Five Palo Alto Square, 7th Floor
Palo Alto, California 94306-2109
Telephone: (650) 739-7000
Facsimile: (650) 739-7100

Attorneys for Plaintiff UniRAM TECHNOLOGY, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

UniRAM TECHNOLOGY, INC., a California corporation,

Plaintiff,

v.

MONOLITHIC SYSTEM TECHNOLOGY, INC., a Delaware corporation; TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD., a Taiwan corporation; and TSMC NORTH AMERICA, a California corporation,

Defendants.

CASE NO. CV-04-01268-VRW

SECOND AMENDED COMPLAINT FOR TRADE SECRET MISAPPROPRIATION, PATENT INFRINGEMENT, INTERFERENCE WITH CONTRACT, UNFAIR COMPETITION, AND BREACH OF CONTRACT

DEMAND FOR JURY TRIAL

PARTIES

1. Plaintiff UniRAM Technology, Inc. ("UniRAM") is a corporation organized under the laws of California and has a principal place of business at 3375 Scott Boulevard, Santa Clara, California.

2. Defendant Monolithic System Technology, Inc. ("MoSys") is a corporation organized under the laws of Delaware and has a principal place of business at 1020 Stewart Drive, Sunnyvale, California.

3. Defendant Taiwan Semiconductor Manufacturing Company, Ltd. is a corporation organized under the laws of Taiwan and has a principal place of business at No. 8 Li-Hsin Road 6, Science-Based Industrial Park, Hsin-Chi, Taiwan 300-77.

4. Defendant TSMC North America is a corporation organized under the laws of California and has a principal place of business at 2585 Junction Avenue, San Jose, California.

5. Defendants Taiwan Semiconductor Manufacturing Company, Ltd. and TSMC North America will be collectively referred to herein as "TSMC." Defendants Monolithic System Technology, Inc., Taiwan Semiconductor Manufacturing Company, Ltd., and TSMC North America will be collectively referred to herein as "Defendants."

JURISDICTION AND VENUE

6. This is an action for damages and injunctive relief based upon patent infringement arising under Title 35 of the United States Code, upon trade secret misappropriation under California Civil Code section 3426, upon interference with contract, and upon violations of California unfair competition law.

7. This Court has jurisdiction over the subject matter of this action pursuant to 28 U.S.C. § 1331 and 28 U.S.C. § 1338. Supplemental subject matter jurisdiction for the state law claims is based on 28 U.S.C. § 1367. Venue is proper in this District pursuant to 28 U.S.C. § 1391.

8. This Court has jurisdiction over TSMC and MoSys because TSMC and MoSys have committed, induced, and/or contributed to acts of patent infringement, misappropriated trade secrets, and committed acts of unfair competition during the course of their business in this District.

THE PATENT IN SUIT

9. On August 22, 2000, U.S. Patent No. 6,108,229 ("the '229 patent"), entitled "High Performance Embedded Semiconductor Memory Device With Multiple Dimension First-Level Bit-Lines" was duly and legally issued to Jeng-Jye Shau. UniRAM is the owner of the entire right, title, and interest in and to the '229 patent. A copy of the '229 patent is attached as Exhibit A.

THE HIGH-PERFORMANCE COMPUTER MEMORY PROBLEM

10. In the mid-1990s, Dr. Shau, the inventor of the '229 patent, realized that the development of semiconductor memory circuits was falling behind the pace of improvements in logic integrated circuits (commonly referred to as "processors" and in some cases as "CPUs"). In short, he anticipated that by the late 1990s, memories would be the limiting factor for computer evolution. Dr. Shau, who had formerly worked with Intel on microprocessor design, founded his own company (the predecessor in interest to UniRAM) to set about solving this problem.

11. Conventional computer memory circuits are of two basic types. The first, known as "DRAM," combines one transistor and one capacitor. The capacitor can store an electrical charge for a short time, and the presence or absence of that electrical charge represents one bit of information—a zero or a one. DRAM circuits can be dense (i.e., many such transistor/capacitor sets can be packed onto a single chip), but they have certain drawbacks. First, the speed at which information can be accessed is usually slow. Second, and related, the capacitors storing the electrical charges will leak over time, so the information in the memory circuit needs to be periodically refreshed, just as a bucket of water with a hole in the bottom will store water for some period before it needs to be topped off again. And during that topping off process, no information can be retrieved from that DRAM circuit, forcing the processor to wait.

12. The second conventional type of memory circuit is known as "SRAM." Rather than using a transistor and capacitor, an SRAM circuit uses six transistors (or in some cases four). Those transistors form a circuit that can be toggled back and forth between two states, like a household light switch. One state represents a zero; the other, a one. SRAM circuits are faster than DRAM, and because there is no gradual draining of an electrical charge, they do not need to stop and top off their stored data. The chief problem with SRAM is that it consumes a relatively large amount of space on a computer chip: instead of taking up only enough room for a single transistor and capacitor, it requires space and interconnection among six transistors. Space on a computer chip is always a precious commodity.

13. Also in the mid-1990s, and continuing today, chip designers sought to combine logic and memory onto a single chip. In a mobile telephone, for instance, having separate processor and memory chips takes up valuable space and costs more to build than a mobile telephone that has its processor and its memory combined on the same chip. "System-On-a-Chip" combinations provide tremendous advantages to designers, but the actual production of memory and logic (processor) circuits on the same chip has been extremely difficult. Memory and logic circuits tend to be built with different—and incompatible—processes. Moreover, even if it were possible to combine the two processes, doing so would add many extra steps to the fabrication, and every step increases the likelihood that a defect will creep into the circuit being built.

14. In short, then, computer memory needed to be fast, it needed to be small, and its construction and operation needed to be compatible with nearby logic circuits on the same chip. In the mid-1990s, these problems were daunting. Dr. Shau's solution was a radically new approach to building memory circuits.

DR. SHAU'S SOLUTION

15. Dr. Shau's inspiration was to combine the small size of DRAM with the speed of SRAM, and—crucially—to build these new memory circuits ***during*** the logic circuit fabrication, eliminating the problems of incompatible processes and many extra steps.

16. The solution is simple in principle; in execution, it is complex. Dr. Shau developed a solution, and on May 24, 1996, he filed for the first in a series of patents on this technology. During the remainder of 1996—and throughout 1997 and 1998—Dr. Shau and his company invested considerable sums of money and engineering time proving that his technical solutions could be efficiently produced on a large scale.

DR. SHAU'S NON-DISCLOSURE AGREEMENTS WITH TSMC

17. Because only a handful of very large companies have semiconductor fabrication plants (often called "fabs") of their own, most semiconductor design firms arrange to have their chip designs built by specialized fab companies. One of the largest and oldest of such contract fabs is TSMC. TSMC works with companies around the world, building chips from those

companies' designs. TSMC's work is widely recognized as high-caliber, and Dr. Shau was interested in building his chips at TSMC.

18. Since TSMC is constantly exposed to innovative designs from its customers, many of whom are in competition with each other, it is accustomed to signing and abiding by non-disclosure agreements with its customers to ensure that their valuable trade secrets are kept confidential. Moreover, because TSMC is only interested in working with a small company if it can be convinced that the company's technology is successful and will generate substantial sales for TSMC, TSMC demanded full disclosure of UniRAM's technology under an NDA.

19. On September 16, 1996, Dr. Shau's company at the time (Telesis Innovation, Inc.—a predecessor in interest to UniRAM) and TSMC executed an NDA under which TSMC agreed to protect the secrecy of Dr. Shau's invention. A copy of that NDA is attached as Exhibit B. They executed additional NDAs on October 11, 1999 (between InTempo—another predecessor in interest to UniRAM—and TSMC, attached as Exhibit C), and August 29, 2000 (between UniRAM and TSMC, attached as Exhibit D). TSMC and UniRAM remain subject to an NDA today.

DR. SHAU'S DISCLOSURES OF TRADE SECRETS TO TSMC

20. Once an NDA was in place, Dr. Shau revealed his inventions to TSMC so that TSMC would understand the value of his inventions and agree to build circuits for UniRAM. The first presentation was late 1996 to TSMC sales managers, most of whom had Ph.D. degrees in engineering. The audience for this first presentation was sufficiently impressed that the current president of TSMC, Mr. F.C. Tseng, telephoned Dr. Shau to praise the invention and express TSMC's interest.

21. TSMC asked Dr. Shau to make a series of detailed presentations to TSMC in early 1997. Attendees from TSMC included the Vice President for Corporate Research and Development, the Deputy Director of the Embedded DRAM Product Management Program, the Program Deputy Director of the Memory Technology Development Division for Research and

Development, and the Deputy Director of Technical Marketing for the Corporate Marketing Division.

22. In the presentations, Dr. Shau explained how to build embedded memory devices using a logic fabrication process. This was a revolutionary advance, and TSMC expressed great interest in the value of Dr. Shau's technology. Dr. Shau told TSMC that he expected to serve a significant portion of the market for logic devices made with embedded memory.

23. Dr. Shau explained to TSMC that its then-existing embedded DRAM devices were difficult to construct because of conflicts between the memory and logic processes. His advance was to build embedded DRAM with a logic, or near-logic, process, but implementing that advance would require that Dr. Shau work closely with TSMC. Dr. Shau also told TSMC that his architecture was to break up large memory arrays into very small blocks, creating a high signal-to-noise ratio, and to use error correction circuitry to ensure reliability.

24. At the same time, TSMC and Dr. Shau discussed plans for rolling out Dr. Shau's second and third generation devices. The first generation approach—building a memory circuit with a logic circuit fabrication process (known as "1T," for "1 transistor")—provided very good results once the fabrication techniques were ironed out. During the development stage, Dr. Shau made detailed studies of the problems, and worked with TSMC manufacturing data to develop solutions to problems encountered in development. Some of Dr. Shau's solutions to the problems were the subject of continuation patent applications. Dr. Shau's 1T circuits had very high speed, low power consumption, and good space savings over SRAM 6 or 4 transistor memory technology. Dr. Shau achieved part of his success by using small blocks of memory cells that could react to information requests or be refreshed at very high speed. The first generation process also included error correction circuitry to detect any anomalies in the data retrieved from the memory cells, and it required no additional steps in fabrication. But Dr. Shau had already developed innovative improvements which he also disclosed in confidence to TSMC.

25. Dr. Shau also developed a variation of the first generation device, planned for testing in 1997, which requires one more step in the fabrication process, but increases the density of the memory cells by twenty percent. Given that space on a chip is always at a premium, this savings was well worth the extra step.

26. The second generation device involved two extra steps during fabrication. In those steps, the first generation 1T process was modified by placing a "shallow trench" near the memory cell's transistor. In essence, this trench would create a vertical capacitor, rather than a horizontal one, thus occupying much less space on the chip. While conventional DRAM circuits can use similar vertical capacitors, one of Dr. Shau's innovations was to build the "shallow trench" using a logic fabrication process. The resulting capacitor had more leakage and a smaller stored charge than a typical DRAM capacitor, but Dr. Shau also developed methods of overcoming those problems. The second generation device can reach near-DRAM memory cell densities, while retaining extremely high speeds that would be unattainable with DRAM technology—all without causing a significant increase in the manufacturing cost.

27. The third generation device used conventional DRAM storage capacitors, coupled with a logic transistor acting as a "word line" transistor in the memory cell. This process achieves the best density—allowing more memory cells to be packed onto a single chip—while reducing manufacturing complexities (typical DRAM transistors are high voltage, "thick gate" devices that are difficult to build using standard logic processes.) In addition, Dr. Shau further increased the speed of this third generation device by using a small memory block design.

28. In their meetings, Dr. Shau disclosed to TSMC all details, including memory cell and circuit design key factors and architecture, and the parties agreed this information was trade secret and was protected by the parties' NDA. Dr. Shau explained to TSMC that he was seeking a long-term relationship with a reliable fab so both parties could reap the rewards of his inventions.

29. Dr. Shau also told TSMC in confidence that his goal was to begin 1T production in 1997, and testing the third generation device by early 1998.

30. In a recap of these plans that Dr. Shau presented to TSMC in early 1997, it was acknowledged that TSMC would only be providing "foundry" (chip fabrication) services, and that no licensing or partnership with UniRAM was contemplated. The value of the relationship for TSMC would come through its fabrication fees, while UniRAM would realize on the value of its innovations through sales of chips and licenses to make them.

31. In the second half of 1998, UniRAM's predecessor in interest completed the design for a 128k Cache RAM circuit using UniRAM's technology. Strangely, TSMC held that design for nearly six months, finally building parts from it in April, 1999, and collecting its fabrication fees. However, unknown to UniRAM at the time, a competitor was about to emerge, a company that had improperly gained access to its secret technology via TSMC.

MOSYS ACQUIRES UNIRAM'S TRADE SECRETS FROM TSMC

32. MoSys began working with TSMC in the mid-1990s, and to help pay for the parts TSMC fabricated, MoSys transferred 5% of its stock to TSMC in late 1996. After MoSys' IPO in 2001, TSMC continued to own 2% of MoSys' stock.

33. In the mid-1990s, MoSys developed proprietary memory banks that could operate at reasonably high speed—an attractive feature for high-resolution computer graphics components, which need the ability to store and display graphics (for instance, for use in video games) quickly. However, MoSys' proprietary technology prevented mainstream adoption, and its sales were weak.

34. In 1996, MoSys released a new DRAM-based memory chip that provided reasonable speed, was somewhat smaller and cost less than comparable SRAM technology. MoSys continued to use non-standard interfaces for these parts, which limited consumer acceptance, and oversupply in the SRAM market led to a collapse in SRAM prices, erasing MoSys' price advantage. Sales, again, were unimpressive.

35. MoSys went back to what it termed "research and development" for nearly two years. Prior to 1998, all of MoSys' products were stand-alone memory circuits using conventional DRAM designs; before 1998, MoSys had never built an embedded ("System on a Chip")

memory circuit. But in 1998, MoSys released a 1T memory cell built using a logic fabrication process. Its technology bears an uncanny resemblance to UniRAM's inventions.

36. At the time, UniRAM had no reason to be suspicious: it knew little about the design details of MoSys' 1T memory cells, and it had no reason to believe TSMC would have violated the parties' confidential relationship. Over time, though, details about MoSys' designs became public. Like UniRAM, MoSys' 1T memories are made using standard logic fabrication methods. Like UniRAM, MoSys' 1T memories are extremely fast because MoSys used small blocks of memory cells. And like UniRAM, MoSys includes error correction circuitry to ensure the reliability of data retrieved from the memory blocks.

37. MoSys has even announced second (1T-SRAM-M), third (1T-SRAM-R), and fourth (1T-SRAM-Q) generation memory technologies that tracked UniRAM's secret roadmap. Indeed, MoSys has recently begun licensing a vertical capacitor design—1T-SRAM-Q—the key to UniRAM's second generation device. Since 1998, all of the significant technology "developments" made by MoSys followed, step by step, the road maps UniRAM had earlier provided to TSMC. With MoSys' release of 1T-SRAM-Q, UniRAM developed suspicions that MoSys had somehow gained access to that secret road map and perhaps other secret details of UniRAM's devices.

38. UniRAM now believes that the dramatic and sudden shift in MoSys' business—a shift that led it to mimic UniRAM—cannot be explained by coincidence, nor can the striking similarity of MoSys' technology be squared with independent development. UniRAM is informed and believes, and thereon alleges, that MoSys acquired UniRAM's trade secrets from TSMC, and that MoSys then set about deliberately copying UniRAM's inventions.

MOSYS' PROFITS FROM ITS USE OF UNIRAM'S TRADE SECRETS

39. MoSys' plan seems to have brought it near-term success. Its first major design win came in 1999, when it licensed embedded memory to Nintendo for use in Nintendo's forthcoming video game console. It followed that transaction by licensing similar technology to

companies such as Sanyo and Fujitsu. Significantly, it also granted a fabrication license for that technology to TSMC.

40. In 2002, MoSys realized revenue for the sales of products totaling nearly $3 million, almost $11 million in license fees, and more than $14 million in royalties. In short, MoSys earned $28 million by using technology misappropriated from UniRAM.

41. In 2003, MoSys' sales totaled close to $20 million, and its plans to release a fourth-generation product (1T-SRAM-Q) using UniRAM's technology are touted by MoSys as driving its expected 2004 and 2005 revenues. In the space of two years, MoSys' misappropriation of UniRAM's trade secrets has yielded it almost $50 million.

TSMC's AND MOSYS' PAST AND FUTURE PATENT INFRINGEMENT

42. UniRAM filed its first patent application on its memory cell inventions in 1996. By the time its trade secrets were leaked to MoSys through TSMC, UniRAM had 4 applications on file. At present, UniRAM has a portfolio of more than a dozen issued patents on its first, second, and third generation memory technology. MoSys' future products—which UniRAM is informed and believes it plans to license to TSMC—will apparently be copies or derivatives of UniRAM's second generation device using the vertical capacitor, a feature patented by UniRAM since early 1997. Moreover, UniRAM is informed and believes that TSMC provides both foundry (manufacture) and design services for 1T memories using UniRAM's technology.

CLAIM I—TRADE SECRET MISAPPROPRIATION

43. UniRAM realleges and incorporates by reference each of the preceding paragraphs of this complaint.

44. UniRAM enjoys an advantage over its existing and would-be competitors in the design, development, production, promotion and marketing of advanced memory circuits because of the UniRAM trade secrets described above, including but not limited to its first, second, and third generation devices, its small blocks of memory cells, and its error correction circuitry.

45. UniRAM has made reasonable efforts under the circumstances to protect the confidentiality of its trade secrets, including the expression of some of those secrets in patent applications before they were published. UniRAM's confidential information shared with TSMC derives independent economic value from not being generally known to the public or other persons who could obtain economic value from its disclosure or use. Accordingly, this information qualifies as trade secrets under California's Uniform Trade Secrets Act, Cal. Civ. Code § 3426 *et seq*.

46. TSMC and its employees were under a duty to keep UniRAM's confidential information secret. MoSys knew or reasonably should have known that TSMC owed a duty to UniRAM to maintain the information in secrecy. Nevertheless, on information and belief, MoSys obtained this information from TSMC through improper means and without the express or implied consent of UniRAM, and MoSys and TSMC are now using the trade secrets in connection with their own business activities.

47. Each of the acts of misappropriation was, on information and belief, done willfully and maliciously by MoSys and TSMC.

48. As a direct result of MoSys and TSMC's misappropriation of UniRAM's trade secrets, MoSys and TSMC have been unjustly enriched and UniRAM has sustained damages in an amount to be proven at trial. UniRAM has also suffered irreparable harm as a result of MoSys and TSMC's activities and will continue to suffer irreparable injury that cannot be adequately remedied at law unless MoSys, TSMC, their officers, agents, employees, and all persons acting in concert with them, are temporarily, preliminarily, and permanently enjoined from engaging in further such acts of misappropriation or enjoying the fruits of its misappropriation.

CLAIM II—INFRINGEMENT OF THE '229 PATENT

49. UniRAM realleges and incorporates by reference each of the preceding paragraphs of this complaint.

50. MoSys and TSMC have infringed and continue to infringe; have induced and continue to induce others to infringe; and/or have committed and continue to commit acts of contributory infringement of one or more of the claims of the '229 patent. TSMC and MoSys' infringing activities in the United States and this District include development, manufacture, use, importation, sale, and/or offer for sale of UniRAM's memory cell technology. Such infringing activities violate 35 U.S.C. § 271. Upon information and belief, such infringement has been, and continues to be, willful.

51. As a consequence of the infringing activities of TSMC and MoSys regarding the '229 patent as complained of herein, UniRAM has suffered monetary damages in an amount not yet determined, and UniRAM will continue to suffer irreparable damages in the future unless and until TSMC and MoSys' infringing activities are enjoined by this Court.

CLAIM III—INTENTIONAL INTERFERENCE WITH CONTRACT

52. UniRAM realleges and incorporates by reference each of the preceding paragraphs of this complaint.

53. The nondisclosure agreements between TSMC and UniRAM (including UniRAM's predecessors in interest) are valid and enforceable contracts obligating TSMC to maintain UniRAM's trade secrets in confidence.

54. On information and belief, MoSys is and has been aware of the existence of these contracts between TSMC and UniRAM.

55. MoSys interfered with UniRAM's contractual obligations with TSMC by obtaining and misusing the information UniRAM had disclosed in confidence to TSMC.

56. This interference has caused UniRAM to suffer monetary damages in an amount not yet determined, and it will continue to suffer irreparable damages in the future unless and until MoSys' interference is enjoined by this Court.

CLAIM IV—UNFAIR COMPETITION IN VIOLATION OF CALIFORNIA LAW

57. UniRAM realleges and incorporates by reference each of the preceding paragraphs of this complaint.

58. TSMC and MoSys' actions complained of above constitute California common law unfair competition and violations of California Business and Professions Code § 17200 *et seq.*

CLAIM V—BREACH OF CONTRACT

59. UniRAM realleges and incorporates by reference each of the preceding paragraphs of this complaint.

60. The nondisclosure agreements between TSMC and UniRAM (including UniRAM's predecessors in interest) are valid and enforceable contracts obligating TSMC to maintain UniRAM's trade secrets in confidence and not to use them for any unauthorized purpose.

61. On information and belief, TSMC revealed those trade secrets to MoSys or to persons or entities who in turn revealed them to MoSys, for purposes not authorized by UniRAM, in violation of TSMC's contracts with UniRAM.

62. Those breaches have caused UniRAM to suffer monetary damages in an amount not yet determined, and it will continue to suffer irreparable damages in the future unless and until TSMC's improper conduct is enjoined by this Court.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff UniRAM prays for judgment and relief as follows:

1. A declaration that TSMC and MoSys have misappropriated UniRAM's trade secrets;

2. Temporary, preliminary, and permanent injunctions restraining TSMC, MoSys, their officers, agents, servants, employees, attorneys, parents, subsidiaries, and other persons in concert or participation with them, from directly or indirectly obtaining, using, or communicating to any person or entity any trade secrets or confidential information of UniRAM;

3. An award of compensatory damages for trade secret misappropriation, including an accounting and award of all TSMC and MoSys' gains, profits, and savings derived from its improper conduct;

4. An award of treble damages pursuant to Cal. Civil Code § 3426.3;

5. A declaration that TSMC and MoSys have infringed, induced infringement of, and contributorily infringed, the '229 patent in violation of 35 U.S.C. § 271;

6. An award of actual and consequential damages pursuant to, *inter alia*, 35 U.S.C. § 284 in an amount appropriate to compensate UniRAM for the damages caused by TSMC and MoSys' infringement of the '229 patent;

7. Temporary, preliminary, and permanent injunctions pursuant to 35 U.S.C. § 283 restraining TSMC, MoSys, their officers, agents, servants, employees, attorneys, parents, subsidiaries, and other persons in concert or participation with them, from further infringing the '229 patent, and from making, using, offering for sale, licensing, importing or selling their infringing memory products;

8. A declaration that TSMC and MoSys' infringement of the '229 patent has been willful and deliberate and that this case is exceptional pursuant to 35 U.S.C. §§ 284 and 285;

9. An award of treble damages pursuant to 35 U.S.C. § 284;

10. A declaration that MoSys has interfered with contracts between UniRAM and TSMC;

11. Temporary, preliminary, and permanent injunctions restraining MoSys, its officers, agents, servants, employees, attorneys, parents, subsidiaries, and other persons in concert or participation with it, from directly or indirectly interfering with contracts between UniRAM and TSMC;

12. Temporary, preliminary, and permanent injunctions restraining TSMC, its officers, agents, servants, employees, attorneys, parents, subsidiaries, and other persons in concert or participation with it, from directly or indirectly breaching its contracts with UniRAM;

13. An award of compensatory damages for interference with contract, including an accounting and award of all MoSys' gains, profits, and savings derived from its improper conduct;

14. An award of compensatory damages for TSMC's breach of contract, including an accounting and award of all TSMC's gains, profits, and savings derived from its improper conduct;

15. Damages in an amount to be determined at trial;

16. Restitution and disgorgement of defendants' unjust enrichment, including but not

limited to all sales revenues, licensing revenues, royalties, and other sums earned by manufacturing, selling and/or licensing MoSys' 1T technology, pursuant to Cal. Bus. & Prof. Code § 17203;

17. An award of costs and attorneys' fees as permitted by law, including pursuant to 35 U.S.C. § 285 and Cal. Civil Code § 3426.4;

18. An award of pre-judgment interest; and

19. Such other and further relief as the Court may deem just and proper.

Dated: April 28, 2004

Respectfully submitted,

MILBANK, TWEED, HADLEY & McCLOY LLP

By: /s/
James Pooley
L. Scott Oliver
Marc David Peters
Anupam Sharma

Attorneys for Plaintiff UniRAM Technology, Inc.

JURY DEMAND

UniRAM demands a jury trial on all issues triable to a jury in this matter.

Dated: April 28, 2004

Respectfully submitted,

MILBANK, TWEED, HADLEY & McCLOY LLP

By: /s/
James Pooley
L. Scott Oliver
Marc David Peters
Anupam Sharma

Attorneys for Plaintiff UniRAM Technology, Inc.