

1 ANDREW D. FORTNEY (SBN 178699)  
2 SHERRIE M. FLYNN (SBN 240215)  
3 BRADLEY J. LEVANG (SBN 226922)  
4 The Law Offices of Andrew D. Fortney, Ph.D., P.C.  
5 1725 N. Fine Ave., Suite 101  
6 Fresno, CA 93727  
7 Telephone: (559) 432-6847  
8 Facsimile: (559) 432-6872  
9 Email: *andrew.fortney@fortneylaw.com*  
10 Email: *sherrie.flynn@fortneylaw.com*  
11 Email: *bradley.levang@fortneylaw.com*

12 Attorneys for Plaintiff  
13 GOLDEN GATE TECHNOLOGY, INC.

14  
15  
16  
17  
18  
19  
20  
21  
22  
23  
24  
25  
26  
27  
28

**UNITED STATES DISTRICT COURT**  
**NORTHERN DISTRICT OF CALIFORNIA**  
**SAN FRANCISCO DIVISION**

GOLDEN GATE TECHNOLOGY, INC., a  
California Corporation

Plaintiff,

vs.

MENTOR GRAPHICS CORP., an Oregon  
Corporation,

Defendant

) Case No.: 3:12-cv-01840-SI

) **FIRST AMENDED COMPLAINT FOR**  
) **PATENT INFRINGEMENT**

) **JURY TRIAL DEMANDED**

//

//

//

1 Plaintiff GOLDEN GATE TECHNOLOGY, INC (“GGT”) hereby alleges as follows:

2 **INTRODUCTION**

3 1. This is a patent infringement action wherein GGT alleges that MENTOR  
4 GRAPHICS CORP. (“MENTOR”) is, and has been, infringing, contributing to the  
5 infringement of, and/or actively inducing others to infringe claims of U.S. Patent Nos.  
6 7,260,804 (“‘804 Patent”), 7,360,193 (“‘193 Patent”), 7,823,112 (“‘112 Patent”) and  
7 7,992,122 (“‘122 Patent”) (collectively “Asserted Patents”).

8 **PARTIES**

9 2. Plaintiff GOLDEN GATE TECHNOLOGY, INC. is a California corporation  
10 with its principal place of business at 1101 S. Winchester Blvd., Suite J-255, San Jose,  
11 California 95128.

12 3. On information and belief, and thereon alleged, Defendant MENTOR  
13 GRAPHICS CORP. is an Oregon corporation with its principal place of business at 8005  
14 Southwest Boeckman Road, Wilsonville, Oregon 97070.

15 4. On information and belief, and thereon alleged, MENTOR owns a facility  
16 located at, or near, 46871 Bayside Parkway, Fremont, California 94538, from which  
17 MENTOR conducts business operations, including research and development, sales, and  
18 administration.

19 **JURISDICTION AND VENUE**

20 5. This Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and  
21 1338(a) as this action arises under the patent laws of the United States, 35 U.S.C. § 1, et seq.,  
22 including 35 U.S.C. § 271.

23 6. This Court has personal jurisdiction over MENTOR, who maintains significant  
24 business operations in this District, has conducted and does conduct business within the State  
25 of California and within this District, and because a substantial part of the events giving rise to  
26 GGT’s claims occurred in this District.

27 7. Venue is proper in this Court pursuant to 28 U.S.C. §§ 1391(b), (c) and/or  
28 1400(b) because MENTOR is subject to personal jurisdiction in this District, conducts

1 business in this District, and because a substantial part of the events giving rise to GGT's  
2 claims occurred in this District.

### 3 INTRADISTRICT ASSIGNMENT

4 8. This is an Intellectual Property Action to be assigned on a district-wide basis  
5 pursuant to Civil Local Rule 3-2(c).

### 6 FACTUAL BACKGROUND

7 9. The field of electronic design automation ("EDA") pertains to the use of  
8 computer software and hardware for the design, analysis and creation of electronics and  
9 electronic components, including circuits and integrated circuits.

10 10. Circuit designers may use EDA software to automatically, or semi-  
11 automatically, place and/or configure circuit components and circuits.

12 11. Circuits often incorporate the use of 1) timing circuits, to ensure that signals are  
13 captured at predetermined locations at certain times, and 2) switches, which can interrupt  
14 and/or divert signals. As circuits become more complex, accurate and reliable timing and  
15 switching are increasingly important in circuit design and function.

16 12. Circuit designers face multiple challenges in designing circuits to meet the  
17 demand for ever smaller sized components and for products with increased functionality and  
18 more efficient power consumption. As circuits are made ever smaller and more complex, the  
19 size and placement of wires and components for such circuits have an ever increasing impact  
20 on the timing and switching that occurs in the circuit. Improper or inefficient component  
21 placement and/or wire routing can result in inefficiencies and improper function, such as  
22 increased power consumption, inconsistent timing, inefficient function, and even outright  
23 inoperability.

24 13. GGT's innovations in the EDA field are critical for increasing the efficiency of  
25 EDA-based circuit design and reducing power consumption in circuits designed using EDA  
26 tools. GGT's innovations provide for improvements in the ability to design circuits and  
27 integrated circuits by taking into account, among other things, timing, switching, and power  
28 utilization when placing circuit components and routing wires in such circuits.

1           14.     On or about August 21, 2007, the United States Patent and Trademark Office  
2 (“USPTO”) issued the ‘804 Patent entitled “Method for Circuit Block Routing Based on  
3 Switching Activity” to GGT, the assignee of the entire interest. Attached hereto as Exhibit A  
4 is a true and correct copy of the ‘804 Patent.

5           15.     On or about April 15, 2008, the USPTO issued the ‘193 Patent entitled “Method  
6 for Circuit Block Placement and Circuit Block Arrangement Based on Switching Activity” to  
7 GGT, the assignee of the entire interest. Attached hereto as Exhibit B is a true and correct  
8 copy of the ‘193 Patent.

9           16.     On or about October 26, 2010, the USPTO issued the ‘112 Patent entitled  
10 “Method, Software and System for Ensuring Timing Between Clocked Components in a  
11 Circuit” to GGT, the assignee of the entire interest. Attached hereto as Exhibit C is a true and  
12 correct copy of the ‘112 Patent.

13           17.     On or about August 2, 2011, the United States Patent and Trademark Office  
14 (“USPTO”) issued the ‘122 Patent entitled “Method of Placing and Routing for Power  
15 Optimization and Timing Closure” to GGT, the assignee of the entire interest. Attached  
16 hereto as Exhibit D is a true and correct copy of the ‘122 Patent.

17           18.     On information and belief, and thereon alleged, MENTOR designs, develops,  
18 makes, sells and supports EDA software, and provides consulting, training, and other services  
19 in support of their products.

20           19.     On information and belief, and thereon alleged, MENTOR has made, used, sold,  
21 imported and/or offered for sale, and/or continues to make, use, sell, import and/or offer for  
22 sale products in the United States consisting of, or including, EDA algorithms, methods and  
23 software (collectively “Accused Products”) which infringe on the Asserted Patents.

24           20.     On information and belief, and thereon alleged, the Accused Products include  
25 MENTOR’s Olympus-SoC system.

26           21.     MENTOR’s making, using, selling, offering for sale, and/or importing of the  
27 Accused Products in the United States constitutes direct infringement of the Asserted Patents.

28     //

22. On information and belief, and thereon alleged, MENTOR has sold or offered to sell the Accused Products to third parties who use the Accused Products to design and/or make their own products. Thus, MENTOR is inducing and/or contributing, and has induced and/or contributed to, infringement of the Asserted Patents.

23. MENTOR has been aware of the '193, '112 and '804 Patents at least as early as November 8, 2010 and the '122 Patent at least as early as August 10, 2012.

24. GGT is entitled to recover from MENTOR the actual damages it sustained and continues to sustain as a result of MENTOR's wrongful acts alleged herein under 35 U.S.C. § 284 in an amount to be proven at trial, together with interest and costs.

25. On information and belief, and thereon alleged, MENTOR's infringement of the Asserted Patents is, and has been, willful, deliberate, and in disregard of GGT's patent rights, and pursuant to 35 U.S.C. §§ 284 and 285, GGT is therefore entitled to enhanced damages up to three times the amount of actual damages and attorneys' fees.

**FIRST CAUSE OF ACTION**  
**Infringement of U.S. Patent No. 7,260,804**  
**under 35 U.S.C. § 271, et seq.**

26. The allegations of paragraphs 1-25 are incorporated herein as if fully set forth.

27. MENTOR actively and knowingly has infringed, and is infringing, the '804 Patent with knowledge of GGT's patent rights and without reasonable basis for believing that MENTOR's conduct is lawful.

28. MENTOR has induced and contributed, and is continuing to induce and contribute, to the infringement of the '804 Patent by purchasers, licensees, and users of the Accused Products.

29. MENTOR's acts of infringement have been and continue to be willful, deliberate, and in reckless disregard of GGT's patent rights.

30. MENTOR has injured GGT and is thus liable to GGT for infringement of the '804 Patent pursuant to 35 U.S.C. § 271.

//

//

**SECOND CAUSE OF ACTION**  
**Infringement of U.S. Patent No. 7,360,193**  
**under 35 U.S.C. § 271, et seq.**

31. The allegations of paragraphs 1-25 are incorporated herein as if fully set forth.

32. MENTOR actively and knowingly has infringed, and is infringing, the '193 Patent with knowledge of GGT's patent rights and without reasonable basis for believing that MENTOR's conduct is lawful.

33. MENTOR has induced and contributed, and is continuing to induce and contribute, to the infringement of the '193 Patent by purchasers, licensees, and users of the Accused Products.

34. MENTOR's acts of infringement have been and continue to be willful, deliberate, and in reckless disregard of GGT's patent rights.

35. MENTOR has injured GGT and is thus liable to GGT for infringement of the '193 Patent pursuant to 35 U.S.C. § 271.

**THIRD CAUSE OF ACTION**  
**Infringement of U.S. Patent No. 7,823,112**  
**under 35 U.S.C. § 271, et seq.**

36. The allegations of paragraphs 1-25 are incorporated herein as if fully set forth.

37. MENTOR actively and knowingly has infringed and is infringing the '112 Patent with knowledge of GGT's patent rights and without reasonable basis for believing that MENTOR's conduct is lawful.

38. MENTOR has induced and contributed, and is continuing to induce and contribute, to the infringement of the '112 Patent by purchasers, licensees, and users of the Accused Products.

39. MENTOR's acts of infringement have been and continue to be willful, deliberate, and in reckless disregard of GGT's patent rights.

40. MENTOR has injured GGT and is thus liable to GGT for infringement of the '112 Patent pursuant to 35 U.S.C. § 271.

//

//

**FOURTH CAUSE OF ACTION**  
**Infringement of U.S. Patent No. 7,992,122**  
**under 35 U.S.C. § 271, et seq.**

41. The allegations of paragraphs 1-25 are incorporated herein as if fully set forth.

42. MENTOR actively and knowingly has infringed and is infringing the '122 Patent with knowledge of GGT's patent rights and without reasonable basis for believing that MENTOR's conduct is lawful.

43. MENTOR has induced and contributed, and is continuing to induce and contribute, to the infringement of the '122 Patent by purchasers, licensees, and users of the Accused Products.

44. MENTOR's acts of infringement have been and continue to be willful, deliberate, and in reckless disregard of GGT's patent rights.

45. MENTOR has injured GGT and is thus liable to GGT for infringement of the '122 Patent pursuant to 35 U.S.C. § 271.

**PRAYER FOR RELIEF**

WHEREFORE, PLAINTIFF prays for the following relief from this Court:

a) An adjudication that MENTOR has infringed and continues to infringe the Asserted Patents as alleged above;

b) An accounting of all damages sustained by GGT as a result of MENTOR's acts of infringement of the Asserted Patents;

c) An award to GGT of actual damages adequate to compensate GGT for MENTOR's acts of patent infringement, together with prejudgment and post judgment interest;

d) An award of GGT's attorneys' fees and costs pursuant to 35 U.S.C. § 285;

e) Awarding such other and further relief as this Court may deem just and proper.

//

//

//

1 Date: October 17, 2012

Respectfully Submitted,  
THE LAW OFFICES OF ANDREW D.  
FORTNEY, Ph.D., P.C.

2  
3  
4 By: 

ANDREW D. FORTNEY  
SHERRIE M. FLYNN  
BRADLEY J. LEVANG

Attorneys for Plaintiff  
GOLDEN GATE TECHNOLOGY, INC.

5  
6  
7  
8  
9 **DEMAND FOR A JURY TRIAL**

10 GGT hereby demands a jury trial for all issues so triable.

11  
12 Date: October 17, 2012

Respectfully Submitted,  
THE LAW OFFICES OF ANDREW D.  
FORTNEY, Ph.D., P.C.

13  
14  
15 By: 

ANDREW D. FORTNEY  
SHERRIE M. FLYNN  
BRADLEY J. LEVANG

Attorneys for Plaintiff  
GOLDEN GATE TECHNOLOGY, INC.



# **EXHIBIT A**

(12) **United States Patent**  
**Burstein et al.**

(10) **Patent No.:** **US 7,260,804 B1**  
(45) **Date of Patent:** **Aug. 21, 2007**

(54) **METHOD FOR CIRCUIT BLOCK ROUTING  
BASED ON SWITCHING ACTIVITY**

2005/0050496 A1 \* 3/2005 Kovacs et al. .... 716/6

(75) Inventors: **Michael Burstein**, Cupertino, CA (US);  
**Vladimir Zakladny**, San Jose, CA  
(US); **Alexander Kouznetsov**,  
Campbell, CA (US)

(73) Assignee: **Golden Gate Technology, Inc.**, San  
Jose, CA (US)

(\*) Notice: Subject to any disclaimer, the term of this  
patent is extended or adjusted under 35  
U.S.C. 154(b) by 109 days.

(21) Appl. No.: **10/946,688**

(22) Filed: **Sep. 21, 2004**

(51) **Int. Cl.**  
**G06F 17/50** (2006.01)

(52) **U.S. Cl.** ..... **716/12; 716/14**

(58) **Field of Classification Search** ..... 716/8-10,  
716/12-14

See application file for complete search history.

(56) **References Cited**

#### U.S. PATENT DOCUMENTS

5,774,380	A *	6/1998	Pickup et al. ....	703/14
6,230,304	B1	5/2001	Groeneveld et al.	
6,253,361	B1	6/2001	Buch	
6,397,170	B1 *	5/2002	Dean et al. ....	703/14
6,453,446	B1	9/2002	van Ginneken	
6,496,965	B1	12/2002	van Ginneken et al.	
6,507,941	B1	1/2003	Leung et al.	
6,553,338	B1	4/2003	Buch et al.	
6,681,338	B1 *	1/2004	Kollipara ....	713/503
6,725,438	B2	4/2004	van Ginneken	
6,950,998	B1 *	9/2005	Tuan ....	716/2
2002/0069396	A1 *	6/2002	Bhattacharya et al. ....	716/7

#### OTHER PUBLICATIONS

Jim Flynn and Brandon Waldo; Power Management in Complex SoC Design (16 Pages); Apr. 2004; Synopsis, Inc., 700 East Middlefield Rd., Mountain View, CA 94043; <http://www.synopsys.com/sps>.

Astro-Rail: A Comprehensive Power-Integrity Analysis, Implementation and Verification Tool (2 Pages); Data Sheet, May 2003; Synopsis, Inc., 700 East Middlefield Rd., Mountain View, CA 94043.

\* cited by examiner

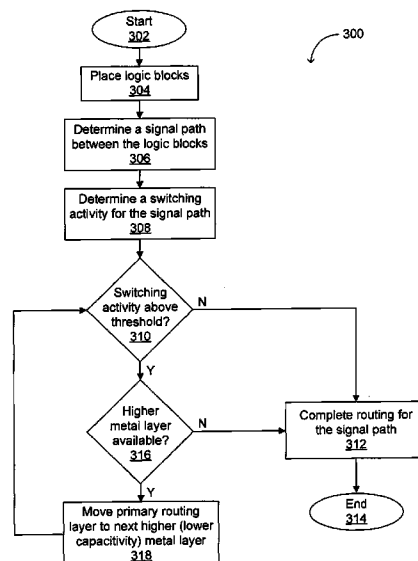
*Primary Examiner*—Stacy A Whitmore

(74) *Attorney, Agent, or Firm*—Andrew D. Fortney

(57) **ABSTRACT**

A method, algorithm, software, architecture and/or system for routing signal paths or connections between circuit blocks in a circuit design is disclosed. In one embodiment, a method of routing can include: (i) determining a switching activity for signal path between a first circuit block and a second circuit block; and (ii) routing the signal path substantially in a connectivity layer related to the switching activity of the signal path. The circuit blocks can include standard cells configured to implement a logic or timing function, other components, and/or integrated circuits, for example. The switching activity can include a switching frequency determination based on simulation results of the signal path between the circuit blocks. Embodiments of the present invention can advantageously reduce power consumption as well as supply noise by optimally routing signal paths between circuit blocks in an automated place-and-route flow. Further, signal integrity problems due to non-optimal routing can be reduced or minimized relative to conventional techniques.

**44 Claims, 7 Drawing Sheets**



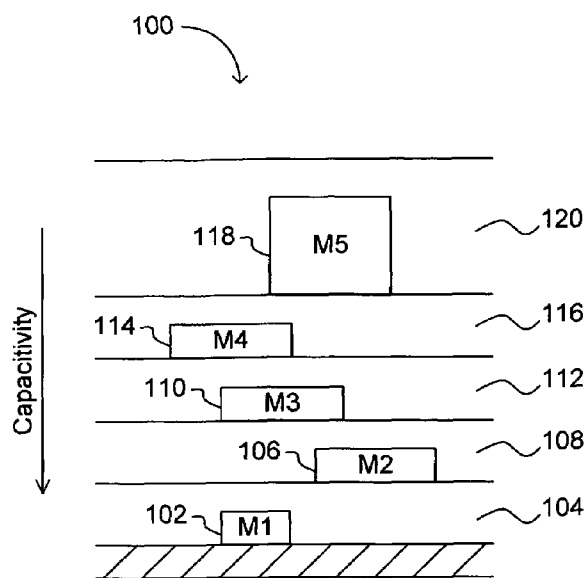


FIG. 1A (conventional)

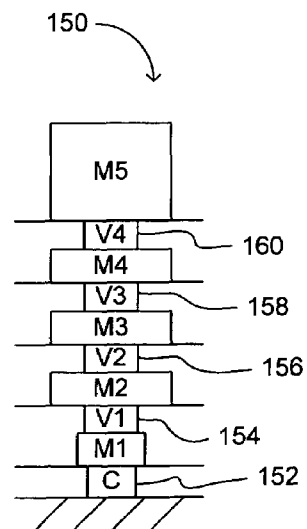


FIG. 1B (conventional)

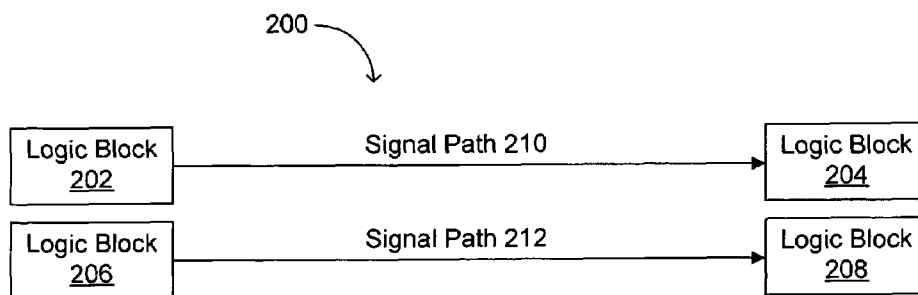


FIG. 2A

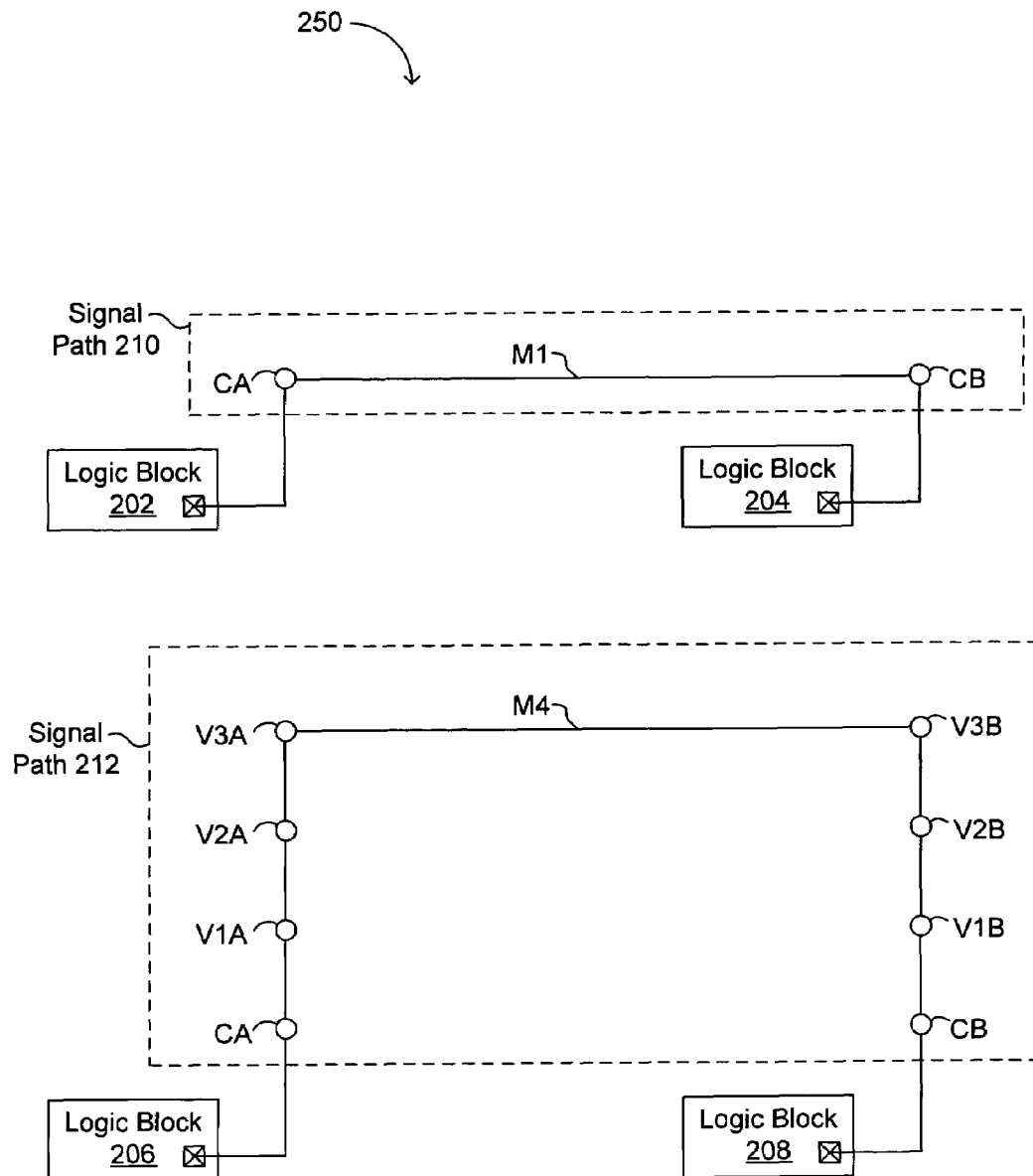


FIG. 2B

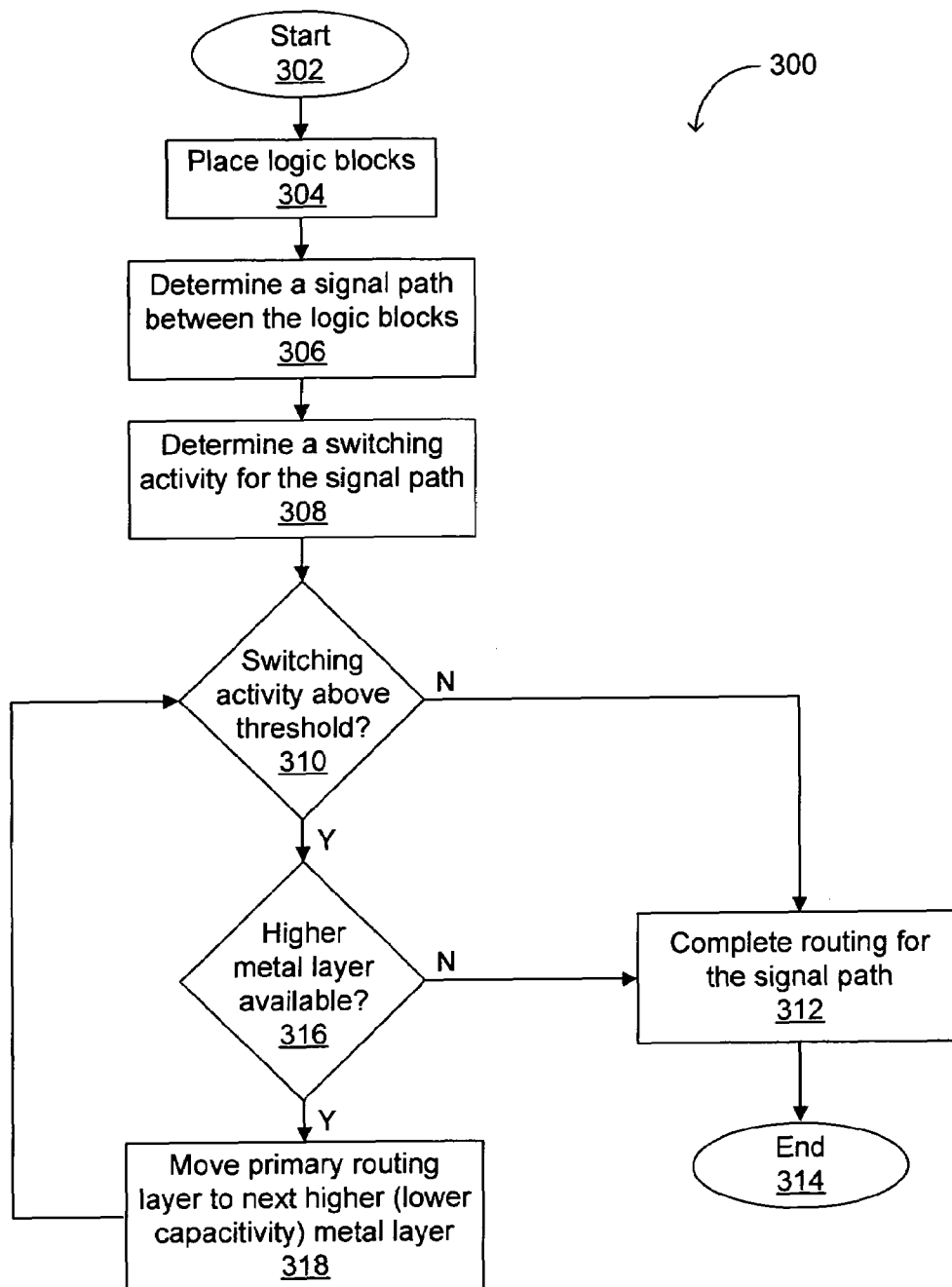


FIG. 3A

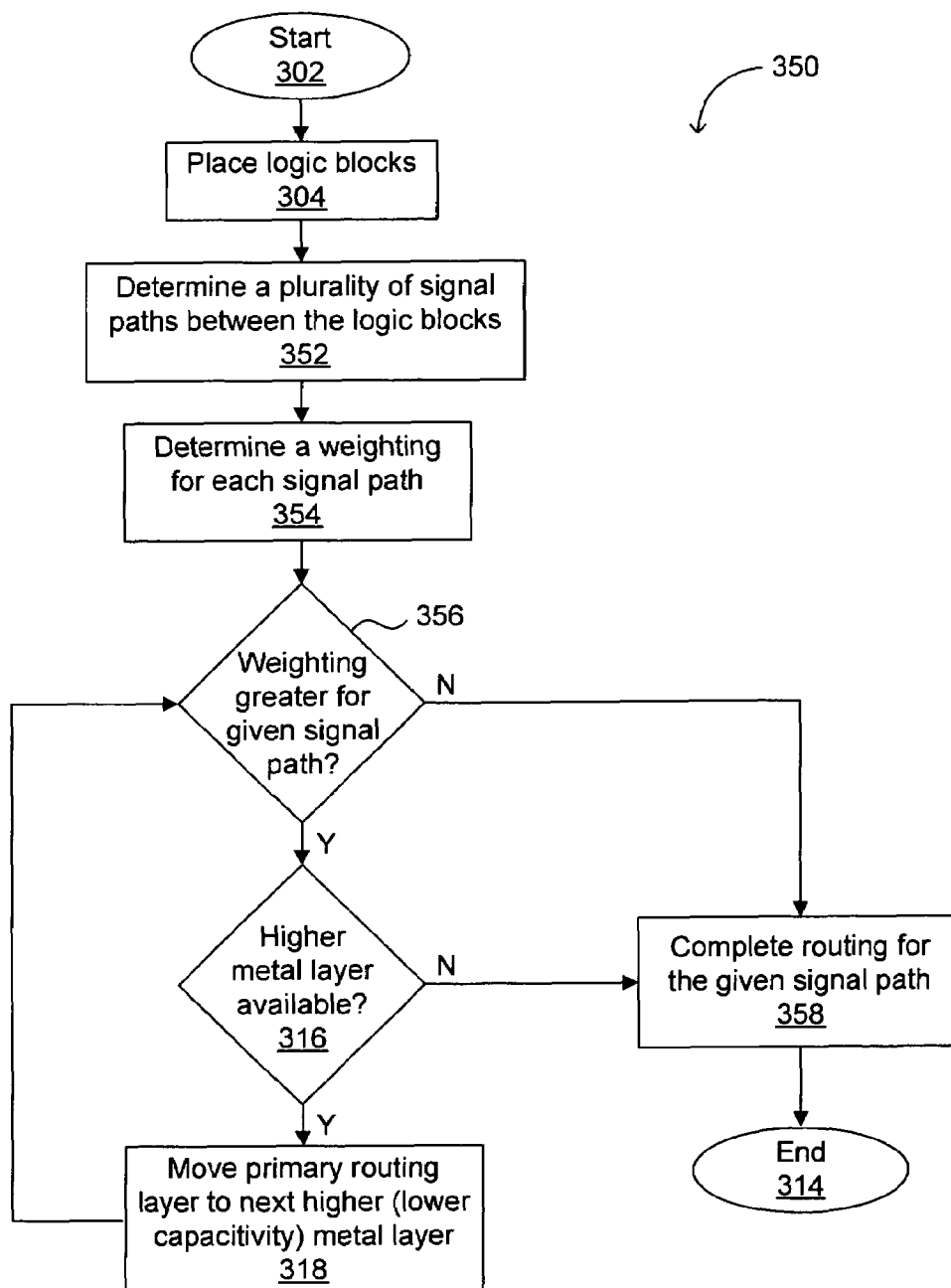


FIG. 3B

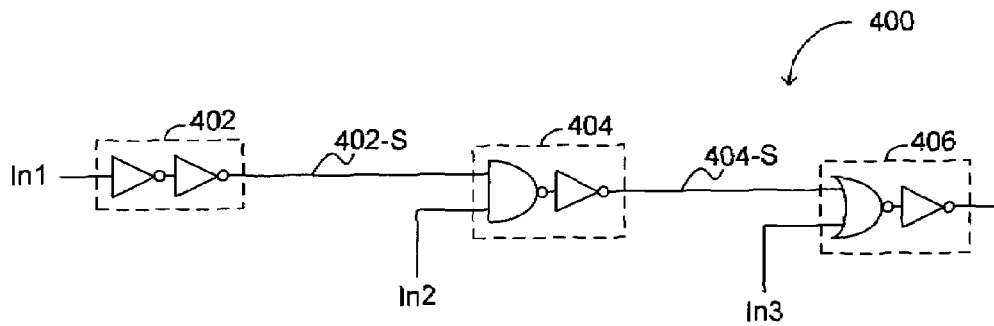


FIG. 4A

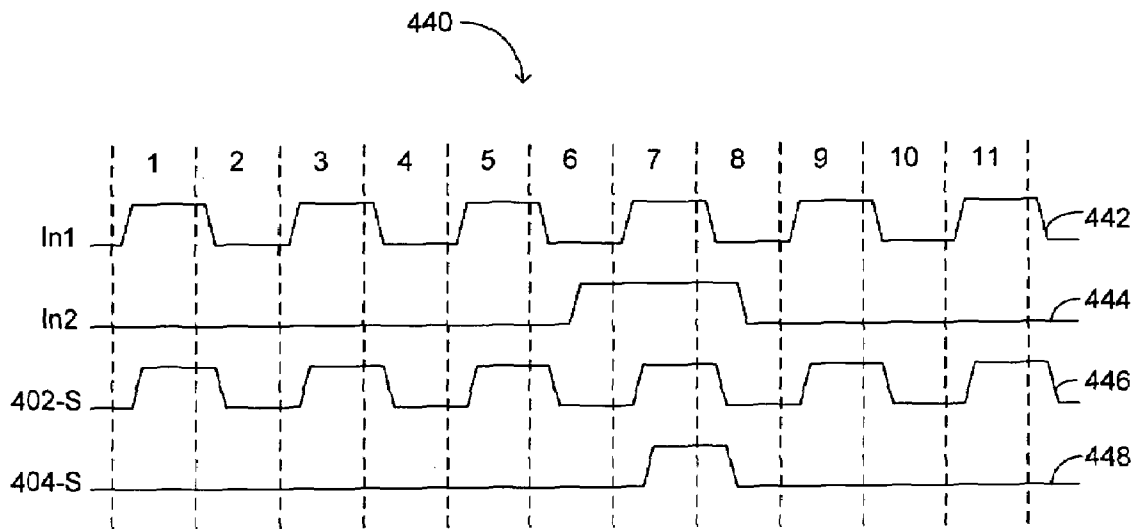
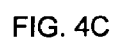


FIG. 4B





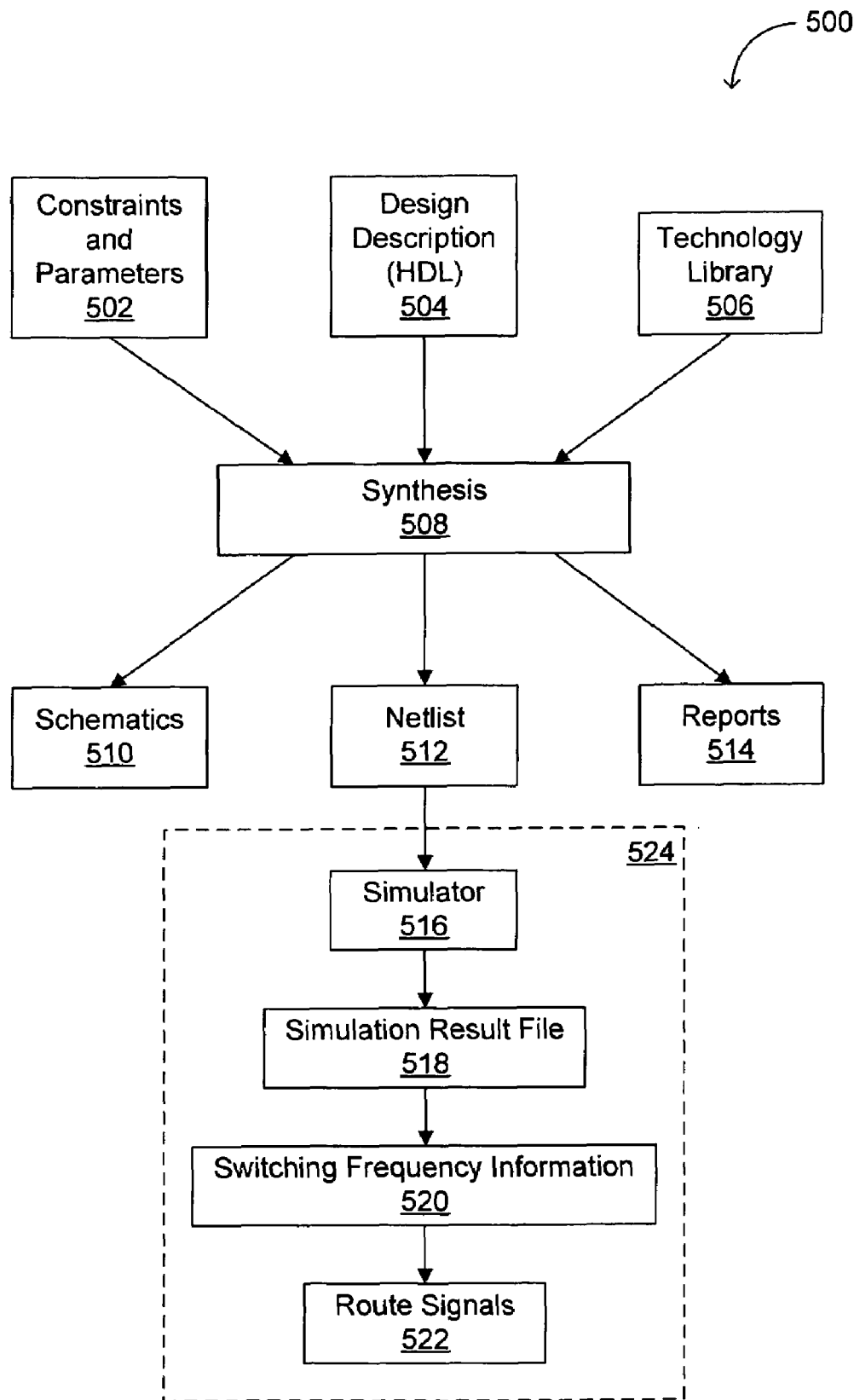


FIG. 5

US 7,260,804 B1

1

## METHOD FOR CIRCUIT BLOCK ROUTING BASED ON SWITCHING ACTIVITY

### FIELD OF THE INVENTION

The present invention generally relates to the field of circuit design, particularly integrated circuit (IC) design. More specifically, embodiments of the present invention pertain to methods, algorithms, software, systems and architectures for reducing power consumption and improving signal integrity in the design of an IC.

### DISCUSSION OF THE BACKGROUND

In typical circuit design, circuit components are arranged to optimize space and/or circuit performance. Such arrangements can include the "layout" or pattern definition of each of the layers used in a semiconductor manufacturing process. For example, such layout can include metal interconnect or connectivity layers that are converted to masks or reticles for use in a wafer fabrication facility that manufactures ICs (i.e., "chips").

While some circuits are designed using "custom" layout, others are designed using a partially or fully automated design flow. Application-Specific Integrated Circuit (ASIC) designs, as well as other functional blocks within a larger chip, such as System-On-Chip (SOC) designs, may employ custom and/or ASIC type flows on the same chip. In any event, typical ASIC flows use "place-and-route" tools for placing logic or circuit "blocks" and then "routing" or connecting the interface signals between the blocks. Such routing between circuit blocks is typically done using one or more metal connectivity layers.

Referring now to FIG. 1A, a conventional connection layer cross section diagram is shown and indicated by the general reference character 100. The five metal layers shown include metal-1 (M1) 102, metal-2 (M2) 106, metal-3 (M3) 110, metal-4 (M4) 114, and metal-5 (M5) 118. Dielectric 104 isolates the M1 connectivity layer, dielectric 108 isolates the M2 connectivity layer, dielectric 112 isolates the M3 connectivity layer, dielectric 116 isolates the M4 connectivity layer, and dielectric 120 isolates the M5 connectivity layer. In FIG. 1B, layer-to-layer connections associated with the diagram of FIG. 1A are shown and indicated by the general reference character 150. In FIG. 1B, contact (C) 152 connects M1 to a layer below, via-1 (V1) 154 connects M2 to M1, via-2 (V2) 156 connects M3 to M2, via-3 (V3) 158 connects M4 to M3, and via-4 (V4) 160 connects M5 to M4. In conventional automated signal path routing approaches, either certain connectivity layers are strictly designated for specific signal categories (e.g., M5 for power signal routing, M4 for clock signals, etc.) to restrict routing choices, or the routing is randomized with respect to the connectivity layer so as to emphasize minimized layout area.

However, such conventional approaches to automated signal path routing are typically not optimized for power consumption or signal integrity concerns. Limitations of such conventional approaches result from the routing not being done with sufficient consideration of the "capacitance" (i.e., capacitance per unit length or area) and the switching activity of the signal path. Accordingly, a signal path routing using a conventional approach may not minimize the capacitance for a high switching activity signal.

Given the increasing demands on circuit designers to create chips of increasing density, decreasing wire and transistor widths, and decreasing power supply and power consumption, it is difficult to ensure optimal signal path

2

routing in a manner that also takes steps to minimize power consumption, particularly in an automated routing flow. Increasing the complexity, flexibility and/or functionality of the circuitry on a chip exacerbates these challenges. Thus, what is needed is a tool with which integrated circuit designers can automatically optimize signal path routing so as to reduce power consumption and increase signal integrity.

### SUMMARY OF THE INVENTION

Embodiments of the present invention relate to methods, algorithms, software, architectures and/or systems for routing signals or wires between circuit blocks in a circuit design.

In one embodiment, a method of routing can include: (i) determining a switching activity for signal path between a first circuit block and a second circuit block; and (ii) routing the signal path substantially in a connectivity layer related to the switching activity of the signal path. The circuit blocks can include standard cells configured to implement a logic or timing function, other components, and/or integrated circuits, for example. The switching activity can include a switching frequency determination based on simulation results of the signal path between the circuit blocks.

Embodiments of the present invention can advantageously reduce power consumption as well as supply noise by optimally routing signal paths between circuit blocks in an automated place-and-route flow. Further, signal integrity problems due to non-optimal routing can be reduced or minimized relative to conventional techniques. Embodiments of the invention are suitable for the automated routing of signal paths between circuit blocks within an integrated circuit (IC) and/or routing between ICs or components on a board, such as a printed circuit board (PCB).

These and other advantages of the present invention will become readily apparent from the detailed description of preferred embodiments below.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is a conventional connection layer cross section diagram showing metal layers.

FIG. 1B is a conventional connection layer cross section diagram showing layer-to-layer connections.

FIG. 2A is a box diagram showing circuit block signal path connections that may be used in embodiments of the present invention.

FIG. 2B is a schematic diagram showing an exemplary signal path routing for the circuit of FIG. 2A resulting from the use of embodiments of the present invention.

FIG. 3A is a flow diagram showing a signal path routing method according to an embodiment of the present invention.

FIG. 3B is a flow diagram showing a signal path routing method according to an alternate embodiment of the present invention.

FIG. 4A is schematic diagram showing an exemplary circuit that may be used in embodiments of the present invention.

FIG. 4B is an exemplary timing diagram for the circuit of FIG. 4A.

FIG. 4C is a schematic diagram showing a signal path routing for the circuit of FIG. 4A resulting from the use of embodiments of the present invention.

FIG. 5 is a box diagram showing a synthesis flow adapted for use with embodiments of the present invention.

US 7,260,804 B1

3

DETAILED DESCRIPTION OF THE  
PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be readily apparent to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail so as not to unnecessarily obscure aspects of the present invention.

Some portions of the detailed descriptions which follow are presented in terms of processes, procedures, logic blocks, functional blocks, processing, and other symbolic representations of operations on code, data bits, data streams or waveforms within a computer, processor, controller and/or memory. These descriptions and representations are generally used by those skilled in the data processing arts to effectively convey the substance of their work to others skilled in the art. A process, procedure, logic block, function, process, etc., is herein, and is generally, considered to be a self-consistent sequence of steps or instructions leading to a desired and/or expected result. The steps generally include physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical, magnetic, optical, or quantum signals capable of being stored, transferred, combined, compared, and otherwise manipulated in a computer or data processing system. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, waves, waveforms, streams, values, elements, symbols, characters, terms, numbers, or the like, and to their representations in computer programs or software as code (which may be object code, source code or binary code).

It should be borne in mind, however, that all of these and similar terms are associated with the appropriate physical quantities and/or signals, and are merely convenient labels applied to these quantities and/or signals. Unless specifically stated otherwise and/or as is apparent from the following discussions, it is appreciated that throughout the present application, discussions utilizing terms such as "processing," "operating," "computing," "calculating," "determining," "manipulating," "transforming," "displaying" or the like, refer to the action and processes of a computer or data processing system, or similar processing device (e.g., an electrical, optical, or quantum computing or processing device), that manipulates and transforms data represented as physical (e.g., electronic) quantities. The terms refer to actions and processes of the processing devices that manipulate or transform physical quantities within the component (s) of a system or architecture (e.g., registers, memories, other such information storage, transmission or display devices, etc.) into other data similarly represented as physical quantities within other components of the same or a different system or architecture.

Furthermore, in the context of this application, the terms "net list" (or "netlist") and "hardware description" may be

4

used interchangeably to refer to a circuit design represented in an appropriate language, such as VERILOG simulation language, Hardware Description Language (HDL) or VERILOG HDL (VHDL; VERILOG is a registered trademark of Gateway Design Automation Corporation for computer aided electrical engineering programs). Similarly, the terms "wire," "wiring," "line," "signal," "conductor" and "bus" refer to any known structure, construction, arrangement, technique, method and/or process for physically transferring a signal from one point in a circuit to another. Also, unless indicated otherwise from the context of its use herein, the terms "known," "fixed," "given," "certain" and "predetermined" generally refer to a value, quantity, parameter, constraint, condition, state, process, procedure, method, practice, or combination thereof that is, in theory, variable, but is typically set in advance and not varied thereafter when in use.

Similarly, for convenience and simplicity, the terms "clock," "time," "timing," "rate," "period" and "frequency" are, in general, interchangeable and may be used interchangeably herein, but are generally given their art-recognized meanings. Also, for convenience and simplicity, the terms "data," "data stream," "waveform" and "information" may be used interchangeably, as may (a) the terms "flip-flop," "latch" and "register," and (b) the terms "connected to," "coupled with," "coupled to," and "in communication with," but these terms are generally given their art-recognized meanings herein.

The present invention concerns a method and/or algorithm (e.g., a computer-readable set of instructions) for routing signal paths or connections between circuit blocks, and can include: (i) determining a switching activity for a signal path between first and second circuit blocks; and (ii) routing the signal path substantially in a connectivity layer related to the switching activity of the signal path. The circuit blocks can include standard cells configured to implement a logic or timing function, other components, and/or integrated circuits, for example. The switching activity can include a switching frequency determination based on simulation results of the signal path between the circuit blocks.

In a further aspect of the invention, software relates to a medium or waveform containing a computer-readable set of instructions, where the instructions can include: (i) determining a weighting of a signal path between first and second circuit blocks; and (ii) routing the signal path substantially in a connectivity layer related to the weighting. The weighting can each include a switching activity factor for the signal paths.

In another aspect of the invention, a method and/or algorithm of connecting can include: (i) placing first and second circuit blocks; (ii) determining a signal path between the first and second circuit blocks; (iii) determining a switching activity for the signal path; and (iv) if the switching activity is above a predetermined value, routing the signal path substantially in a first connectivity layer instead of a second connectivity layer. The first connectivity may have a lower capacitance than the second connectivity layer.

In another aspect of the invention, a connection of circuit blocks can include: (i) a first circuit block coupled to a second circuit block via a signal path; and (ii) a connectivity layer substantially forming the signal path being based on a switching activity of the signal path.

Embodiments of the present invention can advantageously reduce power consumption as well as supply noise by optimally routing signal paths between circuit blocks in an automated place-and-route flow. Further, signal integrity problems due to non-optimal signal path routing can be

## US 7,260,804 B1

5

reduced or minimized. Embodiments of the invention are suitable for the automated routing of signal paths or connections between circuit blocks within an integrated circuit (IC) and/or between ICs or components on a board, such as a printed circuit board (PCB).

The invention further relates to hardware and/or software implementations of the present architecture, method and system. The invention, in its various aspects, will be explained in greater detail below with regard to exemplary embodiments.

Referring now to FIG. 2A, a box diagram showing circuit block signal path connections that may be used in embodiments of the present invention is indicated by the general reference character 200. Logic Block 202 can interface to Logic Block 204 via signal or "signal path" 210. Logic Block 206 can interface to Logic Block 208 via signal path 212. In this example, the switching activity of signal 212 may be higher than the switching activity of signal 210. For example, signal 212 may switch state (i.e., from a "high" or "1" to a "low" or "0" or vice versa) ten times in a given time period. However, in that same given time period, signal 210 may only switch state one time. Because the current drawn from the power supply is proportional to the capacitive load being driven, it is typically desirable to minimize the capacitive load or "capacitance" of the routed connections, particularly for signals that may switch states often (i.e., high "switching activity" signals). According to embodiments of the present invention, the switching activity of each of signal paths 210 and 212 can be determined and compared, either directly or indirectly, with a predetermined threshold value or with each other so as to minimize the capacitance of the signal path routing.

Referring now to FIG. 2B, a schematic diagram showing an exemplary signal path routing for the circuit of FIG. 2A resulting from the use of embodiments of the present invention is indicated by the general reference character 250. Following the example of FIG. 2A, signal path 210 may have a relatively low switching activity. Accordingly, signal path 210 may be routed substantially in a relatively high capacitance layer, such as metal-1 (M1). As shown in FIG. 2B, signal path 210 may include a connection from Logic Block 202 to the M1 layer through a contact (CA). Most of the signal path length can be routed in M1 and the connection to Logic Block 204 can be made through another contact (CB). Of course, as one skilled in the art will recognize, signal path 210 may also be routed partially in another connectivity layer, such as a higher layer (e.g., metal-2 (M2)), based on process technology (e.g., design rules restricting maximum routing in a connectivity layer) and/or design constraints without departing from the scope of the present invention.

Signal path 212, however, may have a relatively high switching activity. Accordingly, signal path 212 may be routed substantially in a relatively low capacitance layer, such as metal-4 (M4). Signal path 212 can include connections from Logic Block 206 to M4 through a contact (CA), a via-1 (V1A), a via-2 (V2A), and a via-3 (V3A). Most of the signal path length can be routed in M4 and the connection to Logic Block 208 can be completed through via-3 (V3B), via-2 (V2B), via-1 (V1B), and contact (CB) connections. Of course, as one skilled in the art will recognize, signal path 212 may also be routed partially in another connectivity layer, such as a higher layer (e.g., metal-5 (M5)) or a lower layer (e.g., metal-3 (M3)), based on process technology (e.g., design rules restricting maximum routing in a connectivity layer) and/or design constraints without departing from the scope of the present invention.

6

In this fashion, a signal path can be routed between circuit or logic blocks, or other routing termination points (e.g., ports or other designations for subsequent signal connections), relative to a switching activity of the signal path.

Accordingly, the capacitance of signal paths for certain higher switching activity signals can typically be reduced by routing substantially on lower capacitance layers. Thus, the overall power consumption of a circuit can effectively be reduced by the use of embodiments of the present invention. In one implementation, a power reduction of about 3-4% was realized. Further, signal integrity problems (e.g., due to power supply noise) can also be reduced or minimized due to increased power supply stability. Also, a particularly advantageous application for embodiments of the present invention involves routing clock signals or other high switching activity type signals in a highest available connectivity layer.

Of course, as one skilled in the art will recognize, embodiments of the present invention are also applicable to analog, ternary, or other non-digital circuits. As one example, "small-signal" circuits, either alone or embedded within a larger chip or PCB may employ embodiments of the present invention. In general, embodiments of the present invention can be used in the routing of signal paths between circuit blocks or other routing termination points having interface signals that change states. Further, such state changes suitable for a "switching activity" determination may be of any type (e.g., analog, digital, etc.) recognizable by the interfacing or surrounding circuitry.

Referring now to FIG. 3A, a flow diagram showing a signal path routing method according to an embodiment of the present invention is indicated by the general reference character 300. The flow can begin in Start 302 and logic blocks or the like can be placed (304). Next, a signal path can be determined between the logic blocks (306). Of course, any appropriate signal path suitable for automated routing can be determined. Such a determination of an "interface" between logic blocks can be made by reference to a "netlist" file. Netlist files can be generated, for example, by a synthesizer based on a Hardware Description Language (HDL) representation of the logic functions of a circuit (which generally includes the logic blocks of the circuit), as will be discussed in more detail below with reference to FIG. 5.

In FIG. 3A, switching activity information for the signal path may next be accessed (308). Such switching activity information can include a switching frequency based on an event-driven simulation, such as a VERILOG simulation. Further, the switching activity information can include a user-controlled factor that may be multiplied with a switching activity (i.e., switching frequency) factor, as shown in formula (1), as follows:

$$\text{weight}(\text{net}) = \text{length}(\text{net}) + P * \text{Sw}(\text{net}) \quad (1)$$

The result term "weight(net)" can be a weighting so as to designate the relative routing or connectivity layer of a signal path. The term "length(net)" can be an initial length of the signal path, such as may be determined by a distance between logic block placements or other routing termination points. Alternatively, "length(net)" can represent a current or a projected length of a signal path due to other routing constraints, for example. The term "P" in the above formula may be the user-controlled factor. The user-controlled factor can be a representation of the importance or priority of a particular signal path relative to other signal paths. For example, a clock signal may have a high priority designation by a user. Further, the term "Sw(net)" can be a switching



US 7,260,804 B1

7

frequency or switching activity term, for example. As discussed above, this term can be determined by way of simulation of a netlist representation of the overall circuit, for example.

The weighting ("weight(net)") can be used as a more detailed measure of the "switching activity" of a signal path so as to determine an optimized substantial routing layer. Accordingly, a primary or substantial routing layer can be changed according to embodiments of the present invention by comparing the weighting for a signal path against a predetermined value. In an alternate embodiment, a more direct "switching activity" measure, such as strictly the "Sw(net)" term can be used to compare against the predetermined or threshold value to obtain an optimal routing layer for a given signal path.

Continuing with FIG. 3A, the switching activity can be compared against a predetermined or "threshold" value (310). The threshold may be different for each connectivity layer or a same threshold value may be used for each of the connectivity layers. If the switching activity is below the threshold, the routing for the signal path can be completed substantially in the current connectivity layer (312) and the flow can complete in End 314. However, if the switching activity is above the designated threshold, the automated router flow can look to see if a higher layer of connectivity is available (316). This can include a higher metal layer (i.e., lower capacitance layer). If no higher layer is available, the signal path can be completed substantially in the current connectivity layer (312) and the flow can complete in End 314. No further layers may be available due to either all connectivity layers in the process technology being used in the current signal path route or where the top one or two metal layers (e.g., metal-7 and metal-8 in an eight metal layer process) are reserved for power supply routing, for example. If, however, a higher metal layer is available, the primary routing layer can be moved to the next higher layer (i.e., lower capacitance layer) (318) and the flow can return to decision box 310.

In this fashion, a signal path can be routed in a connectivity layer optimized based on the switching activity of the signal path. Further, the routing can also be made dependent on a user-controlled factor as well as an initial and/or projected signal path length.

Referring now to FIG. 3B, a flow diagram showing a signal path routing method according to an alternate embodiment of the present invention is indicated by the general reference character 350. For blocks or elements serving the same or similar functions as those of FIG. 3A, the same block number is used. Accordingly, blocks 302, 304, 314, 316, and 318 are the same or similar to the corresponding blocks shown in FIG. 3A.

In the alternate embodiment of FIG. 3B, once the logic blocks are placed (304), a plurality of signal paths between the logic blocks can be determined (352). A weighting for each of the signal paths can be determined (354) in similar fashion as discussed above. For a given signal path (e.g., a signal path undergoing automated routing), a weighting for the given signal path can be compared against a weighting for another signal path (356). If the weighting for the given signal path is less than the weighting of the other signal path in the comparison, the routing can be completed for the given signal path (358) and the flow can complete in End 314. If, however, the weighting for the given signal path is greater than the other signal path in the comparison, a determination of whether a higher layer is available for routing can be made (316). If no higher layer is available, the routing for the given signal path can be completed (358) and

8

the flow can complete in End 314. If there is a higher layer available for routing, the routing for the given signal path can be moved to the next higher layer (318) and the flow can return to the weighting comparison (356), as discussed above.

Referring now to FIG. 4A, a schematic diagram showing an exemplary circuit that may be used in embodiments of the present invention is indicated by the general reference character 400. This example shows a simple circuit structure using standard cells or gates to implement logic or other functions that is suitable for IC design. Such logic functions could include AND/NAND, OR/NOR, XOR/XNOR, INV, or flip-flops, as just a few examples. In practice, any circuit can be designed and treated as a "standard cell" for automatic placement and routing in a larger design. More commonly, a set of standard cells are provided and characterized for each design technology and are utilized in an "off-the-shelf" manner in a typical ASIC design flow.

In the example of FIG. 4A, standard cell 402 can be a buffer stage receiving input In1 and outputting signal 402-S. Standard cell 404 can be an "AND" function having a NAND-gate followed by an inverter. Standard cell 404 can receive signal 402-S and input In2 and can output signal 404-S. Standard cell 406 can be an "OR" function having a NOR-gate followed by an inverter. Standard cell 406 can receive signal 404-S and input In3. Embodiments of the present invention can be used to determine an optimized routing for signal paths 402-S and 404-S based on their respective switching activities. Consistent with such embodiments, a simulation of circuit 400 may be done to determine the switching activity of signals 402-S and 404-S.

Referring now to FIG. 4B, an exemplary timing diagram for the circuit of FIG. 4A is shown and indicated by the general reference character 440. Such a timing diagram can be a waveform representation of a VERILOG simulation result, such as a Value Change Data (VCD) file, for example. Input In1 (waveform 442) can be an oscillating signal, such as a clock, and may go high (i.e., transition from "0" to "1") in odd cycles and go low (i.e., transition from "1" to "0") in even cycles. Input In2, which may be a clock enable signal, for example, can go high in cycle 6 and go low in cycle 8, as shown by waveform 444. Signal 402-S (waveform 446) can be a simple delay of In1 because signal 402-S is the output of buffer stage 402. Signal 404-S can go high in cycle 7 and go low in cycle 8 to reflect the "AND" function of standard cell 404. Thus, over the time period of 11 cycles shown in FIG. 4B, the switching activity of signal 402-S is six times the switching activity of signal 404-S (i.e., six full switching cycles for 402-S versus only one switching cycle for 404-S).

The switching activity of various signals in a circuit, where that circuit has been simulated, can also be determined using a commercially available or custom software tool. For example, if the circuit simulation is done using VERILOG simulation language, a VCD file can be created as an output file. A switching activity interface (SAIF) can be used to determine the switching activity of each signal or "net" in the circuit. An example of a free utility for conversion of a VCD output to SAIF is the "vcd2saif" script, which is available from Synopsys, Inc., of Mountain View, Calif. ([www.synopsys.com](http://www.synopsys.com); in particular, see [www.synopsys.com/partners/tapin/saif.html](http://www.synopsys.com/partners/tapin/saif.html)).

Referring now to FIG. 4C, a schematic diagram showing a signal path routing for the circuit of FIG. 4A resulting from the use of embodiments of the present invention is indicated by the general reference character 480. Based on the switching activity of signals 402-S and 404-S in the above

US 7,260,804 B1

9

example, signal path **402-S** can be routed substantially in a relatively low capacitivity layer (e.g., metal-**4** (**M4**)) and signal path **404-S** can be routed in a relatively high capacitivity layer (e.g., metal-**1** (**M1**)). Signal path **402-S** can include connections from standard cell **402** to **M4** through a contact (**CA**), a via-**1** (**V1A**), a via-**2** (**V2A**), and a via-**3** (**V3A**). Most of the signal path length can be routed in **M4** and the connection to standard cell **404** can be completed through via-**3** (**V3B**), via-**2** (**V2B**), via-**1** (**V1B**), and contact (**CB**) connections. Signal path **404-S** may include a connection from standard cell **404** to the **M1** layer through a contact (**CA**). Most of the signal path length can be routed in **M1** and the connection to standard cell **406** can be made through another contact (**CB**).

In this fashion, power consumption due to driving the relatively high switching frequency signal **402-S** can be reduced or minimized. Further, the signal integrity of all signals affected by localized power supply noise in the region of standard cells **402**, **404**, and **406** can be improved because such noise can be reduced or minimized according to embodiments of the present invention.

While the exemplary circuit block arrangements discussed above generally show the routing of signal paths between circuit blocks, these illustrations should not be considered limiting. As one skilled in the art will recognize, such routing may be accomplished between any two or more designated points and embodiments of the present invention are equally adaptable to such applications. Further, the routing can be done on any type of connectivity layer, including polysilicon. In one embodiment, such routing can be done for multiple connections to a common line, such as a clock signal, based on the signal switching activity. In any event, in accordance with embodiments of the present invention, any signal paths may be routed substantially in a layer in relation to the switching activity of the signal path.

Referring now to FIG. 5, a box diagram showing a synthesis flow adapted for use with embodiments of the present invention is indicated by the general reference character **500**. Box **524** shows elements adapted for use in accordance with embodiments of the present invention. The remaining boxes in FIG. 5 represent a conventional synthesis flow. Inputs to Synthesis **508** typically include Constraints and Parameters **502**, Design Description (HDL) **504**, and Technology Library **506**. Constraints and Parameters **502** may include physical expectations of the design, such as the circuit operating speed and/or the circuit layout area. Design Description (HDL) **504** can be a VERILOG HDL (VHDL) description of the logic operation(s) for synthesis. Technology Library **506** may contain a functional description as well as other information, such as may be related to the area and speed of all standard cells in a given process technology. For example, Technology Library **506** may be specific to a technology generation (e.g., 0.13 micron technology), a company (e.g., TSMC), and a process type (e.g., CMOS; eight-level metal; fast/normal/slow lot variation).

Outputs from Synthesis **508** may include Schematics **510**, Netlist **512**, and Reports **514**. Schematics **510** can be schematic representations of the synthesized functions of Design Description (HDL) **504**. Netlist **512** can be a text file description of a physical connection of components, such as standard cells, and can include a description of the various circuit blocks in the design and signal paths between the circuit blocks. Reports **514** can include speed and area data associated with results of Synthesis **508**.

As discussed above, a netlist representation (e.g., Netlist **512**) may be used for simulation to determine the switching activity of various signals. Accordingly, Simulator **516** can

10

receive Netlist **512** and provide Simulation Result File **518**. For example, Simulator **516** can be a VERILOG simulator and Simulation Result File **518** can be a VCD file. Simulation Result File **518** can be used to determine Switching Frequency Information **520**. As discussed above, this can be accomplished by the use of a "vcd2saif" utility, for example. Finally, Route Signals **522** can receive Switching Frequency Information **520** so as to make optimized signal path routes based on the switching activity of the associated signals.

In this fashion, a conventional ASIC type design flow including synthesis can be adapted for routing of signal paths between standard cells in accordance with embodiments of the present invention. Alternatively, embodiments of the present invention may be used in other design flows whereby a switching activity of signals can be determined via simulation or other means.

Further examples of suitable systems, tools and/or methods in which the present invention is generally applicable include those described in, e.g., U.S. Pat. Nos. 6,080,201 and 5,798,936, the relevant portions of which are each incorporated herein by reference, and those commercially available from place-and-route software vendors such as Cadence Design Systems (e.g., the SILICON ENSEMBLE™, SILICON ENSEMBLE-PKS™, FIRST ENCOUNTER™, and NANO ENCOUNTER™ tools), Silicon Valley Research, Inc. (e.g., the QIC/APR™, GARDS™, SCT™ and FLOORPLACER™ tools), Synopsys (e.g., the CHIP ARCHITECT™, DESIGN COMPILER™, and FLOORPLAN COMPILER™ tools) and Mentor Graphics (e.g., the AUTOCELLS™ tool).

Thus, embodiments of the present invention can advantageously reduce power consumption as well as supply noise by optimally routing signal paths between circuit blocks in an automated place-and-route flow. Further, signal integrity problems due to non-optimal signal path routing can be reduced or minimized. Embodiments of the invention are suitable for the automated routing of signal paths between circuit blocks within an IC and/or routing between ICs or components on a board, such as a printed circuit board (PCB).

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents.

What is claimed is:

1. A method of routing, comprising the steps of:

- a) assigning a first switching activity threshold value to a lower connectivity layer and a second switching activity threshold value to a higher connectivity layer, wherein said second threshold value is higher than said first threshold value;
- b) determining a switching activity for a signal path between a first circuit block and a second circuit block;
- c) selecting said higher connectivity layer instead of said lower connectivity layer if said switching activity for said signal path is above said first threshold value and below said second threshold value; and

## US 7,260,804 B1

11

d) when said higher connectivity layer is selected, routing said signal path substantially in said higher connectivity layer.

2. The method of claim 1, wherein the step of determining said switching activity occurs prior to the step of routine said signal path.

3. The method of claim 1, further including the step of determining said signal path.

4. The method of claim 3, wherein the step of determining said signal path includes matching said signal path to a corresponding one of a plurality of nets in a netlist describing said first and second circuit blocks.

5. The method of claim 4, wherein the step of determining said switching activity includes simulating using said netlist.

6. The method of claim 5, wherein the step of determining said switching activity further includes converting an output file from said simulating to a switching activity file.

7. The method of claim 6, wherein said switching activity file includes a frequency of switching for said signal path over a predetermined time period.

8. The method of claim 7, wherein the step of selecting includes selecting said higher connectivity layer in response to a length of said signal path, a user-controlled factor, and said frequency of switching.

9. The method of claim 1, wherein each of said circuit blocks includes a standard cell configured to implement a logic or timing function.

10. The method of claim 5, wherein said simulating includes an event-based logic simulation.

11. The method of claim 10, wherein said event-based logic simulation includes a VERILOG simulation.

12. The method of claim 9, further including the step of accessing a technology library having a characterization of said standard cell.

13. The method of claim 1, wherein said higher connectivity layer is configured for lower capacitance than said lower connectivity layer.

14. The method of claim 1, further including the step of synthesizing a circuit implementation in response to a hardware description.

15. The method of claim 1, wherein each of the circuit blocks includes an integrated circuit or component.

16. The method of claim 1, wherein said second circuit block includes a routing termination.

17. A computer-readable medium containing a set of instructions for execution on a computer, the instructions comprising the steps of:

a) assigning a first weighting threshold value to a lower connectivity layer and a second weighting threshold value to a higher connectivity layer, wherein said second threshold value is higher than said first threshold value;

b) determining a weighting of a signal path between first and second circuit blocks;

c) selecting said higher connectivity layer instead of said lower connectivity layer if said weighting for said signal path is above said first threshold value and below said second threshold value; and

d) when said higher connectivity layer is selected, routing said signal path substantially in said higher connectivity layer.

18. The medium of claim 17, further comprising at least one instruction for determining said signal path.

19. The medium of claim 18, wherein the step of determining said weighting further includes the step of determining a switching activity factor.

12

20. The medium of claim 19, wherein the step of determining said weighting further includes (i) multiplying said switching activity factor by a user-controlled factor to form a product and (ii) adding said product to a signal path length.

21. The medium of claim 20, wherein the step of determining said signal path occurs prior to the steps of selecting and routing.

22. The medium of claim 21, wherein the step of determining said signal path includes matching said signal path to a corresponding one of a plurality of nets in a netlist describing said first and second circuit blocks.

23. The medium of claim 22, wherein the step of determining said switching activity factor includes simulating using said netlist.

24. The medium of claim 17, wherein each of said circuit blocks includes a standard cell configured to implement a logic or timing function.

25. The medium of claim 17, further including at least one instruction for synthesizing a circuit implementation in response to a hardware description.

26. The medium of claim 17, wherein each of said circuit blocks includes an integrated circuit or component.

27. The medium of claim 17, wherein said second circuit block includes a routing termination.

28. A computer system comprising the medium of claim 17, configured to execute the set of instructions.

29. A method of connecting, comprising the steps of:

a) assigning a first switching activity threshold value to a lower connectivity layer, and a second switching activity threshold value to a higher connectivity layer, wherein said second threshold value is higher than said first threshold value;

b) placing first and second circuit blocks;

c) determining a signal path between said first and second circuit blocks;

d) determining a switching activity for said signal path; and

e) selecting said higher connectivity layer instead of lower connectivity layer if said switching activity is above said first threshold value and below said second threshold value; and

f) when said higher connectivity layer is selected, routing said signal path substantially in said higher connectivity layer.

30. The method of claim 29, wherein the step of determining said signal path includes accessing a netlist created by a synthesizer in response to a hardware description.

31. The method of claim 30, wherein the step of determining said switching activity includes simulating based on said netlist to determine a switching frequency.

32. The method of claim 31, wherein said simulating includes using an event-based logic state simulation.

33. The method of claim 31, wherein the step of determining said switching activity further includes forming a product of said switching frequency and a user-controlled factor.

34. The method of claim 33, wherein the step of selecting further includes comparing a weighting factor for said signal path and said predetermined value, said weighting factor including said product and a length of said signal path.

35. The method of claim 29, wherein said higher connectivity layer is a higher layer than said lower connectivity layer.

36. The method of claim 29, wherein said higher connectivity layer has a lower capacitance than said lower connectivity layer.

## US 7,260,804 B1

## 13

37. The method of claim 29, wherein said first and lower connectivity layers include metal layers.

38. The method of claim 29, wherein said second circuit block includes a routing termination.

39. A computer-readable medium containing a set of 5 instructions for execution on a computer, said instructions adapted to perform the method of claim 29.

40. A computer system comprising the medium of claim 39, configured to execute the set of instructions.

41. A connection of circuit blocks, comprising:

- a) a first circuit block; and
- b) a second circuit block coupled to said first circuit block via a signal path, said signal path being substantially routed in a preferred connectivity layer, said preferred

## 14

connectivity layer selected from a plurality of connectivity layers based at least in part on a switching activity of said signal path and on threshold switching activity values for each of said plurality of connectivity layers.

42. The connection of claim 41, wherein said preferred connectivity layer is selected to reduce a capacitance as said switching activity increases.

43. The connection of claim 41, wherein each of said circuit blocks includes a standard cell configured to implement a logic or timing function.

44. The connection of claim 41, wherein each of said circuit blocks includes an integrated circuit or component.

\* \* \* \* \*



UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 7,260,804 B1  
APPLICATION NO. : 10/946688  
DATED : August 21, 2007  
INVENTOR(S) : Michael Burstein et al.

Page 1 of 1

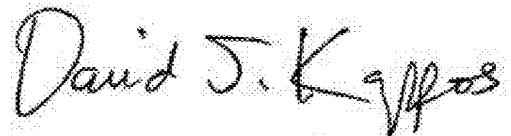
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

IN THE CLAIMS

Claim 2, col. 11, line 5: change “step of routine said signal path” to --step of routing said signal path--.

Claim 34, col. 12, line 60: change “said predetermined value” to --a predetermined value--.

Signed and Sealed this  
Ninth Day of August, 2011

A handwritten signature in black ink that reads "David J. Kappos". The signature is written in a cursive, flowing style.

David J. Kappos  
*Director of the United States Patent and Trademark Office*

# **EXHIBIT B**

(12) **United States Patent**  
**Burstein et al.**

(10) **Patent No.:** **US 7,360,193 B1**  
(45) **Date of Patent:** **Apr. 15, 2008**

(54) **METHOD FOR CIRCUIT BLOCK  
PLACEMENT AND CIRCUIT BLOCK  
ARRANGEMENT BASED ON SWITCHING  
ACTIVITY**

6,662,348 B1 \* 12/2003 Naylor et al. .... 716/9  
6,725,438 B2 4/2004 Van Ginneken

(Continued)

#### OTHER PUBLICATIONS

(75) Inventors: **Michael Burstein**, Cupertino, CA (US);  
**Mikhail Komorov**, Moscow (RU);  
**Georgy Sergeev**, Moscow (RU)

Jim Flynn and Brandon Waldo; Power Management in Complex SoC Design (16 Pages); Apr. 2004; Synopsis, Inc., 700 East Middlefield Rd., Mountain View, CA 94043; <http://www.synopsys.com/sps>.

(73) Assignee: **Golden Gate Technology, Inc.**, San Jose, CA (US)

(Continued)

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 371 days.

*Primary Examiner*—Paul Dinh

*Assistant Examiner*—Suresh Memula

(74) *Attorney, Agent, or Firm*—Andrew D. Fortney; Alec B. Plumb

(21) Appl. No.: **10/946,925**

(57) **ABSTRACT**

(22) Filed: **Sep. 21, 2004**

(51) **Int. Cl.**  
**G06F 17/50** (2006.01)  
**G06F 9/45** (2006.01)  
**G06F 9/455** (2006.01)

(52) **U.S. Cl.** ..... **716/10**; 716/9; 716/6

(58) **Field of Classification Search** ..... 716/9–10,  
716/6

See application file for complete search history.

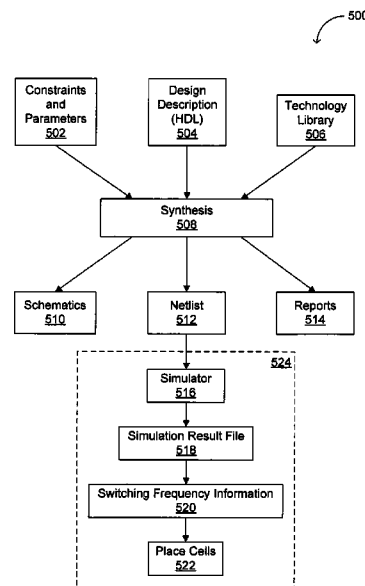
(56) **References Cited**

#### U.S. PATENT DOCUMENTS

6,230,304 B1	5/2001	Groeneveld et al.	
6,253,361 B1	6/2001	Buch	
6,321,183 B1 *	11/2001	Tatsumi	703/14
6,453,446 B1	9/2002	Van Ginneken	
6,496,965 B1	12/2002	Van Ginneken et al.	
6,507,941 B1	1/2003	Leung et al.	
6,530,065 B1 *	3/2003	McDonald et al.	716/4
6,553,338 B1	4/2003	Buch et al.	

A method, algorithm, software, architecture and/or system for placing circuit blocks and/or routing wires in a circuit design is disclosed. In one embodiment, a method of placing can include: (i) determining a first signal path between first and second circuit blocks and determining a second signal path between first and third circuit blocks; and (iii) placing the first circuit block relative to the second and third circuit blocks in a position related to a switching activity of the first and second signal paths. The circuit blocks can include standard cells configured to implement a logic function, other components, or integrated circuits, for example. The switching activity can include a switching frequency determination based on simulation results of the first and second signal paths between the circuit blocks. Embodiments of the present invention can advantageously reduce power consumption as well as supply noise by optimally placing circuit blocks in an automated place-and-route flow. Further, signal integrity problems due to non-optimal circuit block or component placement can be minimized.

**25 Claims, 4 Drawing Sheets**



**US 7,360,193 B1**

Page 2

## U.S. PATENT DOCUMENTS

6,950,998 B1 \* 9/2005 Tuan ..... 716/2  
 7,062,425 B1 \* 6/2006 Bell et al. .... 703/14  
 2004/0015803 A1 \* 1/2004 Huang et al. .... 716/10  
 2004/0049747 A1 \* 3/2004 Yamasaki et al. .... 716/4  
 2004/0073878 A1 \* 4/2004 Hasegawa et al. .... 716/8  
 2004/0150422 A1 \* 8/2004 Wong ..... 326/41  
 2004/0199883 A1 \* 10/2004 Palumbo ..... 716/4  
 2005/0034091 A1 \* 2/2005 Harn ..... 716/6

2006/0031795 A1 \* 2/2006 Rahmat et al. .... 716/5

## OTHER PUBLICATIONS

Astro-Rail: A Comprehensive Power-Integrity Analysis, Implementation and Verification Tool (2 Pages); Data Sheet, May 2003; Synopsis, Inc., 700 East Middlefield Rd., Mountain View, CA 94043.

\* cited by examiner

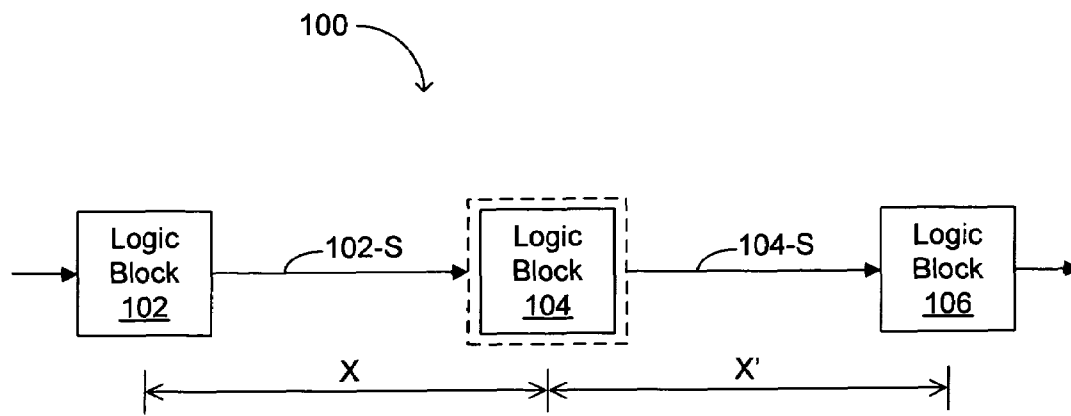


FIG. 1 (conventional)

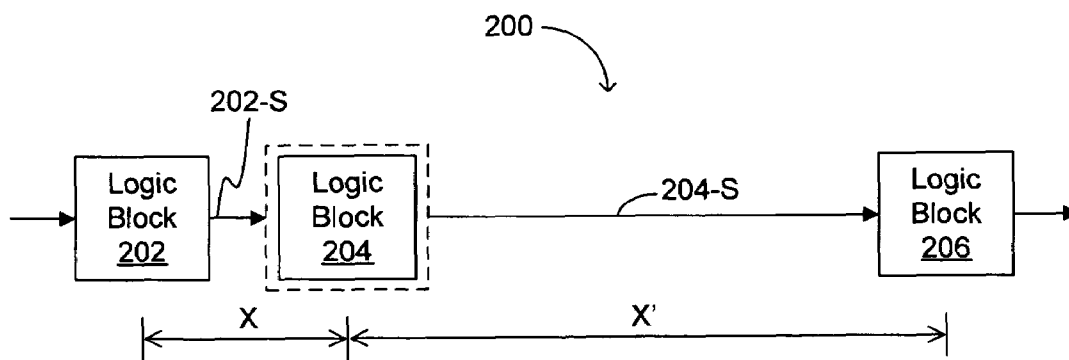


FIG. 2

U.S. Patent

Apr. 15, 2008

Sheet 2 of 4

US 7,360,193 B1

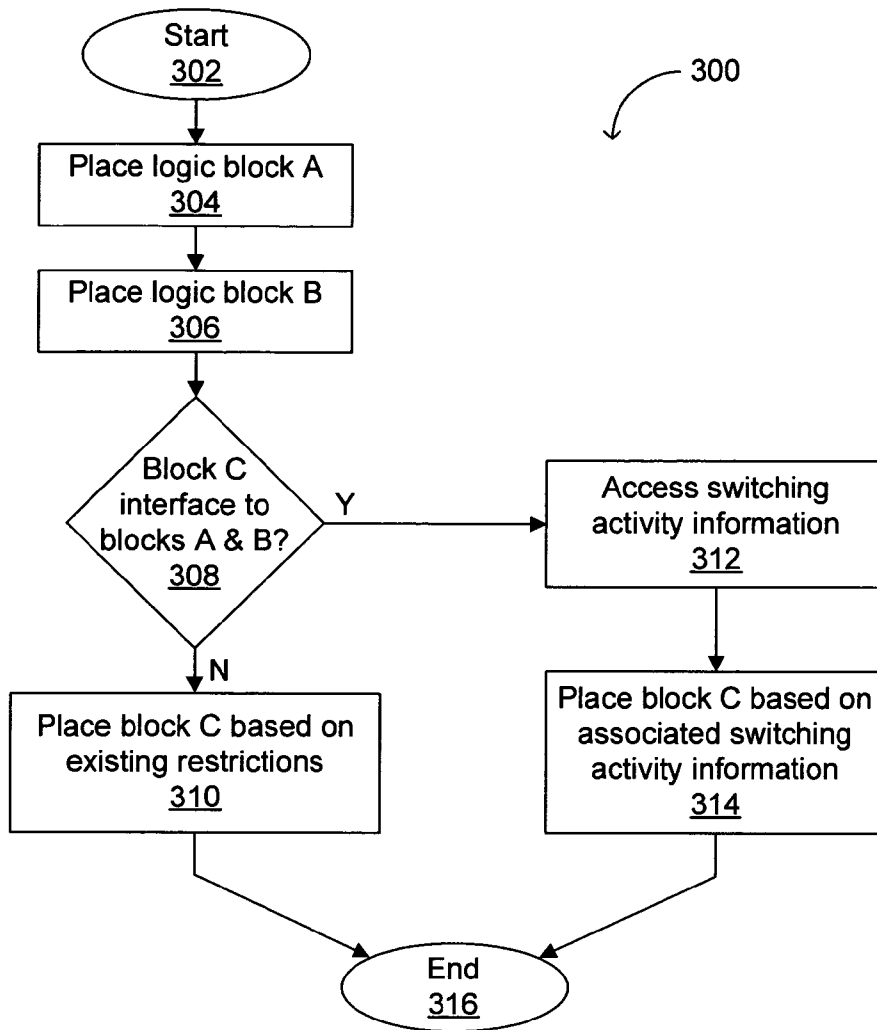


FIG. 3

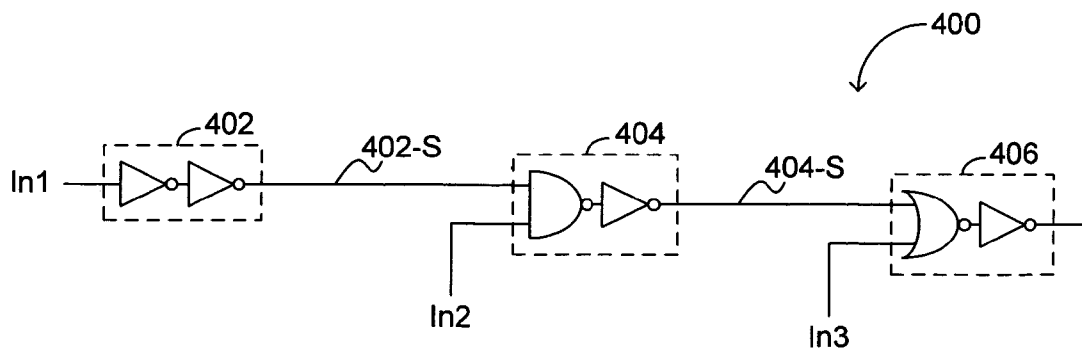


FIG. 4A

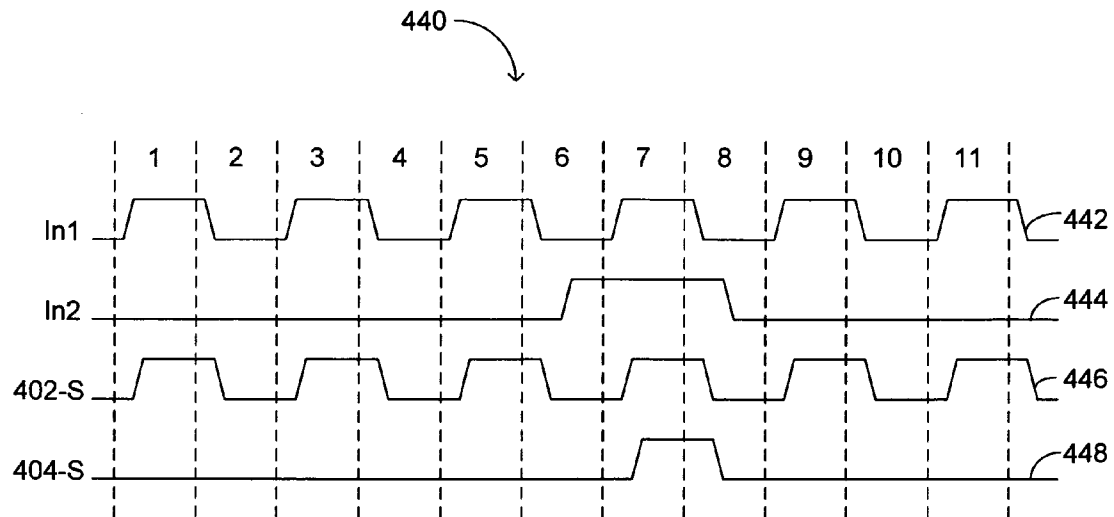


FIG. 4B

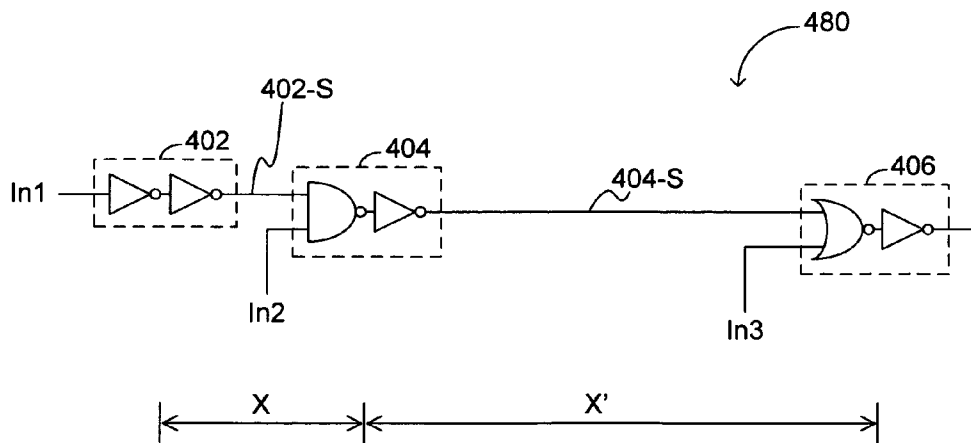


FIG. 4C

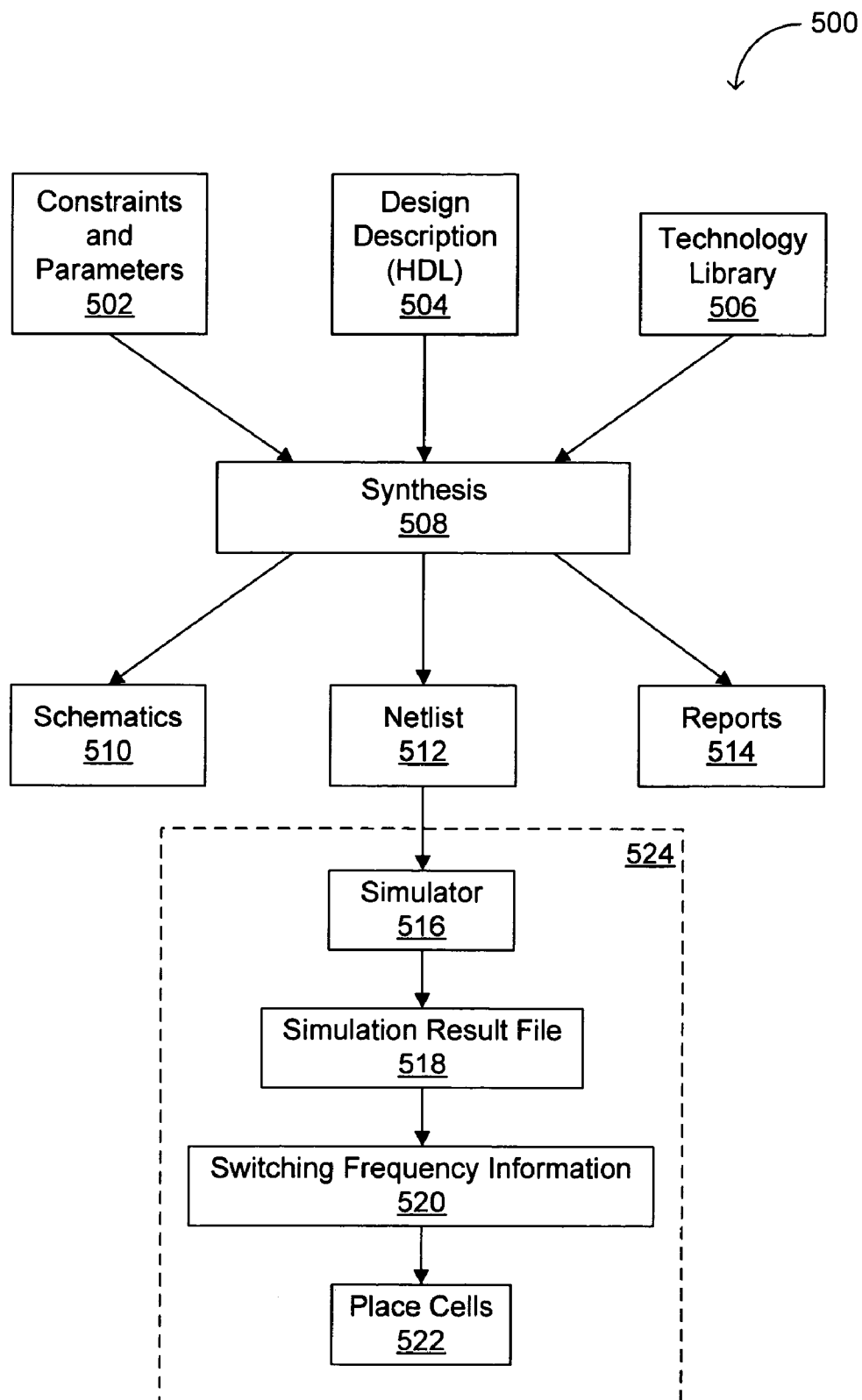


FIG. 5



US 7,360,193 B1

1

# METHOD FOR CIRCUIT BLOCK PLACEMENT AND CIRCUIT BLOCK ARRANGEMENT BASED ON SWITCHING ACTIVITY

## FIELD OF THE INVENTION

The present invention generally relates to the field of circuit design, particularly integrated circuit (IC) design. More specifically, embodiments of the present invention pertain to methods, algorithms, software, systems and architectures for reducing power consumption and improving signal integrity in the design of an IC.

## DISCUSSION OF THE BACKGROUND

In typical circuit design, circuit components are arranged to optimize space and/or circuit performance. Such arrangements can include the "layout" or pattern definition of each of the layers used in a semiconductor manufacturing process. For example, such layout can include metal interconnect layers that are converted to masks or reticles for use in a wafer fabrication facility that manufactures ICs (i.e., "chips").

While some circuits are designed using "custom" layout, others are designed using a partially or fully automated design flow. Application-Specific Integrated Circuit (ASIC) designs, as well as other functional blocks within a larger chip, such as System-On-Chip (SOC) designs, may employ custom and/or ASIC type flows on the same chip. In any event, typical ASIC flows use "place-and-route" tools for placing logic or circuit "blocks" and then "routing" or connecting the interface signals between the blocks.

Referring now to FIG. 1, a box diagram of a circuit block placement resulting from the use of conventional placement tools is shown and indicated by the general reference character 100. Logic Block 102 can interface to Logic Block 104 via signal 102-S. Similarly, Logic Block 104 can interface to Logic Block 106 via signal 104-S. In this example, Logic Block 102 and Logic Block 106 are initially placed by the conventional placement tool. Then, Logic Block 104 is placed. Because of interfaces to both Logic Block 102 and Logic Block 106, the conventional placement tool will place Logic Block 104 either arbitrarily or substantially in the middle between Logic Blocks 102 and 106 (i.e., distance X is about equal to distance X'). One conventional approach, for example, uses a summation of the squares in the interface signal paths to determine the middle location for the placement of Logic Block 104.

However, such conventional approaches to automated block placement are not optimized for power consumption or signal integrity concerns. Limitations of such conventional approaches result from the fact that the switching frequency of signal 102-S is not likely to be the same as that of signal 104-S. Accordingly, the placement of Logic Block 104 substantially in the middle between Logic Blocks 102 and 106 does not necessarily minimize the power being drawn or the supply noise in the situation where the switching frequencies are not equal.

Given the increasing demands on circuit designers to create chips of increasing density, decreasing wire and transistor widths, and decreasing power supply and power consumption, it is difficult to ensure optimal circuit block placement, particularly in an automated placement flow. Increasing the complexity, flexibility and/or functionality of the circuitry on a chip exacerbates these challenges. Thus, what is needed is a tool with which integrated circuit

2

designers can automatically optimize circuit placement so as to reduce power consumption and increase signal integrity.

## SUMMARY OF THE INVENTION

Embodiments of the present invention relate to methods, algorithms, software, architectures and/or systems for placing circuit blocks and/or routing wires in a circuit design.

In one embodiment, a method of placing can include: (i) determining a switching activity for (1) a first signal path between a first circuit block and a second circuit block and (2) a second signal path between the first circuit block and a third circuit block; and (ii) placing the first circuit block relative to the second and third circuit blocks in a position related to a switching activity of the first and second signal paths. The circuit blocks can include standard cells configured to implement a logic function, other components, or integrated circuits, for example. The switching activity can include a switching frequency determination based on simulation results of the first and second signal paths between the circuit blocks.

Embodiments of the present invention can advantageously reduce power consumption as well as supply noise by optimally placing circuit blocks in an automated place-and-route flow. Further, signal integrity problems due to non-optimal circuit block or component placement can be minimized relative to placing the circuit blocks by a summation of the squares (or "middle placement") technique. Embodiments of the invention are suitable for the automated placement of circuit blocks within an integrated circuit (IC) and/or placements of ICs or components on a board, such as a printed circuit board (PCB).

These and other advantages of the present invention will become readily apparent from the detailed description of preferred embodiments below.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a box diagram of a circuit block placement resulting from the use of conventional placement tools.

FIG. 2 is a box diagram of circuit block placement resulting from the use of an embodiment of the present invention.

FIG. 3 is a flow diagram showing a circuit block placement method according to an embodiment of the present invention.

FIG. 4A is schematic diagram showing an exemplary circuit that may be used in embodiments of the present invention.

FIG. 4B is an example timing diagram for the circuit of FIG. 4A.

FIG. 4C is a schematic diagram showing a relative placement of circuit block portions of the circuit of FIG. 4A resulting from the use of embodiments of the present invention.

FIG. 5 is a box diagram showing a synthesis flow adapted for use with embodiments of the present invention.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary,

US 7,360,193 B1

3

the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be readily apparent to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail so as not to unnecessarily obscure aspects of the present invention.

Some portions of the detailed descriptions which follow are presented in terms of processes, procedures, logic blocks, functional blocks, processing, and other symbolic representations of operations on code, data bits, data streams or waveforms within a computer, processor, controller and/or memory. These descriptions and representations are generally used by those skilled in the data processing arts to effectively convey the substance of their work to others skilled in the art. A process, procedure, logic block, function, process, etc., is herein, and is generally, considered to be a self-consistent sequence of steps or instructions leading to a desired and/or expected result. The steps generally include physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical, magnetic, optical, or quantum signals capable of being stored, transferred, combined, compared, and otherwise manipulated in a computer or data processing system. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, waves, waveforms, streams, values, elements, symbols, characters, terms, numbers, or the like, and to their representations in computer programs or software as code (which may be object code, source code or binary code).

It should be borne in mind, however, that all of these and similar terms are associated with the appropriate physical quantities and/or signals, and are merely convenient labels applied to these quantities and/or signals. Unless specifically stated otherwise and/or as is apparent from the following discussions, it is appreciated that throughout the present application, discussions utilizing terms such as "processing," "operating," "computing," "calculating," "determining," "manipulating," "transforming," "displaying" or the like, refer to the action and processes of a computer or data processing system, or similar processing device (e.g., an electrical, optical, or quantum computing or processing device), that manipulates and transforms data represented as physical (e.g., electronic) quantities. The terms refer to actions and processes of the processing devices that manipulate or transform physical quantities within the component(s) of a system or architecture (e.g., registers, memories, other such information storage, transmission or display devices, etc.) into other data similarly represented as physical quantities within other components of the same or a different system or architecture.

Furthermore, in the context of this application, the terms "net list" (or "netlist") and "hardware description" may be used interchangeably to refer to a circuit design represented in an appropriate language, such as VERILOG simulation language, Hardware Description Language (HDL) or VERILOG HDL (VHDL; VERILOG is a registered trademark of Gateway Design Automation Corporation for computer aided electrical engineering programs). Similarly, the terms "wire," "wiring," "line," "signal," "conductor" and "bus" refer to any known structure, construction, arrangement, technique, method and/or process for physically transferring

4

a signal from one point in a circuit to another. Also, unless indicated otherwise from the context of its use herein, the terms "known," "fixed," "given," "certain" and "predetermined" generally refer to a value, quantity, parameter, constraint, condition, state, process, procedure, method, practice, or combination thereof that is, in theory, variable, but is typically set in advance and not varied thereafter when in use.

Similarly, for convenience and simplicity, the terms "clock," "time," "timing," "rate," "period" and "frequency" are, in general, interchangeable and may be used interchangeably herein, but are generally given their art-recognized meanings. Also, for convenience and simplicity, the terms "data," "data stream," "waveform" and "information" may be used interchangeably, as may (a) the terms "flip-flop," "latch" and "register," and (b) the terms "connected to," "coupled with," "coupled to," and "in communication with," but these terms are generally given their art-recognized meanings herein.

The present invention concerns a method and/or algorithm (e.g., a computer-readable set of instructions) for placing circuit blocks, and can include: (i) determining switching activities for a first signal path between first and second circuit blocks and a second signal path between first and third circuit blocks; and (ii) placing the first circuit block relative to the second and third circuit blocks in a position related to a switching activity of the first and second signal paths. The circuit blocks can include standard cells configured to implement a logic function, other components, or integrated circuits, for example. The switching activity can include a switching frequency determination based on simulation results of the first and second signal path between the circuit blocks.

In a further aspect of the invention, the software relates to a medium or waveform containing a computer-readable set of instructions, where the instructions can include: (i) determining a first weighting of a first signal path between first and second circuit blocks and a second weighting of a second signal path between first and third circuit blocks; and (ii) placing the first circuit block relative to the second and third circuit blocks in a position related to the first and second weightings. The weightings can each include a switching activity factor for each of the signal paths.

In another aspect of the invention, a method and/or algorithm of arranging can include: (i) placing first and second circuit blocks; (ii) determining whether a third circuit block interfaces with the first and second circuit blocks; and (iii) if the third circuit block interfaces with the first and second circuit blocks, then: accessing switching activity information for signal paths connecting the third circuit block to the first and second blocks; and placing the third circuit block relative to the first and second circuit blocks in a position related to the switching activity information for the signal paths.

In another aspect of the invention, an arrangement of circuit blocks can include: (i) a first circuit block in a first position and coupled to a third circuit block via a first signal path; (ii) a second circuit block in a second position and coupled to the third circuit block via a second signal path; and (iii) the third circuit block in a third position, the third position being based at least in part on the relative switching activities of the first and second signal paths.

Embodiments of the present invention can advantageously reduce power consumption as well as supply noise by optimally placing circuit blocks in an automated place-and-route flow. Further, signal integrity problems due to non-optimal circuit block or component placement can be

## US 7,360,193 B1

5

minimized. Embodiments of the invention are suitable for the automated placement of circuit blocks within an integrated circuit (IC) and/or placements of ICs or components on a board, such as a printed circuit board (PCB).

The invention further relates to hardware and/or software implementations of the present architecture, method and system. The invention, in its various aspects, will be explained in greater detail below with regard to exemplary embodiments.

Referring now to FIG. 2, a box diagram of circuit block placement resulting from the use of an embodiment of the present invention is shown and indicated by the general reference character 200. Logic Block 202 can interface to Logic Block 204 via signal or "signal path" 202-S. Logic Block 204 can also interface to Logic Block 206 via signal 204-S. In this example, the switching activity of signal 202-S may be higher than the switching activity of signal 204-S. For example, signal 202-S may switch state (i.e., from a "high" or "1" to a "low" or "0" or vice versa) ten times in a given time period. However, in that same given time period, signal 204-S may only switch state one time. Because the current drawn from the power supply is proportional to the capacitive load being driven, it is typically desirable to minimize capacitive loads, particularly on signals that may switch states often (i.e., high "switching activity" signals). According to embodiments of the present invention, the switching activity of signal 202-S can be determined and compared with that of signal 204-S so as to identify a relative position for the placement of Logic Block 204. Thus, in this example, distance X is less than distance X', so as to reduce the capacitance of signal path 202-S, as indicated. Moreover, Logic Block 204 may be placed substantially adjacent to or otherwise in proximity with Logic Block 202.

Of course, as one skilled in the art will recognize, embodiments of the present invention are also applicable to analog, ternary, or other non-digital circuits. As one example, "small-signal" circuits, either alone or embedded within a larger chip or PCB may employ embodiments of the present invention. In general, embodiments of the present invention can be used in the placement of circuit blocks having interface signals that change states. Further, such state changes suitable for a "switching activity" determination may be of any type (e.g., analog, digital, etc.) recognizable by the interfacing or surrounding circuitry.

In this fashion, a circuit or logic block can be placed in a relative position based on the switching activity of associated signals. Accordingly, the capacitance of signal paths for certain higher switching activity signals can typically be reduced. Thus, the overall power consumption of a circuit can effectively be reduced by the use of embodiments of the present invention. In one implementation, a power reduction of about 15-20% was realized. Further, signal integrity problems can also be minimized due to increased power supply stability.

Referring now to FIG. 3, a flow diagram showing a circuit block placement method according to an embodiment of the present invention is indicated by the general reference character 300. The flow can begin in Start 302 and a logic block "A" can be placed (304). Logic block "B" can be placed in 306. In this example, logic blocks A and B may be placed using conventional placement restrictions, such as placement within designated areas or regions on a chip floorplan. Of course, while the placing of logic block B (306) is shown in FIG. 3 as a sequential operation to the placing of logic block A (304), one skilled in the art will recognize that no sequential dependency is implied. In fact,

6

logic block B could be placed prior to logic block A or logic blocks A and B could be placed simultaneously. Next, it can be determined whether the next block to be placed (logic block "C") interfaces to the already-placed logic blocks A and B (308). Such a determination of an "interface" between logic blocks can be made by reference to a "netlist" file. Netlist files can be generated, for example, by a synthesizer based on a Hardware Description Language (HDL) representation of the logic functions of a circuit (which generally includes logic blocks A, B and C), as will be discussed in more detail below with reference to FIG. 5.

In FIG. 3, if logic block C does not interface to logic blocks A and B, then block C can be placed based on existing or conventional restrictions (310) and the flow can complete in End 316. For example, if block C interfaces to block A, but not block B, then logic block C may be placed in the region of block A, but not necessarily between blocks A and B. Similarly, if block C interfaces to block B, but not block A, then logic block C may be placed in the region of block B, but not necessarily between blocks A and B. Such placements may of course be subject to overriding restrictions, such as placement within designated areas or regions on a chip floorplan.

If it is determined that logic block C does interface to already-placed logic blocks A and B, then associated switching activity information can be accessed (312). Such switching activity information can include a switching frequency based on an event-driven simulation, such as a VERILOG simulation. Further, the switching activity information can include a user-controlled factor that may be multiplied with a switching activity (i.e., switching frequency) factor. Next, logic block C can be placed in a relative position based on associated switch activity information (314) and the flow can complete in End 316. The placement of block C in a relative position between, or in proximity with at least one of, blocks A and B can be determined by formula (1), as follows:

$$\text{weight}(\text{net}) = \text{length}(\text{net}) + P * \text{Sw}(\text{net}) \quad (1)$$

The result term "weight(net)" can be a weighting so as to designate the relative position of the new block placement. The term "length(net)" can be an initial length of a signal path, such as may be determined by conventional placement approaches. Alternatively, "length(net)" can represent a current or a projected length of a signal path. The term "P" in the above formula may be the user-controlled factor. The user-controlled factor can be a representation of the importance or priority of a particular signal path relative to other signal paths. For example, a clock signal may have a high priority designation by a user. Further, the term "Sw(net)" can be a switching frequency or switching activity term, for example. As discussed above, this term can be determined by way of simulation of a netlist representation of the overall circuit, for example.

The weighting ("weight(net)") can be used to determine the relative position of a new block placement with respect to existing block placements, such as Logic Block 204 relative to Logic Blocks 202 and 206, as discussed above with reference to FIG. 2. Accordingly, distance X versus distance X' can be determined by accessing the weighting for "nets" or signal paths 202-S and 204-S, for example. In this fashion, a circuit block can be placed in a relative position based on the switching activity of associated signals. Further, the placement can further be dependent on a user-controlled factor as well as an initial and/or projected signal path length.



US 7,360,193 B1

7

Referring now to FIG. 4A, a schematic diagram showing an exemplary circuit that may be used in embodiments of the present invention is indicated by the general reference character 400. This example shows a simple circuit structure using standard cells or gates to implement logic or other functions that is suitable for IC design. Such logic functions could include AND/NAND, OR/NOR, XOR/XNOR, INV, or flip-flops, as just a few examples. In practice, any circuit can be designed and treated as a "standard cell" for automatic placement and routing in a larger design. More commonly, a set of standard cells are provided and characterized for each design technology and are utilized in an "off-the-shelf" manner in a typical ASIC design flow.

In the example of FIG. 4A, standard cell 402 can be a buffer stage receiving input In1 and outputting signal 402-S. Standard cell 404 can be an "AND" function having a NAND-gate followed by an inverter. Standard cell 404 can receive signal 402-S and input In2 and can output signal 404-S. Standard cell 406 can be an "OR" function having a NOR-gate followed by an inverter. Standard cell 406 can receive signal 404-S and input In3. Particularly if standard cells 402 and 406 are placed first, embodiments of the present invention can be used to determine a relative placement of standard cell 404. Consistent with such embodiments, a simulation of circuit 400 may be done to determine the switching activity of signals 402-S and 404-S.

Referring now to FIG. 4B, an example timing diagram for the circuit of FIG. 4A is shown and indicated by the general reference character 440. Such a timing diagram can be a waveform representation of a VERILOG simulation result, such as a Value Change Data (VCD) file, for example. Input In1 (waveform 442) can be an oscillating signal, such as a clock, and may go high (i.e., transition from "0" to "1") in odd cycles and go low (i.e., transition from "1" to "0") in even cycles. Input In2, which may be a clock enable signal, for example, can go high in cycle 6 and go low in cycle 8, as shown by waveform 444. Signal 402-S (waveform 446) can be a simple delay of In1 because signal 402-S is the output of buffer stage 402. Signal 404-S can go high in cycle 7 and go low in cycle 8 to reflect the "AND" function of standard cell 404. Thus, over the time period of 11 cycles shown in FIG. 4B, the switching activity of signal 402-S is six times the switching activity of signal 404-S (i.e., six full switching cycles for 402-S versus only one switching cycle for 404-S).

The switching activity of various signals in a circuit, where that circuit has been simulated, can also be determined using a commercially available or custom software tool. For example, if the circuit simulation is done using VERILOG simulation language, a VCD file can be created as an output file. A switching activity interface (SAIF) can be used to determine the switching activity of each signal or "net" in the circuit. An example of a free utility for conversion of a VCD output to SAIF is the "vcd2saif" script, which is available from Synopsys, Inc., of Mountain View, Calif. (www.synopsys.com; in particular, see www.synopsys.com/partners/tapin/saif.html).

Referring now to FIG. 4C, a schematic diagram showing a relative placement of circuit block portions of the circuit of FIG. 4A resulting from the use of embodiments of the present invention is indicated by the general reference character 480. Based on the switching activity of signals 402-S and 404-S in the above example, standard cell 404 can be placed relatively close to standard cell 402. Thus, distance X can be substantially less than distance X' and the capacitance of signal path 402-S can accordingly be less than the capacitance of signal path 404-S. In this fashion,

8

power consumption due to driving the relatively high switching frequency signal 402-S can be minimized. Further, the signal integrity of all signals affected by localized power supply noise in the region of standard cell 402 can be improved because such noise can be minimized according to embodiments of the present invention.

While the exemplary circuit block arrangements discussed above generally show the placement of a third circuit block where two other circuit blocks interfacing to the third block have already been placed, these illustrations should not be considered limiting. As one skilled in the art will recognize, three or more previously-placed circuit blocks may have signals that interface to a new block to be placed and embodiments of the present invention are equally adaptable to such applications. In one embodiment, such a new block may be placed in accordance with a two-dimensional average relative position based on associated signal switching activities. In any event, in accordance with embodiments of the present invention, the new block may be placed relative to or in proximity with previously-placed circuit blocks in relation to the switching activity of the associated interface signals.

Referring now to FIG. 5, a box diagram showing a synthesis flow adapted for use with embodiments of the present invention is indicated by the general reference character 500. Box 524 shows elements adapted for use in accordance with embodiments of the present invention. The remaining boxes in FIG. 5 represent a conventional synthesis flow. Inputs to Synthesis 508 typically include Constraints and Parameters 502, Design Description (HDL) 504, and Technology Library 506. Constraints and Parameters 502 may include physical expectations of the design, such as the circuit operating speed and/or the circuit layout area. Design Description (HDL) 504 can be a VERILOG HDL (VHDL) description of the logic operation(s) for synthesis. Technology Library 506 may contain a functional description as well as other information, such as may be related to the area and speed of all standard cells in a given process technology. For example, Technology Library 506 may be specific to a technology generation (e.g., 0.18 micron technology), a company (e.g., TSMC), and a process type (e.g., CMOS; triple-level metal; fast/normal/slow lot variation).

Outputs from Synthesis 508 may include Schematics 510, Netlist 512, and Reports 514. Schematics 510 can be schematic representations of the synthesized functions of Design Description (HDL) 504. Netlist 512 can be a text file description of a physical connection of components, such as standard cells, and can include a description of the various circuit blocks in the design and signal paths between the circuit blocks. Reports 514 can include speed and area data associated with results of Synthesis 508.

As discussed above, a netlist representation (e.g., Netlist 512) may be used for simulation to determine the switching activity of various signals. Accordingly, Simulator 516 can receive Netlist 512 and provide Simulation Result File 518. For example, Simulator 516 can be a VERILOG simulator and Simulation Result File 518 can be a VCD file. Simulation Result File 518 can be used to determine Switching Frequency Information 520. As discussed above, this can be accomplished by the use of a "vcd2saif" utility, for example. Finally, Place Cells 522 can receive Switching Frequency Information 520 so as to make placements based on the switching activity of associated signals.

In this fashion, a conventional ASIC type design flow including synthesis can be adapted for placement of standard cells in accordance with embodiments of the present invention. Alternatively, embodiments of the present invention

## US 7,360,193 B1

9

may be used in other design flows whereby a switching activity of signals can be determined via simulation or other means.

Further examples of suitable systems, tools and/or methods in which the present invention is generally applicable include those described in, e.g., U.S. Pat. Nos. 6,080,201 and 5,798,936, the relevant portions of which are each incorporated herein by reference, and those commercially available from place-and-route software vendors such as Cadence Design Systems (e.g., the SILICON ENSEMBLE™, SILICON ENSEMBLE-PK™, FIRST ENCOUNTER™, and NANO ENCOUNTER™ tools), Silicon Valley Research, Inc. (e.g., the QIC/APR™, GARDS™, SCT™ and FLOORPLACER™ tools), Synopsys (e.g., the CHIP ARCHITECT™, DESIGN COMPILER™, and FLOORPLAN COMPILER™ tools) and Mentor Graphics (e.g., the AUTOCELLS™ tool).

Thus, embodiments of the present invention can advantageously reduce power consumption as well as supply noise by optimally placing circuit blocks in an automated place-and-route flow. Further, signal integrity problems due to non-optimal circuit block or component placement can be minimized. Embodiments of the invention are suitable for the automated placement of circuit blocks within an IC and/or placements of ICs or components on a board, such as a printed circuit board (PCB).

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents.

What is claimed is:

1. A method of placing, comprising the steps of:

- a) determining a first signal path length and a first switching activity for a first signal path between a first circuit block and a second circuit block and a second signal path length and a second switching activity for a second signal path between said first circuit block and a third circuit block;
- b) determining a first weighting by multiplying said first switching activity by a first user-controlled factor to form a first result and adding said first result to said first signal path length and a second weighting by multiplying said second switching activity by a second user-controlled factor to form a second result and adding said second result to said first signal path length;
- c) placing said second and third circuit blocks prior to placing said first circuit block; and
- d) placing said first circuit block relative to said second and third circuit blocks in a position related to said first weighting and said second weighting.

2. The method of claim 1, wherein the step of determining said first weighting and said second weighting occurs prior to the step of placing said first circuit block.

3. The method of claim 1, further including the step of determining said first and second signal paths.

4. The method of claim 3, wherein the step of determining said first and second signal paths includes matching said first

10

and second signal paths to a corresponding two of a plurality of nets in a netlist describing said first, second and third circuit blocks.

5. The method of claim 4, wherein the step of determining said switching activity includes simulating using said netlist.

6. The method of claim 5, wherein said simulating includes an event-based logic simulation.

7. The method of claim 6, wherein said event-based logic simulation includes a VERILOG simulation.

8. The method of claim 5, wherein the step of determining said switching activity further includes converting an output file from the simulating step to a switching activity file.

9. The method of claim 8, wherein said switching activity file includes a frequency of switching for each signal path over a predetermined time period.

10. The method of claim 9, wherein the step of placing includes placing said first circuit block closer to said second circuit block if the frequency of switching for said first signal path is greater than the frequency of switching for said second signal path.

11. The method of claim 1, wherein each of the circuit blocks includes a standard cell configured to implement a logic or timing function.

12. The method of claim 11, further including the step of accessing a technology library having a characterization of said standard cell.

13. The method of claim 1, wherein said position is automatically determined by said weighting.

14. The method of claim 1, further including the step of synthesizing a circuit implementation in response to a hardware description.

15. The method of claim 1, wherein each of the circuit blocks includes an integrated circuit or component.

16. The method of claim 1, wherein determining said switching activity for said first signal path comprises determining a frequency of state changes in a signal on said first signal path and determining said switching activity for said second signal path comprises determining a frequency of state changes in a signal on said second signal path.

17. A computer readable medium comprising a computer executable set of instructions adapted to perform the steps of:

- a) determining a first signal path length and a first switching activity factor of a first signal path between first and second circuit blocks and a second signal path length and a second switching activity factor of a second signal path between first and third circuit blocks;
- b) determining a first weighting by multiplying said first switching activity factor by a first user-controlled factor to form a first result and adding said first result to said first signal path length and a second weighting by multiplying said second switching activity factor by a second user-controlled factor to form a second result and adding said second result to said first signal path length; and
- c) placing said first circuit block relative to said second and third circuit blocks in a position related to said first weighting and said second weighting.

18. The medium of claim 17, wherein the step of determining said first and second signal paths occurs prior to the step of placing.

19. The medium of claim 18, wherein the step of determining said first and second signal paths includes matching said first and second signal paths to a corresponding two of a plurality of nets in a netlist describing said first, second and third circuit blocks.

## US 7,360,193 B1

**11**

**20.** The medium of claim **19**, wherein the step of determining said first and second switching activity factors includes simulating using said netlist.

**21.** The medium of claim **17**, wherein each of the circuit blocks includes a standard cell configured to implement a logic function. 5

**22.** The medium of claim **17**, further including at least one instruction for synthesizing a circuit implementation in response to a hardware description.

**23.** The medium of claim **17**, wherein each of the circuit blocks includes an integrated circuit or component. 10

**12**

**24.** A computer system comprising the medium of claim **17**, configured to execute said instructions.

**25.** The method of claim **17**, wherein determining said switching activity for said first signal path comprises determining a frequency of state changes in a signal on said first signal path and determining said switching activity for said second signal path comprises determining a frequency of state changes in a signal on said second signal path.

\* \* \* \* \*

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 7,360,193 B1  
APPLICATION NO. : 10/946925  
DATED : April 15, 2008  
INVENTOR(S) : Michael Burstein et al.

Page 1 of 1

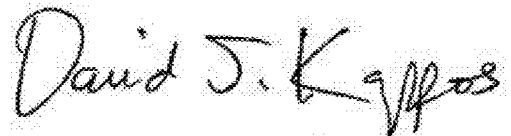
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

IN THE CLAIMS:

Claim 1, col. 9, line 55: change “adding said second result to said first signal path length” to --adding said second result to said second signal path length--.

Claim 17, col. 10, line 55: change “adding said second result to said first signal path length” to --adding said second result to said second signal path length--.

Signed and Sealed this  
Twenty-first Day of June, 2011

A handwritten signature in black ink that reads "David J. Kappos". The signature is written in a cursive, flowing style with a large, stylized 'D' and 'K'.

David J. Kappos  
*Director of the United States Patent and Trademark Office*

# **EXHIBIT C**



(12) **United States Patent**  
**Makarov et al.**

(10) **Patent No.:** **US 7,823,112 B1**  
(45) **Date of Patent:** **Oct. 26, 2010**

(54) **METHOD, SOFTWARE AND SYSTEM FOR ENSURING TIMING BETWEEN CLOCKED COMPONENTS IN A CIRCUIT**

(75) Inventors: **Mikhail Makarov**, Moscow (RU); **Igor Chourkin**, Moscow (RU); **Mikhail Komarov**, Moscow (RU); **Boris Ginzburg**, Santa Clara, CA (US)

(73) Assignee: **Golden Gate Technology, Inc.**, San Jose, CA (US)

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 422 days.

(21) Appl. No.: **10/449,757**

(22) Filed: **May 30, 2003**

(51) **Int. Cl.**  
**G06F 17/50** (2006.01)  
**G01R 31/28** (2006.01)

(52) **U.S. Cl.** ..... **716/12**; 716/6; 716/7; 716/13; 716/14; 716/17; 716/18

(58) **Field of Classification Search** ..... 716/6, 716/7, 12-14, 17, 18; 714/725, 727, 736; 375/356; 365/201

See application file for complete search history.

(56) **References Cited**

#### U.S. PATENT DOCUMENTS

5,473,756 A \* 12/1995 Traylor ..... 710/57  
5,521,837 A 5/1996 Frankle et al.  
5,550,748 A 8/1996 Xiong  
5,638,291 A 6/1997 Li et al.  
5,644,496 A 7/1997 Agrawal et al.  
5,717,729 A \* 2/1998 Iknaian et al. .... 375/356  
5,761,078 A 6/1998 Fuller et al.  
5,774,380 A 6/1998 Pickup et al.  
5,784,600 A 7/1998 Doreswamy et al.

5,798,936 A 8/1998 Cheng  
5,918,058 A 6/1999 Budd  
5,974,245 A 10/1999 Li et al.  
5,987,086 A 11/1999 Raman et al.  
6,080,201 A 6/2000 Hojat et al.  
6,081,656 A \* 6/2000 Witt ..... 716/3  
6,086,631 A 7/2000 Chaudhary et al.

(Continued)

#### OTHER PUBLICATIONS

Yang et al., "Timing-driven placement using design hierarchy guided constraint generation", Nov. 10-14, 2002, Computer Aided Design, 2002. ICCAD 2002. IEEE/ACM International Conference on, pp. 177-180.\*

(Continued)

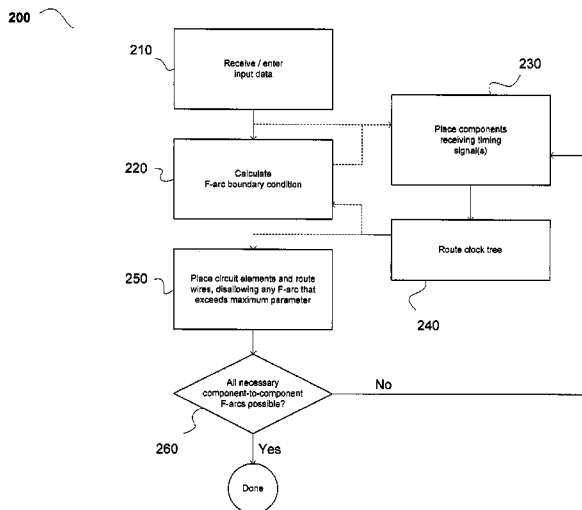
*Primary Examiner*—Helen Rossoshek

(74) *Attorney, Agent, or Firm*—The Law Offices of Andrew D. Fortney; Andrew D. Fortney

(57) **ABSTRACT**

A method, software, and system for placing circuit elements and routing wires. The method, software, and system generally include the steps of (a) determining a boundary condition for signal paths between components in a circuit, wherein each of the components receives a clock signal and the signal paths include  $n$  wires and  $(n-1)$  circuit elements in alternating serial communication between the components,  $n$  being 2 or more; and (b) placing the circuit elements and routing the wires between the components and the circuit elements such that no signal path in the circuit exceeds the boundary condition. In preferred embodiments, the boundary condition is a maximum length, and the method further includes placing the clocked components in a floor plan such that no signal path can exceed the boundary condition. The present invention advantageously ensures that timing requirements for signal paths between clocked circuit components are met automatically.

**36 Claims, 9 Drawing Sheets**



## US 7,823,112 B1

Page 2

## U.S. PATENT DOCUMENTS

6,099,583	A	8/2000	Nag	
6,145,117	A	11/2000	Eng	
6,212,489	B1	4/2001	Klein et al.	
6,230,304	B1	5/2001	Groeneveld et al.	
6,253,361	B1	6/2001	Buch	
6,305,001	B1 *	10/2001	Graef	716/12
6,321,183	B1	11/2001	Tatsumi	
6,341,092	B1 *	1/2002	Agrawal	365/201
6,397,170	B1	5/2002	Dean et al.	
6,415,420	B1	7/2002	Cheng et al.	
6,418,552	B1	7/2002	Osborn	
6,434,731	B1	8/2002	Brennan et al.	
6,442,739	B1 *	8/2002	Palermo et al.	716/6
6,453,446	B1	9/2002	Van Ginneken	
6,496,965	B1	12/2002	Van Ginneken et al.	
6,505,330	B1	1/2003	Osborn	
6,507,941	B1	1/2003	Leung et al.	
6,519,745	B1	2/2003	Srinivas et al.	
6,525,587	B2 *	2/2003	Makino	327/292
6,530,065	B1	3/2003	McDonald et al.	
6,543,041	B1 *	4/2003	Scheffer et al.	716/10
6,553,338	B1	4/2003	Buch et al.	
6,594,807	B1	7/2003	Tetelbaum et al.	
6,662,348	B1	12/2003	Naylor et al.	
6,681,338	B1	1/2004	Kolipara	
6,694,464	B1 *	2/2004	Quayle et al.	714/725
6,725,438	B2	4/2004	Van Ginneken	
6,785,873	B1	8/2004	Tseng	
6,817,005	B2	11/2004	Mason et al.	
6,842,045	B2 *	1/2005	Shimazaki et al.	326/95
6,845,494	B2	1/2005	Burks et al.	
6,851,095	B1	2/2005	Srinivasan et al.	
6,877,143	B1 *	4/2005	Palermo et al.	716/6
6,907,590	B1 *	6/2005	Al-Dabagh et al.	716/6
6,950,998	B1	9/2005	Tuan	
7,032,198	B2 *	4/2006	Sano et al.	716/5
7,039,887	B2 *	5/2006	Khalil et al.	716/5
7,062,425	B1	6/2006	Bell et al.	
7,178,124	B1 *	2/2007	Makarov et al.	716/12
2002/0069396	A1	6/2002	Bhattacharya et al.	
2002/0112220	A1	8/2002	Miller	
2003/0056185	A1 *	3/2003	Nakajima	716/5
2003/0208736	A1 *	11/2003	Teng et al.	716/7
2004/0015803	A1	1/2004	Huang et al.	
2004/0025129	A1 *	2/2004	Batchelor	716/6
2004/0049747	A1	3/2004	Yamasaki et al.	
2004/0073878	A1	4/2004	Hasegawa et al.	
2004/0150422	A1	8/2004	Wong	
2004/0199883	A1	10/2004	Palumbo	
2005/0034091	A1	2/2005	Harn	
2005/0050496	A1	3/2005	Kovacs et al.	
2006/0031795	A1	2/2006	Rahmat et al.	

2006/0168551 A1 7/2006 Mukuno

## OTHER PUBLICATIONS

Swinnen et al., "Timing issues related to the automated placement and routing of high performance ASICs", Sep. 23-27, 1991, ASIC Conference and Exhibit, Proceedings., Fourth Annual IEEE International, pp. P14-6/1-4.\*

Yeh et al., "Sequential delay budgeting with interconnect prediction", Oct. 2004, Very Large Scale Integration (VLSI) Systems, IEEE Transactions on, vol. 12, Issue 10, pp. 1028-1037.\*

Kay et al., "EWA: efficient wiring-sizing algorithm for signal nets and clock nets", Jan. 1998, Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, vol. 17, Issue 1, pp. 40-49.\*

Yang et al., "Delay budgeting in sequential circuit with application on FPGA placement", Jun. 2-6, 2003, Design Automation Conference, 2003. Proceedings, pp. 202-207.\*

Zhuoyuan et al., "Incremental placement algorithm for standard-cell layout", May 26-29, 2002, Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on, vol. 2, pp. II-883-II-886 vol. 2.\* Datasheet, "CANDENCE SE-PKS," Cadence Design Systems, Inc., San Jose, California (2002).

"Cadence Design Systems—Silicon Ensemble-PKS," Apr. 9, 2003, <http://www.cadence.com/products/sepks.html>.

Datasheet, "Nano Encounter," Cadence Design Systems, Inc., San Jose, California (2003).

"Nano Encounter," printed Apr. 9, 2003, at <http://www.cadence.com/products/nanoencounter.html>.

"AutoCells 2002.1 Enhancement Value Sheet," Mentor Graphics Corp., Wilsonville OR (2002).

"OpenDoor Catalog, Avanti," printed Apr. 9, 2003, at <http://www.mentor.com/partners/opendoo/Avant.html>.

"Products—SVR SC," printed Apr. 9, 2003, at <http://www.svri.com/sc.htm>.

"Products—SVR FloorPlacer," printed Apr. 9, 2003, at <http://www.svri.com/floorplacer.htm>.

"Products—SVR GARDS," printed Apr. 9, 2003, at <http://www.svri.com/gards.htm>.

"Synopsys FlexRoute Top Level Router," Apr. 9, 2003, at [http://www.synopsys.com/products/tlr/tlr\\_ds.html](http://www.synopsys.com/products/tlr/tlr_ds.html).

"Chip Architect," printed Apr. 9, 2003, at [http://www.synopsys.com/products/designplanning/ca\\_ds.html](http://www.synopsys.com/products/designplanning/ca_ds.html).

"Synopsys Physical Synthesis," Apr. 9, 2003, at [http://www.synopsys.com/products/phy\\_syn/phy\\_syn.html](http://www.synopsys.com/products/phy_syn/phy_syn.html).

"Products—SVR QIC/APR," printed Apr. 9, 2003, at <http://www.svri.com/qic-apr.htm>.

Astro-Rail: A Comprehensive Power-Integrity Analysis, Implementation and Verification Tool; 2 Pgs.; Synopsys; www.synopsys.com; Mountain View, CA.

Advanced Clock Implementation; Blast Chip TM 3.0 User Guide; Magma Design Automation TM Incorporated; 52 Pgs; Cupertino, CA

\* cited by examiner

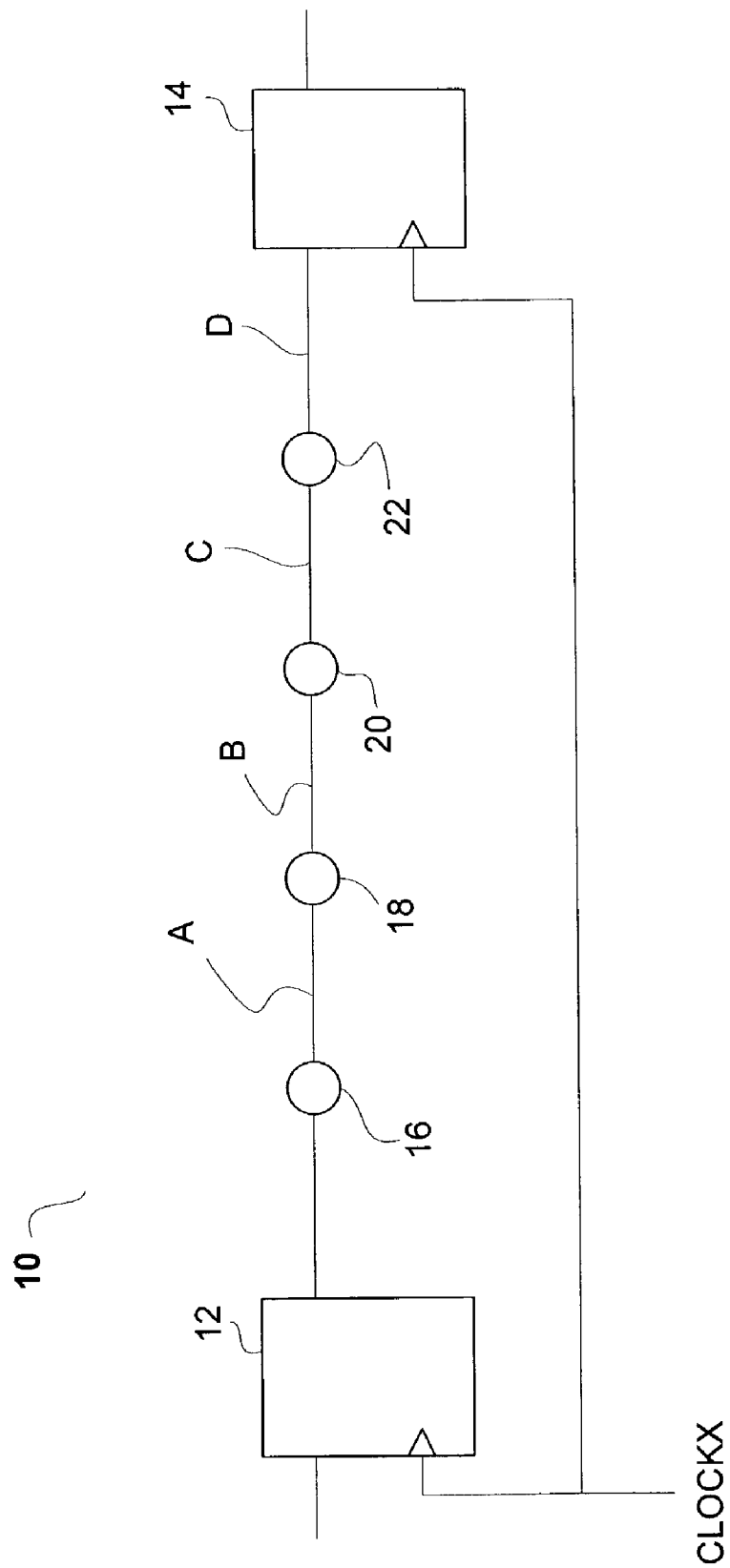
U.S. Patent

Oct. 26, 2010

Sheet 1 of 9

US 7,823,112 B1

FIG. 1



U.S. Patent

Oct. 26, 2010

Sheet 2 of 9

US 7,823,112 B1

FIG. 2

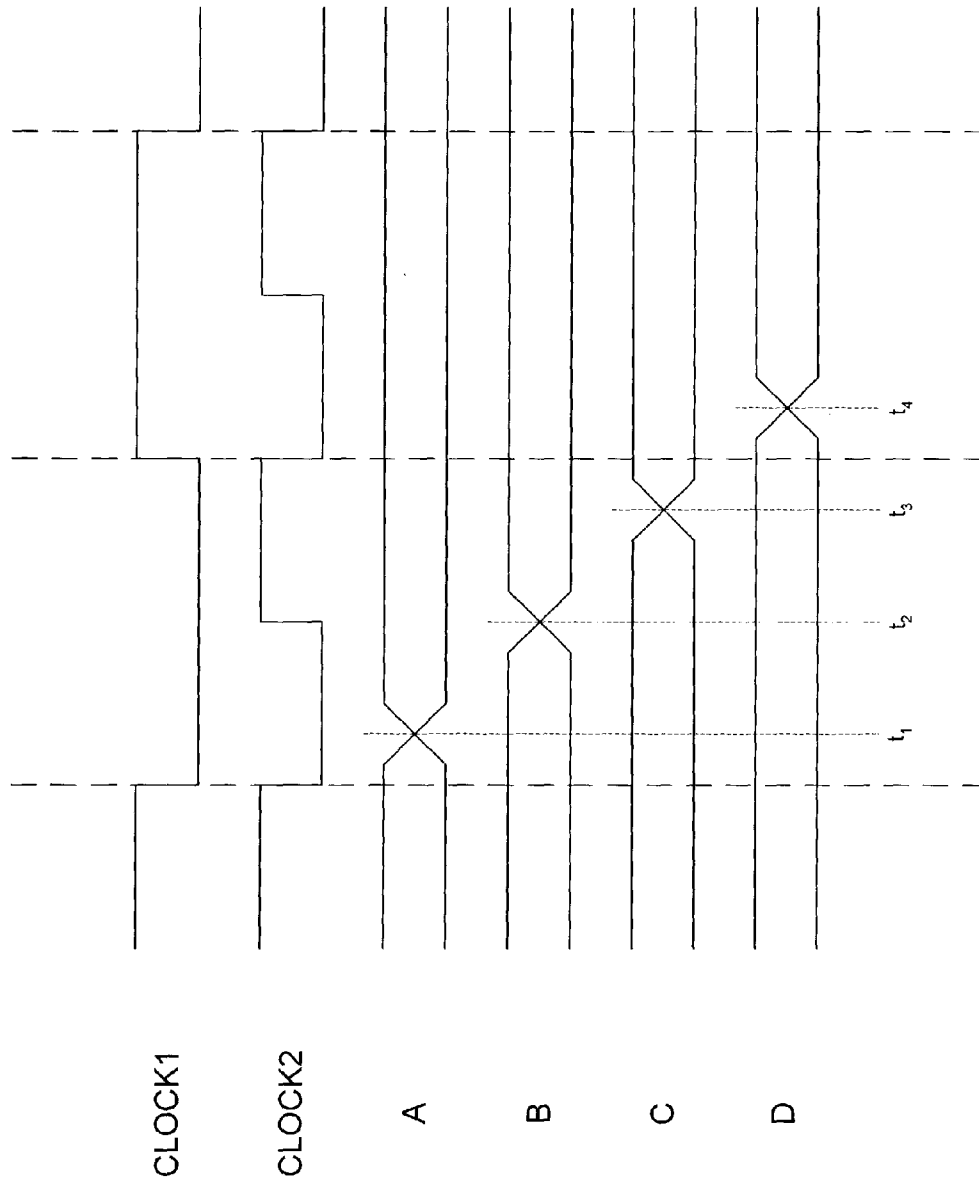


FIG. 3

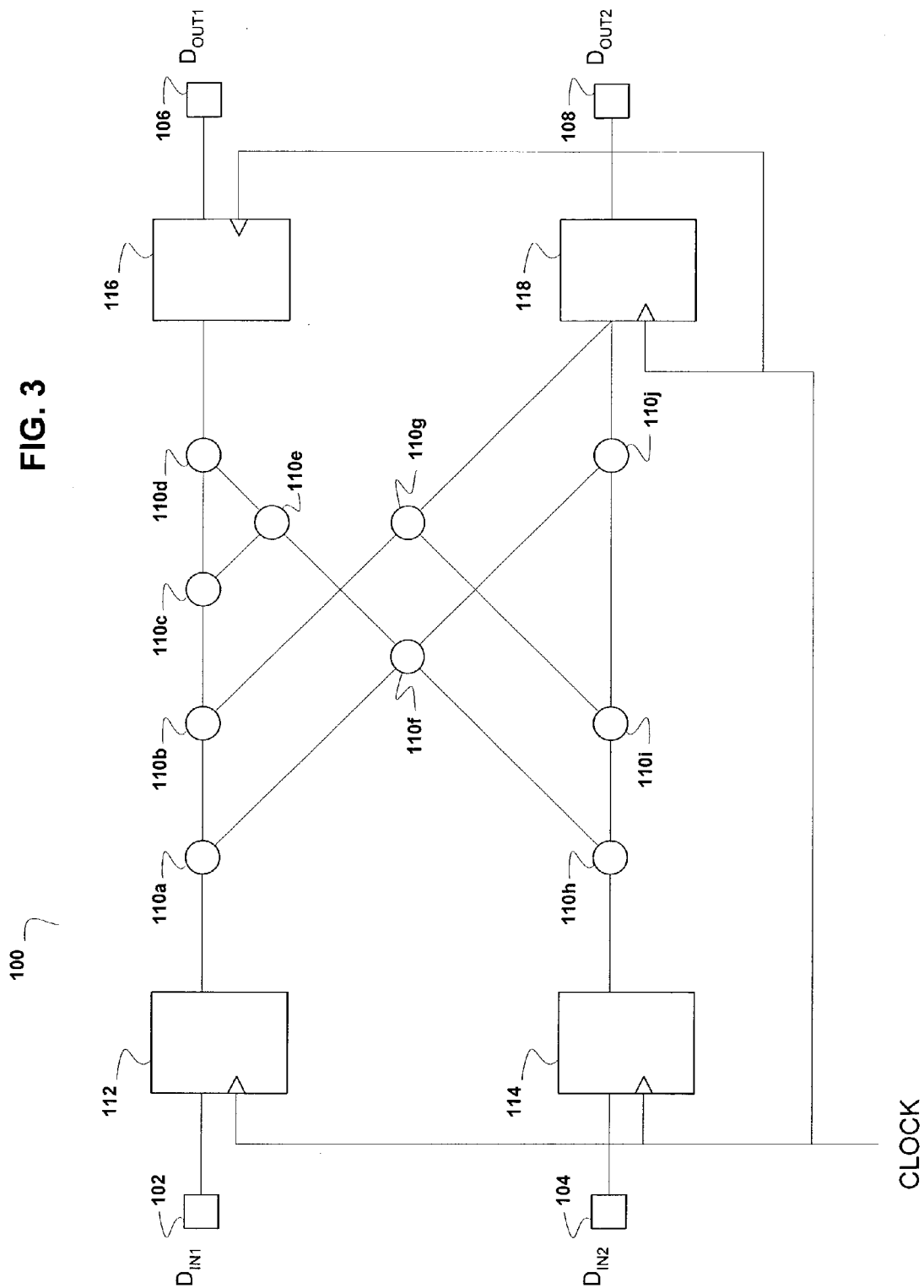


FIG. 4

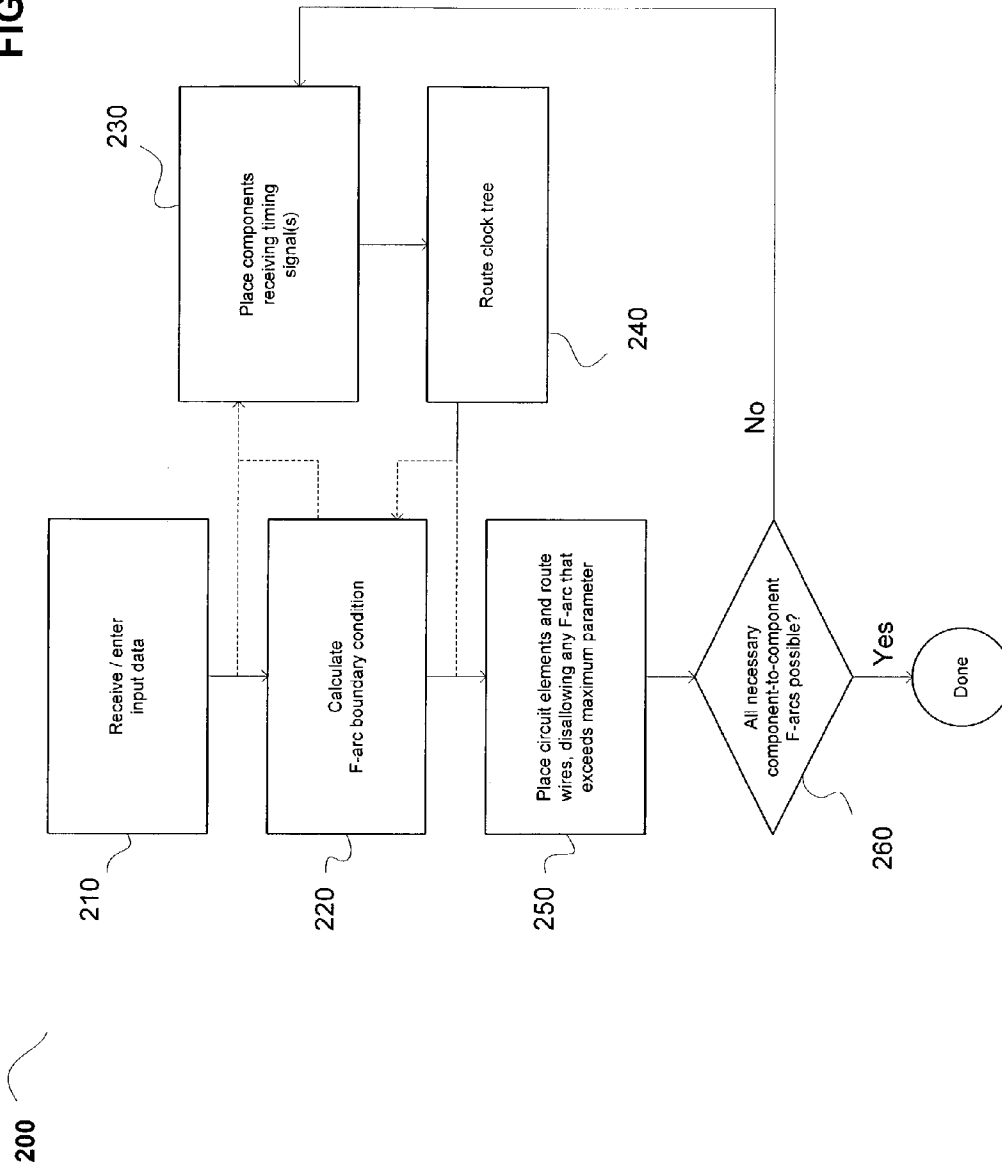


FIG. 5

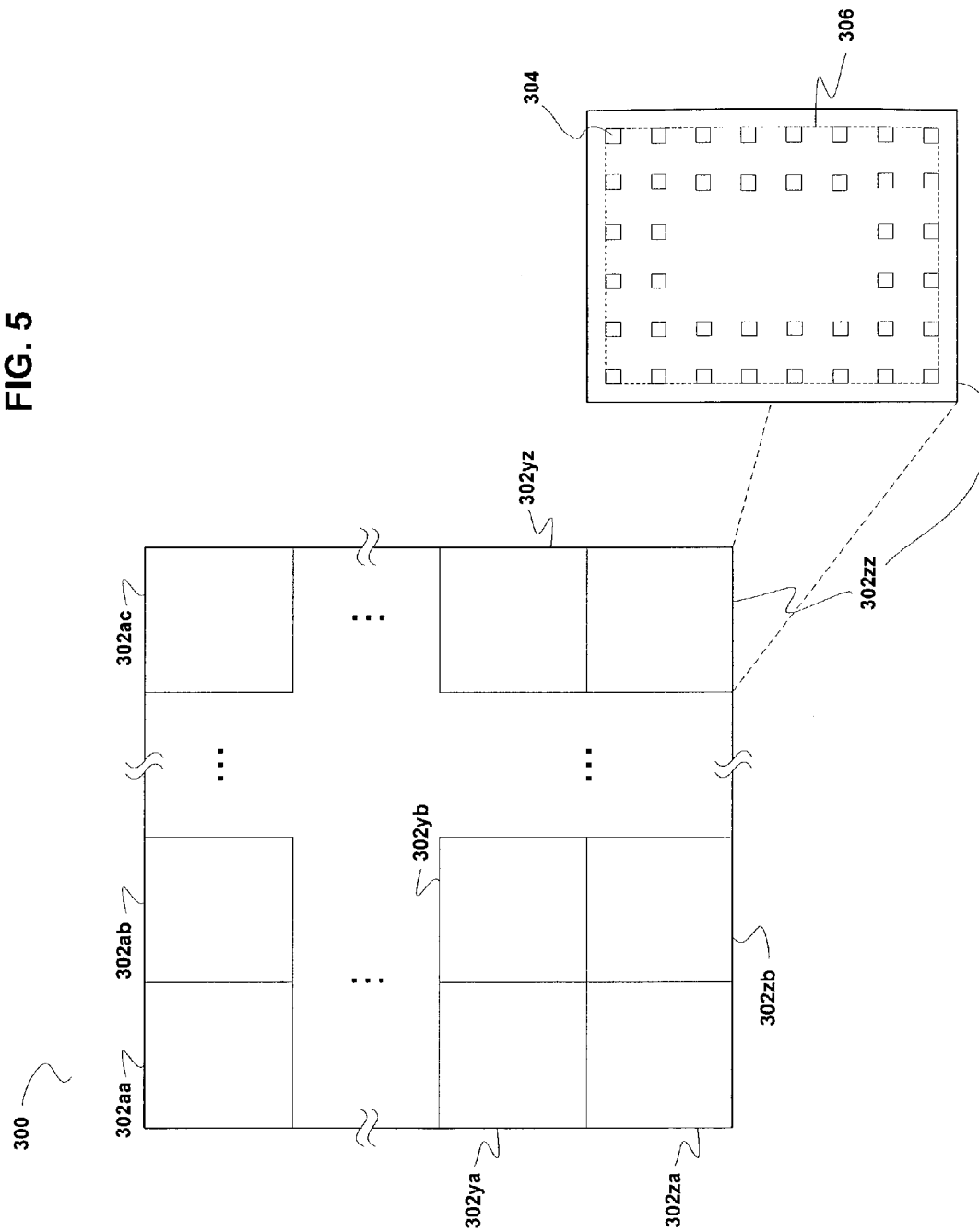


FIG. 6

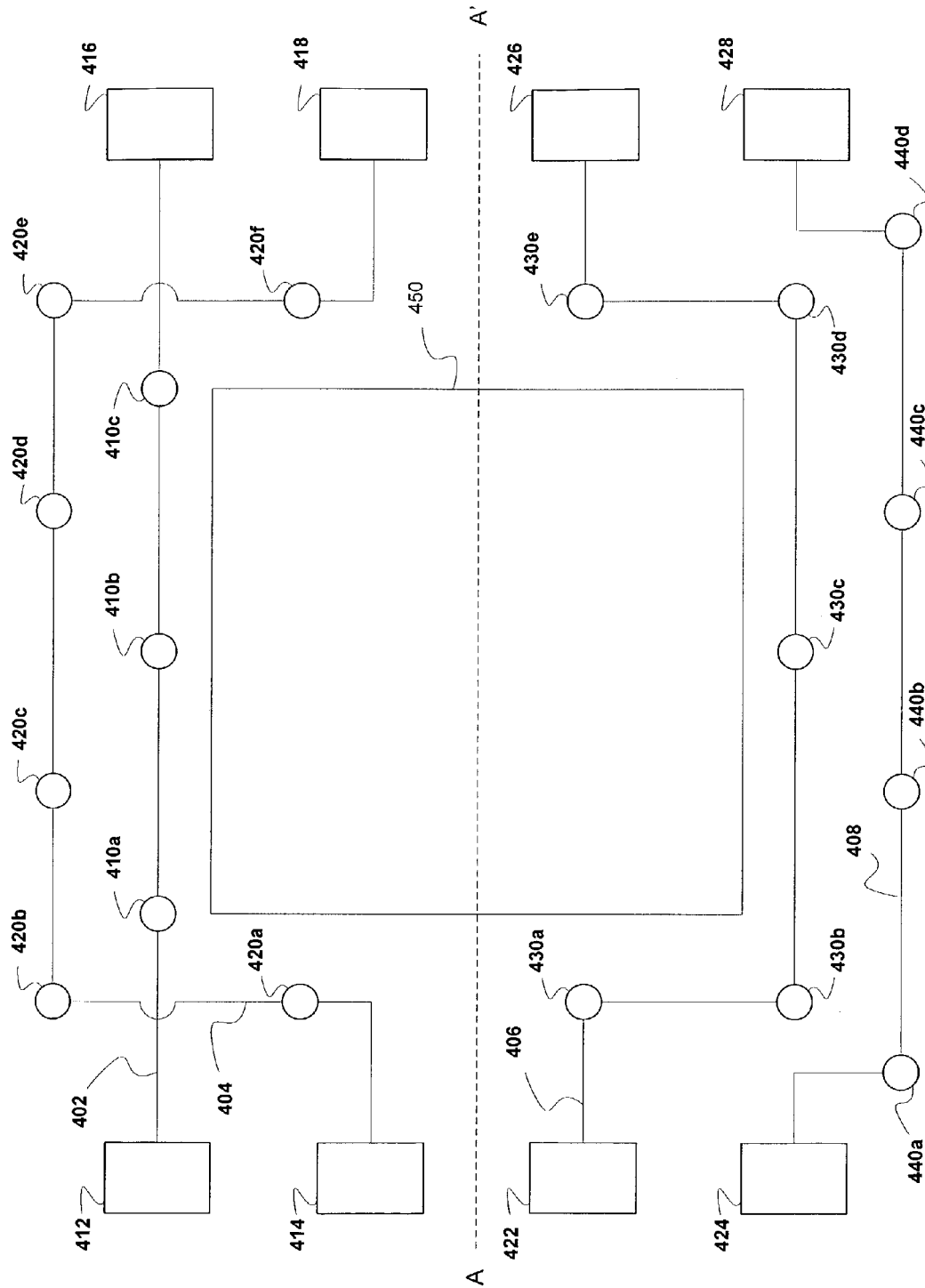
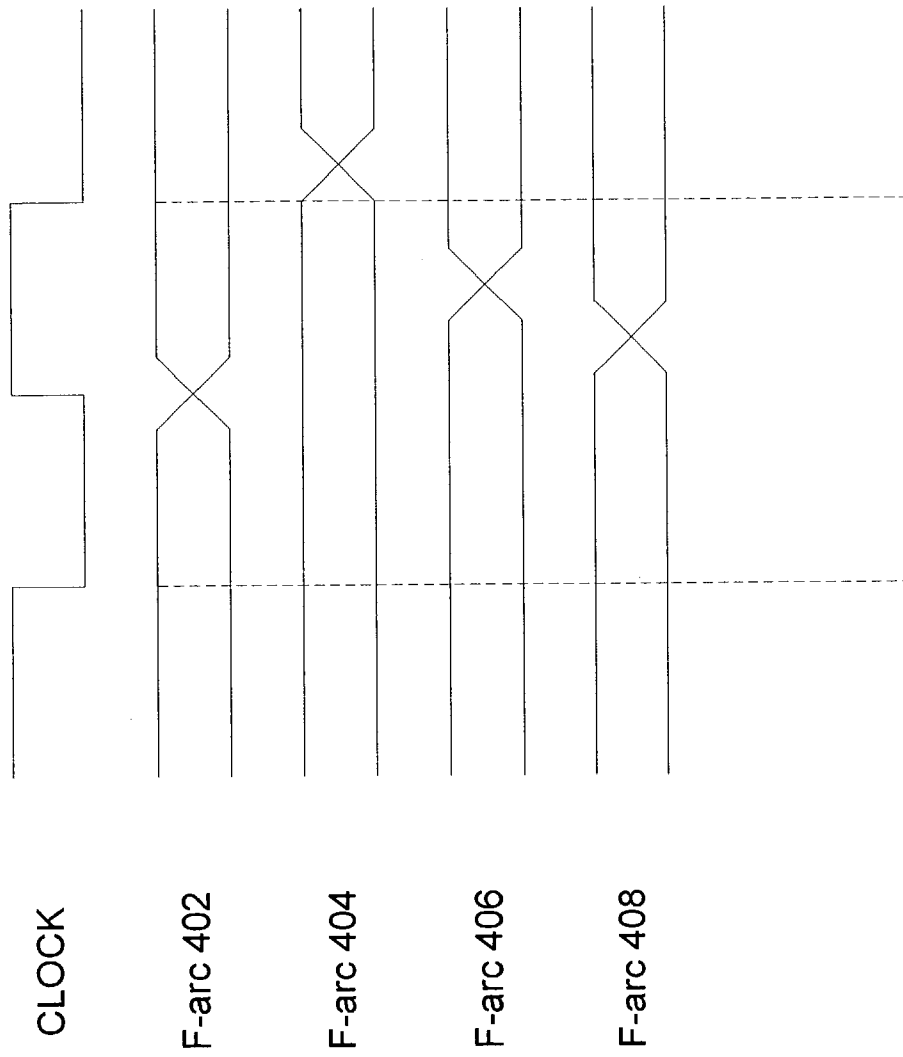
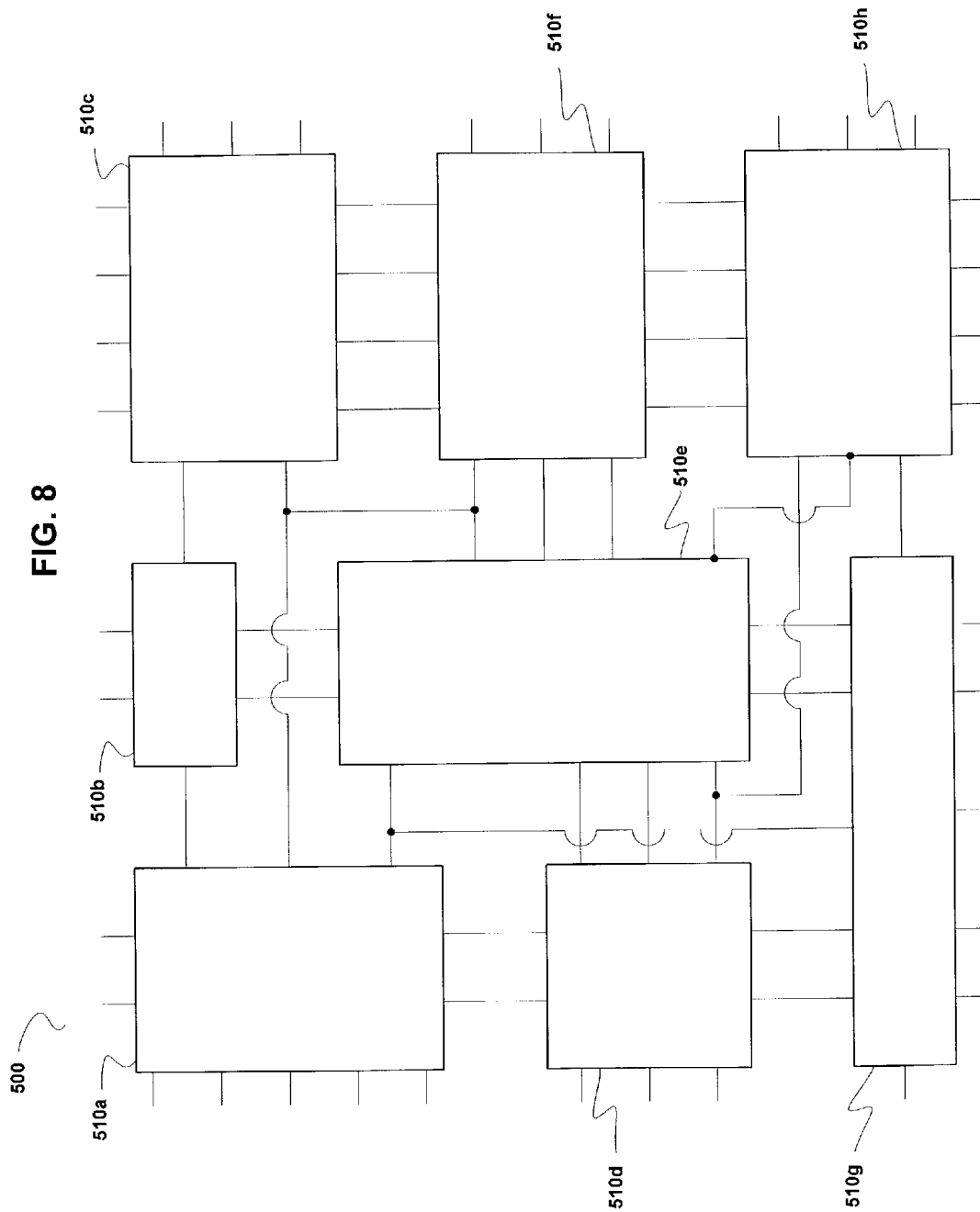
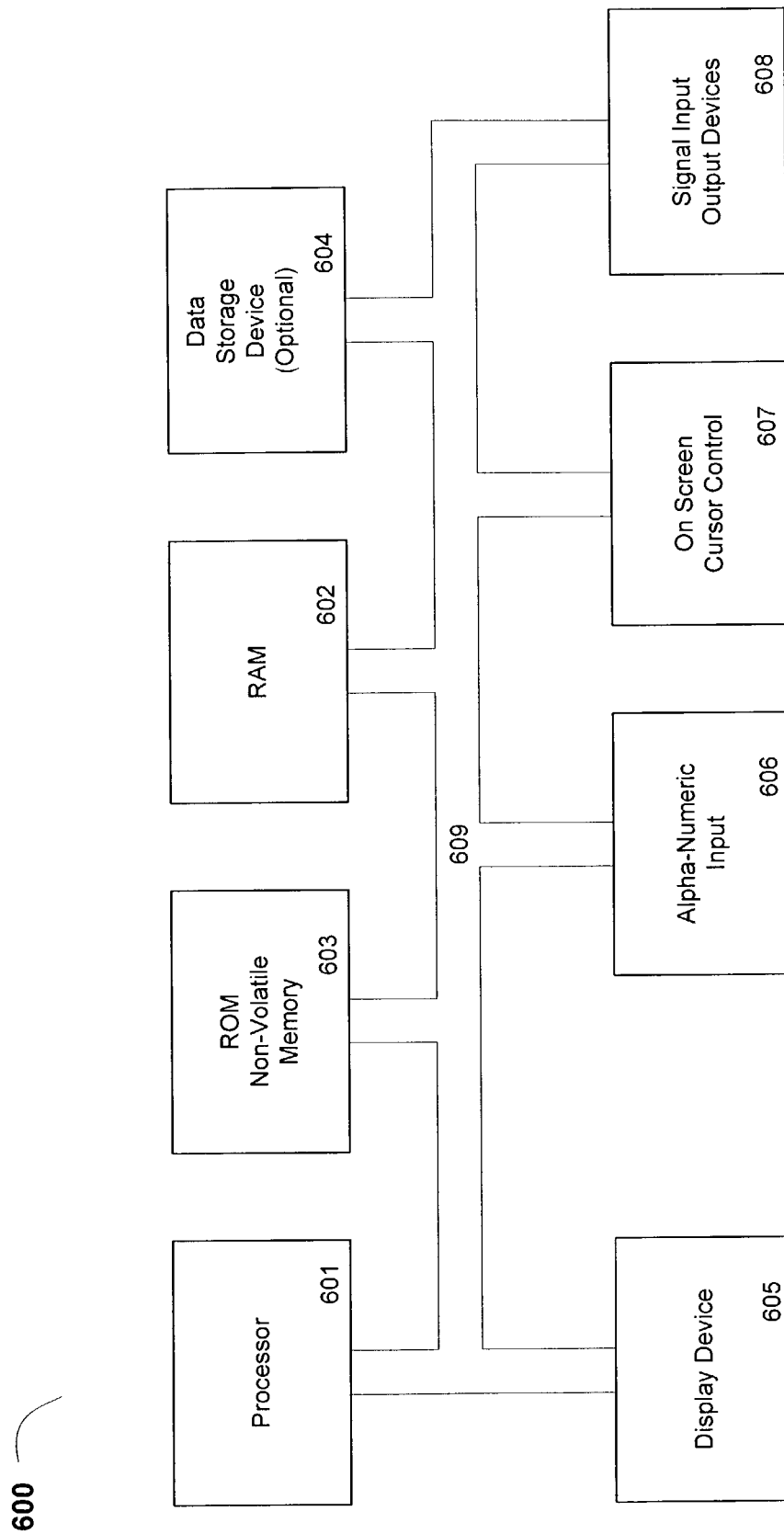




FIG. 7





**FIG. 9**

US 7,823,112 B1

1

# **METHOD, SOFTWARE AND SYSTEM FOR ENSURING TIMING BETWEEN CLOCKED COMPONENTS IN A CIRCUIT**

## **FIELD OF THE INVENTION**

The present invention generally relates to the field of circuit design, particularly integrated circuit design. More specifically, embodiments of the present invention pertain to methods, algorithms, software, systems and architectures for improving timing in the design of an integrated circuit and/or ensuring that timing constraints in an integrated circuit are met.

## **DISCUSSION OF THE BACKGROUND**

Traditionally, in the field of integrated circuit design, the length of time that a signal takes to go from a predetermined origin to a predetermined destination (herein, generally referred to as “timing”) is an important parameter. Integrated circuit designers typically include contributions from (1) transistors and/or other circuit devices (such as capacitors, resistors, diodes, etc.) and (2) wires when predicting or evaluating the timing of a particular design. As lines widths and device dimensions decrease, the relative contributions of wires to timing increase. At or below minimum or critical dimensions of 0.18 microns, wires become the major or dominant contributor to delays in timing.

Integrated circuits also generally have timing, or “clock,” circuitry thereon. Such timing circuitry generally ensures that signals are captured at predetermined locations on the chip at certain times. The times at which certain circuit components capture data in the signals is generally defined by the clock signal waveform and the distribution of the clock signal to component locations on the chip.

Place and route software is generally used by integrated circuit designers to place circuit structures and/or configure wiring in a design automatically or semi-automatically. One typical challenge for place and route software has been to place circuit components (e.g., transistors, capacitors, diodes, logic gates, flip-flops, latches, registers, etc.) in a manner leaving sufficient room for wires to interconnect them. A number of such software tools are available in the marketplace today. However, such commercially available tools generally do not distinguish between clocked circuit components, such as flip-flops, latches and registers, and combinatorial circuit elements that do not receive a clock signal, such as switches and logic gates. Consequently, such tools generally do not ensure, or “guarantee by design,” timing of signal paths from any clocked circuit component to the next downstream clocked circuit component. Rather, timing in a design is generally met by iteratively designing circuitry, then analyzing or determining the timing of various signal paths through the circuitry, and changing the design to shorten the signal paths that violate certain predetermined timing constraints or parameters.

Given the increasing demands on integrated circuit designers to create chips of increasing density, decreasing wire and transistor widths, and decreasing power supply and power consumption, it is difficult, if not impossible, to ensure meeting timing constraints automatically or “by design.” Increasing the complexity, flexibility and/or functionality of the circuitry on a chip exacerbates these challenges. Thus, what is needed is a tool with which integrated circuit designers can ensure timing of signals from any given origin to any given destination in a circuit.

2

## **SUMMARY OF THE INVENTION**

Embodiments of the present invention relate to methods, algorithms, software, architectures and/or systems for placing circuit elements and/or routing wires in a circuit design, such that the design automatically meets timing constraints between circuit components receiving a clock signal.

The present invention advantageously ensures that timing requirements for signal paths between clocked circuit components (such as flip-flops and/or registers) are met automatically or “by design.” In certain preferred embodiments, the invention helps to reduce power consumption, improve timing between circuit blocks and/or clock domains on an integrated circuit, improve pin-to-pin timing at a chip level, and/or reduce the total number of circuit elements and/or components in a design.

These and other advantages of the present invention will become readily apparent from the detailed description of preferred embodiments below.

## **BRIEF DESCRIPTION OF THE DRAWINGS**

FIG. 1 is a box diagram showing an exemplary F-arc.

FIG. 2 is a set of waveforms for illustrating how the invention operates with respect to the F-arc of FIG. 1.

FIG. 3 is a box diagram showing a relatively simple, exemplary array of gates between two pairs of flip-flops, in which the present invention may be implemented.

FIG. 4 is a flow chart outlining the steps taken in one embodiment of method and/or algorithm of the present invention.

FIG. 5 is a diagram showing a preferred embodiment of the present invention.

FIG. 6 shows a simplified layout showing a number of signal paths between clocked circuit components, further illustrating an exemplary operation of the present invention.

FIG. 7 is a set of waveforms for illustrating how the invention operates with respect to the layout of FIG. 6.

FIG. 8 is an exemplary box-level chip design, in which the present invention may be implemented.

FIG. 9 is an exemplary computer system, in which the present invention may be implemented.

## **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be readily apparent to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail so as not to unnecessarily obscure aspects of the present invention.

Some portions of the detailed descriptions which follow are presented in terms of processes, procedures, logic blocks, functional blocks, processing, and other symbolic represen-

US 7,823,112 B1

3

tations of operations on code, data bits, data streams or waveforms within a computer, processor, controller and/or memory. These descriptions and representations are generally used by those skilled in the data processing arts to effectively convey the substance of their work to others skilled in the art. A process, procedure, logic block, function, process, etc., is herein, and is generally, considered to be a self-consistent sequence of steps or instructions leading to a desired and/or expected result. The steps generally include physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical, magnetic, optical, or quantum signals capable of being stored, transferred, combined, compared, and otherwise manipulated in a computer or data processing system. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, waves, waveforms, streams, values, elements, symbols, characters, terms, numbers, or the like, and to their representations in computer programs or software as code (which may be object code, source code or binary code).

It should be borne in mind, however, that all of these and similar terms are associated with the appropriate physical quantities and/or signals, and are merely convenient labels applied to these quantities and/or signals. Unless specifically stated otherwise and/or as is apparent from the following discussions, it is appreciated that throughout the present application, discussions utilizing terms such as "processing," "operating," "computing," "calculating," "determining," "manipulating," "transforming," "displaying" or the like, refer to the action and processes of a computer or data processing system, or similar processing device (e.g., an electrical, optical, or quantum computing or processing device), that manipulates and transforms data represented as physical (e.g., electronic) quantities. The terms refer to actions and processes of the processing devices that manipulate or transform physical quantities within the component(s) of a system or architecture (e.g., registers, memories, other such information storage, transmission or display devices, etc.) into other data similarly represented as physical quantities within other components of the same or a different system or architecture.

Furthermore, in the context of this application, the terms "net list" and "hardware description" may be used interchangeably to refer to a circuit design represented in an appropriate language, such as VERILOG, HDL or VHDL. Similarly, the terms "wire," "wiring," "line," "signal," "conductor" and "bus" refer to any known structure, construction, arrangement, technique, method and/or process for physically transferring a signal from one point in a circuit to another. Also, unless indicated otherwise from the context of its use herein, the terms "known," "fixed," "given," "certain" and "predetermined" generally refer to a value, quantity, parameter, constraint, condition, state, process, procedure, method, practice, or combination thereof that is, in theory, variable, but is typically set in advance and not varied thereafter when in use.

Similarly, for convenience and simplicity, the terms "clock," "time," "timing," "rate," "period" and "frequency" are, in general, interchangeable and may be used interchangeably herein, but are generally given their art-recognized meanings. Also, for convenience and simplicity, the terms "data," "data stream," "waveform" and "information" may be used interchangeably, as may (a) the terms "flip-flop," "latch" and "register," and (b) the terms "connected to," "coupled with," "coupled to," and "in communication with," but these terms are generally given their art-recognized meanings herein.

4

The present invention concerns a method and/or algorithm (e.g., a computer-readable set of instructions) for placing circuit elements and routing wires, comprising the steps of (a) determining a boundary condition for signal paths between components in a circuit, wherein each of the components receives a clock signal and a plurality of the signal paths comprise  $n$  wires and  $(n-1)$  circuit elements in alternating serial communication between the components,  $n$  being an integer of 2 or more; and (b) placing the circuit elements and routing the wires between the components and the circuit elements such that no signal path in the circuit exceeds the boundary condition. In preferred embodiments, the boundary condition comprises a maximum length, and the method further comprises placing the clocked components in a floor plan such that no signal path in said circuit can exceed said boundary condition.

In a further aspect of the invention, the method relates to verifying a circuit design, comprising the steps of determining whether, in a floor plan corresponding to said circuit, any of a plurality of signal paths between components receiving a clock signal exceeds a boundary condition, where each of the signal paths comprise  $n$  wires and  $(n-1)$  circuit elements in alternating serial communication,  $n$  being an integer of 2 or more; and if any of said signal paths exceeds said boundary condition, then (i) re-placing at least one of said circuit elements and/or said circuit components in a different location in said floor plan, and (ii) re-routing said wires between replaced circuit elements and/or circuit components such that no signal path in said circuit exceeds said boundary condition.

In a further aspect of the invention, the software relates to a medium or waveform containing a computer-readable set of instructions, where the instructions comprise (a) calculating a boundary condition for all signal paths between components in a circuit, wherein each of said components receives a timing signal in a common clock domain and a plurality of said signal paths independently comprise  $n$  wires and  $(n-1)$  circuit elements in alternating serial communication between said components,  $n$  being an integer of 2 or more; and (b) placing said circuit elements and routing said wires between said components such that no signal path in said circuit exceeds said boundary condition. In an even further aspect of the invention, the system comprises a general purpose computer or workstation that includes the present software and is configured to execute the steps of the present method(s) and/or algorithm(s).

In a further aspect of the invention, the chip or circuit architecture comprises at least one block of circuitry having a plurality of signal paths, each of the signal paths comprising (a) first and second components at the endpoints thereof, and (b) at least two wires and at least one combinational circuit element alternately, serially coupled between said first and second components, wherein each component receives a clock signal and each signal path does not exceed a predetermined boundary condition.

The invention further relates to hardware and/or software implementations of the present architecture, method and system. The invention, in its various aspects, will be explained in greater detail below with regard to exemplary embodiments.

#### F-Arcs and an Exemplary Implementation of the Invention

FIG. 1 shows a simple signal or data path 10 from a first circuit component 12 receiving a clock signal (e.g., CLOCKX) to a second circuit component 14 receiving the same clock signal. Between first and second circuit components 12 and 14 are circuit elements 16, 18, 20 and 22.

## US 7,823,112 B1

5

Signal/data path **10** is a very simple example of an F-arc. Generally, an "F-arc" is considered herein to be a signal path having two components at its endpoints and a series of alternating wires and combinational circuit elements between the two components, where the components receive a common clock signal (e.g., the same clock or logically equivalent clocks).

First and second circuit components **12** and **14**, which may be the same or different, are generally any circuit or device configured to operate under the control of, or in response to, a clock signal. First and second circuit components **12** and **14** may be edge- or voltage level-controlled or -triggered. Examples of suitable circuit components include storage or memory components, such as a flip-flop, a latch or a register; switches or gates, such as a transistor configured to receive the clock signal at its gate; a counter; a synchronous adder or subtractor; a divider or multiplier; parallel combinations thereof; etc. Preferably, circuit components receiving a clock signal comprise a flip-flop or a register.

Circuit elements **16**, **18**, **20** and **22**, which may be independently selected, are generally any circuit or device not configured to receive a clock signal. Suitable examples include an inverter or a buffer (e.g., an even-numbered series of inverters, typically 2 inverters in series, which may be 3-statable or configured to be placed in a "high z" state); a switch or transistor receiving a control signal (other than a clock) at its gate; a logic gate (such as an AND, OR, NAND, NOR, or XOR gate); a multiplexer or demultiplexer; a comparator, encoder or decoder; an combinational adder or subtractor; parallel or serial combinations thereof; etc. While the invention focuses on F-arc signal paths having at least one circuit element therein, preferably the signal paths include at least 2 circuit elements, and more preferably at least 3 circuit elements. While the upper limit of circuit elements is constrained only by the design and fabrication technology available, typical upper limits in a 0.15 or 0.18 micron fabrication technology and design are on the order of 15-20 circuit elements.

Similarly, the length of wires has upper and lower limits constrained only by the design and fabrication technology available. However, typical lower limits in a 0.15 or 0.18 micron fabrication technology and design are on the order of 4× the minimum feature dimension of the immediately underlying layer (e.g., for a 0.15 micron wide transistor, a minimum length for the first layer of metal is about 0.6 microns), while typical upper limits in a 0.15 or 0.18 micron fabrication technology and design are on the order of about 1000 microns (preferably about 500 microns).

In general, the invention relies on a boundary being placed on the maximum length of an F-arc. This maximum length may be based on input data relating to characteristic properties of the fabrication process used to make the circuit and/or provide timing signals to the circuit. Such input data generally include (i) a period or frequency of the clock signal, (ii) a resistivity of the wire in the F-arc, (iii) an operating voltage and/or (iv) a characteristic resistivity or time delay contributed by each circuit element in the F-arc. However, for design rules at or below 0.18 microns, the characteristic resistivity or time delay contributed by each circuit element may be negligible in comparison with the time delays contributed by the wires, and may be ignored or taken into account by a simple approach. For convenience and/or simplicity, one may simply factor in a potential maximum delay that could be caused by a combination of circuit elements and processing and operational "corners (e.g., processing and/or fabrication variations, operating voltage fluctuations, etc.), and decrease the appli-

6

cable length of time (e.g., the clock period or fraction or multiple thereof) by that potential maximum delay.

In certain embodiments, the method and/or algorithm further include identifying, defining or specifying an F-arc as any combinational path between two clocked circuit components. One skilled in the art understands how to identify in a net list (or hardware description) circuit components receiving a clock signal, combinational circuit elements and wires (or "nets") between such combinational circuit elements or between such a circuit component and a combinational circuit element. One skilled in the art understands also how to write code (which in one embodiment, may be source code) that will predict certain properties and/or characteristics for F-arcs, compare such properties and/or characteristics for each F-arc identified against a boundary and determine whether each such F-arc is allowed or disallowed, and (iteratively) re-place circuit components and elements and/or re-route wires so that all identified F-arcs are allowed. The boundary condition identified against each F-arc may be determined empirically.

The wires themselves may directly link only two combinational circuit elements or a combinational circuit component and a combinational circuit element, or they may be branched (e.g., linking a combinational circuit element to two or more combinational circuit elements or vice versa, or a clocked circuit component to two or more combinational circuit elements or vice versa). The inventive method also encompasses further embodiments where the signal path in an additional F-arc has no combinational circuit elements, but instead, includes only a wire (which may comprise two or more segments as discussed above).

Furthermore, there is no maximum limit to the number of F-arcs to which the method and/or algorithm can be applied. However, circuit designers generally attempt to keep designs as small as possible and/or feasible, while still achieving desired functionality and/or performance. These "natural" constraints will generally tend to limit the number of F-arcs in a circuit, circuit block or chip design. However, in a typical design of moderate to high complexity, there will be at least a million F-arcs to be placed and routed, frequently several million F-arcs or more, and occasionally 10 million or more F-arcs.

In the simplest case, the boundary placed on the F-arc corresponds to the period of one clock cycle. In other words, an F-arc violates the boundary condition if it takes longer than one clock cycle for a signal to traverse the F-arc. Of course, other boundary conditions may apply, such as one-half of a clock cycle (e.g., for two components defining the endpoints of an F-arc that receive complementary clock signals CLOCK and CLOCKb), or x clock cycles, where x is an integer of at least 2. One skilled in the art is capable of designing circuitry configured to account for and/or control such conditions.

The wire resistivity is generally known from the process technology to be used for fabricating the device being designed. The wire resistivity may be characterized as a sheet resistance, a bulk resistivity, or other known resistance or resistivity parameter, and it may be calculated for a given wire from such resistance or resistivity and the height and width of the wire (which are also known for a known process technology).

The time delay is generally a constant value for a given circuit element having certain dimensions in a known process technology. For example, a transistor of a known type and having predetermined dimensions in a given process technology will generally cause a delay of known or calculable length in a signal changing states. Furthermore, operating voltages are generally standard or predetermined values for a



## US 7,823,112 B1

7

given minimum transistor dimension (generally width). As a result, a given set of design rules for a given process technology will generally have a fixed and/or predetermined operating voltage.

Now referring to FIG. 2, two different exemplary waveforms, CLOCK1 and CLOCK2, are shown for the generic clock signal, CLOCKX. CLOCK1 has a relatively long period and low frequency, and CLOCK2 has a relatively short period and high frequency. Although the exemplary clock signal CLOCK1 is shown having a period twice that of CLOCK2, this is simply for ease of illustration only.

The state of a signal along exemplary F-arc 10 can be determined at nodes A, B, C and D (respectively, along the wires immediately downstream from circuit elements 16, 18, 20 and 22) at certain times. As shown by the waveforms in FIG. 2, component 12 is a negative edge-triggered component. The state of the signal at node A may change a certain time  $t_1$  after CLOCKX changes state. Similarly, the state of the signal at nodes B, C and D may change a certain time  $t_2$ ,  $t_3$  and  $t_4$ , respectively, after the negative edge of CLOCKX is received at component 12. To a first approximation, the signal is received by component 14 immediately after the characteristic time that node D can change state,  $t_4$ .

In this example, for simplicity, the maximum F-arc length is determined in part on a one clock period length of time. When CLOCK1 is operable,  $t_4$  is less than one period of CLOCK1, and the length of F-arc 10 falls comfortably below the CLOCK1-defined maximum. On the other hand, since  $t_4$  is greater than one period of CLOCK2, when CLOCK2 is operable, the length of F-arc 10 exceeds the boundary condition defined in part by the CLOCK2 period.

F-arcs that exceed the maximum length boundary are disallowed. By doing so, the present invention ensures that signal propagation timing requirements are met in a circuit, circuit block and/or circuit design receiving a particular clock. In the present invention, the clock signal need not be the same signal for all timing-controlled components on a chip, only that the signal or a logical equivalent thereof (e.g., an integer multiple and/or divisor thereof, complement thereof, etc.) be supplied to all such components within a given circuit or block of circuitry. In other words, the invention applies a maximum boundary condition on all F-arcs within a common clock domain.

Thus, in one aspect, the invention concerns a method of placing and routing, comprising the steps of (a) determining a maximum length of a signal path between components in a circuit, and (b) placing circuit elements and routing wires between the components such that no signal path in the circuit has a length exceeding the maximum length. In the invention, the signal path generally contains two or more wires and one or more circuit elements, and each of the components receives a clock signal. Generally, the circuit elements do not receive the clock signal.

In further embodiments, the method further includes the step(s) of routing or distributing the clock signal to the components; placing the components and/or circuit elements in a floor plan corresponding to said circuit; and/or routing the wires from a first component to one or more first circuit elements, and from one or more first circuit elements to either one or more second circuit elements or said second component. In even further embodiments, wires can be routed along any number of circuit elements, as long as the final wire in the signal path is to a second component and as long as the maximum boundary condition on F-arcs is not violated.

Alternatively, as will be readily apparent to those skilled in the art, a maximum F-arc length is but one boundary condition encompassed by the present invention. Other exemplary

8

F-arc boundary conditions, which may be related to time, length, resistance and/or other physical properties of an F-arc, include a maximum time or delay for signal propagation along the F-arc, a maximum resistance and/or capacitance, a maximum or minimum inductance, a maximum and/or minimum impedance (depending on the states of the F-arc, the second component and/or the circuitry downstream from the second component), etc.

#### Exemplary Application #1

Referring now to FIG. 3, a functional circuit block 100 may comprise an array of logic elements 110a-110j that process data signals  $D_{IN1}$  and  $D_{IN2}$ , respectively received at input nodes 102 and 104, and outputs data signals  $D_{OUT1}$  and  $D_{OUT2}$  at output nodes 106 and 108, respectively. Data signals  $D_{IN1}$  and  $D_{IN2}$  are clocked into flip-flops 112 and 114, and data signals  $D_{OUT1}$  and  $D_{OUT2}$  are clocked out of flip-flops 116 and 118, by a timing signal CLOCK. As mentioned above, flip-flops 112, 114, 116 and 118 are exemplary circuit components receiving a timing signal within a common clock domain, and logic elements 110a-110j are examples of circuit elements (generally comprising one or more transistors, or preferably, one or more buffers) that do not receive a clock signal. Thus, for the purposes of explaining the invention, circuit elements that do not receive a clock signal may be considered "combinational."

The circuit elements are electrically coupled to each other and to circuit components by wires, as shown in FIG. 3. When actually fabricated, the wires may be located on the same or different layers of metallization in the chip, and may individually comprise one or more wire segments, electrically coupled to each other and/or to circuit elements by contacts or vias. Each of the wire segments and the contacts or vias contributes to the length and/or propagation/delay time of the F-arc. Furthermore, there is no defined or specific relationship between the locations of circuit element depictions 110 in FIG. 3 and the locations of actual, physical circuit elements in the fabricated chip. However, there may be a general correlation in that circuit element depictions 110 that are proximate to each other in FIG. 3 (e.g., 110c and 110b) are likely to correspond to physical circuit elements that are proximate to each other on the fabricated chip (or at least relatively closer to each other than to relatively distant circuit elements in the depiction in FIG. 3), and circuit element depictions 110 that are relatively distant from each other in FIG. 3 (e.g., 110a and 110j) are likely to correspond to physical circuit elements that are relatively distant from each other on the fabricated chip.

In another aspect, the present invention concerns a method, algorithm and software that determines or calculates an F-arc boundary condition from certain input data, then places combinational circuit elements and routes wires that enable electrical communication to form F-arcs such that F-arcs that exceed the boundary condition are disallowed. A flow chart outlining an exemplary embodiment 200 of the method and/or algorithm is shown in FIG. 4.

In the general method and/or algorithm of the invention, input data relating to characteristic properties of the fabrication technology and/or timing signals for the circuit being designed are input into the design software (see step 210 of FIG. 4). In some embodiments, such input data may be automatically generated and/or received by the design software by selection or designation of the fabrication process and/or operating frequency of an internal or external (master) clock signal. From this input data, the F-arc boundary condition is calculated (see step 220 of FIG. 4). In preferred embodiments, the F-arc boundary condition is a maximum length or maximum time delay, more preferably a maximum length.

## US 7,823,112 B1

9

In parallel or in serial fashion, components of the circuit receiving a clock or timing signal are placed in a floor plan corresponding to the physical circuit being designed. In one embodiment, such components are placed without reference to the F-arc boundary condition (e.g., before determining or calculating the F-arc boundary condition, or in parallel with such determination or calculation). In another (and preferred) embodiment, the method and/or algorithm places such components in the floor plan in a manner disallowing any placement that will exceed or violate the boundary condition (e.g., components are placed after determining or calculating the F-arc boundary condition). Now referring to FIG. 5, in an even more preferred embodiment, the floor plan 300 comprises a plurality or array of tiles 302aa-302zz, and the method and/or algorithm places components 304 in at least a subset of the tiles in an array or a regular or evenly-spaced pattern 306 (also see U.S. patent application Ser. No. 10/452, 811, filed May 30, 2003 and incorporated herein by reference).

Referring back to FIG. 3, components 112, 114, 116 and 118 have been placed with regular spacing between components. For example, the distance between individual "input" components (i.e., components 112 and 114) is the same as the distance between individual "output" components (i.e., components 116 and 118). Also, the distance between any "input" component and its nearest "output" component (e.g., components 112 and 116, or 114 and 118) is the same. However, the invention is not so constrained; clocked circuit components can be placed in any allowed location, preferably such that the F-arc boundary condition is not violated. Thus, all of the possible signal paths in FIG. 3, from any "input" component to any "output" component along any possible series of wires and circuit elements 110, have a length below the maximum allowed F-arc length.

Thus, the invention is not only useful for preventing disallowed F-arcs (e.g., ensuring intra-circuit timing between clocked components "by design"), but also for detecting or finding erroneously placed and/or routed F-arcs, and optionally, replacing components or combinational circuit elements and rerouting wires to correct such design errors. Consequently, in further embodiments, the inventive method and/or algorithm may be included as part of a circuit design verification tool, in which timing of a fully placed and routed circuit is verified at a number of levels, from chip input pin to chip output pin, circuit block input node to circuit block output node, clock domain input node to clock domain output node, and/or (as described herein) F-arc input component to F-arc output component.

Although specific steps are disclosed in regard to the operation of the exemplary method and/or algorithm of FIG. 4, such steps are exemplary. That is, the present invention is well suited to use with various other steps or variations of the steps described above. Additionally, for purposes of clarity and brevity, the discussion herein is directed at times to specific examples. The present invention, however, is not limited solely to use with a particular architecture, method, process, software tool or device. Instead, the present invention is well suited to use with other architectures, software, circuitry, methods and processes in which it may be desirable to accomplish a multitude of tasks as part of an overall process directed at ensuring timing at a clocked circuit component level.

Further examples of suitable systems, tools and/or methods in which the present invention is generally applicable include those described in, e.g., U.S. Pat. Nos. 6,080,201, 6,212,489, 5,798,936 and 5,550,748, the relevant portions of which are each incorporated herein by reference, and those commercially available from place-and-route software vendors such

10

as Cadence Design Systems (e.g., the SILICON ENSEMBLE™, SILICON ENSEMBLE-PKST™, FIRST ENCOUNTER™, and NANO ENCOUNTER™ tools), Silicon Valley Research, Inc. (e.g., the QIC/APR™, GARDST™, SCT™ and FLOORPLACER™ tools), Synopsis (e.g., the CHIP ARCHITECT™, DESIGN COMPILER™, and FLOORPLAN COMPILER™ tools) and Mentor Graphics (e.g., the AUTOCELLS™ tool).

## Exemplary Application #2

FIG. 6 shows a simplified, exemplary circuit layout 400 comprising F-arcs 402, 404, 406 and 408, for further illustrating the present invention. In general, component and signal/bus numbers common to both FIGS. 3 and 6 reflect the suitability of the same structures, signals and/or functions for both of the exemplary embodiments. However, these examples do not require that the same component(s), signal(s), bus(es) and/or function(s) be used or implemented in both examples, other than as specifically described herein.

Input data or signals are received by clocked circuit components 412, 414, 422 and 424, which store or hold the data or signal on the appropriate edge, transition and/or logic level of the clock, in accordance with conventional design. For clarity, the clock signal is not shown in FIG. 6. The data or signals are propagated in parallel through a series of combinational circuit elements 410a-410c, 420a-420f, 430a-430e and 440a-440d, and are input into or stored in "output" components 416, 418, 426 and 428 on the next appropriate clock edge or level. Block 450 is a disallowed placement area (e.g., it is devoted to a circuit function such as memory/storage, signal and/or data processing, clock signal generation, power/current transmission, etc.).

One issue the invention addresses is placing circuit components and elements and routing wires around disallowed placement areas. Again, for purposes of illustrating the invention, input components 412 and 414 are complementary to input components 422 and 424 with respect to the A-A' axis bisecting disallowed placement area 450, and output components 416 and 418 are similarly complementary to output components 426 and 428. If a circuit design requires routing signals from a set of input components, around bisecting disallowed placement area 450, to a set of output components, the invention provides a tool by which such routing can be accomplished while ensuring that timing constraints are met at the level of clocked components, such as flip-flops, latches and registers.

Referring now to FIG. 7, for purposes of illustration, the F-arc boundary is based on a one clock period length of time. F-arc 402, which is relatively short in comparison to the other F-arcs of FIG. 6, easily falls below the boundary condition. However, F-arc 404, which is relatively long in comparison to the other F-arcs of FIG. 6, exceeds the boundary condition. Such a circuit element placement and wire routing would be disallowed by the present invention.

On the other hand, F-arcs 406 and 408, which have lengths intermediate to those of F-arcs 402 and 404, both fall below the boundary condition. Consequently, this placement is allowed by the present invention, and the present invention would automatically place combinational circuit elements and wires (and optionally, components receiving a clock signal) in this manner rather than as shown for F-arcs 402 and 404.

## An Exemplary Chip Architecture and/or Design

FIG. 8 shows an exemplary architecture and/or a chip-level design 500, comprising a plurality of functional blocks and/or clock domains 510a-510i, wherein at least 1 (and preferably at least 2) of the functional blocks and/or clock domains are designed according to the method(s) described above. Func-



## US 7,823,112 B1

11

tional blocks and/or clock domains **510a-510i** are individually connected with other functional blocks and/or clock domains via wires or busses, which may be single bit or multi-bit, and which may comprise a single wire segment or multiple wire segments as described above. In general, a “functional block” is a block of circuitry that physically occupies an area on a chip defined by a single border (although the border may be arbitrary in shape and/or dimensions), and a “clock domain” is circuitry that receives a common clock signal or its logical equivalent, in order to have certain events within the circuitry occur at expected and/or predetermined times. Preferably, the invention applies to a chip having at least 2 clock domains, and each clock domain comprises one or more functional blocks.

This, the invention further relates to a chip architecture, in which at least one block of circuitry comprises a plurality of signal paths, each of the signal paths having first and second components at the endpoints thereof and comprising at least 2 wires and at least 1 combinational circuit element alternately and serially coupled between the first and second components, in which each component receives a clock signal (the same clock signal or a logical equivalent thereof) and each signal path does not exceed a predetermined boundary condition. In preferred embodiments, the block of circuitry comprises components that are regularly spaced from the nearest component thereto, and the boundary condition comprises a maximum length.

Naturally, the invention is not limited to a design having the same number or configuration of blocks **510** and/or wires. However, in preferred embodiments, the chip design has at least 2 such blocks, more preferably at least 4 such blocks, that are coupled at least to physically adjacent blocks by either (i) a plurality of single-bit wires, or (ii) at least one multi-bit bus. For example, in FIG. 8, blocks **510a-c** may each operate according to a common clock signal, in which case at least one of the wires between blocks so operating electrically communicates the clock signal from one block to the other block. In addition, blocks **510d-i** may each operate in a common clock domain, in which case one of the blocks provides a clock generation, clock replication and/or clock recovery function, and at least one of the wires from the block providing such clock function(s) to the other block(s) electrically communicates the generated, replicated and/or recovered clock signal.

An Exemplary System for Performing the Present Method

Referring now to FIG. 9, in a further aspect of the invention, the system comprises at least one computer system **600**, which may form a platform for practicing embodiments of the invention. Computer system **600** includes an address/data bus **609** for communicating information, a central processor **601** coupled with the bus for processing information and instructions, a volatile memory **602** (e.g., random access memory or RAM) coupled with the bus **609** for storing information and instructions for the central processor **601**, and a non-volatile memory **603** (e.g., read only memory or ROM) coupled with the bus **609** for storing static information and instructions for the processor **601**. Computer system **600** also includes a data storage device **604** (e.g., a magnetic or optical disk and disk drive) coupled with the bus **609** for storing information and instructions. With reference still to FIG. 9, system **600** of the present invention also includes an optional alphanumeric input device **606** including alphanumeric and function keys (e.g., a conventional keyboard). Alphanumeric input device **606** may be coupled to bus **609** for communicating information and command selections to central processor unit **601**. System **600** also optionally includes a cursor control device **607** (e.g., a conventional mouse) coupled to bus **609** for

12

communicating user input information and command selections to central processor unit **601**. System **600** also includes an optional display device **605** (e.g., a conventional monitor) coupled to bus **609** for displaying information. One or more signal input/output communication devices **608** coupled to bus **609** may provide communication with external devices.

The present invention has particular advantage in integrated circuits having moderate to high logic complexity, such as microprocessors, digital signal processors, field programmable gate arrays (FPGAs), complex programmable logic devices (CPLDs), and speech recognition chips.

## CONCLUSION/SUMMARY

Thus, the present invention provides a convenient, simple and efficient architecture, method and system for. The present method, system and architecture greatly, enabling one to, and improve.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.

What is claimed is:

1. A method of placing and routing, comprising:

- a) determining a boundary condition for signal paths between components at endpoints of said signal paths in a circuit, wherein each of said components receives a clock signal and a plurality of said signal paths comprise  $n$  wires and  $(n-1)$  circuit elements in alternating serial communication between said components,  $n$  being an integer of 2 or more; and
- b) using a computer or data processing system, placing said circuit elements and routing said wires between said components and said circuit elements such that no signal path in said circuit exceeds said boundary condition, wherein said boundary condition is based on (i) a period or frequency of said clock signal and (ii) a resistivity of said wires.

2. The method of claim 1, wherein said boundary condition comprises a maximum propagation time or a maximum length of said signal paths.

3. The method of claim 2, wherein said boundary condition comprises a maximum length of said signal paths.

4. The method of claim 1, further comprising the step of routing said clock signal to said components.

5. The method of claim 1, wherein said clock signal received by each of said components is the same clock signal or a logical equivalent thereof.

6. The method of claim 1, further comprising the step of placing said components, elements, and wires in a floor plan corresponding to said circuit.

7. The method of claim 6, wherein said components are placed in said floor plan such that no signal path in said circuit exceeds said boundary condition.

8. The method of claim 7, wherein placing said components in said floor plan comprises regularly spacing said

US 7,823,112 B1

13

components at first endpoints of said signal paths from a nearest component at a second endpoint of each of said signal paths in said floor plan.

9. The method of claim 6, wherein placing said components in said floor plan comprises regularly spacing at least a subset of said components at first endpoints of said signal paths from a nearest component at a second endpoint of each of said signal paths.

10. The method of claim 6, further comprising determining whether any of a plurality of signal paths exceeds said boundary condition, and if any of said signal paths exceeds said boundary condition, then:

- i) re-placing at least one of said elements and/or said components in a different location in said floor plan, and
- ii) re-routing said wires between said re-placed elements and/or components such that no signal path in said circuit exceeds said boundary condition.

11. The method of claim 10, wherein said determining comprises calculating said boundary condition from circuit parameters comprising (i) a period or frequency of said clock signal and (ii) a resistivity of said wire.

12. The method of claim 11, wherein said circuit parameters further comprise (iii) a characteristic resistivity or time delay associated with each circuit element.

13. The method of claim 1, wherein said circuit elements do not receive said clock signal.

14. The method of claim 13, further comprising the step of placing said components and said circuit elements in a floor plan corresponding to said circuit.

15. The method of claim 14, further comprising the step of routing said clock signal to said components.

16. The method of claim 15, wherein said clock signal received by each of said components is the same clock signal or a logical equivalent thereof.

17. The method of claim 1, wherein said boundary condition is further based on (iii) a characteristic resistivity or time delay associated with each circuit element.

18. The method of claim 1, wherein said determining comprises calculating said boundary condition from (i) said period or frequency of said clock signal and (ii) said resistivity of said wire.

19. The method of claim 1, wherein said boundary condition is determined empirically from input data.

20. The method of claim 1, wherein said components comprise a first component at a first endpoint and a second component at a second endpoint of each of said signal paths.

21. A non-transitory computer-readable medium comprising a computer-executable set of instructions, said instructions adapted to perform the steps of:

- a) calculating a boundary condition for all signal paths between components at endpoints of said signal paths in a circuit, wherein each of said components receives a timing signal in a common clock domain, a plurality of said signal paths independently comprise  $n$  wires and  $(n-1)$  circuit elements in alternating serial communication between said components,  $n$  being an integer of 2 or more, and said boundary condition is calculated from circuit parameters comprising (i) a period or frequency of said clock signal and (ii) a resistivity of said wires; and
- b) placing said circuit elements and routing said wires between said components such that no signal path in said circuit exceeds said boundary condition.

14

22. The non-transitory computer-readable medium of claim 21, wherein said boundary condition comprises a maximum propagation time or a maximum length of said signal paths.

23. A non-transitory computer system comprising the computer-readable medium of claim 22, configured to execute said computer-executable set of instructions.

24. The non-transitory computer-readable medium of claim 21, further comprising the step of placing said components, elements, and wires in a floor plan corresponding to said circuit such that no signal path in said circuit exceeds said boundary condition.

25. The non-transitory computer-readable medium of claim 24, wherein placing said components in said floor plan comprises regularly spacing said components at first endpoints of said signal paths from a nearest component at a second endpoint of each of said signal paths in said floor plan.

26. The non-transitory computer-readable medium of claim 24, wherein said circuit elements are placed in said floor plan.

27. The non-transitory computer-readable medium of claim 24, further comprising determining whether any of a plurality of signal paths exceeds said boundary condition, and if any of said signal paths exceeds said boundary condition, then:

- i) re-placing at least one of said elements and/or said components in a different location in said floor plan, and
- ii) re-routing said wires between said re-placed elements and/or components such that no signal path in said circuit exceeds said boundary condition.

28. The non-transitory computer-readable medium of claim 27, wherein said determining comprises calculating said boundary condition from circuit parameters comprising (i) a period or frequency of said clock signal and (ii) a resistivity of said wire.

29. The non-transitory computer-readable medium of claim 28, wherein said circuit parameters further comprise (iii) a characteristic resistivity or time delay associated with each circuit element.

30. A non-transitory computer system comprising the computer-readable medium of claim 27, configured to execute said computer-executable set of instructions.

31. The non-transitory computer-readable medium of claim 21, further comprising the step of routing said clock signal to said components.

32. The non-transitory computer-readable medium of claim 31, wherein said clock signal received by each of said components is the same clock signal or a logical equivalent thereof.

33. The non-transitory computer-readable medium of claim 21, wherein said circuit parameters further comprise (iii) a characteristic resistivity or time delay associated with each circuit element.

34. A non-transitory computer system comprising the computer-readable medium of claim 21, configured to execute said computer-executable set of instructions.

35. The non-transitory computer-readable medium of claim 21, wherein said components comprise a first component at a first endpoint and a second component at a second endpoint of each of said signal paths.

36. The non-transitory computer-readable medium of claim 21, wherein said circuit elements do not receive said clock signal.

\* \* \* \* \*

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 7,823,112 B1  
APPLICATION NO. : 10/449757  
DATED : October 26, 2010  
INVENTOR(S) : Mikhail Makarov et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page, item (57),

IN THE ABSTRACT

Line 9 of the Abstract: change “comments” to --components--.

IN THE SPECIFICATION

Column 11, line 15: change “This” to --Thus--.

IN THE CLAIMS

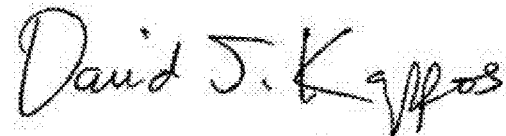
Column 12, Claim 3, line 54: change “a maximum length” to --said maximum length--.

Column 13, Claim 10, line 10: change “a plurality of signal paths” to --said plurality of signal paths--.

Column 13, Claim 18, line 40: change “said boundary condition” to --a boundary condition-- and change “said period” to --a period--.

Column 14, Claim 27, line 22-23: change “a plurality of signal paths” to --said plurality of signal paths--.

Signed and Sealed this  
Twenty-sixth Day of April, 2011

A handwritten signature in black ink, reading "David J. Kappos". The signature is written in a cursive, flowing style with a large initial 'D' and 'K'.

David J. Kappos  
*Director of the United States Patent and Trademark Office*

# **EXHIBIT D**

(12) **United States Patent**  
**Burstein et al.**

(10) **Patent No.:** **US 7,992,122 B1**  
(45) **Date of Patent:** **Aug. 2, 2011**

(54) **METHOD OF PLACING AND ROUTING FOR POWER OPTIMIZATION AND TIMING CLOSURE**

(75) Inventors: **Michael Burstein**, Cupertino, CA (US);  
**Boris Ginzburg**, Santa Clara, CA (US)

(73) Assignee: **GG Technology, Inc.**, San Jose, CA (US)

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 464 days.

(21) Appl. No.: **11/093,713**

(22) Filed: **Mar. 25, 2005**

(51) **Int. Cl.**  
**G06F 17/50** (2006.01)

(52) **U.S. Cl.** ..... **716/131**; 716/113; 716/124; 716/126; 716/130; 716/134; 703/19

(58) **Field of Classification Search** ..... 716/7, 10, 716/5, 6, 119, 124–126, 130, 132–134; 703/19  
See application file for complete search history.

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

6,230,304 B1 \* 5/2001 Groeneveld et al. .... 716/7  
6,453,446 B1 9/2002 van Ginneken  
6,507,941 B1 1/2003 Leung et al.  
6,519,745 B1 2/2003 Srinivas et al.

6,553,338 B1 4/2003 Buch et al.  
6,725,438 B2 4/2004 van Ginneken  
6,845,494 B2 1/2005 Burks et al.  
6,851,095 B1 2/2005 Srinivasan et al.  
2002/0112220 A1 \* 8/2002 Miller ..... 716/10  
2004/0031010 A1 \* 2/2004 Kaida ..... 716/12  
2006/0168551 A1 \* 7/2006 Mukuno ..... 716/5  
2006/0277520 A1 \* 12/2006 Gennari ..... 716/21

\* cited by examiner

*Primary Examiner* — Paul Dinh

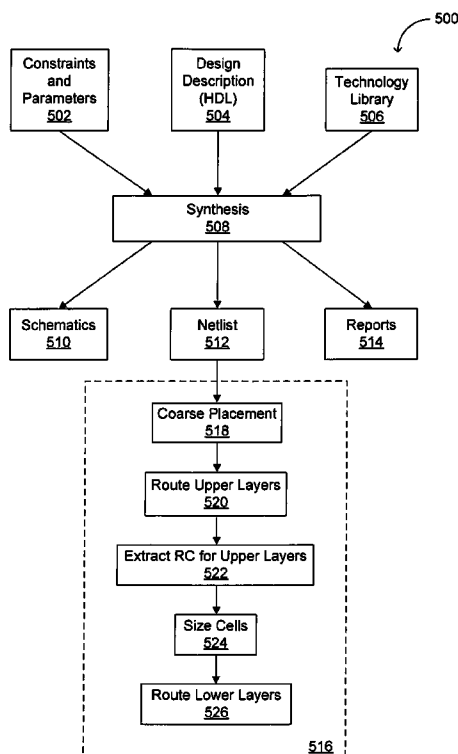
*Assistant Examiner* — Nha T Nguyen

(74) *Attorney, Agent, or Firm* — The Law Offices of Andrew D. Fortney; Andrew D. Fortney

(57) **ABSTRACT**

A method, algorithm, software, architecture and/or system for placing circuit blocks and routing signal paths or connections between the circuit blocks in a circuit design is disclosed. In one embodiment, a method of placing and routing can include: (i) routing signal paths in one or more upper metal layers for connecting circuit blocks; (ii) adjusting the circuit blocks based on electrical characteristics of the signal paths; and (iii) routing in one or more lower metal layers connections between the circuit blocks and the upper layers. The circuit blocks can include standard cells, blocks, or gates configured to implement a logic or timing function, other components, and/or integrated circuits, for example. Embodiments of the present invention can advantageously reduce power consumption and improve timing closure in an automated place-and-route flow.

**30 Claims, 6 Drawing Sheets**



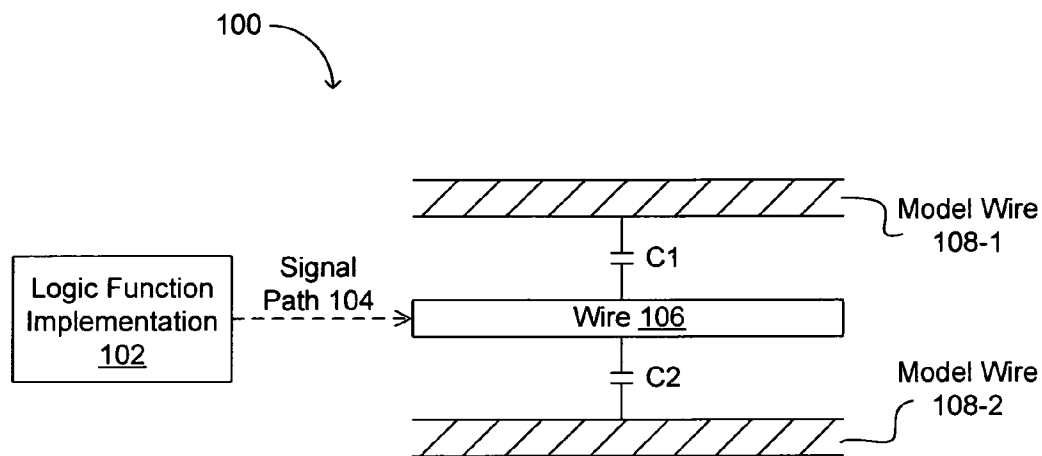


FIG. 1 (conventional)

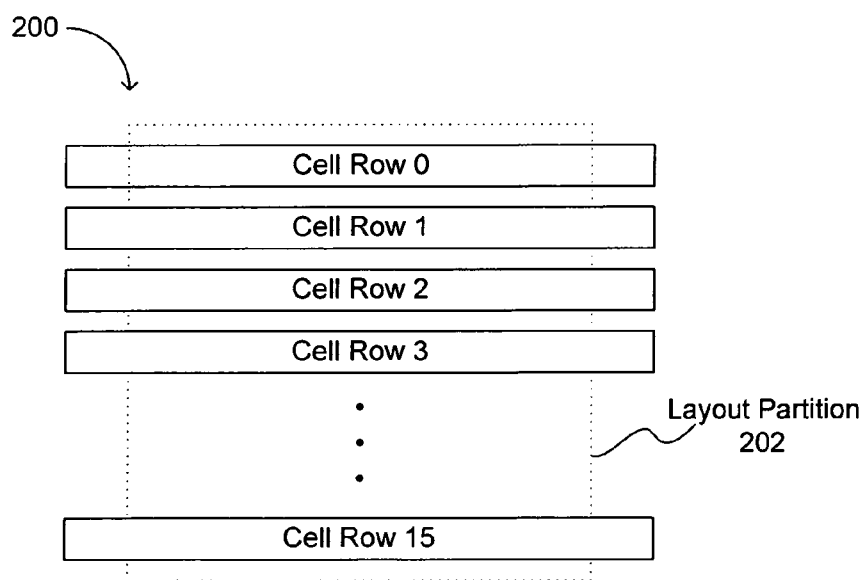


FIG. 2

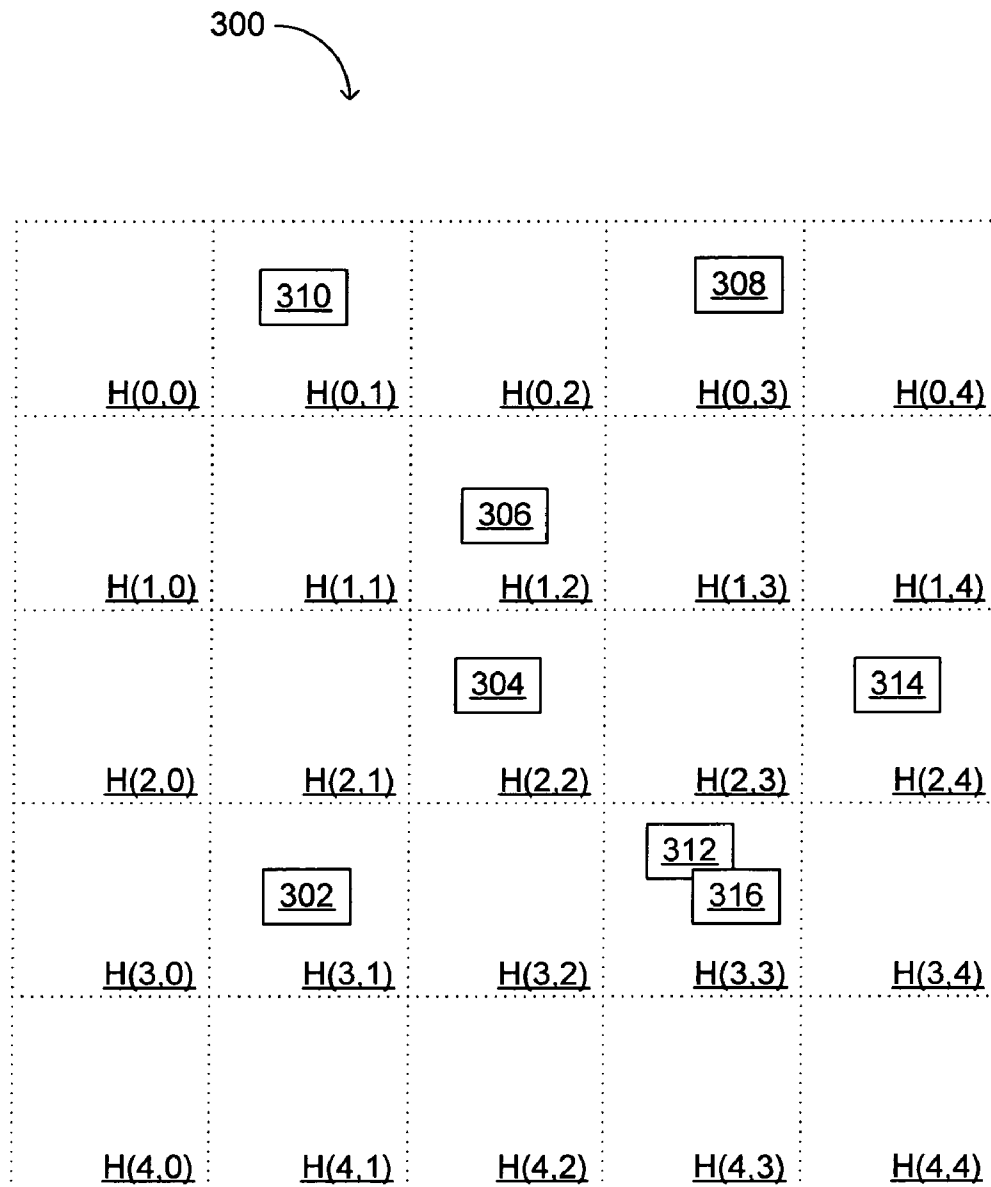


FIG. 3A

U.S. Patent

Aug. 2, 2011

Sheet 3 of 6

US 7,992,122 B1

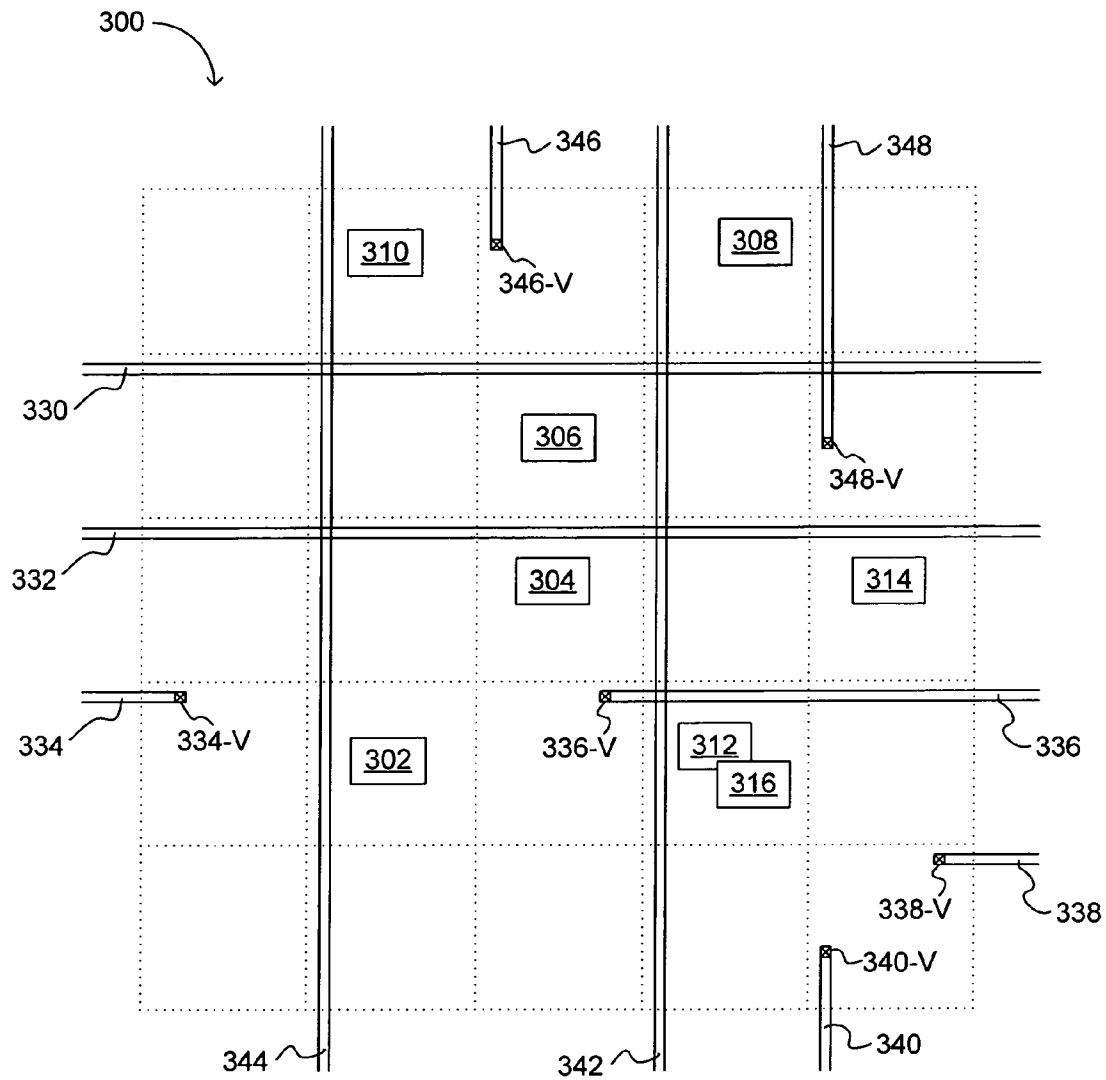


FIG. 3B



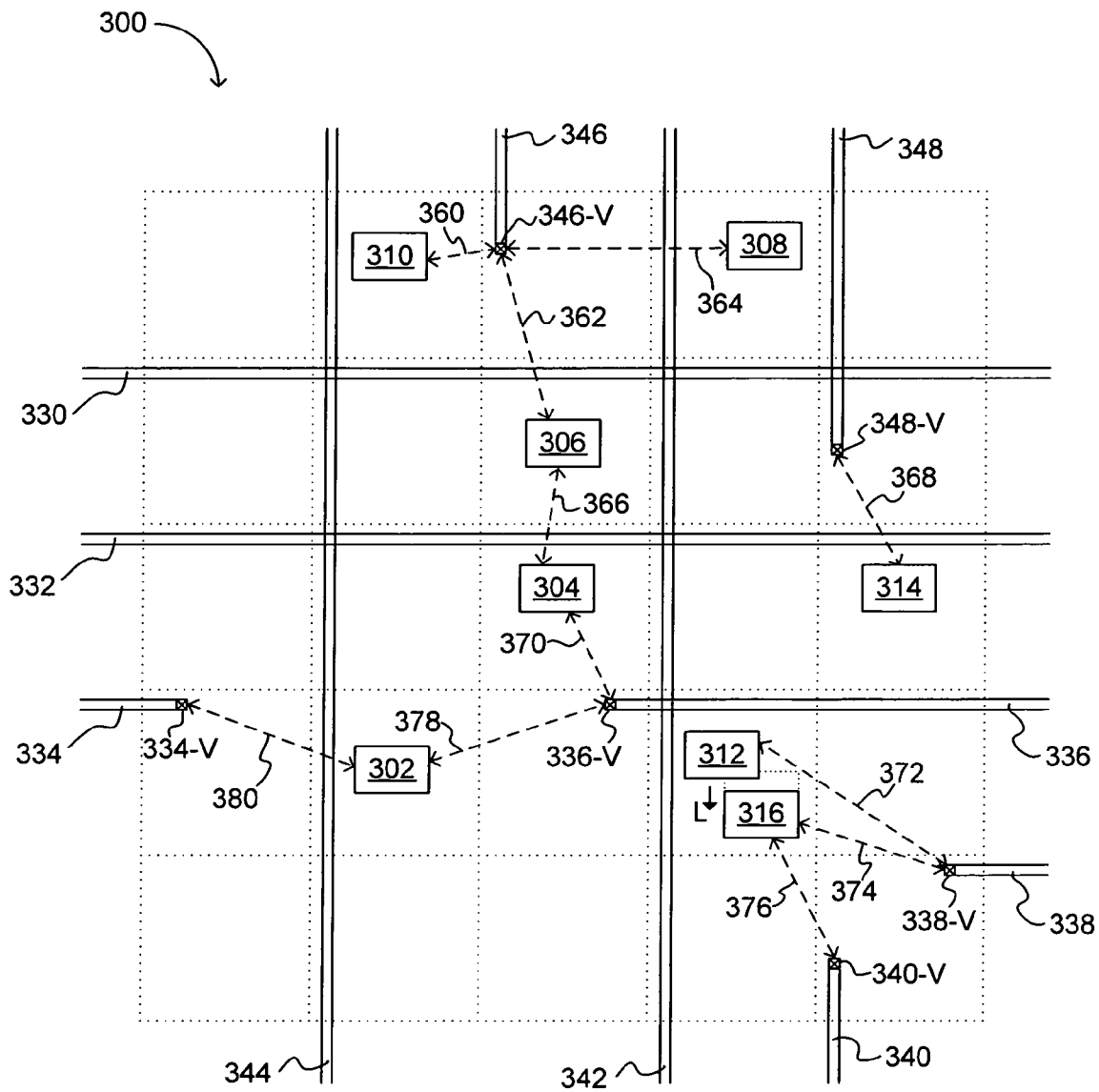


FIG. 3C

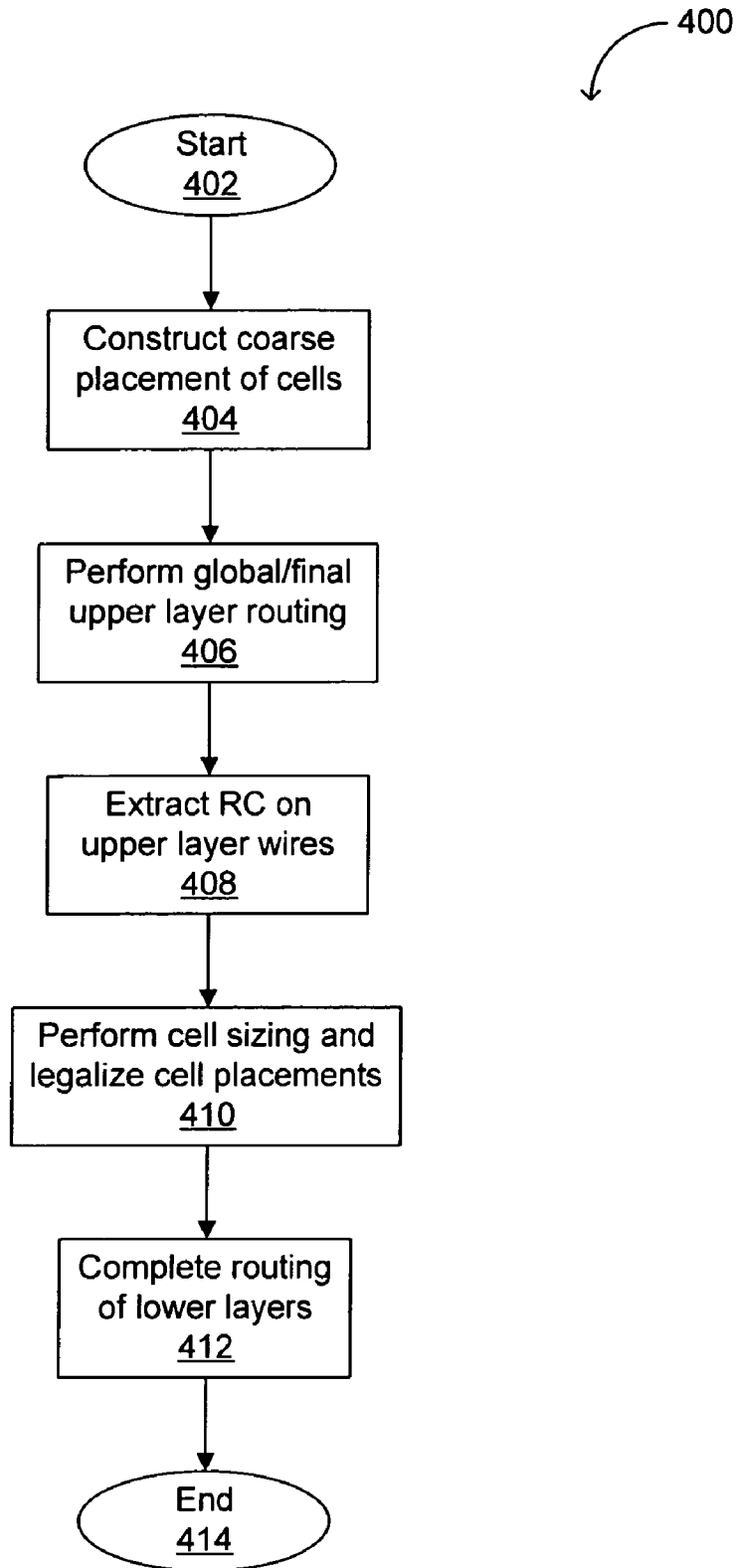
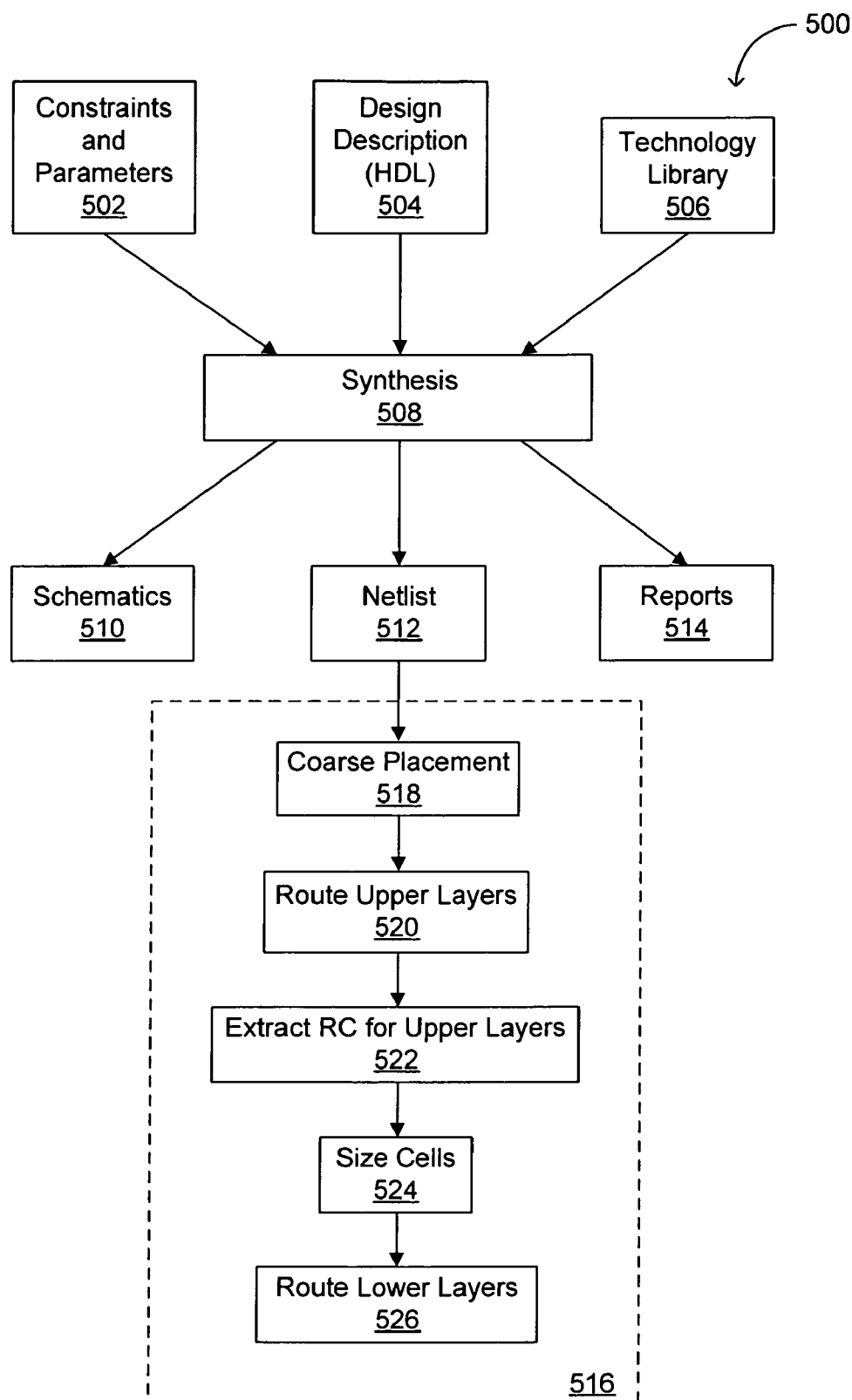


FIG. 4



US 7,992,122 B1

1

# METHOD OF PLACING AND ROUTING FOR POWER OPTIMIZATION AND TIMING CLOSURE

## FIELD OF THE INVENTION

The present invention generally relates to the field of circuit design, particularly integrated circuit (IC) design. More specifically, embodiments of the present invention pertain to methods, algorithms, software, systems and architectures for reducing power consumption in the design of an IC.

## DISCUSSION OF THE BACKGROUND

In typical circuit design, circuit components are arranged to optimize space and/or circuit performance. Such arrangements can include the "layout" or pattern definition of each of the layers used in a semiconductor manufacturing process. For example, such layout can include metal interconnect or connectivity layers that are converted to masks or reticles for use in a wafer fabrication facility that manufactures ICs (i.e., "chips").

While some circuits are designed using "custom" layout, others are designed using a partially or fully automated design flow. Application-Specific Integrated Circuit (ASIC) designs, as well as other functional blocks within a larger chip, such as System-On-Chip (SOC) designs, may employ custom and/or ASIC type flows on the same chip. In any event, typical ASIC flows use "place-and-route" tools for placing logic or circuit "blocks" and then "routing" or connecting the interface signals between the blocks. Such routing between circuit blocks is typically done using one or more metal connectivity layers for each signal path. In most modern ASIC designs, at least five layers of metal connectivity are employed.

In conventional place-and-route flows, circuit blocks or "cells" are first placed in desired locations and sized (i.e., adjust drive strength by changing transistor sizes and/or adding buffer stages) in accordance with a projected routing and capacitive load based on these desired cell locations. Then, signals are actually routed between the circuit blocks. A drawback of such an approach is that the cell sizing is done based on an estimated routing that typically provides capacitance values that are worse than the actual routing path. Referring now to FIG. 1, a conventional wire routing estimation approach is shown and indicated by the general reference character 100. Logic Function Implementation 102 can be any circuit block or cell that includes a driver stage to be sized in accordance with a resistance and capacitance (RC) load on Signal Path 104. Wire 106 can be a projected routed path or segment. Model Wire 108-1 can be an estimated wire route adjacent to (i.e., "above" or "below" on different routing layers or side-by-side on the same routing layer) Wire 106, contributing a capacitance C1. Similarly, Model Wire 108-2 can be another estimated wire route adjacent to Wire 106, contributing a capacitance C2. In essence, full coverage both above and below in different routing layers (and/or side-by-side on the same routing layer) would be assumed, making the capacitance estimate "worst case."

Conventionally, the circuit blocks or "cells" are sized in accordance with such a worst case RC estimate. As a result, the cells may be sized too large for the actual routed signal paths and power consumption due to overdriven and non-optimal signal driving based on the actual load could be greater than necessary. Further, this problem gets worse as more advanced processes result in increased capacitance values.

2

For timing considerations, obtaining "timing closure" in conventional approaches may be more difficult due to the worst case estimates and this may further exacerbate the power consumption problem. Typically, capacitances of the actual resultant signal paths are extracted and provided to a simulator and/or timing closure tool. If the circuit meets the timing specifications for the design, timing closure has been obtained. However, if the circuit fails timing closure, adjustments to the circuit block placement and/or routing must be done. This process must be repeated until timing closure is met, delaying the completion of the overall design. In particular, overdriven signals resulting from such conventional solutions are susceptible to hold time violations. The signal paths must then be re-routed and/or the cells re-sized as part of one or more iterations in order to ultimately meet the timing constraints.

Given the increasing demands on circuit designers to more quickly create chips of increasing density, decreasing wire and transistor widths, and decreasing power supply and power consumption, it is difficult to ensure optimal cell sizing in an automated place-and-route flow. Increasing the complexity, flexibility and/or functionality of the circuitry on a chip exacerbates these challenges. Thus, what is needed is a tool with which integrated circuit designers can efficiently (i) route signals such that corresponding characteristics can be determined and/or estimated and (ii) size cells to better optimize power consumption, thereby facilitating timing closure in an automated place-and-route flow.

## SUMMARY OF THE INVENTION

Embodiments of the present invention relate to methods, algorithms, software, architectures and/or systems for placing and sizing circuit blocks to optimize power consumption and improve timing closure in a circuit design.

In one embodiment, a method of placing and routing can include the steps of: (i) routing signal paths in one or more upper layers for connecting circuit blocks; (ii) adjusting the circuit blocks based on RC characteristics of the signal paths; and (iii) routing in one or more lower layers connections between the circuit blocks and the upper layers. The circuit blocks can include standard cells configured to implement a logic or timing function, other components, and/or integrated circuits, for example. The upper layers can include the three uppermost metal connectivity layers (e.g., metal-4, metal-5, metal-6), while the lower layers can include metal-1, metal-2, and metal-3, for example.

In another embodiment, a method of placing and connecting can include the steps of: (i) defining an array of layout partitions including a first subset of circuit blocks and a second subset of circuit blocks; (ii) routing a plurality of signal paths (preferably using one or more upper metal layers) between a first connection point substantially within a predetermined spacing from a corresponding one of said first subset of circuit blocks, and one or more second connection points, each substantially within said predetermined spacing from one or more of said second subset of circuit blocks; (iii) adjusting the circuit blocks based on characteristics (e.g., resistance, capacitance and/or inductance) of the signal path; and (iv) routing each signal path from the first connection point to the corresponding first circuit block and from the second connection point to the corresponding second circuit block(s) (preferably using lower metal layers). The first and second connection points can each include a via for connecting between the upper and lower layers.

In another embodiment, a connection of circuit blocks in an array of layout partitions can include circuit blocks electri-

cally connected by signal paths. The signal paths can have upper layer portions coupled by first connection points to first lower layer portions, which connect to one or more of a first subset of the circuit blocks. The upper layer portions can also have second connection points to second lower layer portions, which connect to one or more of a second subset of the circuit blocks. The first and second connection points may not be farther than a layout partition spacing away from at least one of the circuit blocks. The layout partition spacing can be a diagonal of one of the layout partitions in an array of such partitions. The circuit blocks can be located in the layout partitions.

Embodiments of the present invention can advantageously reduce power consumption and improve timing closure in an automated place-and-route flow. Embodiments of the present invention are suitable for the automated placing of circuit blocks or cells and the routing of signal paths between circuit blocks within an integrated circuit (IC) and/or routing between ICs or components on a board, such as a printed circuit board (PCB).

These and other advantages of the present invention will become readily apparent from the detailed description of preferred embodiments below.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagram showing a conventional wire routing estimation approach.

FIG. 2 is a box diagram showing an exemplary cell row arrangement within a layout partition structure according to embodiments of the present invention.

FIG. 3A is a layout view diagram showing an exemplary coarse circuit block or cell placement within a layout partition array according to embodiments of the present invention.

FIG. 3B is a layout view diagram showing an exemplary upper layer routing for the coarse cell placement of FIG. 3A according to embodiments of the present invention.

FIG. 3C is a layout view diagram showing an exemplary lower layer connection structure for the upper layer routing of FIG. 3B and the coarse cell placement of FIG. 3A according to embodiments of the present invention.

FIG. 4 is an exemplary flow diagram according to an embodiment of the present invention.

FIG. 5 is a box diagram showing a synthesis flow adapted for use with embodiments of the present invention.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be readily apparent to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail so as not to unnecessarily obscure aspects of the present invention.

Some portions of the detailed descriptions which follow are presented in terms of processes, procedures, logic blocks, functional blocks, processing, and other symbolic representations of operations on code, data bits, data streams or waveforms within a computer, processor, controller and/or memory. These descriptions and representations are generally used by those skilled in the data processing arts to effectively convey the substance of their work to others skilled in the art. A process, procedure, logic block, function, process, etc., is herein, and is generally, considered to be a self-consistent sequence of steps or instructions leading to a desired and/or expected result. The steps generally include physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical, magnetic, optical, or quantum signals capable of being stored, transferred, combined, compared, and otherwise manipulated in a computer or data processing system. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, waves, waveforms, streams, values, elements, symbols, characters, terms, numbers, or the like, and to their representations in computer programs or software as code (which may be object code, source code or binary code).

It should be borne in mind, however, that all of these and similar terms are associated with the appropriate physical quantities and/or signals, and are merely convenient labels applied to these quantities and/or signals. Unless specifically stated otherwise and/or as is apparent from the following discussions, it is appreciated that throughout the present application, discussions utilizing terms such as “processing,” “operating,” “computing,” “calculating,” “determining,” “manipulating,” “transforming,” “displaying” or the like, refer to the action and processes of a computer or data processing system, or similar processing device (e.g., an electrical, optical, or quantum computing or processing device), that manipulates and transforms data represented as physical (e.g., electronic) quantities. The terms refer to actions and processes of the processing devices that manipulate or transform physical quantities within the component(s) of a system or architecture (e.g., registers, memories, other such information storage, transmission or display devices, etc.) into other data similarly represented as physical quantities within other components of the same or a different system or architecture.

Furthermore, in the context of this application, the terms “net list” (or “netlist”) and “hardware description” may be used interchangeably to refer to a circuit design represented in an appropriate language, such as VERILOG simulation language, Hardware Description Language (HDL) or VERILOG HDL (VHDL; VERILOG is a registered trademark of Gateway Design Automation Corporation for computer aided electrical engineering programs). Similarly, the terms “wire,” “wiring,” “line,” “signal,” “conductor” and “bus” refer to any known structure, construction, arrangement, technique, method and/or process for physically transferring a signal from one point in a circuit to another. Also, unless indicated otherwise from the context of its use herein, the terms “known,” “fixed,” “given,” “certain” and “predetermined” generally refer to a value, quantity, parameter, constraint, condition, state, process, procedure, method, practice, or combination thereof that is, in theory, variable, but is typically set in advance and not varied thereafter when in use.

Similarly, for convenience and simplicity, the terms “clock,” “time,” “timing,” “rate,” “period” and “frequency” are, in general, interchangeable and may be used interchangeably herein, but are generally given their art-recognized meanings. Also, for convenience and simplicity, the terms “data,” “data stream,” “waveform” and “information” may be

## US 7,992,122 B1

5

used interchangeably, as may (a) the terms “flip-flop,” “latch” and “register,” and (b) the terms “connected to,” “coupled with,” “coupled to,” and “in communication with,” but these terms are generally given their art-recognized meanings herein.

The present invention concerns a method and/or algorithm (e.g., a computer-readable set of instructions) for routing signal paths or connections between circuit blocks, and can include: (i) routing signal paths in one or more upper layers for connecting circuit blocks; (ii) adjusting the circuit blocks based on RC characteristics of the signal paths; and (iii) routing in one or more lower layers connections between the circuit blocks and the upper layers. The circuit blocks can include standard cells configured to implement a logic or timing function, other components, and/or integrated circuits, for example. The upper layers can include the three uppermost metal connectivity layers in a semiconductor fabrication process (e.g., metal-4, metal-5, and metal-6 in a 6-metal layer process), while the lower layers can include metal-1, metal-2, and metal-3, for example.

In a further aspect of the invention, software relates to a medium or waveform containing a computer-readable set of instructions, where the instructions can be adapted to perform a method including: (i) routing signal paths in one or more upper layers for connecting circuit blocks; (ii) adjusting the circuit blocks based on RC characteristics of the signal paths; and (iii) routing in one or more lower layers connections between the circuit blocks and the upper layers.

In another aspect of the invention, a method and/or algorithm of placing and connecting can include the steps of: (i) defining a plurality of layout partitions (e.g., in an array), including first locations for a first subset of circuit blocks and second locations for a second subset of circuit blocks; (ii) routing a plurality of signal paths using one or more first type layers (e.g., upper metal layers) between (A) first connection points within a predetermined spacing from a corresponding first circuit block and (B) second connection points within the predetermined spacing from one or more corresponding second circuit blocks; (iii) adjusting the circuit blocks based on characteristics of the signal path; and (iv) routing the signal paths using one or more first type layers (e.g., lower metal layers) from the first connection points to the corresponding first circuit blocks and from the second connection points to the corresponding second circuit blocks. The first and second connection points can each include a via for connecting between the first and second layer types (e.g., upper and lower metal layers).

In another aspect of the invention, a connection of circuit blocks can include a plurality of circuit blocks coupled together by signal paths having certain characteristics. The signal paths can have upper layer portions coupled by first connection points to first lower layer portions, which connect to one or more of a first subset of the circuit blocks. The upper layer portions can also have second connection points to second lower layer portions, which connect to one or more of a second subset of the circuit blocks. The first and second connection points may not be farther than a layout partition spacing away from at least one of the circuit blocks. The layout partition spacing can be a diagonal of one of the layout partitions in an array of such partitions. The circuit blocks are generally located in the layout partitions.

Embodiments of the present invention can advantageously reduce power consumption and improve timing closure in an automated place-and-route flow. In one implementation, a power consumption reduction of approximately 30% was realized. Embodiments of the present invention are suitable for the automated placing of circuit blocks or cells and routing

6

of signal paths between circuit blocks within an integrated circuit (IC) and/or routing between ICs or components on a board, such as a printed circuit board (PCB).

The invention further relates to hardware and/or software implementations of the present architecture, method and system. The invention, in its various aspects, will be explained in greater detail below with regard to exemplary embodiments.

Referring now to FIG. 2, a box diagram showing an exemplary cell row arrangement within a layout partition structure according to embodiments of the present invention is indicated by the general reference character **200**. The layout partition structure can be a square region of any size, for example. In one embodiment, the layout partition structure size can be user programmable based on particular design requirements. Further, Layout Partition **202** can be arranged to include 16 rows of circuit blocks or cells (e.g., Cell Row **0**, Cell Row **1**, . . . Cell Row **15**). Alternatively, any number of rows of cells can be chosen, such as 2<sup>n</sup> rows, where n=1, 2, 3, etc. Each cell row can include power strips in one or two of the highest metal layers, for example. Such power strips may be connected or “strapped” by power lines running vertically where the rows are oriented horizontally, for example.

Referring now to FIG. 3A, a layout view diagram showing an exemplary coarse circuit block or cell placement within a layout partition array according to embodiments of the present invention is indicated by the general reference character **300**. The layout partition array can be divided into layout partitions as shown [e.g., H(0,0), H(0,1), H(0,2), . . . , H(4,3), H(4,4)] where each layout partition can be Layout Partition **202** of FIG. 2, for example. The array of layout partitions as in FIG. 3A can be any arrangement of layout partitions, such as organized as an “X” by “Y” array (e.g., X and Y can independently be 5, 10, 12, 16, or more). The size and shape of the overall array and/or of the layout partitions within the array may be driven by design considerations, such as the number of gates (where a “gate” may be a subset of or unit within a circuit block) in the design block as well as the process technology. For example, the layout partitions within the array may be sized such that each partition contains from about 20, 30 or 50 gates to about 250, 500 or 1000 gates, depending on the scale of the manufacturing technology. In one implementation, approximately 100 gates per layout partition in a 0.13 micron technology process provided good results.

In FIG. 3A, a “coarse” grid placement of circuit blocks or cells in layout partitions can include cell **302** in layout partition H(3,1), cell **304** in layout partition H(2,2), cell **306** in layout partition H(1,2), cell **308** in layout partition H(0,3), cell **310** in layout partition H(0,1), cells **312** and **316** in layout partition H(3,3), and cell **314** in layout partition H(2,4). In this stage of coarse circuit block placement, all placement and/or design rules need not be followed. For example, as shown in FIG. 3A, cells **312** and **316** may actually overlap at this point. Further, the cells may be placed outside the cell row structure as shown in FIG. 2, and rather, be placed in locations optimizing timing and/or overall wire length considerations.

In one embodiment, the layout partitions can be created after the coarse circuit block or cell placement is done. The coarse placement of cells can essentially be transformed into a layout partition structure. Alternatively, the layout partitions may be defined in advance. Further, the size of the layout partitions can be user-controlled. Also, high-fanout nets and/or signal paths can be buffered because it is known that such signals may need extra buffering regardless of the final load contribution due to wire routing. As is known to those skilled



US 7,992,122 B1

7

in the art, a multiple load and/or connection signal path may be considered a “high-fanout” signal path for automated routing purposes.

Referring now to FIG. 3B, a layout view diagram showing an exemplary upper layer routing for the coarse cell placement of FIG. 3A according to embodiments of the present invention is indicated by the general reference character **300**. At this stage, cells may be treated as being located anywhere within a particular layout partition for upper layer routing purposes. As such, the upper layer routing may extend to within or about a boundary of a particular layout partition for ultimate connection (e.g., using lower layers) to any cell within that layout partition.

Typically, signal path routing is done using metal connectivity layers whereby a particular process technology may provide, for example, five or more metal layers. The lowest layer (i.e., the one closest to the substrate) is typically referred to as “metal-1” or “M1” and each subsequent metal layer is referred to as “metal-2,” “metal-3,” etc. Each such metal layer may be separated by a dielectric isolation layer. Alternatively or additionally, one or more of the metal layers may take the form of “damascene” or “dual damascene” metal layers deposited into trenches and/or vias in a dielectric isolation layer, as is commonly used in copper metallization. According to embodiments of the present invention, a designated set of metal layers can be classified as “upper” layers, such as the three highest metal layers (e.g., metal-4, metal-5 and metal-6 in a 6-layer metal process, or metal-6, metal-7 and metal-8 in an 8-layer metal process) in the particular process technology.

In FIG. 3B, upper layer metal routes **330** and **332** can pass through horizontally to provide connections to other circuit blocks (not shown). Similarly, metal routes **342** and **344** can pass through vertically to provide connections to other circuit blocks (not shown). Such horizontal and vertical tracks can be on different metal layers (e.g., the horizontal tracks on metal-4 and the vertical tracks on metal-5). For portions of signal paths that route fully through a layout partition, characteristics of that signal path may be determined using conventional techniques on a segment basis whereby a “segment” is the portion that spans the layout partition. Additional portions of signal paths that do not span a full layout partition may be characterized using conventional means as “remainders.” The characteristics [e.g., resistance and capacitance (RC)] for a signal path can then be summed accordingly between all segments and remainders on the signal path. Alternatively, conventional approaches for determining such characteristics for a full signal path without regard to layout partition driven segmentation may also be employed.

In addition to strictly resistance and/or capacitance characteristics, any characteristics of a routed wire may be used in accordance with embodiments of the present invention. For example, time constants (the time required for a natural response on a signal to change by a certain amount), such as RC product time constants, may also be used. As another example, inductance characteristics of a wire may also be considered in some applications.

Where a connection to a circuit block is to be made (through lower connectivity layers), a via can be included to provide a path from the lowest “upper” layer to the highest “lower” layer. For example, if metal-4 is the lowest upper layer and metal route **334** (e.g., as other horizontal tracks) is part of a signal path that ultimately will connect to one of the cells (e.g., cell **302**) shown, a via (**334-V**) can be included within one square or layout partition spacing away from cell **302**. Such a layout partition spacing may be a diagonal of a square-shaped layout partition, a horizontal or vertical dimension of a square- or rectangular-shaped layout partition

8

(typically the same dimension as the direction of the signal path terminating at the connection point), or some other predetermined distance, for example. As will be discussed in more detail below with reference to FIG. 3C, a connection between via **334-V** and circuit block or cell **302** can then be made on one or more lower layers. Further, such a connection using lower layers may be strictly a “landing pad” or other such structure, as opposed to a horizontal and/or vertical routing connection to a circuit block.

Metal route **346** can similarly include via **346-V** in proximity to cells **306**, **308**, and **310**. Metal route **348** can include via **348-V** in proximity to cells **308** and **314**. For the vertical tracks that may be routed in metal-5, for example, a path down to metal-4 (one via) can be connected to another path down to metal-3 (another via) so that the lower layer routing can continue from that point. Metal route **336** can include via **336-V** in proximity to cells **304**, **302**, **312**, and **316**. Metal route **338** can include via **338-V** in proximity to cells **312** and **316**. Metal route **340** can include via **340-V** also in proximity to cells **312** and **316**.

At this stage, when the upper layer (e.g., long wire) routing is complete, such routing is finalized. Accordingly, an extraction of resistance and capacitance (RC) characteristics of a routed signal path even at this stage is very accurate. Further, an estimate of the RC characteristics for the remaining routing to be done using lower layers can be included. In one implementation, the capacitance contribution of such lower layer routing amounted to less than 2% of the upper layer capacitance contribution. Accordingly, cell sizing based on the actual upper layer capacitance contribution plus an estimate of the lower layer capacitance contribution for a signal path is highly accurate. As discussed above, techniques for determining and/or estimating the characteristics of a signal path may include “segmented” plus “remainder” or full wire route considerations, each employing conventional extraction techniques.

In addition to the circuit block/cell sizing based on the capacitive load determination, the cell placements can be “legalized” or made to conform to placement and/or design rules. For such legalization, cells may remain in the same layout partition unless there is no available space in that layout partition. Cells on a layout partition boundary may be “snapped” to one layout partition. Further, such cell placement adjustments can be done to minimize the length of unrouted (i.e., those that contain no upper layer portions) signal paths. Also at this stage, Clock Tree Synthesis (CTS) buffer insertion can be completed.

Referring now to FIG. 3C, a layout view diagram showing an exemplary lower layer connection structure between the upper layer routing of FIG. 3B and the coarse cell placement of FIG. 3A according to embodiments of the present invention is indicated by the general reference character **300**. Connection **360** can be routed on one or more lower layers (e.g., metal-1, metal-2, and/or metal-3) between via **346-V** and cell **310**. While the lower layer connections are shown in FIG. 3C merely as dashed lines for illustrative purposes, one skilled in the art will recognize that the actual routing of such connections is typically made by horizontal and/or vertical metal layer routing paths. Also from via **346-V** can be connection **362** to cell **306** and connection **364** to cell **308**. As one skilled in the art will recognize, all such lower layer connections described herein can be made with any combination of such designated lower layers (e.g., metal-1 only, metal-1 and metal-2, or any two or all three lower layer metal layers) as needed or chosen for the particular signal routing path. Further, the layers designated as “lower” layers and “upper” layers for a particular design and/or process technology may

US 7,992,122 B1

9

vary. For example, in an eight metal layer technology, metal-1 through metal-4 may be designated as lower layers and metal-5 through metal-8 may be designated as upper layers.

Continuing with the lower layer connections of FIG. 3C, connection 366 can be made between cell 304 and cell 306 and connection 368 can be made between via 348-V and cell 314. From via 336-V, connection 370 can be made to cell 304 and connection 378 can be made to cell 302. From via 338-V, connection 372 can be made to cell 312 and connection 374 can be made to cell 316. Also from cell 316, connection 376 can be made to via 340-V. Finally, connection 380 can be made between via 334-V and cell 302. As also shown in FIG. 3C and as discussed above, the placement of cell 316 can be “legalized” from its original coarse placement position (see dashed box overlapping cell 312). Such a legalization adjustment is indicated by the arrow labeled “L” for the change in position of cell 316 to a current position that does not violate placement or design rules. Of course, such a placement adjustment is done prior to the lower layer routing.

In this fashion, the routing of signal paths between circuit blocks can be completed. Such routing may be formed substantially in lower layer metals if the circuit blocks or cells are within a layout partition spacing (e.g., a diagonal of a layout partition, as discussed above) apart. On the other hand, if the circuit blocks to be connected are more than a layout partition spacing apart, higher layer routing can be done for longer parts of the signal path routing and then lower layer routing can be used to complete the connections. Accordingly, connections of varying distances can be accommodated according to embodiments of the present invention whereby upper layer routing is finalized prior to lower layer routing.

As another aspect of embodiments of the present invention, a user can click on a layout partition and, using conventional software implementation techniques, obtain statistics related to that partition. For example, a percentage of utilization (i.e., circuit block placement area versus available area in the layout partition) for the layout partition can be displayed. Further, connections terminating in that layout partition can be highlighted. Such statistics and displays can facilitate a user option to manually override automatic placing or routing decisions and/or to better identify the appropriate layout partition size for optimized utilization. Also, an error condition (e.g., a flag indicating that the upper and/or lower layer routing cannot complete or that too many cells have been placed in one layout partition) may show that a chosen layout partition size is too small for the particular place and route application.

Referring now to FIG. 4, an exemplary flow diagram according to an embodiment of the present invention is indicated by the general reference character 400. The flow can begin in Start 402 and cells can be coarsely placed (404). The coarse placement of a cell can be within one of the layout partitions, for example. As discussed above, such layout partitioning can be defined after the coarse cell placement. Global routing using upper metal layers can be done (406) and such routing can be substantially “finalized” so that the routing will not change even if the circuit blocks requiring connection to a particular upper layer track do change. That is, the circuit block locations may change from an initial coarse block placement and/or the circuit block sizing may change, but the associated upper layer routing may not change.

Characteristics (e.g., actual RC values) for the metal routing on the upper layers can be extracted (408). Such extraction can be done, as discussed above, through conventional methods as applied to a full signal path route or through segments and remainders of a wire path, for example. Cells (i.e., circuit blocks) can be sized and the cell placements can

10

be “legalized” (410) so that placement and/or design rules are not violated. Thus, in various embodiments and/or implementations, the first circuit blocks (or first subset of the plurality of circuit blocks) have a size and/or drive strength matched to resistance, capacitance and/or inductance characteristics of a signal path coupled to the circuit block. Next, the lower level routing can be done (412) and the flow can complete in End 414.

In general, embodiments of the present invention can be used in the placing of circuit blocks and the routing of signal paths between the circuit blocks or other routing termination points so that power consumption is minimized and timing closure is improved. However, while such power savings and timing closure improvements are more readily seen in digital full-swing type signals, embodiments of the present invention can also be used for “small signal” and/or reference or relatively stable level signals. Further, any type of signal suitable for automated routing (e.g., analog, digital, etc.) can be accommodated according to embodiments of the present invention.

Referring now to FIG. 5, a box diagram showing a synthesis flow adapted for use with embodiments of the present invention is indicated by the general reference character 500. Box 516 shows elements adapted for use in accordance with embodiments of the present invention. The remaining boxes in FIG. 5 represent a conventional synthesis flow. Inputs to Synthesis 508 typically include Constraints and Parameters 502, Design Description (HDL) 504, and Technology Library 506. Constraints and Parameters 502 may include physical expectations of the design, such as the circuit operating speed and/or the circuit layout area. Design Description (HDL) 504 can be a VERILOG HDL (VHDL) description of the logic operation(s) for synthesis. Technology Library 506 may contain a functional description as well as other information, such as may be related to the area and speed of all standard cells in a given process technology. For example, Technology Library 506 may be specific to a technology generation (e.g., 0.13 micron technology), a company (e.g., TSMC), and a process type (e.g., CMOS; eight-level metal; fast/normal/slow lot variation).

Outputs from Synthesis 508 may include Schematics 510, Netlist 512, and Reports 514. Schematics 510 can be schematic representations of the synthesized functions of Design Description (HDL) 504. Netlist 512 can be a text file description of a physical connection of components, such as standard cells, and can include a description of the various circuit blocks in the design and signal paths between the circuit blocks. Reports 514 can include speed and area data associated with results of Synthesis 508.

A netlist representation (e.g., Netlist 512) may be used for signal path determination, coarse cell placement and upper layer routing. Accordingly, Coarse Placement 518 can receive Netlist 512 and provide input to Route Upper Layers 520. For example, information about the location of cells in a design can be included in the input to Route Upper Layers 520. Extract RC for Upper Layers 522 can provide accurate RC information for the global/final upper layer signal path routes and feed the extracted RC information into Size Cells 524. Finally, the lower (remaining) layers can be routed in Route Lower Layers 526.

In this fashion, a conventional ASIC type design flow including synthesis can be adapted for placement of cells and routing of signal paths between the cells in accordance with embodiments of the present invention.

Further examples of suitable systems, tools and/or methods in which the present invention is generally applicable include those described in, e.g., U.S. Pat. Nos. 6,080,201 and 5,798,



## US 7,992,122 B1

11

936, the relevant portions of which are each incorporated herein by reference, and those commercially available from place-and-route software vendors such as Cadence Design Systems (e.g., the SILICON ENSEMBLE™, SILICON ENSEMBLE-PKS™, FIRST ENCOUNTER™, and NANO ENCOUNTER™ tools), Silicon Valley Research, Inc. (e.g., the QIC/APR™, GARDS™, SC™ and FLOORPLACER™ tools), Synopsys (e.g., the CHIP ARCHITECT™, DESIGN COMPILER™, and FLOORPLAN COMPILER™ tools) and Mentor Graphics (e.g., the AUTOCELLS™ tool).

Thus, embodiments of the present invention can advantageously reduce power consumption and improve timing closure in an automated place-and-route flow. Embodiments of the present invention are suitable for the automated placing of circuit blocks or cells and routing of signal paths between circuit blocks within an integrated circuit (IC) and/or routing between ICs or components on a board, such as a printed circuit board (PCB).

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents.

What is claimed is:

1. A method of placing and routing, comprising:

a) dividing a layout area of an integrated circuit (IC) into an array, said array comprising a plurality of user-defined layout partitions, and said IC comprising at least six metallization layers;

b) using a computer or data processing system, routing portions of a plurality of signal paths in one or more upper metallization layers to within a layout partition spacing of at least one of a plurality of circuit blocks in one of said layout partitions, said plurality of signal paths coupling to said plurality of circuit blocks in said layout partitions, and substantially finalizing said upper metallization layer signal path portions, wherein when the IC comprises at least eight metallization layers, the upper metallization layers consist of the four uppermost metallization layers, and when the IC comprises less than eight metallization layers, the upper metallization layers consist of the three uppermost metallization layers;

c) extracting actual characteristics of said one or more upper metallization layer signal path portions and determining estimated characteristics for portions of said plurality of signal paths in one or more lower metallization layers, said lower metallization layers consisting of those metallization layers of the IC other than the upper metallization layers, wherein said characteristics comprise one or more members of the group consisting of: resistance, inductance, and capacitance;

d) after finalizing said upper metallization layer signal path portions, adjusting said plurality of circuit blocks in response to said actual characteristics of said upper metallization layer signal path portions and said estimated characteristics of said lower metallization layer signal path portions; and

12

e) routing said lower metallization layer signal path portions between said plurality of circuit blocks and said one or more upper metallization layers.

2. The method of claim 1, wherein the step of routing in said one or more lower metallization layers includes routing segments not substantially longer than a diagonal of one of said plurality of layout partitions.

3. The method of claim 1, wherein said characteristics include resistance and capacitance.

4. The method of claim 1, wherein the step of adjusting said plurality of circuit blocks includes changing a location of at least one of said plurality of circuit blocks when there is a placement or design rule violation.

5. The method of claim 1, wherein the step of adjusting said plurality of circuit blocks includes changing a size of at least one of said plurality of circuit blocks.

6. A non-transitory computer-readable medium comprising a computer-executable set of instructions adapted to perform the method of claim 1.

7. The computer-readable medium of claim 6, further including an instruction adapted to provide a division of a layout area into an array of a plurality of layout partitions.

8. The computer-readable medium of claim 7, wherein routing in said one or more upper metallization layers includes an instruction adapted to route to within one of said plurality of layout partitions of at least one of said plurality of circuit blocks.

9. The computer-readable medium of claim 6, wherein said characteristics include resistance, inductance, and/or capacitance.

10. The computer-readable medium of claim 9, wherein said characteristics include resistance and capacitance.

11. The computer-readable medium of claim 6, wherein adjusting said plurality of circuit blocks includes an instruction adapted to change a location of at least one of said plurality of circuit blocks if there is a placement or design rule violation.

12. The computer-readable medium of claim 6, wherein adjusting said plurality of circuit blocks includes an instruction adapted to change a size of at least one of said plurality of circuit blocks.

13. The computer-readable medium of claim 6, wherein said one or more upper metallization layers consist of the three highest metal layers.

14. The computer-readable medium of claim 6, wherein said layout partition spacing is not greater than a diagonal length of one of said layout partitions in said array.

15. The computer-readable medium of claim 14, wherein said layout partition spacing is not greater than a horizontal or vertical length of said one of said layout partitions in said array.

16. The computer-readable medium of claim 15, wherein said layout partition spacing is not greater than a horizontal or vertical length of said one of said layout partitions in said array.

17. The computer-readable medium of claim 15, wherein said circuit blocks are located in the layout partitions.

18. The method of claim 1, wherein said one or more upper metallization layers consist of the three highest metal layers.

19. The method of claim 1, wherein said layout partition spacing is not greater than a diagonal length of one of said layout partitions in said array.

20. The method of claim 19, wherein said layout partition spacing is not greater than a horizontal or vertical length of said one of said layout partitions in said array.

21. The method of claim 19, wherein said circuit blocks are located in the layout partitions.

US 7,992,122 B1

13

22. The computer-readable medium of claim 21, wherein said circuit blocks are located in the layout partitions.

23. The method of claim 1, wherein said IC comprises 6 or 8 metallization layers.

24. A method of placing and connecting, comprising:

1) defining a plurality of user-defined layout partitions of an integrated circuit (IC), wherein a plurality of first locations of a first subset of circuit blocks and a plurality of second locations of a second subset of circuit blocks are within said plurality of user-defined layout partitions, and said IC includes at least six metallization layers;

2) using a computer or data processing system, routing portions of a plurality of signal paths using upper metallization layers between (i) a first plurality of connection points, each of said first plurality of connection points being substantially within a layout partition spacing from a corresponding one of said first subset of circuit blocks, and (ii) a second plurality of connection points, each of said second plurality of connection points being substantially within said layout partition spacing from one or more of said second subset of circuit blocks, wherein when the IC comprises at least eight metallization layers, the upper metallization layers consist of the four uppermost metallization layers, and when the IC comprises less than eight metallization layers, the upper metallization layers consist of the three uppermost metallization layers;

3) extracting actual characteristics of said one or more upper metallization layer signal path portions and determining estimated characteristics for portions of said plurality of signal paths in one or more lower metallization layers, said lower metallization layers consisting of

14

those metallization layers of the IC other than the upper metallization layers, wherein said characteristics include resistance, inductance, and/or capacitance;

4) finalizing said upper metallization layer signal path portions, and adjusting said locations of said first and second circuit blocks in response to said actual characteristics of said upper metallization layer signal path portions and said estimated characteristics said lower metallization layer signal path portions; and

5) routing said lower metallization layer signal path portions from each of said first connection points to each of said first subset of circuit blocks and from each of said second connection points to each of said second subset of circuit blocks.

25. The method of claim 24, wherein said predetermined spacing is a diagonal of one of said first and second layout partitions.

26. The method of claim 24, wherein the step of adjusting said first and second circuit blocks includes changing a size of at least one of said first and second circuit blocks.

27. The method of claim 24, wherein each of said first subset of circuit blocks is at least two layout partitions away from a corresponding one or more of said second subset of circuit blocks to which it is coupled by one or more of said signal paths.

28. The method of claim 24, wherein said one or more upper metallization layers consist of the three highest metal layers.

29. The method of claim 24, wherein said layout partition spacing is not greater than a diagonal length of one of said layout partitions in said array.

30. The method of claim 24, wherein said IC comprises 6 or 8 metallization layers.

\* \* \* \* \*