IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

MICROLINC, L.L.C.,

Plaintiff,

v.

INTEL CORPORATION,
ACER INC.,
ACER AMERICA CORPORATION,
ADVANCED MICRO DEVICES, INC.,
APPLE INC.,
DELL INC.,
GATEWAY INC.,
HEWLETT-PACKARD CO.,
LENOVO GROUP LTD.,
LENOVO (UNITED STATES),
INC.,SONY CORPORATION,
SONY CORPORATION OF AMERICA,
SONY ELECTRONICS, INC.,
SONY COMPUTER ENTERTAINMENT
AMERICA, INC.,
TOSHIBA CORP., and
TOSHIBA AMERICA INFORMATION
SYSTEMS INC.,

Defendants.

Civil Action No. 2:07-cv-00488-MHS

TRIAL BY JURY DEMANDED

FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff, MICROLINC, L.L.C., by its attorneys, hereby complains against Defendants INTEL CORPORATION, ACER INC., ACER AMERICA CORPORATION, ADVANCED MICRO DEVICES, INC., APPLE INC.,DELL INC., GATEWAY INC., HEWLETT-PACKARD CO., LENOVO GROUP LTD., LENOVO (UNITED STATES), INC.,SONY CORPORATION,SONY CORPORATION OF AMERICA, SONY ELECTRONICS, INC.,SONY COMPUTER ENTERTAINMENT

AMERICA,INC.,TOSHIBA CORP., and TOSHIBA AMERICA INFORMATION SYSTEMS INC., (collectively, Defendants), as follows:

I. THE PARTIES

1. Plaintiff MICROLINC, L.L.C. (MICROLINC), is a Delaware Limited Liability Company with a place of business in Plano, Texas.

2. Defendant INTEL CORPORATION (INTEL) is,on information and belief, a corporation established under the laws of the state of Delaware, with its principal place of business at 2200 Mission College Boulevard, Santa Clara, California, 95052.

3. Defendant ACER INC. is, on information and belief, a corporation organized and existing under the laws of Taiwan, with its principal place of business located at 8F, Sec. 1, Hsin Tai Wu Rd. Hsichih, Taipei Hsien 221, Taiwan, R.O.C. Defendant ACER AMERICA CORP. is, on information and belief, a corporation organized and existing under the laws of the State of California, with its principal place of business located at 333 West San Carlos Street, Suite 1500, San Jose, California 95110. ACER INC. and ACER AMERICA CORP. will be collectively referred to as ACER.

4. Defendant ADVANCED MICRO DEVICES, INC. (AMD) is,on information and belief, a corporation organized and existing under the laws of the state of Delaware, with its principal place of business located at One AMD Place, Sunnyvale, California, 94088.

5. Defendant APPLE INC. (APPLE) is, on information and belief, a corporation organized and existing under the laws of the State of California, with its principal place of business located at 1 Infinite Loop, Cupertino, California 95014.

6. Defendant DELL INC. (DELL) is, on information and belief, a corporation organized and existing under the laws of the State of Delaware, with its principal place of business located at One Dell Way, Round Rock, Texas 78682.

7. Defendant GATEWAY INC. (GATEWAY) is, on information and belief, a corporation organized and existing under the laws of the State of Delaware, with its principal place of business located at 7565 Irvine Center Drive, Irvine, California 92618.

8. Defendant HEWLETT-PACKARD CO. (HP) is, on information and belief, a corporation organized and existing under the laws of the State of Delaware, with its principal place of business located at 3000 Hanover Street, Palo Alto, California 94304.

9. Defendant LENOVO GROUP LTD .is, on information and belief, a foreign corporation organized and existing under the laws of Hong Kong. Defendant LENOVO (UNITED STATES) INC. is, on information and belief, a corporation organized and existing under the laws of the State of Delaware, with its principal place of business located at 1009 Think Place, Morrisville, North Carolina 27560. LENOVO GROUP LTD. and LENOVO (UNITED STATES) INC. will be collectively referred to as LENOVO.

10. Defendant SONY CORPORATION is, on information and belief, a foreign corporation organized and existing under the laws of Japan, with its principal place of business located at 1-7-1 Konan, Minato-ku, Tokyo 108-0075, Japan. Defendant SONY CORPORATION OF AMERICA is, on information and belief, a corporation organized and existing under the laws of the State of New York, with its principal place of business located at 550 Madison Avenue, New York, New York, 10022. Defendant SONY ELECTRONICS, INC. is, on information and belief, a corporation organized and

existing under the laws of the State of Delaware, with its principal place of business located at One Sony Drive, Park Ridge, New Jersey, 07656. Defendant SONY COMPUTER ENTERTAINMENT AMERICA, INC. is, on information and belief, a corporation organized and existing under the laws of the State of California, with its principal place of business located at 919 East Hillsdale Boulevard, 2nd Floor, Foster City, California 94404. SONY CORPORATION, SONY CORPORATION OF AMERICA, SONY ELECTRONICS, INC. and SONY COMPUTER ENTERTAINMENT AMERICA, INC. will be collectively referred to as SONY. In a letter agreement between MICROLINC and the SONY defendants, dated February 11, 2008, the SONY defendants have agreed that they will accept service though counsel of record for SONY COMPUTER ENTERTAINMENT AMERICA, INC.

11. Defendant TOSHIBA CORP. is,on information and belief, a foreign corporation organized and existing under the laws of Japan, with its principal place of business located at 1-1, Shibaura 1-chome, Minato-ku, Tokyo 105-8001, Japan. Defendant TOSHIBA AMERICA INFORMATION SYSTEMS, INC.is,on information and belief, a corporation organized and existing under the laws of the State of California, with its principal place of business located at 9740 Irvine Boulevard, Irvine, California 92618. TOSHIBA CORP. and TOSHIBA AMERICA INFORMATION SYSTEMS, INC. will be collectively referred to as TOSHIBA.

II. JURISDICTION AND VENUE

12. This Court has exclusive subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a) because this action arises under the patent laws of the United States, including 35 U.S.C. § 271 *et seq*. This Court has personal jurisdiction over Defendants because each has committed acts giving rise to this action within Texas and this judicial

district and has established minimum contacts within the forum such that the exercise of jurisdiction over Defendants would not offend traditional notions of fair play and substantial justice.

13. Venue properly lies in the Eastern District of Texas pursuant to 28 U.S.C. §§ 1391(b), 1391(c), and 1400(b), because each Defendant has committed acts within this judicial district giving rise to this action, and each Defendant resides in this District as it is subject to personal jurisdiction in this District. Venue is also appropriate because Defendants do business in this judicial district, including one or more of the infringing acts of offering for sale, selling, using infringing products, or providing service and support to Defendants' customers in this District and they do so through established distribution channels.

III. CLAIMS

14. MICROLINC realleges and incorporates by reference the allegations set forth in Paragraphs 1-13 above as if fully set forth herein.

15. On December 28, 1999,United States Patent Number 6,009,488 (the '488 patent), was duly and lawfully issued for an invention entitled "Computer Having Packet-Based Interconnect Channel" to Gautam Kavipurapu. At issuance, MICROLINC owned, by assignment, the '488 patent and continues to hold the right to sue and recover for past, present, and future infringement thereof. A true and correct copy of the '488 patent is attached hereto as **Exhibit A**.

16. The '488 patent discloses and claims pioneering inventions in the field of high performance packet-based interconnects between microprocessors and peripheral devices including; 1) mass storage devices, 2) input / output devices, and 3) random access memory devices.

17. During or before October 2003, representatives of INTEL became aware of the existence of multiple patents and patent applications on which Kavipurapu was the named inventor, including the '488 patent, and raised the possibility of acquiring the '488 patent with Kavipurapu.

18. In the summer of 2004, INTEL began marketing its new PCI Express architecture.

19. On November 10, 2005, MICROLINC filed a suit in the United States District Court for the Eastern District of Texas, Marshal Division, against INTEL and other defendants for infringement of the '488 patent (Civil Action No. 2-05-CV-514) ("the previous lawsuit").

20. Subsequently, INTEL introduced references which it argued would anticipate and/or render obvious some or all of the claims of the '488 patent.

21. To dispense with these new references, MICROLINC decided to have its '488 patent reexamined by the United States Patent and Trademark Office (USPTO) and filed its request (No. 90/008,106) on June 30, 2006 (MICROLINC Reexam).

22. MICROLINC dismissed INTEL and all other defendants from the previous lawsuit on February 20, 2006.

23. On August 28, 2006, INTEL filed its own first *ex parte* reexamination request (No. 90/008,196) (First INTEL Reexam). The MICROLINC Reexam and the First INTEL Reexam were subsequently merged and on October 29, 2007, the USPTO issued a non-final Office Action confirming the patentability of claims 10 and 13 of the '488 patent over all prior art of record.

24. On November 7, 2007, MICROLINC filed the present lawsuit.

25. On March 26, 2008, INTEL filed its second *ex parte* reexamination request (No. 90/009,098) for the '488 patent (Second INTEL Reexam).

26. On May 29, 2008, Defendants INTEL, ACER, DELL, APPLE, GATEWAY, HP, LENOVO, the SONY entities in the case at that time, and TOSHIBA sought to stay this case pending the reexamination of the '488 patent (see Dkt. 111).

27. As of May 2008, Defendants INTEL, ACER, DELL, APPLE, GATEWAY, HP, LENOVO, the SONY entities in the case at that time, and TOSHIBA have been aware of the '488 patent claims that would subsequently issue as new claims 14-28 (see Dkt. 111).

28. On September 16, 2008 the Court granted the Motion (Dkt. 111) and stayed this case.

29. On October 28, 2008, the USPTO issued a Notice of Intent to Issue Reexamination Certificate for the '488 patent, therein confirming the patentability of original claim 13 and new claims 14-28.

30. On December 23, 2008, INTEL filed its third ex parte reexamination request (No. 90/009,376) for the '488 patent (Third INTEL Reexam) which was granted on March 16, 2009.

31. On February 10, 2009, the USPTO issued the first Reexamination Certificate for the '488 patent, despite the pending Third INTEL Reexam.

32. On August 14, 2009, the Court lifted the stay of this case (see Dkt. 201).

33. On June 30, 2010, all Defendants, i.e., INTEL, ACER, AMD, DELL, APPLE, GATEWAY, HP, LENOVO, the SONY entities in the case at that time, and TOSHIBA sought to stay this case for the second time, because of the USPTO had issued a final rejection of all pending claims of the '488 patent (see Dkt. 314).

34. On September 20, 2010, the Court granted Defendant's Motion to Stay (see Dkt. 374).

35. On January 12, 2011, MICROLINC appealed the final rejection to the Board of Patent Appeals and Interferences (BPAI).

36. On June 6, 2012, the BPAI reversed the Examiner on certain rejections pertaining to independent claims 14, 27-29, 31, 34, and 35, and dependent claims 15-17, 20-26, 30, and 37-40 and found that claims 14-17 and 27-31 are patentable over the prior art of record.

37. On November 13, 2012, as a result of the BPAI decision, the USPTO issued the most recent Ex Parte Reexamination Certificate for the '488 patent.The Certificate sets forth that:(1) the patentability of claims 14-17 and 20-28 was confirmed, (2) new claims 29-39 were added and determined to be patentable, and (3) claims 1-13 and 18-19 were (previously) cancelled. A true and correct copy of the Certificate is attached hereto as **Exhibit B**.

38. Claims 14-17 and 20-28 have now survived the third reexamination of the '488 patent initiated by INTEL and are identical to claims14-17 and 20-28 first determined to be patentable on October 28, 2008 (see paragraph 28 above).

39. On November 16, 2012, Microlinc served on all Defendants a List of Accused Instrumentalities (together with its Infringement Contentions). A true and correct copy of this list is attached hereto as **Exhibit C**.

Defendant INTEL

40. INTEL is engaged in the business of manufacturing, assembling and selling integrated microprocessor chips, system-on-chips (SoC) and/or chipsets which are used by INTEL's customers in high-performance and value desktop and mobile PCs, and

entry-level to high-end servers and workstations, a substantial portion of which incorporate a packet-based data channel between a microprocessor and various peripherals.

41. INTEL contributed to the infringement of the '488 patent by manufacturing, assembling and selling integrated microprocessor chips, system-on-chips (SoC) and/or chipsets for use by its customers in high-performance and value desktop and mobile PCs, and entry-level to high-end servers and workstations with structures that are covered by and claimed in the '488 patent in violation of 35 U.S.C. §271.

42. INTEL actively induced and continues to induce the infringement of the '488 patent by distributing to its customers, hardware and system developers, certain reference literature for its products, such as, for example, datasheets and specifications, which encourage and teach the creation of computer systems that infringe the '488 patent.

43. With reference to **Exhibit C**, the INTEL products listed therein are adapted and specifically designed for use in physically non-distributed microprocessor-based computer systems that include at least one microprocessor, at least one random access memory device, at least one mass storage device, and at least one input-output port device.

44. With further reference to the INTEL products identified in **Exhibit C**, those products each include a microprocessor which either incorporates or is connected to at least one interface capable of receiving and transmitting data using packets.

45. With further reference to the INTEL products identified on **Exhibit C**, each of those products include at least one buffer, or memory location, for storing a copy of at least some of the packets that are transmitted by the microprocessor interface.

46. With further reference to the INTEL products identified in **Exhibit C**, each of those products include at least one interface that is incorporated or connected to a microprocessor that is linked to or associated with a cache for storing at least some of the requested data from either a random access memory device, a mass storage device, or an input-output port device.

47. With further reference to the INTEL products identified in **Exhibit C**, each of those products include at least one interface, incorporated or connected to a microprocessor, and such interface includes a controller capable of accepting data and a physical address from the microprocessor, whereby the physical address identifies a particular physical address of either a random access memory device, a mass storage device, or an input-output port device.

48. INTEL has sought to benefit from the reexaminations it initiated by, inter alia, using such reexaminations to seek a stay of this case.

49. INTEL was aware that on October 28, 2008, the USPTO determined claims 14-28 patentable.

50. By continuing infringement during the period after October 28, 2008 and before March 16, 2009 (the date the Third INTEL Reexam was granted), INTEL acted despite an objectively high likelihood that its actions constituted infringement of valid claims of the '488 patent.

51. Further to the immediately preceding paragraph, the objectively high likelihood of infringement was actually known to INTEL or was so obvious it should have been known.

52. In light of the outcome of the First and Second INTEL Reexams, INTEL knew or should have known that there was an objectively high risk that some or all claims at issue in the Third INTEL Reexam would eventually be confirmed.

53. INTEL has willfully infringed valid claims of the '488 patent.

54. INTEL's acts of infringement have caused damage to MICROLINC. Under 35 U.S.C. § 284, MICROLINC is entitled to recover from INTEL the damages sustained by MICROLINC as a result of its infringement of the '488 patent. INTEL's infringement on MICROLINC's exclusive rights under the '488 patent will continue to damage MICROLINC causing irreparable harm, for which there is no adequate remedy of law, unless enjoined by this Court under 35 U.S.C. § 283.

Defendant ACER

55. ACER is engaged in the business of manufacturing, assembling and selling microprocessor-based computer systems which incorporate a packet-based data channel between a microprocessor and various peripherals.

56. ACER has infringed and continues to infringe the '488 patent by its manufacture, use, sale, importation, and/or offer for sale of microprocessor-based computer systems that incorporate the invention disclosed and claimed in the '488 patent.

57. With reference to **Exhibit C**, the ACER products listed therein are physically non-distributed microprocessor-based computer systems that include at least one microprocessor, at least one random access memory device, at least one mass storage device, and at least one input-output port device.

58. With further reference to the ACER products identified in **Exhibit C**, each of those products include a microprocessor, a random access memory device, a mass storage device, and an input-output port device, whereby each of the random access

memory device, mass storage device, and input-output port device can be operated in conjunction with the microprocessor.

59. With further reference to the ACER products identified in **Exhibit C**, each of those products include a microprocessor, a random access memory device, a mass storage device, and an input-output port device, each of which either incorporates or is connected to at least one interface capable of receiving and transmitting data using packets.

60. With further reference to the ACER products identified in **Exhibit C**, each of those products include at least one data channel that extends between a microprocessor and the interface(s) of a random access memory device, a mass storage device, and an input-output port device for transporting data in packet form.

61. With further reference to the ACER products identified in **Exhibit C**, each of those products include at least one buffer, or memory location, for storing a copy of at least some of the packets that are transmitted by the microprocessor interface.

62. With further reference to the ACER products identified in **Exhibit C**, each of those products include at least one interface that is incorporated or connected to a microprocessor that is linked to or associated with a cache for storing at least some of the requested data from either a random access memory device, a mass storage device, or an input-output port device.

63. With further reference to the ACER products identified in **Exhibit C**, each of those products include at least one interface incorporated or connected to a microprocessor, which interface includes a controller capable of accepting data and a physical address from the microprocessor, whereby the physical address identifies a

particular physical address of either a random access memory device, a mass storage device, or an input-output port device.

64. ACER has sought to benefit from the reexaminations initiated by INTEL by, inter alia, using such reexaminations to seek a stay of this case.

65. ACER was aware that on October 28, 2008, the USPTO determined claims 14-28 patentable.

66. By continuing infringement during the period after October 28, 2008 and before March 16, 2009 (the date the Third INTEL Reexam was granted), ACER acted despite an objectively high likelihood that its actions constituted infringement of valid claims of the '488 patent.

67. Further to the immediately preceding paragraph, the objectively high likelihood of infringement was actually known to ACER or was so obvious it should have been known.

68. In light of the outcome of the First and Second INTEL Reexams, ACER knew or should have known that there was an objectively high risk that some or all claims at issue in the Third INTEL Reexam would eventually be confirmed.

69. ACER has willfully infringed valid claims of the '488 patent.

70. ACER's acts of infringement have caused damage to MICROLINC. Under 35 U.S.C. § 284, MICROLINC is entitled to recover from ACER the damages sustained by MICROLINC as a result of its infringement of the '488 patent. ACER's infringement on MICROLINC's exclusive rights under the '488 patent will continue to damage MICROLINC causing irreparable harm, for which there is no adequate remedy of law, unless enjoined by this Court under 35 U.S.C. § 283.

Defendant AMD

71. AMD is engaged in the business of manufacturing, assembling and selling integrated microprocessor chips and/or chipsets which are used by AMD's customers in high-performance and value desktop and mobile PCs, and entry-level to high-end servers and workstations, a substantial portion of which incorporate a packet-based data channel between a microprocessor and various peripherals.

72. AMD contributed to the infringement of the '488 patent by manufacturing, assembling and selling integrated microprocessor chips and/or chipsets for use by its customers in high-performance and value desktop and mobile PCs, and entry-level to high-end servers and workstations with structures that are covered by and claimed in the '488 patent in violation of 35 U.S.C. §271.

73. AMD actively induced and continues to induce the infringement of the '488 patent by distributing to its customers, hardware and system developers, certain reference literature for its products, such as, for example, datasheets, specifications and builder's guides, which encourage and teach the creation of computer systems that infringe the '488 patent.

74. With reference to **Exhibit C**, the AMD products listed therein are adapted and specifically designed for use in physically non-distributed microprocessor-based computer systems that include at least one microprocessor, at least one random access memory device, at least one mass storage device, and at least one input-output port device.

75. With further reference to the AMD products identified in **Exhibit C**, those products each include a microprocessor which either incorporates or is connected to at least one interface capable of receiving and transmitting data using packets.

76. With further reference to the AMD products identified on **Exhibit C**, each of those products include at least one buffer, or memory location, for storing a copy of at least some of the packets that are transmitted by the microprocessor interface.

77. With further reference to the AMD products identified in **Exhibit C**, each of those products include at least one interface that is incorporated or connected to a microprocessor that is linked to or associated with a cache for storing at least some of the requested data from either a random access memory device, a mass storage device, or an input-output port device.

78. With further reference to the AMD products identified in **Exhibit C**, each of those products include at least one interface, incorporated or connected to a microprocessor, and such interface includes a controller capable of accepting data and a physical address from the microprocessor, whereby the physical address identifies a particular physical address of either a random access memory device, a mass storage device, or an input-output port device.

79. AMD has sought to benefit from the reexaminations initiated by INTEL by, inter alia, using such reexaminations to seek a stay of this case.

80. AMD was aware that on October 28, 2008, the USPTO determined claims 14-28 patentable.

81. By continuing infringement during the period after October 28, 2008 and before March 16, 2009 (the date the Third INTEL Reexam was granted), AMD acted despite an objectively high likelihood that its actions constituted infringement of valid claims of the '488 patent.

82. Further to the immediately preceding paragraph, the objectively high likelihood of infringement was actually known to AMD or was so obvious it should have been known.

83. In light of the outcome of the First and Second INTEL Reexams, AMD knew or should have known that there was an objectively high risk that some or all claims at issue in the Third INTEL Reexam would eventually be confirmed.

84. AMD has willfully infringed valid claims of the '488 patent.

85. AMD's acts of infringement have caused damage to MICROLINC. Under 35 U.S.C. § 284, MICROLINC is entitled to recover from AMD the damages sustained by MICROLINC as a result of its infringement of the '488 patent. AMD's infringement on MICROLINC's exclusive rights under the '488 patent will continue to damage MICROLINC causing irreparable harm, for which there is no adequate remedy of law, unless enjoined by this Court under 35 U.S.C. § 283.

Defendant APPLE

86. APPLE is engaged in the business of manufacturing, assembling and selling microprocessor-based computer systems which incorporate a packet-based data channel between a microprocessor and various peripherals.

87. APPLE has infringed and continues to infringe the '488 patent by its manufacture, use, sale, importation, and/or offer for sale of microprocessor-based computer systems that incorporate the invention disclosed and claimed in the '488 patent.

88. With reference to **Exhibit C**, the APPLE products listed therein are physically non-distributed microprocessor-based computer systems that include at least one microprocessor, at least one random access memory device, at least one mass storage device, and at least one input-output port device.

89. With further reference to the APPLE products identified in **Exhibit C**, each of those products include a microprocessor, a random access memory device, a mass storage device, and an input-output port device, whereby each of the random access memory device, mass storage device, and input-output port device can be operated in conjunction with the microprocessor.

90. With further reference to the APPLE products identified in **Exhibit C**, each of those products include a microprocessor, a random access memory device, a mass storage device, and an input-output port device, each of which either incorporates or is connected to at least one interface capable of receiving and transmitting data using packets.

91. With further reference to the APPLE products identified in **Exhibit C**, each of those products include at least one data channel that extends between a microprocessor and the interface(s) of a random access memory device, a mass storage device, and an input-output port device for transporting data in packet form.

92. With further reference to the APPLE products identified in **Exhibit C**, each of those products include at least one buffer, or memory location, for storing a copy of at least some of the packets that are transmitted by the microprocessor interface.

93. With further reference to the APPLE products identified in **Exhibit C**, each of those products include at least one interface that is incorporated or connected to a microprocessor that is linked to or associated with a cache for storing at least some of the requested data from either a random access memory device, a mass storage device, or an input-output port device.

94. With further reference to the APPLE products identified in **Exhibit C**, each of those products include at least one interface incorporated or connected to a

microprocessor, which interface includes a controller capable of accepting data and a physical address from the microprocessor, whereby the physical address identifies a particular physical address of either a random access memory device, a mass storage device, or an input-output port device.

95. APPLE has sought to benefit from the reexaminations initiated by INTEL by, inter alia, using such reexaminations to seek a stay of this case.

96. APPLE was aware that on October 28, 2008, the USPTO determined claims 14-28 patentable.

97. By continuing infringement during the period after October 28, 2008 and before March 16, 2009 (the date the Third INTEL Reexam was granted), APPLE acted despite an objectively high likelihood that its actions constituted infringement of valid claims of the '488 patent.

98. Further to the immediately preceding paragraph, the objectively high likelihood of infringement was actually known to APPLE or was so obvious it should have been known.

99. In light of the outcome of the First and Second INTEL Reexams, APPLE knew or should have known that there was an objectively high risk that some or all claims at issue in the Third INTEL Reexam would eventually be confirmed.

100. APPLE has willfully infringed valid claims of the '488 patent.

101. APPLE's acts of infringement have caused damage to MICROLINC. Under 35 U.S.C. § 284, MICROLINC is entitled to recover from APPLE the damages sustained by MICROLINC as a result of its infringement of the '488 patent. APPLE's infringement on MICROLINC's exclusive rights under the '488 patent will continue to

damage MICROLINC causing irreparable harm, for which there is no adequate remedy of law, unless enjoined by this Court under 35 U.S.C. § 283.

Defendant DELL

102. DELL is engaged in the business of manufacturing, assembling and selling microprocessor-based computer systems which incorporate a packet-based data channel between a microprocessor and various peripherals.

103. DELL has infringed and continues to infringe the '488 patent by its manufacture, use, sale, importation, and/or offer for sale of microprocessor-based computer systems that incorporate the invention disclosed and claimed in the '488 patent.

104. With reference to **Exhibit C**, the DELL products listed therein are physically non-distributed microprocessor-based computer systems that include at least one microprocessor, at least one random access memory device, at least one mass storage device, and at least one input-output port device.

105. With further reference to the DELL products identified in **Exhibit C**, each of those products include a microprocessor, a random access memory device, a mass storage device, and an input-output port device, whereby each of the random access memory device, mass storage device, and input-output port device can be operated in conjunction with the microprocessor.

106. With further reference to the DELL products identified in **Exhibit C**, each of those products include a microprocessor, a random access memory device, a mass storage device, and an input-output port device, each of which either incorporates or is connected to at least one interface capable of receiving and transmitting data using packets.

107. With further reference to the DELL products identified in **Exhibit C**, each of those products include at least one data channel that extends between a microprocessor and the interface(s) of a random access memory device, a mass storage device, and an input-output port device for transporting data in packet form.

108. With further reference to the DELL products identified in **Exhibit C**, each of those products include at least one buffer, or memory location, for storing a copy of at least some of the packets that are transmitted by the microprocessor interface.

109. With further reference to the DELL products identified in **Exhibit C**, each of those products include at least one interface that is incorporated or connected to a microprocessor that is linked to or associated with a cache for storing at least some of the requested data from either a random access memory device, a mass storage device, or an input-output port device.

110. With further reference to the DELL products identified in **Exhibit C**, each of those products include at least one interface incorporated or connected to a microprocessor, which interface includes a controller capable of accepting data and a physical address from the microprocessor, whereby the physical address identifies a particular physical address of either a random access memory device, a mass storage device, or an input-output port device.

111. DELL has sought to benefit from the reexaminations initiated by INTEL by, inter alia, using such reexaminations to seek a stay of this case.

112. DELL was aware that on October 28, 2008, the USPTO determined claims 14-28 patentable.

113. By continuing infringement during the period after October 28, 2008 and before March 16, 2009 (the date the Third INTEL Reexam was granted), DELL acted

despite an objectively high likelihood that its actions constituted infringement of valid claims of the '488 patent.

114. Further to the immediately preceding paragraph, the objectively high likelihood of infringement was actually known to DELL or was so obvious it should have been known.

115. In light of the outcome of the First and Second INTEL Reexams, DELL knew or should have known that there was an objectively high risk that some or all claims at issue in the Third INTEL Reexam would eventually be confirmed.

116. DELL has willfully infringed valid claims of the '488 patent.

117. DELL's acts of infringement have caused damage to MICROLINC. Under 35 U.S.C. § 284, MICROLINC is entitled to recover from DELL the damages sustained by MICROLINC as a result of its infringement of the '488 patent. DELL's infringement on MICROLINC's exclusive rights under the '488 patent will continue to damage MICROLINC causing irreparable harm, for which there is no adequate remedy of law, unless enjoined by this Court under 35 U.S.C. § 283.

Defendant GATEWAY

118. GATEWAY is engaged in the business of manufacturing, assembling and selling microprocessor-based computer systems which incorporate a packet-based data channel between a microprocessor and various peripherals.

119. GATEWAY has infringed and continues to infringe the '488 patent by its manufacture, use, sale, importation, and/or offer for sale of microprocessor-based computer systems that incorporate the invention disclosed and claimed in the '488 patent.

120. With reference to **Exhibit C**, the GATEWAY products listed therein are physically non-distributed microprocessor-based computer systems that include at least

one microprocessor, at least one random access memory device, at least one mass storage device, and at least one input-output port device.

121. With further reference to the GATEWAY products identified in **Exhibit C**, each of those products include a microprocessor, a random access memory device, a mass storage device, and an input-output port device, whereby each of the random access memory device, mass storage device, and input-output port device can be operated in conjunction with the microprocessor.

122. With further reference to the GATEWAY products identified in **Exhibit C**, each of those products include a microprocessor, a random access memory device, a mass storage device, and an input-output port device, each of which either incorporates or is connected to at least one interface capable of receiving and transmitting data using packets.

123. With further reference to the GATEWAY products identified in **Exhibit C**, each of those products include at least one data channel that extends between a microprocessor and the interface(s) of a random access memory device, a mass storage device, and an input-output port device for transporting data in packet form.

124. With further reference to the GATEWAY products identified in **Exhibit C**, each of those products include at least one buffer, or memory location, for storing a copy of at least some of the packets that are transmitted by the microprocessor interface.

125. With further reference to the GATEWAY products identified in **Exhibit C**, each of those products include at least one interface that is incorporated or connected to a microprocessor that is linked to or associated with a cache for storing at least some of the requested data from either a random access memory device, a mass storage device, or an input-output port device.

126. With further reference to the GATEWAY products identified in **Exhibit C**, each of those products include at least one interface incorporated or connected to a microprocessor, which interface includes a controller capable of accepting data and a physical address from the microprocessor, whereby the physical address identifies a particular physical address of either a random access memory device, a mass storage device, or an input-output port device.

127. GATEWAY has sought to benefit from the reexaminations initiated by INTEL by, inter alia, using such reexaminations to seek a stay of this case.

128. GATEWAY was aware that on October 28, 2008, the USPTO determined claims 14-28 patentable.

129. By continuing infringement during the period after October 28, 2008 and before March 16, 2009 (the date the Third INTEL Reexam was granted), GATEWAY acted despite an objectively high likelihood that its actions constituted infringement of valid claims of the '488 patent.

130. Further to the immediately preceding paragraph, the objectively high likelihood of infringement was actually known to GATEWAY or was so obvious it should have been known.

131. In light of the outcome of the First and Second INTEL Reexams, GATEWAY knew or should have known that there was an objectively high risk that some or all claims at issue in the Third INTEL Reexam would eventually be confirmed.

132. GATEWAY has willfully infringed valid claims of the '488 patent.

133. GATEWAY's acts of infringement have caused damage to MICROLINC. Under 35 U.S.C. § 284, MICROLINC is entitled to recover from GATEWAY the damages sustained by MICROLINC as a result of its infringement of the '488 patent.

GATEWAY's infringement on MICROLINC's exclusive rights under the '488 patent will continue to damage MICROLINC causing irreparable harm, for which there is no adequate remedy of law, unless enjoined by this Court under 35 U.S.C. § 283.

Defendant HP

134. HP is engaged in the business of manufacturing, assembling and selling microprocessor-based computer systems which incorporate a packet-based data channel between a microprocessor and various peripherals.

135. HP has infringed and continues to infringe the '488 patent by its manufacture, use, sale, importation, and/or offer for sale of microprocessor-based computer systems that incorporate the invention disclosed and claimed in the '488 patent.

136. With reference to **Exhibit C**, the HP products listed therein are physically non-distributed microprocessor-based computer systems that include at least one microprocessor, at least one random access memory device, at least one mass storage device, and at least one input-output port device.

137. With further reference to the HP products identified in **Exhibit C**, each of those products include a microprocessor, a random access memory device, a mass storage device, and an input-output port device, whereby each of the random access memory device, mass storage device, and input-output port device can be operated in conjunction with the microprocessor.

138. With further reference to the HP products identified in **Exhibit C**, each of those products include a microprocessor, a random access memory device, a mass storage device, and an input-output port device, each of which either incorporates or is connected to at least one interface capable of receiving and transmitting data using packets.

139. With further reference to the HP products identified in **Exhibit C**, each of those products include at least one data channel that extends between a microprocessor and the interface(s) of a random access memory device, a mass storage device, and an input-output port device for transporting data in packet form.

140. With further reference to the HP products identified in **Exhibit C**, each of those products include at least one buffer, or memory location, for storing a copy of at least some of the packets that are transmitted by the microprocessor interface.

141. With further reference to the HP products identified in **Exhibit C**, each of those products include at least one interface that is incorporated or connected to a microprocessor that is linked to or associated with a cache for storing at least some of the requested data from either a random access memory device, a mass storage device, or an input-output port device.

142. With further reference to the HP products identified in **Exhibit C**, each of those products include at least one interface incorporated or connected to a microprocessor, which interface includes a controller capable of accepting data and a physical address from the microprocessor, whereby the physical address identifies a particular physical address of either a random access memory device, a mass storage device, or an input-output port device.

143. HP has sought to benefit from the reexaminations initiated by INTEL by, inter alia, using such reexaminations to seek a stay of this case.

144. HP was aware that on October 28, 2008, the USPTO determined claims 14-28 patentable.

145. By continuing infringement during the period after October 28, 2008 and before March 16, 2009 (the date the Third INTEL Reexam was granted), HP acted

despite an objectively high likelihood that its actions constituted infringement of valid claims of the '488 patent.

146. Further to the immediately preceding paragraph, the objectively high likelihood of infringement was actually known to HP or was so obvious it should have been known.

147. In light of the outcome of the First and Second INTEL Reexams, HP knew or should have known that there was an objectively high risk that some or all claims at issue in the Third INTEL Reexam would eventually be confirmed.

148. HP has willfully infringed valid claims of the '488 patent.

149. HP's acts of infringement have caused damage to MICROLINC. Under 35 U.S.C. § 284, MICROLINC is entitled to recover from HP the damages sustained by MICROLINC as a result of its infringement of the '488 patent. HP's infringement on MICROLINC's exclusive rights under the '488 patent will continue to damage MICROLINC causing irreparable harm, for which there is no adequate remedy of law, unless enjoined by this Court under 35 U.S.C. § 283.

Defendant LENOVO

150. LENOVO is engaged in the business of manufacturing, assembling and selling microprocessor-based computer systems which incorporate a packet-based data channel between a microprocessor and various peripherals.

151. LENOVO has infringed and continues to infringe the '488 patent by its manufacture, use, sale, importation, and/or offer for sale of microprocessor-based computer systems that incorporate the invention disclosed and claimed in the '488 patent.

152. With reference to **Exhibit C**, the LENOVO products listed therein are physically non-distributed microprocessor-based computer systems that include at least

one microprocessor, at least one random access memory device, at least one mass storage device, and at least one input-output port device.

153. With further reference to the LENOVO products identified in **Exhibit C**, each of those products include a microprocessor, a random access memory device, a mass storage device, and an input-output port device, whereby each of the random access memory device, mass storage device, and input-output port device can be operated in conjunction with the microprocessor.

154. With further reference to the LENOVO products identified in **Exhibit C**, each of those products include a microprocessor, a random access memory device, a mass storage device, and an input-output port device, each of which either incorporates or is connected to at least one interface capable of receiving and transmitting data using packets.

155. With further reference to the LENOVO products identified in **Exhibit C**, each of those products include at least one data channel that extends between a microprocessor and the interface(s) of a random access memory device, a mass storage device, and an input-output port device for transporting data in packet form.

156. With further reference to the LENOVO products identified in **Exhibit C**, each of those products include at least one buffer, or memory location, for storing a copy of at least some of the packets that are transmitted by the microprocessor interface.

157. With further reference to the LENOVO products identified in **Exhibit C**, each of those products include at least one interface that is incorporated or connected to a microprocessor that is linked to or associated with a cache for storing at least some of the requested data from either a random access memory device, a mass storage device, or an input-output port device.

158. With further reference to the LENOVO products identified in **Exhibit C**, each of those products include at least one interface incorporated or connected to a microprocessor, which interface includes a controller capable of accepting data and a physical address from the microprocessor, whereby the physical address identifies a particular physical address of either a random access memory device, a mass storage device, or an input-output port device.

159. LENOVO has sought to benefit from the reexaminations initiated by INTEL by, inter alia, using such reexaminations to seek a stay of this case.

160. LENOVO was aware that on October 28, 2008, the USPTO determined claims 14-28 patentable.

161. By continuing infringement during the period after October 28, 2008 and before March 16, 2009 (the date the Third INTEL Reexam was granted), LENOVO acted despite an objectively high likelihood that its actions constituted infringement of valid claims of the '488 patent.

162. Further to the immediately preceding paragraph, the objectively high likelihood of infringement was actually known to LENOVO or was so obvious it should have been known.

163. In light of the outcome of the First and Second INTEL Reexams, LENOVO knew or should have known that there was an objectively high risk that some or all claims at issue in the Third INTEL Reexam would eventually be confirmed.

164. LENOVO has willfully infringed valid claims of the '488 patent.

165. LENOVO's acts of infringement have caused damage to MICROLINC. Under 35 U.S.C. § 284, MICROLINC is entitled to recover from LENOVO the damages sustained by MICROLINC as a result of its infringement of the '488 patent. LENOVO's

infringement on MICROLINC's exclusive rights under the '488 patent will continue to damage MICROLINC causing irreparable harm, for which there is no adequate remedy of law, unless enjoined by this Court under 35 U.S.C. § 283.

Defendant SONY

166. SONY is engaged in the business of manufacturing, assembling and selling microprocessor-based computer systems which incorporate a packet-based data channel between a microprocessor and various peripherals.

167. SONY has infringed and continues to infringe the '488 patent by its manufacture, use, sale, importation, and/or offer for sale of microprocessor-based computer systems that incorporate the invention disclosed and claimed in the '488 patent.

168. With reference to **Exhibit C**, the SONY products listed therein are physically non-distributed microprocessor-based computer systems that include at least one microprocessor, at least one random access memory device, at least one mass storage device, and at least one input-output port device.

169. With further reference to the SONY products identified in **Exhibit C**, each of those products include a microprocessor, a random access memory device, a mass storage device, and an input-output port device, whereby each of the random access memory device, mass storage device, and input-output port device can be operated in conjunction with the microprocessor.

170. With further reference to the SONY products identified in **Exhibit C**, each of those products include a microprocessor, a random access memory device, a mass storage device, and an input-output port device, each of which either incorporates or is connected to at least one interface capable of receiving and transmitting data using packets.

171. With further reference to the SONY products identified in **Exhibit C**, each of those products include at least one data channel that extends between a microprocessor and the interface(s) of a random access memory device, a mass storage device, and an input-output port device for transporting data in packet form.

172. With further reference to the SONY products identified in **Exhibit C**, each of those products include at least one buffer, or memory location, for storing a copy of at least some of the packets that are transmitted by the microprocessor interface.

173. With further reference to the SONY products identified in **Exhibit C**, each of those products include at least one interface that is incorporated or connected to a microprocessor that is linked to or associated with a cache for storing at least some of the requested data from either a random access memory device, a mass storage device, or an input-output port device.

174. With further reference to the SONY products identified in **Exhibit C**, each of those products include at least one interface incorporated or connected to a microprocessor, which interface includes a controller capable of accepting data and a physical address from the microprocessor, whereby the physical address identifies a particular physical address of either a random access memory device, a mass storage device, or an input-output port device.

175. The SONY entities in the case at the time of the reexaminations initiated by Intel sought to benefit from such reexaminations by, inter alia, using such reexaminations to seek a stay of this case.

176. SONY was aware that on October 28, 2008, the USPTO determined claims 14-28 patentable.

177. By continuing infringement during the period after October 28, 2008 and before March 16, 2009 (the date the Third INTEL Reexam was granted), SONY acted despite an objectively high likelihood that its actions constituted infringement of valid claims of the '488 patent.

178. Further to the immediately preceding paragraph, the objectively high likelihood of infringement was actually known to SONY or was so obvious it should have been known.

179. In light of the outcome of the First and Second INTEL Reexams, SONY knew or should have known that there was an objectively high risk that some or all claims at issue in the Third INTEL Reexam would eventually be confirmed.

180. SONY has willfully infringed valid claims of the '488 patent.

181. SONY's acts of infringement have caused damage to MICROLINC. Under 35 U.S.C. § 284, MICROLINC is entitled to recover from SONY the damages sustained by MICROLINC as a result of its infringement of the '488 patent. SONY's infringement on MICROLINC's exclusive rights under the '488 patent will continue to damage MICROLINC causing irreparable harm, for which there is no adequate remedy of law, unless enjoined by this Court under 35 U.S.C. § 283.

Defendant TOSHIBA

182. TOSHIBA is engaged in the business of manufacturing, assembling and selling microprocessor-based computer systems which incorporate a packet-based data channel between a microprocessor and various peripherals.

183. TOSHIBA has infringed and continues to infringe the '488 patent by its manufacture, use, sale, importation, and/or offer for sale of microprocessor-based computer systems that incorporate the invention disclosed and claimed in the '488 patent.

184. With reference to **Exhibit C**, the TOSHIBA products listed therein are physically non-distributed microprocessor-based computer systems that include at least one microprocessor, at least one random access memory device, at least one mass storage device, and at least one input-output port device.

185. With further reference to the TOSHIBA products identified in **Exhibit C**, each of those products include a microprocessor, a random access memory device, a mass storage device, and an input-output port device, whereby each of the random access memory device, mass storage device, and input-output port device can be operated in conjunction with the microprocessor.

186. With further reference to the TOSHIBA products identified in **Exhibit C**, each of those products include a microprocessor, a random access memory device, a mass storage device, and an input-output port device, each of which either incorporates or is connected to at least one interface capable of receiving and transmitting data using packets.

187. With further reference to the TOSHIBA products identified in **Exhibit C**, each of those products include at least one data channel that extends between a microprocessor and the interface(s) of a random access memory device, a mass storage device, and an input-output port device for transporting data in packet form.

188. With further reference to the TOSHIBA products identified in **Exhibit C**, each of those products include at least one buffer, or memory location, for storing a copy of at least some of the packets that are transmitted by the microprocessor interface.

189. With further reference to the TOSHIBA products identified in **Exhibit C**, each of those products include at least one interface that is incorporated or connected to a microprocessor that is linked to or associated with a cache for storing at least some of the

requested data from either a random access memory device, a mass storage device, or an input-output port device.

190. With further reference to the TOSHIBA products identified in **Exhibit C**, each of those products include at least one interface incorporated or connected to a microprocessor, which interface includes a controller capable of accepting data and a physical address from the microprocessor, whereby the physical address identifies a particular physical address of either a random access memory device, a mass storage device, or an input-output port device.

191. TOSHIBA has sought to benefit from the reexaminations initiated by INTEL by, inter alia, using such reexaminations to seek a stay of this case.

192. TOSHIBA was aware that on October 28, 2008, the USPTO determined claims 14-28 patentable.

193. By continuing infringement during the period after October 28, 2008 and before March 16, 2009 (the date the Third INTEL Reexam was granted), TOSHIBA acted despite an objectively high likelihood that its actions constituted infringement of valid claims of the '488 patent.

194. Further to the immediately preceding paragraph, the objectively high likelihood of infringement was actually known to TOSHIBA or was so obvious it should have been known.

195. In light of the outcome of the First and Second INTEL Reexams, TOSHIBA knew or should have known that there was an objectively high risk that some or all claims at issue in the Third INTEL Reexam would eventually be confirmed.

196. TOSHIBA has willfully infringed valid claims of the '488 patent.

197. TOSHIBA's acts of infringement have caused damage to MICROLINC. Under 35 U.S.C. § 284, MICROLINC is entitled to recover from TOSHIBA the damages sustained by MICROLINC as a result of its infringement of the '488 patent. TOSHIBA's infringement on MICROLINC's exclusive rights under the '488 patent will continue to damage MICROLINC causing irreparable harm, for which there is no adequate remedy of law, unless enjoined by this Court under 35 U.S.C. § 283.

IV. PRAYER FOR RELIEF

WHEREFORE, MICROLINC respectfully requests that this Court enter judgment against Defendants INTEL CORPORATION, ACER INC., ACER AMERICA CORPORATION, ADVANCED MICRO DEVICES, INC., APPLE INC.,DELL INC., GATEWAY INC., HEWLETT-PACKARD CO., LENOVO GROUP LTD., LENOVO (UNITED STATES), INC., SONY CORPORATION,SONY CORPORATION OF AMERICA, SONY ELECTRONICS, INC.,SONY COMPUTER ENTERTAINMENT AMERICA, INC., TOSHIBA CORP., and TOSHIBA AMERICA INFORMATION SYSTEMS INC., as follows:

(a) for declaration that United States Patent No. 6,009,488 is good and valid in law;

(b) for judgment that Defendants have infringed and continue to infringe the '488 patent;

(c) for preliminary and permanent injunctions under 35 U.S.C. 283 against Defendants and their respective directors, officers, employees, agents, subsidiaries, parents, attorneys, and all persons acting in concert, on behalf of, in joint venture, or in partnership with any of the Defendants enjoining any further acts of infringement of the '488 patent;

(d) for damages to be paid by Defendants adequate to compensate MICROLINC for their infringement, including interest, costs and disbursements as justified under 35 U.S.C. 284,

(e) for judgment finding this to be an exceptional case, and awarding MICROLINC attorney fees under 35 U.S.C. 285; and

(f) for such further relief at law and in equity as the Court may deem just and proper.

V. DEMAND FOR JURY TRIAL

Pursuant to Federal Rules of Civil Procedure Rule 38, Plaintiff MICROLINC hereby demands a jury trial on all issues triable by jury.

Dated: November 16, 2012

Respectfully submitted,

By: /s/ S. Calvin Capshaw

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CERTIFICATE OF SERVICE

The undersigned attorney hereby certifies that on November 16, 2012, a true and correct copy of the **FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT** was filed electronically with the Clerk of the Court and was served via the Court's CM/ECF System which will automatically provide electronic notice upon all counsel of record.

/s/ S. Calvin Capshaw