IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

INTELLECTUAL VENTURES I LLC and INTELLECTUAL VENTURES II LLC, **Plaintiffs,** **v.** **CANON INC. and CANON U.S.A., INC.,** **Defendants.**	**Civil Action No. 11-cv-792-SLR** **JURY TRIAL DEMANDED**

SECOND AMENDED COMPLAINT

Plaintiffs Intellectual Ventures I LLC ("Intellectual Ventures I") and Intellectual Ventures II LLC ("Intellectual Ventures II") (collectively, "Intellectual Ventures I and II") for their Second Amended Complaint against Defendants Canon Inc. and Canon U.S.A, Inc. (collectively, "Canon") hereby allege as follows:

PARTIES

1. Intellectual Ventures I is a Delaware limited liability company with its principal place of business located in Bellevue, Washington.

2. Intellectual Ventures II is a Delaware limited liability company with its principal place of business located in Bellevue, Washington.

3. Defendant Canon Inc. is a corporation organized under the laws of Japan having a principal place of business at 30-2, Shimomaruko 3-chome, Ohta-ku, Tokyo 146-8501, Japan.

4. Defendant Canon U.S.A., Inc. is a corporation organized under the laws of New York, having a principal place of business at One Canon Plaza, Lake Success, New York, 11042-1113.

NATURE OF THE ACTION

5. This is a civil action for the infringement of United States Patent No. 5,754,348; United States Patent No. 6,023,081, United States Patent No. 6,121,960, United States Patent No. 6,221,686, United States Patent No. 6,979,587, and United States Patent No. 7,365,298 (collectively, the "Patents-in-Suit") under the Patent Laws of the United States, 35 U.S.C. § 1 *et seq*.

JURISDICTION AND VENUE

6. This Court has jurisdiction over the subject matter of this action pursuant to 28 U.S.C. §§ 1331 and 1338(a) because this action arises under the patent laws of the United States, including 35 U.S.C. § 271 *et seq*.

7. This Court has personal jurisdiction over Defendants because Defendants have committed acts of infringement in violation of 35 U.S.C. § 271 and have placed infringing products into the stream of commerce with the knowledge and/or understanding that such products are used and sold in this District. These acts have caused and continue to cause injury to Intellectual Ventures I and II within the District. Defendants derive substantial revenue from the sale of infringing products distributed within the District, and/or expect or should reasonably expect their actions to have consequences within the District, and derive substantial revenue from interstate and international commerce. In addition, Defendants knowingly induced, and continue to knowingly induce, infringement within this District by contracting with others to market and sell infringing products with the knowledge and intent to facilitate infringing sales of the products by others within this District and by creating and/or disseminating instructions and other materials for the products with like mind and intent.

8. Venue is proper in this judicial district as to Defendants pursuant to 28 U.S.C. §§ 1391 and 1400(b).

THE PATENTS-IN-SUIT

9. Paragraphs 1-8 are reincorporated by reference as if fully set forth herein.

10. On May 19, 1998, United States Patent No. 5,754,348 ("the '348 Patent"), titled "Method For Context-Preserving Magnification Of Digital Image Regions," was duly and lawfully issued by the PTO. The '348 Patent is attached hereto as Exhibit A.

11. Intellectual Ventures I owns the '348 Patent, and holds the right to sue and recover damages for infringement thereof, including past infringement.

12. On February 8, 2000, United States Patent No. 6,023,081 ("the '081 Patent"), titled "Semiconductor Image Sensor," was duly and lawfully issued by the PTO. The '081 Patent is attached hereto as Exhibit B.

13. Intellectual Ventures II owns the '081 Patent, and holds the right to sue and recover damages for infringement thereof, including past infringement.

14. On September 19, 2000, United States Patent No. 6,121,960 ("the '960 Patent"), titled "Touch Screen Systems And Methods," was duly and lawfully issued by the PTO. The '960 Patent is attached hereto as Exhibit C.

15. Intellectual Ventures II owns the '960 Patent, and holds the right to sue and recover damages for infringement thereof, including past infringement.

16. On April 24, 2001, United States Patent No. 6,221,686 ("the '686 Patent"), titled "Method Of Making A Semiconductor Image Sensor," was duly and lawfully issued by the PTO. The '686 Patent is attached hereto as Exhibit D.

17. Intellectual Ventures II owns the '686 Patent, and holds the right to sue and recover damages for infringement thereof, including past infringement.

18. On December 27, 2005, United States Patent No. 6,979,587 ("the '587 Patent"), titled "Image Sensor And Method For Fabricating The Same," was duly and lawfully issued by the PTO. The '587 Patent is attached hereto as Exhibit E.

19. Intellectual Ventures II owns the '587 Patent, and holds the right to sue and recover damages for infringement thereof, including past infringement.

20. On April 29, 2008, United States Patent No. 7,365,298 ("the '298 Patent"), titled "Image Sensor And Method For Manufacturing The Same," was duly and lawfully issued by the PTO. The '298 Patent is attached hereto as Exhibit F.

21. Intellectual Ventures II owns the '298 Patent, and holds the right to sue and recover damages for infringement thereof, including past infringement.

FACTUAL BACKGROUND

22. Intellectual Ventures Management, LLC ("Intellectual Ventures") was founded in 2000. Since its founding, Intellectual Ventures has been deeply involved in the business of invention. Intellectual Ventures creates inventions and files patent applications for those inventions; collaborates with others to develop and patent inventions; and acquires and licenses patents from individual inventors, universities, and other institutions. A significant aspect of Intellectual Ventures' business is managing the plaintiffs in this case, Plaintiff Intellectual Ventures I and Plaintiff Intellectual Ventures II.

23. Intellectual Ventures' business includes purchasing important inventions from individual inventors and institutions and then licensing the inventions to those who need them. Through this business, Intellectual Ventures allows inventors to reap a financial reward from

their innovations, a frequently difficult task for individual inventors. To date, Intellectual Ventures has purchased more than 35,000 assets and, in the process, has paid individual inventors more than $400 million for their inventions. Intellectual Ventures, in turn, has earned more than $2 billion by licensing these patents to some of the world's most innovative and successful technology companies who continue to use them to make computer equipment, software, semiconductor devices, consumer products, and a host of other products.

24. Intellectual Ventures also develops its own inventions. Intellectual Ventures has a staff of scientists and engineers who develop ideas in a broad range of fields, including agriculture, computer hardware, life sciences, medical devices, semiconductors, and software. Intellectual Ventures has invested millions of dollars developing such ideas and has filed hundreds of patent applications on its inventions every year, making it one of the top patent filers in the world. Intellectual Ventures also has invested in laboratory facilities to assist with the development and testing of new ideas.

25. Intellectual Ventures also develops inventions by collaborating with inventors and research institutions around the world. For example, Intellectual Ventures has developed inventions by selecting a technical challenge, requesting proposals for inventions to solve the challenge from inventors and institutions, selecting the most promising ideas, rewarding the inventors and institutions for their contributions, and filing patent applications on the ideas. Intellectual Ventures has invested millions of dollars in this way and has created a network of more than 3000 inventors worldwide.

26. Canon is a global company that designs, manufactures, and markets consumer electronics, including digital single-lens reflex ("DSLR") cameras, compact digital cameras, and digital camcorders.

27. Beginning in 2009, Intellectual Ventures approached Canon about taking a license to Intellectual Ventures' patents. Over the next several months, in an effort to negotiate a license, Intellectual Ventures discussed many of its patents with Canon including several of the patents asserted against Canon in this complaint. Further, Intellectual Ventures explained to Canon how Canon was using Intellectual Ventures' patented inventions in its digital imaging products. Despite Intellectual Ventures' good-faith efforts to negotiate a business solution, Canon has failed and refused to license Intellectual Ventures' patents on reasonable terms, and continues to use those inventions without permission.

COUNT I

(Canon's Infringement of the '348 Patent)

28. Paragraphs 1-27 are incorporated by reference as if fully restated herein.

29. Canon, either alone or in conjunction with others, has infringed and/or knowingly and intentionally induced others including its customers to infringe, literally and/or under the doctrine of equivalents, one or more claims of the '348 Patent by making, using, offering to sell, selling and/or importing in or into the United States digital imaging products (including but not limited to digital camera PowerShot models A80, A95, A470, A480, A490, A495, A510, A520, A530, A540, A570 IS, A580, A590 IS, A610, A620, A630, A640, A650 IS, A700, A710 IS, A720 IS, A800, A1000 IS, A1100 IS, A1200, A2000 IS, A2100 IS, A2200, A3200 IS, A3300 IS, A3000 IS, A3100 IS, S1 IS, S2 IS, S3 IS, S5 IS, S45, S50, S60, S70, S80, S90, S95, G3, G5, G6, G7, G9, G10, G11, G12, Pro1, ELPH 100 HS, ELPH 300 HS, ELPH 500 HS, SD770 IS, SD780 IS, SD790 IS, SD880 IS, SD890 IS, SD940 IS, SD960 IS, SD970 IS, SD980 IS, SD990 IS, SD1100 IS, SD1200 IS, SD1300 IS, SD1400 IS, SD3500 IS, SD4000 IS, SD4500 IS, D10, E1,

SX1 IS, SX20 IS, SX30 IS, SX100 IS, SX110 IS, SX120 IS, SX130 IS, SX200 IS, SX210 IS, SX220 HS, and SX230 HS) without authority and in violation of 35 U.S.C. § 271.

30. Canon has had knowledge of and notice of the '348 Patent and its infringement since at least February 8, 2011, through a presentation by Intellectual Ventures to Canon concerning the '348 Patent and its infringement, and September 9, 2011, through the filing and service of the original Complaint with this Court. Intellectual Ventures also notified Canon of the filing of the Complaint on September 9, 2011. Canon possessed, and continues to possess, the specific intent to encourage others, including its customers, to infringe the '348 patent.

31. Intellectual Ventures I has suffered damage as a result of Canon's infringement of the '348 Patent.

COUNT II

(Canon's Infringement of the '081 Patent)

32. Paragraphs 1-31 are incorporated by reference as if fully restated herein.

33. Canon, either alone or in conjunction with others, has infringed and/or knowingly and intentionally induced others including its customers to infringe, literally and/or under the doctrine of equivalents, one or more claims of the '081 Patent by making, using, offering to sell, selling and/or importing in or into the United States digital imaging products (including but not limited to Canon's Vixia HF 20 camcorder) without authority and in violation of 35 U.S.C. § 271.

34. Canon has had knowledge of and notice of the '081 Patent and its infringement since at least September 9, 2011, through the filing and service of the original Complaint with this Court. Intellectual Ventures also notified Canon of the filing of the Complaint on September

9, 2011. Canon possessed, and continues to possess, the specific intent to encourage others, including its customers, to infringe the ’081 patent.

35. Intellectual Ventures II has suffered damage as a result of Canon’s infringement of the ’081 Patent.

COUNT III

(Canon’s Infringement of the ’960 Patent)

36. Paragraphs 1-35 are incorporated by reference as if fully restated herein.

37. Canon, either alone or in conjunction with others, has infringed and/or knowingly and intentionally induced others including its customers to infringe, literally and/or under the doctrine of equivalents, one or more claims of the ’960 Patent by making, using, offering to sell, selling and/or importing in or into the United States digital imaging products (including but not limited to Canon’s Vixia HF M40, HF M31 camcorders, and the PowerShot SD3500IS camera) without authority and in violation of 35 U.S.C. § 271.

38. Canon has had knowledge of and notice of the ’960 Patent and its infringement since at least February 8, 2011, through a presentation by Intellectual Ventures to Canon concerning the ’960 Patent and its infringement, and September 9, 2011, through the filing and service of the original Complaint with this Court. Intellectual Ventures also notified Canon of the filing of the Complaint on September 9, 2011. Canon possessed, and continues to possess, the specific intent to encourage others, including its customers, to infringe the ’960 patent.

39. Intellectual Ventures II has suffered damage as a result of Canon’s infringement of the ’960 Patent.

COUNT IV

(Canon’s Infringement of the ’686 Patent)

40. Paragraphs 1-39 are incorporated by reference as if fully restated herein.

41. Canon, either alone or in conjunction with others, has infringed, knowingly and intentionally induced others including its customers, literally and/or under the doctrine of equivalents, one or more claims of the '686 Patent by making, using, offering to sell, selling and/or importing in or into the United States digital imaging products (including but not limited to Canon's EOS 50D camera) without authority and in violation of 35 U.S.C. § 271.

42. Canon has had knowledge of and notice of the '686 Patent and its infringement since at least August 27, 2010, through a presentation by Intellectual Ventures to Canon concerning the '686 Patent and its infringement, and September 9, 2011, through the filing and service of the original Complaint with this Court. Intellectual Ventures also notified Canon of the filing of the Complaint on September 9, 2011. Canon possessed, and continues to possess, the specific intent to encourage others, including its customers, to infringe the '686 patent.

43. Intellectual Ventures II has suffered damage as a result of Canon's infringement of the '686 Patent.

COUNT V

(Canon's Infringement of the '587 Patent)

44. Paragraphs 1-43 are incorporated by reference as if fully restated herein.

45. Canon, either alone or in conjunction with others, has infringed and/or knowingly and intentionally induced others including its customers to infringe, literally and/or under the doctrine of equivalents, one or more claims of the '587 Patent by making, using, offering to sell, selling and/or importing in or into the United States digital imaging products (including but not limited to Canon's EOS 50D camera, and cameras incorporating the Canon 1100 CMOS Image

Sensor such as Canon's EOS 1DS Mark III and EOS 5D Mark II cameras) without authority and in violation of 35 U.S.C. § 271.

46. Canon has had knowledge of and notice of the '587 Patent and its infringement since at least September 28, 2009, through a presentation by Intellectual Ventures to Canon concerning the '587 Patent and its infringement, and September 9, 2011, through the filing and service of the original Complaint with this Court. Intellectual Ventures also notified Canon of the filing of the Complaint on September 9, 2011. Canon possessed, and continues to possess, the specific intent to encourage others, including its customers, to infringe the '587 patent.

47. Intellectual Ventures II has suffered damage as a result of Canon's infringement of the '587 Patent.

COUNT VI

(Canon's Infringement of the '298 Patent)

48. Paragraphs 1-47 are incorporated by reference as if fully restated herein.

49. Canon, either alone or in conjunction with others, has infringed and/or knowingly and intentionally induced others including its customers to infringe, literally and/or under the doctrine of equivalents, one or more claims of the '298 Patent by making, using, offering to sell, selling and/or importing in or into the United States digital imaging products (including but not limited to Canon's EOS 50D camera, and cameras incorporating the Canon 1100 CMOS Image Sensor) without authority and in violation of 35 U.S.C. § 271.

50. Canon has had knowledge of and notice of the '298 Patent and its infringement through the filing and service of the Second Amended Complaint with this Court. Canon possessed, and continues to possess, the specific intent to encourage others, including its customers, to infringe the '298 patent.

51. Intellectual Ventures II has suffered damage as a result of Canon's infringement of the '298 Patent.

PRAYER FOR RELIEF

WHEREFORE, Intellectual Ventures I and II respectfully request the following relief:

a) A judgment that Canon has infringed the '348 Patent;

b) A judgment that Canon has infringed the '081 Patent;

c) A judgment that Canon has infringed the '960 Patent;

d) A judgment that Canon has infringed the '686 Patent;

e) A judgment that Canon has infringed the '587 Patent;

f) A judgment that Canon has infringed the '298 Patent;

g) A judgment that Intellectual Ventures I be awarded all appropriate damages under 35 U.S.C. § 284 for Canon's past infringement and any continuing or future infringement of the '348 Patent up until the date such judgment is entered, including interest, costs, and disbursements as justified under 35 U.S.C. § 284 and, if necessary, to adequately compensate Intellectual Ventures I for Canon's infringement, an accounting:

   a. that Intellectual Ventures I be awarded the attorney fees, costs, and expenses that it incurs in prosecuting this action; and

   b. that Intellectual Ventures I be awarded such further relief at law or in equity as the Court deems just and proper.

h) A judgment that Intellectual Ventures II be awarded all appropriate damages under 35 U.S.C. § 284 for Canon's past infringement and any continuing or future infringement of the '081, '960, '686, '587, and '298 Patents up until the date such judgment is entered,

including interest, costs, and disbursements as justified under 35 U.S.C. § 284 and, if necessary, to adequately compensate Intellectual Ventures II for Canon's infringement, an accounting:

a. that Intellectual Ventures II be awarded the attorney fees, costs, and expenses that it incurs in prosecuting this action; and

b. that Intellectual Ventures II be awarded such further relief at law or in equity as the Court deems just and proper.

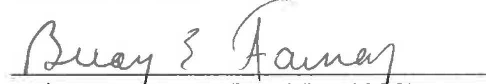
DEMAND FOR JURY TRIAL

Intellectual Ventures I and Intellectual Ventures II hereby demand trial by jury on all claims and issues so triable.

DATED: December 21, 2012

Respectfully submitted,

FARNAN LLP



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Counsel for Plaintiffs

EXHIBIT A

US005754348A

United States Patent [19]

Soohoo

[11] Patent Number: 5,754,348

[45] Date of Patent: May 19, 1998

[54] **METHOD FOR CONTEXT-PRESERVING MAGNIFICATION OF DIGITAL IMAGE REGIONS**

[75] Inventor: **Kenneth Soohoo**, Redwood Shores, Calif.

[73] Assignee: **Planetweb, Inc.**, Mountain View, Calif.

[21] Appl. No.: **645,853**

[22] Filed: **May 14, 1996**

[51] **Int. Cl.**⁶ **G02B 27/02**

[52] **U.S. Cl.** **359/802**; 359/803; 359/436; 359/442

[58] **Field of Search** 359/802, 803, 359/804, 806, 809, 810, 436, 440, 441, 442

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,704,938	12/1972	Fanselow	359/442
3,739,739	6/1973	Brase	359/436
3,762,799	10/1973	Shapiro	359/442
4,757,616	7/1988	Hills	359/442
5,031,918	7/1991	Brill	359/802
5,275,019	1/1994	Pagani	359/802
5,309,279	5/1994	Halstead	359/442
5,369,527	11/1994	McCracken	359/803

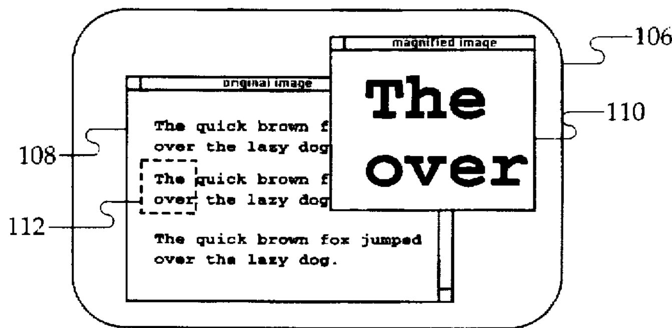
Primary Examiner—Loha Ben

Attorney, Agent, or Firm—Wilson Sonsini Goodrich & Rosati

[57] **ABSTRACT**

A method for digital image magnification in a graphical user interface is disclosed. In contrast with prior methods which magnify a selected region of an original image without preserving its context, the present method provides a method for magnification that allows simultaneous viewing of the magnified image and its unmagnified context. In a preferred embodiment, the method provides a floating window [122] superimposed on an original image. Displayed within the floating window is a magnified image of a selected region of the original image. The floating window is centrally positioned over the selected region. In one aspect of the invention, the floating window is partially transparent so that portions of the original image within the floating window [124] are displayed in a faint manner in comparison to portions of the original image outside the floating window [126]. As the selected region is moved, typically by a user-controlled pointing device, the floating window [122] also moves.

11 Claims, 6 Drawing Sheets



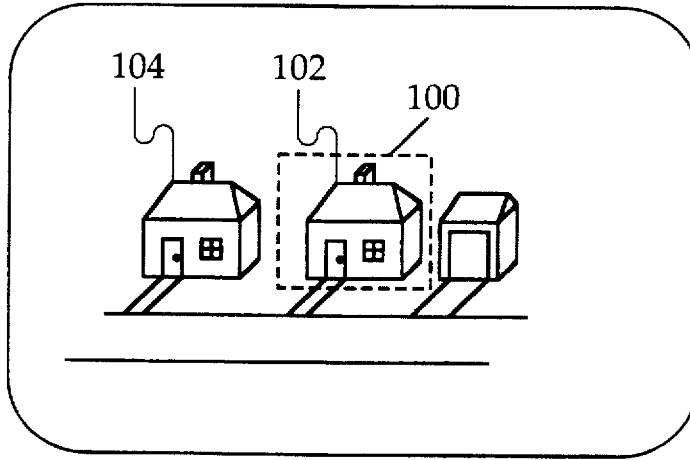


FIG. 1

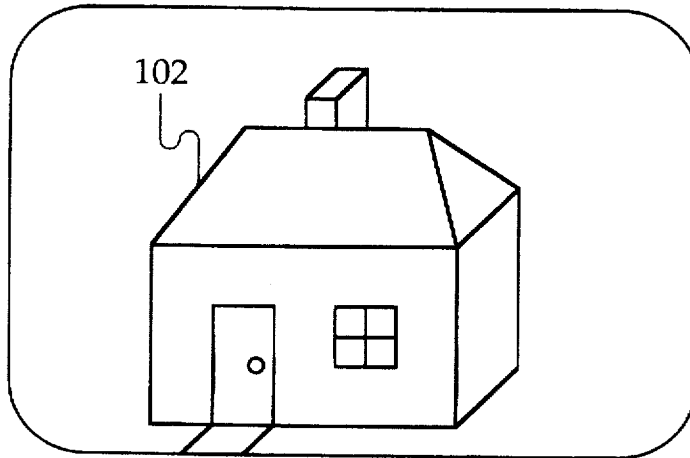


FIG. 2

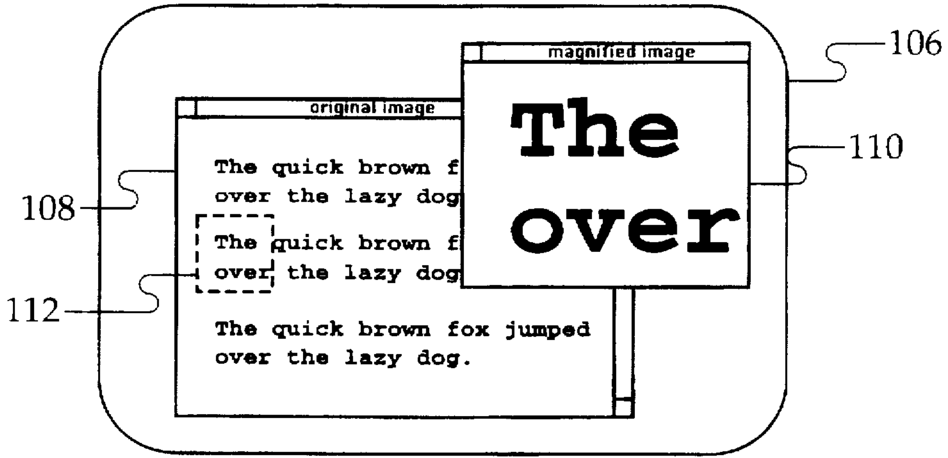


FIG. 3

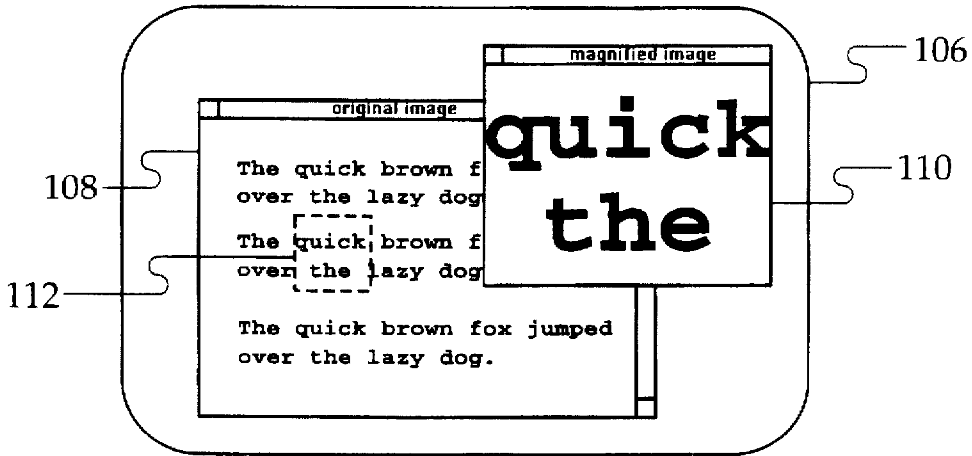


FIG. 4

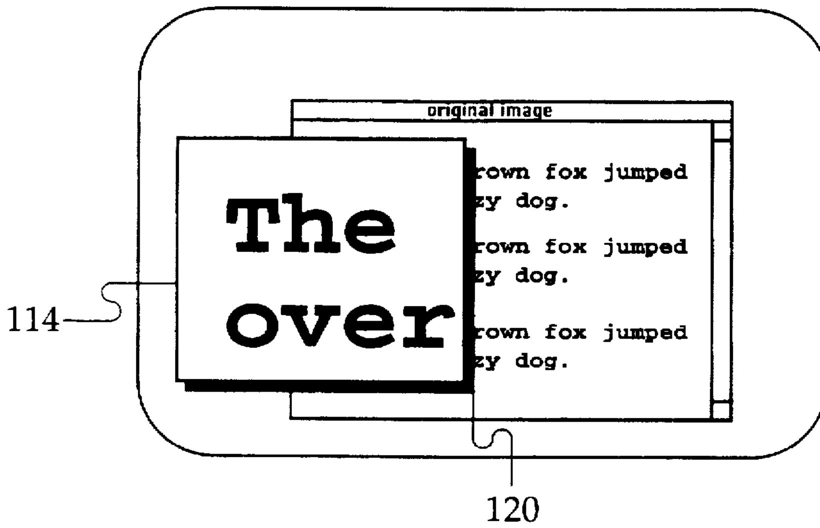
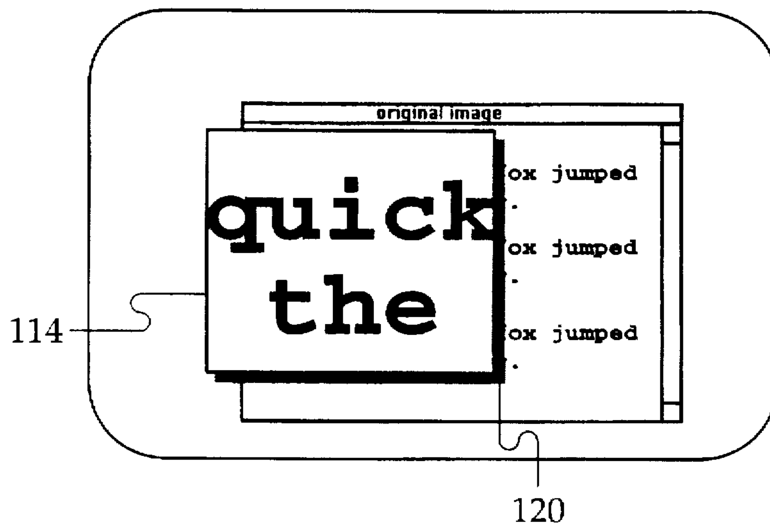


FIG. 5



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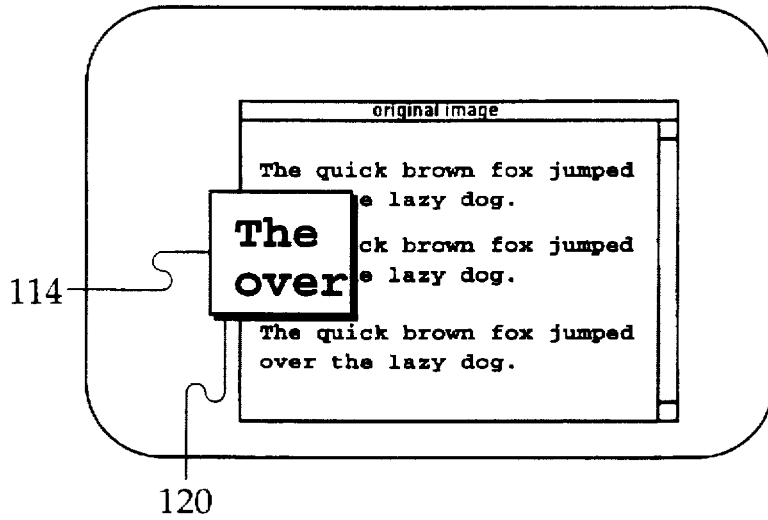

FIG. 7

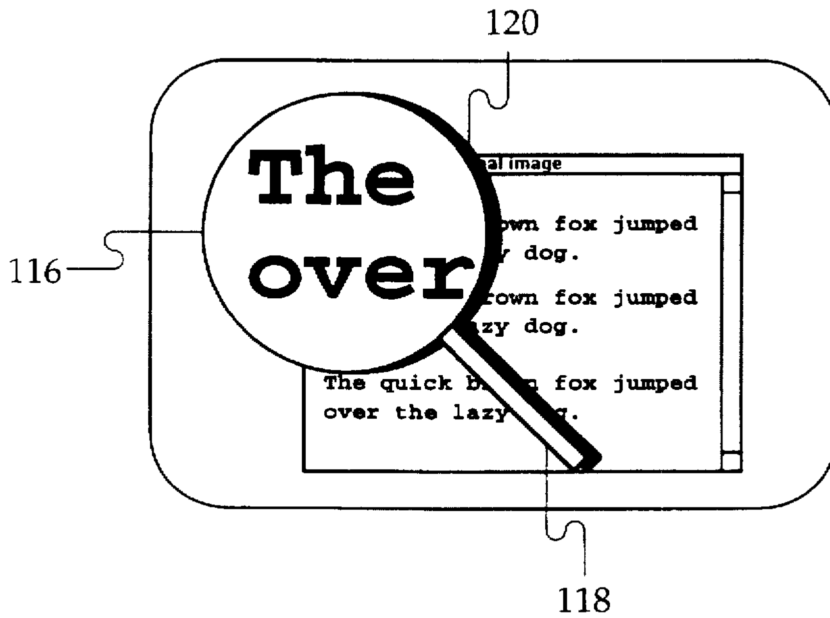

FIG. 8

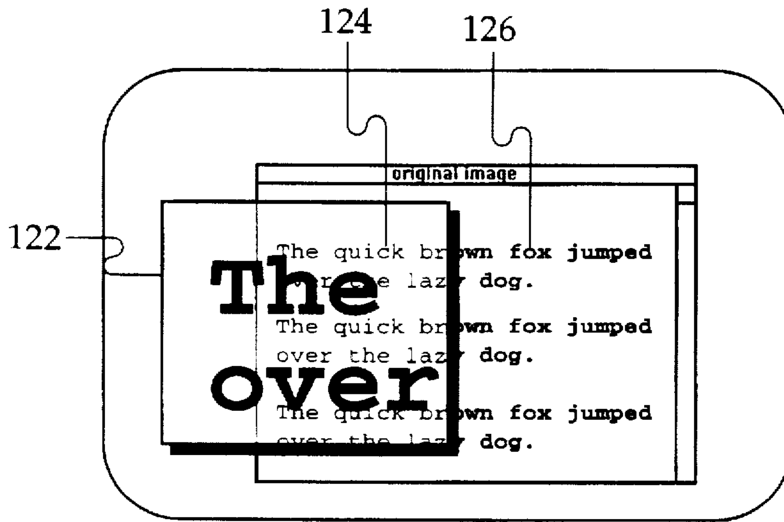

FIG. 9

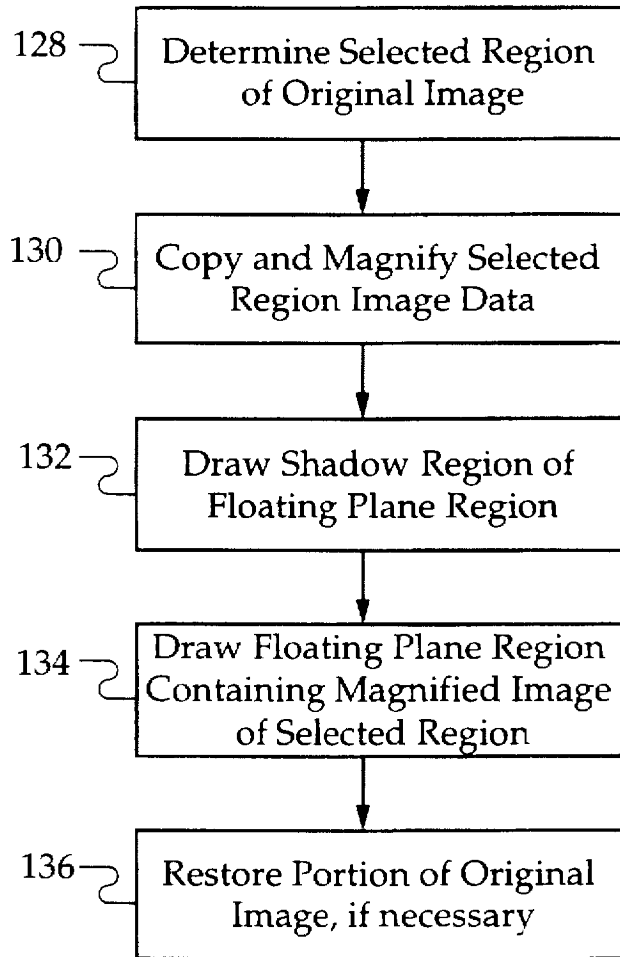

FIG. 10

METHOD FOR CONTEXT-PRESERVING MAGNIFICATION OF DIGITAL IMAGE REGIONS

BACKGROUND

The field of the invention relates generally to graphical user interfaces. More particularly, the field of the invention relates to a method for dynamically magnifying a moveable selected region of a digital image while preserving the visual context of the image.

When viewing images displayed on a computer or television screen, one often experiences difficulty discerning small details and would like to view a portion of the image in a magnified format. Conventional methods for digital image magnification solve this problem by replacing the original unmagnified image with a magnified image of a selected region of the original image. Although this provides a magnified format for viewing small details of the original image, it has the disadvantage that the context of the magnified image presented to the viewer is lost.

For example, FIG. **1** shows an original unmagnified image as it is displayed on a typical computer or television screen. After selecting a region **100** of the image, conventional magnification methods fill the entire screen with a magnified image of the selected region, as shown in FIG. **2**. The magnified image displayed in FIG. **2**, however, does not provide any context for the magnified region. Without contextual cues, the viewer can lose track of the meaning of the magnified image. Also, the image can be confused with other portions of the original unmagnified image. For instance, house **102** in FIG. **2** may be confused with house **104** in FIG. **1** since the houses are distinguishable only by their context. Some methods for magnification allow dynamic movement of the selected region **100** that is magnified. A pointing device is used to control the position of the magnified region while the magnified image is being viewed. Using this technique, however, one must determine the context of the magnified image by moving the selected region in various directions to bring the contextual information into view. This approach is both slow and inconvenient.

In view of the above problems present in conventional methods of image magnification, there is a need to provide an image magnification method that magnifies a selected region of an image while simultaneously preserving the continuity and integrity of the original unmagnified image that forms the visual context of the magnified region. There is also a need to provide a method of image magnification that permits dynamic control of the position of the magnified region and the degree of magnification. Other objectives and advantages will be apparent from the following description and drawings.

SUMMARY

In order to achieve the foregoing objectives and advantages, an aspect of the present invention provides a method for magnifying a selected region of an image while preserving the visual context of the region. A selected region of a digital image is magnified and displayed in a floating plane region superimposed on the original image. The floating plane region is also termed a magnifier since the image data in the floating plane may be selectively magnified to provide a greatly enlarged image of the selected region while preserving the visual context of the image outside the parameters of the magnifier. Because the floating plane area is smaller than the original image area, the context of the magnified region remains displayed around the magnified image. The area of the floating plane region is equal to a magnification factor times the area of the selected region. In another aspect of the invention, the selected region may be moved, e.g., in response to the movement of a user-controlled pointing device. As the selected region moves across the original image, the magnified image displayed in the floating plane region is dynamically modified.

In one implementation of the invention, the floating plane region is superimposed above the selected region so that the floating plane moves as the selected region moves. The effect is similar to that of a magnifying glass moving in a plane above the image. As the floating plane is moved, an aspect of the invention provides for restoring a portion of the original image which was previously covered by the floating plane. The visual context of the image is therefore preserved while enabling a movable portion of the image to be magnified.

It will be appreciated that preserving visual context is especially advantageous when magnifying a line of text or other image data whose interpretation is context dependent.

According to an aspect of the invention, the magnified image in the floating plane region can be superimposed on a moving image to provide a moving magnified image while preserving the visual context of the moving image on the computer screen.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows an original unmagnified image as it is displayed on a typical computer or television screen.

FIG. **2** shows the result of using a conventional magnification method to magnify the selected region of FIG. **1**.

FIG. **3** shows the result of using a simplified embodiment of the invention to magnify a selected region of an original image.

FIG. **4** shows the result of moving the selected region from the position shown in FIG. **3**, according to a preferred embodiment of the present invention.

FIG. **5** shows the result of using a preferred embodiment to generate a floating plane region containing a magnified image of a selected region of the original image.

FIG. **6** shows the result of moving the selected region from the position shown in FIG. **5**, according to the present invention.

FIG. **7** shows an aspect of the present invention wherein the image is magnified to a lesser degree than that shown in FIGS. **3–6**.

FIG. **8** shows the result of using an embodiment of the present invention wherein the floating plane region is circular.

FIG. **9** shows an aspect of a preferred embodiment wherein the floating plane region is partially transparent.

FIG. **10** is a flow diagram outlining the steps of a preferred embodiment of the present invention.

DETAILED DESCRIPTION

For the purposes of explanation, a simplified embodiment of the invention will be described first. The invention is presently executable on a Sega Saturn system. However, one skilled in the art would be readily capable of implementing the invention on any personal computer without undue experimentation. In this embodiment, an original image is magnified as shown in FIG. **3**. Displayed on a computer screen **106** are an original image window **108** containing an

original image, and a magnified image window **110** containing a magnified image. A selected region **112** of the original image is magnified and displayed within magnified image window **110**. Typically, selected region **112** will have a position determined by a user-controlled pointing device, such as a mouse. In this example, selected region **112** contains two words of text. The enlarged text in the magnified image will provide an easy and convenient means for making the text in the selected region more legible. As shown in FIG. **4**, as the selected region **112** is moved to a different part of the original image, the magnified image **110** changes accordingly. It is clear that this method of image magnification, in contrast to those of the prior art, preserves the context of the selected region while the magnified image is displayed.

In a preferred embodiment of the invention, the magnified image is displayed in a floating plane region **114**, as shown in FIG. **5**. Floating plane region **114** is a magnified image window that is positioned on top of the selected region, and moves as the selected region is moved. For example, FIGS. **5** and **6** show the movement of the floating plane region as the selected region is moved. The positions of the selected region in FIGS. **5** and **6** are the same as the positions of the selected region shown in FIGS. **3** and **4**, respectively. The original image is preferably defined to be the entire screen, and is not necessarily restricted to an original image window, which is used in this description only for clarity of explanation.

It will be appreciated that the magnified image data in the floating plane region **114** are continually updated, as the floating plane is moved, to preserve the visual context of the underlying image. The image data outside the parameters of the magnified floating plane region **114** are also restored to preserve the preexisting visual context of the overall image. This aspect of the invention advantageously provides in-place magnification that can be dynamically moved while restoring underlying nonselected image data. This also provides the advantage of preserving and restoring the visual context of the entire image.

In the preferred embodiment illustrated in FIG. **7**, the size of the floating plane region **114** may be changed in size and the magnification factor may also be changed. That is, the plane region **114** provides a magnifier that can dynamically magnify a moveable selected region to any desired magnification factor while preserving the visual context of the preexisting image. As the magnification factor for the floating plane region **114** increases, the nonselected image data outside the parameters of the floating plane region are restored to preserve the visual context of the overall image. Anyone of ordinary skill in the art will appreciate that these and many other specifics may be changed as well. For example, FIG. **8** shows a variation of the preferred embodiment having a floating plane region **116** with a circular shape. A handle **118** attached to region **116** gives this variation of the invention the look and feel of a conventional magnifying glass. The preferred embodiment of the invention further includes a shadow region **120** having a shape corresponding to that of its corresponding floating plane region. Shadow region **120** provides the magnification method with the added advantage of helping distinguish the magnified region from the original image, and creates the illusion that the corresponding floating plane region is floating above the original image.

Referring to FIGS. **7** and **8**, it will be appreciated that the magnifier or floating plane region **114**, **116** also can have a rectilinear shape. A rectilinear magnifier has the advantage of preserving a line of text. Since text flows from left to right, moving a rectilinear magnified region from left to right has the advantage of communicating an increased amount of information from a line of text, while preserving the overall visual context of the page.

In another aspect of the invention, a floating plane region **122** is provided which is transparent to the original image beneath it, as shown in FIG. **9**. This feature has the advantage that it allows the user to see even more context. In order to prevent confusion within the floating plane between the magnified image and the original image, the floating plane is not fully transparent. As shown in FIG. **9**, parts of the original image under the floating plane, such as the word "quick" **124**, are faded or of reduced intensity compared with parts of the original image outside the floating plane, such as the word "fox" **126**.

In a preferred embodiment, the present method for digital image magnification in a graphical user interface is implemented on a device including a microprocessor connected to a display and a pointing device. For example, the present invention is executable on a Sega Saturn system. However, the present method also may be implemented on a common desktop computer, a video game, a video editing or viewing system, or a desktop publishing system by one skilled in the art. As illustrated in FIG. **10**, the position of a user-controlled pointing device determines a selected region of the original image (block **128**). The microprocessor then executes commands (block **130**) to copy or otherwise acquire image data within the selected region and magnify it by standard methods. This image data may be represented in the form of pixels, a page description language, or any another form. The microprocessor then draws the shadow region for the floating plane region (block **132**) and draws the floating plane region containing the magnified image data (block **134**). Because the user-operated pointing device may have caused the selected region to change position, the floating plane may have changed position accordingly. Consequently, a portion of the original image that was covered by a previous position of the floating plane may need to be restored. If this is the case, the microprocessor executes commands to restore this previously covered portion of the original image (block **136**).

Referring again to FIGS. **1** and **2** and assuming FIGS. **1** and **2** represent a moving video image, in accordance with another aspect of the invention, it is possible to dynamically magnify a selected portion of a moving video image while preserving the visual context of the overall image. For example, assuming FIG. **2** represents a real time video surveillance image of a house, it is possible to selectively magnify a portion of the house such as a doorway or window to identify a person. Here also the preexisting visual context of the image is preserved.

The application to a moving image is accomplished, as is well known to those skilled in the art, by making appropriate timing modifications for refreshing the contents of the floating plane or magnifier. One normally needs to refresh the contents of the floating plane every time it is moved. In the case of dynamically magnifying a moving image, it is necessary to synchronize the refreshing of the contents of the floating plane with the movement of the underlying image data. For example, if the underlying image is running at 12 frames per second (fps), the contents of the magnified floating plane must be refreshed in synchronization with the 12 fps movement of the image. Synchronization and data refresh techniques are well known to those skilled in the art and can be readily implemented by one skilled in the art with respect to the present invention to provide dynamic magnification of a moving image while preserving the visual context of the overall image.

The hardware required to implement the above described functions is well known in the art. In a preferred embodiment, a customized video processor is used to perform the required video display functions. In addition, anyone of ordinary skill in the art of computer programming is able to appropriately program a microprocessor to magnify image regions in accordance with the present teaching.

Although the foregoing description contains many details particular to specific embodiments of the present invention, these details are for the purpose of illustrating and enabling such embodiments, and are not intended to limit the scope of the invention. Accordingly, the scope of the invention should be determined by the following claims and their legal equivalents.

What is claimed is:

1. A method of digital image magnification in a graphical user interface, the method comprising: selecting for magnification a selected region of an original image in the graphical user interface; and superimposing on the original image a floating plane region in the graphical user interface containing a magnified image of the selected region, wherein the floating plane region has an area larger than an area of the selected region and smaller than an area of the original image, such that the selected region of the original image is magnified and viewed while preserving the context of the selected region.

2. The method of claim 1 further comprising restoring a portion of the original image, wherein the portion restored was previously covered by a prior position of the floating plane region.

3. The method of claim 1 wherein the floating plane region is superimposed on the original image such that the floating plane region covers the selected region of the original image.

4. The method of claim 1 wherein the selected region is selected by a user-operated pointing device.

5. The method of claim 1 further comprising the step of superimposing on the original image a shadow region corresponding to the floating plane region.

6. The method of claim 1 wherein the floating plane region is superimposed on the original image such that the floating plane region has a position that remains constant while the selected region is moved.

7. A method for dynamically magnifying a moveable selected region of a video image comprising the steps of:

providing an arbitrary moveable selection region;

creating a magnified floating plane of image data corresponding to said moveable selection region;

dynamically magnifying the moveable selection region;

restoring image data outside of the moveable selection region.

8. A method for dynamically magnifying a selected portion of a moving digital video image moving at a selected frame rate, while preserving the visual context of the overall image comprising the steps of:

selecting an arbitrary region of the moving video image for magnification;

providing a floating plane of data corresponding to the selected region;

refreshing the contents of the selected region in synchronization with the frame rate of the moving video image;

dynamically magnifying the digital video image in the selected region; and

restoring the digital video image outside the selected region to preserve the context of the overall video image.

9. A method of digital image magnification in a graphical user interface, the method comprising:

selecting for magnification a selected region of an original image in the graphical user interface;

superimposing on the original image a floating plane region in the graphical user interface containing a magnified image of the selected region, the floating plane region having an area larger than an area of the selected region and smaller than an area of the original image; and

in response to input from a user

moving the selected region,

moving the floating plane while the selected region is moved, and

dynamically modifying the magnified image of the selected region to correspond to the selected region.

10. The method of claim 9, wherein the input from a user comprises movement of a user-controlled pointing device.

11. The method of claim 9, wherein the floating plane region is partially transparent.

* * * * *

EXHIBIT B

US006023081A

United States Patent [19]

Drowley et al.

[11] Patent Number: 6,023,081

[45] Date of Patent: Feb. 8, 2000

[54] SEMICONDUCTOR IMAGE SENSOR

[75] Inventors: **Clifford I. Drowley**, Phoenix; **Mark S. Swenson**, Higley; **Jennifer J. Patterson**, Mesa; **Shrinath Ramaswami**, Gilbert, all of Ariz.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **08/970,720**

[22] Filed: **Nov. 14, 1997**

[51] **Int. Cl.**[7] **H01L 31/062**; H01L 31/113

[52] **U.S. Cl.** **257/292**; 257/290; 257/293

[58] **Field of Search** 257/290–293, 257/53, 232–233, 369, 225–230

[56] **References Cited**

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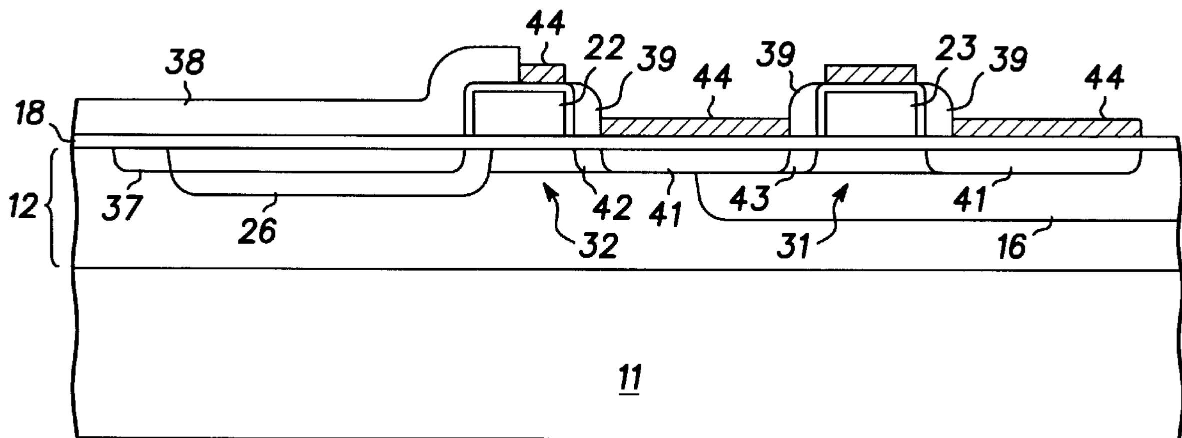
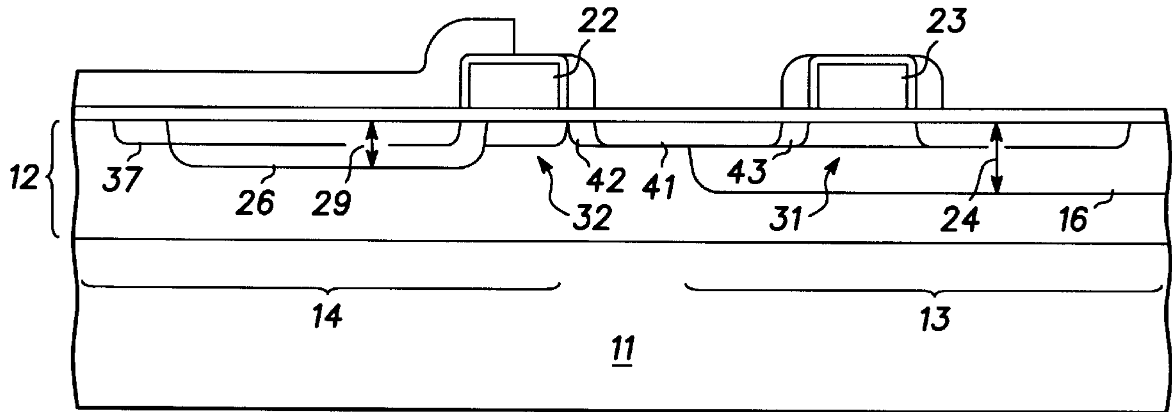
Primary Examiner—Minh Loan Tran
Assistant Examiner—Cuong Quang Nguyen
Attorney, Agent, or Firm—Robert F. Hightower; A. Kate Huffman

[57] **ABSTRACT**

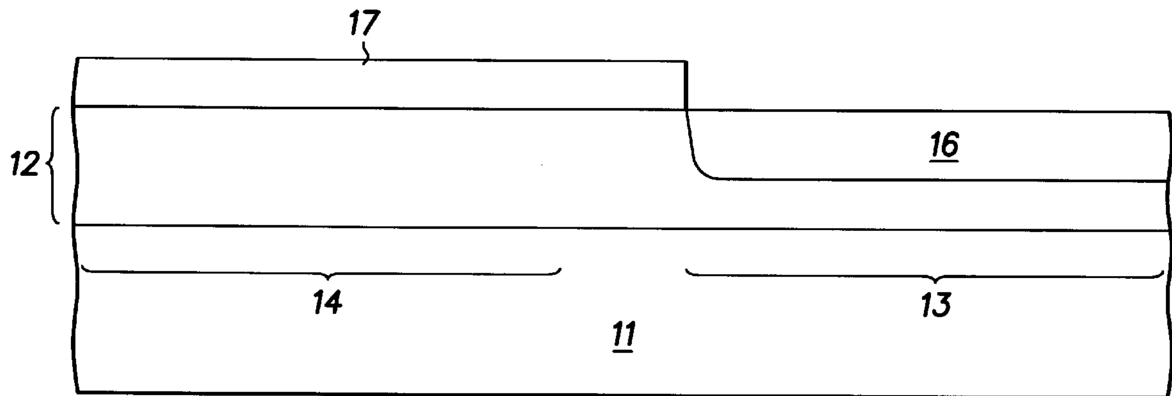
An image sensor (**10**) has an image sensing element that includes an N-type conducting region (**26**) and a P-type pinned layer (**37**). The two regions form two P-N junctions at different depths that increase the efficiency of charge carrier collection at different frequencies of light. The conducting region (**26**) is formed by an angle implant that ensures that a portion of the conducting region (**26**) can function as a source of an MOS transistor (**32**).

4 Claims, 3 Drawing Sheets

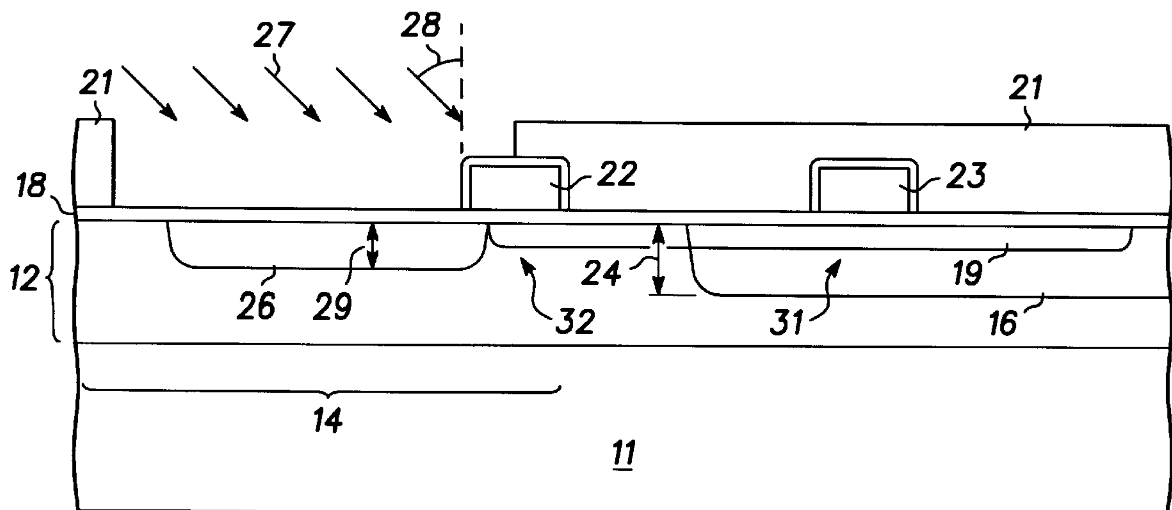




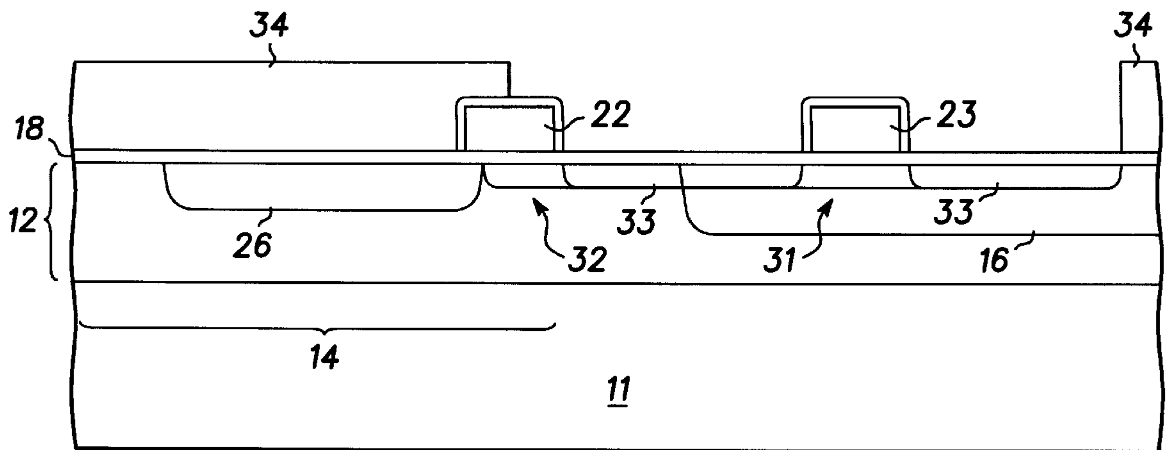
10 FIG. 1



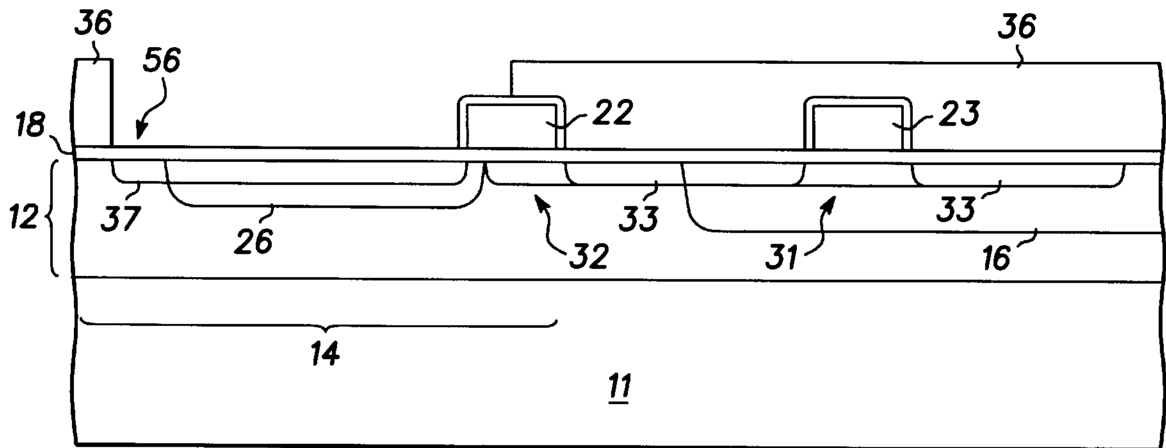
10 FIG. 2



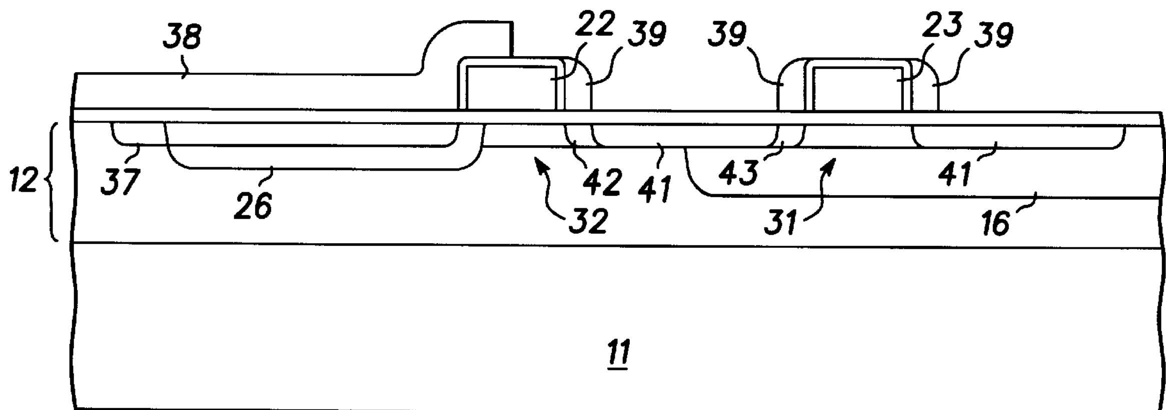
10 FIG. 3



10 FIG. 4



10 FIG. 5



10 FIG. 6

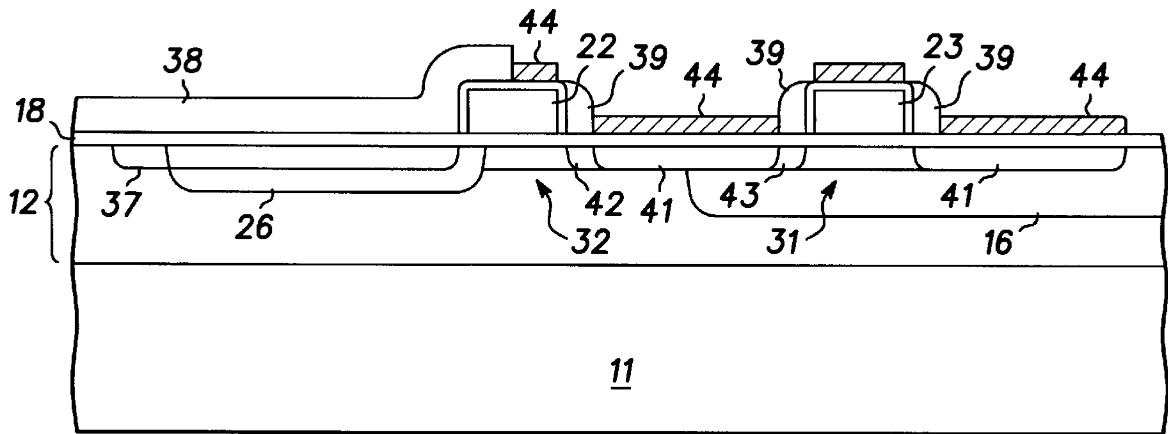


FIG. 7

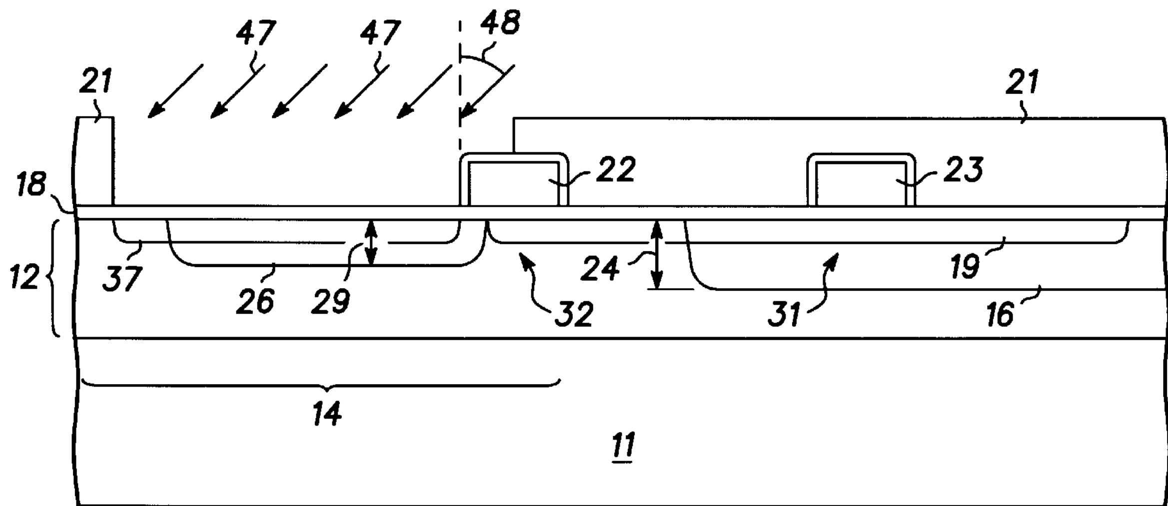


FIG. 8

SEMICONDUCTOR IMAGE SENSOR

BACKGROUND OF THE INVENTION

This application is related to an application entitled CMOS IMAGE SENSOR by Michael Guidash filed on the same day as the instant application, and an application entitled METHOD OF FORMING A SEMICONDUCTOR IMAGE SENSOR AND STRUCTURE by Drowley et al and filed concurrently herewith.

This invention relates, in general, to semiconductor devices, and more particularly to a semiconductor image sensor.

In the past, a variety of methods were used to form semiconductor image sensors on a substrate with complementary metal oxide semiconductor (CMOS) devices. Typically, the optical receiving portion of the sensor is formed either as a gate of a large area transistor, often referred to as a photo-gate, or as a source-drain junction of a metal oxide semiconductor (MOS) transistor. The photo-gate transistor implementation requires that light travel through the silicon gate of the transistor in order to convert light to electrical energy. Consequently, the photo-gate implementation has reduced sensitivity. Additionally, the depletion region generally is shallow (less than one micron) thereby reducing the collection efficiency of carriers induced by red light absorption. Also conventional photo-gate implementations are susceptible to noise created by surface recombination.

The source-drain junction implementation generally has a junction that is optimized for transistor operation and therefor also has a shallow junction that results in inefficient collection of carriers induced by red light. Another disadvantage of the source-drain junction implementation is that the junction typically is formed in a highly doped (greater than 10^{16} atoms/cm^3) region that limits the width of the junction depletion region thereby further reducing the collection efficiency of carriers induced by red light absorption. Furthermore, forming the junction in such a highly doped region results in a large capacitance that reduces the amount of charge that can be transferred from the photo sensing element to other electronics.

Traditional CMOS image sensor implementations often form a silicide layer over the image sensing element thereby further reducing sensitivity.

Accordingly, it is desirable to have an image sensor that does not utilize a photo-gate thereby resulting in higher efficiency, that does not have a shallow junction depth thereby increasing efficiency, that minimizes noise from surface recombination, that does not use a silicide overlying the light sensing area thereby further increasing efficiency, that has a wide depletion region for further increasing of carrier conversion for all wavelengths of light, and that does not have a large capacitance that minimizes the charge transferred from the image sensing element to other electronics.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates an enlarged cross-sectional portion of an image sensor embodiment in accordance with the present invention;

FIG. **2** illustrates an enlarged cross-sectional portion of the FIG. **1** embodiment at a manufacturing stage in accordance with the present invention;

FIGS. **3**–**7** illustrate enlarged cross-sectional portions of the FIG. **1** embodiment at a subsequent manufacturing stages in accordance with the present invention; and

FIG. **8** illustrates an enlarged cross-sectional portion of an alternate embodiment of an image sensor in accordance with the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates an enlarged cross-sectional portion of a semiconductor image sensor **10**. Sensor **10** includes an underlying P-type substrate formed by a semiconductor substrate **11** and an enhancement layer **12** formed thereon. Sensor **10** has a first well or P-type well **16** formed in a first portion **13** of the underlying substrate. Well **16** typically has a doping concentration that is higher than the doping concentration in a second portion **14** of the underlying substrate's layer **12**. Portions **13** and **14** of layer **12** are identified by a brackets shown below layer **12**. This second portion of layer **12** forms a second well within the underlying substrate. The surface doping concentration of well **16** typically is at least 1×10^{16} atoms/cm^3. A first depth or depth **24** of well **16** typically is less than the depth of layer **12** and typically is about two to four microns in order to facilitate forming other CMOS devices on substrate **11**.

The image capturing or light sensing element of sensor **10** includes an N-type conducting region **26** that is formed in the second well or second portion **14**. Conducting region **26** forms a first P-N junction with the P-type material of the underlying substrate. This first P-N junction is positioned at a second depth or depth **29** of conducting region **26** in order to readily sense light in the red wavelengths and typically is less than approximately 0.7 microns, and preferably about 0.5 microns, from the surface of the underlying substrate. A P-type pinning layer **37** is formed within region **26** and extends outward from region **26** into layer **12** of the underlying substrate in order to form an electrical connection with the underlying substrate. This electrical connection pins the potential applied to this element of the image sensor. Consequently, the resulting photodiode is often referred to as a pinned photodiode. A second P-N junction is formed along the intersection of layer **37** and region **26**. Typically layer **37** is formed simultaneously with the formation of lightly doped drain and source regions of other P-channel MOS transistors (not shown) on substrate **11**. The depth of the second P-N junction is less than that of the first P-N junction. This depth is selected to optimize the absorption or sensing of light in the blue wavelengths. A transfer transistor or first MOS transistor **32** is formed adjacent to conducting region **26** so that a portion of region **26** forms a source of transistor **32**. A second or reset MOS transistor **31** is formed within well **16**. Transistor **31** has a source that is electrically coupled to transistor **32** by a coupling region **41**.

Conducting region **26** is formed by applying a mask having an opening that exposes some of the surface of portion **14** extending up to and including a portion of a gate **22** of transistor **32**. Then dopants are implanted at an angle away from perpendicular to substrate **11** and toward gate **22** to ensure that region **26** extends under gate **22**, thereby saving masking and other processing operations in forming region **26** and the source of transistor **32**.

FIG. **2** illustrates an enlarged cross-sectional portion of a stage in an embodiment of manufacturing sensor **10** shown in FIG. **1**. Sensor **10** includes a heavily doped P-type substrate **11** having a lightly doped P-type enhancement layer **12** formed thereon. Typically, substrate **11** has a first or P-type doping concentration of at least 1×10^{16}, and preferably 1×10^{18}, atoms/cm^3 and layer **12** has a P-type doping concentration no greater than approximately 1×10^{15} atoms/cm^3. Additionally, layer **12** includes first portion **13** in which

first well or P-well **16** is formed, and second well or second portion **14** in which the light sensing element of sensor **10** will be formed. Forming the light sensing elements in lightly doped second portion **14** that overlies more heavily doped substrate **11** enhances carrier collection in the light sensing element.

P-type well **16** is formed by applying a mask **17** to expose the surface of first portion **13** of layer **12**. Dopants are formed within the exposed surface to form well **16**. After forming well **16**, mask **17** is removed.

FIG. **3** illustrates an enlarged cross-sectional portion of sensor **10** shown in FIGS. **1** and **2** at a subsequent formation stage. Like elements in FIGS. **1**, **2**, and **3** have the same element numbers. A gate oxide **18** is formed across the surface of sensor **10**. Thereafter, a channel doping region **19** is formed to facilitate creating channels for MOS transistors **31** and **32**. Gates **23** and **22** are formed on oxide **18** to facilitate the formation of transistors **31** and **32**, respectively.

Thereafter, a mask **21** is applied to expose the area of second portion **14** in which conducting region **26** is to be formed. Mask **21** has an opening that exposes a portion of the surface of gate oxide **18** in second portion **14** the exposed portion extends from an edge of gate **22** into second portion **14**, and also exposes a portion of gate **22**. Dopants, illustrated by arrows **27**, are implanted at an angle **28** toward gate **22**. Angle **28** is measured away from a line normal to the surface of sensor **10**. Angle **28** typically is greater than fifteen degrees, and preferably is at least twenty five degrees, from normal to the surface of sensor **10**. This angle implant is used to ensure that region **26** extends slightly under gate **22** to facilitate utilizing a portion of region **26** to function as the source of transistor **32**, thereby connecting the channel of transistor **32** to conducting region **26**. Subsequent to forming region **26**, mask **21** is removed.

Alternately, two different implants can be utilized to form region **26**. A high energy implant, for example 120–190 keV, can be used near normal to the surface of sensor **10** in order to form region **26** deep within layer **12**. Thereafter a lower energy implant, for example 90–130 keV, can be formed at an angle substantially equal to angle **28** and at a low energy to ensure that a portion of region **26** extends under gate **22**.

FIG. **4** represents a subsequent stage in the formation of sensor **10**. Similar elements in FIGS. **1**, **2**, **3**, and **4** are represented by the same element numbers. A mask **34** is applied with an opening that exposes the areas for forming the drain of transistor **32**, and the source and drain of transistor **31**. Thereafter, source-drain dopants **33** are formed in layer **12** using the edges of gates **22** and **23** as masks to self-align the source and drain areas to gates **22** and **23**. Thereafter, mask **34** is removed.

FIG. **5** illustrates an enlarged cross-sectional portion of a subsequent stage in forming sensor **10**. Similar elements in FIGS. **1**, **2**, **3**, **4**, and **5** are represented by the same element numbers. A mask **36** is applied having an opening that exposes an edge of gate **22**, the surface of conducting region **26**, and an area **56**, shown by an arrow, extending past region **26**. P-type dopants are formed in the exposed surface to form P-type pinning layer **37** within the exposed portion of region **26** and extending outward from region **26** into area **56** and away from transistor **32**. The depth and doping concentration of layer **37** are chosen to facilitate transferring all photo induced charge from region **26** to the drain of transistor **32**. Typically, layer **37** has a depth of approximately 0.2 to 0.3 microns and a surface doping concentration greater than approximately 5×10^{17} atoms/cm^3. Subsequent to forming layer **37**, mask **36** is removed.

FIG. **6** illustrates a subsequent stage in the formation of sensor **10**. Similar elements in FIGS. **1**, **2**, **3**, **4**, **5**, and **6** are represented by the same element numbers. A dielectric material is applied to the surface of sensor **10** and is patterned to form spacers **39** on the sidewalls of gates **22** and **23**, and to form a dielectric covering **38** overlying the light sensing element of sensor **10**. Covering **38** typically extends onto gate **22** to form a mask for subsequent operations. The material used to form spacers **39** and covering **38** is chosen to have a dielectric constant between the dielectric constant of the underlying substrate and any material overlying covering **38**. The dielectric constant of covering **38** chosen in order to minimize reflections between the underlying semiconductor material and any other dielectric or material placed on top of covering **38**. For example, the material of covering **38** can be silicon nitride having a thickness of thirty to seventy nanometers in order to minimize reflections for light between the blue and red spectrums. Additionally, thickness of one hundred thirty to two hundred nanometers will also perform properly. Other materials such as aluminum oxide and aluminum nitride are also believed to be suitable materials for forming covering **38** and spacers **39**.

Subsequently, spacers **39** and covering **38** are used as masks to form N-type dopants in layer **12** that result in forming coupling region **41** electrically connecting drain **42** and source **43**.

FIG. **7** illustrates a subsequent stage in the formation of sensor **10**. Similar elements in FIGS. **1**–**7** are represented by the same element numbers. A low resistance material is applied to minimize the resistance of contacts made to both coupling region **41** and gates **22** and **23**. Typically, titanium is blanket deposited across sensor **10** and then annealed to form titanium silicide with any exposed underlying silicon material. Consequently, layer **38** prevents forming a silicide overlying the photo-diode formed by region **26** and layer **37**. The remaining titanium that does not form titanium silicide is removed thereby leaving low resistance contact materials **44** on gates **22**, **23**, and coupling region **41**. Such formation techniques are well known to those skilled in the art. Generally, an interlayer dielectric, not shown, is formed over sensor **10** and contacts made to appropriate portions thereof.

FIG. **8** illustrates an alternate embodiment for forming pinned layer **37** of sensor **10**. Subsequent to forming conducting region **26** as discussed in FIG. **3**, layer **37** can be formed by performing an implant at an angle opposite to angle **28** shown in FIG. **3**. In this embodiment, dopants, represented by arrows **47**, are implanted away from gate **22** at an angle **48** from normal to the surface of sensor **10**. Typically, angle **48** is between ten and twenty five degrees to ensure that a portion of layer **37** extends outward from region **26** away from transistor **32**. This portion of layer **37** is utilized to form contact with enhancement layer **12**. For some processing sequences, this alternate embodiment can reduce the number of processing operations.

By now it should be appreciated that there has been provided a novel image sensor and method therefor. Forming the image sensor in a lightly doped region that overlies a more heavily doped region enhances carrier collection. Forming a deep conducting region and a shallower pinned layer forms two P-N junctions where one P-N junction, and the associated depletion region, is deep to facilitate capturing light in the red wavelengths and a second P-N junction, and the associated depletion region, is shallow facilitating capturing blue wavelength light. This structure also minimizes surface recombination and maximizes charge transfer. Using an angled implant to form the conducting region ensures the conducting region can be used as a source of a

charge transfer transistor thereby minimizing manufacturing operations. Utilizing a dielectric material having a dielectric constant between the dielectric constant of the underlying substrate and overlying material minimizes reflections and enhances efficiency of the sensor. Ensuring that the light sensing element is devoid of an overlying silicide material also improves the efficiency of the sensor.

We claim:

1. An image sensor comprising:

a substrate of a first conductivity type having a first doping concentration;

an enhancement layer of the first conductivity type having a second doping concentration lower than the first doping concentration, the enhancement layer on the substrate;

a first MOS transistor on the enhancement layer;

a first well on the enhancement layer, the first well having the first conductivity type and a third doping concentration that is less than the first doping concentration and greater than the second doping concentration wherein the first MOS transistor is outside the first well; and

a pinned photodiode on the enhancement layer wherein a portion of the pinned photodiode forms a source of the first MOS transistor.

2. The image sensor of claim **1** further including a second MOS transistor within the first well.

3. An image sensor comprising:

a substrate;

a pinned photodiode on the substrate;

a dielectric layer overlying the pinned photodiode; and

a silicide layer on a portion of the image sensor wherein an area overlying the pinned photodiode is devoid of the silicide layer.

4. The sensor of claim **3** wherein the silicide layer on the portion of the image sensor includes the silicide layer on a gate of a MOS transistor.

* * * * *

EXHIBIT C

United States Patent [19]

[11] **Patent Number: 6,121,960**

[45] **Date of Patent: Sep. 19, 2000**

Carroll et al.

[54] **TOUCH SCREEN SYSTEMS AND METHODS**

[75] Inventors: **David W. Carroll**; **James L. Carroll**; **Steven V. Case**, all of Northfield, Minn.

[73] Assignee: **ViA, Inc.**, Burnsville, Minn.

[21] Appl. No.: **08/919,527**

[22] Filed: **Aug. 28, 1997**

Related U.S. Application Data

[60] Provisional application No. 60/024,780, Aug. 28, 1996, provisional application No. 60/028,028, Oct. 9, 1996, and provisional application No. 60/036,195, Jan. 21, 1997.

[51] **Int. Cl.**[7] **G09G 5/00**

[52] **U.S. Cl.** **345/173**; 345/172; 345/169

[58] **Field of Search** 345/173, 172, 345/168, 169, 429, 113; 361/683

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[57] **ABSTRACT**

A screen peripheral system according to an embodiment of the invention includes a computing device for producing a main image and a touch-activated input device for generating and displaying a composite image visible to a user. The composite image simultaneously includes a representation of at least one key, for example a QWERTY keyboard, for activating an input function, and the main image provided by the computing device. The keyboard representation preferably is laid over the main image. According to one embodiment, the main image is an output image generated by an application being executed by the computing device. Other touch screen systems and methods are also disclosed.

30 Claims, 9 Drawing Sheets

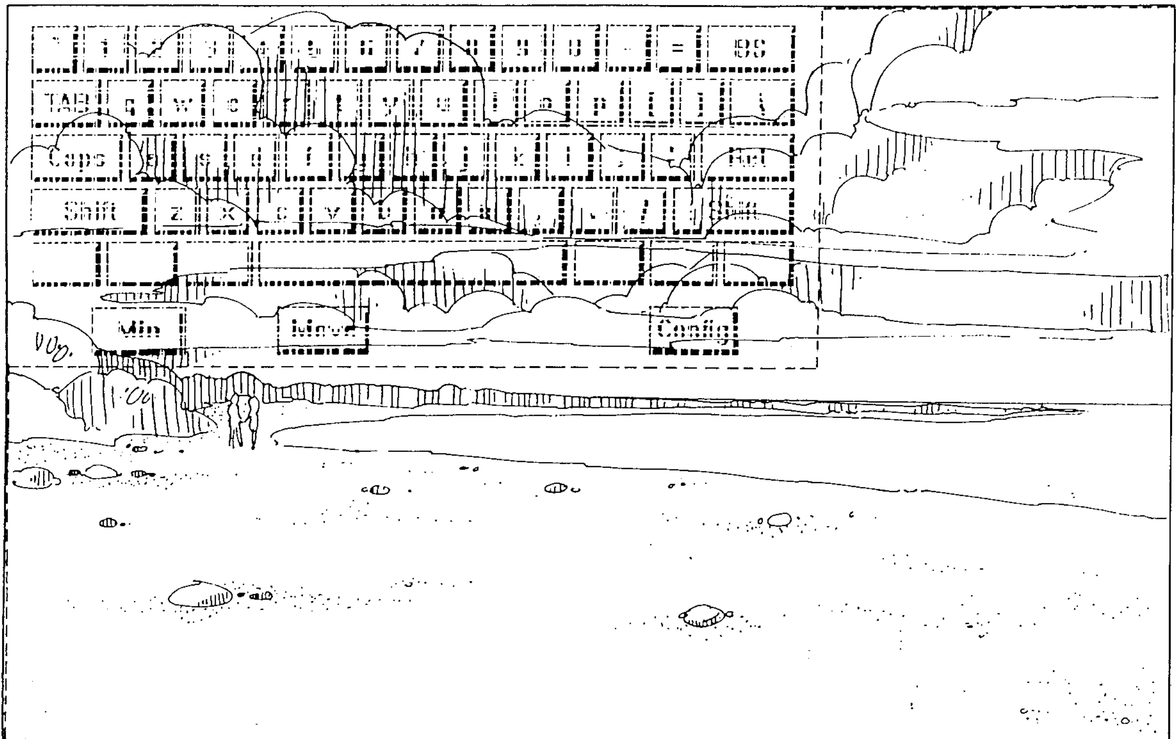


FIG. 1

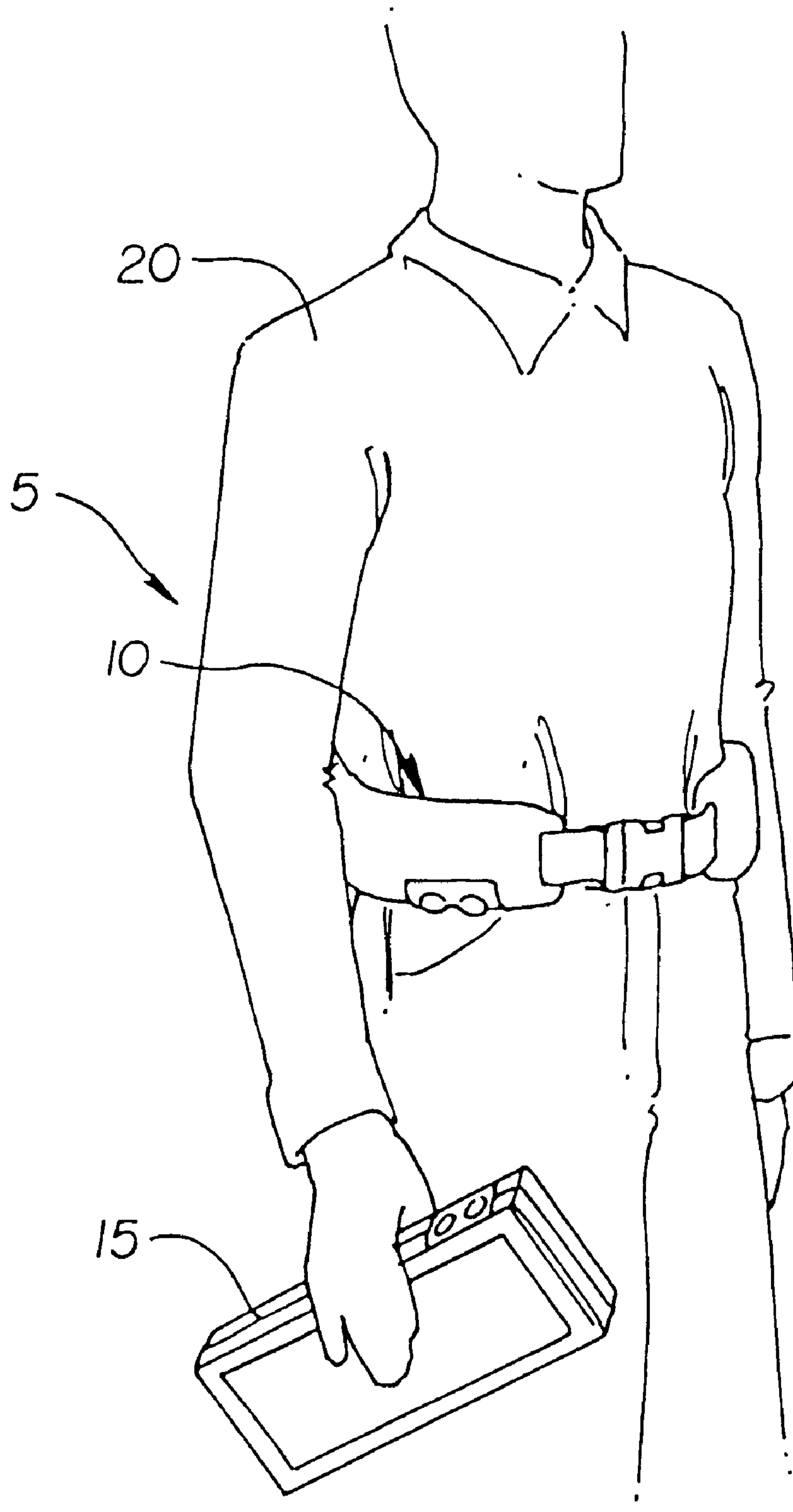
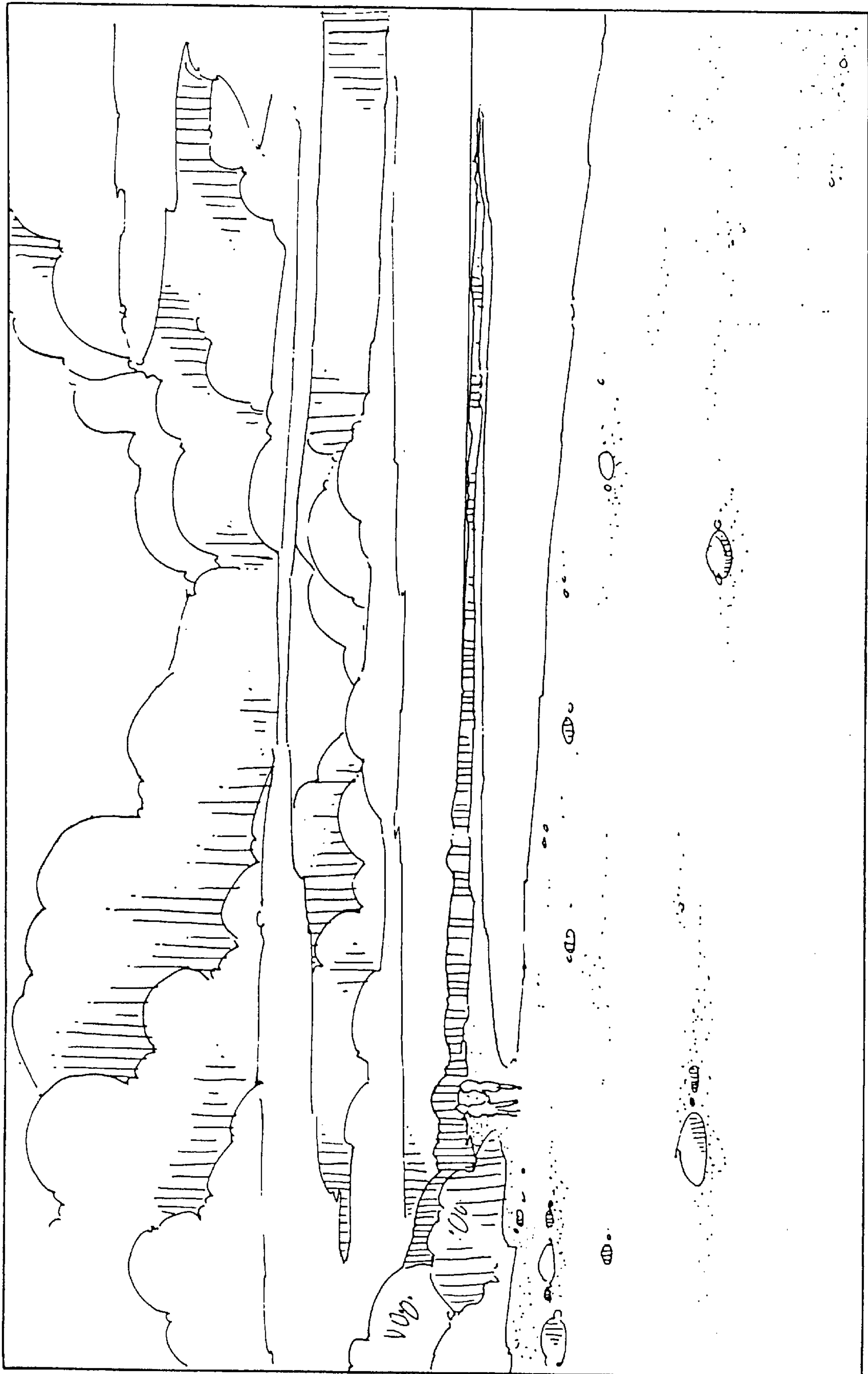


FIG. 2

FIG. 3



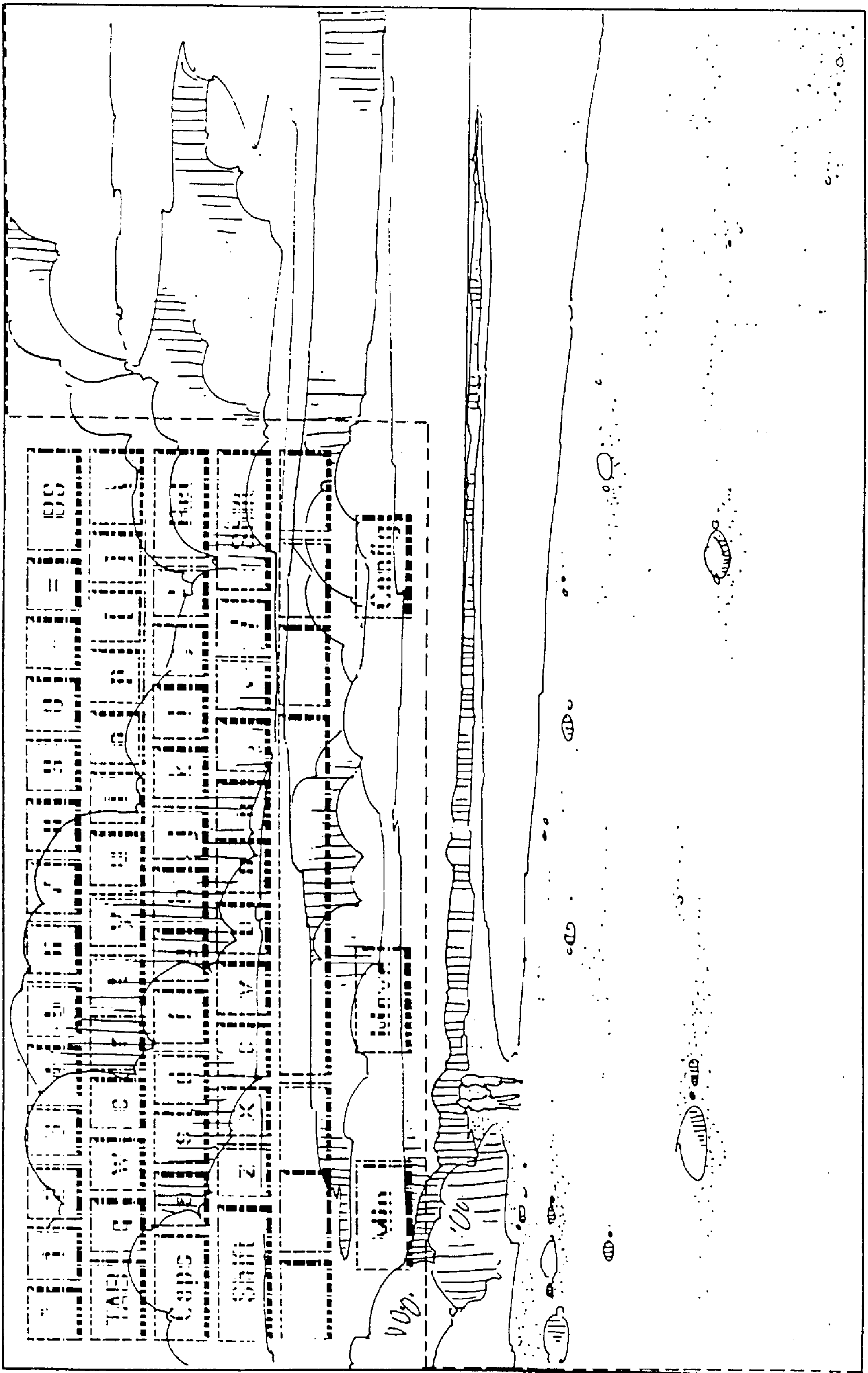
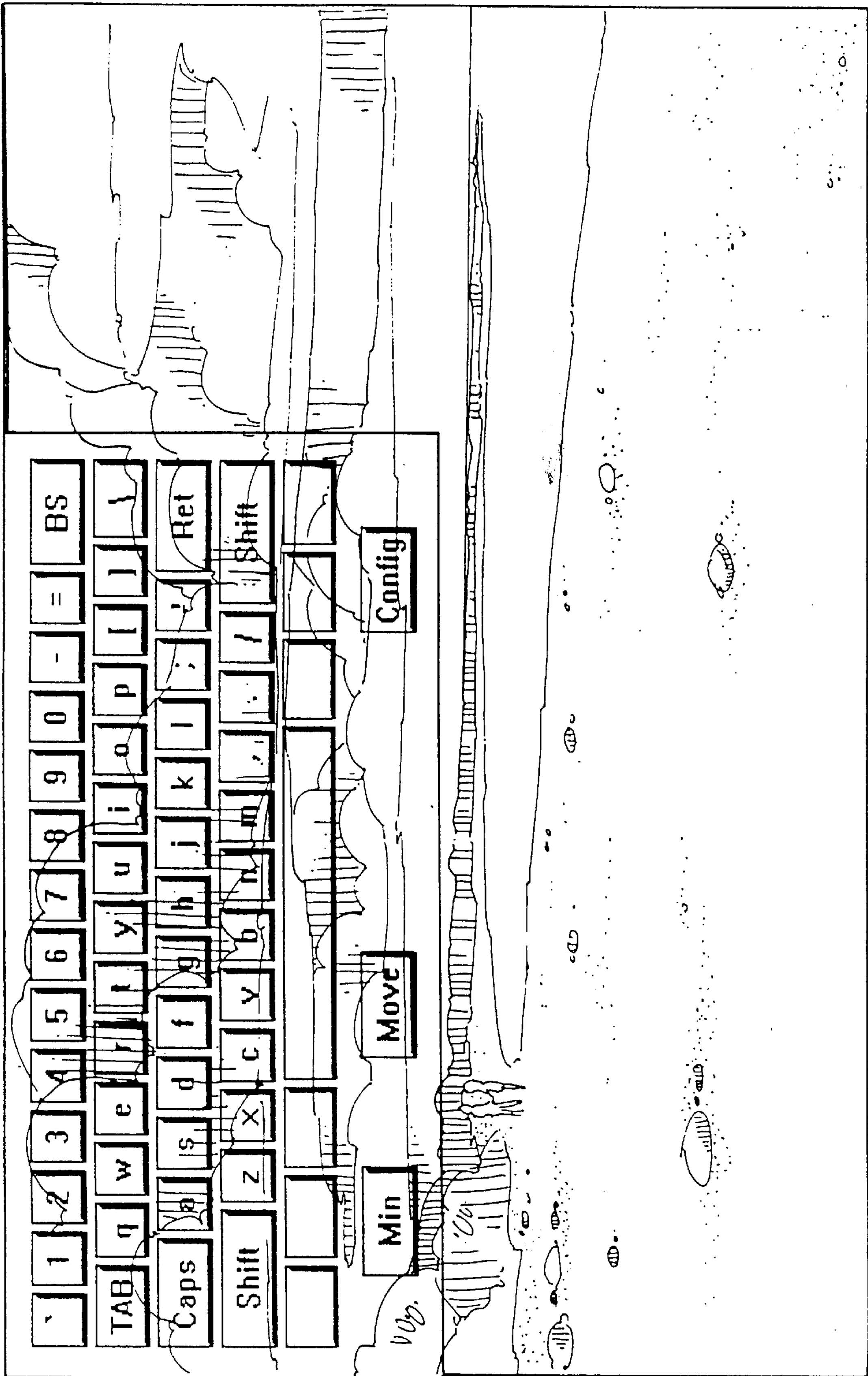


FIG. 4

FIG. 5



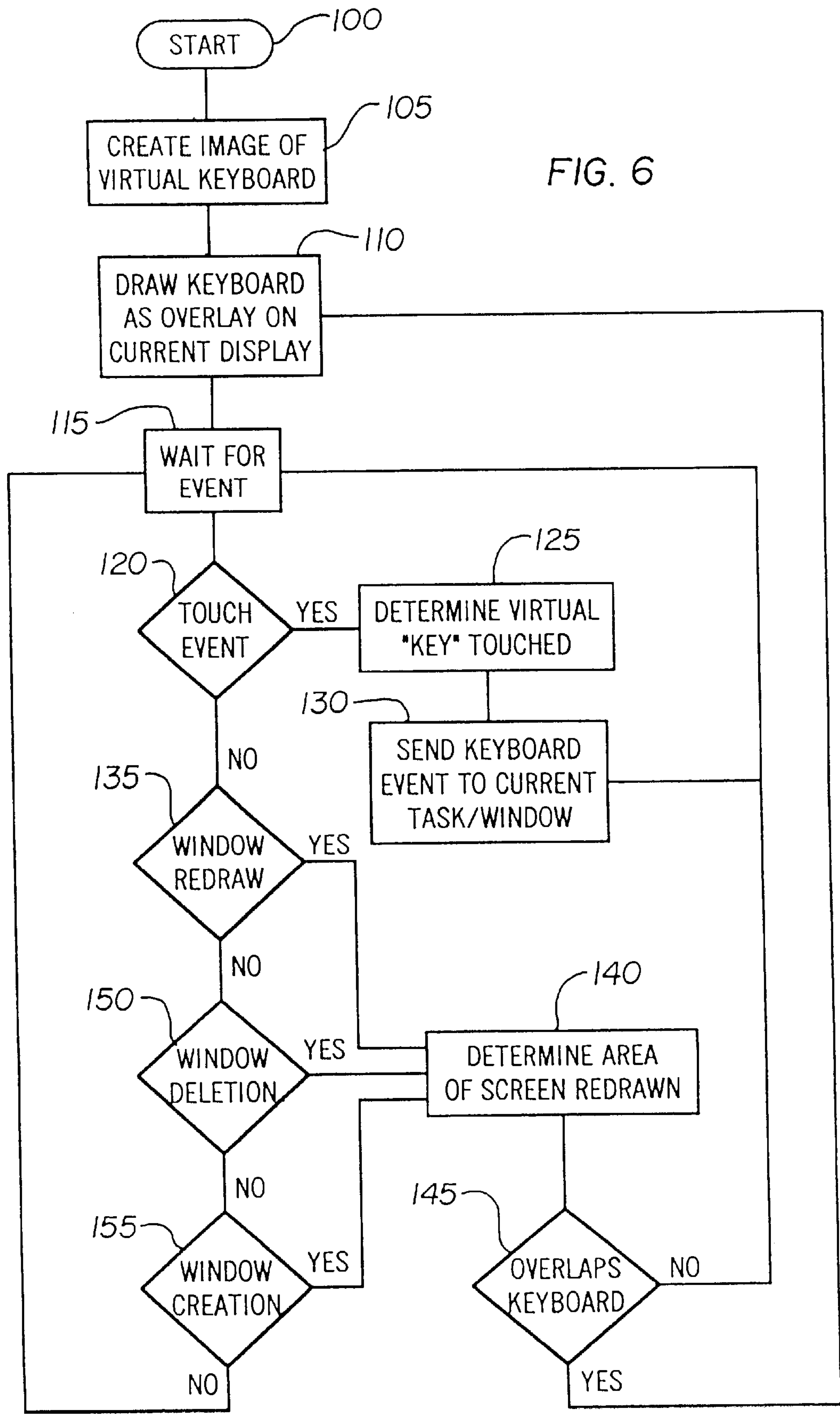


FIG. 6

FIG. 7

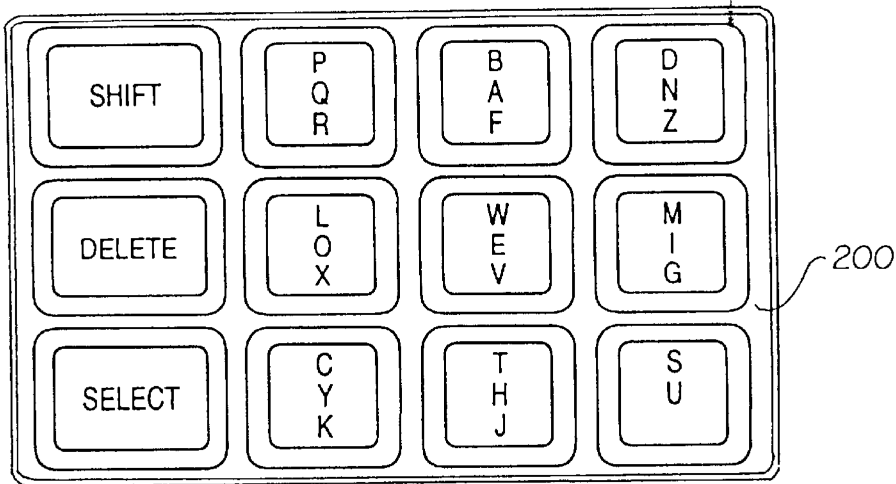


FIG. 8

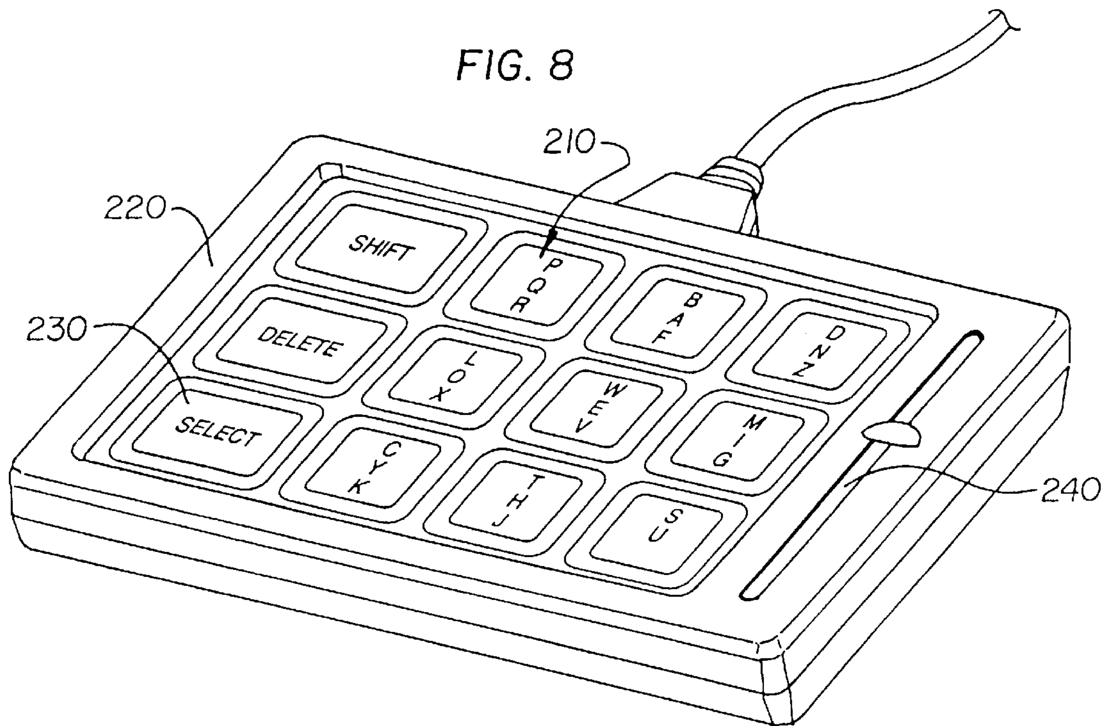


FIG. 9

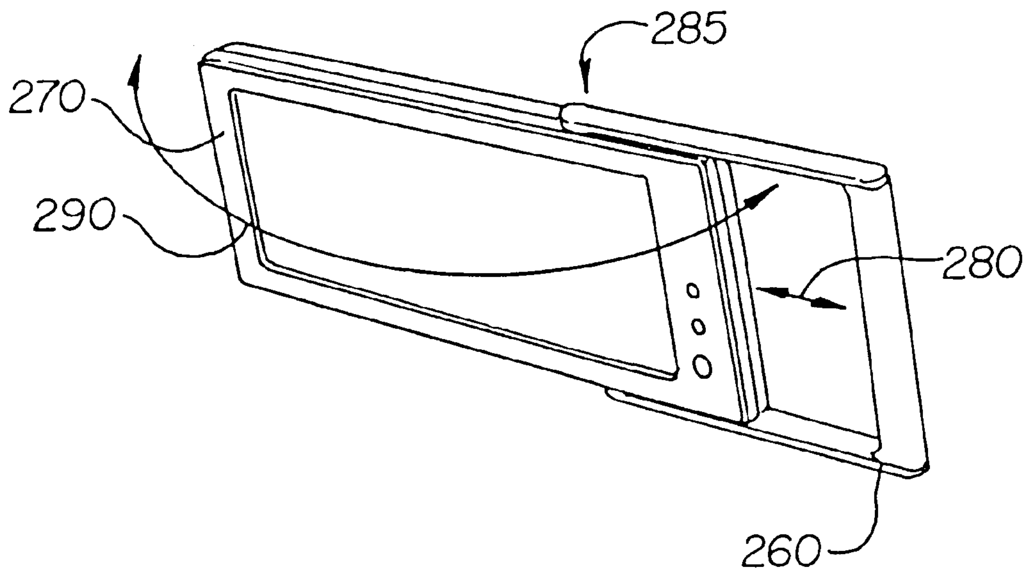


FIG. 10

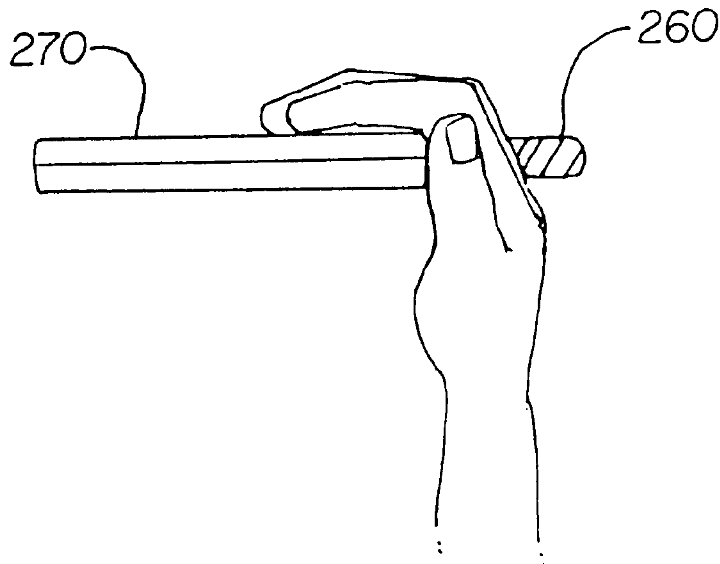


FIG. 11

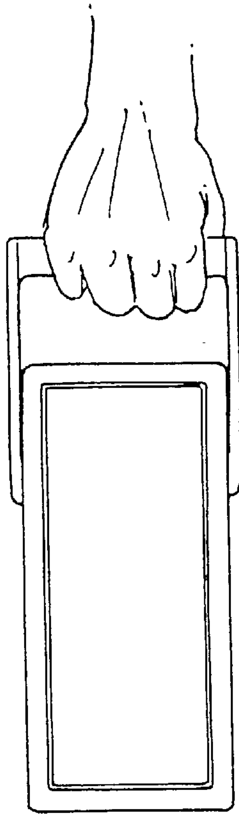


FIG. 12

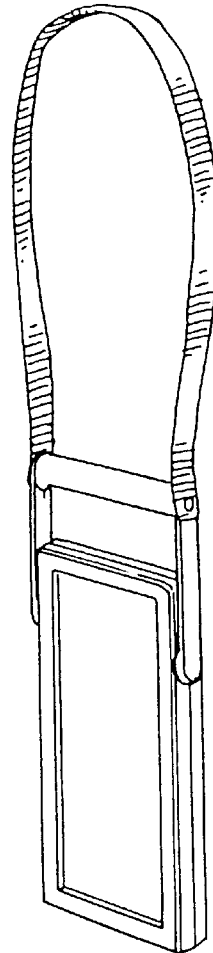
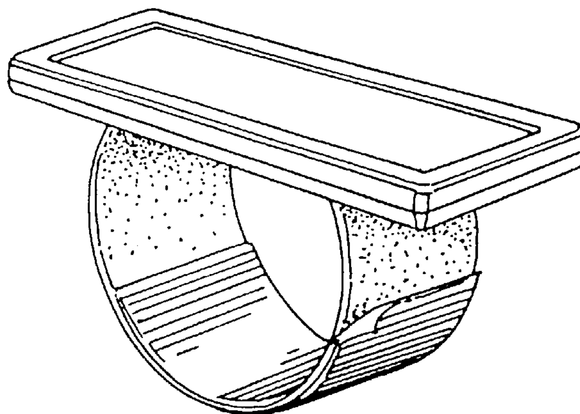


FIG. 13



TOUCH SCREEN SYSTEMS AND METHODS

CROSS-REFERENCE TO RELATED APPLICATIONS

The subject matter of this application is related to the subject matter of commonly assigned U.S. Provisional Applications Ser. No. 60/024,780, filed Aug. 28, 1996, Ser. No. 60/028,028, filed Oct. 9, 1996, and Ser. No. 60/036,195, filed Jan. 21, 1997, all of which provisional applications are incorporated by reference herein and priority to which is claimed under 35 U.S.C. §119(e).

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to touch-sensitive input and output devices, and more particularly, to touch screens that simultaneously can display a keyboard-type image superimposed on a background image. The invention also relates to other features of touch-sensitive i/o devices. Embodiments of the invention have particular application to wearable-computing devices and environments, although non-wearable embodiments are also contemplated.

2. Description of Related Art

It is known in the art to superimpose a keyboard over an image that is output by an application being executed on a computer, i.e. to form a "phantom" keyboard, on a touch-sensitive input display device. U.S. Pat. No. 5,581,243 to Ouellette et al., for example, which is incorporated by reference herein in its entirety, describes a system for displaying a simulated keyboard on a touch-sensitive display, without occluding from view an underlying application output image. An output image is generated and displayed for a first period of time at a first luminous radiation intensity having a predetermined persistence. A simulated keyboard image is generated and displayed for a second, shorter period of time at a second, lower luminous radiation intensity having the predetermined persistence. The keyboard and output images are generated in alternation, and the amount of time each is displayed is controlled, to try to create the illusion that both images are being displayed continuously.

The system described in Ouellette et al., however, is believed to suffer a number of disadvantages. First, it is believed that flashing between application and keyboard screens, as the reference discloses, would significantly reduce the refresh rate achievable relative to a continuously displayed application output (or a keyboard) image. This reduction could cause considerable detriment to the viewer and potentially could confuse the displayed interpretive features. Second, it is believed that displaying the keyboard and the application output in alternation requires additional hardware features for proper functioning, for example a second frame buffer for switching back and forth between the screens. Additionally, although this feature is not disclosed or apparently contemplated in Ouellette, using the Ouellette device in a wireless-transmission (e.g. RF) environment, for example in a wearable-computing context, would require e.g. twice as much information to wirelessly be transmitted and therefore would greatly increase the required bandwidth.

SUMMARY OF THE INVENTION

To overcome the above and other disadvantages, a screen peripheral system according to an embodiment of the invention includes a computing device for producing a main

image and a touch-activated input device for generating and displaying a composite image visible to a user. The composite image simultaneously includes a representation of at least one key, for example a QWERTY keyboard, for activating an input function, and the main image provided by the computing device. The keyboard representation preferably is laid over the main image.

The system implements variable-pixel control to form the keyboard representation and to form the main image, causing the pixels selected to form the keyboard representation and selected to form the main image to be dependent on each other. In other words, the keyboard-representation pixels are not independent of the main-image pixels. According to one embodiment, the main image is an output image generated by an application being executed by the computing device.

Various image-adjustment, mode-switching, zoom-up/zoom-down and other embodiments associated with invention are also described, as are corresponding methods.

Embodiments of the invention have particular application to wearable computing devices, such as those available from ViA, Inc., Northfield, Minn. Attention also is directed to the following U.S. patents, each of which is incorporated by reference herein: U.S. Pat. Nos. 5,581,492; 5,572,401; 5,555,490; 5,491,651 and 5,285,398, all of which are owned by ViA, Inc.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will be described with respect to the figures, in which like reference numerals denote like elements, and in which:

FIG. **1** is a perspective view of a wearable computing environment according to an embodiment of the invention;

FIG. **2** shows a keyboard representation according to an embodiment of the invention;

FIG. **3** shows a main image according to an embodiment of the invention;

FIG. **4** shows a composite image according to an embodiment of the invention;

FIG. **5** shows a second composite image according to an embodiment of the invention;

FIG. **6** is a flow chart showing operational steps according to an embodiment of the invention;

FIG. **7** shows a reduced-key keyboard;

FIG. **8** shows a touch screen according to an embodiment of the invention; and

FIGS. **9–13** show touch screens having a handle, according to embodiments of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Embodiments of the invention have wide application in a number of computing environments. The invention is particularly applicable to wearable computing environments, as discussed above, in which portability and compactness are fundamental considerations. The invention is also applicable to a number of different input/output devices. For example, embodiments of the invention contemplate i/o devices with full, partial, reduced-key, alphanumeric or non-alphanumeric keyboards comprising one or more "keys," "buttons," "contact zones" or the like. The invention also contemplates a number of input schemes in which a user manually or audibly directs certain keys to be activated, not just screens requiring direct manual contact with e.g. a user's finger. Proximity-based, pen-based and voice-based

inputs are among the functionalities encompassed by embodiments of the invention. In fact, any display with any "pointing" device, i.e. a device that designates a particular point or zone on the display, is contemplated for use with embodiments of the invention. Therefore, although particular embodiments will be described with respect to touch screens, keyboards and touch input, the invention is intended to be broadly interpreted as needed and not necessarily limited to those particular embodiments.

Additionally, various images can be combined/superimposed according to embodiments of the invention. In primary embodiments, the superimposed image is that of at least one key, e.g. a keyboard. The background image is that output by an application executed by a computing device, for example a graphics, spreadsheet, word-processing, etc. application for use in private, commercial, military, public-service fields or other fields. However, either the background image or the superimposed image can be of other types; for example the background image, or both images, can be provided by a processor or storage device associated with the system, instead of by an application program per se. Either or both image can be the subject of an enlargement or reduction process, to provide composite images having elements of different sizes. More than two images can be combined according to the invention as well; any combination of application, keyboard, or other images can be combined in a composite image. Therefore, although particular embodiments will be described herein with reference to application-output images, keyboards, etc., the invention is intended to be broadly interpreted as needed and not necessarily limited to those particular embodiments.

Touch screen keyboard overlays according to embodiments of the invention can be selectively turned on and off by a user of an associated personal computing device, for example a wearable personal computer. A representation of a keyboard, as will be described, lies over a main image on the touch screen, the main image preferably being formed in connection with a main software application. A keyboard overlay according to the invention eliminates a physical keyboard or the necessity of having a split screen with a touch keyboard on a lower portion and a main screen squeezed into the remaining upper portion, for example. A keyboard overlay according to the invention also reduces and/or eliminates the space-conflict problems that can arise when a superimposed keyboard occupies the same portion of the display screen as a critical portion of the application output image.

Keyboard overlays according to the invention are especially advantageous for very small screens, because of the relatively large and accessible overlay "buttons" (keys) that are provided, along with the ability to see all of the data behind the keyboard at the same time.

Embodiments of the invention are especially advantageous in situations where voice-based input is undesirable. Although voice-recognition technology is making significant advances, it still requires verbal input, which can be disruptive to a meeting, for example. Verbal input also potentially announces to all within earshot of the speaker the exact notes, etc. that are being entered. According to embodiments of the invention, therefore, the user inputs directly to the machine in complete silence. Still, voice-based input may be desirable in many cases, so optional switching between voice input and keyboard-overlay input is also contemplated. This can be activated by a physical button or key on the side or other surface of the touchscreen or associated device, or by a virtual button or key on the touch-sensitive portion of the screen itself, or by voice.

Keyboard overlays according to embodiments of the invention can take a number of forms. For example, a solid-line or dashed/dotted-line overlay is contemplated, providing outlines of each key. Alternatively, and selectively as chosen by a user, each key can be represented by a dot, or as a letter-area zone between intervening markers such as x's, dots, etc. Ideally, the representation of the keyboard is provided faintly on the standard screen, so that it and data/images from the main program can be seen simultaneously. Variable-pixel controls, described in more detail below, can be provided to change the thickness, brightness, and/or dotted-ness of the keyboard representation. In many cases the keyboard overlay can be extremely faint. Additionally, a color difference can be imparted to the pixels of either the keyboard overlay or the underlying image, or both, to highlight the difference between the two.

The characters of the keyboard themselves, e.g. the letters associated with each key or zone, can be turned off if the user has memorized the keyboard layout, for example. The keyboard can be active without being visible at all, for the user who can type effectively without even seeing representations of the keys/zones themselves.

Contrast adjustment buttons are contemplated, preferably represented on the touch screen itself but possibly on a housing of the touch screen, to adjust contrast between the keyboard and the main screen. A keyboard on-off button is also contemplated. Alternatively, these features can be controlled by voice.

Variable-pixel controls

In accordance with embodiments of the invention, software-based variable-pixel controls are provided to determine and control which pixels of the touch screen will be used for displaying the keyboard representation and which pixels for displaying the main image. In some cases, each pixel of the screen is 100% dedicated to either the keyboard or the main image. In other cases, touch screen pixels may be dedicated to both the keyboard and the main image, producing a "blended" effect as will be described.

Merging the image of the virtual keyboard with the normal output image on the display according to the invention can occur by a variety of methods and programming schemes. Using most current video graphics controllers, however, it is believed a highly efficient method available to perform the merging of images is to use bit-block or bit-block-type transfer operations, i.e. BitBlt operations.

BitBlt operations provide an efficient method of performing logical combination of up to three sets of pixels on raster-based display devices. According to embodiments of the invention, BitBlt operations are used with the following three sets of pixels:

(1) The original pixels on the display, i.e. the image that would be presented in the absence of the virtual keyboard.

(2) The pixels representing the image of the virtual keyboard.

(3) An image mask, allowing control of which pixels within the virtual keyboard will be merged with the original display pixels.

Using BitBlt operations, the virtual keyboard can be combined with the display using a variety of effects. The following table summarizes the typical operations that can be performed:

Source (S)	1 1 0 0 1 1 0 0		
Destination (D)	1 0 1 0 1 0 1 0	Boolean	
Mask (M)	1 1 1 1 0 0 0 0	Operation	Operation
Result	0 0 0 0 0 0 0 0	0	Blackness
	0 0 0 1 0 0 0 1	~(S|D)	Not source erase
	0 0 1 1 0 0 1 1	~S	Not source copy
	0 1 0 0 0 1 0 0	S & ~D	Source erase
	0 1 0 1 0 1 0 1	~D	Destination invert
	0 1 0 1 1 0 1 0	M ^ D	Mask invert
	0 1 1 0 0 1 1 0	S ^ D	Source invert
	1 0 0 0 1 0 0 0	S & D	Source and
	1 0 1 1 1 0 1 1	~S|D	Merge paint
	1 1 0 0 0 0 0 0	M & S	Merge copy
	1 1 0 0 1 1 0 0	S	Source copy
	1 1 1 0 1 1 1 0	S|D	Source paint
	1 1 1 1 0 0 0 0	M	Mask copy
	1 1 1 1 1 0 1 1	M|~S|D	Mask paint
	1 1 1 1 1 1 1 1	1	Whiteness

Additionally, those of skill in the art upon reading this disclosure will comprehend that similar logic functions can be applied to the color-differentiation capability described earlier; such functions are not limited to black/white/grey capabilities.

The logical operations described herein each preferably have a different blending or merging effect. Although some of them do not have substantive effect, e.g. they just copy the source in to the destination or just fill it with zeros or ones and are ignorant of what the source and destination have, the large majority of these operations can be used to create a number of different effects to determine how to mesh the keyboard image and the application output image together. Additionally, the various logical operations can be combined as needed to produce an even greater variety of visual effects, e.g. harshness/intensity of one image with respect to the other.

Two examples of the myriad of meshing possibilities contemplated according to the invention will now be described. In the first example, the keyboard is blended with the original display application-output image by using 25% of the pixels to represent the keyboard and 75% of the pixels to represent the original display image. In the second example, the two images are more truly blended together, with each pixel of the final composite display image receiving a contribution from both images. For the second example, the composite realized image can appear as e.g. a blended shadow from the original images. For both examples, it is assumed according to one embodiment that the graphics controller of the computer system is using an 8-bit bit plane, which is typical of most personal computers supporting 256 colors per pixel. Of course, those of ordinary skill will readily be able to adapt these examples for use in other current and future graphics controllers, bit planes, etc.

In the first example, where the keyboard is blended with the display by using 25% of the pixels to represent the keyboard and 75% of the pixels to represent the original display image, each display update preferably is performed in three steps. The first step removes that portion of the keyboard image that is not to be seen, i.e. it eliminates 75% of the keyboard image. The second step removes that portion of the main display image that is not to be seen, i.e. it eliminates 25% of the main display image. The third step merges these two images. The following pseudocode represents one embodiment of the associated processing used according to this example:

```
reduced_kbd := BitBlt        (source       => keyboard image,
                              destination  => keyboard image,
                              mask         => [0xFF, 0x00, 0x00, 0x00,
                                               0xFF, 0x00, 0x00, 0x00,
                                               . . . ],
                              operation    => merge copy);
reduced_display := BitBlt    (source       => original display image,
                              destination  => original display image,
                              mask         => [0x00, 0xFF, 0xFF, 0xFF,
                                               0x00, 0xFF, 0xFF, 0xFF,
                                               . . . ],
                              operation    => merge copy);
display := BitBlt            (source       => reduced_kbd,
                              destination  => reduced_display,
                              mask         => null,
                              operation    => source paint);
```

With the first example, for performance reasons the first BitBlt can be performed once at initialization and then stored for reuse in future display updates. Essentially, the process eliminates from the two images those pixels that are not desired for the single, final composite image that is displayed to the user. In this way, neither image contains overlapping pixels. In the combined image, therefore, each pixel is contributed 100% by either the keyboard or the display, but 0% from the alternate.

With the second example, the two images are logically combined using a single BitBlt, according to one embodiment. The following pseudocode represents one embodiment of the associated processing used according to this example:

```
display := BitBlt    (source       => keyboard image,
                      destination  => original display image,
                      mask         => null,
                      operation    => source paint);
```

Current embodiments of the invention employ the following assumptions for performance reasons. It is contemplated that embodiments of the invention are for typically available operating systems, ones that support multi-tasking, with each application having its own thread of control, and a graphical user interface using windows as the visual representation of each task. Examples of such operating systems are Microsoft Windows 95, Microsoft Windows NT, SCO Unix, and Sun's Solaris operating system. Embodiments of the invention are also for typical video graphics controllers, ones that support bit-block transfer (BitBlt) operations and DMA between processor memory and video memory. Graphics controllers from Chips and Technologies, S3, NeoMagic, Trident, and other companies all support these operations, for example.

Embodiments of the invention should be useable without necessarily relying on these assumptions, as hardware and software technologies evolve, for example (such as with multiprocessors used in one device, for example). Even currently, implementation in environments other than those described above is contemplated according to the invention, even though implementation in at least some of those environments may be more complex and subject to slower operation.

Thus, according to embodiments of the invention, and as shown in e.g. FIGS. **1**–**5**, screen peripheral system **5** according to an embodiment of the invention includes computing device **10** for e.g. executing a software application, and touch-activated input device **15** for generating and display-

ing a composite image visible to a user **20** of screen peripheral system **5**. The composite image includes, according to one embodiment, a representation of at least one key for activating an input function, e.g. a keyboard-input function. The composite image also includes a main display image, for example the output image produced by the software application being executed by computing device **10**. The representation of at least one key is laid over the main image produced by the software application.

FIG. **1** shows screen peripheral system **5** in a wearable-computing environment, which as described earlier is especially well-suited to embodiments of the invention. Embodiments of the invention can also be used in connection with a miniature, low-power, spread-spectrum "bodyLAN"-type system allowing selective control based on proximity to a user. With such a system, touch-activated input device **15** can be in either wired or wireless communication with computing device **10** and/or other devices/systems, for example LANs, WANs, etc. Wired and wireless communication embodiments are also contemplated for use with non-wearable computing devices as well. Fiber optic, electrical, infrared, RF and other data-transmission schemes between e.g. the disclosed input device and the wearable or other computer, or between any other elements of the system, are contemplated. For example, RF transmission to keyboard or a wearable, desktop, laptop or other computer. Embodiments of the invention are especially useful with tablet-type touch screens and other small, readily portable/pocketable input/output devices.

Embodiments of the invention also can be used in connection with heads-up and/or body-worn display devices, e.g. dual-screen stereo displays. A keyboard overlay according to the invention, preferably a voice-activated and/or voice-controlled overlay, appears on the display, allowing the user to input data without looking down. Automatic typing features with voice-recognition can be provided, whereby the user sees individual keys of the keyboard being activated as the user speaks. Voice can thus be used as an intuitive keyboard approach for the spoken words/letters in a hands-free environment.

Screen peripheral system **5** implements variable-pixel control to form the representation of at least one key and to form the output image, for example in the manner described above. The variable-pixel control causes the pixels used to form the representation of at least one key and the pixels used to form the output image to be directly dependent on each other, in a manner that for example is also described above. In other words, unlike the Ouellette reference disclosed above, the pixels chosen to represent the images are not independent.

The variable-pixel control can provide contrast adjustment between the representation of at least one key and the output image produced by the software application. The contrast adjustment can include changing at least one of the thickness, brightness, color and dotted-ness of the representation of at least one key.

As referenced above, according to one example computing device **5** eliminates X% of the pixels of a full representation of at least one key, X% representing that portion of the keyboard that is not to be seen in the composite image. In the first example described above, X=75, although X can have a variety of different values to suit a particular display or purpose. Computing device **5** also eliminates (100-X)%, e.g. 25% as described above, of the pixels of a full application output image. Here, (100-X)% represents that portion of the application output image that is not to be seen in the composite image. Computing device **5** merges the pixel-eliminated key representation with the pixel-eliminated main image to form the composite image. Alternatively and/or additionally, as in the second example described above, the composite image can include a blended shadow of the representation of at least one key and the main image. Computing device **5** can control the lightness/darkness of the blended shadow by controlling the blending of pixels of the at least one key representation and the main image, according to one embodiment. By changing the darkness of the pixels of the composite image, for example the keyboard portion of the composite image, the keyboard can be made to appear to "bleed through" the other image. Thus, the keyboard "steals away" appropriate pixels from the main image, and/or shades them differently in a selected manner, to produce the keyboard image.

As will be appreciated by those of ordinary skill in the art upon reading this disclosure, methods corresponding to the above-described apparatus and systems are also contemplated according to the invention.

FIGS. **2**–**5** illustrate sample images and composite screens according to embodiments of the invention. FIG. **2** illustrates a representation of at least one key—in this example a full QWERTY keyboard with several function/option keys/buttons. FIG. **3** illustrates a main image generated by a computing device. FIG. **3** should also be interpreted to cover the situation where the main image is an output image or images of an application or applications being executed by a processor or other element of the computing device. FIG. **4** shows a composite image formed in accordance with Example 1 above, and FIG. **5** shows a composite image formed in accordance with Example 2 above.

FIG. **6** illustrates a flow chart according to an embodiment of the invention, identifying the generalized processing that occurs to allow a virtual keyboard to be overlayed upon a normal display. This processing maintains consistency of the virtual keyboard image with the rest of the information being displayed.

After start step **100**, a virtual keyboard image is created, at step **105**. The keyboard is drawn as an overlay on the current display in step **110**, and then an event is awaited at step **115**. When a touch event occurs at step **120**, the virtual key touched is determined at step **125** and the keyboard event is sent to the current task/window at step **130**. The next event is then awaited at step **115**.

If there is no touch event at step **120**, it is determined whether a pertinent window has been redrawn, at step **135**. If so, the area of screen redrawn is determined at step **140**, and then it is determined at step **145** whether the area of screen redrawn overlaps the keyboard image. If not, the next event is simply awaited at step **115**. If so, the keyboard is (re)drawn as an overlay on the current display at step **110**. It is also determined whether a window is deleted at step **150**, and whether a window is created, at step **155**. If the answer is yes, steps **140**, **145** and **110** or **115** occur as described above. If the answer is no, the next event is (still) awaited at step **115**.

Mode-switching

According to one embodiment, if a representation of a key or button is held "down" for a set time, for example one second, a cursor appears at the point of the depressed key and the remainder of the keyboard (optionally) disappears. By dragging a finger along the touch screen, the user can move the cursor to a desired location. According to one embodiment, upon entering the cursor mode a number of new keys/buttons (or representations thereof, as above) appear on a side of the screen, for example, cut, paste, copy, delete and/or hold buttons. An appropriately placed mouse

button is also contemplated on the screen, e.g. in a corner of the screen, to be accessed by a user's thumb. A convenient holding mechanism for the screen, allowing easy access by the user's thumb, is described below.

In use, a user types on the keyboard overlay for a desired time, and then holds one finger down for a set period of time to exit the keyboard mode and enter the cursor mode. Selected text can be highlighted using the above-described mouse button in e.g. a corner or on a side of the touch screen, and then the cursor can be dragged to hover over a cut button or other desired button. Movement of the user's finger becomes equivalent to movement of the mouse when the finger is held down, and the touch button for the mouse is in the corner of the screen so that it is accessible by the thumb. Upon exiting the cursor mode, the user's fingers are again used for typing.

Reduced-key embodiments

According to one keyboard overlay embodiment, the number of keys of a virtual QWERTY keyboard is reduced to e.g. twelve, nine of which are letter keys and the other three of which are shift, delete and select keys, for example. Note FIG. **7**, showing one type of reduced-key keyboard **200**. Each letter key represents multiple letters, for example three letters or letter combinations. A word-recognition program discerns the word intended to be typed by hitting the letter keys, e.g. upon depressing the select (or space) keys. Reduced-key keyboard patterns enhance miniaturization achievable according to the invention and provide other advantages.

According to one embodiment of the invention, a reduced-key keyboard is incorporated as a virtual or physical touch layout **210** on a standard touch screen/slidepad mouse **220**, as shown in FIG. **8**. A program monitors the touch screen **220** continually, detecting when a virtual option button **230** or physical option button **240** is selected to change the mode of operation from a standard touchpad mouse ("relative" mode) to a keyboard-input touchpad ("absolute" mode). Upon entering the keyboard mode, a key pattern overlay (e.g. a letter keyboard, number pad, and/or individual keys) according to the invention appears on the touchscreen directly and/or on an associated screen. It is then detected which key of the keyboard the finger of the user is tapping on to generate letter/word or other input. Using a reduced-key keyboard in connection with a standard touchpad mouse, with mode-switching as described above, provides significant display-miniaturization and key-enlargement advantages, as well as other advantages such as an increase in one-finger typing speed.

According to another embodiment, the virtual or physical select or other buttons **230**, **240**, or another area on the touch screen itself, can be depressed multiple times, or held down for a longer period of time, to enter and/or exit various submodes of operation. The first touch can cause a change from a relative mode to an absolute mode, and subsequent touches to absolute submodes such as alphabet, numeric, punctuation and/or other sub-modes. For example, if a user desires to input e.g. punctuation while in a standard relative mouse mode, the user taps the appropriate button or buttons twice, first to enter the absolute mode and then to enter the punctuation input sub-mode, enters the appropriate punctuation, and then taps the button or buttons twice again to return to an absolute keypad mode. One or a plurality of buttons can be used to switch between relative and absolute modes, and, within e.g. the absolute mode, to choose a keyboard, number pad, punctuation input sub-mode or other option.

It is also known in the art to reduce the size of a full keyboard, with alphabetic, numeric and function sub-keyboards, by superimposing the keys of the sub-keyboards on top of each other. According to one example, the alphabetic sub-keyboard is superimposed on the numeric and function sub-keyboards. For numeric input, the numbers are printed not at the top of each key but where multiple adjacent letter keys meet, at the interstices between the keys. Four "quarter" keys thus operate together to register the desired number, but each virtual number key is full-sized. Beneath the four letter keys associated with each number are sensing areas, i.e. points or elements or regions, with activation of a sufficient number of sensing areas by the user's finger registering the desired number. This technology reduces the overall size of the keyboard, for example to credit-card size. Examples of these types of key layouts are shown in U.S. Pat. No. 5,612,690, among others. U.S. Pat. No. 5,612,690 is incorporated herein by reference.

Superimposing the keys of various sub-keyboards on top of each other, such as an alphabetic sub-keyboard superimposed on a numeric and/or function sub-keyboard, can be combined with the reduced-key concepts disclosed above with respect to FIGS. **7–8**, to further reduce the size of a keyboard or keyboard overlay according to the invention. With the layout of the FIG. **7** embodiment, for example, number and/or function keys would be placed at the physical or virtual "interstices" between the three-letter keys shown. The resulting composite image would then be superimposed over an application output in a manner described previously, for example.

Zoom embodiments

According to other embodiments, zoom-up/zoom-down capabilities are incorporated through a touch screen or other touch-sensitive input device, for example in a manner compatible with the above-described technologies. Once an appropriate zoom mode is activated, e.g. by virtual or physical keys, contact of one, two, three or more of a user's fingers with the touch-sensitive surface causes activation of an appropriate number of sensing areas and/or "zones" thereon to control screen size and/or the amount of magnification displayed. According to one example embodiment, one-finger contact causes normal screen size and/or magnification, two-finger contact causes a zoom-up to double size/magnification, three-finger contact causes triple size/magnification, and so on. Zoom-down capabilities function can be configured similarly. Sequential step-up or step-down is not required; for example triple-size/magnification can be reduced to normal size/magnification merely with the touch of one finger, without entering a double-size/magnification mode.

Thus, the user is spared the burden of going to a file menu, pulling down to the zoom feature and then selecting zoom-in and zoom-out functions using e.g. the mouse. A virtual, physical, or voice-activated zoom function select button is activated, and, simultaneously or thereafter, the touchscreen/slidepad itself determines how much of the touchscreen is covered at any one time by the user's fingers (or other pointing device), providing a specific screen size/magnification related to the number of fingers being used. According to a more specific embodiment, appropriate zoom functionality occurs based on the number of sensing areas or contact zones activated on the touch-sensitive input device. A particular area of a screen chosen can "zoom up" at the user as that area is touched.

These features have special relevance to portable, wearable computing, in which miniaturized screens are used, for example on the wrist, and generally are not full-sized. To use existing software, a user may want to see screen features in larger, zoomed-in format at certain times and, at other times,

in a zoomed-out format in refer ence to how items look on an overall page. Flip and rotate commands, either voice-based or touch-based, can also be implemented to improve/augment the user's view of the displayed information.

Other hardware embodiments

One problem with prior touch screens is that for miniature computers and miniature screens, the user's hand is often bigger than the screen itself. According to the embodiments of the invention, therefore, retractable handle **260** (FIGS. **9–10**) slides relative to touch screen **270** between extended and retracted positions, as shown at **280**, to provide a convenient holding mechanism at either the left or right side of touch screen **270**. To shift handle **260** from the left side to the right side, or vice versa, pivot **285** is provided to swing the handle over the touch screen, as shown at **290**. In the retracted position, the handle catches on the back side of the touch screen, permitting the pivoting motion. Upon traveling to or remaining in an extended position, a ball or similar projection snaps into a lateral groove or equivalent mechanism to prevent pivoting. Thus, embodiments of the invention are significantly advantageous for use by both left-handed and right-handed individuals, as shown in FIG. **10**, as well as those who need to use alternative hands for different tasks. Handle **260** can also be used as a carrying handle (FIG. **11**), as part of a necklace embodiment (FIG. **12**), or in a wristband embodiment (FIG. **13**) using e.g. a VELCRO strap. Additionally, according to another embodiment, a double-sided touch screen is provided, with the capability of flipping the screen by voice or by touch to accommodate left-handed or right-handed gripping of the touch screen by the handle without pivoting the handle from one side to the other. Multiple screen bleedthroughs, e.g. from one screen to another, on multiple screens, are also contemplated. A person with a folding screen or two displays can have them on more than one screen.

As indicated earlier, embodiments of the invention have application in voice-recognition and/or hands-free embodiments. A microphone/speaker can be built in the face of the touch-sensitive input device, permitting a user to look at and talk to the device without having a separate microphone/speaker. Voice commands can be used to change turn keyboard overlays and/or voice-input modes on and off, and to change contrast, keyboard representation types, keyboard/cursor modes, etc. Voice commands also can be used to activate the touch screen itself, so that it doesn't turn on by e.g. being depressed in a user's pocket, for example.

Other features

Sound and flashing can also be used in connection with an area to highlight where and when a user has touched the input device. Merging program use can be incorporated to highlight certain program outputs that are active and/or de-emphasize those that are inactive, for example by using a 25% pixel ratio for de-emphasis. As a user switches from one active program to another, their bleed-through intensities can shift and change accordingly. Multiprocessing be incorporated, wherein separate screens are run by separate processors, one for each screen. Keyboards can be moved, and percentage areas changed, by dragging. Although preferred embodiments have been described with respect to two images, any number of images can be combined/blended according to embodiments of the invention as long as their visual distinctions are preserved to the user's eye.

It is contemplated that features disclosed in this application, as well as those described in the above applications incorporated by reference, can be mixed and matched to suit particular circumstances. Various other modifications and changes will be apparent to those of ordinary skill.

What is claimed is:

1. A screen peripheral system, comprising:

a computing device for providing a main image; and

a touch-activated input device for generating and displaying a composite image visible to a user of the screen peripheral system, the touch-activated input device comprising a plurality of pixels, the composite image simultaneously including:

a representation of at least one key, the representation of at least one key activating an input function; and

the main image provided by the computing device, the representation of at least one key being laid over the main image;

wherein the screen peripheral system implements variable-pixel control to form the representation of at least one key and to form the main image, the variable-pixel control causing pixels selected to form the representation of at least one key in the composite image to depend on and be activated simultaneously with pixels selected to form the main image, such that the main image and the representation of at least one key are displayed simultaneously to form the composite image;

further wherein the variable-pixel control includes logical operators to provide different blending/merging effects such that individual pixels of the touch-activated input device can be dedicated simultaneously to both the main image and the representation of at least one key.

2. The screen peripheral system of claim **1**, wherein the variable-pixel control provides contrast adjustment between the representation of at least one key and the main image produced by the computing device.

3. The screen peripheral system of claim **2**, wherein the contrast adjustment includes changing at least one of the thickness, brightness, and dotted-ness of the representation of at least one key.

4. The screen peripheral system of claim **1**, wherein the representation of at least one key is a dotted-line representation.

5. The screen peripheral system of claim **1**, wherein the representation of at least one key includes a representation of a full keyboard.

6. The screen peripheral system of claim **1**, wherein the touch-activated input device operates in two modes, the first mode being a keyboard mode in which a user activates input functions by intermittently touching the input device, and the second mode being a cursor mode in which the user moves a cursor associated with the touch-activated input device, the second mode being entered from the first mode and/or the first mode being entered from the second by continuously touching the input device for a set time.

7. The screen peripheral system of claim **1**, wherein the computing device forms the composite image by merging the representation of at least one key with the main image.

8. The screen peripheral system of claim **7**, wherein the computing device merges the representation of at least one key with the main image by using a bit-block-type transfer operation.

9. The screen peripheral system of claim **8**, wherein the bit-block-type transfer operation performs logical combinations of three sets of pixels:

(a) the pixels of the main image;

(b) the pixels of the representation of at least one key; and

(c) optionally, an image mask for controlling which pixels of the main image will be merged with which pixels of the representation of at least one key.

10. The screen peripheral system of claim 1, wherein each pixel of the touch-activated input device is contributed 100% by either the pixels of the main image or the pixels of the representation of the at least one key to form the composite image.

11. The screen peripheral system of claim 1:

wherein the computing device eliminates X% of the pixels of a full representation of at least one key, X% representing that portion of the keyboard that is not to be seen in the composite image;

further wherein the computing device eliminates (100-X)% of the pixels of a full main image, (100-X)% representing that portion of the main image that is not to be seen in the composite image;

further wherein the computing device merges the pixel-eliminated key representation with the pixel-eliminated main image to form the composite image.

12. The screen peripheral system of claim 1, wherein the composite image includes a blended shadow of the representation of at least one key and the main image, or a clear space around a blended area to highlight the area of blending.

13. The screen peripheral system of claim 12, wherein the computing device controls the lightness/darkness of the blended shadow by controlling the blending of pixels of the at least one key representation and the main image.

14. The screen peripheral system of claim 1, wherein the computing device executes a software application, the main image being an output image produced by the software application executed by the computing device.

15. The screen peripheral system of claim 1, wherein the touch-activated input device provides zoom-up/zoom-down capability dependent on the number of the user's fingers in contact with the touch-activated input device.

16. The screen peripheral system of claim 1, wherein the touch-activated input device allows switching between relative and absolute input modes depending on the number of times or amount of time a user contacts a selected area of the touch-activated input device.

17. The screen peripheral system of claim 1, wherein the touch-activated input device allows switching between keyboards/alphanumeric sets depending on the number of times a user contacts a selected area of the touch-activated input device.

18. A wearable computing system comprising the screen peripheral system of claim 1.

19. A method of superimposing a representation of at least one key over a main image provided by a computing device, the method comprising:

(a) using variable-pixel control to form a representation of at least one key, the representation of at least one key activating an input function, and to form the main image, the variable-pixel control causing pixels selected to form the representation of at least one key to be activated simultaneously with pixels selected to form the main image; and

(b) generating and displaying a composite image visible to a user of the screen peripheral system, the composite image simultaneously including the representation of at least one key and the main image produced by the computing device, the representation of at least one key being superimposed on the main image;

wherein the variable-pixel control allows individual pixels to be dedicated simultaneously to both the main image and the representation of at least one key.

20. The method of claim 19, wherein the step of (b) includes the step of merging the representation of at least one key with the main image.

21. The method of claim 20, wherein said merging includes using a bit-block-type transfer operation.

22. The method of claim 21, wherein (b) further includes combining three sets of pixels:

(aa) the pixels of the main image;

(bb) the pixels of the representation of at least one key; and

(cc) optionally, an image mask for controlling which pixels of the main image will be merged with which pixels of the representation of at least one key.

23. The method of claim 21, wherein (b) further includes:

(c) eliminating X% of the pixels of a full representation of at least one key, X% representing that portion of the keyboard that is not to be seen in the composite image;

(d) eliminating (100-X)% of the pixels of a full main image, (100-X)% representing that portion of the main image that is not to be seen in the composite image; and

(e) merging the pixel-eliminated key representation with the pixel-eliminated main image to form the composite image.

24. The method of claim 19, wherein the composite image includes a blended shadow of the representation of at least one key and the main image.

25. The method of claim 24, wherein (b) includes controlling the lightness/darkness of the blended shadow by controlling the blending of pixels of the at least one key representation and the main image.

26. A screen peripheral system, comprising:

means for computing, the means for computing providing a main image;

means for displaying a composite image visible to a user of the screen peripheral system, the means for displaying also being for input to the means for computing, wherein the means for displaying comprises a plurality of pixels, the composite image simultaneously including:

a representation of at least one input zone, the representation of at least one input zone activating an input function; and

the main image provided by the means for computing, the representation of at least one input zone being laid over the main image;

wherein pixels selected to form the representation of at least one input zone are activated simultaneously with pixels selected to form the main image, such that the main image and the representation of at least one input zone are displayed simultaneously to form the composite image;

further wherein individual pixels of the means for displaying can be dedicated simultaneously to both the main image and the representation of at least one input zone.

27. The system of claim 26, wherein the representation of at least one input zone comprises at least one key of a keyboard.

28. The system of claim 26, wherein the representation of at least one input zone comprises a contact zone.

29. The system of claim 26, wherein the representation of at least one input zone comprises a button.

30. The system of claim 26, wherein the means for displaying a composite image comprises a touch screen.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,121,960
DATED : September 19, 2000
INVENTOR(S) : David W. Carroll et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the front page of the patent, in the "References Cited" section, the following U.S. Patent has been added:

--5,148,155 9/1992 Martin, et al.--

Signed and Sealed this

Twelfth Day of June, 2001

Nicholas P. Godici

Attest:

NICHOLAS P. GODICI

Attesting Officer *Acting Director of the United States Patent and Trademark Office*

EXHIBIT D

US006221686B1

(12) **United States Patent**
Drowley et al.

(10) **Patent No.: US 6,221,686 B1**
(45) **Date of Patent: Apr. 24, 2001**

(54) **METHOD OF MAKING A SEMICONDUCTOR IMAGE SENSOR**

(75) Inventors: **Clifford I. Drowley**, Phoenix; **Mark S. Swenson**, Higley; **Jennifer J. Patterson**, Mesa; **Shrinath Ramaswami**, Gilbert, all of AZ (US)

(73) Assignee: **Motorola, Inc.**, Schaumburg, IL (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/493,366**

(22) Filed: **Jan. 28, 2000**

Related U.S. Application Data

(62) Division of application No. 08/970,720, filed on Nov. 14, 1997, now Pat. No. 6,023,081.

(51) **Int. Cl.**[7] **H01L 21/00**
(52) **U.S. Cl.** **438/57**; 438/66; 438/69; 438/72; 438/73; 257/290; 257/292; 257/293
(58) **Field of Search** 438/57, 66, 69, 438/72, 73; 257/290, 292, 293, 233

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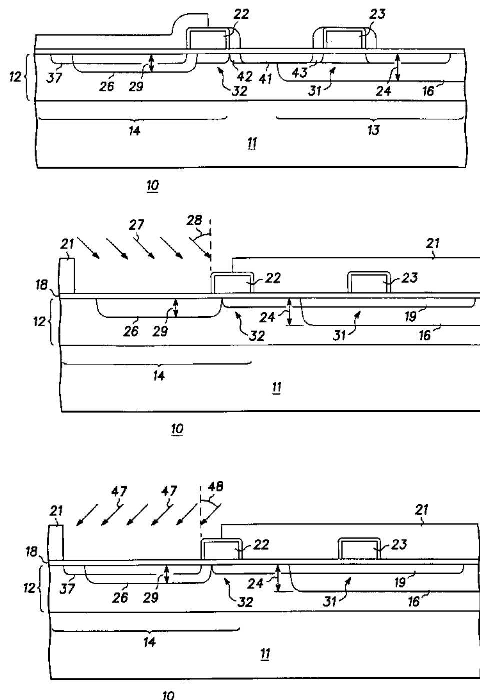
Primary Examiner—Charles Bowers
Assistant Examiner—Erik J. Kielin
(74) *Attorney, Agent, or Firm*—A. Kate Huffman

(57) **ABSTRACT**

An image sensor (**10**) has an image sensing element that includes an N-type conducting region (**26**) and a P-type pinned layer (**37**). The two regions form two P-N junctions at different depths that increase the efficiency of charge carrier collection at different frequencies of light. The conducting region (**26**) is formed by an angle implant that ensures that a portion of the conducting region (**26**) can function as a source of a MOS transistor (**32**).

34 Claims, 3 Drawing Sheets



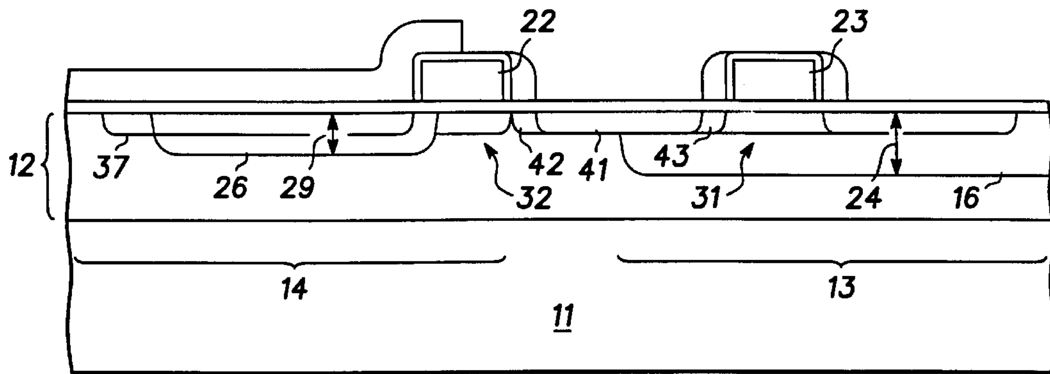


FIG. 1

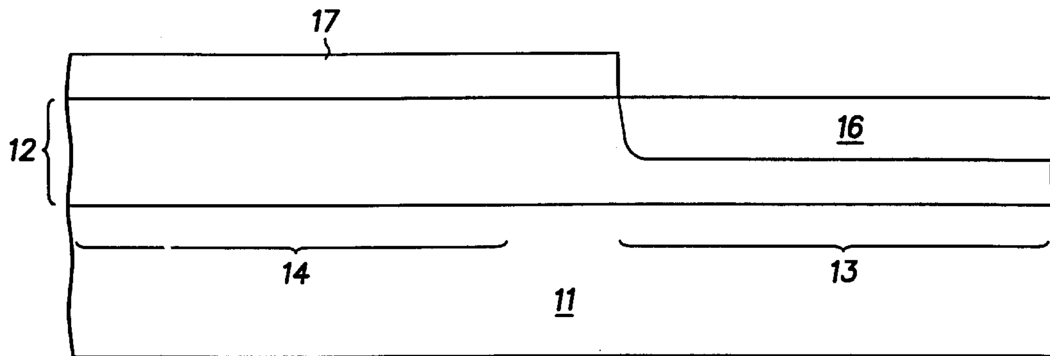


FIG. 2

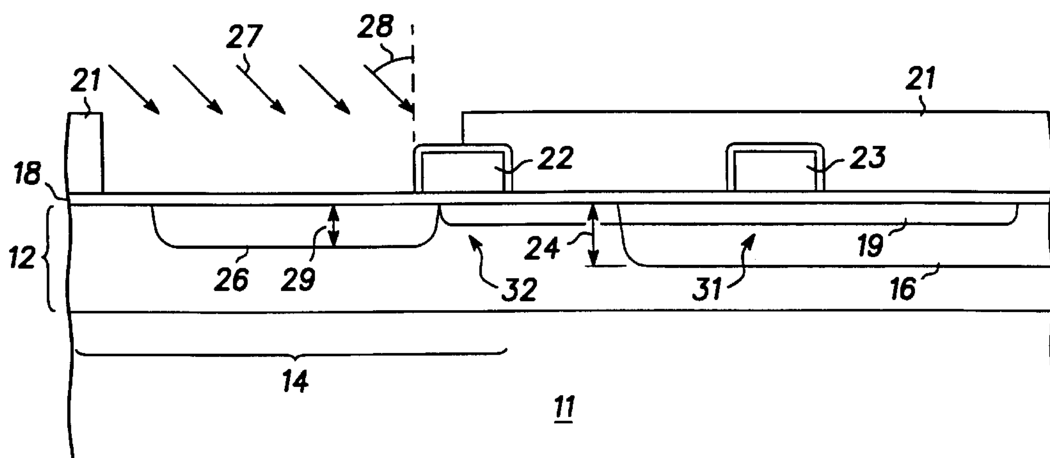
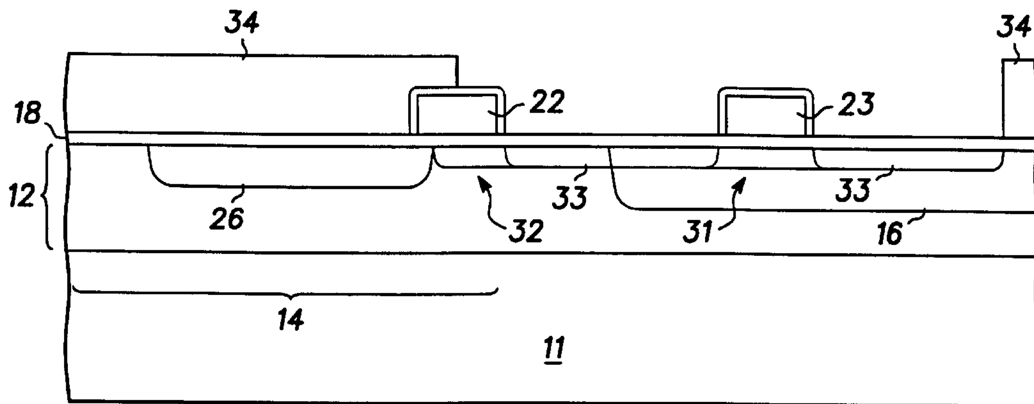
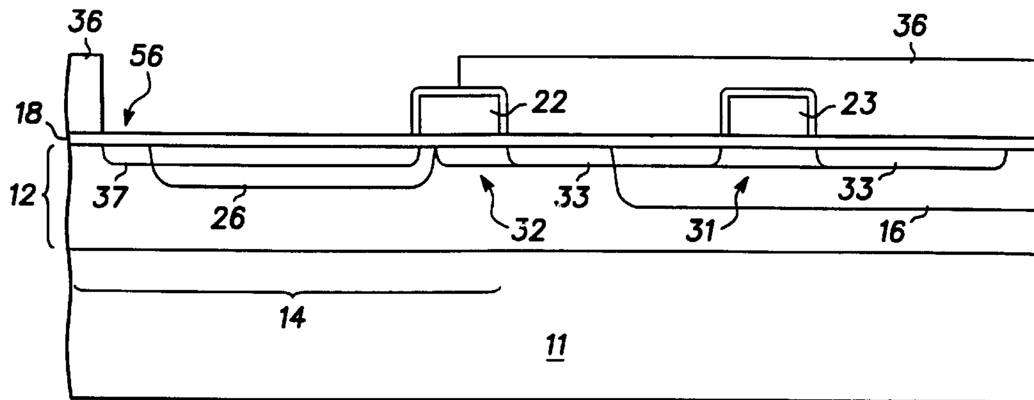


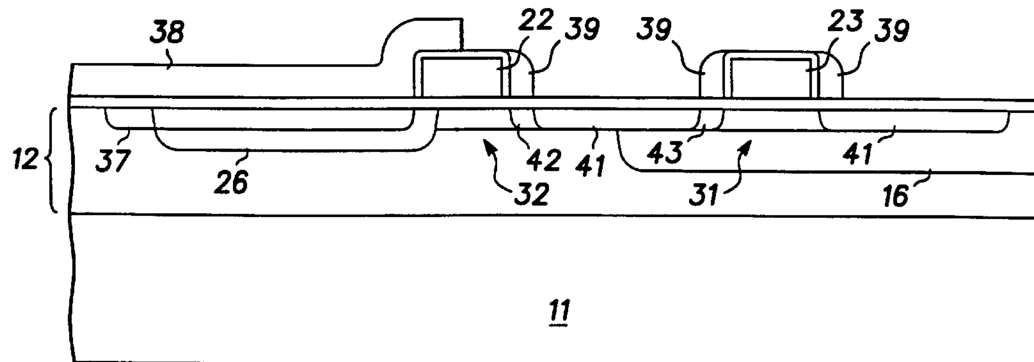
FIG. 3



10 FIG. 4



10 FIG. 5



10 FIG. 6

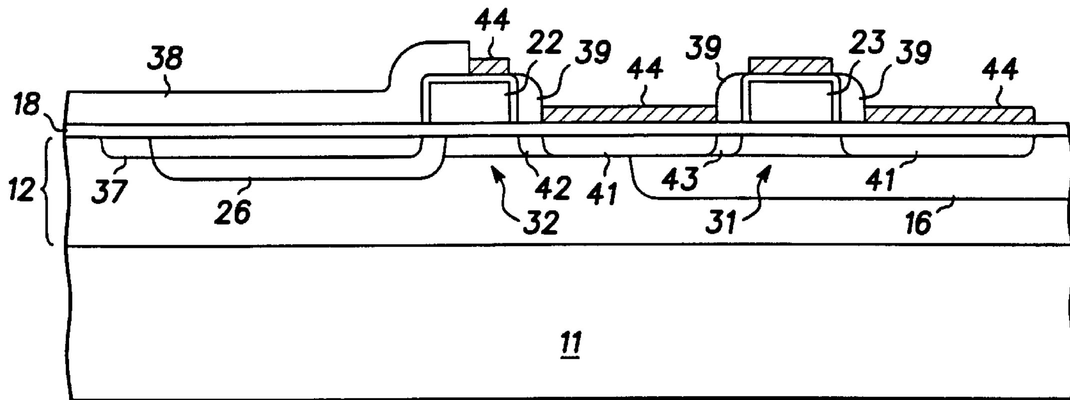


FIG. 7

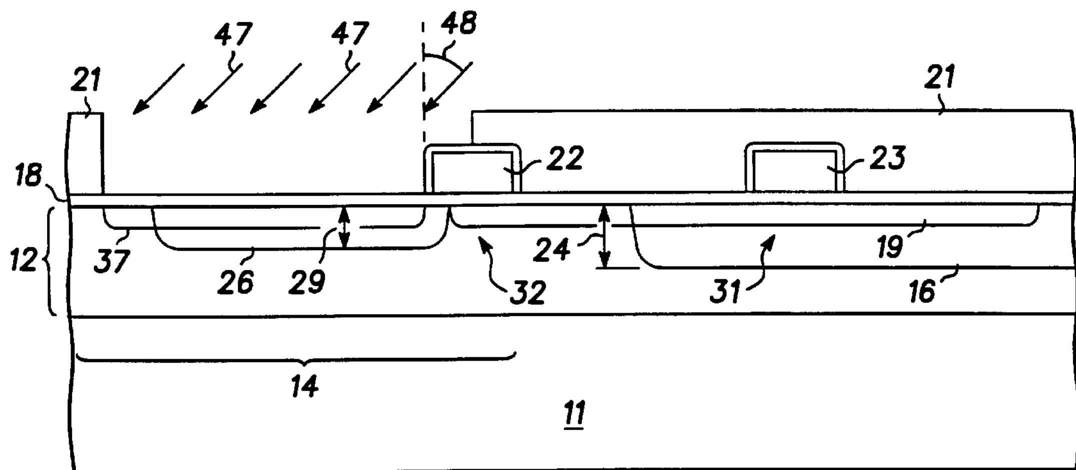


FIG. 8

METHOD OF MAKING A SEMICONDUCTOR IMAGE SENSOR

This application is a division of application Ser. No. 08/970,720 filed Nov. 14, 1997, now U.S. Pat. No. 6,023, 081.

BACKGROUND OF THE INVENTION

This application is related to an application entitled CMOS IMAGE SENSOR by Michael Guidash filed on the same day as the instant application, and an application entitled METHOD OF FORMING A SEMICONDUCTOR IMAGE SENSOR AND STRUCTURE by Drowley et al and filed concurrently herewith.

This invention relates, in general, to semiconductor devices, and more particularly to a semiconductor image sensor.

In the past, a variety of methods were used to form semiconductor image sensors on a substrate with complementary metal oxide semiconductor (CMOS) devices. Typically, the optical receiving portion of the sensor is formed either as a gate of a large area transistor, often referred to as a photo-gate, or as a source-drain junction of a metal oxide semiconductor (MOS) transistor. The photo-gate transistor implementation requires that light travel through the silicon gate of the transistor in order to convert light to electrical energy. Consequently, the photo-gate implementation has reduced sensitivity. Additionally, the depletion region generally is shallow (less than one micron) thereby reducing the collection efficiency of carriers induced by red light absorption. Also conventional photo-gate implementations are susceptible to noise created by surface recombination.

The source-drain junction implementation generally has a junction that is optimized for transistor operation and therefor also has a shallow junction that results in inefficient collection of carriers induced by red light. Another disadvantage of the source-drain junction implementation is that the junction typically is formed in a highly doped (greater than 10^{16} atoms/cm^3) region that limits the width of the junction depletion region thereby further reducing the collection efficiency of carriers induced by red light absorption. Furthermore, forming the junction in such a highly doped region results in a large capacitance that reduces the amount of charge that can be transferred from the photo sensing element to other electronics.

Traditional CMOS image sensor implementations often form a silicide layer over the image sensing element thereby further reducing sensitivity.

Accordingly, it is desirable to have an image sensor that does not utilize a photo-gate thereby resulting in higher efficiency, that does not have a shallow junction depth thereby increasing efficiency, that minimizes noise from surface recombination, that does not use a silicide overlying the light sensing area thereby further increasing efficiency, that has a wide depletion region for further increasing of carrier conversion for all wavelengths of light, and that does not have a large capacitance that minimizes the charge transferred from the image sensing element to other electronics.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates an enlarged cross-sectional portion of an image sensor embodiment in accordance with the present invention;

FIG **2** illustrates an enlarged cross-sectional portion of the FIG. **1** embodiment at a manufacturing stage in accordance with the present invention;

FIGS. **3–7** illustrate enlarged cross-sectional portions of the FIG. **1** embodiment at a subsequent manufacturing stages in accordance with the present invention; and

FIG. **8** illustrates an enlarged cross-sectional portion of an alternate embodiment of an image sensor in accordance with the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates an enlarged cross-sectional portion of a semiconductor image sensor **10**. Sensor **10** includes an underlying P-type substrate formed by a semiconductor substrate **11** and an enhancement layer **12** formed thereon. Sensor **10** has a first well or P-type well **16** formed in a first portion **13** of the underlying substrate. Well **16** typically has a doping concentration that is higher than the doping concentration in a second portion **14** of the underlying substrate's layer **12**. Portions **13** and **14** of layer **12** are identified by a brackets shown below layer **12**. This second portion of layer **12** forms a second well within the underlying substrate. The surface doping concentration of well **16** typically is at least 1×10^{16} atoms/cm^3. A first depth or depth **24** of well **16** typically is less than the depth of layer **12** and typically is about two to four microns in order to facilitate forming other CMOS devices on substrate **11**.

The image capturing or light sensing element of sensor **10** includes an N-type conducting region **26** that is formed in the second well or second portion **14**. Conducting region **26** forms a first P-N junction with the P-type material of the underlying substrate. This first P-N junction is positioned at a second depth or depth **29** of conducting region **26** in order to readily sense light in the red wavelengths and typically is less than approximately 0.7 microns, and preferably about 0.5 microns, from the surface of the underlying substrate. A P-type pinning layer **37** is formed within region **26** and extends outward from region **26** into layer **12** of the underlying substrate in order to form an electrical connection with the underlying substrate. This electrical connection pins the potential applied to this element of the image sensor. Consequently, the resulting photodiode is often referred to as a pinned photodiode. A second P-N junction is formed along the intersection of layer **37** and region **26**. Typically layer **37** is formed simultaneously with the formation of lightly doped drain and source regions of other P-channel MOS transistors (not shown) on substrate **11**. The depth of the second P-N junction is less than that of the first P-N junction. This depth is selected to optimize the absorption or sensing of light in the blue wavelengths. A transfer transistor or first MOS transistor **32** is formed adjacent to conducting region **26** so that a portion of region **26** forms a source of transistor **32**. A second or reset MOS transistor **31** is formed within well **16**. Transistor **31** has a source that is electrically coupled to transistor **32** by a coupling region **41**.

Conducting region **26** is formed by applying a mask having an opening that exposes some of the surface of portion **14** extending up to and including a portion of a gate **22** of transistor **32**. Then dopants are implanted at an angle away from perpendicular to substrate **11** and toward gate **22** to ensure that region **26** extends under gate **22**, thereby saving masking and other processing operations in forming region **26** and the source of transistor **32**.

FIG. **2** illustrates an enlarged cross-sectional portion of a stage in an embodiment of manufacturing sensor **10** shown in FIG. **1**. Sensor **10** includes a heavily doped P-type

substrate **11** having a lightly doped P-type enhancement layer **12** formed thereon. Typically, substrate **11** has a first or P-type doping concentration of at least 1×10^{16}, and preferably 1×10^{18}, atoms/cm^3 and layer **12** has a P-type doping concentration no greater than approximately 1×10^{15} atoms/cm^3. Additionally, layer **12** includes first portion **13** in which first well or P-well **16** is formed, and second well or second portion **14** in which the light sensing element of sensor **10** will be formed. Forming the light sensing elements in lightly doped second portion **14** that overlies more heavily doped substrate **11** enhances carrier collection in the light sensing element.

P-type well **16** is formed by applying a mask **17** to expose the surface of first portion **13** of layer **12**. Dopants are formed within the exposed surface to form well **16**. After forming well **16**, mask **17** is removed.

FIG. **3** illustrates an enlarged cross-sectional portion of sensor **10** shown in FIGS. **1** and **2** at a subsequent formation stage. Like elements in FIGS. **1**, **2**, and **3** have the same element numbers. A gate oxide **18** is formed across the surface of sensor **10**. Thereafter, a channel doping region **19** is formed to facilitate creating channels for MOS transistors **31** and **32**. Gates **23** and **22** are formed on oxide **18** to facilitate the formation of transistors **31** and **32**, respectively.

Thereafter, a mask **21** is applied to expose the area of second portion **14** in which conducting region **26** is to be formed. Mask **21** has an opening that exposes a portion of the surface of gate oxide **18** in second portion **14** the exposed portion extends from an edge of gate **22** into second portion **14**, and also exposes a portion of gate **22**. Dopants, illustrated by arrows **27**, are implanted at an angle **28** toward gate **22**. Angle **28** is measured away from a line normal to the surface of sensor **10**. Angle **28** typically is greater than fifteen degrees, and preferably is at least twenty five degrees, from normal to the surface of sensor **10**. This angle implant is used to ensure that region **26** extends slightly under gate **22** to facilitate utilizing a portion of region **26** to function as the source of transistor **32**, thereby connecting the channel of transistor **32** to conducting region **26**. Subsequent to forming region **26**, mask **21** is removed.

Alternately, two different implants can be utilized to form region **26**. A high energy implant, for example 120–190 keV, can be used near normal to the surface of sensor **10** in order to form region **26** deep within layer **12**. Thereafter a lower energy implant, for example 90–130 keV, can be formed at an angle substantially equal to angle **28** and at a low energy to ensure that a portion of region **26** extends under gate **22**.

FIG. **4** represents a subsequent stage in the formation of sensor **10**. Similar elements in FIGS. **1**, **2**, **3**, and **4** are represented by the same element numbers. A mask **34** is applied with an opening that exposes the areas for forming the drain of transistor **32**, and the source and drain of transistor **31**. Thereafter, source-drain dopants **33** are formed in layer **12** using the edges of gates **22** and **23** as masks to self-align the source and drain areas to gates **22** and **23**. Thereafter, mask **34** is removed.

FIG. **5** illustrates an enlarged cross-sectional portion of a subsequent stage in forming sensor **10**. Similar elements in FIGS. **1**, **2**, **3**, **4**, and **5** are represented by the same element numbers. A mask **36** is applied having an opening that exposes an edge of gate **22**, the surface of conducting region **26**, and an area **56**, shown by an arrow, extending past region **26**. P-type dopants are formed in the exposed surface to form P-type pinning layer **37** within the exposed portion of region **26** and extending outward from region **26** into area **56** and away from transistor **32**. The depth and doping concentra-

tion of layer **37** are chosen to facilitate transferring all photo induced charge from region **26** to the drain of transistor **32**. Typically, layer **37** has a depth of approximately 0.2 to 0.3 microns and a surface doping concentration greater than approximately 5×10^{17} atoms/cm^3. Subsequent to forming layer **37**, mask **36** is removed.

FIG. **6** illustrates a subsequent stage in the formation of sensor **10**. Similar elements in FIGS. **1**, **2**, **3**, **4**, **5**, and **6** are represented by the same element numbers. A dielectric material is applied to the surface of sensor **10** and is patterned to form spacers **39** on the sidewalls of gates **22** and **23**, and to form a dielectric covering **38** overlying the light sensing element of sensor **10**. Covering **38** typically extends onto gate **22** to form a mask for subsequent operations. The material used to form spacers **39** and covering **38** is chosen to have a dielectric constant between the dielectric constant of the underlying substrate and any material overlying covering **38**. The dielectric constant of covering **38** chosen in order to minimize reflections between the underlying semiconductor material and any other dielectric or material placed on top of covering **38**. For example, the material of covering **38** can be silicon nitride having a thickness of thirty to seventy nanometers in order to minimize reflections for light between the blue and red spectrums. Additionally, thickness of one hundred thirty to two hundred nanometers will also perform properly. Other materials such as aluminum oxide and aluminum nitride are also believed to be suitable materials for forming covering **38** and spacers **39**.

Subsequently, spacers **39** and covering **38** are used as masks to form N-type dopants in layer **12** that result in forming coupling region **41** electrically connecting drain **42** and source **43**.

FIG. **7** illustrates a subsequent stage in the formation of sensor **10**. Similar elements in FIGS. **1**–**7** are represented by the same element numbers. A low resistance material is applied to minimize the resistance of contacts made to both coupling region **41** and gates **22** and **23**. Typically, titanium is blanket deposited across sensor **10** and then annealed to form titanium silicide with any exposed underlying silicon material. Consequently, layer **38** prevents forming a silicide overlying the photo-diode formed by region **26** and layer **37**. The remaining titanium that does not form titanium silicide is removed thereby leaving low resistance contact materials **44** on gates **22**, **23**, and coupling region **41**. Such formation techniques are well known to those skilled in the art. Generally, an interlayer dielectric, not shown, is formed over sensor **10** and contacts made to appropriate portions thereof.

FIG. **8** illustrates an alternate embodiment for forming pinned layer **37** of sensor **10**. Subsequent to forming conducting region **26** as discussed in FIG. **3**, layer **37** can be formed by performing an implant at an angle opposite to angle **28** shown in FIG. **3**. In this embodiment, dopants, represented by arrows **47**, are implanted away from gate **22** at an angle **48** from normal to the surface of sensor **10**. Typically, angle **48** is between ten and twenty five degrees to ensure that a portion of layer **37** extends outward from region **26** away from transistor **32**. This portion of layer **37** is utilized to form contact with enhancement layer **12**. For some processing sequences, this alternate embodiment can reduce the number of processing operations.

By now it should be appreciated that there has been provided a novel image sensor and method therefor. Forming the image sensor in a lightly doped region that overlies a more heavily doped region enhances carrier collection. Forming a deep conducting region and a shallower pinned layer forms two P-N junctions where one P-N junction, and

the associated depletion region, is deep to facilitate capturing light in the red wavelengths and a second P-N junction, and the associated depletion region, is shallow facilitating capturing blue wavelength light. This structure also minimizes surface recombination and maximizes charge transfer. Using an angled implant to form the conducting region ensures the conducting region can be used as a source of a charge transfer transistor thereby minimizing manufacturing operations. Utilizing a dielectric material having a dielectric constant between the dielectric constant of the underlying substrate and overlying material minimizes reflections and enhances efficiency of the sensor. Ensuring that the light sensing element is devoid of an overlying silicide material also improves the efficiency of the sensor.

What is claimed is:

1. A method of forming an image sensor comprising:

providing a semiconductor substrate of a first conductivity type;

forming an enhancement layer on the substrate, the enhancement layer having the first conductivity type and a first doping concentration;

forming a first well on a first portion of the enhancement layer, the first well having the first conductivity type and a second doping concentration that is greater than the first doping concentration wherein the first well has a first depth into the enhancement layer;

forming a conducting region of a second conductivity type in a second portion of the enhancement layer wherein a first portion of the conducting region forms a portion of a MOS transistor; and

forming a pinned layer of the first conductivity type in the second region of the enhancement layer by forming a first portion of the pinned layer within the conducting region and a second portion of the pinned layer extending laterally from the conducting region in a direction away from the MOS transistor.

2. The method of claim **1** wherein providing the substrate includes providing the substrate with a third doping concentration greater than the first and second doping concentrations.

3. The method of claim **1** wherein forming the conducting region includes implanting a first dopant at a first angle from normal to the substrate and angled toward the MOS transistor.

4. The method of claim **3** wherein implanting the first dopant at the first angle includes using an angle of at least fifteen degrees.

5. The method of claim **3** wherein implanting the first dopant at the first angle includes implanting a first doping concentration substantially normal to the substrate and implanting a second doping concentration at the first angle.

6. The method of claim **5** wherein the first doping concentration is implanted at a first energy and the second doping concentration is implanted at a second energy.

7. The method of claim **3** wherein the steps of forming the conducting region and forming the pinned layer of the first conductivity type includes implanting the conducting region by implanting the first dopant at the first angle away from normal to the substrate and toward the MOS transistor and implanting the pinned layer at a second angle away from normal to the substrate and away from the MOS transistor.

8. The method of claim **7** wherein implanting the first dopant at the first angle includes implanting a first doping concentration substantially normal to the substrate and implanting a second doping concentration at the first angle.

9. The method of claim **8** wherein the first doping concentration is implanted at a first energy and the second doping concentration is implanted at a second energy.

10. The method of claim **1** wherein forming the conducting region includes forming the conducting region to a depth less than 0.7 microns.

11. The method of claim **1** wherein forming the first well includes forming the first well to a first depth no greater than a depth of the enhancement layer.

12. The method of claim **1** further including forming a dielectric layer overlying the pinned layer, and forming a silicide layer on a portion of the image sensor wherein an area overlying the pinned layer is devoid of the silicide layer.

13. The method of claim **1** further including forming a dielectric layer overlying the pinned layer wherein the dielectric layer has a dielectric constant that is between a dielectric constant of any material overlying the dielectric layer and a dielectric constant of an underlying substrate on which the pinned layer is formed.

14. A method of forming an image sensor comprising:

using an implant at a first angle to form a conducting region of the image sensor; and forming a pinned layer at least partially within the conducting region.

15. The method of claim **14** further including using a substrate of a first doping concentration, and forming an enhancement layer on the substrate, the enhancement layer having a doping concentration that is less than the first doping concentration wherein the conducting region is formed in the enhancement layer.

16. The method of claim **14** further including forming the pinned layer by implanting at a second angle.

17. The method of claim **14** further including forming a dielectric layer overlying the pinned layer, and forming a silicide layer on a portion of the image sensor wherein an area overlying the pinned layer is devoid of the silicide layer.

18. The method of claim **14** further including forming a dielectric layer overlying the pinned layer wherein the dielectric layer has a dielectric constant that is between a dielectric constant of any material overlying the dielectric layer and a dielectric constant of an underlying substrate on which the pinned layer is formed.

19. A method of forming an active pixel sensor comprising:

providing a semiconductor substrate of a first conductivity type;

forming an enhancement layer on the substrate, the enhancement layer having the first conductivity type and a first doping concentration;

forming a first well on a first portion of the enhancement layer, the first well having the first conductivity type and a second doping concentration that is greater than the first doping concentration wherein the first well has a first depth into the enhancement layer;

forming at least one MOS transistor in the first well in the first portion; and

providing a pinned photodiode in a second portion of the enhancement layer, the pinned photodiode having a first P-N junction at a first depth from the surface, a second P-N junction at a second depth that is less than the first depth, and a conducting region of the second conductivity type between the first depth and the second depth; and

forming at least one MOS transistor in the second portion of the enhancement layer, such that the pinned photodiode forms a portion of the MOS transistor in the second portion, and a gate of the MOS transistor in the second portion is within the second portion and a drain of the MOS transistor is within the first portion and the second portion.

20. The method of claim **19** wherein the step of forming the portion of the MOS transistor in the second portion of the enhancement layer such that the portion of the MOS transistor formed from the pinned photodiode further comprises forming the photodiode portion such that the portion underlies the gate of the MOS transistor.

21. The method of claim **20** wherein forming the pinned photodiode includes forming a pinned layer of the first conductivity type in the second portion of the enhancement layer by forming a first portion of the pinned layer within the conducting region of the second conductivity type and a second portion of the pinned layer extending laterally from the conducting region of the second conductivity type in a direction away from the MOS transistor.

22. The method of claim **19** wherein providing the substrate includes providing the substrate with a third doping concentration greater than the first and second doping concentrations.

23. The method of claim **19** wherein forming the conducting region of the second conductivity type includes implanting a first dopant at a first angle from normal to the substrate and angled toward the MOS transistor.

24. The method of claim **23** wherein implanting the first dopant at the first angle includes using an angle of at least fifteen degrees.

25. The method of claim **23** wherein implanting the first dopant at the first angle includes implanting a first doping concentration substantially normal to the substrate and implanting a second doping concentration at the first angle.

26. The method of claim **25** wherein the first doping concentration is implanted at a first energy and the second doping concentration is implanted at a second energy.

27. The method of claim **23** wherein the steps of forming the conducting region and forming the pinned layer of the first conductivity type includes implanting the conducting region by implanting the first dopant at the first angle away from normal to the substrate and toward the MOS transistor and implanting the pinned layer at a second angle away from normal to the substrate and away from the MOS transistor.

28. The method of claim **27** wherein implanting the first dopant at the first angle includes implanting a first doping concentration substantially normal to the substrate and implanting a second doping concentration at the first angle.

29. The method of claim **28** wherein the first doping concentration is implanted at a first energy and the second doping concentration is implanted at a second energy.

30. The method of clam **19** wherein forming the conducting region includes forming the conducting region to a depth less than 0.7 microns.

31. The method of claim **19** wherein forming the first well includes forming the first well to a first depth no greater than a depth of the enhancement layer.

32. The method of claim **19** further including forming a dielectric layer overlying the pinned photodiode, and forming a silicide layer on a portion of the image sensor wherein an area overlying the pinned photodiode is devoid of the silicide layer.

33. The method of claim **19** further including forming a dielectric layer overlying the pinned photodiode wherein the dielectric layer has a dielectric constant that is between a dielectric constant of any material overlying the dielectric layer and a dielectric constant of an underlying substrate on which the pinned photodiode is formed.

34. The method of claim **19** further including forming the enhancement layer and first well such that the first well, the enhancement region and the substrate are connected by an ohmic conduction path below the surface of the semiconductor.

* * * * *

EXHIBIT E

US006979587B2

(12) **United States Patent**
Lee

(10) **Patent No.:** **US 6,979,587 B2**
(45) **Date of Patent:** **Dec. 27, 2005**

(54) **IMAGE SENSOR AND METHOD FOR FABRICATING THE SAME**

(75) Inventor: **Won-Ho Lee**, Ichon-shi (KR)

(73) Assignee: **Hynix Semiconductor Inc.**, Kyoungki-do (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 224 days.

(21) Appl. No.: **10/330,287**

(22) Filed: **Dec. 30, 2002**

(65) **Prior Publication Data**

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(30) **Foreign Application Priority Data**

Jan. 10, 2002 (KR) 10-2002-0001367

(51) **Int. Cl.**[7] **H01L 21/00**

(52) **U.S. Cl.** **438/57**; 438/451; 257/292; 257/446

(58) **Field of Search** 438/57, 73, 449, 438/451, 525, 527, 529; 257/291, 292, 446, 463

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Primary Examiner—Amir Zarabian
Assistant Examiner—Christy Novacek
(74) *Attorney, Agent, or Firm*—Birch, Stewart, Kolasch & Birch, LLP

(57) **ABSTRACT**

The present invention provides an image sensor capable of suppressing the dark current due to crystalline defects occurring at an edge of a field oxide layer and a method for fabricating the same. The present invention provides an image sensor including: a semiconductor substrate; an active area including a photodiode area formed in a predetermined position of the substrate, a floating diffusion area having a smaller area than the photodiode area and a channel area having a bottle-neck structure connecting to the photodiode area and the floating diffusion area; a field area for isolating electrically the active area; a field stop layer being formed beneath the field area by having a wider area than the field area through an expansion towards the active area with a first width; and a gate electrode formed on the substrate by covering the channel area and having one side superposed with a second width on one entire side of the photodiode contacted to the channel area.

10 Claims, 11 Drawing Sheets

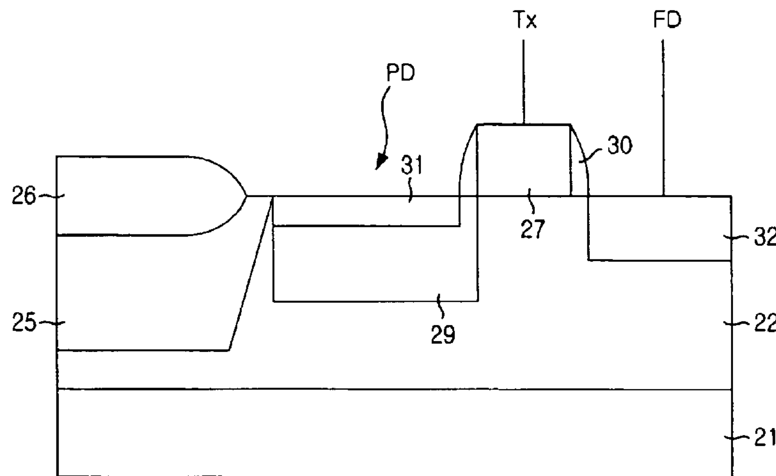

FIG. 1
(PRIOR ART)

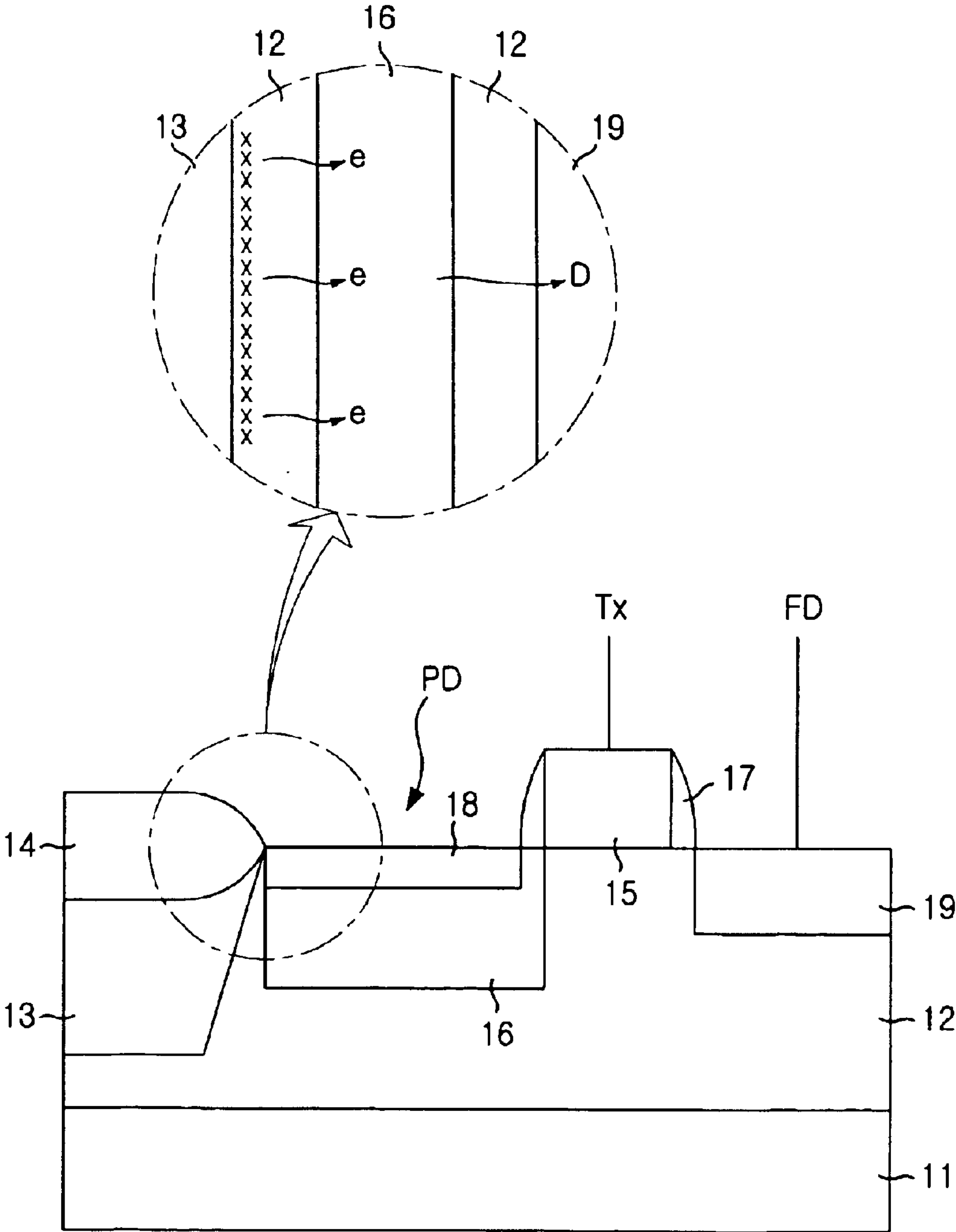

FIG. 2
(PRIOR ART)

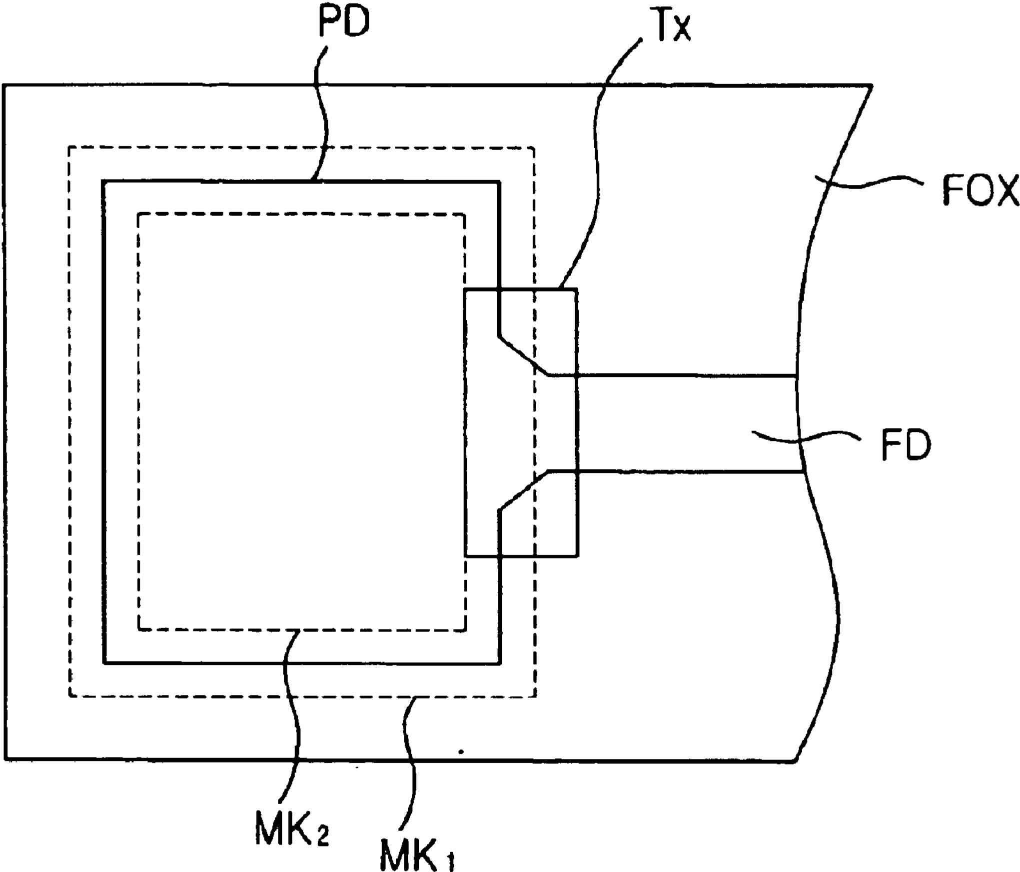

FIG. 3

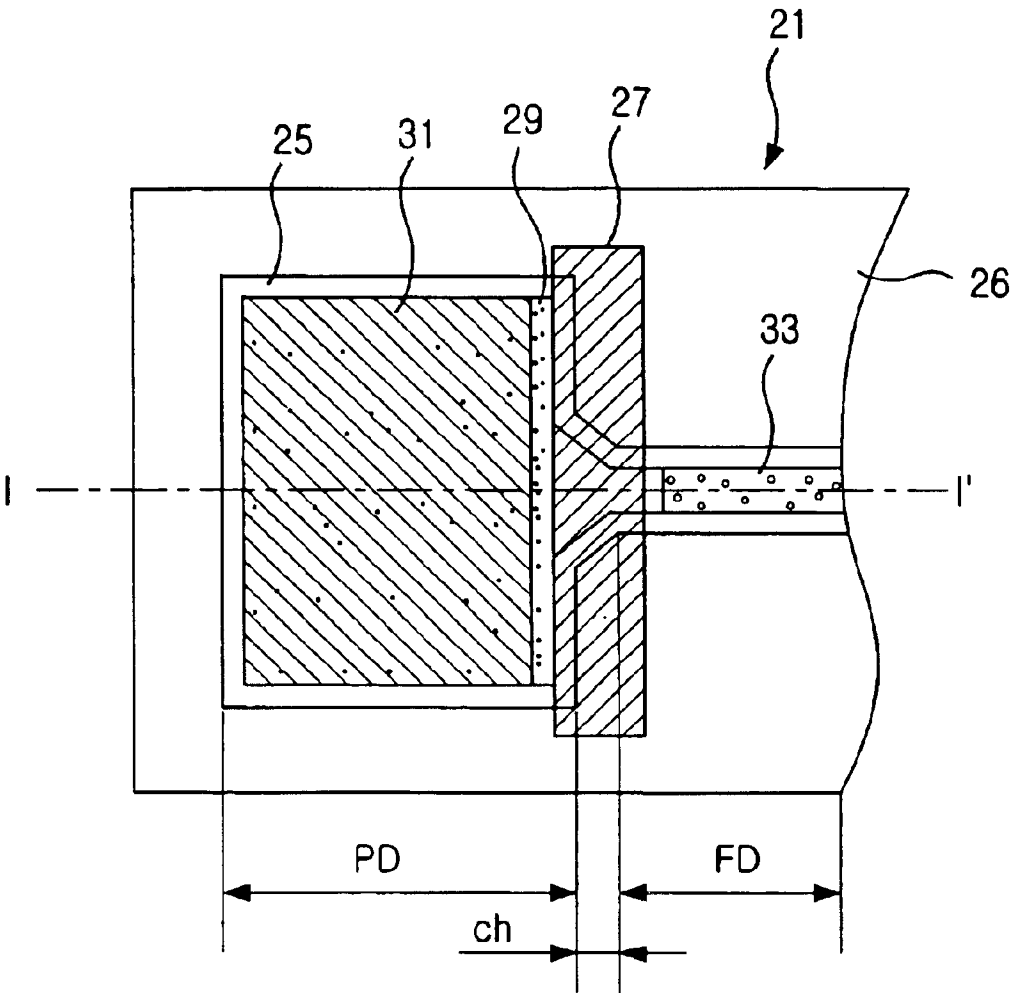

FIG. 4A

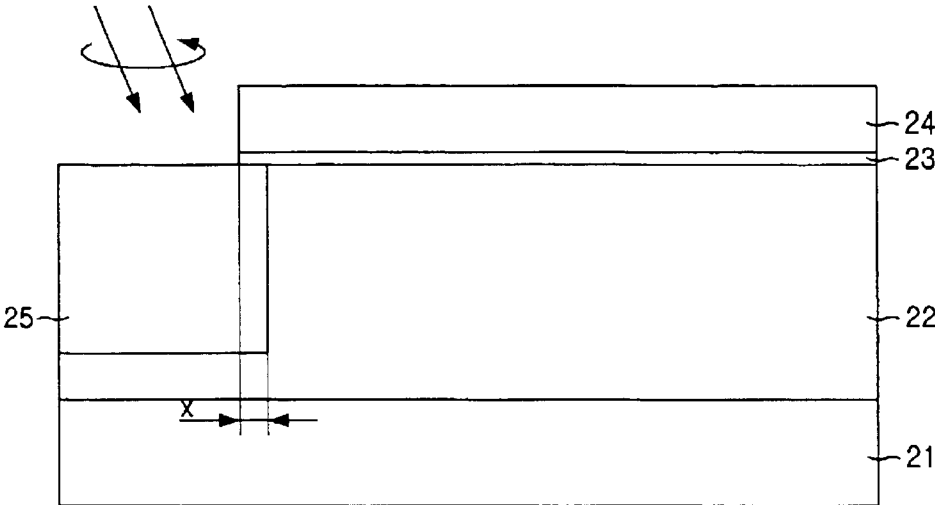

FIG. 4B

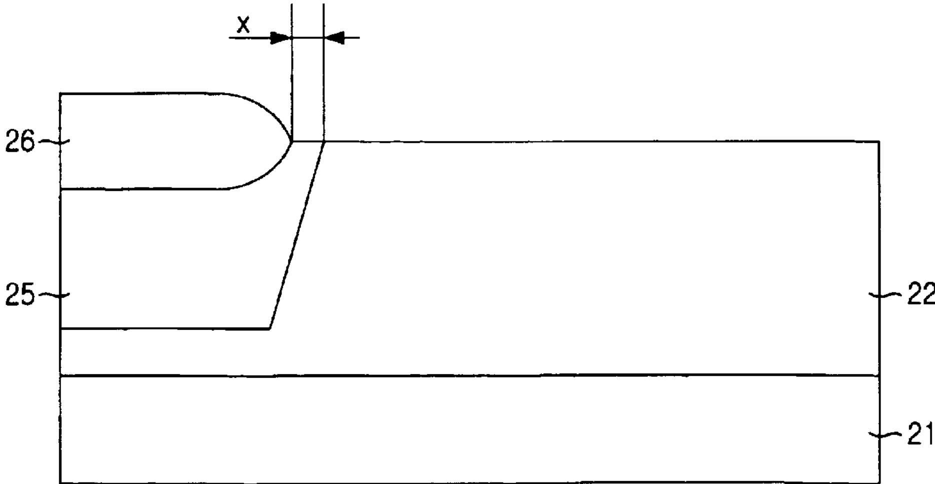

FIG. 4C

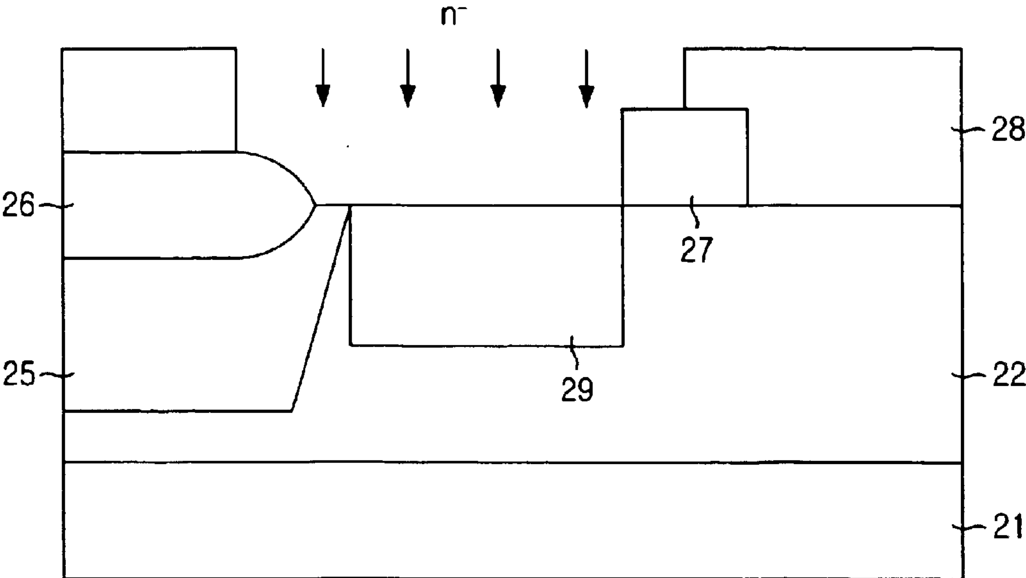

FIG. 4D

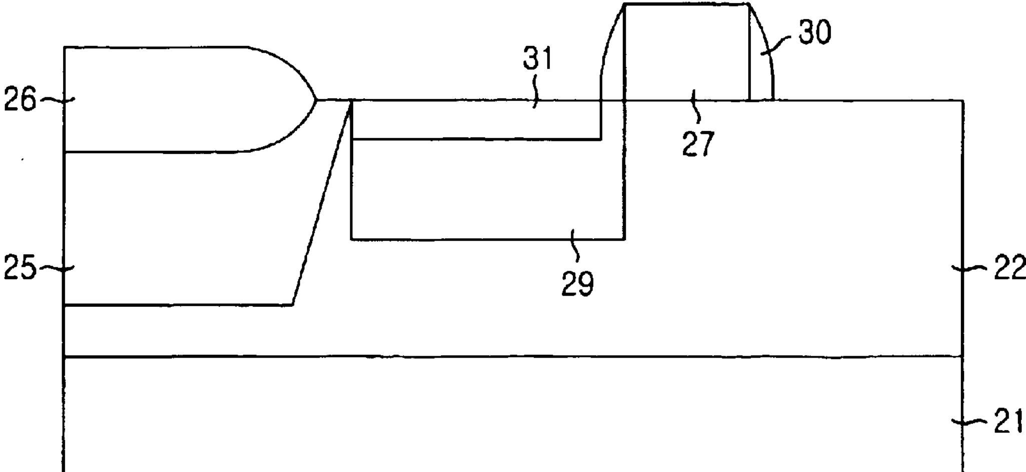

FIG. 4E

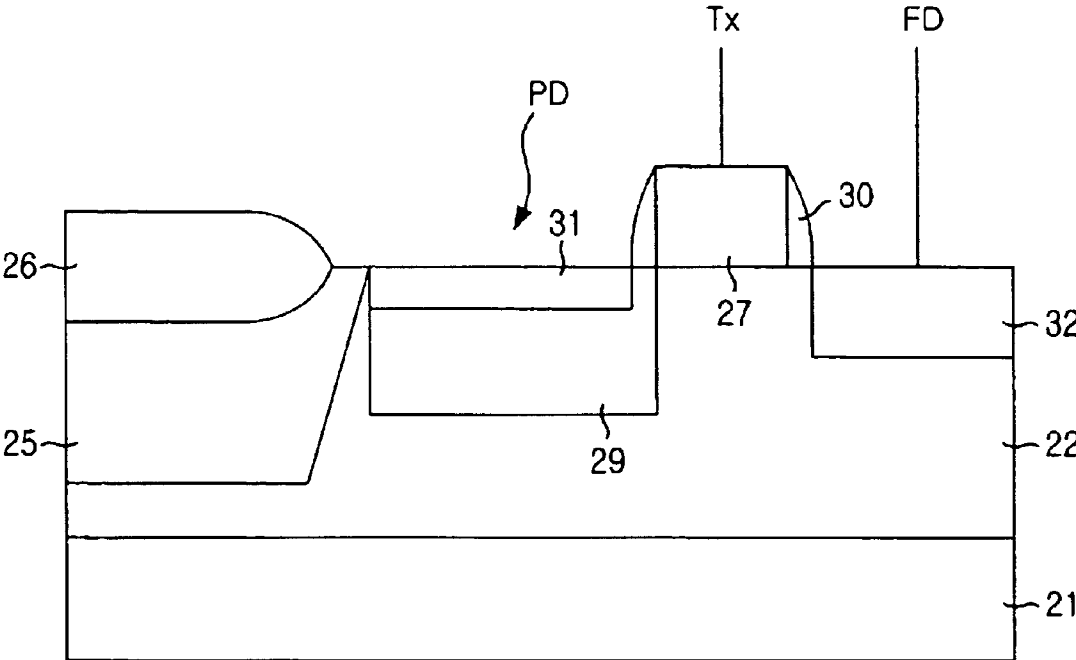

FIG. 5A

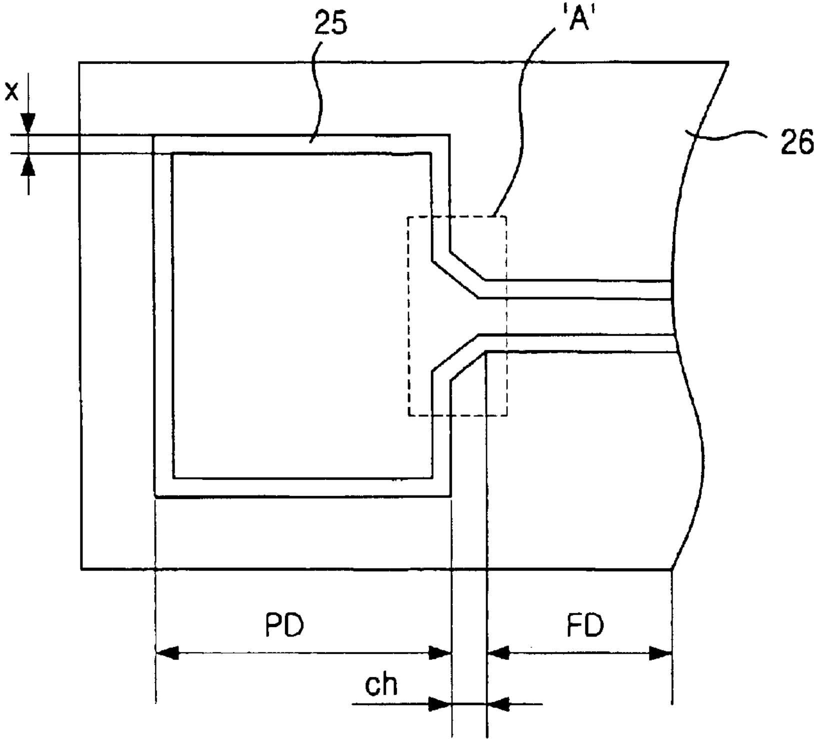

FIG. 5B

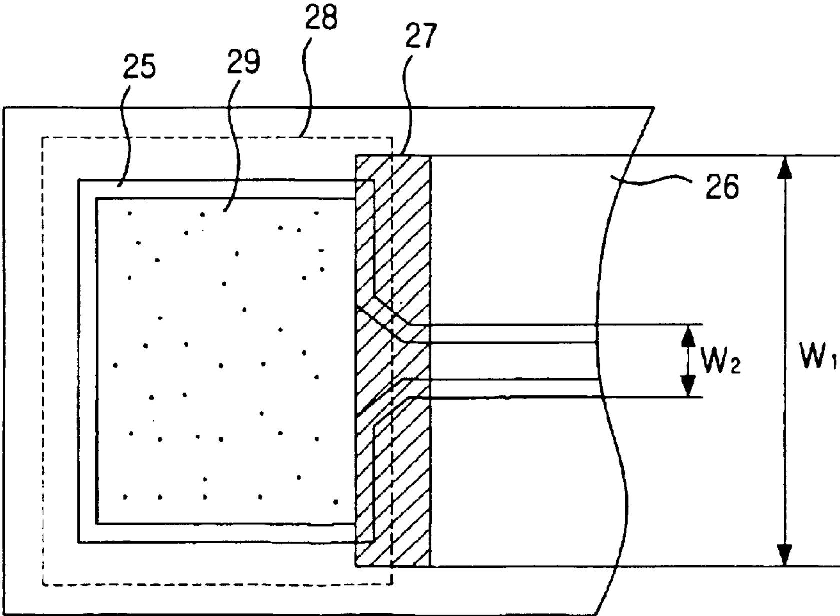

FIG. 5C

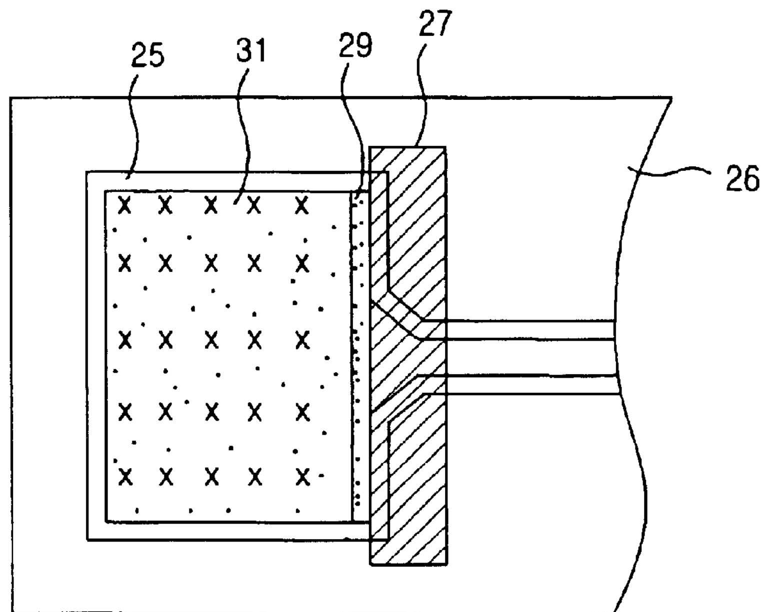

FIG. 5D

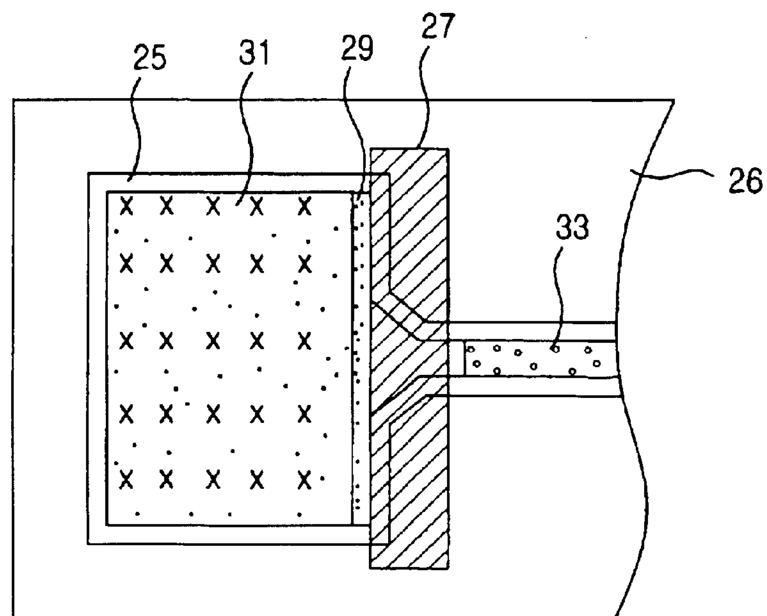

FIG. 6

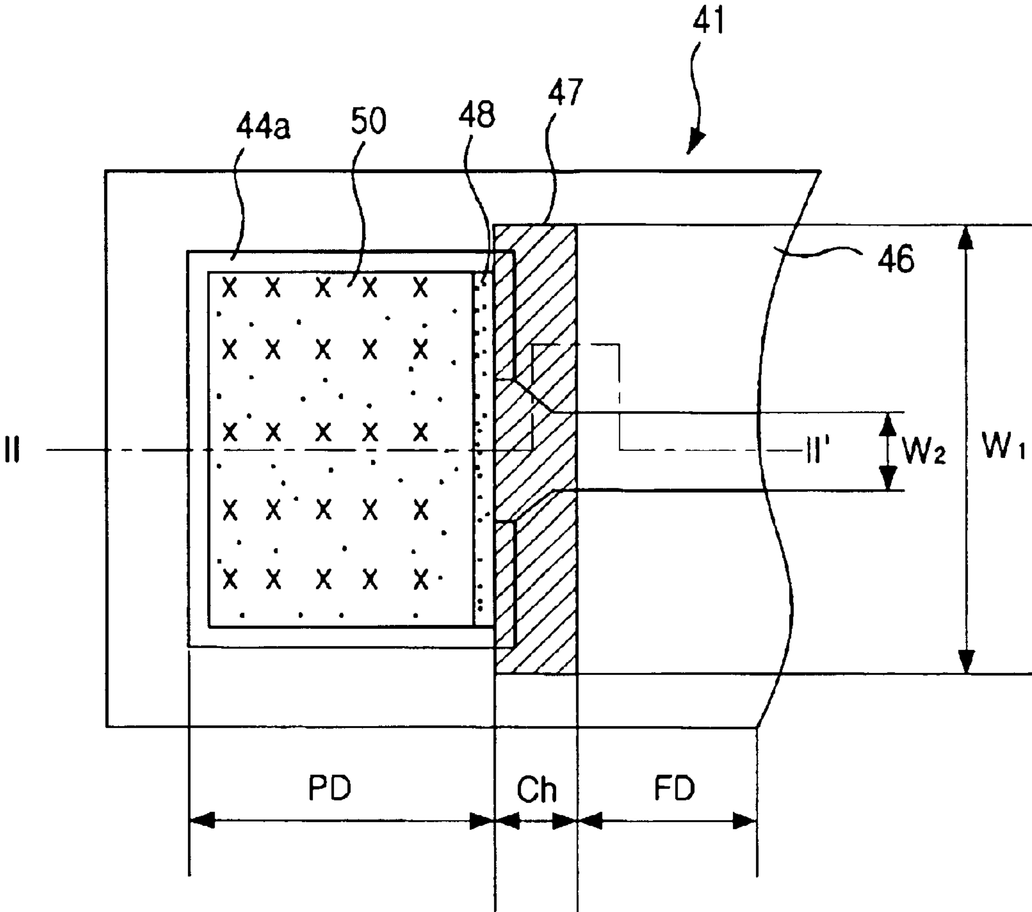

FIG. 7A

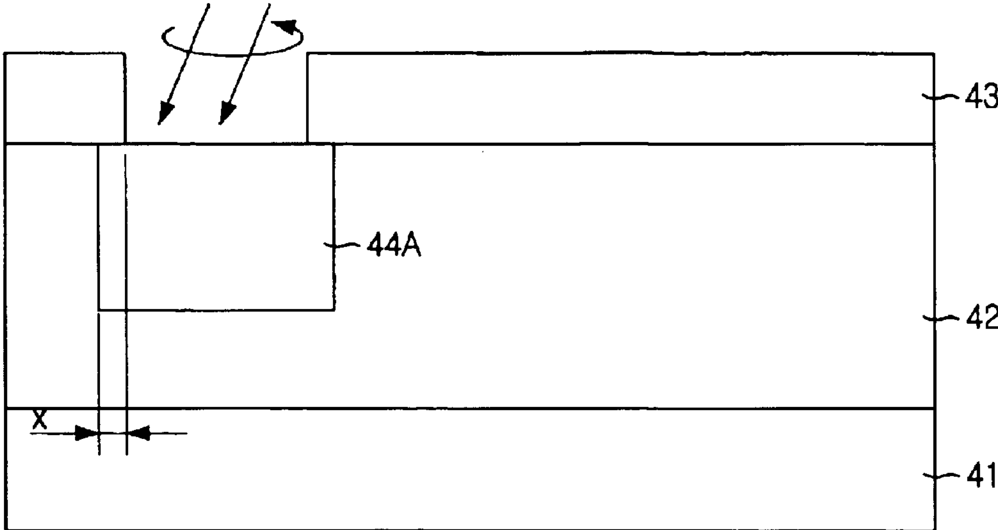

FIG. 7B

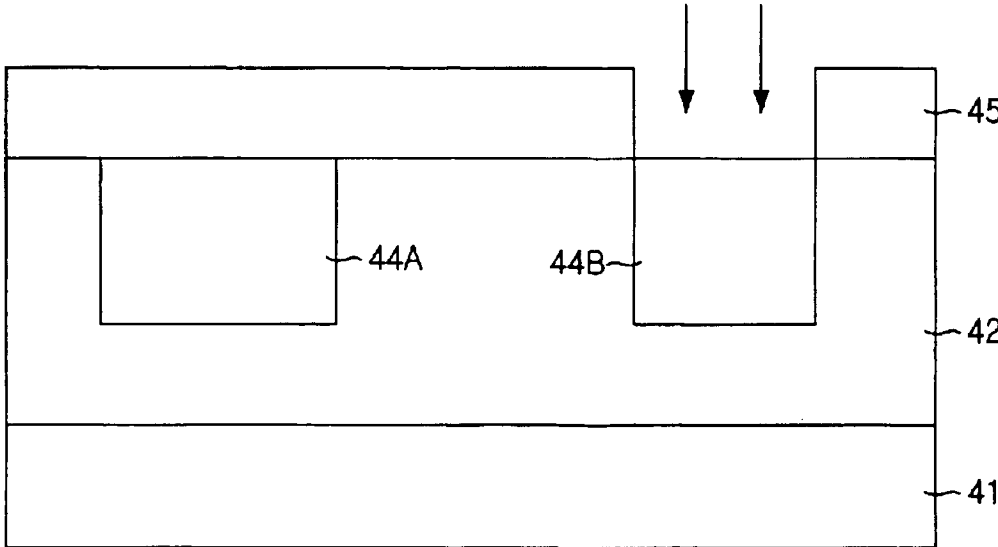

FIG. 7C

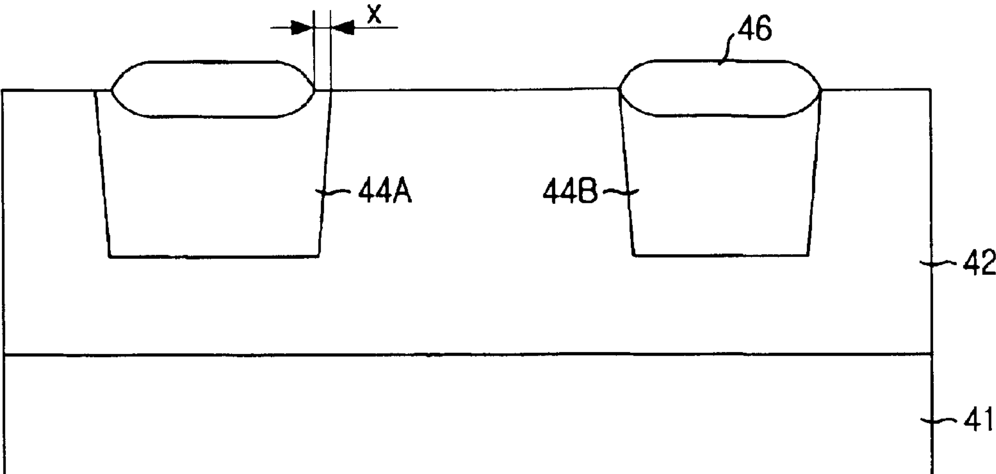

FIG. 7D

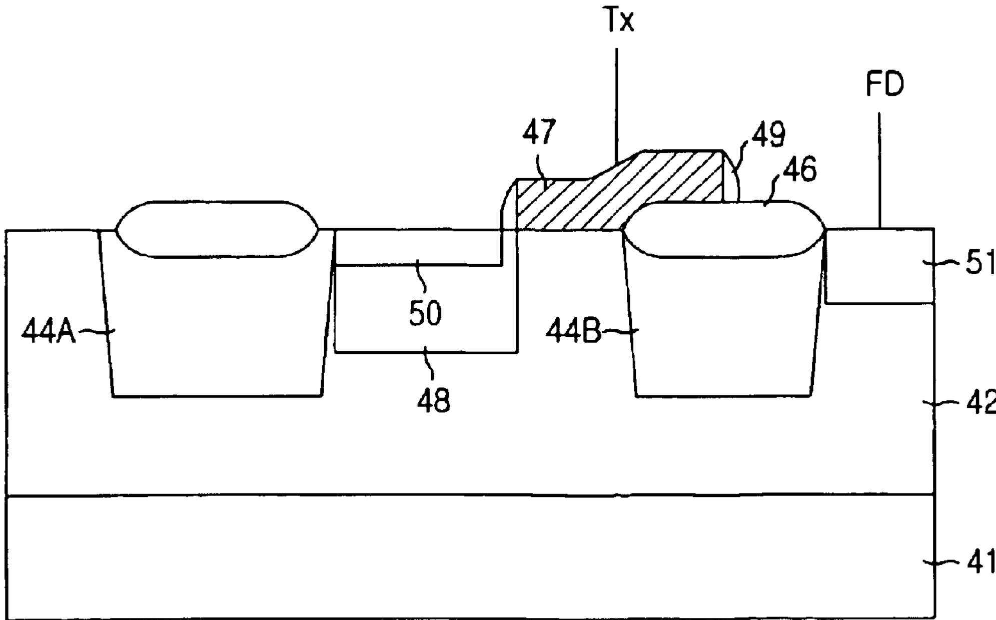

IMAGE SENSOR AND METHOD FOR FABRICATING THE SAME

This nonprovisional application claims priority under 35 U.S.C. §119(a) on Patent Application No. 2002-0001367 filed in KOREA on Jan. 10, 2002, which is herein incorporated by reference.

FIELD OF THE INVENTION

The present invention relates to a method for fabricating a semiconductor device; and, more particularly, to an image sensor and a method for fabricating the same.

DESCRIPTION OF RELATED ARTS

Image sensor is a semiconductor device that converts an optical image into an electrical signal. Among the image sensors, a charge coupled device (CCD) is a device wherein an individual metal-oxide-silicon (CMOS) capacitor is closely allocated to each other, and carriers are stored and transferred to the MOS capacitor. A complementary metal-oxide semiconductor device (CMOS) image sensor employs CMOS technology using a control circuit and a signal processing circuit as peripheral circuits. In the CMOS image sensor, MOS transistors are formed as the same number of pixels in the peripheral circuit, and a switching mode is adopted for detecting sequentially outputs with use of the MOS transistors.

The CMOS image sensor includes a color filter arrayed on top of a light sensing element that generates and stores an optical charge after receiving light from an external source. The color filter array (CFA) can be classified with three colors of red (R), green (G) and blue (B) or those of yellow (Y), magenta (M) and cyan (C).

Also, the image sensor is constituted with a light sensing element for sensing light and a logic circuit component for processing the sensed light into an electrical signal, which is, in turn, systemized into data. There has been numerously attempted to improve a fill factor, which represents an areal ratio of the light sensing element with respect to the overall image sensor. However, these attempts are limited since the logic circuit component cannot be basically removed.

Accordingly, there introduced a light condensing technology for changing paths of incident lights that enter to areas other than the light sensing element and condensing the incident lights into the light sensing element so as to enhance a level of light sensing. To realize the light condensing technology, a method for forming a microlens on the color filter of the image sensor is particularly used.

A unit pixel of the typical CMOS image sensor has one photodiode area (hereinafter referred as to PD) and four N-channel metal-oxide semiconductor (NMOS) transistors, that are, a transfer transistor T_x, a reset transistor R_x, select transistor S_x and a drive transistor D_x. With respect to a specific function of each of the four NMOS transistors, the T_x is for transferring photo-generated charges collected at the PD to a floating diffusion area (hereinafter referred as to FD). The R_x is for resetting the FD by setting an electric potential of a node into a desired value and then releasing a charge (C_{pd}). Also, the D_x enacts as a source follower buffer amplifier, and the S_x is for providing a function of addressing with a switch.

Herein, the T_x and the R_x uses a native NMOS transistor, whereas the D_x and the S_x uses a normal NMOS transistor. Especially, the R_x is a transistor for a correlated double sampling (CDS).

The unit pixel of the above-described CMOS image sensor uses the native NMOS transistor so to sense rays in the visible wavelength bandwidth at the PD and then transfer detected photo-generated charges to the FD, i.e., an amount of the photo-generated charges transferred to a gate of the D_x is outputted in an electric signal from an output terminal V_{out}.

FIG. **1** is a cross-sectional view showing a typical CMOS image sensor in accordance with a prior art. Particularly, FIG. **1** shows merely a PD, a transfer transistor T_x and a FD.

Referring to FIG. **1**, a p-type epi layer **12** that is undergone with an epitaxial growth is formed on a P^+ substrate **11**. Also, a field oxide layer **14** for isolating devices is formed on the p-type epi layer **12**. A field stop layer **13** for an n-channel field stop layer is formed beneath the field oxide layer **14**.

Herein, the field stop layer **13** is allocated only beneath the field oxide layer **14** since ions are implanted without any tilts into the p-type epi layer **12** where the field oxide layer **14** is formed. Therefore, an n diffusion area **16** constituting the PD has only a boundary with an edge of the field oxide layer **14**, but does not affect an area of the n^- diffusion area **16**.

In addition, a gate electrode **15** of a T_x is formed on the p-type epi layer **12**. Also, a spacer **17** is then formed at lateral sides of the gate electrode **15**. The n^- diffusion area **16** is formed deeply in the p-type epi layer **12** by being aligned to an edge of one side of the gate electrode **15**. A shallow p^0 diffusion layer **18** is then formed on top of the n^- diffusion layer **16** as being aligned to one side of the spacer **17**.

Eventually, a PD including a deep n^- diffusion area **16** and a shallow p^0 diffusion area **18** is formed. A FD **19** is formed in the p-type epi layer **12** as being aligned to the spacer formed at the other side of the gate electrode **15**.

Meanwhile, one side of an ion implantation mask MK_1 (not shown) for forming the n^- diffusion area **16** is aligned to a center of the gate electrode of the T_x, while the other side of the ion implantation mask MK_1 is aligned to the field oxide layer **14**.

FIG. **2** is a plane view of FIG. **1** showing the typical CMOS image sensor in accordance with the prior art. One side of the gate electrode of the T_x is overlapped to an active area for providing the PD. The FD is formed below the other side of the gate electrode of the T_x.

Also, in the active area defined by the field oxide layer (FOX), the PD has a relatively larger area; however, an area between the PD and the FD becomes smaller. This effect is called a bottle-neck effect.

Meanwhile, as shown in FIG. **1**, when forming the n^- diffusion layer **16** constituting the PD, the n^- diffusion layer **16** is formed entirely on the active area except for a portion superposed on the gate electrode **15** of the T_x since the ion implantation mask MK_1 has a wide width compared to the actually formed n^- diffusion layer **16**. Therefore, the n^- diffusion area **16** is contacted to the field oxide layer FOX.

In the above-described prior art, if there exists a reverse bias between the n^- diffusion layer **16** and the p-area including the p^0 diffusion layer and the p-type epi layer, the n^- diffusion layer **16** becomes fully depleted when a concentration of impurities contained in the n^- diffusion layer **16** and the p-area is properly controlled. As a result of this full depletion, the depletion is also extended to the p-type epi layer **12** allocated beneath the n^- diffusion layer **16** and the p^0 diffusion layer **18** allocated above the n^- diffusion layer **16**. Especially, the depletion occurs in more extents in the p-type epi layer **12** having a relatively lower dopant concentration.

The image sensor having the above PD takes out electrons stored into the PD and obtains an electrical output signal, i.e., current or voltage. A maximum output signal is in a proportional relationship with the number of electrons that can be taken out from the PD, and thus, the number of electrons generated and stored in the PD due to inputs of light should be increased in order to increase the output signals.

The electrons generated at the depletion layer of the PD are converted to an electrical output signal such as a voltage or a current. Hence, the ion implantation is proceeded in such that a dopant concentration of the p^0 diffusion layer **18**, which is a surface layer, should be higher than that of the n^- diffusion layer **16** and the p-type epi layer **12**, which are a bottom layer.

Meanwhile, in the prior art, when incident lights are inputted, there occurs an electron hole pair (EHP) at the n^- diffusion layer **16**, which is the depletion layer. The hole (H) of the EHP is drained to the p^+ substrate **11**, and the electron (e) is accumulated and transferred to the FD **19** through the transfer transistor T_x so as to attain image data.

However, the prior art has a problem in that crystalline defects occur mainly at the edge of the field oxide layer **13** when applying an oxidation process to the field oxide layer **13**. A point defect, a line defect, an area defect and a volume defect are examples of the crystalline defects.

Eventually, electrons (e) are generated and stored due to the crystalline defects occurring at the edge of the field oxide layer **14** even when incident lights are not inputted. Therefore, there occurs dark current (D) flowing from the PD to the FD **19**.

In other words, the electrons should be generated and stored at the depletion layer, i.e., the n^- diffusion layer **16** of the PD only when the incident lights are inputted, and then, the stored electrons are transferred to the FD so to make current flow. However, the crystalline defects present at the edge of the field oxide layer **14** are in a state of generating electrons easily in a thermal aspect even without inputs of the incident lights. Thus, if there exists a plurality of defects even in a dark state without any light, the image sensor shows an abnormal state by acting as if there are inputs of the incident lights.

To solve the above problem, it is suggested to employ an ion implantation mask MK_2 of which linewidth is relatively smaller than the MK_1 for forming the deep n^- diffusion layer **16** (referred to FIG. **2**). However, this approach is sensitive to an overlay since there occurs no self-alignment during the ion implantation mask MK_2 process for forming the deep n^- diffusion layer **16**. Also, there is another problem in that the n^- diffusion layer **16** is extended near to an edge of the field oxide layer FOX due to a subsequent thermal process.

SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to provide an image sensor capable of suppressing generation of dark current due to crystalline defects at an edge of a field oxide layer and a method for fabricating the same.

In accordance with an aspect of the present invention, there is provided an image sensor, comprising: a semiconductor substrate; an active area including a photodiode area formed in a predetermined position of the substrate, a floating diffusion area having a smaller area than the photodiode area and a channel area having a bottle-neck structure connecting to the photodiode area and the floating diffusion area; a field area for isolating electrically the active area; a field stop layer being formed beneath the field area by having a wider area than the field area through an expansion towards the active area with a first width; and a gate electrode formed on the substrate by covering the channel area and having one side superposed with a second width on one entire side of the photodiode contacted to the channel area.

In accordance with another aspect of the present invention, there is also provided an image sensor, comprising: a substrate; an active area including a photodiode area formed in a predetermined position of the substrate, a floating diffusion area having a smaller area than the photodiode area and a channel area having a bottle-neck structure connecting to the photodiode area and the floating diffusion area; a field area for isolating electrically the active area; a field stop layer being formed beneath the field area by having a wider area than the field area through an expansion towards the photodiode area with a first width; and a gate electrode formed on the substrate by covering the channel area and having one side superposed with a second width on one entire side of the photodiode contacted to the channel area.

In accordance with still another aspect of the present invention, there is also provided a method for fabricating an image sensor, comprising the steps of: forming an isolation mask that exposes partially a surface of the substrate; forming a first diffusion layer having a wider area than an exposed area of the isolation mask in the exposed substrate; forming a field oxide layer having a smaller area than the first diffusion layer on the first diffusion layer; forming a gate electrode on an active area of the substrate defined by the field oxide layer; forming a second diffusion layer being aligned to an edge of one side of the gate electrode in the substrate and to the first diffusion layer; and forming a third diffusion layer being aligned with a predetermined distance from the edge of the one side of the gate electrode formed in the second diffusion layer.

In accordance with still another aspect of the present invention, there is also provided a method for forming an image sensor, comprising the steps of: forming on the substrate a first isolation mask that exposes a surface of one side of the substrate; forming a first diffusion layer having a wider area than an exposed area of the first isolation mask formed in the exposed substrate; forming on the substrate a second isolation mask that exposes the other side of the substrate; forming a second diffusion layer having an area identical to an exposed area of the second isolation mask formed in the exposed substrate; forming on the first diffusion layer a first field oxide layer having a smaller area than the first diffusion layer as simultaneously as forming on the second diffusion layer a second field oxide layer having an area identical to the second diffusion layer; forming a gate electrode extending on the active area of the substrate and simultaneously on the second field oxide layer; forming a third diffusion layer being aligned to an edge of one side of the gate electrode in the substrate and the first diffusion layer; and forming a forth diffusion layer being aligned with a predetermined distance from the edge of the one side of the gate electrode in the third diffusion layer.

BRIEF DESCRIPTION OF THE DRAWING(S)

The above and other objects and features of the present invention will become apparent from the following description of the preferred embodiments given in conjunction with the accompanying drawings, in which:

FIG. **1** is a cross-sectional view showing a complementary metal-oxide semiconductor (CMOS) image sensor in accordance with a prior art;

FIG. 2 is a plane view showing the CMOS image sensor in accordance with the prior art;

FIG. 3 is a plane view showing a CMOS image sensor in accordance with a first preferred embodiment of the present invention;

FIGS. 4A to 4E are cross-sectional views illustrating a process for fabricating the CMOS image sensor with respect to a I-I' line of FIG. 3;

FIGS. 5A to 5D are plane views illustrating a process for fabricating the CMOS image sensor with respect to the I-I' line of FIG. 3;

FIG. 6 is a plane view showing a CMOS image sensor in accordance with a second preferred embodiment of the present invention; and

FIGS. 7A to 7D are cross-sectional views illustrating a process for fabricating the CMOS image sensor with respect to a II-II' line of FIG. 6.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 3 is a plane view showing a complementary metal-oxide semiconductor device (hereinafter referred as to CMOS) image sensor in accordance with a first preferred embodiment of the present invention. The-CMOS image sensor shown in FIG. 3 includes a photodiode area (hereinafter referred as to PD), a gate electrode of a transfer transistor T_x and a floating diffusion area (hereinafter referred as to FD).

On a predetermined place of a substrate **21**, an active area including the PD, the FD having a smaller area than the PD and a channel area ch having a bottle-neck structure that connects the PD and the FD is formed.

Then, a field oxide layer **26** for isolating electrically the active area is formed. A field stop layer **25** having a greater area than the field oxide layer **26** as being extended towards the active area with a first predetermined distance is formed beneath the field oxide layer **26**.

Also, a gate electrode **27** having one side superposed entirely on one side of the PD connected to the channel area ch with a second predetermined distance and the other side aligned to the FD is formed on the substrate **21**. Herein, the gate electrode also covers the channel area ch.

In the mean time, the PD includes an n^- diffusion area **29** formed by being self-aligned to the field stop layer **25** and the one side of the gate electrode **27** of the transfer transistor T_x and a p^0 diffusion area **31** formed in the n^- diffusion area **29** by being self-aligned to the field stop layer **25** with a predetermined distance from the one side of the gate electrode **27**.

Meanwhile, an n^+ diffusion layer **33** is formed at the other side of the gate electrode **27**.

FIGS. 4A to 4E are cross-sectional views illustrating a process for fabricating the CMOS image sensor with respect to an I-I' line of FIG. 3. Also, FIGS. 5A to 5D are plane views illustrating a process for fabricating the CMOS image sensor with respect to the I-I' line of FIG. 3.

With reference to FIGS. 4A to 4E and FIGS. 5A to 5D, the process for forming the CMOS image sensor with respect to the I-I' line of FIG. 3 will be explained in more detail.

Referring to FIG. 4A, a p-type epi layer **22** is grown on a p^+ substrate **21** doped with a high concentration of p-type impurities. On the p-type epi layer **22**, a pad oxide layer **23** and a pad nitride layer **24** are formed thereafter.

Herein, the reason for growing the p-type epi layer **22** is because a depth of a depletion layer of the PD can be increased due to the existence of the p-type epi layer **22** with a low dopant concentration. As a result, it is possible to obtain an excellent photosensitivity and to prevent the crosstalk phenomenon, which occurs between unit pixels of the CMOS image sensor due to irregular movements of optical charges that may be taken place at the deeper p^+-substrate **21**, by recombining the optical charges through the p^+-substrate **21** with the high dopant concentration.

Next, an isolation mask (not shown) is formed on the pad nitride layer **24**. Subsequently, the pad nitride layer **24** exposed by the isolation mask is firstly etched. After etching the pad nitride layer, the exposed pad nitride layer **23** is then etched so as to expose a surface of the p-type epi layer **22** where a field oxide layer will be formed.

Herein, the exposed p-type epi layer **22** has an area where the field oxide layer is formed and the unexposed p-type epi layer **22** is an active area.

After removing the isolation mask, impurities for an n-channel field stop layer **25** (hereinafter referred as to field stop layer) are ion implanted partially on the surface of the exposed p-type epi layer **22** by giving a tilt angle through rotation and twist. Herein, the pad nitride layer **24** exposed through the removal of the isolation mask is used as a mask.

At this time, the ion implantation for forming the field stop layer **25** is proceeded by giving a predetermined tilt angle α and rotating four times with 3.0×10^{13} cm of a dose quantity of boron (B_{11}) and 30 keV of ion implantation energy.

If the impurities are ion implanted with a tilted angle and rotations, the field stop layer **25** is expanded to the active area by distance X compared to the ion implantation without the tilt angle and the rotation. That is, the field stop layer formed through the ion implantation without the tilt angle and the rotation is merely allocated below the field oxide layer but is unable to penetrate to the active area.

Although an ion implantation mask for forming the field stop layer **25** uses the pad nitride layer **24**, it is also possible to use an additional ion implantation mask.

With reference to FIG. 5A, the field stop layer **25** is formed and penetrated from the area where the field oxide layer will be formed to the exposed p-type epi layer **22** by a distance X.

Referring to FIG. 4B, the surface of the p-type epi layer **22** where the field stop layer **25** is formed is oxidated so to grow the field oxide layer **26** on the field stop layer **25**. Thereafter, the pad nitride layer **24** and the pad oxide layer **23** are removed.

At this time, the active area defined by the field oxide layer **26** can be classified into a first active area ACT_1 having a wide area, a second active area ACT_2 having a relatively smaller area and width of an long and short axis and a third active area ACT_3 having a bottle-neck structure 'A' (referred to FIG. 5A).

Herein, the first active area ACT_1 is an area for providing the PD, and the second active area ACT_2 is an area for providing the FD. The third active area ACT_3 is an area for providing a channel ch of the transfer transistor T_x.

Hereinafter, the first active area ACT_1, the second active area ACT_2 and the third active area ACT_3 are referred as to the PD, the FD and the channel area ch, respectively.

Meanwhile, before forming the field oxide layer **26**, a p-well (not shown) is formed in a predetermined area of the p-type epi layer **22** as to include a drive transistor D_x and a select transistor S_x through a lateral expansion due to a subsequent thermal process.

Next, after removing the pad oxide layer **23**, a general transistor fabrication process for forming the drive transistor D_x and the select transistor S_x among 4 transistors of the unit pixel.

Also, another ion implantation process (not shown) for a threshold voltage control ion that controls a threshold voltage of the transistor in the p-well and a deep ion implantation process (not shown) for p-type impurities that controls a punchthrough property are proceeded. However, these ion implantation processes are not proceeded at the active area where the PD will be formed and the area where a source/drain, i.e., the FD of the transfer transistor T_x.

Referring to FIG. **4**C, a conductive layer for forming the gate electrode **27** of the four transistors of the unit pixel is deposited. Then, a photosensitive film is coated and patterned through a photo-exposure process and a developing process so as to form a photosensitive pattern (not shown) for forming the gate electrode **27**.

At this time, since a doping profile of the PD at one side of the transfer transistor T_x determines charge transfer efficiency, the gate electrode **27** is formed to have a sufficient thickness so that ion implantations of high energy n-type impurities for forming the PD and low energy p-type impurities can be aligned at the one side of the transfer transistor T_x.

Afterwards, the conductive layer is etched by using the photosensitive pattern for forming the PD as an etch mask so as to form the gate electrode **27** of the four transistors of the unit pixel. Herein, the gate electrode **27** is the gate electrode of the transfer transistor T_x.

At this time, the gate electrode **27** can increase highly a width of long axis **W1** overlapped with the active area where the PD will be formed since the third activation area ACT_3 located at a bottom of the gate electrode **27** has the bottle-neck structure (referred to FIG. **5**B).

Accordingly, in the transfer transistor T_x of which channel area ch have the bottle-neck structure, a width W of the transistor that determines major parameters such as a drain current (I_{dsat}) and a threshold voltage V_t is the width **W2** of short axis of the FD not that **W1** of long axis of the gate electrode **27** that is overlapped with the FD.

For instance, in case that currents are flowing from a path having a wide width to a path having a narrow width, the path having the narrow width determines a speed of the current flow. In other words, the path having the wide width is not related to the speed of the current flow.

Next, a photosensitive film is coated entirely on the structure including the gate electrode **27** and patterned selectively so as to form a first mask **28** for ion implanting a low concentration of the n-type impurities n^- with high energy.

At this time, one side of the first mask **28** is aligned to a center of the gate electrode **27** while the other side of the first mask **28** is aligned to a predetermined portion of the field oxide layer **26** without having any portion penetrates into the PD (referring to FIG. **5**B).

Afterwards, an n^- diffusion layer **29** is formed through the ion implantation of the low concentration of the n-type impurities n^- with high energy by using the first mask **28** as an ion implantation mask.

At this time, one side of the n^- diffusion layer **29** is aligned to an edge of one side of the gate electrode **27** while the other side of the n^- diffusion layer **29** is aligned to an edge of one side of the field stop layer **25**. That is, even if the ion implantation mask that opens a partial portion of the field oxide layer **26** is used, the n^- diffusion layer **29** is not contacted to the field oxide layer **26** due to the field stop layer **25** penetrated into the active area with the predetermined distance X.

In the end, the n– diffusion layer **29** is self-aligned due to the gate electrode **27** and the field stop layer **25** as simultaneously as being isolated electrically from the edge of the field oxide layer **26** due to the field stop layer **25**.

Also, both ends of the gate electrode **27** are expanded to cover sufficiently one side of the PD. Since the n^- diffusion layer **29** is self-aligned due to the field stop layer **25**, it is possible to apply a reticle for forming a conventional n^- diffusion layer without any modification.

As described above, if the n^- diffusion layer **29** is formed by using the reticle without any modification, it is possible to reduce costs for forming a new reticle and freely control a distance between the field oxide layer **26** and the n^- diffusion layer **29**. It is also possible to obtain a mask overlay margin due to the self-alignment of the n^- diffusion layer **29**.

In case of using the new reticle for forming the n^- diffusion layer **29**, it is difficult to control the distance between the field oxide layer **23** and the n^- diffusion layer **29**.

Referring to FIG. **5**B, the n^- diffusion layer **29** is self-aligned to the one side of the gate electrode **27** of which long axis becomes elongated. Meanwhile, the rest of sides of the n^- diffusion layer **29** except for the portion self-aligned to the one side of the gate electrode **27** are also self-aligned due to the field stop layer **25** and formed in the PD.

Therefore, since the n– diffusion layer **29** is self-aligned only to the one side of the gate electrode **27** instead of aligning to both ends of the long axis of the gate electrode **27**, it is possible to minimize a contact between corners of the n– diffusion layer **29** and the field oxide layer **26**. This contact is a cause for the dark current.

After removing the first mask **28**, an ion implantation process for forming a lightly doped drain (LDD) structure of the four transistors of the unit pixel is proceed (not shown). Firstly, a photosensitive film is coated on entire structure and patterned through a photo-exposure process and a developing process so as to form a second mask (not shown) for forming the LDD structure.

Referring to FIG. **4**D, the second mask (not shown) is removed, and an insulating layer for a spacer is deposited on the entire structure. Then, the insulating layer is proceeded with an etch-back process so to form a spacer **30** at lateral sides of the gate electrode **27**.

With use of a blanket ion implantation technique, low energy p-type impurities p^0 are ion implanted so that a p^0 diffusion layer **31** is formed on the n^- diffusion layer **29** and at the other side of the gate electrode **27** as simultaneously as on the exposed p-type epi layer **22**. At this time, p^0 diffusion layer **31** formed in the n^- diffusion layer **29** is aligned to the spacer **30** with a distance as much as a thickness the spacer **30**.

Meanwhile, the p^0 diffusion layer **31** is also formed on the p-type epi layer **22** exposed at the other side of the gate electrode **27** through the blanket ion implantation technique. However, this p^0 diffusion layer **31** does not have any specific effect since it uses the identical p-type impurities used for the p-type epi layer **22**.

Through the ion implantation of the low energy p-type impurities p^0, a shallow pn junction including the p^0 diffusion layer **31** and the n^- diffusion layer **29** and a pnp-type PD including the p-type epi layer **22**, the n^- diffusion layer **29** and the p^0 diffusion layer **31** are formed.

With reference to FIG. **5**C, which showing a plane view of the p^0 diffusion layer **31**, one side of the p^0 diffusion layer **31** is aligned to the spacer (not shown) while the rest of sides are self-aligned to the field stop layer **25**.

As shown in FIG. **4**E, a photosensitive film is coated on the entire structure and patterned through a photo-exposure process and a developing process so to form a third mask (not shown) for forming a source/drain area. Then, n-type impurities n^+ with a high concentration are ion implanted by using the third mask as an ion implantation mask so as to form an n^+ diffusion layer **32**. Herein, the n^+ diffusion layer **32** is the source/drain area (not shown) of the drive transistor D_x and the select transistor S_x and that of the transfer transistor T_x and the reset transistor R_x, i.e., the FD of the unit pixel.

Referring to FIG. **5**D, the third mask exposes the other side of the gate electrode **27** of the transfer transistor T_x and the FD near to the other side of the gate electrode **27** but is aligned at a center of the gate electrode **27**. That is, the ion implantation of the n-type impurities n^+ with a high concentration does not occur at the area for providing the PD.

FIG. **6** is a plane view of a CMOS image sensor in accordance with a second preferred embodiment of the present invention.

With reference to FIG. **6**, an active area including a substrate **41**, a PD formed on a predetermined portion of the substrate **41**, a FD having a relatively smaller area than the PD, a channel area ch having a bottle-neck structure connecting the PD and the FD is formed.

Then, a field oxide layer **46** for isolating electrically the active area is formed, and then a field stop layer **44**A having a wider area than the field oxide layer **46** by extended towards the PD with a first predetermined width is formed below the field oxide layer **46**.

That is, the field stop layer **44**A is extended only to the active area where the PD will be formed, and formed below the channel area ch and the FD.

A gate electrode **47** having one side supposed with a second predetermined width with an entire area of one side of the PD and the other side is aligned to the FD as simultaneously as covering the channel area ch is formed on the substrate **41**. Herein, the PD is connected to the channel area ch.

Meanwhile, the PD includes an n^- diffusion layer **48** formed through a self-alignment to the one side of the gate electrode **47** and the field stop layer **44**A and a p^0 diffusion layer **50** formed in the n^- diffusion layer **48** by being self-aligned to the field stop layer **44**A with a predetermined distance from the one side of the gate electrode **47**.

On the other side of the gate electrode **47**, a n^+ diffusion layer **51** is formed.

In the following second preferred embodiment, a method for proceeding an ion implantation process for forming the field stop layer by classifying the channel area of the transfer transistor T_x sensitive to a tilt angle and other areas with each different mask will be described.

FIGS. **7**A to **7**D are cross-sectional views illustrating a process for fabricating the CMOS image sensor with respect to an II-II' line of FIG. **6**.

Referring to FIG. **7**A, a p-type epi layer **42** is grown on a p^+ substrate **41** doped with a high concentration of p-type impurities. Subsequently, a first ion implantation mask **43** is formed on the p-type epi layer **42**.

At this time, the p-type epi layer **42** exposed by the first ion implantation mask **43** is an area where a field oxide layer allocated close to the PD is formed.

Next, impurities for forming a first field stop layer **44**A are ion implanted on the exposed p-type epi layer **42** by giving a tilt angle and rotations or twists.

At this time, the ion implantation for forming the first field stop layer **44**A is proceeded with a predetermined tilt angle α and 4 times of rotations by using 3.0×10^{13} cm^{-3} of a dose quantity of boron (B_{11}) and 30 keV of ion implantation energy.

As described above, if the impurities are ion implanted with the tilt angle and the rotations, the first field stop layer **44**A has an increased overlapping distance X with the active area compared to the ion implantation without any tilt angle and the rotation.

With reference to FIG. **6**, which is a plane view of the first field stop layer **44**A, the field stop layer **44**A is formed with a distance X penetrated into the PD from the area where the field oxide layer will be formed.

Referring to FIG. **7**B, after removing the first ion implantation mask **43**, a second ion implantation mask **45** is formed entirely on the above structure. At this time, the p-type epi layer **42** exposed by the second ion implantation mask **45** is an area where the field oxide layer near to the channel area ch of the transfer transistor T_x.

Next, impurities for forming a second field stop layer **44**B are ion implanted on the exposed p-type epi layer r**42** without any tilt angle.

At this time, the ion implantation for forming the second field stop layer **44**B is proceeded with 3.0×10^{13} cm^{-3} of a dose quantity of boron (B11) and 30 keV of ion implantation energy.

In case that the impurities are ion implanted without the tilt angle, the first field stop layer **44**A is not overlapped with the active area. Thus, this case does not appear in FIG. **6**.

Meanwhile, the first ion implantation mask **43** and the second ion implantation mask **45** uses the identical pad oxide layer and the pad nitride layer for a LOCOS process explained in the first preferred embodiment. However, the first and the second ion implantation masks **43** and **45** uses each different reticles.

In other words, the pad oxide layer and the pad nitride layer are simultaneously patterned to expose a portion of the p-type epi layer **42** where the first field stop layer **44**A will be formed. Subsequently, an ion implantation for forming the first field stop layer **44**A is proceeded. In continuous to the ion implantation for the first field stop layer **44**A, the rest of the p-type epi layer **42** except for the portion for the first field stop layer **44**A are exposed, and another ion implantation for forming the second field stop layer **44**B is proceeded.

With reference to FIG. **7**C, the surface of the p-type epi layer **42** for providing the first and the second field stop layers **44**A and **44**B are oxidated, and then grow the field oxide layer **46** on the first and the second field stop layer **44**A and **44**B.

Herein, the first field stop layer **44**A penetrated to the active area for providing the PD with a predetermined distance X isolates electrically the active area and the field oxide layer **46**. However, this first field stop layer **44**A does not isolate electrically the active area for providing the channel area ch of the transfer transistor T_x and a bottom part of the field oxide layer closed to the active area for the channel area ch.

All process for forming a subsequent gate electrode including an n^- diffusion layer and a p^0 diffusion layer are identical to the processes described in the first preferred embodiment.

Referring to FIG. 7D, a gate electrode **47** of four transistors is formed on the p-type epi layer **42**. Herein, the gate electrode **47** shown in FIG. 7D is the gate electrode of the transfer transistor T_x.

At this time, since the gate electrode **47** has a bottle-neck structure at a bottom part, it is possible to highly increase a width **W1** of a long axis superposed on the active area for providing the PD.

Therefore, with respect to the transfer transistor T_x of which channel area has the bottle-neck structure, a width of the transistor that determines major parameters such as a drain current (I_{dsat}) and a threshold voltage (V_t) is the width **W2** of a short axis of the FD not the width **W1** of the long axis of the gate electrode **47**.

Next, a low concentration of n-type impurities n^- are ion implanted by using an ion implantation mask of which one side is aligned to a center of the gate electrode **47** and the other side is aligned to a predetermined portion of the field oxide layer **46** without having portions penetrated into the PD so as to form an n^- diffusion layer **48**.

After forming a LDD structure, an insulating layer for a spacer is deposited on the above entire structure. The insulating layer is then proceeded with an etch-back process so to form a spacer **49** contacting to both lateral sides of the gate electrode **47**.

Through the blanket ion implantation technique, low energy p-type impurities p^0 are ion implanted so that a p^0 diffusion layer **50** is formed on the n^- diffusion layer **48** and simultaneously on the p-type epi layer **42** exposed at the other side of the gate electrode **47**. At this time, the p^0 diffusion layer **50** formed in the n^- diffusion layer **48** is aligned to the spacer **49** with a distance as same as a thickness of the spacer **49**.

A shallow pn junction including the p^0 diffusion layer **50** and the n^- diffusion layer **48** is formed through the ion implantation of the low energy p-type impurities p^0. Also, a pnp-type PD including the p-type epi layer **42**, the n^- diffusion layer **48** and the p^0 diffusion layer **50** is formed.

Next, a high concentration of n-type impurities n^+ are ion implanted through the use of an ion implantation mask that exposes the p-type epi layer **42** where an n^+ diffusion layer will be formed so as to form an n^+ diffusion layer **51**. The n^+ diffusion layer **51** is a source/drain area (not shown) of a drive transistor D_x and a select transistor S_x and a source/drain area of the transfer transistor T_x and a reset transistor R_x, i.e., the FD.

The first and the second preferred embodiments can be used not only in a process for fabricating the CMOS image sensor but also in other processes applicable for controlling the dark current of a charge coupled device (CCD).

The present invention provides an effect of fabricating the CMOS image sensor with high immunity against the dark current.

When proceeding the ion implantation process for forming the deep n^- diffusion layer constituting the PD, it is possible to improve a process margin since a dark current elimination structure capable of an self-alignment is applied.

Also, instead of fixing a distance between the n^- diffusion layer and the field oxide layer with a reticle, the distance is variable in accordance with a tilt angle during the formation of the n^- diffusion layer, thereby providing an effect of easily controlling optical characteristics of the CMOS image sensor.

While the present invention has been described with respect to certain preferred embodiments, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the scope of the invention as defined in the following claims.

What is claimed is:

1. An image sensor, comprising:

a semiconductor substrate;

an active area including a photodiode area formed in a predetermined position of the substrate, a floating diffusion area having a smaller area than the photodiode area and a channel area having a bottle-neck structure connecting to the photodiode area and the floating diffusion area;

a field area for isolating electrically the active area;

a field stop layer being formed beneath the field area and being wider than the field area in a direction towards the active area; and

a gate electrode formed on the substrate by covering the channel area and a portion of the photodiode contacted to the channel area.

2. The image sensor as recited in claim **1**, wherein the photodiode area further includes:

a first diffusion layer formed in the photodiode area by being aligned to one side of the gate electrode and the field stop layer; and

a second diffusion layer formed in the first diffusion layer being aligned to the field stop layer with a predetermined distance from the one side of the gate electrode.

3. The image sensor as recited in claim **1**, wherein the gate electrode is aligned to the floating diffusion area.

4. An image sensor, comprising:

a substrate;

an active area including a photodiode area formed in a predetermined position of the substrate, a floating diffusion area having a smaller area than the photodiode area and a channel area having a bottle-neck structure connecting to the photodiode area and the floating diffusion area;

a field area for isolating electrically the active area;

a field stop layer being formed beneath the field area and being wider than the field area in a direction towards the active area; and

a gate electrode formed on the substrate by covering the channel area and a portion of the photodiode contacted to the channel area.

5. A method for fabricating an image sensor, comprising the steps of:

forming an isolation mask that exposes partially a surface of a substrate;

forming a first diffusion layer having a wider area than an area of the partially exposed substrate;

forming a field oxide layer having a smaller area than the first diffusion layer on the first diffusion layer;

forming a gate electrode on an active area of the substrate defined by the, field oxide layer;

forming a second diffusion layer being aligned to an edge of one side of the gate electrode in the substrate and to the first diffusion layer; and

forming a third diffusion layer being aligned with a predetermined distance from the edge of the one side of the gate electrode formed in the second diffusion layer.

6. The method as recited in claim **5**, wherein the step of forming the first diffusion layer is proceeded with an ion implantation that gives impurities a plurality of rotations or twists with a predetermined tilt angle.

7. The method as recited in claim **5**, wherein the active area of the substrate defined by the field oxide layer includes a photodiode area, a floating diffusion area having a smaller area than the photodiode area and a channel area having a bottle-neck structure connecting the photodiode area and the floating diffusion area,

wherein the gate electrode has one entire side of the floating diffusion area.

8. A method for forming an image sensor, comprising the steps of:

forming a first isolation mask that exposes a portion of a surface of one side of a substrate;

forming a first diffusion layer having a wider area than an exposed area of the substrate;

forming on the substrate a second isolation mask that exposes the other side of the substrate;

forming a second diffusion layer having an area identical to an exposed area of the substrate;

forming on the first diffusion layer a first field oxide layer having a smaller area than the first diffusion layer, and simultaneously forming on the second diffusion layer a second field oxide layer having an area identical to the second diffusion layer;

forming a gate electrode extending on the active area of the substrate and simultaneously on the second field oxide layer;

forming a third diffusion layer being aligned to an edge of one side of the gate electrode in the substrate and the first diffusion layer; and

forming a fourth diffusion layer being aligned with a predetermined distance from the edge of the one side of gate electrode in the third diffusion layer.

9. The method as recited in claim **8**, wherein the step of forming the first diffusion layer is proceeded with an ion implantation that gives impurities a plurality of rotations or twists with a predetermined tilt angle.

10. The method as recited in claim **8**, wherein the step of forming the second diffusion layer is proceeded with an ion implantation that implants impurities vertically.

* * * * *

EXHIBIT F

US007365298B2

(12) **United States Patent**
Ryu

(10) **Patent No.: US 7,365,298 B2**
(45) **Date of Patent: Apr. 29, 2008**

(54) **IMAGE SENSOR AND METHOD FOR MANUFACTURING THE SAME**

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(73) Assignee: **Hynix Semiconductor Inc.**, Kyungki-do (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 219 days.

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(22) Filed: **Sep. 20, 2004**

(65) **Prior Publication Data**

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(30) **Foreign Application Priority Data**

Sep. 29, 2003 (KR) 10-2003-0067561

(51) **Int. Cl.**
H01L 21/77 (2006.01)

(52) **U.S. Cl.** **250/208.1**; 250/226; 257/294; 438/70; 438/57

(58) **Field of Classification Search** 250/208.1, 250/226; 257/294, 223, 225, 215; 438/70, 438/57, 69, 73
See application file for complete search history.

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Assistant Examiner—Tony Ko
(74) *Attorney, Agent, or Firm*—Marshall Gerstein & Borun LLP

(57) **ABSTRACT**

The present invention discloses an image sensor and a method for manufacturing the same which is capable of increasing the light-collection efficiency of a photodiode. The image sensor comprises: at least one photodiode formed on a semiconductor substrate; multilayer interlayer insulating films formed on the photodiode and stacked in at least two layers so that the density of the upper interlayer insulating film becomes lower than that of the lower interlayer insulating film as the multilayer interlayer insulating films proceed upward; a light shield layer and an element-protecting film sequentially stacked on the multilayer interlayer insulating film; color filter arrays and a flattening layer sequentially stacked on the element-protecting film; and microlenses arranged on the positions corresponding to the color filters on the flattening layer. Therefore, the light-collection efficiency of the photodiode can be increased with an increased transmittance of a vertical light reaching to the photodiode by making the multilayer interlayer insulating films have a lower density as they proceed upward to decrease the refraction angle of the incident light penetrated through the microlenses and color filters.

12 Claims, 4 Drawing Sheets

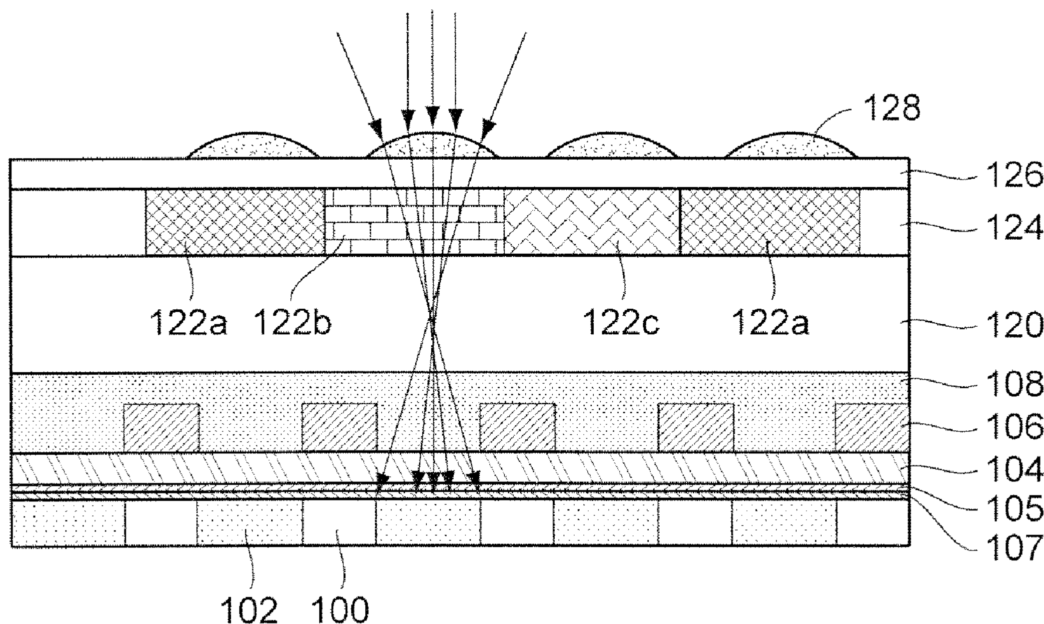


FIG. 1
(PRIOR ART)

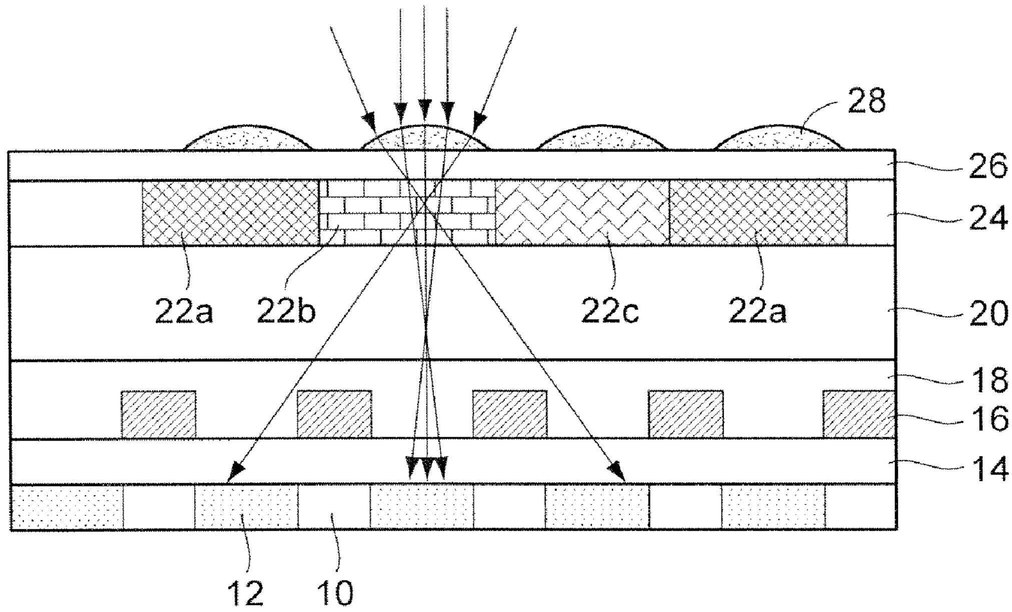


FIG. 2

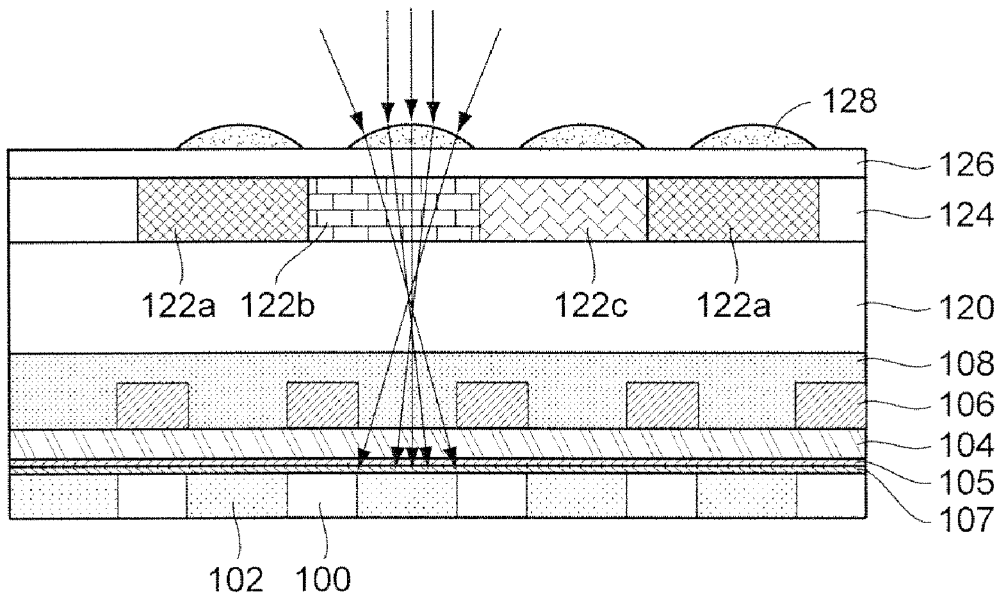


FIG.3a

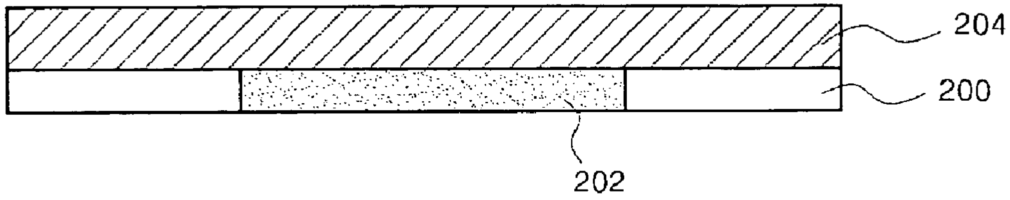


FIG.3b

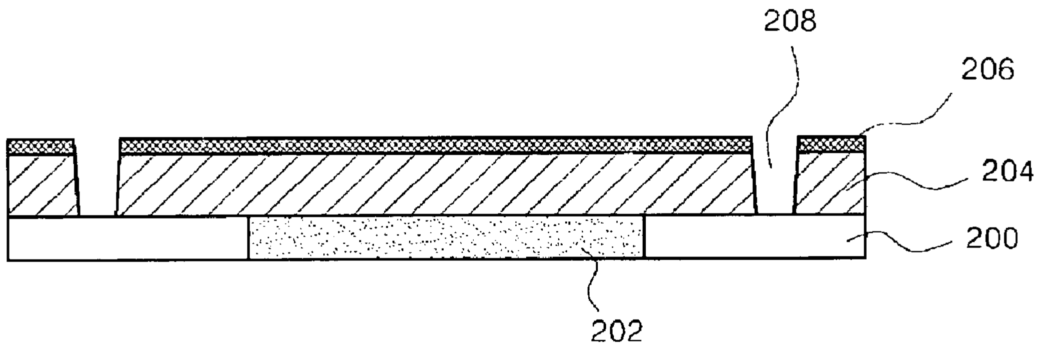


FIG.3c

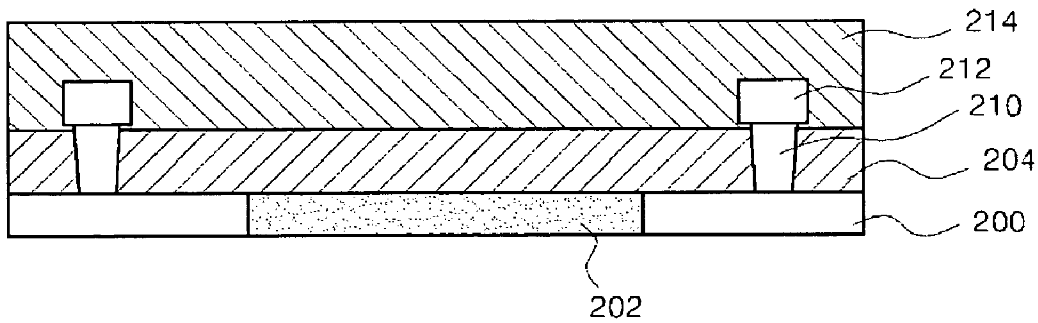


FIG.3d

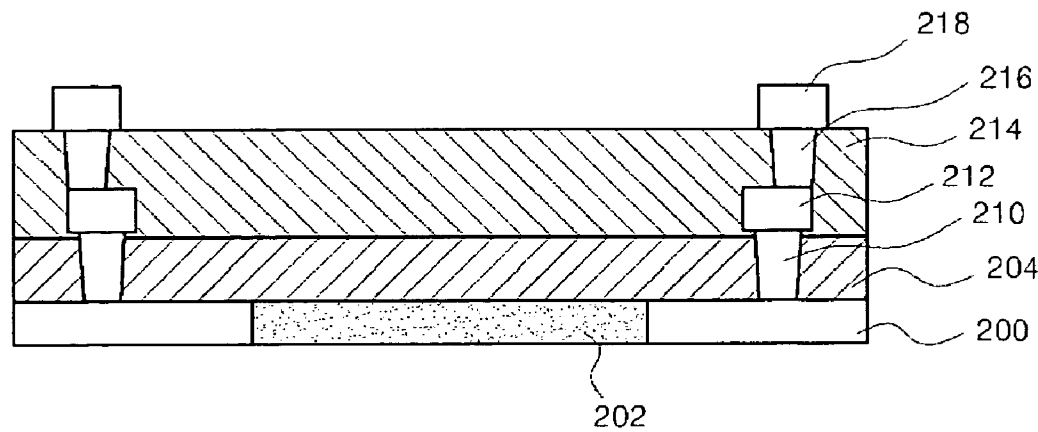


FIG.3e

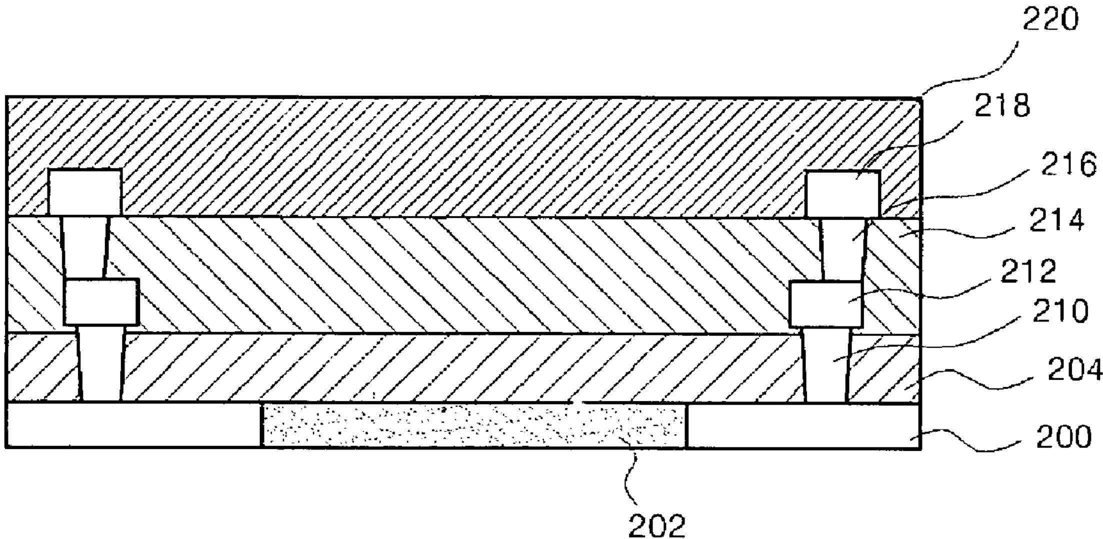


FIG.3f

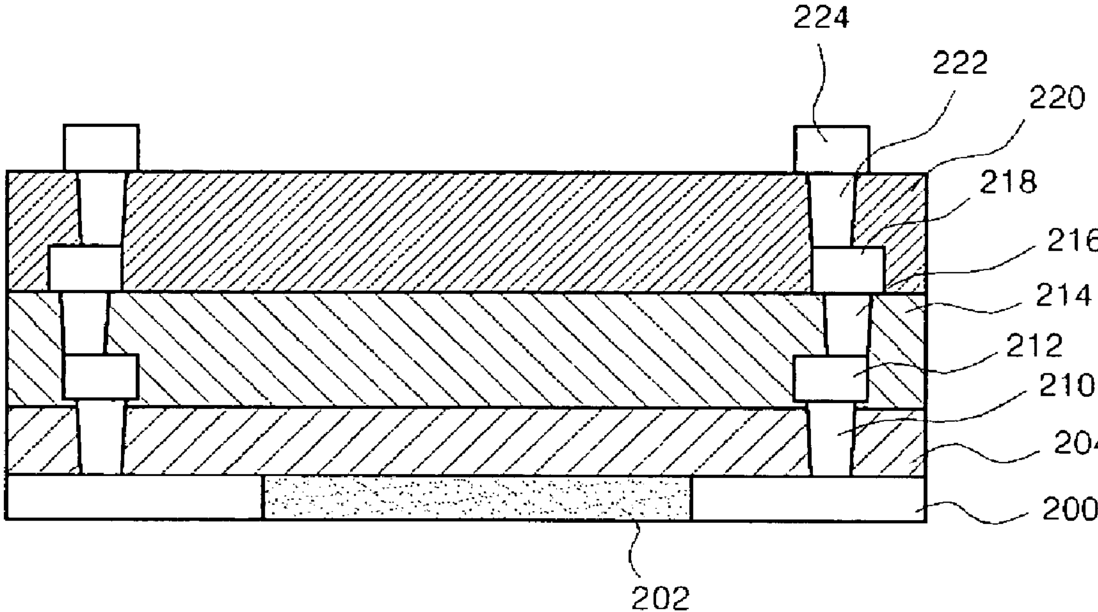


FIG.3g

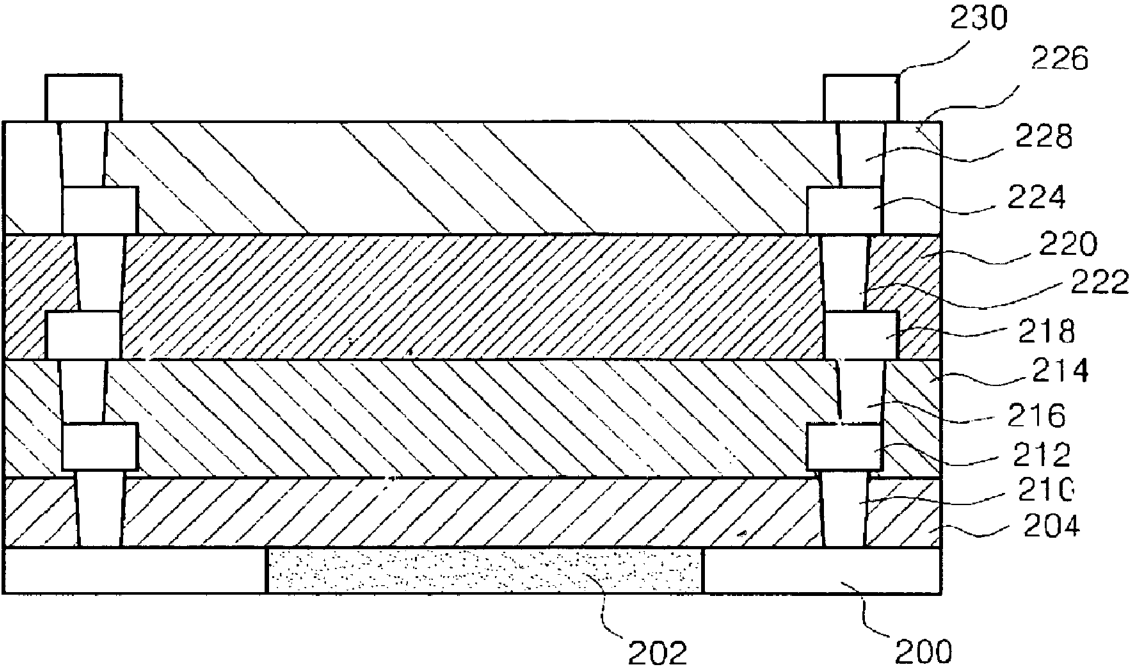


FIG.4

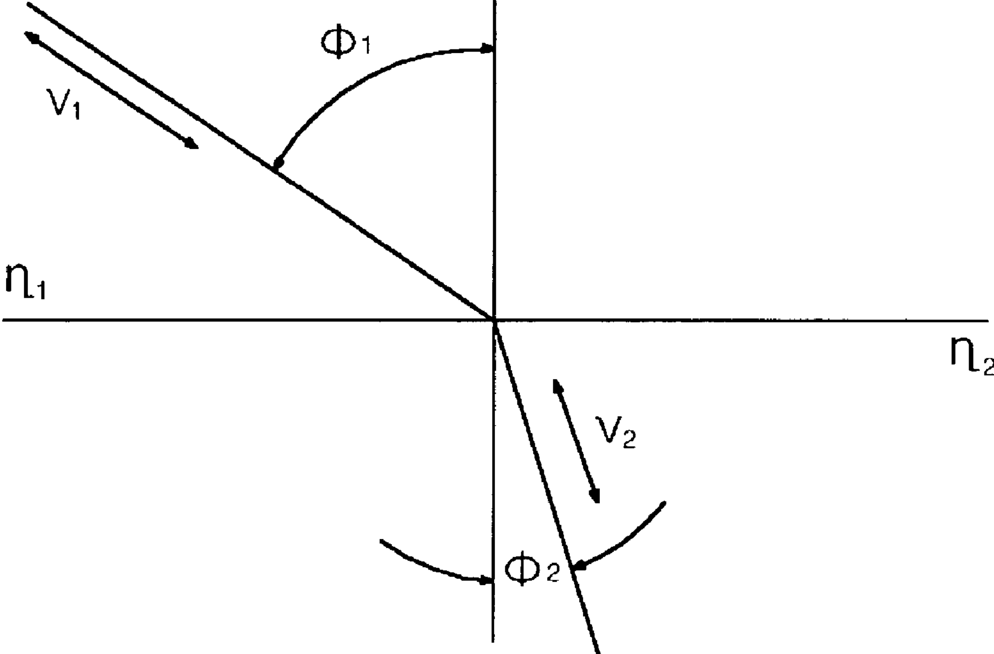


IMAGE SENSOR AND METHOD FOR MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an image sensor and a method for manufacturing the same, and more particularly, to an image sensor, which is capable of increasing the light-collection efficiency of a photodiode, and a method for manufacturing the same.

2. Description of the Related Art

Generally, an image sensor is a semiconductor device that converts an optical image into an electric signal. Among the image sensors, a charge coupled device (CCD) is a device wherein each metal-oxide-silicon (hereinafter referred as to MOS) capacitor is closely located and charge carriers are stored into the MOS capacitor and transferred. A complementary metal oxide semiconductor (hereinafter referred as to CMOS) image sensor employs CMOS technology that uses a control circuit and a signal processing circuit as peripheral circuits to form as many arrays of MOS transistors as the number of pixels, and adopts a switching mode that detects outputs sequentially. MOS transistors formed in the peripheral circuit as the same number of pixels.

In manufacturing such a variety of image sensors, there have been many endeavors to increase the photosensitivity of the image sensor. Among those endeavors to increase the photosensitivity, a light-collecting technique is the most important technique.

The image sensor generally includes photosensitive circuit parts sensing light and CMOS logic circuit parts transforming the light into electric signals and generating data. Recently, there have been many studies of light-collecting techniques by which the pathways of the incident lights injecting to the regions other than the photosensitive circuit parts are changed and collected in photodiodes that are photosensitive elements.

FIG. **1** is a cross sectional view showing an image sensor in accordance with a prior art, in which the main components of a conventional CMOS image sensor are directly related to light-collection are illustrated.

Referring to FIG. **1**, the prior art image sensor includes a plurality of field insulating films **10** formed on a semiconductor substrate (not shown), at least one photodiode **12** which is an optical active region formed between these field insulating films **10**, multilayer interlayer insulating films **14** and **18** insulating between layers of the top parts of the field insulating films **10** and photodiode **12** and a light shield layer **16** formed of metal or the like in the interlayer insulating film **18** in order to prevent incident light from being focused onto the field insulating films **10**. An element-protecting film **20** is formed on the interlayer insulating film **18**, and an interlayer insulating film **24** is formed on the element-protecting film **20**. The color filter arrays **22***a*, **22***b* and **22***c* of red, green and blue are formed in the interlayer insulating film **24**. A flattening layer **26** is formed over these color filter arrays **22***a*, **22***b* and **22***c*. Microlenses **28** are formed at the positions corresponding to the color filters **22***a*, **22***b* and **22***c*.

As the materials of the color filters **22***a*, **22***b* and **22***c* of red, green and blue, mainly used are photoresists dyed in colors capable of absorbing only the light of a specific wavelength. As the materials of the microlenses **28**, mainly used are polymer type resins.

The interlayer insulating films **14**, **18** and **24** and the element-protecting film **20** are typically made by using silicon oxide films that are transparent insulating materials.

The flattening layer **26** is made by using a photoresist in order to compensate for the roughness of the color filters.

In the constructed conventional CMOS image sensor, the incident light received via the microlenses **28** is separated into corresponding red, green and blue light through the red color filter **22***a*, green color filter **22***b* and blue color filter **22***c*. The separated red, green and blue lights are focused on the photodiode **12** at the positions corresponding to the color filters through the element-protecting film **20** and the interlayer insulating films **14** and **18**, respectively. The light shield layer **16** arranged between the interlayer insulating films **14** and **18** plays the role of shielding the incident light so as not to deviate to other light pathways.

However, if the incident light on the photodiode through the microlenses **28** and the color filters **22***a*, **22***b* and **22***c* is not focused in parallel but focused to other light pathways, the photodiode **12** in the corresponding light pathway will be unable to sense the light or interference will occur with other adjacent photodiode **12**. Such a phenomenon acts as noise in embodying a high performance image in a CMOS image sensor.

SUMMARY OF THE INVENTION

The present invention is designed in consideration of the problems of the prior art, and therefore it is an object of the present invention to provide an image sensor which can improve the light-collection efficiency of the photodiode with an increased transmittance of vertical light reaching the photodiode by making the multi-layer interlayer insulating films have a lower density as they proceed upward to decrease the refraction angle of the incident light penetrated through the microlenses and color filters, and a method for manufacturing the same.

To achieve the above object, there is provided an image sensor in accordance with the present invention, comprising: at least one photodiode formed on a semiconductor substrate; multi-layer interlayer insulating films formed on the photodiode and stacked in at least two layers so that the density of the upper interlayer insulating film becomes lower than that of the lower interlayer insulating film as the multi-layer interlayer insulating films proceed upward; a light shield layer and an element-protecting film sequentially stacked on the multi-layer interlayer insulating film; color filter arrays and a flattening layer sequentially stacked on the element-protecting film; and microlenses arranged on the positions corresponding to the color filters on the flattening layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and aspects of the present invention will become apparent from the following description of embodiments with reference to the accompanying drawings in which:

FIG. **1** is a cross sectional view showing an image sensor in accordance with a prior art;

FIG. **2** is a cross sectional view showing the structure of an image sensor in accordance with the present invention;

FIGS. **3***a* to **3***g* are process views showing a process for manufacturing multi-layer wiring in multi-interlayer insulating films of the image sensor in accordance with the present invention; and

FIG. **4** is a view for explaining the difference of the index of refraction caused by a density difference in the multi-layer interlayer insulating film of the image sensor in accordance with the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Hereinafter, a preferred embodiment of the present invention will be described in more detail referring to the drawings.

FIG. **2** is a cross sectional view showing the structure of an image sensor in accordance with the present invention, in which the main components of the CMOS image sensor of this invention directly related to light-collection are illustrated.

Referring to FIG. **2**, the CMOS image sensor of this invention includes a plurality of field insulating films **100** formed on a semiconductor substrate (not shown), at least one photodiode **102** which is an optical active region formed between these field insulating films **100**, multi-layer interlayer insulating films **104** and **108** insulating between layers of the top parts of the field insulating films **100** and photodiode **102** and being stacked in at least two layers so that the density is lower in upper parts than lower parts and a light shield layer **106** formed of metal or the like in the interlayer insulating film **108** in order to prevent an incident light from being focused onto the field insulating films **100**.

An element-protecting film **120** is formed on the interlayer insulating film **108**, and an interlayer insulating film **124** is formed on the element-protecting film **120**. The color filter arrays **122***a*, **122***b* and **122***c* of red, green and blue are formed in the interlayer insulating film **124**. A flattening layer **116** is formed over these color filter arrays **122***a*, **122***b* and **122***c*. Microlenses **128** are formed on the positions corresponding to the color filters **122***a*, **122***b* and **122***c*.

As the materials of the color filters **122***a*, **122***b* and **122***c* of red, green and blue, mainly used are photoresists dyed in colors capable of absorbing only the light of a specific wavelength. As the materials of the microlenses **128**, mainly used are polymer type resins. At this time, the interlayer insulating films **104** and **108** below the color filter arrays **122***a*, **122***b* and **122***c* are made so that the density of the interlayer insulating film in the upper side is lower than that of the interlayer insulating film in the lower side. For this, in the present invention, the density of an oxide film becomes higher in the order of PE-CVD<HDP-CVD<LP-CVD<thermal oxidation. Further, if the deposition temperature is lowered, the density of the oxide film is lowered. Accordingly, it is possible to carry out a density adjustment by this deposition process and by the adjustment of the deposition temperature. For example, in the manufacture of the interlayer insulating film **108** in the upper side, an oxide film is deposited by PE-CVD or HDP-CDP and in a low temperature range. On the contrary, in the manufacture of the interlayer insulating film **104** in the lower side, an oxide film is deposited by LP-CVD or a thermal oxidization process and deposited in the range of a higher temperature in comparison with the interlayer insulating film in the upper side. Also, it is possible to adjust the density of the upper interlayer insulating film **108** to be lower than that of the lower interlayer insulating film **104** by adjusting the deposition temperature while carrying out the same deposition process to all of the upper and lower interlayer insulating films **108** and **104**.

In the present invention, the interlayer insulating films **104** and **108** are transparent insulating materials and typically formed of silicon oxide films. At this time, the density can be lowered by increasing the concentration of impurities to be doped in the upper interlayer insulating film than in the lower interlayer insulating film. For example, if the interlayer insulating film **104** in the lower position is deposited

with FSG, BPSG, PSG and BSG and the interlayer insulating film **108** in the upper position is deposited with USG, the density of the interlayer insulating film in the upper position becomes lower than that of the interlayer insulating film in the lower position.

The element-protecting film **120** is typically formed of a silicon oxide film that is a transparent insulating material, and the flattening layer **116** is formed of a photoresist in order to compensate for the roughness of the color filters.

In the CMOS image sensor of the above-described structure of the present invention, the incident light received via the microlenses **128** are separated into the corresponding red light, green light and blue light through the red color filter **122***a*, green color filter **122***b* and blue color filter **122***c*. The separated red, green and blue lights are focused on the photodiode **102** at the positions corresponding to the color filters through the element-protecting film **120** and the interlayer insulating films **108** and **104**. The light shield layer **106** arranged between the interlayer insulating films **104** and **108** plays a role of shielding the incident light so as not to deviate to other light pathways.

Further, according to the present invention, in the multi-layer interlayer insulating films **104** and **108** included in the CMOS image sensor, the density of the interlayer insulating film **108** in the upper position is lower than that of the interlayer insulating film **104** in the lower position. Due to this, the red, green and blue lights penetrated through the microlenses **128** and the color filters **122***a*, **122***b* and **122***c* are focused on the photodiode **102** in vertical light pathways without a light loss as the refraction angle on those interlayer insulating films **108** and **104** decreases until the incident lights are focused on the photodiode **102**. The light shield layer **106** arranged between the interlayer insulating films **108** and **104** plays a role of shielding the incident lights so as not to deviate to other light pathways.

As shown, in the present invention, a borderless contact or a photosensitivity adjusting film **105** is also formed of a silicon oxide film or the like below the multi-layer interlayer insulating films **104** and **108**. Also, a buffer insulating film **107** may be additionally formed of a silicon oxide film below the photosensitivity adjusting film.

Next, the process for manufacturing the thus constructed CMOS image sensor in accordance with the present invention will be described.

First, in order to insulate elements of the CMOS image sensor electrically, a field insulating film **100** is formed on a silicon substrate (not shown) and at least one photodiode **102** is formed in the gaps of the field insulating film **100**.

Next, an upper interlayer insulating film **104** having a large density is deposited on the entire surface of the field insulating film **100** and photodiode **102**, and a light shield layer **106** of metal or the like is formed thereon.

Continually, an upper interlayer insulating film **108** flattened and having a low density is formed over the entire surface of the lower interlayer insulating film **104** on which the light shield layer **106** is formed. Here, the adjusting processes of the deposition temperature and the impurity concentration in the deposition process for adjusting the density difference between the lower interlayer insulating film **104** and the upper interlayer insulating film **108** have been described above, the description thereof will be omitted.

Next, in order to protect the elements from moisture or scratching, a flattened element-protecting film **120** is formed on the entire surface of the upper interlayer insulating film **108**.

Then, a photoresist dyed in red, green and blue is applied onto the flattened element-protecting film **120** and developed, to form arrays of color filters **122***a*, **122***b* and **122***c* of red, green and blue, and then form a flattened interlayer insulating film **124** on the sides of the color filter arrays **122***a*, **122***b* and **122***c*. On the entire surface of the resultant material, a flattening layer **116** for flattening and adjusting the focal distance is formed. Next, microlenses **128** are formed on the flattening layer **116** at the positions corresponding to the red, green and blue color filters **122***a*, **122***b* and **122***c*.

FIGS. **3***a* to **3***g* are views showing a process for manufacturing multi-layer wiring in multi-layer interlayer insulating films of the image sensor in accordance with the present invention.

First, as shown in FIG. **3***a*, a field insulating film **200** for electrically insulating elements of a CMOS image sensor formed on a semiconductor substrate (not shown), and at least one photodiode **202** is formed in the gaps of the interlayer insulating film **200**. Next, a BPSG having a high rate of flow is deposited at 2000 to 15000 Å on the field insulating film **200** and photodiode **202**, and its surfaces are polished by chemical mechanical polishing (CMP) to thus forming a first interlayer insulating film **204** of 2000 to 9000 Å and then flatten it.

Next, as shown in FIG. **3***b*, HDP-USG is deposited at 300 to 9000 Å to form a second interlayer insulating film **206** having a high density. Then, the second and first interlayer insulating films **206** and **204** are etched to form contact holes **208**.

Continually, glue layer/barrier metal layer (not shown) such as Ti/TiN are deposited on the contact holes **208**. As shown in FIG. **3***c*, metal such as tungsten, etc. is buried and patterned to form first contacts **210** and metal wires **212**. Next, HDP-FSG is deposited at 9000 to 40000 Å to form a third interlayer insulating film **214** having a lower density than the second interlayer insulating film **206** and flatten the surface thereof by CMP.

Next, as shown in FIG. **3***d*, via holes are formed on the third interlayer insulating film **214** and tungsten plugs **216** and second metal wires **218** connected to the first metal wires **212** in the lower position are formed in the via holes.

Continually, as shown in FIG. **3***e*, PE-USG is deposited at 3000 to 8000 Å to form a fourth interlayer insulating film **220** having a lower density than the third interlayer insulating film **214** and flatten the surface thereof by CMP.

Continually, as shown in FIG. **3***f*, via holes are formed on the fourth interlayer insulating film **220** and tungsten plugs **222** and second metal wires **224** connected to the second metal wires **218** in the lower position are formed in the via holes.

Next, as shown in FIG. **3***g*, PE-FSG is deposited at 500 to 20000 Å to form a fifth interlayer insulating film **226** having a lower density than the fourth interlayer insulating film **220** and flatten the surface thereof by CMP. Afterwards, tungsten plugs **228** and fourth metal wires **230** connected to the third metal wires **224** in the upper position are formed in the fifth interlayer insulating film **226**.

As seen above, in the multi-layer interlayer insulating films of the CMOS image sensor of FIG. **2** and in the multi-layer interlayer insulating films having multi-layer metal wirings of FIGS. **3***a* to **3***g*, the density of the interlayer insulating film is lower in the upper position than in the lower position, thus making it possible to lower the refraction angle of an incident light.

FIG. **4** is a view for explaining the difference of the index of refraction caused by a density difference in the multi-layer interlayer insulating film of the image sensor in accordance with the present invention. In this drawing, the density is $n1<n2$ and has a size of $\Phi 1$(incident angle)>$\Phi 2$(refraction angle). Herein, the incident light injected to a medium **n2** having a high density from a medium **n1** having a low density has a refraction angle $\Phi 2$ smaller than the incident angle $\Phi 1$.

Subsequently, in the multi-layer interlayer insulating film of the present invention, the density of the interlayer insulating film in the upper position is lower than that of the interlayer insulating film in the lower position. Resultantly, since the density of the interlayer insulating film in the upper position becomes lower than that of the interlayer insulating film in the lower position as the multi-layer interlayer insulating films proceed upward, the refraction angle of the incident light becomes smaller and smaller. Due to this, while the light penetrated through the microlenses and color filters reaches the photodiode in a lower position, the refraction angle becomes smaller and smaller by the multi-layer interlayer insulating film whose density difference gradually increases, and thereby the light is not refracted to other light pathways but reaches the photodiode at a right angle.

As described above, the present invention can improve the light-collection efficiency of the photodiode with an increased transmittance of a vertical light reaching to the photodiode by making the multi-layer interlayer insulating films have a lower density as they proceed upward to decrease the refraction angle of the incident light penetrated through the microlenses and color filters. Accordingly, the optical properties of the image sensor can be enhanced because the loss of the light as being refracted to other light pathways can be minimized.

While the present invention has been described with respect to certain preferred embodiment only, other modifications and variations may be made without departing from the spirit and scope of the present invention as set forth in the following claims

What is claimed is:

1. An image sensor, comprising:

at least one photodiode formed on a semiconductor substrate;

multi-layer interlayer insulating films formed on the photodiode and stacked in at least two layers of oxide film having different density and the refractive index so that the density and the refractive index of the upper interlayer insulating film becomes lower than that of the lower interlayer insulating film as the multi-layer interlayer insulating films proceed upward;

a light shield layer and an element-protecting film sequentially stacked on the multi-layer interlayer insulating film;

color filter arrays and a flattening layer sequentially stacked on the element-protecting film; and

microlenses arranged on the positions corresponding to the color filters on the flattening layer.

2. The image sensor of claim **1**, wherein the density of the oxide films becomes higher in the order of PE-CVD<HDP-CVD<LP-CVD<thermal oxidations.

3. The image sensor of claim **1**, multi-layer wiring is vertically formed on the multi-layer interlayer insulating films, the element-protecting film and the flattening layer.

4. The image sensor of claim **1**, further comprising a photosensitivity adjusting film formed below the multi-layer interlayer insulating films.

5. The image sensor of claim **4**, further comprising a buffer insulating film formed below the photosensitivity adjusting film.

6. A method for manufacturing an image sensor, comprising the steps of:

making at least one photodiode on a semiconductor substrate;

forming on the photodiode multi-layer interlayer insulating films stacked in at least two layers of oxide film having different density and the refractive index so that the density and the refractive index of the upper interlayer insulating film becomes lower than that of the lower interlayer insulating film as the multi-layer interlayer insulating films proceed upward;

forming a light shield layer and an element-protecting film sequentially stacked on the multi-layer interlayer insulating film;

forming color filter arrays and a flattening layer sequentially stacked on the element-protecting film; and

forming microlenses arranged on the positions corresponding to the color filters on the flattening layer.

7. The method of claim **6**, wherein the density of the oxide films becomes higher in the order of PE-CVD<HDP-CVD<LP-CVD<thermal oxidation.

8. The method of claim **7**, wherein the density of the upper interlayer insulating film becomes lower than that of the

lower interlayer insulating film by adjusting the deposition process, the deposition temperature and the concentration of impurities doped on the interlayer insulating films.

9. The method of claim **6**, wherein the multi-layer interlayer insulating films are formed of oxides and the density is lowered by making the concentration of impurities to be doped higher in the upper interlayer insulating film than in the lower interlayer insulating film.

10. The method of claim **6**, further comprising the step of forming multi-layer wiring in the step of forming the multi-layer interlayer insulating films, the element-protecting film and the flattening layer.

11. The method of claim **6**, further comprising the step of forming a photosensitivity adjusting film below the multi-layer interlayer insulating films.

12. The method of claim **11**, further comprising the step of forming a buffer insulating film below the photosensitivity adjusting film.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

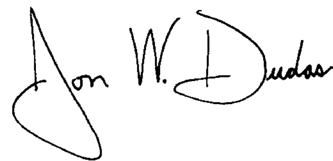
PATENT NO. : 7,365,298 B2
APPLICATION NO. : 10/945182
DATED : April 29, 2008
INVENTOR(S) : Sang Wook Ryu

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

At Column 6, line 58, “oxidations” should be -- oxidation --.

Signed and Sealed this

Second Day of September, 2008



JON W. DUDAS
Director of the United States Patent and Trademark Office