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*~~pro~~ *hac vice* application to be filed

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JCS

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

STMICROELECTRONICS, INC.,

Plaintiff,

vs.

INVENSENSE, INC.,

Defendant.

CASE NO. C 13 1116

COMPLAINT FOR PATENT INFRINGEMENT

DEMAND FOR JURY TRIAL

Plaintiff STMicroelectronics, Inc. ("STI") alleges for its complaint against Defendant InvenSense, Inc. ("InvenSense") as follows:

INTRODUCTION

1. This is an action for patent infringement brought before this Court pursuant to 28 U.S.C. §§ 1331 and 1338(a). STI seeks remedies for InvenSense's infringement of one or more claims of each of United States Patents Nos. 6,370,954 (the "'954 patent") and 6,034,419 (the "'419 patent") (collectively, "the Asserted Patents"). True and correct copies of the Asserted Patents are attached hereto as Exhibits A and B.

PARTIES

2. STMicroelectronics, Inc. is a corporation organized and existing under the laws of the State of Delaware, having its corporate headquarters and principal place of business at 750 Canyon Drive, Coppell, Texas 75019. STI is a subsidiary of STMicroelectronics NV, a Netherlands corporation, and does business in the Northern District of California. STI, STMicroelectronics N.V., and their various subsidiaries and affiliates are hereinafter referred to as "ST."

3. On information and belief, InvenSense: (i) is a corporation organized under the laws of the State of Delaware, having its corporate headquarters and principal place of business here in the Northern District of California at 1197 Borregas Avenue, Sunnyvale, CA 94089; (ii) may be served with process by serving its Delaware registered agent The Corporation Trust Company, The Corporation Trust Center, 1209 Orange Street, Wilmington, Delaware 19801; and (iii) does business in the Northern District of California.

JURISDICTION AND VENUE

4. This lawsuit is a civil action for patent infringement arising under the patent laws of the United States, 35 U.S.C. § 101, *et seq.* Accordingly, this Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

5. This Court has personal jurisdiction over InvenSense for at least the following reasons: (i) on information and belief, InvenSense's corporate headquarters and principal place

of business are located in the Northern District of California; (ii) InvenSense has committed acts of patent infringement, and/or contributed to or induced acts of patent infringement by others, in this District and elsewhere in California and the United States; (iii) InvenSense regularly does business or solicits business, engages in other persistent courses of conduct, and/or derives substantial revenue from products and/or services provided to individuals in this District and in this State; and (iv) InvenSense has purposefully established substantial, systematic, and continuous contacts with this District and expects or should reasonably expect to be sued here. Thus, this Court's exercise of jurisdiction over InvenSense will not offend traditional notions of fair play and substantial justice.

6. Venue is proper in this judicial district pursuant to 28 U.S.C. §§ 1391(b)-(c) and 1400(b) because InvenSense does business in the State of California, has committed acts of infringement in this State and in this District, a substantial part of the events or omissions giving rise to this complaint occurred in this District, and InvenSense is subject to and has previously subjected itself to personal jurisdiction in this District. Moreover, InvenSense's corporate headquarters are located in this District.

INTRADISTRICT ASSIGNMENT

7. This is an Intellectual Property Action to be assigned on a district-wide basis pursuant to Civil Local Rule 3-2(c).

BACKGROUND

ST's MEMS Innovations

8. ST is a global leader in the semiconductor market serving customers across the spectrum of sense and power technologies and multimedia convergence applications. Since its inception, ST has maintained an unwavering commitment to research and development ("R&D"). STI and the other ST companies make a substantial investment in the research and development of inventions and other intellectual property. Almost one quarter of the world-wide employees of ST work in R&D and/or product design, and ST has advanced R&D centers around the world including in the United States. Today, STI and the other ST companies own over

21,500 patents and pending patent applications worldwide, including over 7,500 issued U.S. patents and 2,500 pending U.S. patent applications.

9. One area in which ST has made a substantial and long-term R&D investment is in the field of Micro-Electro-Mechanical Systems ("MEMS"). ST launched the consumer MEMS revolution through the combination of innovative product design, manufacturing know-how, deep application expertise, and bold and timely infrastructure investments. ST was the first major manufacturer in the world to start producing MEMS on 8-inch silicon wafers. ST also developed the THELMA (Thick Epi-Poly Layer for Microactuators and Accelerometers) surface micro-machining process for use in manufacturing both accelerometers and gyroscopes. In addition, ST introduced the world's first high-performance 3-axis MEMS gyroscope. ST's patents and products reflect its innovations in MEMS manufacturing, packaging, circuit design, electrical contacts, device integration, actuation and sensing technologies, and component layout.

10. ST is the leading supplier by revenue of MEMS devices for consumer and mobile MEMS. Building on its track record of success, ST continues to invest in MEMS R&D and innovative applications for MEMS.

The Asserted Patents

11. STI is the owner by assignment of all rights, title, and interest in the Asserted Patents, including the right to bring this suit for injunctive relief and damages.

12. **U.S. Patent No. 6,034,419**, entitled "Semiconductor Device With A Tungsten Contact," was duly and legally issued by the United States Patent and Trademark Office on March 7, 2000.

13. **U.S. Patent No 6,370,954,** entitled "Semiconductor Integrated Inertial Sensor With Calibration Microactuator," was duly and legally issued by the United States Patent and Trademark Office on January 25, 2005.

InvenSense Infringes STI's Patents

14. On information and belief, InvenSense was incorporated in California in June 2003 and reincorporated in Delaware in January 2004.

15. InvenSense competes, or seeks to compete, with STI in the United States and other ST companies around the world in the MEMS market.

16. InvenSense has infringed, and continues to infringe, the Asserted Patents. As of April 3, 2011, InvenSense claims to have sold over 110 million units of MEMS products.

17. InvenSense's infringing MEMS products are sold by InvenSense with the expectation that they will be incorporated into consumer electronic products that are purchased, used and/or sold in, or imported to, the United States, including in the Northern District of California. As stated on its website, InvenSense's MEMS gyroscopes "have been designed into digital still cameras and camera phones for image stabilization; GPS devices for dead reckoning; and 3D peripherals such as 3D mice, TV remote controls, and game controllers. There are millions of consumer electronic products and applications incorporating the Company's integrated dual-axis gyros."

18. On information and belief, InvenSense designs its MEMS products in the United States and particularly in the Northern District of California.

19. InvenSense's Registration Statement, as amended, for its initial public offering ("Registration Statement") further touted that "in 2011, its ITG/IMU/MPU-3000 family of products started high volume shipments for the portable gaming, digital television and set-top box remote control, smart phone and tablet markets." In a September 14, 2011 press release, InvenSense announced that "it is shipping in volume the MPU-6050 product to handset and tablet OEMs and ODMs." On information and belief, by way of example, InvenSense's infringing products are intended for use in, and are incorporated into, devices such as the following in order to enable motion-based applications:

- Gaming devices, such as Nintendo Wii MotionPlus Accessory, Nintendo Wii Remote Plus Controller, Nintendo 3DS and Roku 2 XS (which incorporate, by way of example, InvenSense's ITG-3205, IDG-600, ITG-3270 and/or IMU-3000)

- TV remotes, such as LG's Magic Motion Remote Control (which incorporates, by way of example, InvenSense's IXZ-500);
- Toys with motion sensing capabilities, such as the A.R. Drone and A.R. Drone 2 by Parrot (which incorporates, by way of example, InvenSense's IMU-3000);
- Smart phones, such as LG's Optimus Black P970 (which incorporates, by way of example, InvenSense's MPU-3050); and
- Other electronic devices such as Black & Decker's motion-sensing screwdriver (which incorporates, by way of example, InvenSense's ISZ-650) and the Amazon Kindle Fire HD (which incorporates, by way of example, InvenSense's MPU-6050).

20. In addition, InvenSense indirectly infringes the Asserted Patents. InvenSense induces distributors, consumers, and end-users to directly infringe the Asserted Patents by selling or using its MEMS products, including those identified above and herein. InvenSense's marketing, sales, and customer support materials instruct customers to use infringing features of its MEMS products in an infringing manner. For example, InvenSense's website provides customers and potential customers with product specifications, technical papers and other marketing materials for InvenSense's MEMS products that tout their infringing features and instruct customers to use them in an infringing manner. On information and belief, InvenSense also provides verbal and written instructions, including sales support and technical know-how, to its distributors and customers that intentionally aid, assist, and encourage infringement.

21. InvenSense's MEMS products – which it sells directly, as well as through its distribution partners, to consumers and assemblers – are designed to be used (and are used by said parties) in an infringing manner. Additionally, on information and belief, InvenSense's MEMS products were especially designed, made, and/or adapted for use in an infringing manner. InvenSense's MEMS products either embody the claimed inventions on their own or are material, non-staple components of end-user products that embody the claimed inventions, which components have no substantial non-infringing uses. In fact, as part of its Registration Statement, InvenSense touted its "direct customer engagement model": "We work directly with

large original equipment manufacturer (OEM) customers to assist them in developing solutions and applications that may lead to more demand for our products. . . . For our larger OEM customers, we believe that our direct customer engagement approach, ecosystem partnerships and adoption of our APIs into major software operating systems provides us with significant differentiation in the customer sales process by aligning us more closely with the changing needs of these OEM customers and their end markets. We actively utilize field application engineers as part of our sales process to better engage the customer with our products. . . . Our direct customer engagement model extends to service and support."

InvenSense Knowingly Induced And Contributed To The Infringement Of Others

22. InvenSense is on notice of the Asserted Patents, and has been on notice of the Asserted Patents and its infringement thereof since at least February 2012. In or around December 2011, the parties engaged in license negotiations during which ST identified particular patents that InvenSense was infringing. In or around February 2012, ST made various presentations to InvenSense that demonstrated how certain InvenSense products infringed certain patent claims of various ST patents, including the '954 and '419 patents. Despite such notice, InvenSense has failed to cease its infringement. Instead, InvenSense continues to sell its infringing products and encourage its customers to use InvenSense products in an infringing manner.

InvenSense's Infringement Harms STI

23. STI is harmed by InvenSense's use of STI's patented technologies in a way that cannot be remedied by monetary damages alone. InvenSense has received substantial revenue and increased its market share by selling products that incorporate STI's technology without having to incur the costs of developing or licensing this technology.

24. On information and belief, InvenSense's infringement has caused STI to suffer irreparable harm due to, among other things, lost business opportunities, lost market share, and price erosion. Even if InvenSense were to subsequently pay past due royalties, lost profits, or other damages, there is no reason to believe that InvenSense would stop infringing, and it would

still enjoy the market share it has developed while infringing upon the Asserted Patents. Due to the difficulty in predicting whether, if at all, STI can recover this market share, STI's harm cannot be compensated by payment of monetary damages alone.

COUNT I: INFRINGEMENT OF U.S. PATENT NO. 6,370,954

25. STI incorporates by reference the preceding averments set forth in paragraphs 1-24.

26. InvenSense has infringed and continues to infringe, has contributed to and continues to contribute to acts of infringement, and/or has actively and knowingly induced and continues to actively and knowingly induce the infringement of the '954 patent by making, using, offering for sale and selling in the United States, and by importing into the United States without authority, and/or by causing others to make, use, offer for sale and sell in the United States, and import into the United States without authority, MEMS products and services, including but not limited to InvenSense's ISZ-650, IMU-3000, ITG-3050, MPU-3050, ITG-3200, MPU-6000, MPU-6050, and MPU-9150 product lines.

27. On information and belief, InvenSense's infringement, contributory infringement, and/or inducement of infringement is literal infringement or, in the alternative, infringement under the doctrine of equivalents.

28. InvenSense's infringing activities have caused and will continue to cause STI irreparable harm, for which it has no adequate remedy at law, unless InvenSense's infringing activities are enjoined by this Court in accordance with 35 U.S.C. § 283.

29. STI has been and continues to be damaged by InvenSense's infringement of the '954 patent in an amount to be determined at trial.

30. On information and belief, InvenSense's infringement of the '954 patent was willful and deliberate, entitling STI to enhanced damages and attorneys' fees.

COUNT II: INFRINGEMENT OF U.S. PATENT NO. 6,034,419

31. STI incorporates by reference the preceding averments set forth in paragraphs 1-30.

32. InvenSense has infringed and continues to infringe, has contributed to and continues to contribute to acts of infringement, and/or has actively and knowingly induced and continues to actively and knowingly induce the infringement of the '419 Patent by making, using, offering for sale and selling in the United States, and by importing into the United States without authority, and/or by causing others to make, use, offer for sale and sell in the United States, and import into the United States without authority, MEMS products and services, including but not limited to InvenSense's IMU-3000, ITG-3050, MPU-3050, ITG-3200, MPU-6050, and MPU-9150 product lines.

33. On information and belief, InvenSense's infringement, contributory infringement, and/or inducement of infringement is literal infringement or, in the alternative, infringement under the doctrine of equivalents.

34. InvenSense's infringing activities have caused and will continue to cause STI irreparable harm, for which it has no adequate remedy at law, unless InvenSense's infringing activities are enjoined by this Court in accordance with 35 U.S.C. § 283.

35. STI has been and continues to be damaged by InvenSense' infringement of the '419 patent in an amount to be determined at trial.

36. On information and belief, InvenSense's infringement of the '419 patent was willful and deliberate, entitling STI to enhanced damages and attorneys' fees.

REQUEST FOR RELIEF

WHEREFORE, Plaintiff STMicroelectronics, Inc. respectfully requests that:

(a) Judgment be entered that InvenSense has infringed one or more claims of each of the Asserted Patents;

(b) Judgment be entered permanently enjoining InvenSense, its directors, officers, agents, servants, and employees, and those acting in privity or in concert with them, and their subsidiaries, divisions, successors, and assigns, from further acts of infringement, contributory infringement, or inducement of infringement of the Asserted Patents;

(c) Judgment be entered awarding STI all damages adequate to compensate it for InvenSense's infringement of the Asserted Patents including all pre-judgment and post-judgment interest at the maximum rate permitted by law and enhanced damages;

(d) Judgment be entered that this is an exceptional case and awarding STI attorneys' fees and costs; and

(e) Judgment be entered awarding STI such other and further relief as this Court may deem just and proper.

DATED: March 12, 2013

QUINN EMANUEL URQUHART & SULLIVAN, LLP

By Michael D. Powell /MAC
Michael D. Powell
Attorneys for STMicroelectronics, Inc.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

STMICROELECTRONICS, INC.,

Plaintiff,

vs.

INVENSENSE, INC.,

Defendant.

Case No.

DEMAND FOR JURY TRIAL

TO EACH PARTY AND TO THE COUNSEL OF RECORD FOR EACH PARTY:

Plaintiff STMicroelectronics, Inc. hereby demands a jury trial in the above-titled action pursuant to Rule 38(b) of the Federal Rules of Civil Procedure.

DATED: March 12, 2013

Respectfully submitted,

QUINN EMANUEL URQUHART & SULLIVAN, LLP

By: Michael D. Powell 'MAC

Michael D. Powell

Attorneys for STMicroelectronics, Inc.

EXHIBIT A

US006370954B1

(12) **United States Patent**
Zerbini et al.

(10) **Patent No.: US 6,370,954 B1**
(45) **Date of Patent: Apr. 16, 2002**

(54) **SEMICONDUCTOR INTEGRATED INERTIAL SENSOR WITH CALIBRATION MICROACTUATOR**

(75) Inventors: **Sarah Zerbini**, Fontanellato; **Benedetto Vigna**, Pietrapertosa; **Massimo Garavaglia**, Robecchetto; **Gianluca Tomasi**, Vigevano, all of (IT)

(73) Assignee: **STMicroelectronics S.r.l.**, Agrate Brianza (IT)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/659,168**

(22) Filed: **Sep. 11, 2000**

(30) **Foreign Application Priority Data**

Sep. 10, 1999 (EP) 99830566

(51) **Int. Cl.**[7] **G01P 15/00**
(52) **U.S. Cl.** **73/514.01**; 73/514.02
(58) **Field of Search** 73/504.02, 504.03, 73/504.04, 504.08, 504.09, 504.12, 504.13, 514.32, 514.01, 514.02

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,251,484 A * 10/1993 Mastache 73/514.02
5,621,157 A * 4/1997 Zhao et al. 73/1.38
6,257,062 B1 * 7/2001 Rich 73/514.32

FOREIGN PATENT DOCUMENTS

EP	0 840 092 A2	5/1998
WO	89/10567	11/1989
WO	95/34798	12/1995
WO	96/39615	12/1996

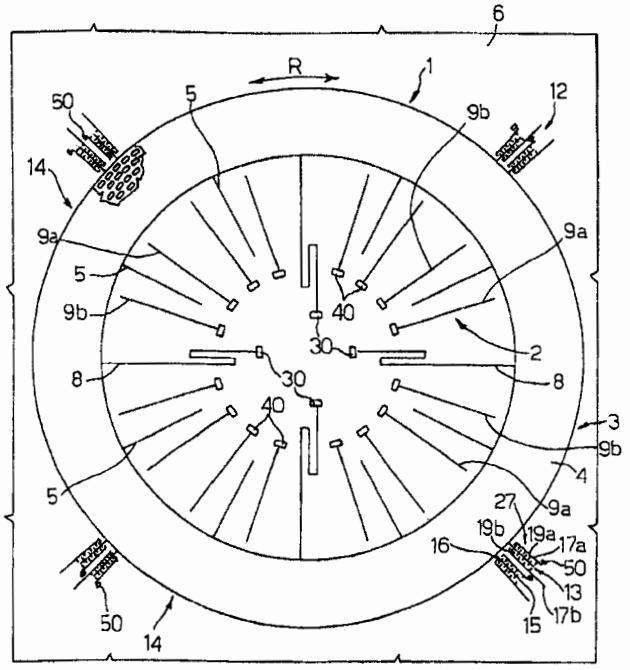
* cited by examiner

Primary Examiner—Richard A. Moller
(74) *Attorney, Agent, or Firm*—Lisa K. Jorgenson; E. Russell Tarleton; SEED IP Law Group PLLC

(57) **ABSTRACT**

An inertial sensor having an inner stator and an outer rotor that are electrostatically coupled together by mobile sensor arms and fixed sensor arms. The rotor is connected to a calibration microactuator comprising four sets of actuator elements arranged one for each quadrant of the inertial sensor. There are two actuators making up each set. The actuators are identical to each other, are angularly equidistant, and each comprises a mobile actuator arm connected to the rotor and bearing a plurality of mobile actuator electrodes, and a pair of fixed actuator arms which are set on opposite sides with respect to the corresponding mobile actuator arm and bear a plurality of fixed actuator electrodes. The mobile actuator electrodes and fixed actuator electrodes are connected to a driving unit which biases them so as to cause a preset motion of the rotor, the motion being detected by a sensing unit connected to the fixed sensor arms.

19 Claims, 3 Drawing Sheets



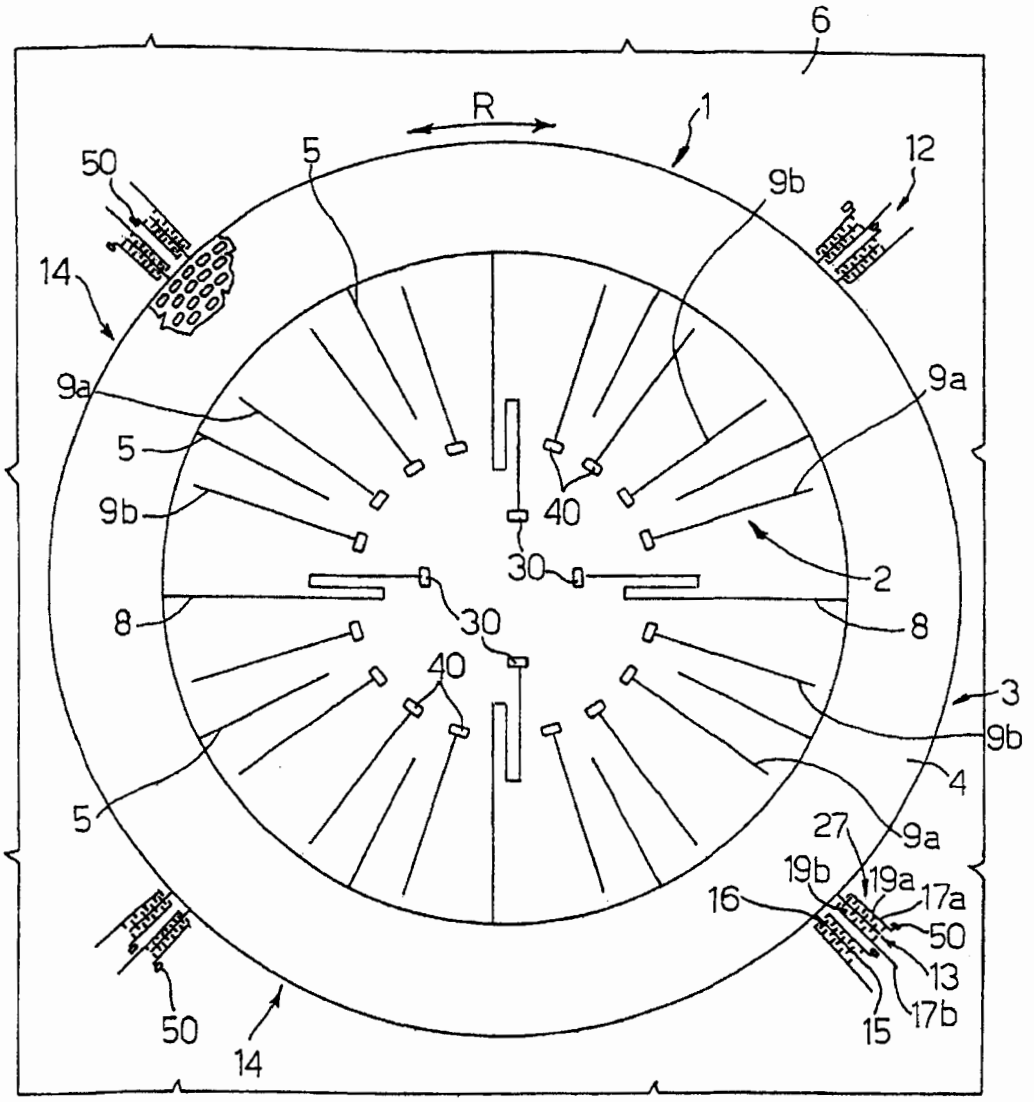

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Fig.1

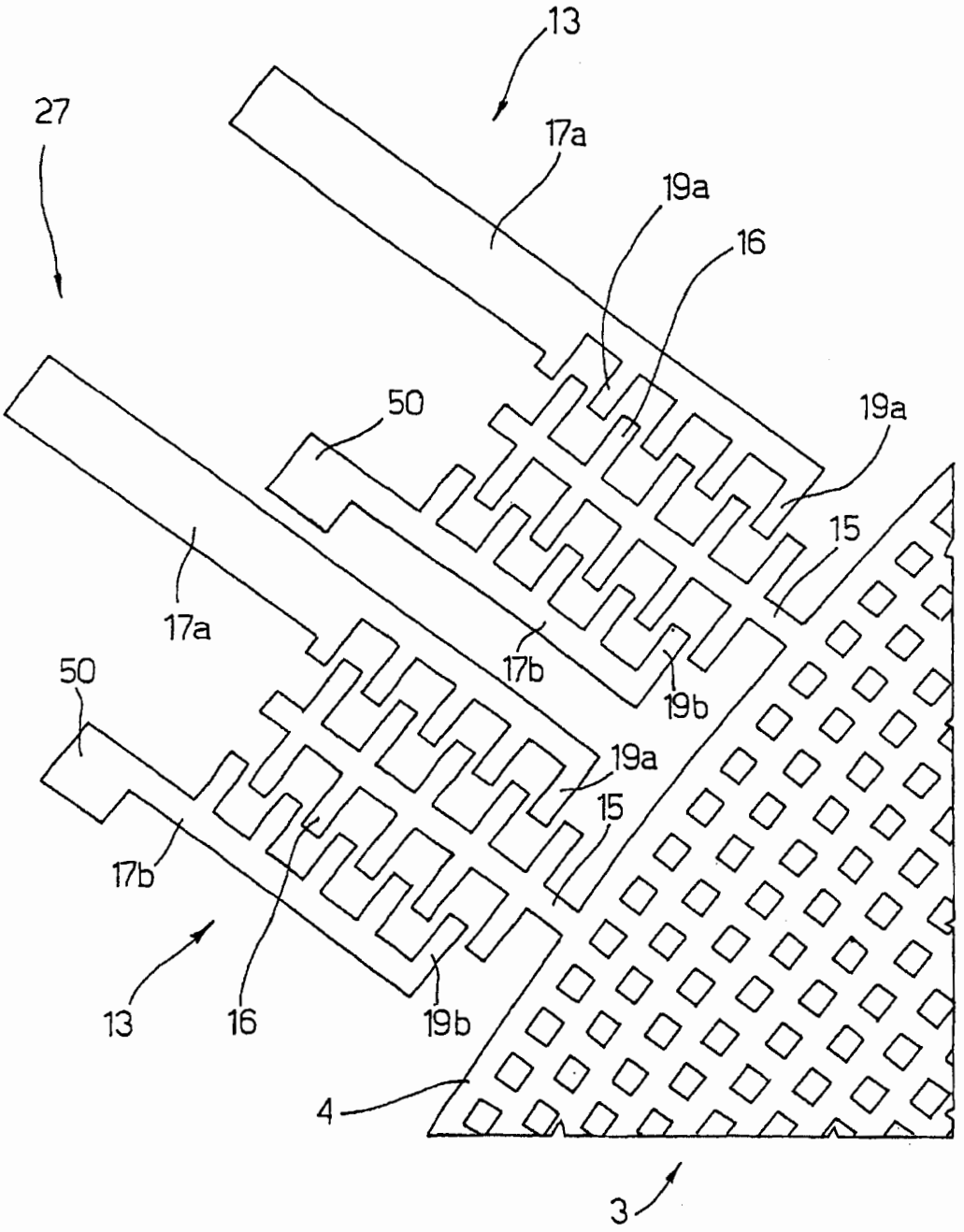

Fig. 2

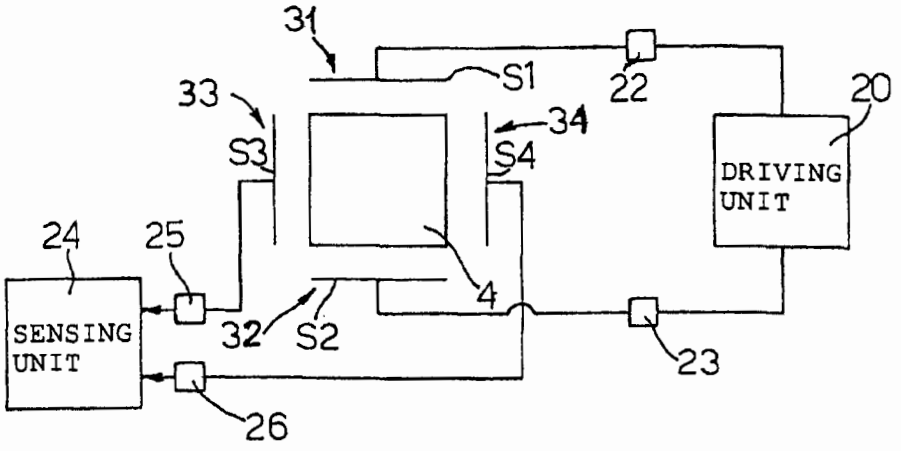
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Fig. 3

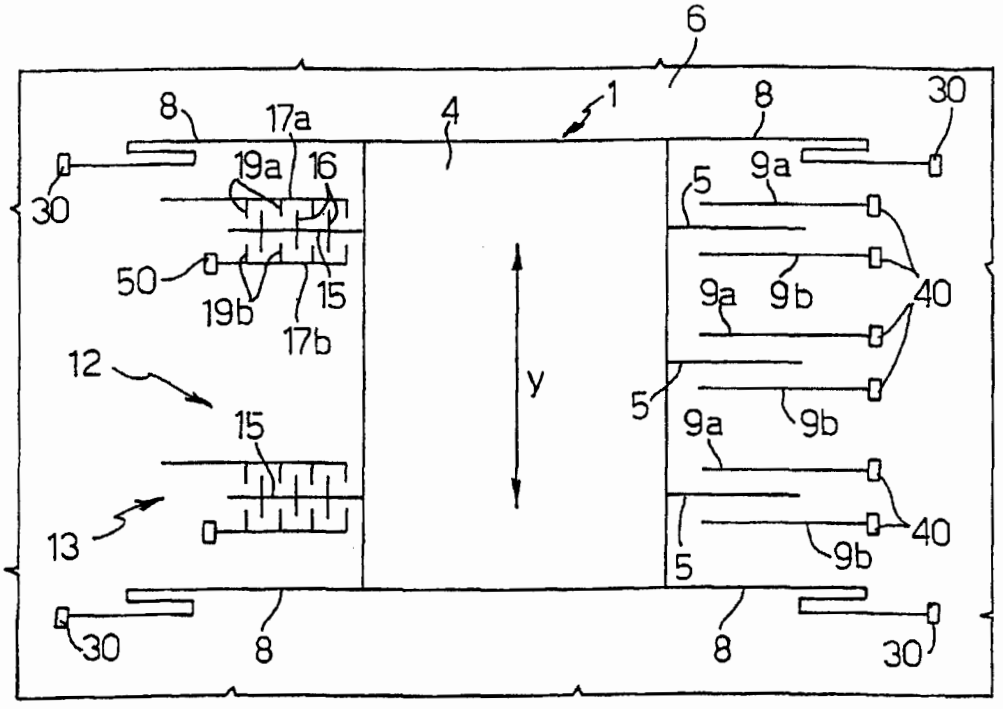
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Fig. 4

SEMICONDUCTOR INTEGRATED INERTIAL SENSOR WITH CALIBRATION MICROACTUATOR

TECHNICAL FIELD

The present invention regards a semiconductor integrated inertial sensor with calibration microactuator.

BACKGROUND OF THE INVENTION

As is known, the possibility of exploiting machinery and manufacturing processes typical of the microelectronics industry enables semiconductor integrated inertial sensors to be manufactured at a low cost, at the same time guaranteeing high reliability in terms of performance.

Although these inertial sensors are advantageous from various points of view, they present the drawback that their calibration is very complex, as well as costly, in that it is difficult to calibrate them at a wafer level.

In addition, the inertial sensors thus obtained have an offset and output/input sensitivity that depends upon the parameters of the process of fabrication, and consequently must be suitably calibrated.

In order to calibrate the sensor, one first known solution involves shaking of the inertial sensor, already inserted in its own package, on an electrodynamic or piezoelectric actuator validated according to required standards. The choice of a particular type of actuator is assessed on the basis of the range of the operating frequencies of the inertial sensor that is to be calibrated. The calibration curve that is obtained is then, generally, stored in a memory device formed in the die in which the inertial sensor itself is made. Even though this first known solution is advantageous from various points of view, it presents the drawback that it is extremely difficult to achieve at the wafer level.

A second known solution is described in U.S. Pat. No. 5,621,157, which envisages integration on one and the same wafer of the inertial sensor to be calibrated and of an electrostatic actuator, which simulates the unknown inertial quantity to be measured, and has the following characteristics:

it is linear in the voltage applied;

it is precise; i.e., its operation is practically independent of the parameters of the integration process.

"Practically independent" means that the electrostatic actuator has a configuration which is less sensitive than the inertial sensor is to the variations in the integration process adopted for the fabrication of the inertial sensor itself.

In addition, this second known solution is valid for all sensors, whether open loop sensors or closed loop sensors.

More in detail, the method and device described in U.S. Pat. No. 5,621,157 are implemented by means of an inertial sensor comprising one mobile electrode (rotor) and two fixed electrodes (stators), underneath which is set a service electrode (actuator also referred to as "ground plane"). By varying the voltage applied to the service electrode and keeping the voltage applied to the mobile electrode at a fixed value, a lateral force is produced that acts upon the mobile electrode along a direction parallel to the plane in which the service electrode lies. This lateral force is independent of the distance between the mobile electrode and the fixed electrodes, a distance which is markedly affected by the variations in the process of fabrication of the inertial sensor, and consequently it can be used as a reference force for the calibration of the inertial sensor itself.

Although this second solution is advantageous from a number of standpoints, it presents, however, the drawback

that, at each variation in the voltage applied to the service electrode, there is produced on the mobile electrode, in addition to the lateral force, also a vertical force in a direction orthogonal to the plane in which the service electrode is set. In addition, the lateral force has a value other than zero only when different voltages are applied to the two fixed electrodes. Consequently, the method devised and the device made according to this second known solution are far from efficient in terms of conversion of electrical energy into mechanical energy, and are valid only for certain electrical configurations of the inertial sensor that is to be calibrated.

SUMMARY OF THE INVENTION

The technical problem that lies at the basis of the disclosed embodiments present invention is that of creating a semiconductor integrated inertial sensor with a calibration microactuator that is able to overcome the limitations and drawbacks referred to above in connection with the known art.

The technical problem is solved by an inertial sensor integrated in a body of semiconductor material and having a stator element and a rotor element that are electrostatically coupled together, the rotor element having a mobile mass, and a microactuator integrated in the body of semiconductor material, the microactuator connected to and coplanar with the mobile mass of the rotor element.

In accordance with another aspect of the present invention, the mobile mass is free to move in one direction and the microactuator has at least one first actuator element having at least one mobile actuator arm that is integral with the mobile mass and at least one first fixed actuator arm facing the mobile actuator arm, the mobile actuator arm and the first fixed actuator arm carrying respective multiple actuator electrodes and fixed actuator electrodes that are comb fingered together and extend in a direction substantially parallel to the first direction.

In accordance with yet another aspect of the invention, the mobile actuator electrodes extend on both sides of the mobile actuator arm, and the microactuator includes a second fixed actuator arm carrying a plurality of second fixed actuator electrodes that are comb fingered with respective mobile actuator electrodes, the first and second fixed actuator arms set on opposite sides with respect to a corresponding mobile actuator arm.

BRIEF DESCRIPTION OF THE DRAWINGS

The characteristics and advantages of the inertial sensor according to the embodiments invention will emerge from the ensuing description, which is given purely to provide a non-limiting illustration, with reference to the attached drawings, in which:

FIG. **1** schematically shows a first embodiment of an inertial sensor according to the present invention;

FIG. **2** shows an example of embodiment of a microactuator for calibrating the inertial sensor of FIG. **1**;

FIG. **3** shows the equivalent electrical diagram of the structure of FIG. **1**; and

FIG. **4** is a schematic representation of a second embodiment of the inertial sensor according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In FIG. **1**, the reference number **1** designates an inertial sensor, for example an angular acceleration sensor, integrated in a semiconductor material, namely, silicon.

More in detail, the inertial sensor **1** comprises an inner stator **2**, which is integral with a die **6** in which the sensor itself is made, and an outer rotor **3**, capacitively coupled to the stator **2**.

The rotor **3** comprises a mobile mass **4**, which is suspended and has a basically annular shape, and a plurality of mobile sensor arms **5**, which extend radially towards the stator **2** starting from the mobile mass **4**, are identical to each other and are at the same angular distance apart, and elastic suspension and anchorage elements (springs **8**) which elastically connect the mobile mass **4** to first anchoring and biasing regions **30**, through which the rotor **3** and the mobile sensor arms **5** are biased at a biasing voltage Vr, typically of the value of 1.5 V.

The stator **2** comprises a plurality of pairs of fixed sensor arms **9***a*, **9***b*, one for each mobile sensor arm **5** of the rotor **3**, which extend inside the mobile mass **4** itself, between the mobile sensor arms **5**, and are fixed to second anchoring and biasing regions **40**. The pairs of fixed sensor arms **9***a*, **9***b* are arranged in such a way that one mobile sensor arm **5** of the rotor **3** is set between a first fixed sensor arm **9***a* and a second fixed sensor arm **9***b* of a pair of fixed sensor arms **9***a*, **9***b*.

Typically, the stator **2** and the fixed sensor arms **9***a*, **9***b* are biased, through the second anchoring and biasing regions **40**, at a biasing voltage Vs, which assumes values of between 1.5 V and 2.2 V.

Consequently, in the presence of angular stresses, the mobile mass **4** and the respective mobile sensor arms **5** rotate, in a micrometric way, either clockwise or counterclockwise, as indicated by the double headed arrow R.

A pair of fixed sensor arms **9***a*, **9***b* and the respective mobile sensor arm **5** set between them can be modeled as a capacitive divider made up of two variable capacitors connected in series together, in which the two outer plates are defined by the fixed sensor arms **9***a* and **9***b* of the stator **2**, and the inner plates are defined by the mobile sensor arms **5** of the rotor **3**. In addition, the capacitive dividers made up of all the pairs of fixed sensor arms **9***a*, **9***b* and of the respective mobile sensor arms **5** are connected together in parallel, with the intermediate nodes of the dividers connected together by means of the mobile mass **4**. Consequently, the entire inertial sensor **1** may be represented in the way shown in FIG. **3**, where the electrode SI represents the set of fixed sensor arms **9***a* and makes up a first variable capacitor **31**, and the electrode S2 represents the set of fixed sensor arms **9***b* and makes up a second variable capacitor **32**.

The inertial sensor **1** also comprises an integrated microactuator **12** connected to the rotor **3**.

More in detail, as shown in FIGS. **1** and **2** the microactuator **12** comprises four sets **27** of actuator elements **13** connected to and coplanar with the rotor **3**. The sets **27** are arranged one for each quadrant **14** of the inertial sensor **1** and are angularly equidistant.

In particular, there are two actuator elements **13** for each set **27**, which are identical to each other, and each of which comprises a mobile actuator arm **15** which is connected to the mobile mass **4** of the rotor **3** and extends radially outwards, starting from the mobile mass **4** itself. Each mobile actuator arm **15** carries a plurality of mobile actuator electrodes **16**, which extend on either side of the respective mobile actuator arm **15** in a basically circumferential direction, the mobile actuator electrodes **16** being positioned equidistantly along the respective mobile actuator arm **15**.

Each actuator element **13** moreover includes a pair of fixed actuator arms **17***a*, **17***b*, which extend radially, each

pair of fixed actuator arms **17***a*, **17***b* being made up of a first fixed actuator arm **17***a* and a second fixed actuator arm **17***b* which are set on opposite sides with respect to the corresponding mobile actuator arm **15**. The first fixed actuator arm **17***a* carries a plurality of first fixed actuator electrodes **19***a*, and the second fixed actuator arm **17***b* carries a plurality of second fixed actuator electrodes **19***b*.

The fixed actuator arms **17***a*, **17***b* are constrained to third anchoring and biasing regions **50**, through which they are biased at a biasing voltage Vb, which assumes values of between 1.5 V and 5 V.

The fixed actuator electrodes **19***a*, **19***b* extend in a basically circumferential direction towards the respective mobile actuator arm **15** and are interspaced or comb fingered with the mobile actuator electrodes **16**. In practice, the fixed actuator electrodes **19***a*, **19***b* and the respective mobile actuator electrodes **16**, like the fixed sensor arms **9***a*, **9***b* and the mobile sensor arms **5**, the fixed actuator electrodes **19***a*, **19***b* and the respective mobile actuator electrodes **16** of each actuator element **13**, may be modeled as a capacitive divider made up of two capacitors connected in series together, in which the two outer plates are defined by the fixed actuator electrodes **19***a*, **19***b*, and the two inner plates are defined by the mobile actuator electrodes **16**. In addition, the capacitive dividers made up of all the actuator elements **13** are connected together in parallel, with the intermediate nodes of the dividers connected together via the mobile mass **4**. Consequently, the microactuator **12** may be represented in the way shown in FIG. **3**, where the electrode S3 represents the set of fixed actuator electrodes **19***a* and forms a first actuation capacitor **33**, and the electrode S4 represents the set of fixed actuator electrodes **19***b* and forms a second actuation capacitor **34**.

FIG. **3** moreover shows a calibration circuit for calibrating the inertial sensor **1**, which comprises a driving unit **20** having output terminals **22** and **23** coupled, respectively, to the fixed actuator arms **17***a* and **17***b*, and hence to the electrodes S1 and S2, and a sensing unit **24** having input terminals **25** and **26** coupled, respectively, to the fixed sensor arms **9***a* and **9***b* of the stator **2**, and hence to the electrodes S3 and S4. The driving unit **20**, as described more in detail in what follows, generates driving voltages V1(t) and V2(t) oscillating in opposition with respect to a constant mean value Vd(t).

Operation of the inertial sensor **1** is as follows:

The driving voltages V1(t) and V2(t), equal to

$$V1(t)=Vb+Vd(t), \text{ and}$$

$$V2(t)=Vb-Vd(t)$$

where Vb is a constant biasing voltage and Vd(t) is an alternating voltage, for example square wave or sinusoidal wave, are applied, respectively, to the fixed actuator electrodes **19***a* and **19***b* by the driving unit **20**.

The voltages V1(t) and V2(t) alternately generate, on the mobile mass **4**, a transverse force proportional to the number of fixed actuator electrodes **19***a*, **19***b* and to the number of interacting mobile actuator electrodes **16**. In addition, given that the voltages V1(t) and V2(t) are in counterphase, this transverse force is directed first in one direction and then in the opposite direction.

In particular, this transverse force tends to move each mobile actuator electrode **16** away from the fixed actuator electrodes **19***a*, **19***b* , with respect to which the mobile actuator electrode **16** has a lower potential difference, and to bring the mobile actuator electrode **16** closer to the fixed actuator electrodes **19***b*, **19***a*, with respect to which it has a higher potential difference. In this way, the mobile mass **4**

undergoes a rotary motion having a twisting moment τ proportional to the biasing voltage Vb of the fixed actuator arms **17***a*, **17***b* and to the alternating voltage Vd(t), according to the following relation:

$$\tau=\alpha*Vb*Vd(t)$$

where the parameter α is the precision of the microactuator **12** and depends upon the number of pairs of electrodes, their thickness and relative distance, according to the following relation:

$$\alpha=4*\epsilon_0*N*R_m*t/g$$

where ϵ_0 is the electric constant, N is the number of electrodes, R_m is the distance of the electrodes from the center of rotation, t is the thickness of the electrodes (which coincides with the thickness of the polysilicon used for making them on the wafer), and g is the distance between the electrodes.

The twisting moment τ is independent of the relative displacement between the fixed actuator electrodes **19***a*, **19***b* and the mobile actuator electrodes **16** in that it depends only upon the distance g of the pairs of mobile/fixed electrodes, which is constant, and does not depend upon the area of mutual facing, which is variable, given that the electrodes extend substantially parallel to the direction of motion R of the rotor **3**, and hence of the mobile electrodes **15**.

The twisting moment τ, to which the mobile mass **4** is subjected, thus determines a modulation in phase opposition of the capacitances of the two variable capacitors **31**, **32**, the two outer plates of which are defined by the fixed sensor arms **9***a*, and **9***b* of the stator **2**, and the two inner plates of which are defined by the mobile sensor arms **5** of the rotor **3**. Of these two variable capacitors **31**, **32**, the one defined by the mobile sensor arms **5** and by the fixed sensor arm **9***a*, **9***b* that is at a smaller distance makes up the effective capacitor, which determines the generation of the sensing signal that indicates the twisting moment τ to which the mobile mass **4** is subjected.

This sensing signal is then sent to the input terminals **25** and **26** of the sensing unit **24**, which uses it as a reference signal for calibrating the inertial sensor **1**.

The advantages that may be obtained with the inertial sensor described herein are the following: In the first place, the actuator elements **13** are defined on silicon together with the mobile mass **4**, and consequently do not require additional fabrication phases. In addition, the inertial sensor **1** is more efficient as regards the conversion of electrical energy into mechanical energy, because the microactuator **12** does not generate any force that acts perpendicularly on the mobile mass **4**. Furthermore, since the transverse force that acts on the mobile mass **4** is independent of the biasing voltages applied to the rotor **3** and the stator **2** of the inertial sensor **1**, calibration of the inertial sensor **1** is independent of its own operating voltage. The last two advantages described are very important in that they render the inertial sensor **1** less costly in terms of energy and, above all, render the circuit configuration of the microactuator **12** independent of the circuit configuration of the inertial sensor **1** (for example, sigma delta, frequency modulation). In addition, the comb finger configuration chosen for the fixed actuator electrodes **19***a*, **19***b* and mobile actuator electrodes **16** is not affected by the problem of electrostatic softening (i.e., reduction in the rigidity of the system). Consequently, the characteristics of the actuator are not modified, and the latter may exert a force independent of the displacement.

Furthermore, for the fabrication of the inertial sensor **1** any type of micromachining technology may be used (for example, surface or epitaxial micromachining, metal electroplating, etc.).

Finally, it is clear that numerous modifications and variations may be made to the inertial sensor described and illustrated herein, all falling within the scope of the inventive idea as defined in the attached claims and the equivalents thereof.

For example, the number of sets **27** of actuator elements **13** and the number of actuator elements **13** in each set **27** could be different from what has been described; in particular, it would be possible to envisage even a single actuator element **13** connected to the mobile mass **4** of the rotor **3**, or else two actuator elements **13** could be envisaged, set on diametrically opposite sides of the mobile mass **4**.

In addition, the inertial sensor **1** may be of a linear type, as shown in FIG. **4**, in which the various parts of the inertial sensor are indicated by the same reference numbers as those used in FIG. **1**. In this case, the microactuator **12** is driven so as to impress on the mobile mass **4** a vibratory motion along a direction Y, and the mobile actuator electrodes **16** and fixed actuator electrodes **19***a*, **19***b* are parallel to the direction Y.

What is claimed is:

1. An inertial sensor integrated in a body of semiconductor material, comprising: a stator element and a rotor element that are electrostatically coupled together, said rotor element comprising a mobile mass, and microactuator means integrated in said body of semiconductor material, said microactuator means connected to and coplanar with said mobile mass of said rotor element.

2. The inertial sensor of claim **1**, wherein said mobile mass is free to move in one direction and said microactuator means comprise at least one first actuator element having at least one mobile actuator arm that is integral with said mobile mass and at least one first fixed actuator arm facing said mobile actuator arm, said mobile actuator arm and said first fixed actuator arm carrying respective mobile actuator electrodes and first fixed actuator electrodes that are comb fingered together and extend in a second direction substantially parallel to said one direction.

3. The inertial sensor of claim **2**, wherein in that said mobile actuator electrodes extend on both sides of said mobile actuator arm and said microactuator means comprise a second fixed actuator arm carrying a plurality of second fixed actuator electrodes which are comb fingered with respective mobile actuator electrodes, said first and second fixed actuator arms being set on opposite sides with respect to a corresponding mobile actuator arm.

4. The inertial sensor of claim **3**, wherein said mobile mass has an annular shape; said mobile actuator arm extends radially outwards from said mobile mass; said first and second fixed actuator arms extend radially towards said mobile mass; said mobile actuator electrodes extend in a substantially circumferential direction and are set equidistantly apart from one another along said mobile actuator arm; and said first and second fixed actuator electrodes extend in a substantially circumferential direction.

5. The inertial sensor of claim **3**, wherein said rotor element moreover comprises a plurality of mobile sensor arms that extend from said mobile mass, and said stator element comprises a plurality of pairs of fixed sensor arms facing said mobile sensor arms, each pair of fixed sensor arms comprising a first fixed sensor arm and a second fixed sensor arm that are set on opposite sides with respect to the corresponding mobile sensor arm.

6. The inertial sensor of claim 4, wherein the inertial sensor constitutes an angular acceleration sensor.

7. The inertial sensor of claim 3, wherein said one direction is a rectilinear direction, and said sensor constitutes a sensor of rectilinear motion.

8. The inertial sensor of claim 3, further comprising a driving unit having output terminals coupled to said fixed actuator arms and a sensing unit having input terminals coupled to said fixed sensor arms.

9. The inertial sensor of claim 2, wherein said microactuator means comprise further actuator elements that are identical to said at least one first actuator element, said at least one first actuator element and further actuator elements being set symmetrically with respect to said mobile mass.

10. The inertial sensor of claim 1, wherein said microactuator means comprise at least one set of actuator elements, each set of actuator elements comprising at least two actuators that are identical to one another and angularly equidistant from one another.

11. An inertial sensor system formed in a body of semiconductor material, comprising:

a stator and a rotor electrostatically coupled together by mobile sensor arms and fixed sensor arms;

a calibration device coupled to the rotor;

a drive unit coupled to the calibration device, the calibration device and the drive unit configured to cause a preset motion of the rotor; and

a sensing unit coupled to the stator and configured to sense the motion of the rotor.

12. The system of claim 11, wherein the calibration device comprises a microactuator comprising at least one first actuator element having at least one mobile actuator arm that is integral with the rotor and at least one fixed actuator arm facing the mobile actuator arm, the mobile actuator arm and the fixed actuator arm having mobile actuator electrodes and fixed actuator electrodes, respectively, that are comb fingered together.

13. The system of claim 11, wherein the calibration device comprises a microactuator that comprises four sets of actuator elements arranged one for each quadrant of the inertial sensor.

14. The system of claim 13, wherein each set of the four sets of actuator elements comprises first and second actuators that are identical to each other and are angularly equidistant apart.

15. The system of claim 14, wherein each actuator comprises a mobile actuator arm connected to the rotor and having a plurality of mobile actuator electrodes, and a pair of fixed actuator arms formed on opposite sides of the mobile actuator arm and having a plurality of fixed actuator electrodes.

16. The system of claim 15, wherein the mobile actuator electrodes and the fixed actuator electrodes are connected to the driving unit, and the driving unit is configured to bias the mobile actuator electrodes and the fixed actuator electrodes to cause the preset motion of the rotor.

17. The system of claim 13, wherein the microactuator is coupled to and coplanar with the rotor.

18. The system of claim 17, wherein the rotor comprises a mobile mass that is free to move in a first direction, and the microactuator comprises at least one actuator having at least one mobile actuator arm that is integral with the mobile mass and first and second fixed actuator arms facing the mobile actuator arm, the mobile actuator arm and the first and second fixed actuator arms carrying respective mobile actuator electrodes and fixed actuator electrodes that are comb fingered together and extend in a second direction substantially parallel to the first direction.

19. The system of claim 18, wherein the mobile mass has an annular shape, and the mobile actuator arm extends radially outwards from the mobile mass; the first and second fixed actuator arms extend radially towards the mobile mass; the mobile actuator electrodes extend in a substantially circumferential direction and are set equidistantly apart from one another along the mobile actuator arm; and the first and second fixed actuator electrodes extend in a substantially circumferential direction.

* * * * *

EXHIBIT B

US006034419A

United States Patent [19]

Nicholls et al.

[11] Patent Number: 6,034,419

[45] Date of Patent: Mar. 7, 2000

[54] **SEMICONDUCTOR DEVICE WITH A TUNGSTEN CONTACT**

[75] Inventors: **Howard Charles Nicholls; Michael John Norrington**, both of Cardiff; **Michael Kevin Thompson**, Newport, all of United Kingdom

[73] Assignee: **Inmos Limited**, Bristol, United Kingdom

[21] Appl. No.: **08/161,604**

[22] Filed: **Dec. 6, 1993**

Related U.S. Application Data

[62] Division of application No. 07/739,381, Aug. 1, 1991, abandoned, which is a continuation of application No. 07/502,526, Mar. 30, 1990, abandoned.

[30] **Foreign Application Priority Data**

Apr. 7, 1989 [GB] United Kingdom 8907898

[51] **Int. Cl.**[7] **H01L 23/58**

[52] **U.S. Cl.** **257/641**; 257/649; 257/760; 257/763

[58] **Field of Search** 257/640, 641, 257/649, 760, 763, 369

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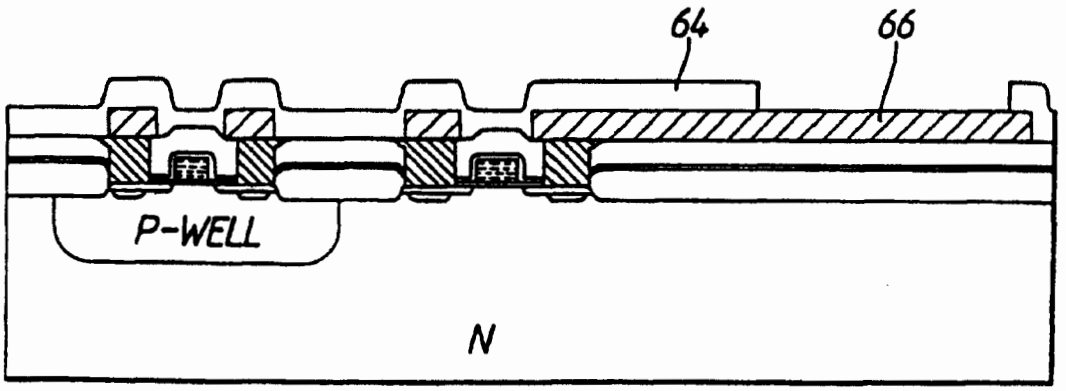
Primary Examiner—J. Carroll

Attorney, Agent, or Firm—McDermott, Will & Emery

[57] **ABSTRACT**

A method of fabricating a tungsten contact in a semiconductor device comprises providing an oxide layer on a region of a silicon substrate; depositing a sealing dielectric layer over the oxide layer; and depositing an interlevel dielectric layer over the sealing layer. The interlevel dielectric layer, the sealing dielectric layer and the oxide layer are then etched through as far as the substrate thereby to form a contact hole and to expose the said region. A dopant is implanted into the said region whereby the implanted dopant is self-aligned to the contact hole. The substrate is thermally annealed. Tungsten is selectively deposited in the contact hole and an interconnect layer is deposited over the deposited tungsten contact. The invention also provides a semiconductor device which incorporates a tungsten contact and which can be fabricated by the method.

13 Claims, 3 Drawing Sheets



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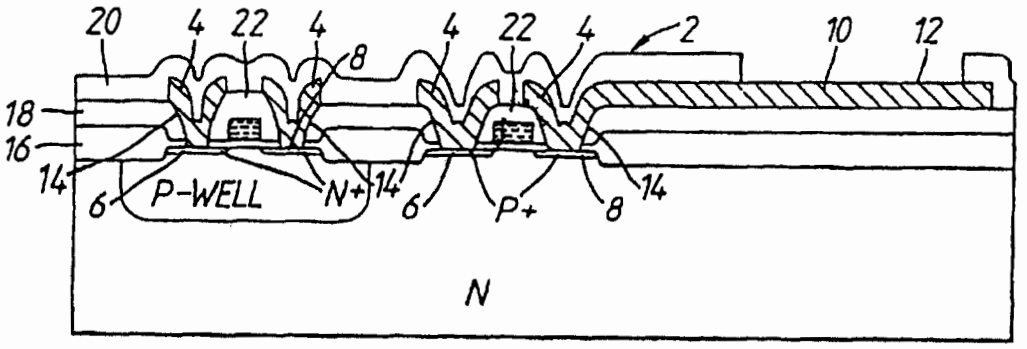

Fig.1. PRIOR ART

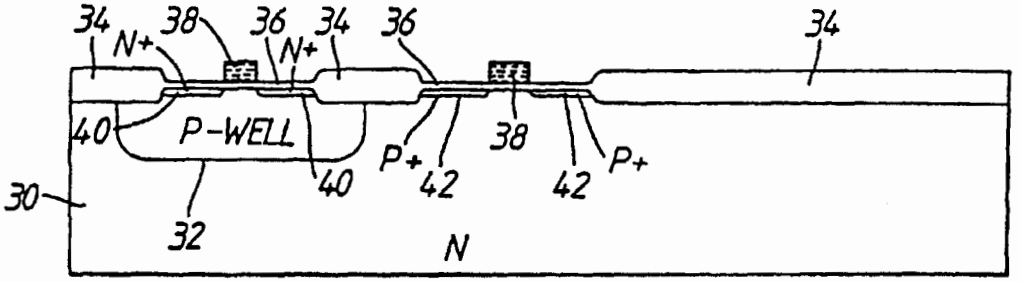

Fig.2.

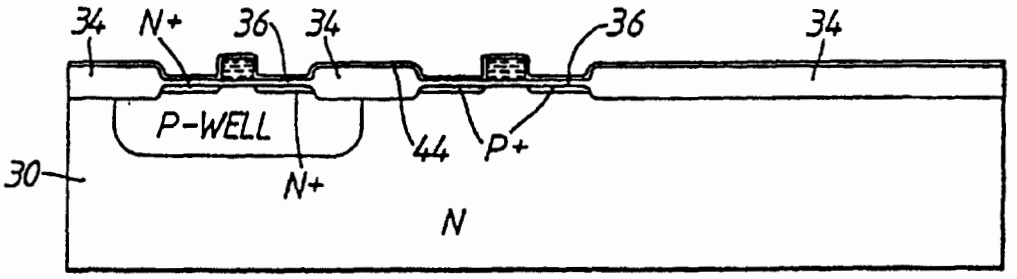

Fig.3.

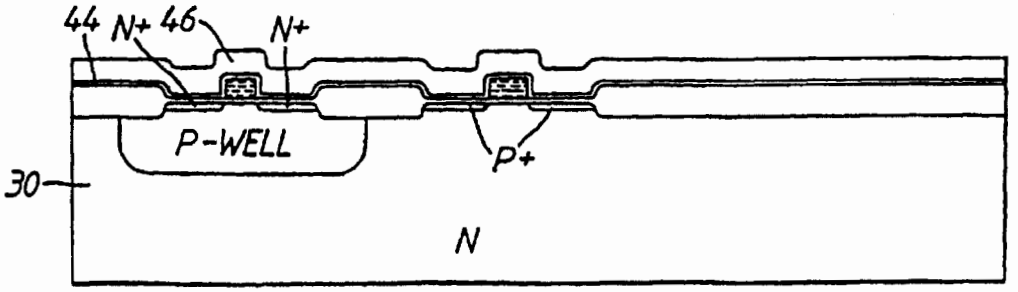

Fig.4.

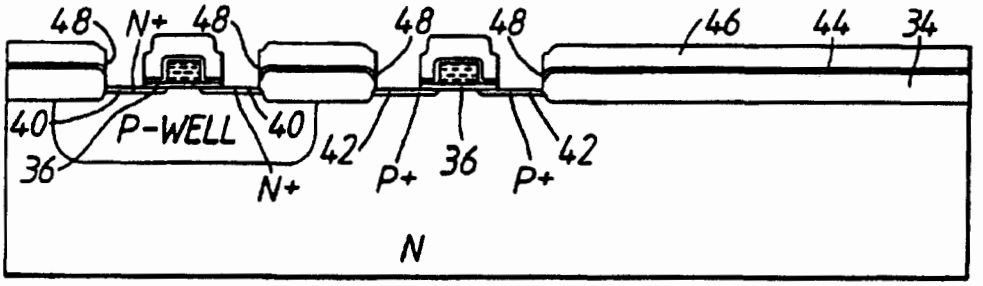

Fig. 5.

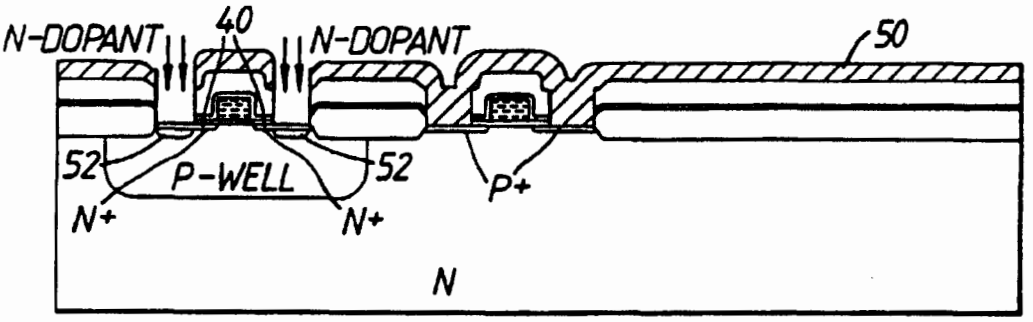

Fig. 6.

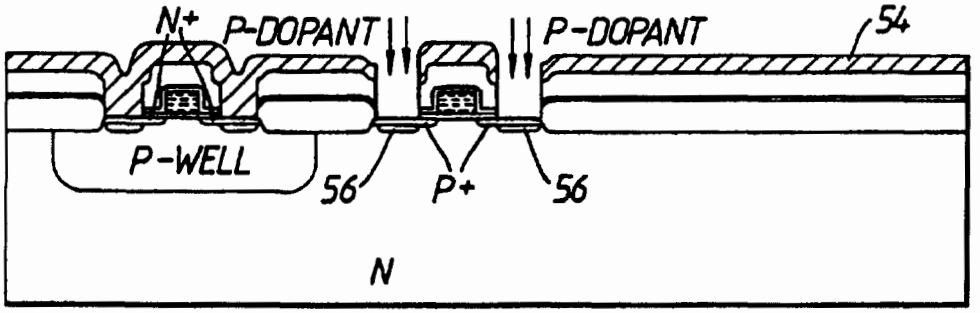

Fig. 7.

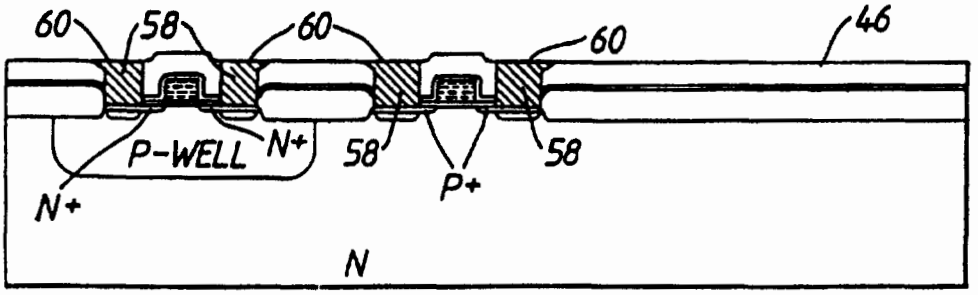

Fig. 8.

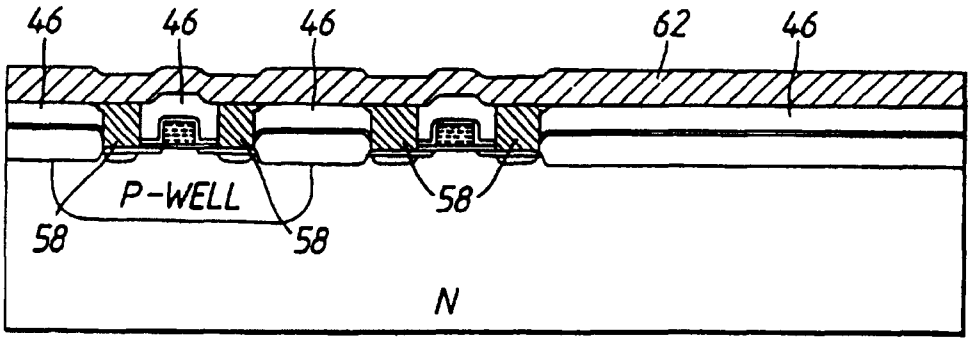

Fig.9.

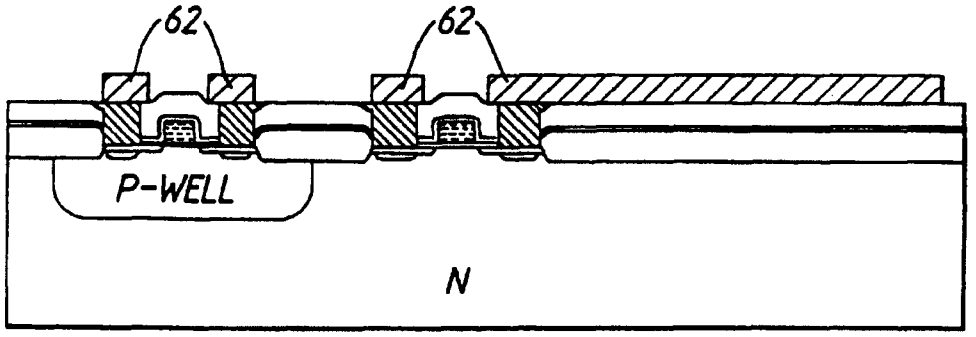

Fig.10

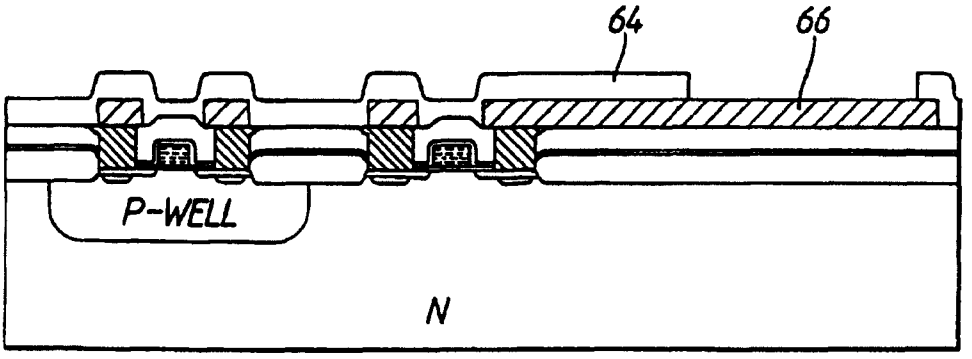

Fig.11.

SEMICONDUCTOR DEVICE WITH A TUNGSTEN CONTACT

This patent is a divisional application of Ser. No. 07/739,381, filed on Aug. 1, 1991, now abandoned, which is a Continuation of U.S. Ser. No. 07/502,526 filed Mar. 30, 1990, now abandoned.

BACKGROUND OF THE INVENTION

The present invention relates to semiconductor devices and fabrication thereof. In particular, the present invention relates to a method of fabricating a tungsten contact in a semiconductor device and to a semiconductor device incorporating such a tungsten contact.

In the manufacture of the semiconductor devices it is necessary to provide electrically conductive contacts and interconnect layers in order to connect electrically various parts of the device to each other and to external circuitry. Manufacturers of semiconductor devices have appreciated that there is a need further to reduce the size of the devices by, inter alia, reducing the size of the electrical contacts and also the interconnect pitch, without reducing the reliability of the devices and while still keeping the surface planar so that subsequent interconnect layers can be formed. Conventional methods of depositing metal contacts, such as by sputtering, have great difficulty in depositing enough material into the contact holes in order to form reliable electrical connections between the substrate silicon and the metal contact. In addition, the resulting topology is non-planar and can place severe constraints on the complexity of the interconnect layers. These technical problems are particularly encountered in the manufacture of CMOS devices which may require multiple interconnect layers.

A typical conventional CMOS device as shown in FIG. 1 which is a cross-section through a CMOS device. In this known device **2**, metal contacts **4** are provided to connect the sources and drains **6,8** of the device **2** to interconnect layers such as metal interconnect layer **10** which defines a bonding pad **12** for connection to external circuitry. The metal contacts **4** are disposed in contact holes **14** defined in the dielectric layers comprised of the field oxide layer **16** the interlevel dielectric layer **18**, and the gate oxide layer **22**. The method of manufacturing this known device has the limitation that the contact hole **14** must be wide enough and have the correct profile (i.e. it is wider at the top than at the bottom) to allow a limited amount of metal to enter the contact hole **14** thereby to form the contact **4**. The obtainable reduction in size of the contact hole is limited by the step coverage capability of conventional sputtering systems. In addition, the metal line width has to be large enough to cover the contact by at least the possible misalignment of the pattern so that the contact is protected during plasma etching of the metal to form the desired patterning of the interconnect layer. Furthermore, by making the contact hole large, any subsequent dielectric layer not only has to be capable of covering the non-planar surface resulting from previous interconnect layers but also has to cover the profile of the metal when it goes down into a contact hole. This requires an involved technique for planarising the next dielectric layer which must be used if further interconnect layers are required. From FIG. **1** it will be seen that in the resultant structure the upper surface of the top dielectric layer **20** is non-planar in the region of the metal contacts **4** and it will also be seen that the width of the metal contacts formed is substantially greater than the width of the corresponding source and drain regions of the semiconductor device which are not covered by the gate and field oxide layers **22,16**.

It has been proposed to use tungsten plug technology as a means to enhance semiconductor device planarization and to reduce interconnect pitch design rules. For example, in a paper entitled "Submicron wiring technology with tungsten and planarization" (by C. Kaanta, W. Cote, J. Cronin, K. Holland, P. Lee, and T. Wright, IEDM Conference Proceedings, 9.3, p. 209, 1987) it is disclosed that vercial contact studs can be formed from tungsten. However, it is known that such tungsten plug technology suffers substantial technical problems which are related to the agressive chemistry of the selective tungsten deposition process. In this process, tungsten is deposited by chemical vapour deposition (CVD) and the deposition is auto-catalyzed on silicon or metal surfaces and hence tungsten only deposits in contact holes which have silicon (or tungsten) exposed and not on the dielectric itself. The agressive flourine chemistry can also cause significant damage to the silicon interface and to the source/drain junction. It is well known that particular problems which can occur in the known tungsten plug technology are the phenomenon of tunnelling (which is the formation of microscopic filamentary voids in the silicon beneath the chemically vapour deposited tungsten); encroachment of the tungsten underneath the silicon/dielectric interface; consumption of the silicon by the tungsten thereby lowering the tungsten/silicon interface; and high contact resistances (especially for p+-doped silicon substrates) in the source/drain regions. A paper entitled "Conditions for tunnel formation in LPCVD tungsten films on single crystal silicon" (by R. Blewer, T. Headley and M. Tracy, Tungsten and Other Refractory Metals for VLSI Applications, ed. V. Wells, MRS Pittsburgh Pa., p.115, 1987), a paper entitled "Some recent observations on tunnel defect formation during high temperature post-deposition anneal of CVD W on Si" (by E. Broadbent, D. Sadana, A. Morgan, J. Flanner and R. Ellwanger, Workshop on Tungsten and Other Refractory Metals for VLSI Applications, ed. V. Wells, MRS Pittsburgh Pa., P. 111, 1987) and a paper entitled "Detrimental effects of residual silicon oxides on LPCVD tungsten depositions in shallow junction devices" (by R. Blewer and M. Tracy, Workshop on Tungsten and Other Refractory Metals for VLSI Applications, ed. E. Broadbent, MRS Pittsburgh Pa., P. 235, 1986) all disclose specific problems which can be encountered in the deposition of tungsten on silicon. These articles suggest procedures for reducing the occurrence of the defects in the silicon which can occur on CVD tungsten deposition. For example, it has been suggested carefully to choose the operating regimes in the CVD reactor and to control the gas purity. It has also been noted that pre-cleaning of the silicon surface can reduce the occurrence of defects in the silicon. However, the prior art fails to teach a method of fabricating a tungsten contact in the semiconductor device which can properly control the occurrence of defects such as tunnelling, encroachment of tungsten underneath the silicon/dielectric interface, consumption of the silicon and high contact resistances without compromising the inherent advantages of tungsten plug processing in a viable manufacturing technique.

British Patent Specification No. 2206234 discloses a multi-layer metallisation method for integrated circuits in which a metal sandwich structure of refractory metal/aluminium/refractory metal or alloy is deposited onto a semiconductor substrate. The refractory metal is titanium or an alloy of titanium and tungsten. Portions of the sandwich structure are removed to form interconnect and bonding pad conductors.

British Patent Specification No. 1574582 discloses a method of making a surface barrier connection to a piece of

semiconductor material in which a contact metal layer is deposited over an oxide layer on a silicon substrate. The oxide layer has a window exposing the silicon substrate. The contact metal is reacted with the silicon to form a silicide.

British Patent Specification No. 1208030 discloses a semiconductor device having metal layers contacting regions of a silicon substrate. The metal layers extend through holes in an insulating film including a lower insulating layer, a middle glass layer and an upper insulating layer. The glass layer is composed of phosphorus oxide.

SUMMARY OF THE INVENTION

The present invention aims at least partially to overcome the above specified problems of the prior art.

The present invention accordingly provides a method of fabricating a tungsten contact in a semiconductor device, which method comprises the steps of:

(a) providing an oxide layer on a region of a silicon substrate;

(b) depositing a sealing dielectric layer over the oxide layer;

(c) depositing an interlevel dielectric layer over the sealing layer;

(d) etching through the interlevel dielectric layer, the sealing dielectric layer and the oxide layer as far as the substrate thereby to form a contact hole and to expose the said region;

(e) implanting a dopant into the said region whereby the implanted dopant is self-aligned to the contact hole;

(f) thermally annealing the substrate;

(g) selectively depositing tungsten in the contact hole; and

(h) depositing an interconnect layer over the deposited tungsten contact.

Preferably, the semiconductor device is a CMOS device, and a plurality a method according to any foregoing claim wherein the semiconductor device is a CMOS device, and wherein a plurality of the tungsten contacts are fabricated over a corresponding number of the said regions, the said regions being divided into pairs of such regions, each pair of regions defining a source and a drain for a respective semiconductor element, and wherein a polysilicon gate is deposited on the said oxide layer between each pair of source and drain regions.

More preferably a first pair of source and drain regions is initially doped with an N+ dopant and is disposed in a P-doped well in the substrate which is N-doped, and during the implantation step (e) an N-dopant is implanted into the first pair of source and drain regions, and a second pair of source and drain regions is initially doped with a P+ dopant and is disposed in the N-doped substrate, and during the implantation step (e) a P-dopant is implanted into the second pair of source and drain regions.

The present invention also provides a semiconductor device incorporating a tungsten contact, the device including a silicon substrate having a region doped with a dopant; a tungsten contact disposed on the region and extending upwardly away therefrom, the tungsten contact being disposed in a contact hole which is defined in a series of dielectric layers comprising a bottom layer of oxide on the substrate, a sealing layer on the oxide layer, the sealing layer acting to seal the underlying oxide layer, and an interlevel layer on the sealing layer; and an interconnect layer which is disposed over the tungsten contact.

The said region may constitute part of a field effect transistor.

Preferably, the semiconductor device is a CMOS device and the device incorporates a plurality of the tungsten contacts which are each disposed on a respective one of a corresponding plurality of the regions, the said regions being divided into pairs of such regions, each pair of regions defining a source and a drain for a respective semiconductor element, and wherein a polysilicon gate is disposed on the said oxide layer between each pair of source and drain regions.

The present invention further provides a method of fabricating a tungsten contact in a semiconductor device, which method comprises the steps of:

(a) providing an oxide layer on a region of a silicon substrate;

(b) depositing a dielectric layer over the oxide layer;

(c) etching through the dielectric layer and the oxide layer as far as the substrate thereby to form a contact hole and to expose the said region;

(d) implanting a dopant into the said region whereby the implanted dopant is self-aligned to the contact hole;

(e) thermally annealing the substrate;

(f) selectively depositing tungsten in the contact hole; and

(g) depositing an interconnect layer over the deposited tungsten contact.

BRIEF DESCRIPTION OF THE DRAWINGS

An embodiment of the present invention will now be described by way of example only with reference to the accompanying drawings in which:

FIG. **1** is a section through a known CMOS semiconductor device;

FIG. **2** shows a section through a silicon wafer structure in a CMOS process after polysilicon gates have been deposited onto respective gate oxide layers which cover respectively doped regions of the silicon between regions of field oxide;

FIG. **3** shows a structure of FIG. **2** after deposition of a sealing dielectric layer;

FIG. **4** shows a structure of FIG. **3** after the deposition of an interlevel dielectric layer over the sealing layer;

FIG. **5** shows the structure of FIG. **4** after reflow of the interlevel dielectric layer and the etching of contact holes;

FIG. **6** shows the structure of FIG. **5** after the deposition of a photoresist pattern and during implantation of an N-dopant into N+-doped sources and drains;

FIG. **7** shows the structure of FIG. **6** after removal of the photoresist pattern of FIG. **6** and subsequent application of a second photoresist pattern and during implantation of a P-dopant into P+-doped regions of the silicon;

FIG. **8** shows the structure of FIG. **7** after removal of the second photoresist pattern, a rapid thermal anneal, and selective CVD tungsten deposition in the contact holes;

FIG. **9** shows the structure of FIG. **8** after deposition of a metal interconnect layer;

FIG. **10** shows the structure of FIG. **9** after patterned etching of the interconnect layer; and

FIG. **11** shows the structure of FIG. **10** after subsequent deposition of a patterned dielectric layer over the metal interconnect layer.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. **2**, there is shown a section through a silicon wafer structure after conventional CMOS processing.

The structure comprises a substrate **30** of N-doped silicon in which a P-well **32** has been defined by implantation and well drive in of a p-dopant such as boron. Regions **34** of field oxide are grown on the silicon layer **30** and a gate oxide layer **36** is grown over the silicon layer **30** between the field oxide regions **34**. Subsequently, polysilicon gates **38** are formed on the gate oxide layer **36**. A sequence of masking and dopant implantation steps is carried out to define N+-source and drain regions **40** in the P-well **32** and P+-source and drain regions **42** in the N-doped substrate **30**. The gates **38** are also doped with the appropriate N- or P-dopant as the case may be. It should be noted that this conventional CMOS processing is independent of the choice of CMOS structure, which may be N-well, P-well or twin-well, and is independent of the transistor formation and the isolation formation.

Referring now to FIG. **3**, in accordance with the present invention a sealing dielectric layer **44** is deposited over the oxide layer which comprises the field oxide **34** and the gate oxide **36**. The sealing dielectric layer **44** comprises a CVD silicon nitride layer having a thickness of from 200 to 600 A. Typically, the silicon nitride layer **44** is deposited at a pressure of from 290 to 350 millitor and at a temperature of 750° C. using $SiCl_2H_2$ and NH_3 to produce a layer having a refractive index of 2.00±0.05. As is shown in FIG. **4**, an interlevel dielectric layer **46** is subsequently deposited over the silicon nitride layer **44**. The interlevel dielectric layer **46** must be composed of a material which is compatible with subsequent selective tungsten processing, i.e. it must not promote the growth of tungsten on its surface. A preferred interlevel dielectric material is borophosphosilicate glass (BPSG) deposited at atmospheric pressure and at a temperature of 450° C. using O_2, SiH_4, B_2H_6, and PH_3 to give a layer with 3% boron concentration and 5% phosphorus concentration. The BPSG interlevel dielectric is reflowable and after deposition of the interlevel dielectric layer **46** the composite structure is subjected to dielectric densification and reflow by heating the structure at a temperature of at least 900° C. for at least 30 minutes. This heating step provides the multiple function of repairing and annealing out any damage in the silicon caused by previous implantations; sealing the nitride/silicon interface; and densifying the dielectric layer.

Subsequently, a photoresist pattern is formed over the interlevel dielectric layer **46** which selectively exposes areas of the interlevel dielectric layer **46** in which the tungsten contacts are subsequently to be formed. The structure is then etched by means of any suitable plasma etch system capable of anisotropically etching silicon dioxide with a selectivity to silicon of greater than 7:1. A preferred etch involves a 7:1 H_2O:HF dip for 60 seconds to clean the surface of the exposed BPSG followed by a C_2F_6/CHF_3 plasma etch. This etching step etches down through the interlevel dielectric layer **46**, the sealing dielectric layer **44**, and the gate oxide layer **36** as far as the silicon substrate thereby to form contact holes **48** in the series of dielectric layers which contact holes **41** are aligned with the source and drain regions **40,42**. The resultant structure is shown in FIG. **5**. The etching step exposes the source and drain regions **40,42** of the substrate **30** and the P-well **32**. The contact hole **48** has substantially vertical sides as is shown in FIG. **5**.

Referring now to FIG. **6**, a photoresist pattern **50** is formed over the structure of FIG. **5**, the photoresist pattern **50** exposing all of the areas of N+-silicon **40**. A N-dopant (e.g. phosphorous) enhancement implant is then carried-out. This implant increases the junction depth and the N-type dopant surface concentration to give an increased tolerance to damage during subsequent processing and to lower the N+-contact resistance respectively. The implant is self-aligned to the ultimate tungsten contact since the sides of the contact hole **48** define the lateral dimensions of the implanted regions. The enhanced implanted regions **52** are shown in FIG. **6**. The photoresist pattern **50** is then removed.

Referring to FIG. **7**, a further photoresist pattern **54** is then formed over the structure and the photoresist pattern **54** exposes all the areas of P+-silicon **42**. A P-dopant (e.g. boron) is then implanted as an enhancement implant into the exposed areas of the P+-silicon **42** thereby to provide implanted regions **56** which are self-aligned to the ultimate tungsten contacts. Again, the enhancement implant increases the junction depth and the P-dopant surface concentration to give a tolerance to damage during subsequent processing and to lower the P+-contact resistance respectively. The photoresist pattern **54** is then removed. A preferred final step for this photoresist removal consists of an oxygen-containing plasma treatment to remove residual polymer.

The resultant structure is then subjected to a rapid thermal anneal at a temperature high enough to repair any damage to the silicon which may have resulted from the implants and low enough to retain near-vertical contact well profiles. The preferred process is a rapid thermal anneal at a temperature of about 1035° C. for 5 seconds in an argon atmosphere.

The next stage in the processing is the precleaning of the exposed regions of the silicon prior to selective tungsten deposition. The exposed regions of silicon are precleaned initially by treatment with an organic removing agent such as sulphuric acid or nitric acid. The exposed regions are then further precleaned preferably by treatment with hydrofluoric acid which has been buffered with ammonium fluoride in a ratio of at least 1:40 for at least 3 minutes. A final pretreatment step of H_2 or NF_3 in a plasma environment at a pressure of less than 500 mTorr and a temperature of less than 450° C. can be carried out immediately before deposition to act as a final preparation of the surface. Deposition should then take place following this step without breaking the vacuum.

Subsequently, CVD tungsten is selectively deposited in the contact holes **48** in order to fill the holes and to planarize them, i.e. the upper surface of the tungsten plugs is substantially aligned with the upper surface of the dielectric. The resultant structure is shown in FIG. **8** in which tungsten contacts **58** having planar upper surfaces **60** are disposed in the contact holes **48**. A preferred CVD tungsten deposition process is carried out at a temperature of about 230° C. and at a pressure of less than 250 millitorr using WF_6, SiH_4 and H_2. Preferably, both the WF_6 and the SiH_4 partial pressures are less than 3% of the total pressure.

As is shown in FIG. **9**, the next step is the deposition over the interlevel dielectric layer **46** and the tungsten contacts **58** of a metal interconnect layer **62**. The metal interconnect layer **62** may be deposited by conventional sputtering methods. Next, a photoresist pattern is formed on the metal interconnect layer **62** which covers areas which are to form the ultimate patterned interconnect layer underneath which are disposed the tungsten contacts **58** which connect to the silicon. The metal interconnect layer **62** is then anisotropically etched in any plasma etch system which is capable of etching the metal with a selectivity to silicon dioxide and tungsten which is sufficient to remove less than 2000 A of either material. The photoresist is then removed. The resultant structure is shown in FIG. **10** in which respective portions of the patterned metal interconnect layer **62** are disposed over respective tungsten contacts **58**.

The remaining steps to manufacture this semiconductor device are standard CMOS process steps and include the deposition over the metal interconnect layer **62** of a top layer of oxide **64** which defines a bonding pad **66** of the metal interconnect layer **62**. The structure of the resultant FET semiconductor device is shown in FIG. **11**.

By employing the process steps described above, the present inventors have discovered that the encroachment of tungsten underneath the dielectric/silicon interface is minimized and also that the consumption of silicon and damage to the silicon resulting from the tungsten deposition can also be minimized.

As far as silicon encroachment is concerned, this phenomenon is characterised by a lateral growth of deposited tungsten along the relatively high energy boundary between the oxide layer and the silicon substrate. Such encroachment can lead to electrical shorting by the tungsten formed between laterally adjacent structures of the semiconductor device. The present inventors have discovered surprisingly that the presence of a silicon nitride layer, which acts as a sealing and barrier layer, in the region of the junction of the oxide and the silicon reduces the tendency for lateral encroachment of the tungsten at the bottom of the contact hole. Without wishing to be bound by theory, the present inventors believe that the mechanism of tungsten encroachment, and the reason why the silicon nitride layer can assist reduction of the encroachment phenomenon are as follows. Tungsten encroachment requires rapid diffusion of tungsten fluorides (which may be in the form of subfluorides) along the oxide/silicon interface. The tungsten fluorides react with the silicon to form tungsten. The sealing barrier dielectric layer of silicon nitride resists mechanical deformation and accordingly modifies the resulting stress in the layers, thus causing a reduction in the diffusion of fluorides along the interface and hence a reduction in the encroachment of tungsten. The sealing barrier dielectric layer has high stress so that the accumulative stress in the layers inhibits diffusion along the silicon/oxide interface. The interlevel dielectric layer of BPSG, also resists the mechanical deformation of the sealing dielectric layer. The result is that the encroachment of tungsten can be limited to about 0.1 um which is about the same distance as the depth of silicon consumption beneath the tungsten plug.

The sealing dielectric layer of the illustrated embodiment is silicon nitride. However, the sealing dielectric layer may be composed of other substances having high density and a high dielectric constant. The sealing dielectric layer must be compatible with the silicon, oxide, tungsten and interlevel interconnect to which it is adjacent and must provide mechanical resistance as described above, to diffusion of fluorides along the interface by modifying the stress in the films. The sealing dielectric layer should be resistant to mechanical deformation but not brittle and it should also have a low diffusion coefficient to gases such as hydrogen, fluorine and gaseous fluorides. The sealing dielectric layer may alternatively be comprised of TiO_2, WO_2, ZrO_2, HfO_2 or other insulating refractories or rare earth metal oxides which have the physical characteristics referred to above.

In addition, the rapid thermal anneal step tends to remove any implantation damage in the silicon at the bottom of the contact hole and it is believed that this reduces the energy at the oxide/silicon interface which again minimizes encroachment of the tungsten at the interface.

As far as minimization of silicon consumption and damage to the silicon is concerned, the present inventors believe that this is at least partially achieved by the implantation steps and the rapid thermal anneal step. With the n-dopant implant (i.e. phosphorous), the implant causes the N+-regions to be deeper and in addition the rapid thermal anneal causes driving-in of the N-dopant implant. The result of this is that even if some of the silicon of the N+-region **40** is consumed by the tungsten during tungsten deposition, nevertheless the N+-implant is sufficiently deep so as not substantially to be affected by the tungsten thereby affecting the subsequent operation of the source/drain regions. Typically, the junction depth is about 0.25 um whereas about 0.1 um of silicon is removed by the tungsten deposition. The implant ensures sufficient resultant junction depth for the operation of the device not to be jeopardised by the removal of an upper part of the silicon during tungsten deposition. Similarly, for the P-dopant (i.e. boron) implant, this also provides a deeper P+-region **42** which is enhanced by the rapid thermal anneal which drives the P-dopant deeper into the silicon substrate. In addition, this also gives a higher P+-concentration at the interface with the tungsten which results in an improved electrical contact between the tungsten and the P+-region which consequently lowers the contact resistance of the P+-sources and drains. The rapid thermal anneal actuates the implant without causing diffusion of the implant. This removes defects in the silicon lattice. The rapid thermal anneal also smooths out the BPSG interlevel dielectric layer which leads to improved tungsten deposition since the "window" through which the tungsten is deposited into the contact hole is wider at its entrance. Furthermore, the rapid thermal anneal step can cause at least partial recrystallisation of the silicon which can remove damage to the silicon caused by the earlier processing i.e. implantation steps.

Additionally, the present inventors believe that the precleaning and contact etching steps tend to minimize the occurrence of defects such as tunnelling by reducing impurities such as oxide impurities on the exposed regions of silicon which can promote defect formation.

In addition, the present invention provides a further advantage in that it can provide protection against etch damage to the tungsten contacts which can occur when defining the interconnect layer by removing the need for overlap of the metal interconnect layer over the contacts since the tungsten contacts are accurately aligned with respect to the sources and drains. The interconnect widths no longer need to overlap on either side of the contact to eliminate etch damage which can occur in the processes of the prior art.

In summary, the primary advantage of the present invention is that it can enable selectively deposited tungsten contact plugs to be integrated into standard CMOS process flows whilst minimizing the detrimental effects which were reported in the prior art resulting from CVD tungsten depositions on silicon substrates.

What we claim is:

1. A semiconductor device incorporating a tungsten contact, the device including a silicon substrate having a doped region which is doped with a dopant; a tungsten contact disposed on the region and extending upwardly away therefrom, the tungsten contact being disposed in a contact hole which is defined in a series of dielectric layers comprising a bottom layer of oxide on the substrate, a sealing layer on the oxide layer, the sealing layer acting to seal the underlying oxide layer, and an interlevel layer on the sealing layer; and an interconnect layer which is disposed over the tungsten contact, the interconnect layer being non-overlapping on at least one side of the contact.

2. A semiconductor device according to claim **1** wherein the said region is aligned with the contact hole in which the tungsten contact is disposed.

3. A semiconductor device according to claim 1 wherein the sealing dielectric layer is composed of a substance which can act mechanically to modify the stress at the interface between the oxide layer and the silicon substrate.

4. A semiconductor device according to claim 3 wherein the sealing dielectric layer is composed of silicon nitride.

5. A semiconductor device according to claim 1 wherein the interlevel dielectric layer is composed of a reflowable material.

6. A semiconductor device according to claim 1 wherein the said region constitutes part of a field effect transistor.

7. A semiconductor device according to claim 1 which is a CMOS device, and wherein the device incorporates a plurality of the tungsten contacts which are each disposed on a respective one of a corresponding plurality of the regions, the said regions being divided into pairs of such regions, each pair of regions defining a source and a drain for a respective semiconductor element, and wherein a polysilicon gate is disposed on the said oxide layer between each pair of source and drain regions.

8. A semiconductor device according to claim 1 wherein encroachment of tungsten from the contact along an interface between the oxide layer and the silicon substrate is up to about 0.1 microns.

9. A semiconductor device comprising:

a silicon substrate including a region doped with a dopant;

a bottom dielectric oxide layer disposed over said silicon substrate;

a sealing dielectric layer disposed over said dielectric oxide layer, said sealing layer mechanically modifying stresses at the interface between said silicon substrate and said dielectric oxide layer so as to impede the lateral diffusion of tungsten into the interface between said substrate and said oxide layer;

an interlevel dielectric layer disposed over said sealing dielectric layer;

a tungsten plug member disposed in contact with said region doped with a dopant and extending up through a contact hole etched through said bottom dielectric oxide layer, said sealing dielectric layer, and said interlevel dielectric layer; and

an interconnect layer disposed over said tungsten plug member, the interconnect layer having no overlap over at least one side of the tungsten plug member.

10. A semiconductor device according to claim 9 wherein the region doped with a dopant is aligned with the contact hole in which the tungsten plug member is disposed.

11. A semiconductor device according to claim 9 wherein the sealing layer comprises silicon nitride.

12. A semiconductor device according to claim 11 wherein the oxide layer comprises a gate oxide layer and the sealing layer has a thickness of from 200 to 600 Angstroms.

13. A semiconductor device according to claim 9 wherein encroachment of tungsten from the contact along an interface between the oxide layer and the silicon substrate is up to about 0.1 microns.

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