IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

HITACHI CONSUMER ELECTRONICS CO., LTD., and HITACHI ADVANCED DIGITAL, INC.

Plaintiff,

v.

TOP VICTORY ELECTRONICS (TAIWAN) CO. LTD., TPV INT'L (USA), INC., ENVISION PERIPHERALS, INC., TOP VICTORY ELECTRONICS (FUJIAN) CO. LTD., TPV ELECTRONICS (FUJIAN) CO. LTD., TPV TECHNOLOGY LTD., and VIZIO, INC.,

Defendants;

and

VIZIO, INC.,

Counterclaim-Plaintiff,

v.

HITACHI, LTD., HITACHI CONSUMER ELECTRONICS CO., LTD., HITACHI ADVANCED DIGITAL, INC., HITACHI AMERICA, LTD., and HITACHI HOME ELECTRONICS (AMERICA), INC.

Counterclaim-Defendants,

CIVIL ACTION NO. 2:10-CV-260-JRG

JURY

FIRST AMENDED COMPLAINT

Plaintiffs Hitachi Consumer Electronics Co., Ltd. ("HCE") and Hitachi Advanced Digital, Inc. ("HAD") (collectively, "Plaintiffs"), by way of this First Amended Complaint

against Defendants Top Victory Electronics (Taiwan) Co. Ltd., TPV Int'l (USA), Inc., Envision Peripherals, Inc., Top Victory Electronics (Fujian) Co. Ltd., TPV Electronics (Fujian) Co. Ltd., TPV Technology Ltd., (collectively, ""TPV") and Vizio, Inc. ("Vizio"), hereby allege as follows:

NATURE OF THE ACTION

1. This is an action for patent infringement arising under the Patent Laws of the United States, 35 U.S.C. § 101, *et seq*.

THE PARTIES

2. Plaintiff Hitachi Consumer Electronics Co. Ltd. ("HCE") is a corporation organized under the laws of Japan with its principal place of business at 2-1, Otemachi 2-chome Chiyoda-ku Tokyo, Japan. HCE is a wholly-owned subsidiary of Hitachi, Ltd. (Tokyo, Japan).

3. Plaintiff Hitachi Advanced Digital, Inc. ("HAD") is a corporation organized under the laws of Japan with its principal place of business at 292, Yoshidacho, Totsuka-Ku, Yokohama, Kanagawa, Japan. HAD is a wholly-owned subsidiary of Hitachi, Ltd. (Tokyo, Japan).

4. On information and belief, Defendant Top Victory Electronics (Taiwan) Co. Ltd. is a corporation organized under the laws of Taiwan with its principal place of business at 10F, No. 230, Liancheng Road, Zhonghe City, Taipei County, Taiwan.

5. On information and belief, Defendant TPV Int'l (USA), Inc. is a corporation organized under the laws of California with its principal place of business at 3737 Executive Center Drive, Suite 261, Austin, Texas 78731, and with a registered agent at 350 North St. Paul Street, Suite 2900, Dallas, Texas 75201.

6. On information and belief, Defendant Envision Peripherals, Inc. is a corporation organized under the laws of California with its principal place of business at 47490 Seabridge Drive, Fremont, California 94538, and with a registered agent at 350 North St. Paul Street, Suite 2900, Dallas, Texas 75201.

7. On information and belief, Defendant Top Victory Electronics (Fujian) Co. Ltd. is a corporation organized under the laws of the People's Republic of China with its principal place of business at Shangzheng Yuanhong Road, Fuquing City, Fujian Province, China.

8. On information and belief, Defendant TPV Electronics (Fujian) Co. Ltd. is a corporation organized under the laws of the People's Republic of China with its principal place of business at Shangzheng Yuanhong Road, Fuquing City, Fujian Province, China.

9. On information and belief, TPV Technology Ltd. is a corporation organized under the laws of Bermuda with its principal place of business at Suite 1023, Ocean Centre, Harbour City, Kowloon, Hong Kong.

10. On information and belief, the companies identified in paragraphs 4-9 above (collectively, "TPV") are an interrelated group of companies that together comprise one of the world's largest manufacturers of televisions. TPV is a leading importer and seller of televisions in the United States.

11. On information and belief, Vizio, Inc. is a corporation organized under the laws of California with its principal place of business at 39 Tesla, Irvine, California 92618, and with a registered agent at 350 North St. Paul Street, Suite 2900, Dallas, Texas 75201. Vizio is a leading seller of televisions in the United States.

12. Hitachi America Ltd. ("HAL") is a corporation organized under the laws of New York with its principal place of business at 50 Prospect Avenue, Tarrytown, NY 10591. HAL is a wholly-owned subsidiary of Hitachi, Ltd. (Tokyo, Japan). HAL markets and sells ATSC-compatible televisions that practice the Patents-in-Suit in the United States. HAL and Hitachi, Ltd. have been and continue to be harmed by Defendants' infringement of the patents-in-suit.

JURISDICTION AND VENUE

13. This is an action for patent infringement arising under the patent laws of the United States, Title 35 of the United States Code. In this lawsuit, Plaintiffs allege infringement of U.S. Patent Nos. 5,502,497, 5,534,934, 6,037,995, 6,388,713, 6,549,243, 7,012,769, 7,286,310, 6,144,412, 7,889,281, and 8,009,375 (the "Patents-in-Suit"). This Court has jurisdiction over the subject matter of this action under 28 U.S.C. §§ 1331 and 1338(a). Venue is proper in this judicial district under 28 U.S.C. §§ 1391(b), (c), (d) and 1400(b).

14. TPV designs, manufactures and assembles televisions. TPV imports, offers to sell, and sells those televisions in the United States, including in the State of Texas generally and this judicial district in particular. In addition, TPV has created a well-established distribution chain for its televisions, and that distribution chain delivers those products into the United States, including the State of Texas generally and this judicial district in particular. Furthermore, TPV knows, expects, and intends that by selling televisions designed for use in the U.S. market, some of those products will be sold in the State of Texas, including in this judicial district.

15. Vizio designs and specifies televisions for sale and use in the United States. Vizio imports, offers for sale, and sells televisions in the United States, including in the State of Texas generally and this judicial district in particular. Vizio has created a well-established distribution

chain for its televisions, and that distribution chain delivers those products into the United States, including the State of Texas generally and this judicial district in particular. Furthermore, Vizio knows, expects, and intends that by selling televisions designed for use in the U.S. market, some of those products will be sold in the State of Texas, including in this judicial district.

16. The six TPV defendants identified in paragraphs 4-9 above operate as a unitary business venture and are jointly and severally liable for patent infringement relating to the televisions made, imported, offered for sale, sold, or used in the United States by any one of them. Plaintiffs' right to relief against each of these six defendants arises out of the same transaction, occurrence, or series of transactions or occurrences relating to the importing, offering for sale, and sale of the same accused television units in the United States. Additionally, questions of fact common to all six of these defendants will arise in this action, including whether these same television units infringe the asserted patents. Therefore, joinder of these TPV defendants is proper.

17. In addition, TPV manufactures and imports into the United States and sells certain accused televisions to Vizio. In turn, Vizio offers to sell and sells these same accused televisions in the United States under its own brand name. These televisions include, but are not limited to, Vizio models: E320VA, E420VT, M220VA, and VA26LHDTV10T. TPV and Vizio are jointly and severally liable for patent infringement relating to at least these accused televisions. Further, on information and belief, TPV has contractually indemnified and agreed to defend Vizio against claims of patent infringement, such as those alleged herein, brought against Vizio for TPV supplied televisions. Moreover, HCE's right to relief arises out of the same transaction, occurrence, or series of transactions or occurrences relating to the importing, offering for sale,

and selling of the same accused television units in the United States by the Defendants. In addition, questions of fact common to all Defendants will arise in the action. These questions include whether these same televisions, imported and sold by TPV and then sold by Vizio, infringe the asserted patents. Therefore, joinder of these Defendants is proper.

COUNT I – INFRINGEMENT OF U.S. PATENT NO. 5,502,497

18. Plaintiffs repeat and reallege the allegations of the preceding paragraphs as if set forth herein.

19. On March 26, 1996, U.S. Patent No. 5,502,497 ("the '497 Patent) entitled TELEVISION BROADCASTING METHOD AND SYSTEM ENABLING PICTURE BROADCASTING FROM THE TRANSMITTING EQUIPMENT TO THE RECEIVING EQUIPMENT USING ALTERNATIVE BROADCASTING SYSTEM STANDARDS, was duly and legally issued by the United States Patent and Trademark Office. A true and correct copy of the '497 Patent is attached as Exhibit A to this Complaint.

20. HCE is the assignee and owner of the right, title, and interest in and to the '497 Patent, including the right to assert all causes of action arising under said patent, the right to recover damages for past, present, or future infringement of the patent, and the right to any other remedies for infringement of the patent.

21. TPV has been directly infringing and continues to directly infringe, either literally or under the doctrine of equivalents, the '497 Patent by importing, offering to sell, and selling Advanced Television Systems Committee (ATSC) compatible televisions that embody or practice the claimed inventions. In addition, Vizio, TPV's customer, directly infringes the '497 Patent by offering to sell and selling, among other things, TPV-supplied televisions in the United

States. Further, end users in the United States directly infringe the '497 Patent by using their TPV-manufactured televisions. TPV, with knowledge of the '497 Patent, has and does possess the specific intent to encourage Vizio and end users to directly infringe the '497 Patent. TPV is therefore liable to HCE under at least 35 U.S.C. §§ 271(a) and (b).

22. Vizio has been directly infringing and continues to directly infringe, either literally or under the doctrine of equivalents, the '497 Patent by importing, offering to sell, and selling ATSC-compatible televisions, including both TPV and non-TPV supplied units, that embody or practice the claimed inventions. Further, end users in the United States directly infringe the '497 Patent by using their Vizio televisions. Vizio, with knowledge of the '497 Patent, has and does possess the specific intent to encourage end users to directly infringe the '497 Patent. Vizio is therefore liable to HCE under at least 35 U.S.C. §§ 271(a) and (b).

23. On information and belief, Defendants have continued to infringe the '497 Patent despite being on notice of the patent, and their infringement of the patent, since before the filing of the original complaint on July 22, 2010.

24. On information and belief, Defendants' acts of infringement as set out in the previous paragraphs have been and continue to be deliberate, willful, and in reckless disregard of HCE's patent rights.

25. HCE has been damaged by Defendants' infringing activities. On information and belief, Defendants will continue their infringing activities, and thus continue to damage HCE, unless enjoined by this Court. HCE has no adequate remedy at law.

COUNT II – INFRINGEMENT OF U.S. PATENT NO. 5,534,934

26. Plaintiffs repeat and reallege the allegations of the preceding paragraphs as if set forth herein.

27. On July 9, 1996, U.S. Patent No. 5,534,934 ("the '934 Patent") entitled TELEVISION RECEIVER CAPABLE OF ENLARGING AND COMPRESSING IMAGE, was duly and legally issued by the United States Patent and Trademark Office. A true and correct copy of the '934 Patent is attached as Exhibit B to this Complaint.

28. HCE is the assignee and owner of the right, title, and interest in and to the '934 Patent, including the right to assert all causes of action arising under said patent, the right to recover damages for past, present, or future infringement of the patent, and the right to any other remedies for infringement of the patent.

29. TPV has been directly infringing and continues to directly infringe, either literally or under the doctrine of equivalents, the '934 Patent by importing, offering to sell, and selling ATSC-compatible televisions that embody or practice the claimed inventions. In addition, Vizio, TPV's customer, directly infringes the '934 Patent by offering to sell and selling, among other things, TPV-supplied televisions in the United States. Further, end users in the United States directly infringe the '934 Patent by using their TPV-manufactured televisions. TPV, with knowledge of the '934 Patent, has and does possess the specific intent to encourage Vizio and end users to directly infringe the '934 Patent. TPV is therefore liable to HCE under at least 35 U.S.C. §§ 271(a) and (b).

30. Vizio has been directly infringing and continues to directly infringe, either literally or under the doctrine of equivalents, the '934 Patent by importing, offering to sell, and selling ATSC-compatible televisions, including both TPV and non-TPV supplied units, that

embody or practice the claimed inventions. Further, end users in the United States directly infringe the ’934 Patent by using their Vizio televisions. Vizio, with knowledge of the ’934 Patent, has and does possess the specific intent to encourage end users to directly infringe the ’934 Patent. Vizio is therefore liable to HCE under at least 35 U.S.C. §§ 271(a) and (b).

31. On information and belief, Defendants have continued to infringe the ’934 Patent despite being on notice of the patent, and their infringement of the patent, since before the filing of the original complaint.

32. On information and belief, Defendants’ acts of infringement as set out in the previous paragraphs have been and continue to be deliberate, willful, and in reckless disregard of HCE’s patent rights.

33. HCE has been damaged by Defendants’ infringing activities. On information and belief, Defendants will continue their infringing activities, and thus continue to damage HCE, unless enjoined by this Court. HCE has no adequate remedy at law.

COUNT III – INFRINGEMENT OF U.S. PATENT NO. 6,037,995

34. Plaintiffs repeat and reallege the allegations of the preceding paragraphs as if set forth herein.

35. On March 14, 2000, U.S. Patent No. 6,037,995 (the ’995 Patent”) entitled BROADCASTING AND COMMUNICATION RECEIVER APPARATUS, was duly and legally issued by the United States Patent and Trademark Office. A true and correct copy of the ’995 Patent is attached as Exhibit C to this Complaint.

36. HCE is the assignee and owner of the right, title, and interest in and to the ’995 Patent, including the right to assert all causes of action arising under said patent, the right to

recover damages for past, present, or future infringement of the patent, and the right to any other remedies for infringement of the patent.

37. TPV has been directly infringing and continues to directly infringe, either literally or under the doctrine of equivalents, the '995 Patent by importing, offering to sell, and selling ATSC-compatible televisions that embody or practice the claimed inventions. In addition, Vizio, TPV's customer, directly infringes the '995 Patent by offering to sell and selling, among other things, TPV-supplied televisions in the United States. Further, end users in the United States directly infringe the '995 Patent by using their TPV-manufactured televisions. TPV, with knowledge of the '995 Patent, has and does possess the specific intent to encourage Vizio and end users to directly infringe the '995 Patent. TPV is therefore liable to HCE under at least 35 U.S.C. §§ 271(a) and (b).

38. Vizio has been directly infringing and continues to directly infringe, either literally or under the doctrine of equivalents, the '995 Patent by importing, offering to sell, and selling ATSC-compatible televisions, including both TPV and non-TPV supplied units, that embody or practice the claimed inventions. Further, end users in the United States directly infringe the '995 Patent by using their Vizio televisions. Vizio, with knowledge of the '995 Patent, has and does possess the specific intent to encourage end users to directly infringe the '995 Patent. Vizio is therefore liable to HCE under at least 35 U.S.C. §§ 271(a) and (b).

39. On information and belief, Defendants have continued to infringe the '995 Patent despite being on notice of the patent, and their infringement of the patent, since before the filing of the original complaint.

40. On information and belief, Defendants' acts of infringement as set out in the previous paragraphs have been and continue to be deliberate, willful, and in reckless disregard of HCE's patent rights.

41. HCE has been damaged by Defendants' infringing activities. On information and belief, Defendants will continue their infringing activities, and thus continue to damage HCE, unless enjoined by this Court. HCE has no adequate remedy at law.

COUNT IV – INFRINGEMENT OF U.S. PATENT NO. 6,388,713

42. Plaintiffs repeat and reallege the allegations of the preceding paragraphs as if set forth herein.

43. On January 28, 2003, U.S. Patent No. 6,388,713 ("the '713 Patent"), entitled IMAGE DISPLAY APPARATUS, AND METHOD TO PREVENT OR LIMIT USER ADJUSTMENT OF DISPLAYED IMAGE QUALITY, was duly and legally issued by the United States Patent and Trademark Office. A true and correct copy of the '713 Patent is attached as Exhibit D to this Complaint.

44. HCE is the assignee and co-owner of the right, title, and interest in and to the '713 Patent, including the right to assert all causes of action arising under said patent, the right to recover damages for past, present, or future infringement of the patent, and the right to any other remedies for infringement of the patent.

45. HAD is the assignee and co-owner of the right, title, and interest in and to the '713 Patent, including the right to assert all causes of action arising under said patent and the right to any remedies for infringement of it.

46. TPV has been directly infringing and continues to directly infringe, either literally or under the doctrine of equivalents, the ’713 Patent by importing, offering to sell, and selling ATSC-compatible televisions that embody or practice the claimed inventions. In addition, Vizio, TPV’s customer, directly infringes the ’713 Patent by offering to sell and selling, among other things, TPV-supplied televisions in the United States. Further, end users in the United States directly infringe the ’713 Patent by using their TPV-manufactured televisions. TPV, with knowledge of the ’713 Patent, has and does possess the specific intent to encourage Vizio and end users to directly infringe the ’713 Patent. TPV is therefore liable to HCE under at least 35 U.S.C. §§ 271(a) and (b).

47. Vizio has been directly infringing and continues to directly infringe, either literally or under the doctrine of equivalents, the ’713 Patent by importing, offering to sell, and selling ATSC-compatible televisions, including both TPV and non-TPV supplied units, that embody or practice the claimed inventions. Further, end users in the United States directly infringe the ’713 Patent by using their Vizio televisions. Vizio, with knowledge of the ’713 Patent, has and does possess the specific intent to encourage end users to directly infringe the ’713 Patent. Vizio is therefore liable to HCE under at least 35 U.S.C. §§ 271(a) and (b).

48. On information and belief, Defendants have continued to infringe the ’713 Patent despite being on notice of the patent, and their infringement of the patent, since before the filing of the original complaint.

49. On information and belief, Defendants’ acts of infringement as set out in the previous paragraphs have been and continue to be deliberate, willful, and in reckless disregard of Plaintiffs’ patent rights.

50. Plaintiffs have been damaged by Defendants' infringing activities. On information and belief, Defendants will continue their infringing activities, and thus continue to damage Plaintiffs, unless enjoined by this Court. Plaintiffs have no adequate remedy at law.

COUNT V – INFRINGEMENT OF U.S. PATENT NO, 6,549,243

51. Plaintiffs repeat and reallege the allegations of the preceding paragraphs as if set forth herein.

52. On April 15, 2003, U.S. Patent No. 6,549,243 ("the '243 Patent"), entitled DIGITAL BROADCAST RECEIVER UNIT, was duly and legally issued by the United States Patent and Trademark Office. A true and correct copy of the '243 Patent is attached as Exhibit E to this Complaint.

53. HCE is the assignee and owner of the right, title, and interest in and to the '243 Patent, including the right to assert all causes of action arising under said patent, the right to recover damages for past, present, or future infringement of the patent, and the right to any other remedies for infringement of the patent.

54. TPV has been directly infringing and continues to directly infringe, either literally or under the doctrine of equivalents, the '243 Patent by importing, offering to sell, and selling ATSC-compatible televisions that embody or practice the claimed inventions. In addition, Vizio, TPV's customer, directly infringes the '243 Patent by offering to sell and selling, among other things, TPV-supplied televisions in the United States. Further, end users in the United States directly infringe the '243 Patent by using their TPV-manufactured televisions. TPV, with knowledge of the '243 Patent, has and does possess the specific intent to encourage Vizio and

end users to directly infringe the ’243 Patent. TPV is therefore liable to HCE under at least 35 U.S.C. §§ 271(a) and (b).

55. Vizio has been directly infringing and continues to directly infringe, either literally or under the doctrine of equivalents, the ’243 Patent by importing, offering to sell, and selling ATSC-compatible televisions, including both TPV and non-TPV supplied units, that embody or practice the claimed inventions. Further, end users in the United States directly infringe the ’243 Patent by using their Vizio televisions. Vizio, with knowledge of the ’243 Patent, has and does possess the specific intent to encourage end users to directly infringe the ’243 Patent. Vizio is therefore liable to HCE under at least 35 U.S.C. §§ 271(a) and (b).

56. On information and belief, Defendants have continued to infringe the ’243 Patent despite being on notice of the patent, and their infringement of the patent, since before the filing of the original complaint.

57. On information and belief, Defendants’ acts of infringement as set out in the previous paragraphs have been and continue to be deliberate, willful, and in reckless disregard of HCE’s patent rights.

58. HCE has been damaged by Defendants’ infringing activities. On information and belief, Defendants will continue their infringing activities, and thus continue to damage HCE, unless enjoined by this Court. HCE has no adequate remedy at law.

COUNT VI – INFRINGEMENT OF U.S. PATENT NO. 7,012,769

59. Plaintiffs repeat and reallege the allegations of the preceding paragraphs as if set forth herein.

60. On March 14, 2006, U.S. Patent No. 7,012,769 ("the '769 Patent") entitled DIGITAL INFORMATION RECORDING/REPRODUCING APPARATUS, was duly and legally issued by the United States Patent and Trademark Office. A true and correct copy of the '769 Patent is attached as Exhibit F to this Complaint.

61. HCE is the assignee and owner of the right, title, and interest in and to the '769 Patent, including the right to assert all causes of action arising under said patent, the right to recover damages for past, present, or future infringement of the patent, and the right to any other remedies for infringement of the patent.

62. TPV has been directly infringing and continues to directly infringe, either literally or under the doctrine of equivalents, the '769 Patent by importing, offering to sell, and selling ATSC-compatible televisions that embody or practice the claimed inventions. In addition, Vizio, TPV's customer, directly infringes the '769 Patent by offering to sell and selling, among other things, TPV-supplied televisions in the United States. Further, end users in the United States directly infringe the '769 Patent by using their TPV-manufactured televisions. TPV, with knowledge of the '769 Patent, has and does possess the specific intent to encourage Vizio and end users to directly infringe the '769 Patent. TPV is therefore liable to HCE under at least 35 U.S.C. §§271(a) and (b).

63. Vizio has been directly infringing and continues to directly infringe, either literally or under the doctrine of equivalents, the '769 Patent by importing, offering to sell, and selling ATSC-compatible televisions, including both TPV and non-TPV supplied units, that embody or practice the claimed inventions. Further, end users in the United States directly infringe the '769 Patent by using their Vizio televisions. Vizio, with knowledge of the '769

Patent, has and does possess the specific intent to encourage end users to directly infringe the '769 Patent. Vizio is therefore liable to HCE under at least 35 U.S.C. §§ 271(a) and (b).

64. On information and belief, Defendants have continued to infringe the '769 Patent despite being on notice of the patent, and their infringement of the patent, since before the filing of the original complaint.

65. On information and belief, Defendants' acts of infringement as set out in the previous paragraphs have been and continue to be deliberate, willful, and in reckless disregard of HCE's patent rights.

66. HCE has been damaged by Defendants' infringing activities. On information and belief, Defendants will continue their infringing activities, and thus continue to damage HCE, unless enjoined by this Court. HCE has no adequate remedy at law.

COUNT VII – INFRINGEMENT OF U.S. PATENT NO. 7,286,310

67. Plaintiffs repeat and reallege the allegations of the preceding paragraphs as if set forth herein.

68. On October 23, 2007, U.S. Patent No. 7,286,310 ("the '310 Patent") entitled APPARATUS FOR RECEIVING COMPRESSED DIGITAL INFORMATION, was duly and legally issued by the United States Patent and Trademark Office. A true and correct copy of the '310 Patent is attached as Exhibit G to this Complaint.

69. HCE is the assignee and owner of the right, title, and interest in and to the '310 Patent, including the right to assert all causes of action arising under said patent, the right to recover damages for past, present, or future infringement of the patent, and the right to any other remedies for infringement of the patent.

70. TPV has been directly infringing and continues to directly infringe, either literally or under the doctrine of equivalents, the ’310 Patent by importing, offering to sell, and selling ATSC-compatible televisions that embody or practice the claimed inventions. In addition, Vizio, TPV’s customer, directly infringes the ’310 Patent by offering to sell and selling, among other things, TPV-supplied televisions in the United States. Further, end users in the United States directly infringe the ’310 Patent by using their TPV-manufactured televisions. TPV, with knowledge of the ’310 Patent, has and does possess the specific intent to encourage Vizio and end users to directly infringe the ’310 Patent. TPV is therefore liable to HCE under at least 35 U.S.C. §§ 271(a) and (b).

71. Vizio has been directly infringing and continues to directly infringe, either literally or under the doctrine of equivalents, the ’310 Patent by importing, offering to sell, and selling ATSC-compatible televisions, including both TPV and non-TPV supplied units, that embody or practice the claimed inventions. Further, end users in the United States directly infringe the ’310 Patent by using their Vizio televisions. Vizio, with knowledge of the ’310 Patent, has and does possess the specific intent to encourage end users to directly infringe the ’310 Patent. Vizio is therefore liable to HCE under at least 35 U.S.C. §§ 271(a) and (b).

72. On information and belief, Defendants have continued to infringe the ’310 Patent despite being on notice of the patent, and their infringement of the patent, since before the filing of the original complaint.

73. On information and belief, Defendants’ acts of infringement as set out in the previous paragraphs have been and continue to be deliberate, willful, and in reckless disregard of HCE’s patent rights.

74. HCE has been damaged by Defendants' infringing activities. On information and belief, Defendants will continue its infringing activities, and thus continue to damage HCE, unless enjoined by this Court. HCE has no adequate remedy at law.

COUNT VIII –INFRINGEMENT OF U.S. PATENT NO. 6,144,412

75. Plaintiffs repeat and reallege the allegations of the preceding paragraphs as if set forth within.

76. On November 7, 2000, United States Letters Patent No. 6,144,412 ("the '412 Patent"), entitled METHOD AND CIRCUIT FOR SIGNAL PROCESSING OF FORMAT CONVERSION OF PICTURE SIGNAL, was duly and legally issued by the United States Patent and Trademark Office. A true and correct copy of the '412 Patent is attached as Exhibit H to this Complaint.

77. HCE is the assignee and owner of the right, title, and interest in and to the '412 Patent, including the right to assert all causes of action arising under said patent, the right to recover damages for past, present, or future infringement of the patent, and the right to any other remedies for infringement of the patent.

78. TPV has been directly infringing and continues to directly infringe, either literally or under the doctrine of equivalents, the '412 Patent by importing, offering to sell, and selling ATSC-compatible televisions that embody or practice the claimed inventions. In addition, Vizio, TPV's customer, directly infringes the '412 Patent by offering to sell and selling, among other things, TPV-supplied televisions in the United States. Further, end users in the United States directly infringe the '412 Patent by using their TPV-manufactured televisions. TPV, with knowledge of the '412 Patent, has and does possess the specific intent to encourage Vizio and

end users to directly infringe the ’412 Patent. TPV is therefore liable to HCE under at least 35 U.S.C. §§ 271(a) and (b).

79. Vizio has been directly infringing and continues to directly infringe, either literally or under the doctrine of equivalents, the ’412 Patent by importing, offering to sell, and selling ATSC-compatible televisions, including both TPV and non-TPV supplied units, that embody or practice the claimed inventions. Further, end users in the United States directly infringe the ’412 Patent by using their Vizio televisions. Vizio, with knowledge of the ’412 Patent, has and does possess the specific intent to encourage end users to directly infringe the ’412 Patent. Vizio is therefore liable to HCE under at least 35 U.S.C. §§ 271(a) and (b).

80. On information and belief, Defendants have continued to infringe the ’412 Patent despite being on notice of the patent, and their infringement of the patent, since before the filing of the original complaint.

81. On information and belief, Defendants’ acts of infringement as set out in the previous paragraphs have been and continue to be deliberate, willful, and in reckless disregard of HCE’s patent rights.

82. HCE has been damaged by Defendants’ infringing activities. On information and belief, Defendants will continue their infringing activities, and thus continue to damage HCE, unless enjoined by this Court. HCE has no adequate remedy at law.

COUNT IX – INFRINGEMENT OF U.S. PATENT NO. 7,889,281 B2

83. Plaintiff repeats and realleges the allegations of the preceding paragraphs as if set forth herein.

84. On February 15, 2011, U.S. Patent No. 7,889,281 B2 ("the '281 Patent) entitled "DIGITAL BROADCAST RECEIVER UNIT," was duly and legally issued by the United States Patent and Trademark Office. A true and correct copy of the '281 Patent is attached as Exhibit I to this Complaint.

85. HCE is the assignee and owner of the right, title, and interest in and to the '281 Patent, including the right to assert all causes of action arising under said patent, the right to recover damages for past, present, or future infringement of the patent, and the right to any other remedies for infringement of the patent.

86. TPV has been directly infringing and continues to directly infringe, either literally or under the doctrine of equivalents, the '281 Patent by importing, offering to sell, and selling ATSC-compatible televisions that embody or practice the claimed inventions. In addition, Vizio, TPV's customer, directly infringes the '281 Patent by offering to sell and selling, among other things, TPV-supplied televisions in the United States. Further, end users in the United States directly infringe the '281 Patent by using their TPV-manufactured televisions. TPV, with knowledge of the '281 Patent, has and does possess the specific intent to encourage Vizio and end users to directly infringe the '281 Patent. TPV is therefore liable to HCE under at least 35 U.S.C. §§ 271(a) and (b).

87. Vizio has been directly infringing and continues to directly infringe, either literally or under the doctrine of equivalents, the '281 Patent by importing, offering to sell, and selling ATSC-compatible televisions, including both TPV and non-TPV supplied units, that embody or practice the claimed inventions. Further, end users in the United States directly infringe the '281 Patent by using their Vizio televisions. Vizio, with knowledge of the '281

Patent, has and does possess the specific intent to encourage end users to directly infringe the '281 Patent. Vizio is therefore liable to HCE under at least 35 U.S.C. §§ 271(a) and (b).

88. On information and belief, TPV and Vizio have been aware of the existence of the '281 Patent since before the filing of this First Amended Complaint. On information and belief, Defendants became aware of the '281 Patent through their due diligence in preparing their defenses to Plaintiffs' infringement counts in the original complaint. In the alternative, Defendants became aware of the '281 patent upon the filing of civil case no. 2:12-cv-00268-JRG in the United States District Court for the Eastern District of Texas, filed on May 3, 2012. Defendants' acts of infringement have been and continue to be deliberate and willful.

89. HCE has been damaged by Defendants' infringing activities. On information and belief, Defendants will continue their infringing activities, and thus continue to damage HCE, unless enjoined by this Court. HCE has no adequate remedy at law.

COUNT X – INFRINGEMENT OF U.S. PATENT NO. 8,009,375 B2

90. Plaintiff repeats and realleges the allegations of the preceding paragraphs as if set forth herein.

91. On August 30, 2011, U.S. Patent No. 8,009,375 B2 ("the '375 Patent") entitled "APPARATUS AND METHOD FOR RECEIVING AND RECORDING DIGITAL INFORMATION," was duly and legally issued by the United States Patent and Trademark Office. A true and correct copy of the '375 Patent is attached hereto as Exhibit J to this Complaint.

92. HCE is the assignee and owner of the right, title, and interest in and to the '375 Patent, including the right to assert all causes of action arising under said patent, the right to

recover damages for past, present, or future infringement of the patent, and the right to any other remedies for infringement of the patent.

93. TPV has been directly infringing and continues to directly infringe, either literally or under the doctrine of equivalents, the ’375 Patent by importing, offering to sell, and selling ATSC-compatible televisions that embody or practice the claimed inventions. In addition, Vizio, TPV’s customer, directly infringes the ‘375 Patent by offering to sell and selling, among other things, TPV-supplied televisions in the United States. Further, end users in the United States directly infringe the ‘375 Patent by using their TPV-manufactured televisions. TPV, with knowledge of the ‘375 Patent, has and does possess the specific intent to encourage Vizio and end users to directly infringe the ‘375 Patent. TPV is therefore liable to HCE under at least 35 U.S.C. §§ 271(a) and (b).

94. Vizio has been directly infringing and continues to directly infringe, either literally or under the doctrine of equivalents, the ’375 Patent by importing, offering to sell, and selling ATSC-compatible televisions, including both TPV and non-TPV supplied units, that embody or practice the claimed inventions. Further, end users in the United States directly infringe the ‘375 Patent by using their Vizio televisions. Vizio, with knowledge of the ‘375 Patent, has and does possess the specific intent to encourage end users to directly infringe the ‘375 Patent. Vizio is therefore liable to HCE under at least 35 U.S.C. §§ 271(a) and (b).

95. On information and belief, TPV and Vizio have been aware of the existence of the ’375 Patent since before the filing of this First Amended Complaint. On information and belief, Defendants became aware of the ‘375 Patent through their due diligence in preparing their defenses to Plaintiffs’ infringement counts in the original complaint. In the alternative,

Defendants became aware of the ’375 patent upon the filing of civil case no. 2:12-cv-00268-JRG in the United States District Court for the Eastern District of Texas, filed on May 3, 2012. Defendants’ acts of infringement have been and continue to be deliberate and willful.

96. HCE has been damaged by Defendants’ infringing activities. On information and belief, Defendants will continue its infringing activities, and thus continue to damage HCE, unless enjoined by this Court. HCE has no adequate remedy at law.

JURY DEMAND

97. Pursuant to Rule 38 of the Federal Rules of Civil Procedure, Plaintiffs demand a trial by jury on all issues triable as such.

PRAYER FOR RELIEF

WHEREFORE, Plaintiffs respectfully demand judgment for themselves and against Defendants TPV and Vizio as follows:

a. That this Court adjudge that Defendant Vizio has infringed each of the ’497, ’934, ’995, ’713, ’243, ’769, ’310, ’412, ’281 and ’375 Patents;

b. That this Court adjudge that Vizio’s infringement of the ’497, ’934, ’995, ’713, ’243, ’769, ’310, ’412, ’281 and ’375 Patents has been willful;

c. That this Court adjudge that Defendant TPV has infringed each of the ’497, ‘934, ’995, ’713, ’243, ’769, ’310, ’412, ’281 and ’375 Patents;

d. That this Court adjudge that TPV’s infringement of the ’497, ‘934, ’995, ’713, ’243, ’769, ’310, ’412, ’281 and ’375 Patents has been willful;

e. That this Court issue an injunction, enjoining Defendants Vizio and TPV and their officers, agents, servants and employees, privies, and all persons in active concert or participation with it, from further infringement of said patents;

f. That this Court ascertain and award Plaintiffs damages sufficient to compensate them for the above infringement, including but not limited to infringement occurring before the filing of this lawsuit, and that the damages so ascertained be trebled as appropriate and awarded to Plaintiffs with any applicable pre-judgment and post-judgment interest;

g. That this Court find this case to be exceptional and award Plaintiffs their attorneys fees, costs and expenses in this action; and

h. That this Court award Plaintiffs such other relief as the Court may deem just and proper.

DATED: June 5, 2012

Respectfully submitted,

/s/ Jeffrey B. Plies

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CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing document was filed electronically in compliance with Local Rule CV-5(a). As such, this notice was served on all counsel who have consented to electronic service, Local Rule CV-5(a)(3)(A), on June 5, 2012.

/s/ Jeffrey B. Plies

14448573

EXHIBIT A

US005502497A

United States Patent [19]

Yamaashi et al.

[11] Patent Number: 5,502,497

[45] Date of Patent: Mar. 26, 1996

[54] **TELEVISION BROADCASTING METHOD AND SYSTEM ENABLING PICTURE BROADCASTING FROM THE TRANSMITTING EQUIPMENT TO THE RECEIVING EQUIPMENT USING ALTERNATIVE BROADCASTING SYSTEM STANDARDS**

[75] Inventors: **Kimiya Yamaashi**, Hitachi; **Masayuki Tani**, Katsuta; **Koichiro Tanikoshi**, Hitachi; **Masayasu Futakawa**, Hitachi; **Shinya Tanifuji**, Hitachi; **Atsushi Kawabata**, Hitachi; **Norito Watanabe**, Hitachi; **Kazunari Maeda**, Tondabayashi, all of Japan

[73] Assignee: **Hitachi, Ltd.**, Tokyo, Japan

[21] Appl. No.: **470,449**

[22] Filed: **Jun. 6, 1995**

Related U.S. Application Data

[63] Continuation of Ser. No. 936,779, Aug. 28, 1992, abandoned.

[30] **Foreign Application Priority Data**

Aug. 28, 1991 [JP] Japan 3-217508

[51] **Int. Cl.**[6] **H04N 7/08**

[52] **U.S. Cl.** **348/473**; 348/476

[58] **Field of Search** 348/473, 474, 348/484, 476, 6, 7, 10; 358/142, 143, 147, 146, 86; H04N 7/08

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,390,901	6/1983	Keiser	358/147
4,807,031	2/1989	Broughton	348/473
4,994,913	2/1991	Maeshima	358/142
5,014,125	5/1991	Pocock et al. .	
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5,200,823	4/1993	Yoneda	358/146
5,212,551	5/1993	Conanan	348/484
5,229,850	7/1993	Toyoshima	358/86
5,231,494	7/1993	Wachob	358/146

FOREIGN PATENT DOCUMENTS

0444947	9/1991	European Pat. Off. .

Primary Examiner—James J. Groody
Assistant Examiner—Sherrie Hsia
Attorney, Agent, or Firm—Antonelli, Terry, Stout & Kraus

[57] **ABSTRACT**

A television broadcasting system intended to bestow a certain level of selectivity on compression systems and multiplexing systems for broadcast program pictures. A transmitting equipment transmits the broadcast program pictures, and transmits control information on transmission systems for the transmitted broadcast program pictures. A receiving equipment includes a reception module which receives a program channel having a plurality of sorts of video information multiplexed therein, selected by a viewer, and also the control information concerning the selected program channel. A reception controller commands a signal separator to produce the outputs of the video information interleaved in those positions of the program channel which are designated by the control information. Besides, the reception controller sends a decoder a decoding program contained in the control information. The decoder executes the sent decoding program so as to decode the output video information of the signal separator and to display the decoded video information on a display unit.

18 Claims, 13 Drawing Sheets

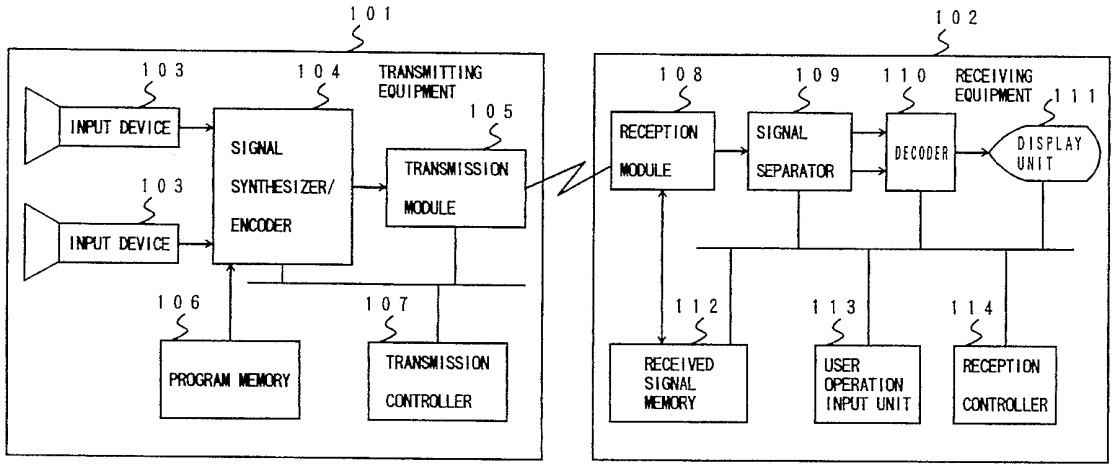


FIG. 1

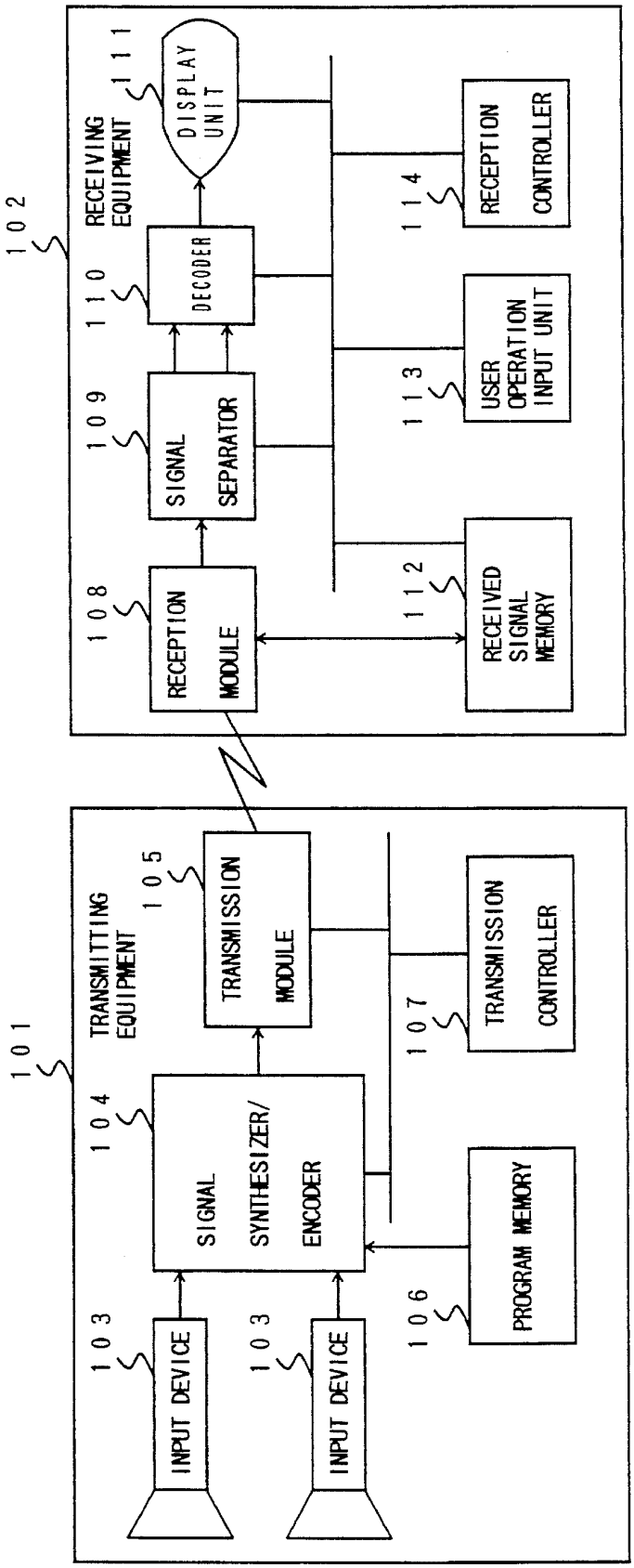

101
TRANSMITTING EQUIPMENT
102
RECEIVING EQUIPMENT
103
INPUT DEVICE
103
INPUT DEVICE
104
SIGNAL SYNTHESIZER/ ENCODER
105
TRANSMISSION MODULE
106
PROGRAM MEMORY
107
TRANSMISSION CONTROLLER
108
RECEPTION MODULE
109
SIGNAL SEPARATOR
110
DECODER
111
DISPLAY UNIT
112
RECEIVED SIGNAL MEMORY
113
USER OPERATION INPUT UNIT
114
RECEPTION CONTROLLER

FIG. 2

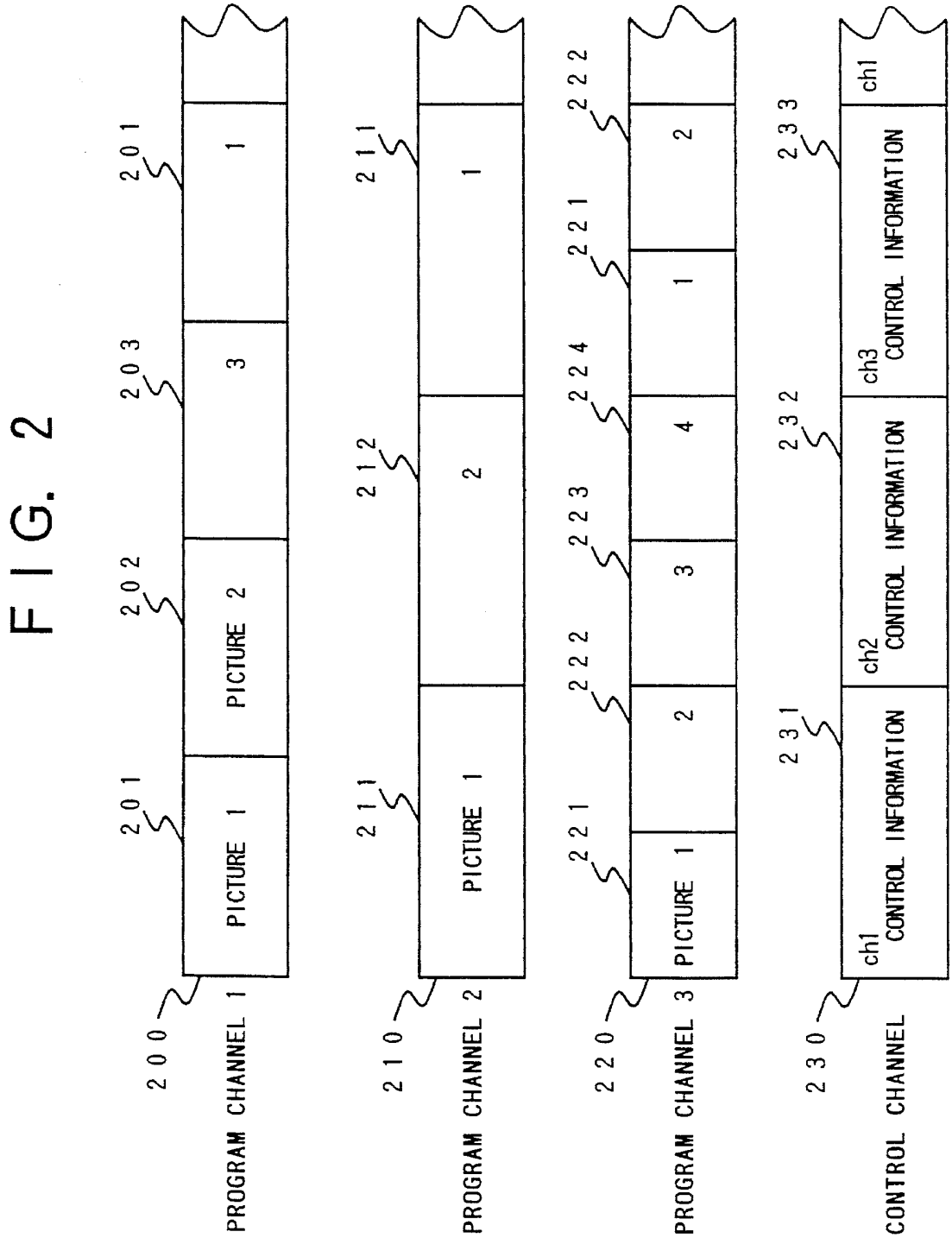

200
PROGRAM CHANNEL 1
201
PICTURE 1
202
PICTURE 2
203
3
201
1
210
PROGRAM CHANNEL 2
211
PICTURE 1
212
2
211
1
220
PROGRAM CHANNEL 3
221
PICTURE 1
222
2
223
3
224
4
221
1
222
2
230
CONTROL CHANNEL
231
ch1
CONTROL INFORMATION
232
ch2
CONTROL INFORMATION
233
ch3
CONTROL INFORMATION
ch1

FIG. 3

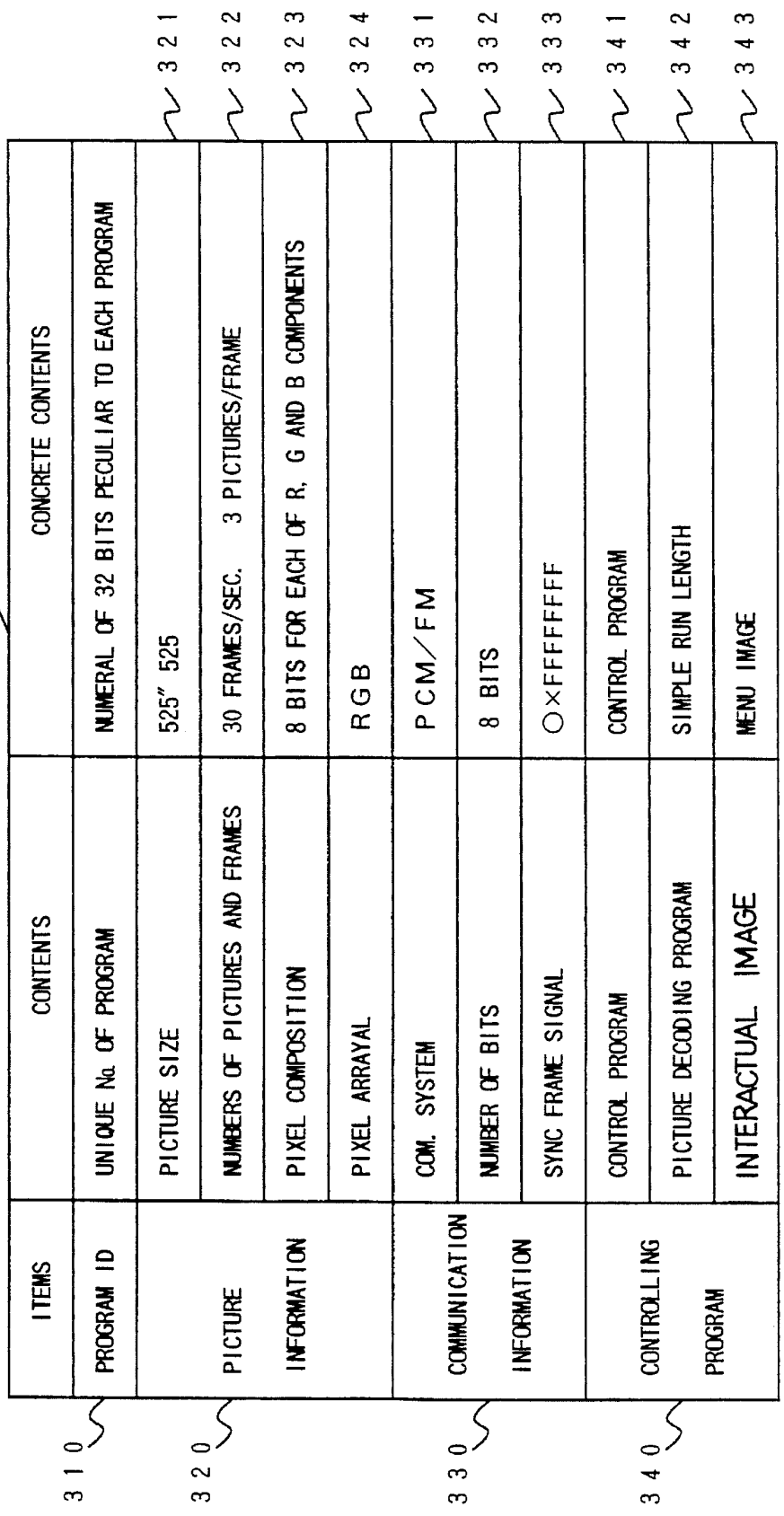

300
ITEMS
CONTENTS
CONCRETE CONTENTS
310
PROGRAM ID
UNIQUE No. OF PROGRAM
NUMERAL OF 32 BITS PECULIAR TO EACH PROGRAM
320
PICTURE INFORMATION
PICTURE SIZE
525" 525
321
NUMBERS OF PICTURES AND FRAMES
30 FRAMES/SEC. 3 PICTURES/FRAME
322
PIXEL COMPOSITION
8 BITS FOR EACH OF R, G AND B COMPONENTS
323
PIXEL ARRAYAL
RGB
324
330
COMMUNICATION INFORMATION
COM. SYSTEM
PCM/FM
331
NUMBER OF BITS
8 BITS
332
SYNC FRAME SIGNAL
○×FFFFFFFF
333
340
CONTROLLING PROGRAM
CONTROL PROGRAM
CONTROL PROGRAM
341
PICTURE DECODING PROGRAM
SIMPLE RUN LENGTH
342
INTERACTUAL IMAGE
MENU IMAGE
343

FIG. 4

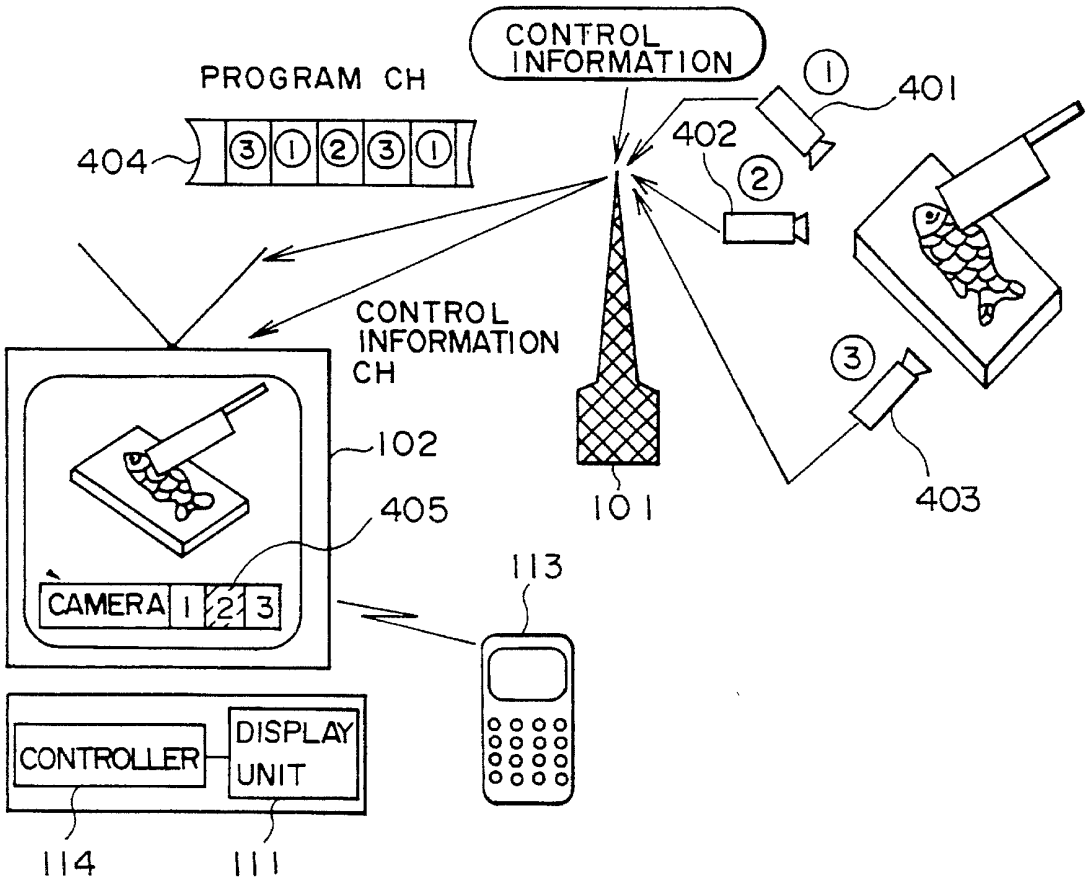

CONTROL INFORMATION
PROGRAM CH
404
3 1 2 3 1
401
402
CONTROL INFORMATION CH
102
405
CAMERA 1 2 3
101
403
113
CONTROLLER
DISPLAY UNIT
114
111

FIG. 5

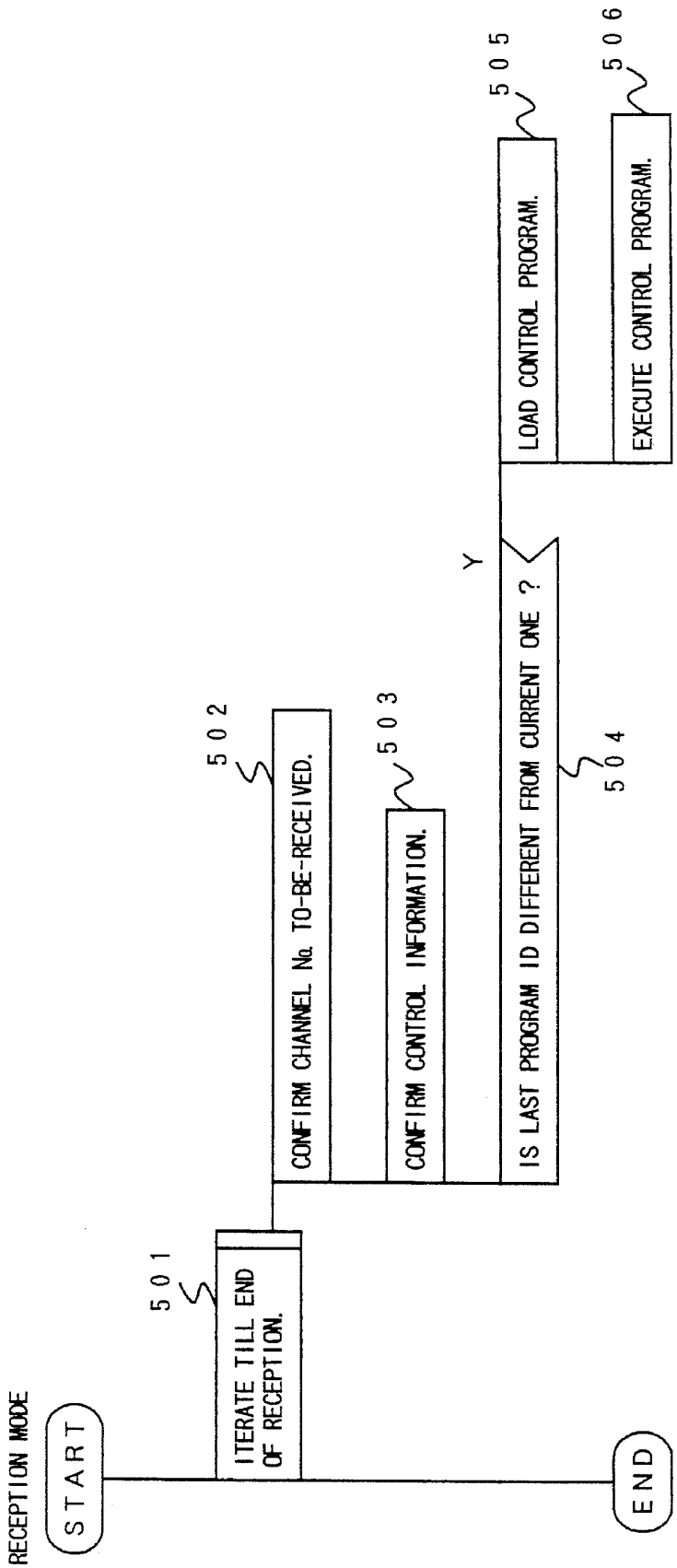

RECEPTION MODE
START
501
ITERATE TILL END OF RECEPTION.
502
CONFIRM CHANNEL No. TO-BE-RECEIVED.
503
CONFIRM CONTROL INFORMATION.
504
IS LAST PROGRAM ID DIFFERENT FROM CURRENT ONE ?
Y
505
LOAD CONTROL PROGRAM.
506
EXECUTE CONTROL PROGRAM.
END

FIG. 6

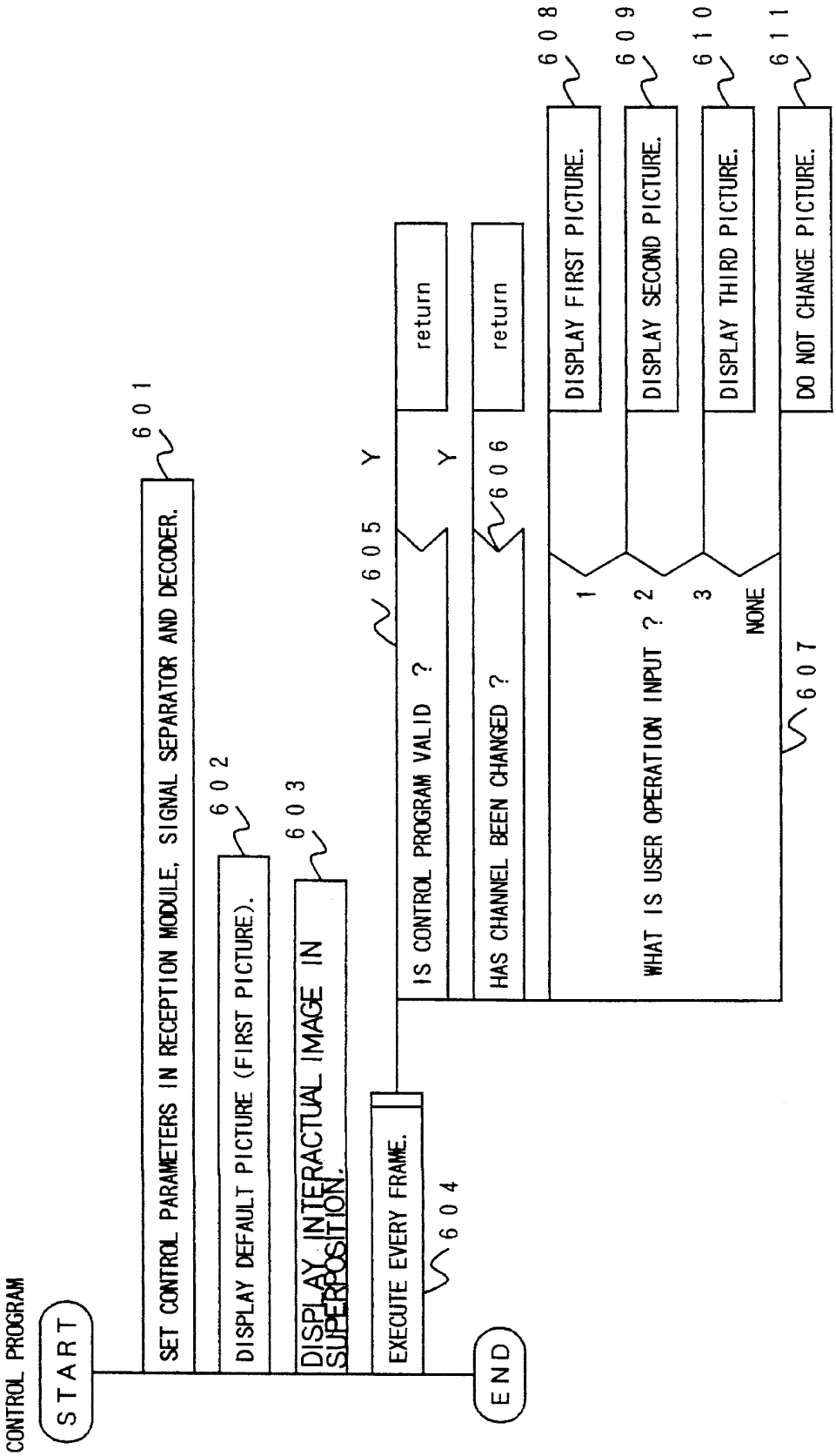

CONTROL PROGRAM
START
SET CONTROL PARAMETERS IN RECEPTION MODULE, SIGNAL SEPARATOR AND DECODER.
601
DISPLAY DEFAULT PICTURE (FIRST PICTURE).
602
DISPLAY INTERACTUAL IMAGE IN SUPERPOSITION.
603
EXECUTE EVERY FRAME.
604
IS CONTROL PROGRAM VALID ?
605
Y
return
HAS CHANNEL BEEN CHANGED ?
606
Y
return
WHAT IS USER OPERATION INPUT ?
607
1
DISPLAY FIRST PICTURE.
608
2
DISPLAY SECOND PICTURE.
609
3
DISPLAY THIRD PICTURE.
610
NONE
DO NOT CHANGE PICTURE.
611
END

FIG. 7

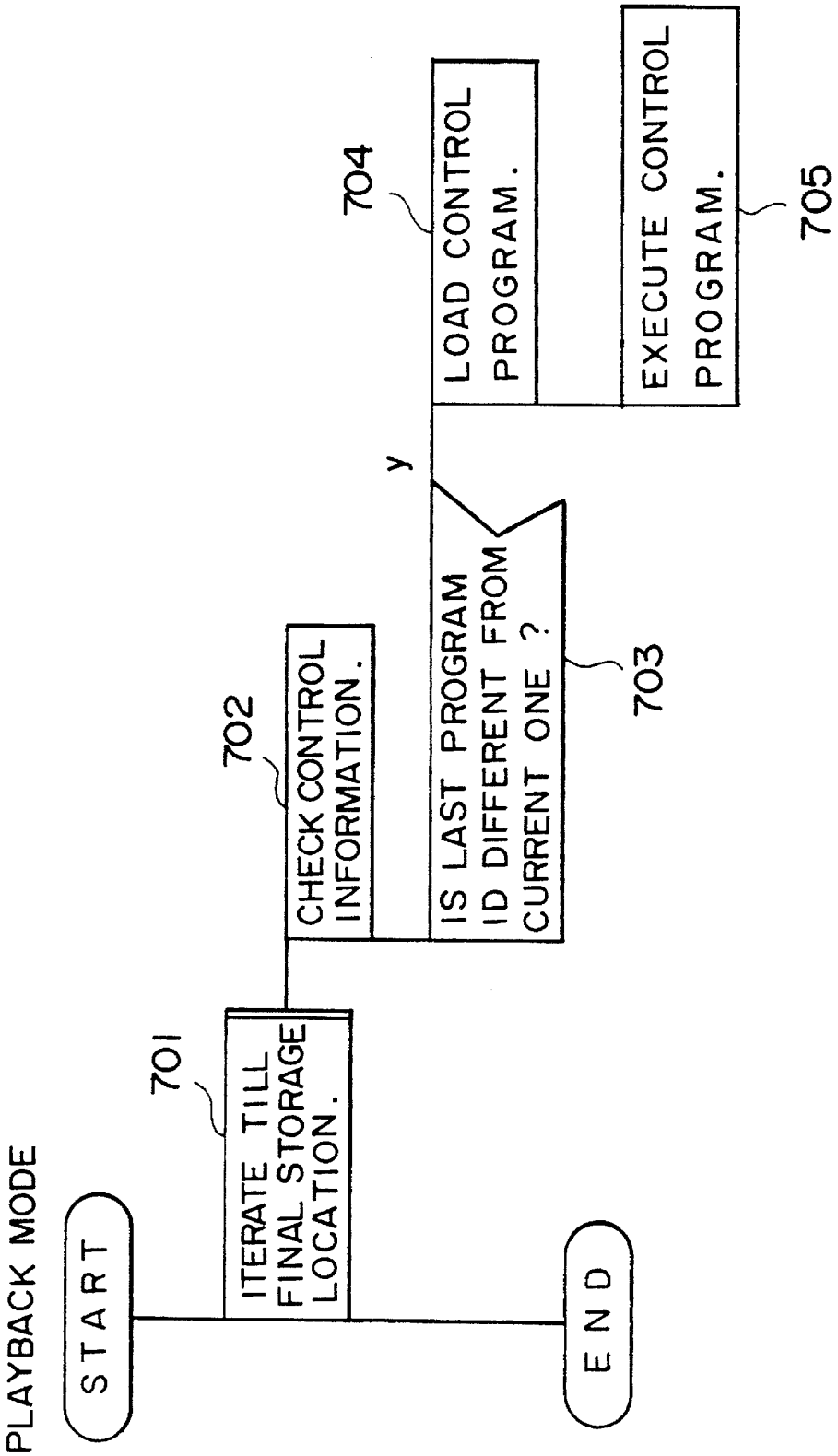

PLAYBACK MODE
START
701
ITERATE TILL FINAL STORAGE LOCATION.
702
CHECK CONTROL INFORMATION.
703
IS LAST PROGRAM ID DIFFERENT FROM CURRENT ONE ?
y
704
LOAD CONTROL PROGRAM.
705
EXECUTE CONTROL PROGRAM.
END

FIG. 8

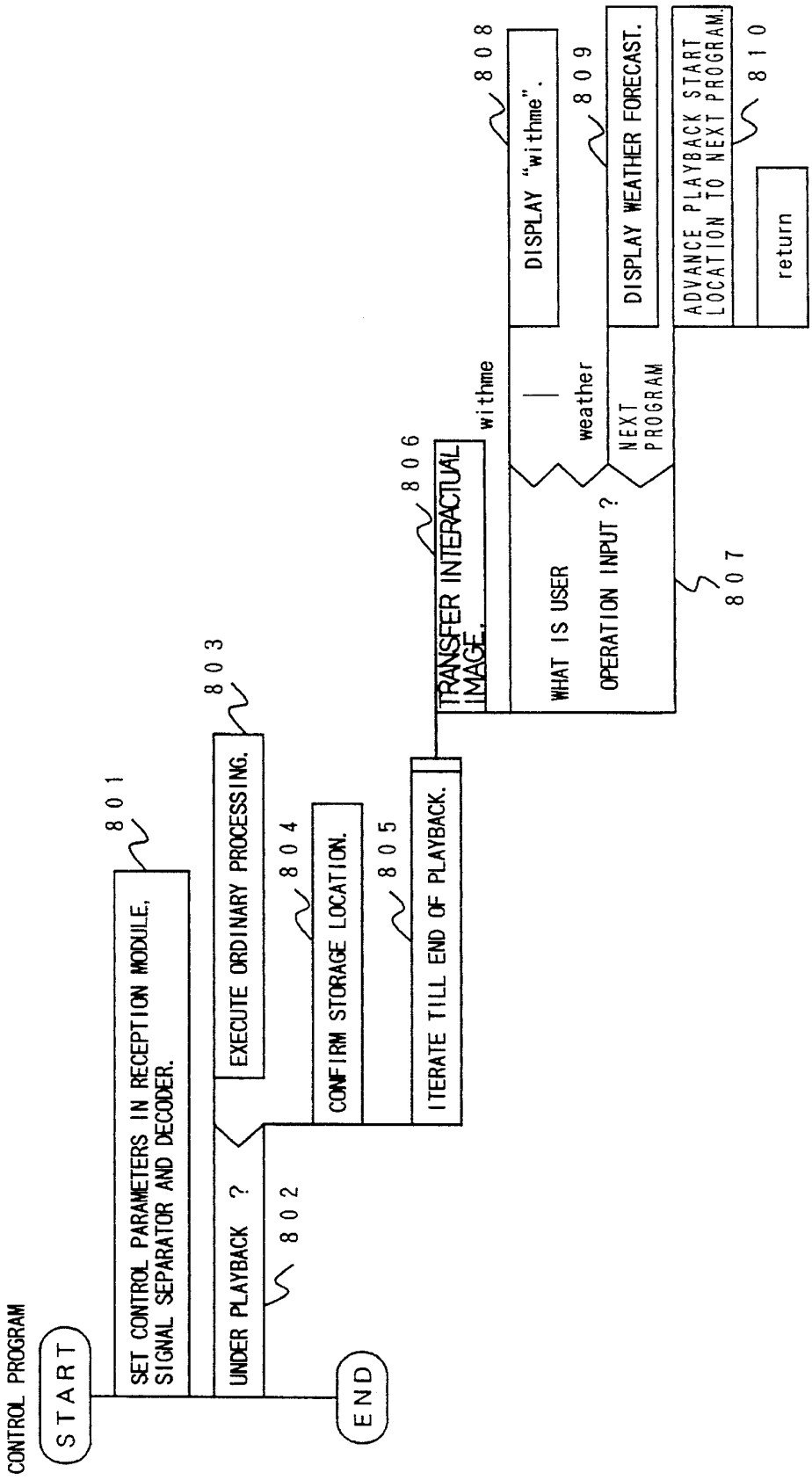

CONTROL PROGRAM
START
801
SET CONTROL PARAMETERS IN RECEPTION MODULE, SIGNAL SEPARATOR AND DECODER.
802
UNDER PLAYBACK ?
803
EXECUTE ORDINARY PROCESSING.
804
CONFIRM STORAGE LOCATION.
805
ITERATE TILL END OF PLAYBACK.
806
TRANSFER INTERACTIVE IMAGE.
807
WHAT IS USER OPERATION INPUT ?
withme
weather
NEXT PROGRAM
808
DISPLAY "withme".
809
DISPLAY WEATHER FORECAST.
810
ADVANCE PLAYBACK START LOCATION TO NEXT PROGRAM.
return
END

FIG. 9

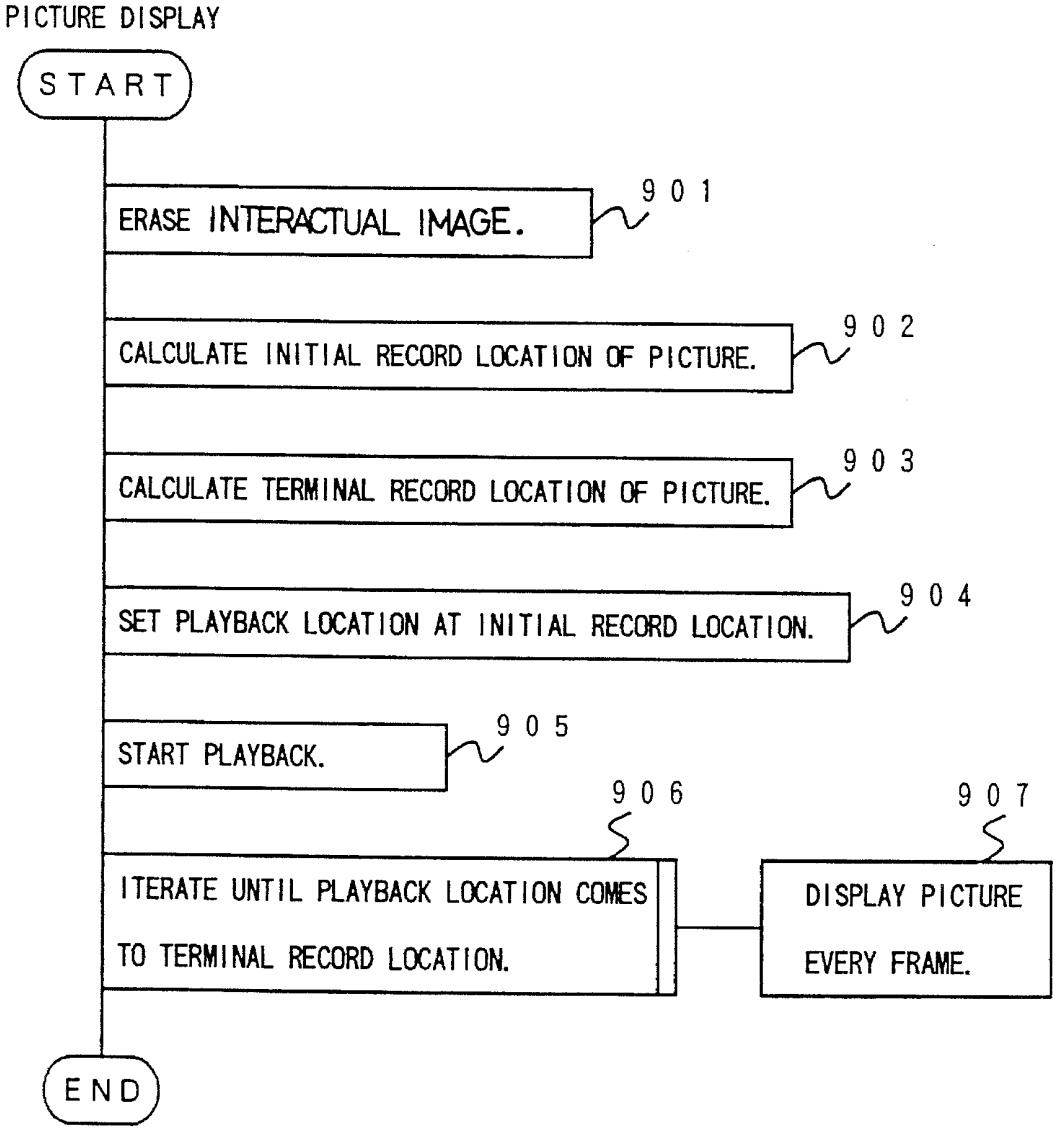

PICTURE DISPLAY
START
ERASE INTERACTUAL IMAGE.
901
CALCULATE INITIAL RECORD LOCATION OF PICTURE.
902
CALCULATE TERMINAL RECORD LOCATION OF PICTURE.
903
SET PLAYBACK LOCATION AT INITIAL RECORD LOCATION.
904
START PLAYBACK.
905
906
ITERATE UNTIL PLAYBACK LOCATION COMES TO TERMINAL RECORD LOCATION.
907
DISPLAY PICTURE EVERY FRAME.
END

FIG. 10

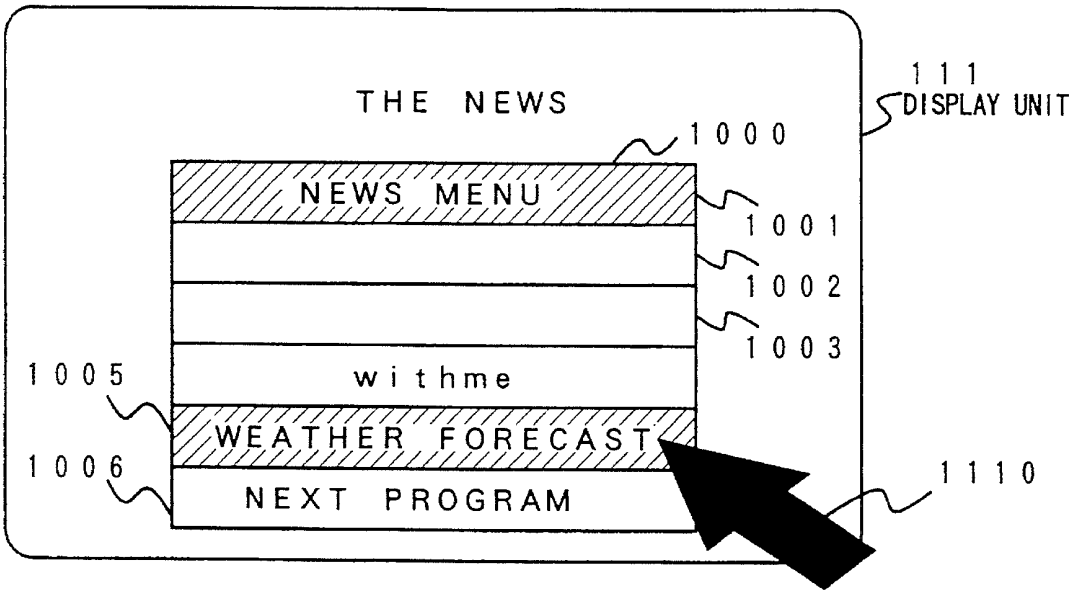

THE NEWS
1000
NEWS MENU
1001
1002
1003
1005
withme
WEATHER FORECAST
1006
NEXT PROGRAM
111
DISPLAY UNIT
1110

FIG. 11

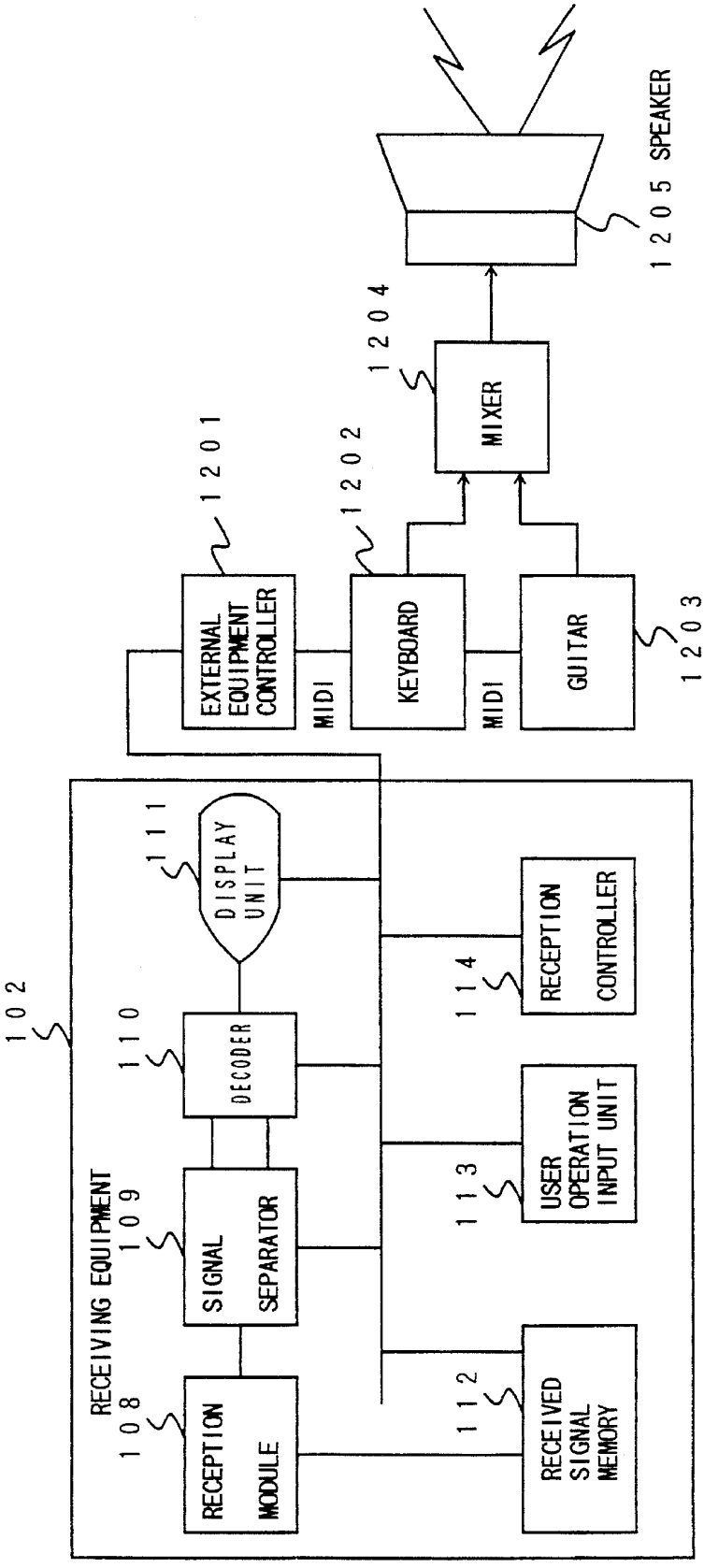

1205 SPEAKER
1204
MIXER
1201
1202
EXTERNAL EQUIPMENT CONTROLLER
MIDI
KEYBOARD
MIDI
GUITAR
1203
102
RECEIVING EQUIPMENT
111
DISPLAY UNIT
110
DECODER
109
SIGNAL SEPARATOR
108
RECEPTION MODULE
114
RECEPTION CONTROLLER
113
USER OPERATION INPUT UNIT
112
RECEIVED SIGNAL MEMORY

FIG. 12A

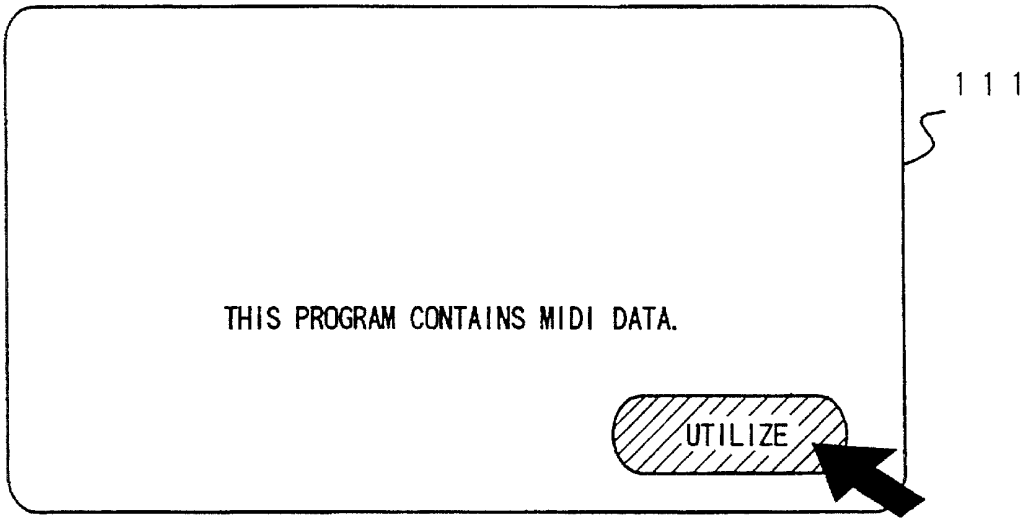


FIG. 12B

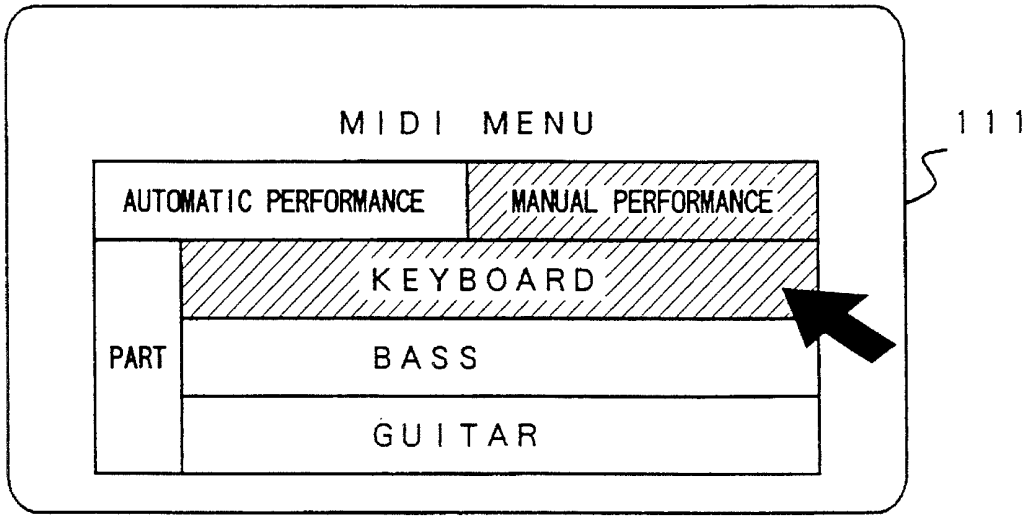
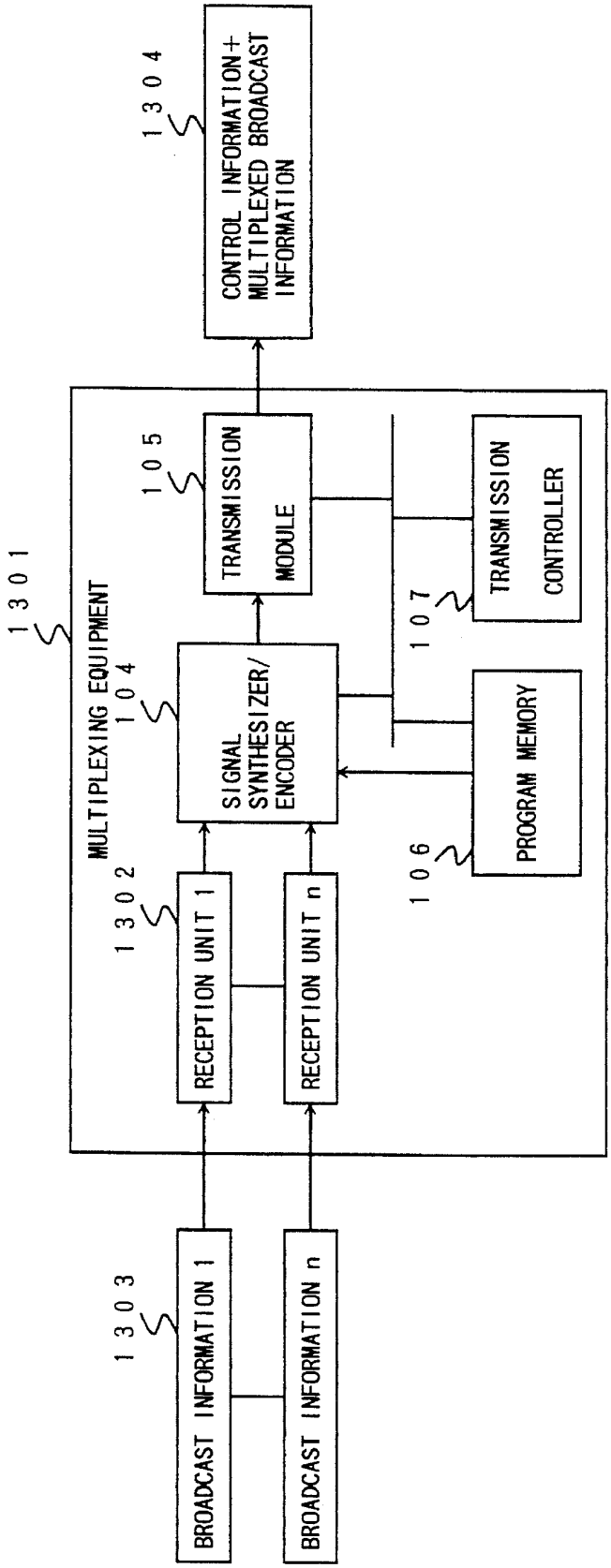


FIG. 13


1304
CONTROL INFORMATION+ MULTIPLEXED BROADCAST INFORMATION
1301
MULTIPLEXING EQUIPMENT
105
TRANSMISSION MODULE
107
TRANSMISSION CONTROLLER
104
SIGNAL SYNTHESIZER/ ENCODER
106
PROGRAM MEMORY
1302
RECEPTION UNIT 1
RECEPTION UNIT n
1303
BROADCAST INFORMATION 1
BROADCAST INFORMATION n

TELEVISION BROADCASTING METHOD AND SYSTEM ENABLING PICTURE BROADCASTING FROM THE TRANSMITTING EQUIPMENT TO THE RECEIVING EQUIPMENT USING ALTERNATIVE BROADCASTING SYSTEM STANDARDS

This application is a continuation application of Ser. No. 07/936,779, filed Aug. 28, 1992, now abandoned.

BACKGROUND OF THE INVENTION

The present invention relates to broadcasting communication systems for television broadcasting, radio broadcasting, etc. More particularly, it relates to a broadcasting system which features an arrangement wherein control information items for viewing broadcast contents are also transmitted and received.

Various broadcasting systems are adopted for present-day television broadcasting.

By way of example, the NTSC system is a broadcast system standard generally employed in Japan. In addition to the NTSC system, the PAL system and the SECAM system are employed in many other countries.

Besides, the ISDB (Integrated Services Digital Broadcasting) system has been studied wherein video signals are digitized and then turned into compressed codes, which are subjected to time-division multiplexed transmission.

In general, one receiving set can receive a plurality of broadcasts allotted to different channels as long as the broadcasts are in an identical broadcasting form. Thus, a viewer selects one of the plurality of channels which his/her receiving set can receive, in accordance with desired information, and he/she views the picture of the selected channel.

SUMMARY OF THE INVENTION

The present invention has for its object an attention to provide a television broadcasting system in which compression systems, multiplexing systems, the selections of pictures by viewers, etc. are rendered flexible in order to offer multifarious services to the viewers.

The present invention consists of a television broadcasting system having a transmitting equipment which transmits a broadcast program picture, and a receiving equipment which receives and displays the transmitted broadcast program picture; characterized in that the transmitting equipment transmits control information for specifying a transmission system for the transmitted broadcast program picture, and that said receiving equipment receives the control information on the basis of a predetermined standard and then receives and displays said broadcast program picture transmitted from the transmitting equipment, on the basis of the received control information.

Accordingly, the transmission systems such as encoding systems and multiplexing systems can be flexibly selected depending upon various conditions such as the characteristics of the broadcast program pictures to-be-transmitted, and multifarious services can be offered to the viewers.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram showing the architecture of a television broadcasting system according to an embodiment of the present invention;

FIG. **2** is an explanatory diagram showing the situation of broadcasting channels for use in the embodiment;

FIG. **3** is an explanatory diagram showing control information for use in the embodiment;

FIG. **4** is an explanatory diagram showing the first operating example of the television broadcasting system of the embodiment;

FIG. **5** is a flow chart showing the reception operation of a reception controller in the first operating example;

FIG. **6** is a flow chart showing a control program which is run by the reception controller in the first operating example;

FIG. **7** is a flow chart showing the playback operation of a reception controller in the second operating example;

FIG. **8** is a flow chart showing a control program which is run by the reception controller in the second operating example;

FIG. **9** is a flow chart showing the picture display operation of the reception controller in the second operating example;

FIG. **10** is an explanatory diagram showing a menu which is displayed on a display unit in the second operating example;

FIG. **11** is a block diagram showing the construction of a receiving side system in the third operating example;

FIGS. **12**A and **12**B are diagrams for explaining a menu which is displayed on a display unit in the third operating example; and

FIG. **13** is a block diagram showing the construction of a transmitting side system in the fourth embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Now, an embodiment of the present invention will be described.

First, the architecture of a television broadcasting system according to this embodiment is illustrated in FIG. **1**.

As shown in the figure, the television broadcasting system in this embodiment is configured of a transmitting equipment **101** and a receiving equipment **102**.

The transmitting equipment **101** transmits broadcast information, while the receiving equipment **102** accepts broadcast information and displays a broadcast content. The broadcasting of the broadcast information from the transmitting equipment **101** may be either wireless broadcasting or wire broadcasting. In other words, it is not restricted to conventional television broadcasting by wireless, but it may well be broadcasting based on so-called cable television or the like.

The transmitting equipment **101** includes a plurality of input devices **103**, a signal synthesizer/encoder **104**, a transmission module **105**, a program memory **106** and a transmission controller **107**.

The receiving equipment **102** includes a reception module **108**, a signal separator **109**, a decoder **110**, a display unit **111**, a received signal memory **112**, a user operation input unit **113** and a reception controller **114**.

The constituents of the transmitting equipment **101** function as stated below.

Each of the input devices **103** accepts into the transmitting equipment **101**, broadcast content information to-be-broadcast such as text, a still picture, motion pictures or voice.

Control information items for respective broadcasting channels are kept stored in the program memory **106**. As will be described later, the control information serves to control the broadcast content of the corresponding broadcasting channel.

The signal encoder/synthesizer **104** encodes the respective broadcast content information items accepted by the plurality of input devices **103**. In addition, it accepts the corresponding control information items stored in the program memory **106** and encodes them. On this occasion, it affixes parity error correction codes to the control programs of the control information items in order to facilitate error corrections on the receiving side.

Subsequently, the signal encoder/synthesizer **104** subjects the encoded broadcast content information items to time-division multiplexing operations for every broadcasting channel and sends the resulting multiplexed signals to the transmission module **105**. In addition, it subjects the encoded control information items to time-division multiplexing together with the control information of other broadcasting channels and sends the resulting multiplexed signals to the transmission module **105**.

The transmission module **105** modulates the broadcast content information items subjected to the time-division multiplexing for every broadcasting channel by the signal encoder/synthesizer **104**, at a frequency specified for every broadcasting channel, and it transmits the resulting modulated signals. In addition, it modulates the control information items subjected to the time-division multiplexing, at a specified frequency, and it transmits the resulting modulated signals.

Further, the transmission controller **107** controls the operations of the other constituents included in the transmitting equipment **101**.

Here, the relationships between the motion picture information and the control information which are transmitted from the transmitting equipment **101** are as illustrated in FIG. **2**. The example shown in FIG. **2** corresponds to a case where the content broadcast information items are motion pictures.

Referring to the figure, numerals **200**, **210** and **220** indicate the broadcasting channels each of which contains the broadcast content information items subjected to the time-division multiplexing. As seen from the figure, the broadcasting channel **200** (program channel #1) contains three motion pictures **201**, **202** and **203** subjected to the time-division multiplexing; the broadcasting channel **210** (program channel #2) contains two motion pictures **211** and **212**; and the broadcasting channel **220** (program channel #3) contains four motion pictures **221**, **222**, **223** and **224**.

The other broadcasting channel **230** (a control channel) contains control information items **231**, **232** and **233** which control the broadcast contents concerning the broadcasting channels **200**, **210** and **220**, respectively, and which have been subjected to the time-division multiplexing.

In the broadcasting channel **230**, the control information items **231**, **232** and **233** have been respectively subjected to the time-division multiplexing in a predetermined sequence, and they bear synchronizing flags for specifying the positions of the individual control information signals. Incidentally, the control information is repeatedly broadcast at certain regular intervals as long as it is valid. This is based on the fact that the reception of the program channel is sometimes started midway through a broadcast program.

Hereinbelow, the broadcasting channel which contains the control information items subjected to the time-division multiplexing shall be called the "control channel", while the broadcasting channel which contains the broadcast content information items subjected to the time-division multiplexing shall be called the "program channel".

Next, the functions of the constituents of the receiving equipment **102** will be stated.

The user operation input unit **113** accepts the viewer's instructions for the receiving equipment **102**. It is now assumed that any program channel desired to be viewed is selected as the viewer's instruction. Here, the viewer is only allowed to select any of the broadcasting channels except the control channel, that is, any of the program channels.

The reception module **108** receives and demodulates the control channel transmitted from the transmitting equipment **101**.

The signal separator **109** separates or demultiplexes the time-division-multiplexed control information items contained in the control channel demodulated by the reception module **108**, samples the control information concerning the selected program channel on the basis of the synchronizing flags, and decodes the sampled control information. In the signal separator **109**, the parity codes affixed in relation to the control signals are checked, and any errors are corrected.

The reception controller **114** sets the reception module **108**, signal separator **109** and decoder **110** in accordance with the decoded control information.

The reception module **108** receives and demodulates the selected program channel in accordance with set contents afforded from the reception controller **114**.

The signal separator **109** separates or demultiplexes the broadcast content information items contained in the demodulated program channel, and delivers any of the separated or demultiplexed broadcast content information items to the decoder **110** in accordance with the set contents afforded from the reception controller **114**.

The decoder **110** decodes the video signals of the broadcast content information in accordance with the set contents afforded from the reception controller **114**. In this embodiment, the decoder **110** is constructed of a DSP (Digital Signal Processor). This decoder **110** runs the set decoding program afforded from the reception controller **114**.

The display unit **111** accepts the decoded signals of the broadcast content information from the decoder **110**, and displays them.

Next, the contents of the-control information used in this embodiment will be explained. The control information is generated for each of the broadcast programs which are televised by the program channel.

FIG. **3** lists the contents of the control information. The illustrated example is the control information concerning the program channel in which all the broadcast content information items subjected to the time-division multiplexing are motion picture data.

As shown in the figure, the control information **300** is formed of a program ID **310**, picture or video information **320**, communication information **330** and a controlling program **340**.

The program ID **310** is a peculiar identification No. which is affixed to every control information for each broadcast program to-be-televised.

The picture or video information **320** serves to notify the reception controller **114** of the picture which is transmitted by the program channel corresponding to the control information **300**.

The video information **320** consists of a picture size **321**, the numbers of picture and frames **322**, a pixel composition **323** and a pixel arrayal **324**.

The picture size **321** denotes the numbers of pixels in the height and width of the picture. The numbers of pictures and frames **322** indicate the frame rate of the picture per second, and the number of pictures multiplexed in the corresponding program channel.

The pixel composition **323** indicates the number of bits which express each of the R, G and B components of one pixel. In the example shown in FIG. **3**, the number of bits is set to 8 (256 gradations).

The pixel arrayal **324** indicates how the information items of the respective color components are stored in the motion picture data. In the example shown in FIG. **3**, the respective color components are stored in single-image units in the order of the image of the component R, that of the component G and that of the component B.

The communication information **330** consists of a communication system **331**, the number of bits **332** and a synchronizing frame signal **333**.

The communication system **331** serves to notify the reception controller **114** of the communication system of the program channel corresponding to the control information **300**. In the illustrated example, this item **331** indicates that the corresponding program channel adopts pulse-code frequency modulation (PCM/FM) as its communication system.

Besides, the number of bits **332** indicates the bit length of the data. In the illustrated example, it is set to 8. The synchronizing frame signal **333** indicates a data value which is used for a synchronizing frame serving as the reference of the positions of the motion picture data signals in the program channel. In the illustrated example, the data value of the synchronizing frame is set at OXFFFFFFFF.

The controlling program **340** is a program which is loaded in the reception controller **114**, and which serves to decode the motion picture of the selected program channel and to offer several services.

This controlling program **340** consists of a control program **341**, a decoding program **342** and interactual image data **343**.

The control program **341** offers several services in relation to the program channel to which the control information **300** corresponds.

The picture decoding program **342** serves to decode the video or picture information which has been encoded and transmitted. In the illustrated example, a run-length decoding program is stored.

The dialog or menu image data **343** is the data of an image which the control program **341** uses in order to offer the services to the viewer.

In this manner, the transmitting equipment **101** enters into the control information **300** the information items which are necessary for reproducing the transmitted broadcast content information and the programs which serve to present the broadcast content information.

The first operating example of the television broadcasting system according to this embodiment will be explained below.

Now, let's consider a program in which a kitchen cookery situation simultaneously photographed by a plurality of cameras is televised.

FIG. **4** illustrates the circumstances of such a program broadcast.

First, operations on the side of the transmitting equipment **101** will be explained.

Referring to FIG. **4**, input devices #1, #2 and #3 (**401**, **402** and **403**) installed in the transmitting equipment **101** pick up respectively the image of hands, that of a knife blade and that of the whole situation. A picture taken by the input device #1 shall be called the "picture #1", a picture taken by the input device #2 the "picture #2", and a picture taken by the input device #3 the "picture #3".

In the transmitting equipment **101**, the signal synthesizer/encoder **104** operates so that the photographed pictures are digitally sampled, that the sampled data items are turned into compressed codes every frame by the run length method, and that the picture or video data items after the data compression are arrayed in frame unit successively in the order of the picture #1, the picture #2 and the picture #3 and are subjected to time-division multiplexing. Subsequently, the transmission module **105** modulates the multiplexed signals at a frequency allotted to a program channel **404** and transmits the modulated signals over the program channel **404**. Incidentally, alternative principal systems for encoding pictures include systems based on the DCT (Discrete Cosine Transform). In this embodiment, the sampled picture data may well be turned into compressed codes by the DCT system. In the case of employing the DCT system for the data compression, the picture decoding program of the control information becomes a program which executes the inverse DCT.

In addition, the control information for controlling the pictures #1, #2 and #3 of the program channel **404** in the receiving equipment **102** is fetched from the program memory **106** into the signal synthesizer/encoder **104** and is subjected to time-division multiplexing with control information items concerning program channels other than the program channel **404**. Subsequently, the transmission module **105** modulates the multiplexed control information items and transmits the modulated signals over a control channel.

Here, the control information concerning the program channel **404** contains as the control program **341** a program which allows the viewer to select a picture to-be-displayed from among the pictures taken by the three cameras.

Next, operations on the side of the receiving equipment **102** which receives the program channel **404** will be explained along flow charts illustrated in FIGS. **5** and **6**.

Upon the start of reception, the reception controller **114** first confirms a program channel to-be-received (step **502**). It loads the program ID (**310** in FIG. **3**) in the control information (**300**) concerning the program channel **404** as decoded by the signal separator or demultiplexor **109** (step **503**), and it compares the current program ID with the program ID of the control information loaded the previous time (step **504**). On condition that the program ID's are different, the current control information is loaded in the reception controller **114** as new control information (step **505**). After having loaded the control information, the reception controller **114** executes the control program (**341**) contained in the control information (step **506**). A step **501** signifies that the above processing is iterated until the end of the reception.

The flow chart of the control program (**341** in FIG. **3**) is illustrated in FIG. **6**.

As shown in the figure, the control program proceeds as stated below.

First, the reception controller **114** sets the reception module **108**, signal separator **109** and decoder **110** in accordance with the received control information **300** (step **601**). Specifically, the communication information **330** contained in the control information **300** is sent to the reception module

108. The reception module 108 demodulates the data items of the program channel 404 in succession on the basis of the sent communication information 330. Then, it sends the demodulated data to the signal separator or demultiplexor 109. Further, the reception controller 114 sends the picture or video information 320 to the signal separator 109. The signal separator 109 separates or demultiplexes the demodulated data of the program channel 404 into the data of the picture #1, that of the picture #2 and that of the picture #3 on the basis of the sent picture information 320 and delivers any of the separated picture data items to the decoder 110 in accordance with the command of the reception controller 114. It is now assumed that, at the start of the reception, the data of the picture 441 is delivered to the decoder 110 as a default picture (step 602). Hereinbelow, the picture based on the data of the picture 441 shall be called the "image #1", the picture based on the data of the picture #2 the "image #2", and the picture based on the data of the picture #3 the "image #3". Still further, the reception controller 114 sends the picture decoding program 342 to the decoder 110. The decoder 110 executes the sent program 342, thereby decoding the picture or video data accepted from the signal separator 109 and displaying the decoded data on the display unit 111.

At the next step, those image data items of the interactual image data 343 which are designated in the control program 341 are displayed in superposition on the image displayed on the display unit 111 (step 603). As a result, a user selection menu as shown at numeral 405 in FIG. 4 is displayed at the lower stage of the screen of the display unit 111. The user selection menu 405 allows the user or viewer to select the picture which is to be displayed on the display unit 111.

Subsequently, the ensuing processing is iterated for every picture frame (step 604).

In a case where the viewer has given an instruction in conformity with the user selection menu 405 (step 607), the reception controller 114 commands the signal separator or demultiplexor 109 to change-over the output thereof to the instructed picture data. Then, the output picture data is decoded by the decoder 110 and is displayed on the display unit 111. That is, the viewer can select and view any desired picture from among the image of the hands, that of the knife blade and that of the whole cooking scene of the broadcast program (steps 608~611).

In addition, the reception controller 114 checks for every picture frame, if the program ID of the control information to be received has changed and if the program channel has been changed by the user (steps 605, 606). On condition that the program ID of the control information to be received has changed or that the program channel has been changed, the control program is ended and is returned to the first processing step of accepting the control information.

As thus far described, according to this embodiment, the multiplexing degree of the broadcast content information items in each program channel, the encoding rules of the broadcast content information items, etc. can be designated for the receiving equipment by the control information, so that the transmitting side can broadcast in aspects which conform to services to-be-offered. In particular, many sorts of encoding rules can be utilized in such a way that the program for decoding the encoded broadcast content information is transmitted to the receiving equipment by the control information.

Further, the program which controls the displays of the broadcast content information items in each program channel in compliance with the request of the viewer or user can be sent to the receiving side by the control information, so that the viewer can flexibly utilize the broadcast content information as he/she requests.

That is, according to the broadcasting system of this embodiment, the broadcasting can be realized in the presence of only a standard concerning the control information and without the necessity of a unique standard for the program channels.

Incidentally, in the foregoing, the control information concerning the selected program channel in the receiving equipment 102 has been described as being valid for the broadcast content information which is received from commencement of the reception of the control information until the subsequent reception of the different control information. However, video broadcast content information to be controlled by control information may well be specified so as to validate the control information for only the specified broadcast content information. This control aspect can be realized in the following way: The transmitting equipment 101 transmits the control information in which information on the broadcast content information to be controlled by the pertinent control information has been entered beforehand. On the other hand, the receiving equipment 102 temporarily stores the received control information. It validates the stored control information when the broadcast content information to be controlled by the pertinent control information has been received, whereas it invalidates the validated control information when the reception of the broadcast content information to be controlled by the pertinent control information has ended.

Besides, in the foregoing, the broadcasting frequencies of the program channels have been described as being fixed, but they may well be made variable. In this case, the broadcasting equipment 101 transmits control information in which information for designating the broadcasting frequency of the corresponding program channel has been entered beforehand. The reception controller 114 of the receiving equipment 102 commands the reception module 108 to receive the broadcasting frequency, on the basis of the broadcasting frequency information contained in the control information corresponding to the selected program channel.

In addition, although the control channel and the program channels have been described above as being separately provided, control information items may well be transmitted in the state in which they are multiplexed with broadcast content information items in any predetermined program channel. In this case, however, positions for multiplexing the control information items and the broadcasting frequency of the program channel bearing the multiplexed control information items are fixed. The reason therefor is that the receiving equipment 102 is permitted to uniquely receive the control information corresponding to the selected program channel in accordance with the viewer's selection of the program channel.

Yet in addition, in this embodiment, the decoder 110 is constructed using a DSP, and the decoding programs are set, thereby making it possible to decode the broadcast content information items conforming to any desired encoding rules. However, in a case where the sorts of encoding systems for use in broadcasts are limited, dedicated encoding means may well be provided for the respective encoding systems for use in the broadcasts so as to decode the content information items of the broadcasts. In this case, the transmitting equipment 101 enters information for designating the encoding system, into the control information instead of

the picture decoding program. Then, the reception controller **114** of the receiving equipment **102** validates only the decoding means corresponding to the designated encoding system in accordance with the encoding system-designating information.

Now, the second operating example of the broadcasting system according to this embodiment will be described.

In this operating example, broadcast content information items are temporarily stored and are thereafter utilized.

The broadcast content information items are recorded as stated below.

When a program channel to be recorded is set by the viewer, the reception controller **114** commands the received signal memory or recorder **112** to record control information on the set program channel and the data of the program channel in parallel. However, in a case where the received signal recorder **112** cannot store signals in parallel, the control information and the data of the program channel are multiplexed and then recorded, and the recorded signals are demultiplexed and restored into two parallel signals in a playback mode. In a case where the control information has changed in the recording operation, new control information after the change is also recorded. Incidentally, it is assumed that each broadcast content information item in the program channel bears the header of a program name for every program, and that a peculiar title is affixed as a header to every group or set of information items within each program. A video tape deck, a rewritable type optical disk memory, or the like can be employed for the received signal recorder or memory **112**.

The operation of playing back the broadcast content information recorded in the received signal recorder **112** will be explained along a flow chart shown in FIG. **7**.

When the instruction of playback has been afforded from the user operation input unit **113**, the reception controller **114** checks the control information items stored in the received signal recorder **112**, successively in the order in which they have been recorded (step **702**). Upon detecting the control information **300**, the reception controller **114** compares the last program ID **310** of the pertinent control information with the current program ID thereof (step **703**). On condition that both the ID's are different, the reception controller **114** loads the control program **341** from within the control information **300** (step **704**), and it executes the control program **341** (step **705**). A step **701** signifies that the above steps are iterated until the final storage location is reached.

The flow chart of the control program **341** for use in this operating example is illustrated in FIG. **8**.

As shown in the figure, the reception controller **114** having started the run of the control program **341** first sets the contained communication information **330** of the control information **300** in the reception module **108**, the picture or video information **320** in the signal separator or demultiplexor **109** and the picture decoding program **342** the decoder **110** (step **801**).

Subsequently, the reception controller **114** checks if the playback from the received signal memory **112** is currently instructed (step **802**).

When the playback is not instructed, the ordinary processing (refer to FIG. **6**) explained as the first operating example is performed. On the other hand, when the playback is instructed, the relationship of the respective broadcast content information items within the program corresponding to the control information, with the storage locations in the received signal recorder **112** are confirmed on the basis of the headers of the broadcast content information items for every title affixed to this broadcast content information (step **804**).

The ensuing processing is performed until the end of the playback (step **805**).

More specifically, as illustrated in FIG. **10**, a program name **1001** and a playback menu **1000** which correspond to the control information are displayed on the display unit **111** (step **806**). The items of the menu **1000** are the titles **1002~1004** of the respective information items contained in the program, and the next program **1006**. The example shown in FIG. **10** is in the case of playing back the program "News" which contains the information having the title "With me" and the information having the title "Weather forecast". The titles **1002~1004** of the respective information items within the program correspond to the titles affixed to the broadcast content information items.

Subsequently, when the viewer has designated the title of desired information among the playback menu **1000** through the user operation input unit **113** (step **807**), the broadcast content information bearing the corresponding title as the header is played back in compliance with the designation (step **808** or **809**).

In a case where the next program **1006** has been designated, the start position of playback is advanced to the end location of the broadcast content information bearing the name of the current program as the header (step **810**), and the control program is run from the foregoing process for checking the control signals.

Meanwhile, the broadcast content information to which the title designated by the viewer is affixed as the header is played back in accordance with a flow chart illustrated in FIG. **9**.

First, the reception controller **114** erases the display of the menu image shown in FIG. **10** (step **901**). Subsequently, it calculates the initial or foremost storage location and the terminal or last storage location of the broadcast content information which bears the designated title as the header (steps **902**, **903**).

The broadcast content information in a section from the calculated initial location to the calculated terminal location is played back (steps **904**, **905**, **906**, **907**). The broadcast content information played back is decoded by the decoder **110**, and is displayed on the display unit **111**. Herein, the decoder **110** decodes the broadcast content information which has been played back on the basis of the picture decoding program **342** set by the reception controller **114**.

As thus far described, according to this embodiment, only the required information part in the stored programs can be played back.

In the above embodiment, there is also considered a case where the playback menu **1000** contains a plurality of multiplexed programs. In this case, the received signal memory **112** can simultaneously record all the programs which are being broadcast at the same time. Therefore, such a case can be coped with without hindrance.

Now, the third operating example according to this embodiment will be described.

In the third operating example, as illustrated in FIG. **11**, at least one external equipment is connected to the receiving equipment **102** and is controlled.

Referring to FIG. **11**, numeral **1201** indicates an external equipment controller, numeral **1202** an electronic keyboard, numeral **1203** an electronic guitar, numeral **1204** a mixer, and numeral **1205** a loudspeaker.

Each of the electronic keyboard **1202** and the guitar **1203** is an electronic musical instrument which can be controlled through a MIDI (Musical Instrument Digital Interface).

In this operating example, the transmitting equipment **101** separately encodes the sounds of the respective musical instruments being performed, subjects the respective sound codes to time-division multiplexing as broadcast content information items, and transmits the multiplexed information items over a program channel. In addition, control information corresponding to a pertinent program is endowed with a decoding program which decodes the encoded sound of the musical instrument, and MIDI data which is control information for the external musical instrument connected to the receiving equipment **102**. The MIDI data is generated for every part contained in the performance, and is entered into the control information. Besides, a program which accepts the designation of the external musical instrument to be controlled by the MIDI data is entered into the control program **341** contained in the control information **300**. The control information is transmitted so that the receiving equipment **102** can utilize the MIDI data in real time in synchronism with the performance transmitted over the program channel. In addition, the broadcast content information is transmitted in the state in which synchronizing data for the synchronization with the MIDI data is affixed thereto.

On the other hand, when the receiving equipment **102** having selected the pertinent program receives the control information, the reception controller **114** starts the control program **341** and sets the decoding program in the decoder **110**. The decoder **110** decodes the received sound in accordance with the decoding program, so as to synthesize and produce the sounds of the respective musical instruments.

Further, the reception controller **114** commands the display unit **111** to present an image shown in FIG. **12**A. Thus, it indicates that the MIDI data can be utilized in the pertinent program, and it accepts a request to commence utilization of the MIDI data.

If the utilization of the MIDI data is designated, the reception controller **114** presents a menu shown in FIG. **12**B. Thus, it accepts the designation of either an automatic performance or a manual performance and also accepts the for which it is part desired to utilize the MIDI data.

When the automatic performance is designated and the desired part to utilize the MIDI data is designated, the reception controller **114** commands the decoder **110** to produce no sound for the designated part. Then, the MIDI data of the designated part is output to the external equipment controller **1201** in order that the pertinent part may be performed in synchronism with the output sound of the connected electronic musical instrument, on the basis of the synchronizing data affixed to the broadcast content information.

The external equipment controller **1201** sends the received data onto a MIDI bus, and controls the musical instruments so as to produce the sound of the designated part.

On the other hand, when the user designates the manual performance mode in which he/she plays the musical instrument, the reception controller **114** commands the decoder **110** to produce no sound for the designated part, and it ends its processing.

As thus far described, according to this operating example, the user can play his/her electronic musical instrument in time to the transmitted performance.

Incidentally, this embodiment is not restricted to the broadcasting form, but it is quite similarly applicable to

picture communications in one-to-one correspondence, such as video telephony.

Besides, in this embodiment, the individual broadcasting channels have been described as being physical channels of different broadcasting frequencies. The system of this embodiment, however, is also applicable to a case where the individual broadcasting channels are logical channels. More specifically, in such a case where all the program channels and the control channel are multiplexed into a single physical channel by, e.g., time-division multiplexing, the following measure may be taken: The position of the control channel and the positions of individual control information items contained in the control channel are fixed. The position of a selected one of the program channels, and broadcast content information contained in the program channel are specified by the control information for the selected channel.

Now, the fourth operating example concerning this embodiment will be described. This operating example consists of a multiplexing equipment in which a plurality of broadcast information items are multiplexed into a single item of broadcast information by the use of the transmitting equipment **101** in the first embodiment. FIG. **13** exemplifies the multiplexing equipment **1301** in the fourth embodiment. Referring to the figure, a signal synthesizer/encoder **104**, a transmission module **105**, a program memory **106** and a transmission controller **107** are the same as in the transmitting equipment **101** of the first embodiment. In the case of the multiplexing equipment **1301**, unlike the case of the transmitting equipment **101**, pictures are not directly input to the signal synthesizer/encoder **104**, but broadcast information items **1303** are respectively turned by reception units **1302** into pictures, which are input to the signal synthesizer/encoder **104**. Thereafter, the signals are synthesized and have control information affixed thereto by the signal synthesizer/encoder **104**, and the resulting information **1304** into which the plurality of information items have been multiplexed is output from the transmission module **105**. Thus, the plurality of broadcasts can be accepted and multiplexed. Moreover, in the case where the recording in the second embodiment is carried out, a number of programs desired by the user can all be recorded even when they are broadcast in different channels at the same time, by way of example.

Furthermore, the installation of the multiplexing equipment **1301** on a video recorder makes it possible to multiplex the plurality of broadcast information items into the single broadcast information and to store the multiplexed broadcast information in a record medium. In a playback mode, required information in the recorded broadcast information can be played back by executing the decoding operation in the foregoing embodiment. In this way, the plurality of broadcast information items can be recorded on the single record medium in this embodiment in contrast to the recording aspect in which only one broadcast information (or program) can be recorded on one record medium.

As set forth above, the present invention can provide a television broadcasting system in which compression systems, multiplexing systems, the selection of pictures by viewers, etc. are rendered flexible in order to offer multifarious services to the viewers.

What is claimed is:

1. A television broadcasting method wherein a transmitting equipment broadcasts a broadcast program picture, while a receiving equipment receives and displays a broadcasted broadcast program picture from said transmitting equipment, said method comprising the steps of:

broadcasting control information by means of said transmitting equipment, said control information including

broadcast system standard information specifying a broadcast system standard for receiving and displaying said broadcast program picture at said receiving equipment;

broadcasting said broadcast program picture in accordance with said broadcast system standard by means of said transmitting equipment;

receiving said control information by means of said receiving equipment; and

displaying said broadcast program picture broadcasted from said transmitting equipment, on a basis of said broadcast system standard specified by said broadcast system standard information included in a received said control information by means of said receiving equipment.

2. A television broadcasting method as defined in claim **1**, wherein said transmitting equipment encodes said broadcast program picture and then broadcasts said broadcast program picture as an encoded broadcast program picture, and includes a decoding program for decoding said encoded broadcast program picture into said broadcast system standard information included in said control information which is broadcasted, and wherein said receiving equipment decodes said encoded broadcast program picture by executing said decoding program in said broadcast system standard information included in said received control information and then displays a decoded broadcast program picture.

3. A television broadcasting method as defined in claim **1**, wherein said transmitting equipment multiplexes a plurality of broadcast program pictures in accordance with a multiplex system and then broadcasts multiplexed broadcast program pictures, and includes multiplex information specifying said multiplex system in said broadcast system standard information for use in separating each of said broadcast program pictures at said receiving equipment,

and wherein said receiving equipment selects a subject broadcast program picture which is to-be-displayed, separates said subject broadcast program picture from said multiplexed broadcast program pictures on a basis of said multiplex system specified by said multiplex information in said broadcast system standard information included in received said control information and displays said subject broadcast program picture which has been separated.

4. A television broadcasting method as defined in claim **1**, wherein said transmitting equipment multiplexes a plurality of broadcast program pictures and then broadcasts multiplexed broadcast program pictures, and includes in said control information content information items, each of which indicates a respective content of said broadcast program pictures, and

wherein said receiving equipment displays said each respective content of said broadcast program pictures multiplexed and broadcasted as indicated by said content information items included in a received said control information, accepts a user selection of a subject broadcast program picture to-be-displayed, separates said subject broadcast program picture in accordance with an accepted said user selection, and displays said subject broadcast program picture which has been separated.

5. A television broadcasting method wherein a transmitting equipment transmits a broadcast program picture, and a receiving equipment receives and displays a transmitted said broadcast program picture from said transmitting equipment, said method comprising the steps of:

transmitting a control program by means of said transmitting equipment, said control program, upon execution at said receiving equipment, allowing for acceptance of user instructions from a user and controlling receiving and displaying of said broadcast program picture at said receiving equipment in accordance with said user instructions in order to support customized use of said broadcast program picture by said user of said receiving equipment; and

receiving and executing said control program at said receiving equipment, and thereby supporting customized use of said broadcast program picture by means of said receiving equipment.

6. A television broadcasting system comprising a transmitting equipment which broadcasts a broadcast program picture, and at least one receiving equipment which receives and displays a broadcasted broadcast program picture from said transmitting equipment;

wherein said transmitting equipment comprising a control information transmission means to broadcast control information in accordance with a predetermined format, said broadcast control information including a broadcast system standard information specifying a broadcast system standard for receiving and displaying said broadcast program picture at said receiving equipment, and broadcast program picture transmission means for broadcasting said broadcast program picture in accordance with said broadcast system standard; and

wherein said receiving equipment comprising control information reception means to receive said broadcast control information in accordance with said predetermined manner, and broadcast program picture processing means to receive and display said broadcast program picture broadcasted from said transmitting equipment, in accordance with said broadcast system standard specified by said broadcast system standard information included in a received said broadcast control information.

7. A television broadcasting system as defined in claim **6**, wherein said broadcast program picture processing means of said receiving equipment includes a memory means to store therein a received said broadcast program picture and a received said broadcast control information, and further comprises a playback means to play back said broadcast program picture stored in said memory means, in accordance with a user instruction, and display means to display a played-back said broadcast program picture in accordance with a stored said broadcast control information.

8. A television broadcasting system as defined in claim **6**, wherein said broadcast program picture transmission means of said transmitting equipment encodes said broadcast program picture and then broadcasts an encoded said broadcast program picture, and said control information transmission means of said transmitting equipment includes a decoding program for decoding an encoded said broadcast program picture in said broadcast control information which is broadcasted,

and wherein said broadcast program picture processing means of said receiving equipment includes a decoder which decodes a received said broadcast program picture by executing said program included in a received said broadcast control information, and a display unit which displays said broadcast program picture decoded by said decoder.

9. A television broadcasting system as defined in claim **7**, wherein said broadcast program picture transmission means of said transmitting equipment multiplexes a plurality of

broadcast program pictures using a multiplex system and then broadcasts multiplexed said broadcast program pictures, and said control information transmission means of said transmitting equipment includes multiplex information specifying said multiplex system in said broadcast system standard information included in said broadcast control information which is broadcasted for use in separating each broadcast program picture of said broadcast program pictures at said receiving equipment;

and wherein said broadcast program picture processing means of said receiving equipment includes a separator which selects a subject broadcast program picture to-be-displayed and separates said subject broadcast program picture from said multiplexed broadcast program pictures on a basis of said multiplex system as specified by said multiplex information in said broadcast system standard information included in said received broadcast control information, and a display unit which displays said subject broadcast program picture separated by said separator.

10. A television broadcasting system as defined in claim **9**, wherein said transmitting equipment includes a plurality of reception units which receive a plurality of broadcast information items, respectively, and a received said broadcast information items are multiplexed into multiplexed said broadcast program pictures which are to be transmitted by said transmitting equipment.

11. A television transmission equipment comprising an input means for inputting a plurality of broadcast program picture items, a processing means for converting a plurality of input said broadcast program picture items into a signal for broadcast in accordance with a predetermined broadcast system standard, and transmission means for broadcasting said signal and control information specifying said predetermined broadcast system standard.

12. A television transmission equipment as defined in claim **11**, wherein said input means inputs a plurality of broadcast program picture items, said processing means multiplexes said plurality of input said broadcast program picture item in accordance with a multiplex system, and said transmission means broadcasts a multiplexed said broadcast program picture items and multiplex control information specifying said multiplex system.

13. A television reception equipment comprising a reception means for receiving a broadcast program picture and control information which are broadcasted in accordance with a predetermined format, said control information specifying a broadcast system standard, and a broadcast content processing means for controlling and displaying said broadcast program picture in accordance with said broadcast system standard specified by said control information received by said reception means.

14. A television reception equipment as defined in claim **13**, wherein said broadcast program picture to be received by said reception means is an encoded said broadcast program picture, and said control information to be received by said reception means includes decoding information for specifying a decoding system for an encoded said broadcast program picture, and wherein said broadcast content processing means includes a control means for specifying a decoding system for said broadcast program picture in accordance with said control information received by said reception means, a decoder means for decoding said broadcast program picture in accordance with said decoding system specified by said control means, and display means for displaying said broadcast program picture decoded by said decoder means.

15. A television reception equipment as defined in claim **13**, wherein said reception means receives a plurality of broadcast program pictures multiplexed in a time division manner, and said control information includes a multiplex information item for specifying a time-division multiplexing system of said time-division multiplexed broadcast program pictures, and wherein said broadcast content processing means includes a control means for specifying said time-division multiplexing system in accordance with said multiplex information item included in said control information received by said reception means, a separation means for selecting a subject broadcast program picture to-be-displayed and separating said subject broadcast program picture in accordance with said time-division multiplexing system specified by said control means, and display means for displaying a subject broadcast program picture separated by said separation means.

16. A television reception equipment as defined in claim **15**, wherein said control information further includes content information items indicating contents of said broadcast program pictures multiplexed and broadcasted, and wherein said television reception equipment further comprises a control means and a display means, and said control means operates to display said contents of said plurality of broadcast program pictures indicated by said content information items on said display means on a basis of a received said control information, operates to accept selection of a subject broadcast program picture to-be-displayed, and operates to display a selected said subject broadcast program picture on said display means.

17. A television reception equipment comprising a first reception means for receiving control information including frequency broadcast system standard data indicating each frequency channel of a plurality of broadcast program pictures which are subjected to frequency multiplexing and broadcasted, a second reception means for receiving at least one of frequency-multiplexed and broadcasted said plurality of broadcast program pictures in accordance with said control information and frequency broadcast system standard data received by said first reception means, and a display means for displaying a subject broadcast program picture received by said second reception means.

18. A television broadcasting method as claimed in claim **1**, wherein said transmitting equipment encodes said broadcast program picture in accordance with a coding system and then broadcasts an encoded said broadcast program picture, and includes coding information specifying said coding system of said encoded said broadcast program picture into said broadcast system standard information included in said control information which is broadcasted, and wherein said receiving equipment decodes a received said broadcast program picture, on a basis of said coding system specified by said coding information in said broadcast system standard information included in said received said control information and then displays a decoded said broadcast program picture.

* * * * *

EXHIBIT B

US005534934A

United States Patent [19]

Katsumata et al.

[11] Patent Number: 5,534,934

[45] Date of Patent: Jul. 9, 1996

[54] **TELEVISION RECEIVER CAPABLE OF ENLARGING AND COMPRESSING IMAGE**

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[73] Assignee: **Hitachi, Ltd.**, Tokyo, Japan

[21] Appl. No.: **260,576**

[22] Filed: **Jun. 16, 1994**

[30] **Foreign Application Priority Data**

Jun. 18, 1993 [JP] Japan 5-146674

[51] **Int. Cl.**[6] **H04N 7/01**

[52] **U.S. Cl.** **348/445**; 348/448; 348/556

[58] **Field of Search** 348/445, 448, 348/458, 441, 556, 555, 561, 581, 582, 580, 913, 571, 704; H04N 7/01

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311891	1/1991	Japan	H04N 7/01
66634	1/1994	Japan	H04N 7/01
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Primary Examiner—Safet Metjahic

Attorney, Agent, or Firm—Kenyon & Kenyon

[57] **ABSTRACT**

To provide an image which is matched with an aspect ratio of a screen of a display unit by compressing and enlarging the whole of the image to a desired size. A video signal is sequentially written into a field memory in response to a write clock from an input terminal. A clock generating circuit supplies the field memory with a read clock having a frequency which is about ⅔ times as high as that of the write clock. A vertical enlargement control circuit reads a video signal from the field memory with a line period corresponding to a magnification factor and inhibits writing to a one-line memory with the same period to provide a line delayed output for an output signal from the field memory. A vertical interpolating circuit generates a scanning line signal by an interpolation operation in accordance with a control signal from the vertical enlargement control circuit.

6 Claims, 8 Drawing Sheets

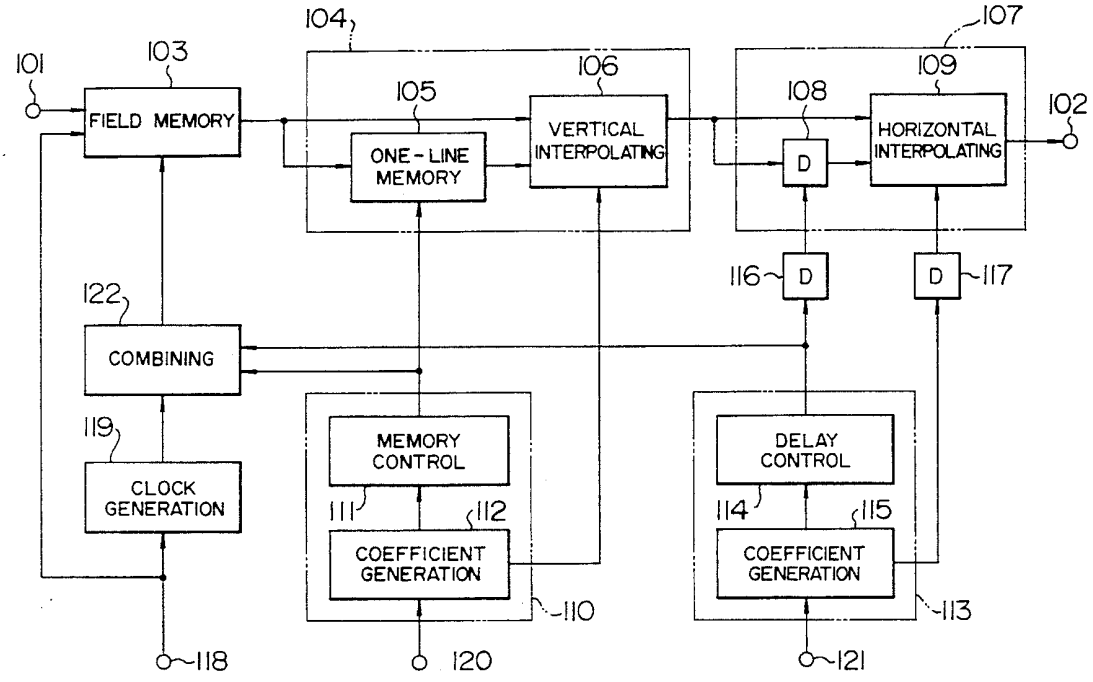


FIG. 1 PRIOR ART

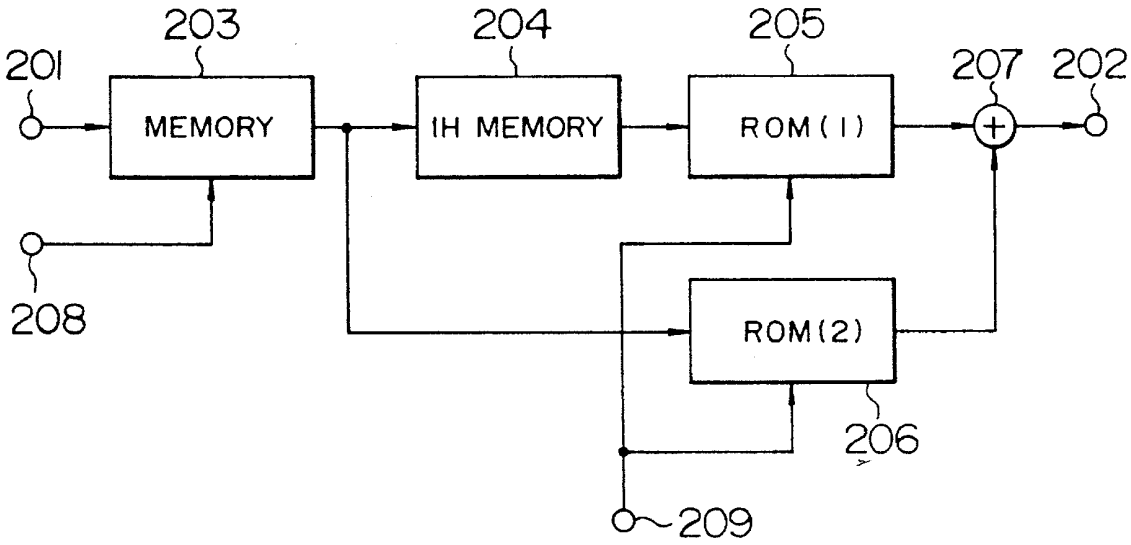


FIG. 4

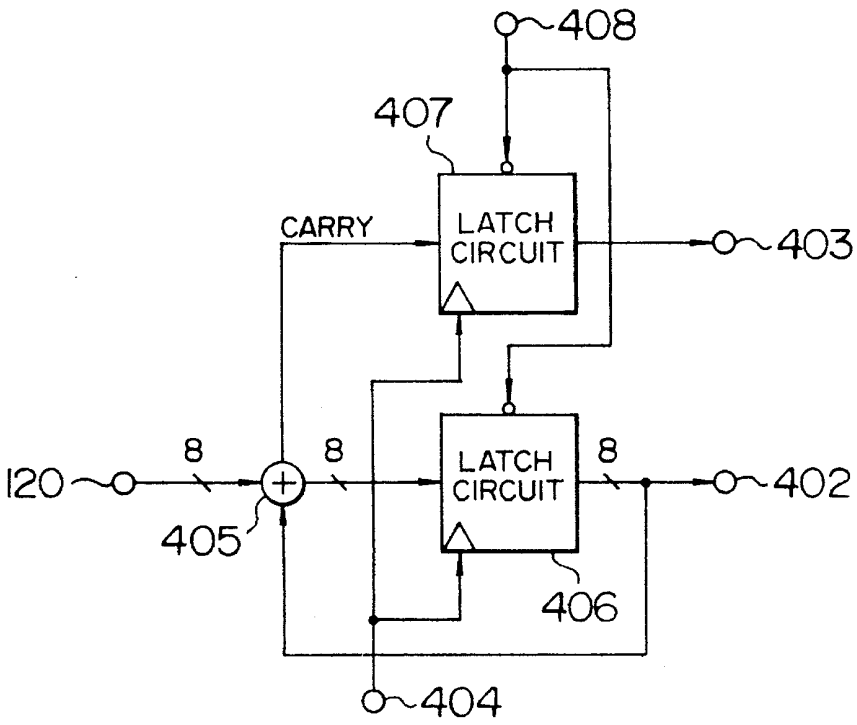


FIG. 2

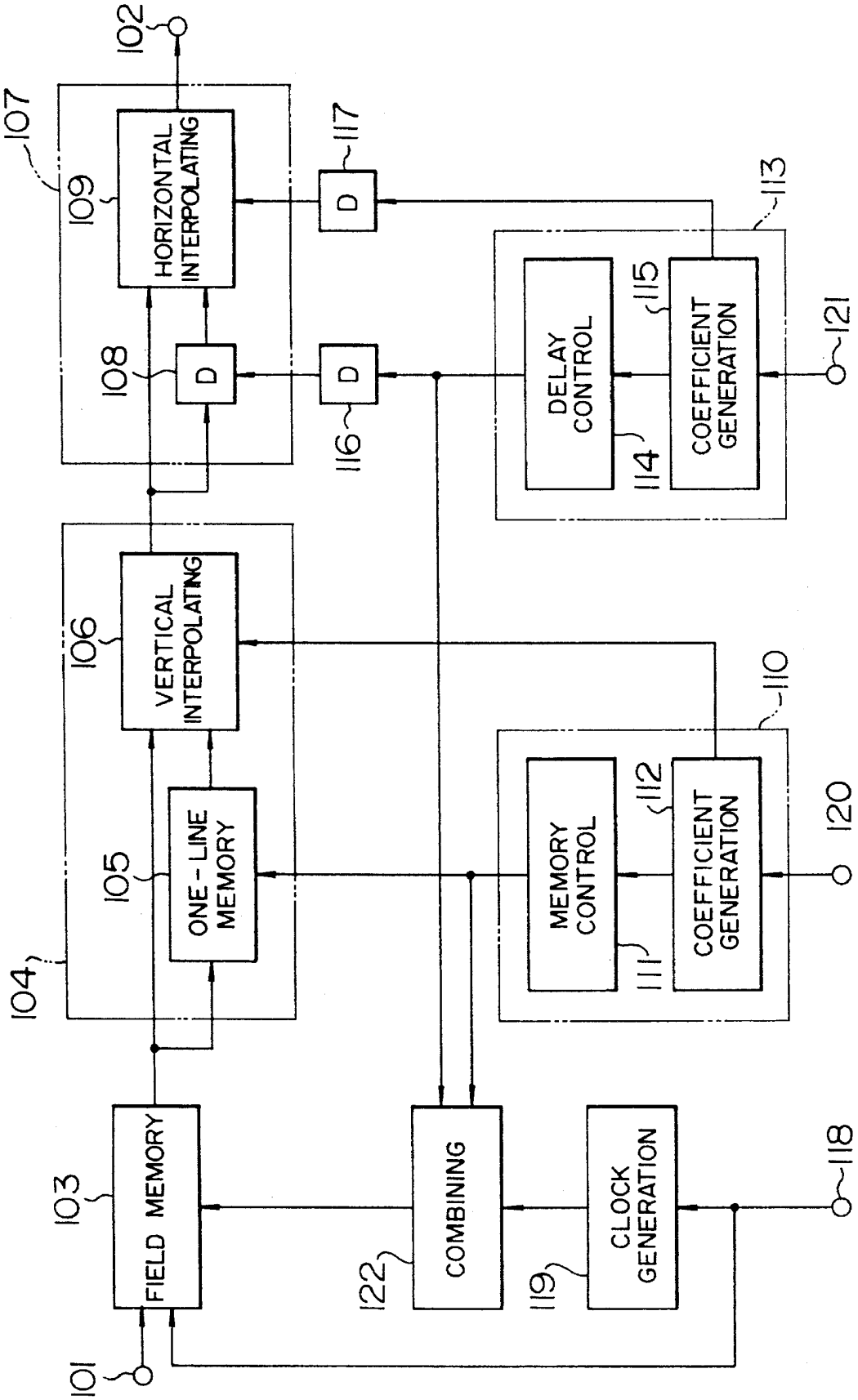

102
107
109
HORIZONTAL INTERPOLATING
117
D
113
108
D
D
116
DELAY CONTROL
115
COEFFICIENT GENERATION
121
114
106
VERTICAL INTERPOLATING
110
105
ONE-LINE MEMORY
MEMORY CONTROL
112
COEFFICIENT GENERATION
120
111
104
103
FIELD MEMORY
COMBINING
CLOCK GENERATION
118
122
119
101

FIG. 3

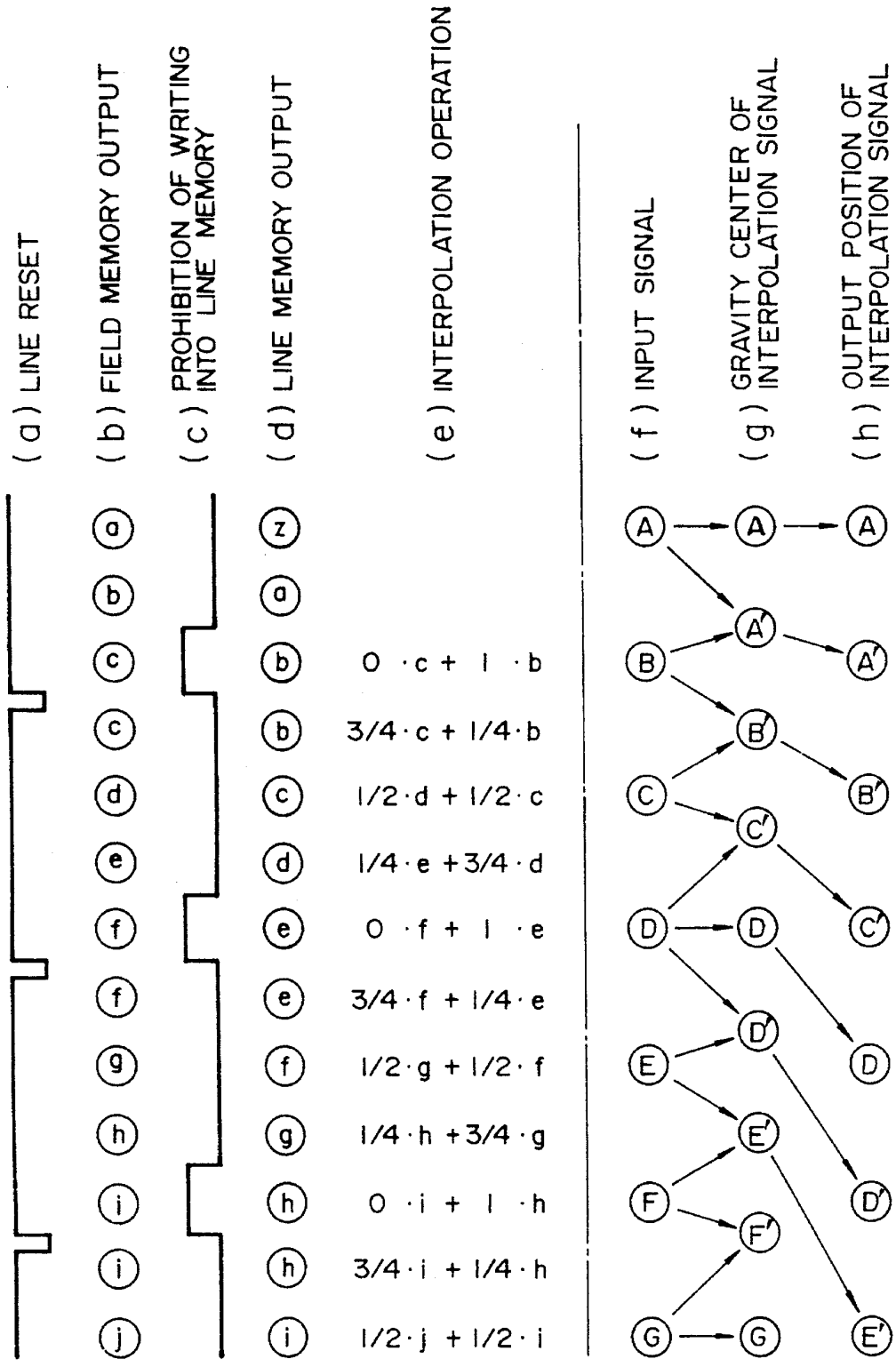

(a) LINE RESET
(b) FIELD MEMORY OUTPUT
(c) PROHIBITION OF WRITING INTO LINE MEMORY
(d) LINE MEMORY OUTPUT
(e) INTERPOLATION OPERATION
(f) INPUT SIGNAL
(g) GRAVITY CENTER OF INTERPOLATION SIGNAL
(h) OUTPUT POSITION OF INTERPOLATION SIGNAL
a
b
c
d
e
f
g
h
i
j
z
a
b
c
d
e
f
g
h
i
0 ·c + 1 ·b
3/4·c + 1/4·b
1/2·d + 1/2·c
1/4·e +3/4·d
0 ·f + 1 ·e
3/4·f + 1/4·e
1/2·g + 1/2·f
1/4·h +3/4·g
0 ·i + 1 ·h
3/4·i + 1/4·h
1/2·j + 1/2·i
A
B
C
D
E
F
G
A'
B'
C'
D'
E'
F'
G'

FIG. 5

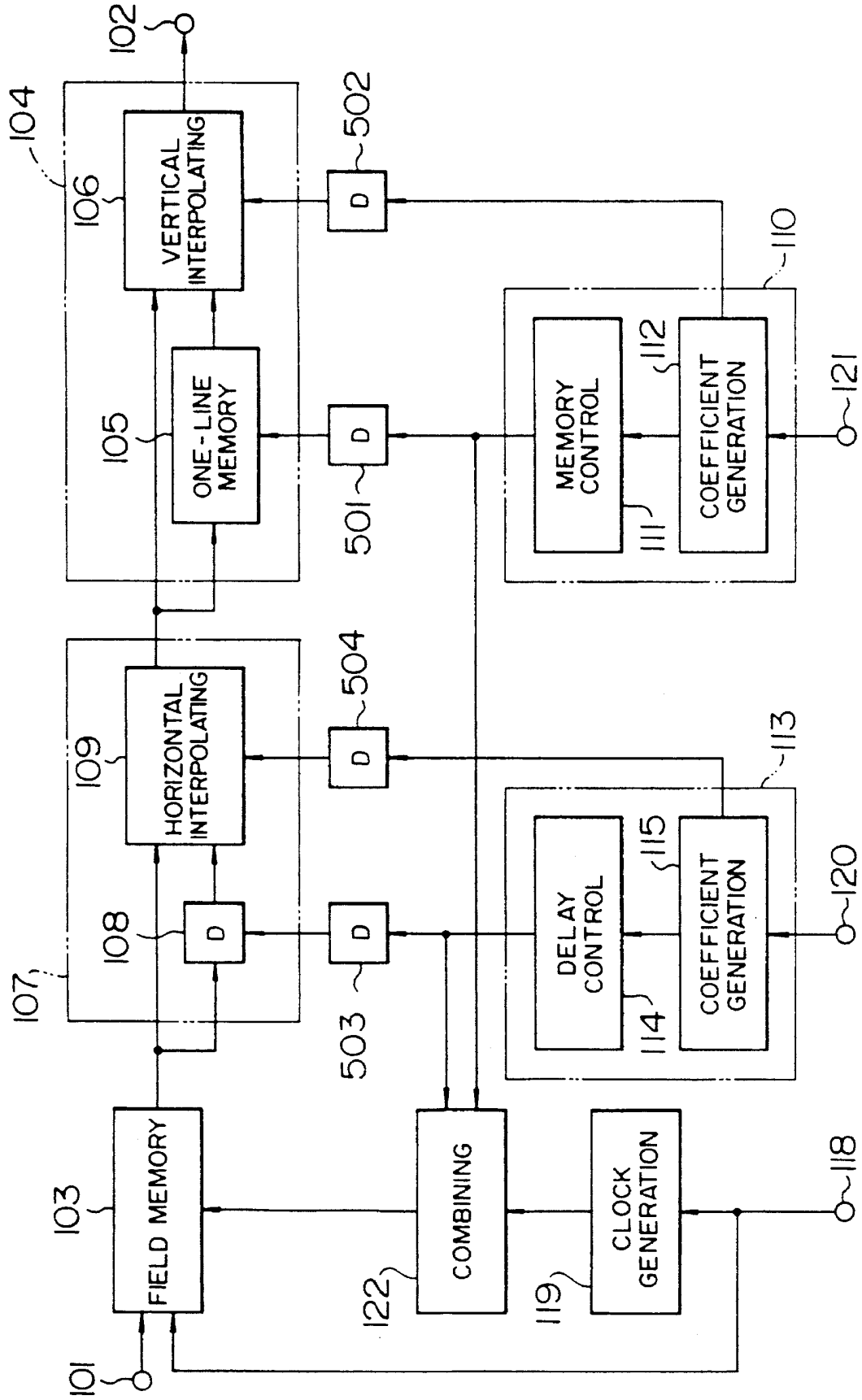

102
104
106
VERTICAL INTERPOLATING
502
D
110
105
ONE-LINE MEMORY
501
D
MEMORY CONTROL
112
COEFFICIENT GENERATION
121
111
109
HORIZONTAL INTERPOLATING
504
D
113
108
D
D
DELAY CONTROL
115
COEFFICIENT GENERATION
120
107
503
114
103
FIELD MEMORY
COMBINING
CLOCK GENERATION
118
122
119
101

FIG. 6

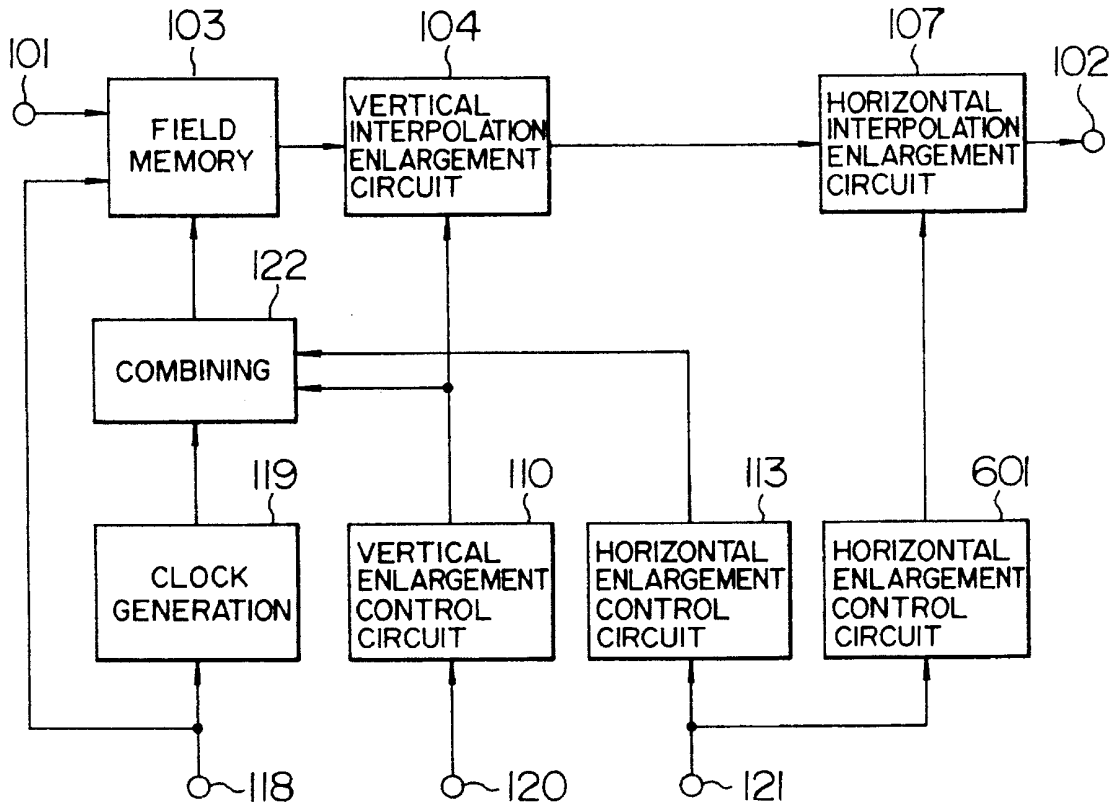

101
103
104
107
102
FIELD MEMORY
VERTICAL INTERPOLATION ENLARGEMENT CIRCUIT
HORIZONTAL INTERPOLATION ENLARGEMENT CIRCUIT
122
COMBINING
119
110
113
601
CLOCK GENERATION
VERTICAL ENLARGEMENT CONTROL CIRCUIT
HORIZONTAL ENLARGEMENT CONTROL CIRCUIT
HORIZONTAL ENLARGEMENT CONTROL CIRCUIT
118
120
121

FIG. 7

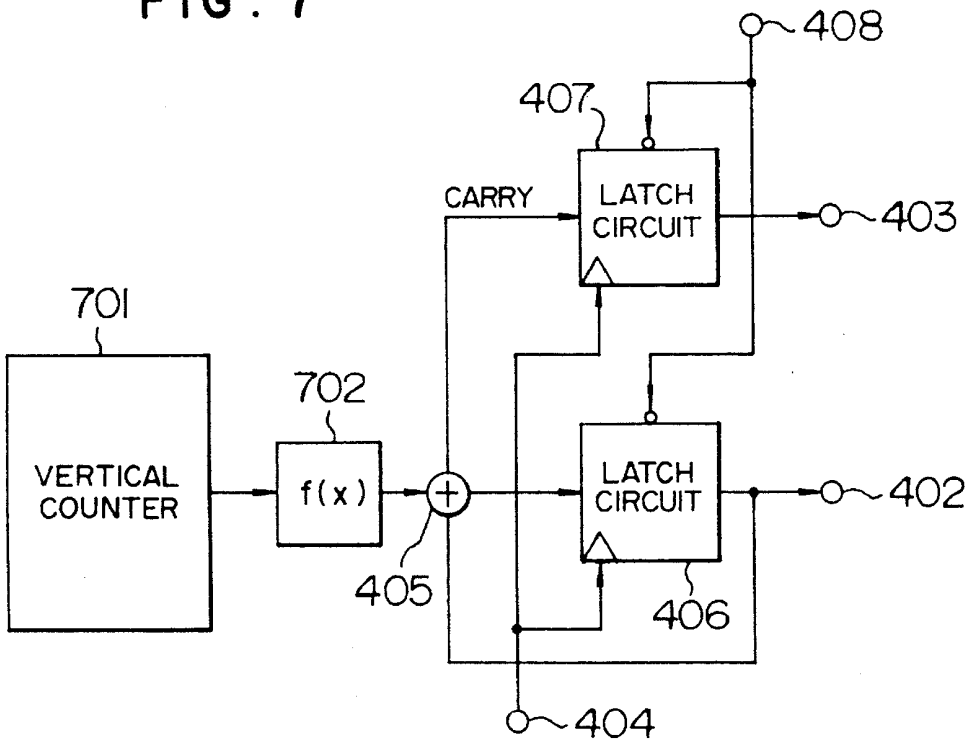
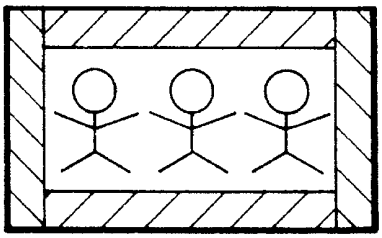

408
407
CARRY
LATCH CIRCUIT
403
701
VERTICAL COUNTER
702
f(x)
LATCH CIRCUIT
402
405
406
404

FIG. 8A

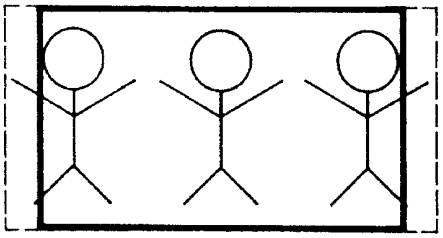


3/2 TIMES

4/3 TIMES

FIG. 8E

FIG. 8B



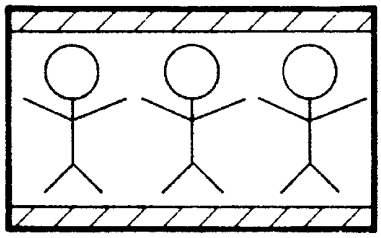
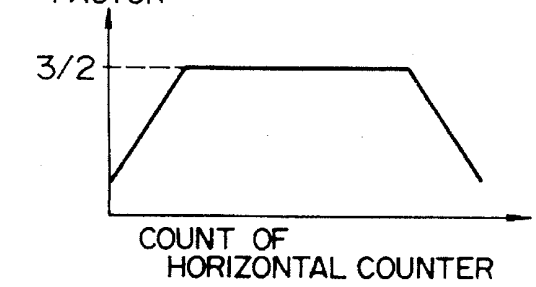


FIG. 8F

FIG. 8C



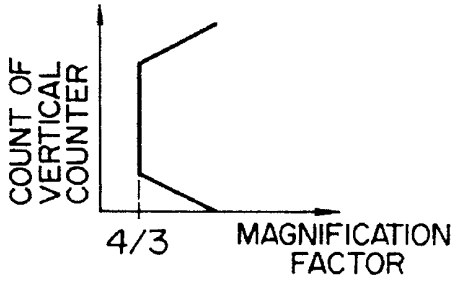
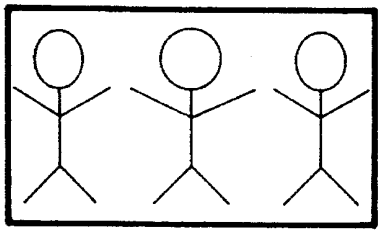


FIG. 8G

FIG. 8D



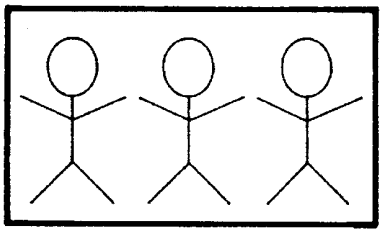


FIG. 9

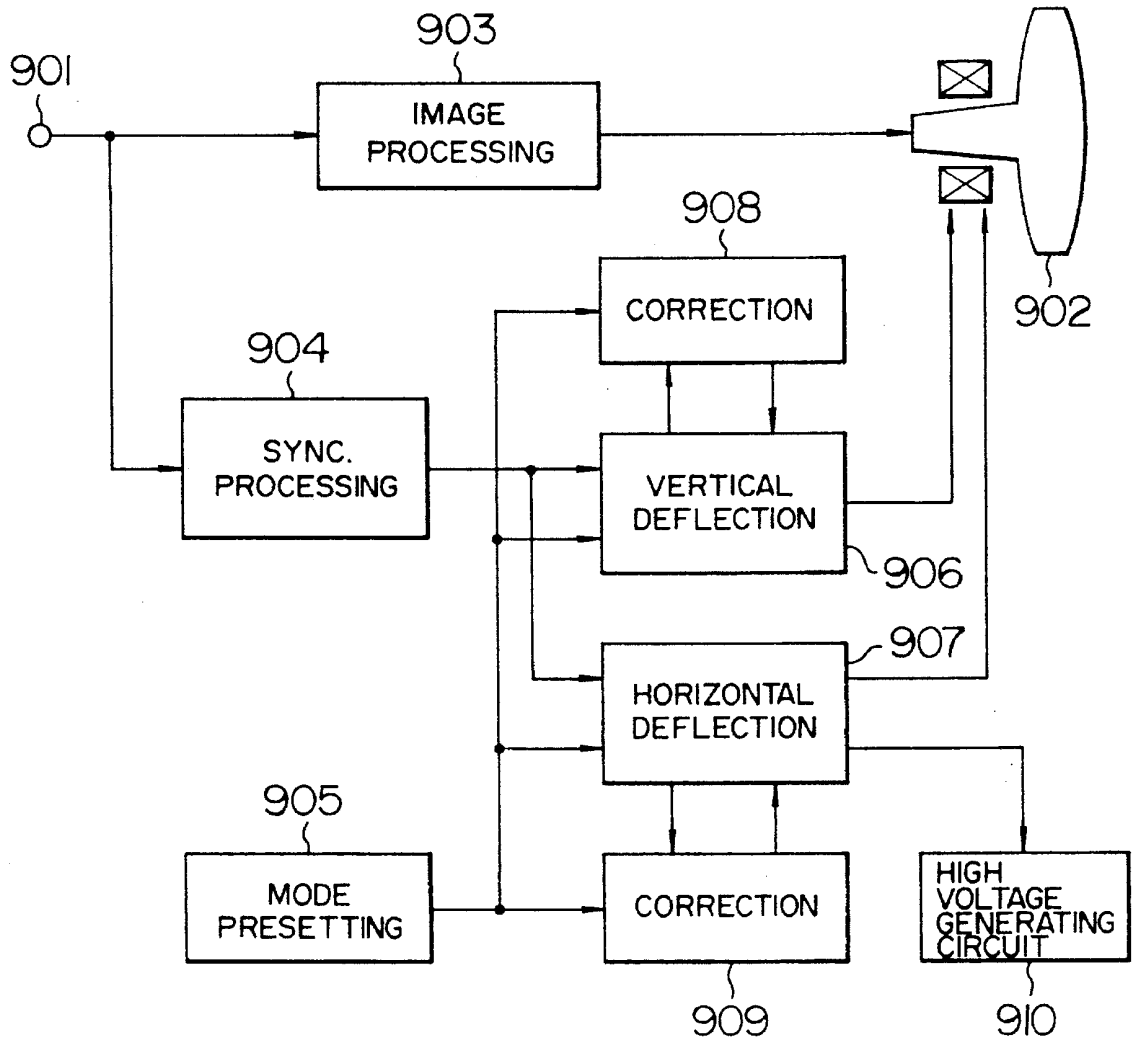

901
903
IMAGE PROCESSING
902
908
CORRECTION
904
SYNC. PROCESSING
VERTICAL DEFLECTION
906
907
HORIZONTAL DEFLECTION
905
MODE PRESETTING
CORRECTION
909
HIGH VOLTAGE GENERATING CIRCUIT
910

FIG. 10A

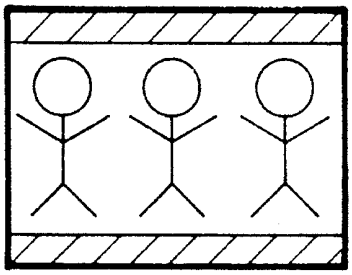
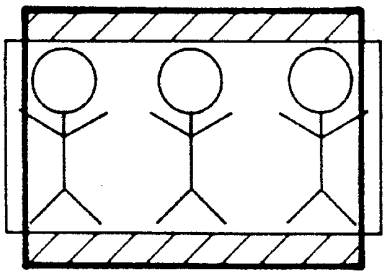
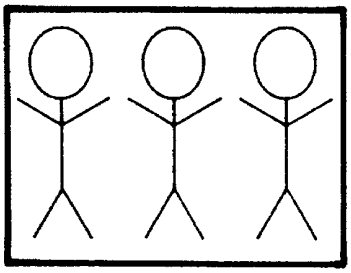


FIG. 10B



VERTICAL, HORIZONTAL ENLARGEMENT

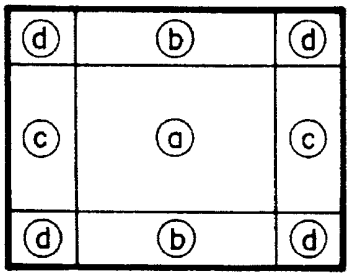
FIG. 10C



VERTICAL ENLARGEMENT AT UPPER AND LOWER SIDE AREAS

HORIZONTAL COMPRESSION AT LEFT AND RIGHT SIDE AREAS

FIG. 10D



(a) NO DISTORTION
(b) ELONGATION AT UPPER AND LOWER SIDE AREAS
(c) CONTRACTION AT RIGHT AND LEFT SIDE AREAS
(d) ELONGATION AT UPPER AND LOWER SIDE AREAS, CONTRACTION AT RIGHT AND LEFT SIDE AREAS

TELEVISION RECEIVER CAPABLE OF ENLARGING AND COMPRESSING IMAGE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to digital processing of a video signal and in particular to an image compressing and enlarging circuitry which is capable of displaying an image on a screen without an apparent disparity between the image and the screen by compressing or enlarging an image to a desired size to match the aspect ratio of the screen of a display even if the aspect ratio of the image obtained by a video signal is different from the aspect ratio of the screen of the display.

2. Description of the Related Art

Test broadcasting of high definition TV started in 1991 in Japan and the home TV sets with a screen having an aspect ratio of 16:9 have been used. Matching the TV sets that have a screen having an aspect ratio of 16:9 with the conventional TV broadcasting is critical. Thus how the aspect ratio of the image of the broadcast is changed into 16:9 is an important problem. If an image having movie size which is commonly found in a number of recent movie software packages, that is, so-called letter box type image (the aspect ratios of the image are various) in which the aspect ratio of the whole image is 4:3 and there are blanking areas on upper and lower sides of a screen is displayed on a display with a screen having an aspect ratio of 16:9, an aspect ratio which is approximate to 16:9 could be obtained by enlarging the image in a vertical direction. Therefore, enlargement of images in a vertical direction has become a critical technology.

JP-A-1-194784 discloses a combined method including a method of adapting an image having an aspect ratio of 4:3 onto a screen having an aspect ratio of 16:9 by changing the write frequency of a line memory and the read frequency thereof to compress the image in a horizontal direction and a method of enlarging the image in a vertical direction by changing the amplitude of an output of the deflecting circuit for cutting the upper and lower areas of the image.

JP-A-3-11891 discloses a technology for enlarging an image in a vertical direction by digital signal processing. The proposed circuit configuration for interpolating scanning lines using digital signal processing to enlarge the image in a vertical direction is shown in FIG. **1**.

In FIG. **1**, reference numerals **201** and **202** denote input and output terminals of digitized video signal, respectively; **203** a memory having a capacity of at least about 120 lines; **204** one-line memory; **205** and **206** ROM tables which are used for multiplying an input signal by a coefficient; **207** an adder; **208** an input terminal for a control signal for the memory **203**; **209** an input terminal for a control signal for switching tables of the ROMs **205** and **206**.

In the disclosed invention, the memory **203** is controlled to conduct reading of the same line plural times with a predetermined line period in accordance with a control signal from the input terminal **208**. As a result of delay of a video signal by one line in the one-line memory **204**, scanning line signals of adjacent upper and lower lines are supplied to the ROMs **205** and **206** and are multiplied by a coefficient in a ROM table which is selected by a control signal from the input terminal **209**. A signal having a suitable center of gravity of scanning lines can be obtained from the adder **207**.

The thus obtained enlarged image provide a large size picture displayed with high quality since the spacings between scanning lines when progressive scanning signals are used are less changed in comparison with a case in which the image are enlarged by changing the amplitude of the output of the deflecting circuit.

In such a manner, various techniques have been used to display an image having an aspect ratio of 4:3 on a screen having an aspect ratio of 16:9.

The above mentioned two inventions are excellent as systems for displaying an image having an aspect ratio of 4:3 on a screen having an aspect ratio of 16:9. However, letter box type image of movie software which are commonly found in recent software packages have various aspect ratios. It has become harder to change an image having various aspect ratios to an optimum size for displays having an aspect ratio of 16:9.

It is necessary to display a framing signal particularly in projector type displays when most images having an aspect ratio of 4:3 are compressed and displayed. A problem of a sticking of the display screen or a difference in luminescence decay of a phosphor may occur. Accordingly, a method of displaying no framing signal is required.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide an image compressing and enlarging circuit which is capable of providing an image having a size which is matched with the aspect ratio of a screen of a display by compressing and enlarging the whole of the image to a desired size.

It is another object of the present invention to provide an image compressing and enlarging circuit which is capable of providing an image that is matched with the aspect ratio of a screen of a display by partially compressing and enlarging the image.

The above mentioned object of the present invention is accomplished by providing an image compressing and enlarging circuit comprising memory means which can be controlled on a line-by-line basis, vertical enlargement control means for controlling the memory means to read the same line plural times with a line period corresponding to a preset magnification factor; horizontal enlargement control means for controlling the memory means to read the same pixel plural times with a pixel period corresponding to the preset magnification factor; clock generating means for generating a read clock having a frequency not less than that of a write clock from the write clock of said memory means; and combining means for combining output signals from said horizontal and vertical enlargement control means with an output signal from said clock generating means.

The input video signal is written into said memory means in response to said write clock. At this time, the input video signal is managed on a line-by-line basis. On the other hand, the vertical enlargement control means determines the line period associated with reading from said memory means in accordance with a preset magnification factor by performing an operation and outputs a control signal. Similarly, the horizontal enlargement control means determines the pixel period associated with reading from said memory means in accordance with a preset magnification factor and outputs a control signal. The clock generating means generates a new clock which depends on the horizontal compression factor of the image from the input write clock. Said combining means combines the control signals from said vertical and horizon-

tal enlargement control means with said read clock to supply the combined signal to said memory means.

If an image having an aspect ratio of 4:3 is displayed on a screen having an aspect ratio of 16:9 with a correct roundness, the frequency of a new read clock is made ⅓ times as high as that of the write clock and the magnification factor is preset **1**. Then, the period which is taken to read the same line again from said on a line-by-line basis and the period which is taken to read the same pixel again on a pixel-by-pixel basis would become infinitely great. This means that the read clock will have a frequency which is ⅓ times. The image will be compressed in a horizontal direction and displayed. Therefore, an image having an aspect ratio of 4:3 will be adapted on a screen having a ratio of 16:9.

If a large magnification factor, for example, ⅓ times is preset, the period which is taken for the vertical enlargement control means to read the same line in every four lines again on a line-by-line basis is preset to 4 lines. The horizontal enlargement control means controls so that the same pixel in every four pixels is read. Accordingly, a video signal which is enlarged ⅓ times in both vertical and horizontal directions will be output. A desired magnification factor can be obtained by changing said preset value.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram showing a configuration of the prior art.

FIG. **2** is a block diagram showing an embodiment of the present invention.

FIG. **3** is an explanatory view illustrating operation of the circuit of FIG. **2** and the principle of the image enlargement.

FIG. **4** is a block diagram showing the configuration of a vertical enlargement control circuit of FIG. **2**;

FIG. **5** is a block diagram showing another embodiment of the present invention.

FIG. **6** is a block diagram showing a further embodiment of the present invention.

FIG. **7** is a block diagram showing the configuration of the vertical enlargement control circuit in a further embodiment of the present invention.

FIGS. **8**A to **8**G are explanatory views showing the applications of the embodiment of FIG. **7**.

FIG. **9** is a block diagram showing a further embodiment of the present invention.

FIGS. **10**A to **10**D are explanatory views showing applications of the embodiment of FIG. **9**.

DETAILED DESCRIPTION

Now, embodiments of the present invention will be described with reference to drawings.

Referring now to FIG. **2**, there is shown an embodiment of the present invention. In FIG. **2**, a reference numeral **101** denotes an input terminal for digitized video signal; **102** an output terminal for the video signal; **103** a field memory; **104** a vertical interpolating enlarging circuit; **106** a vertical interpolating circuit; **107** a horizontal interpolating enlarging circuit; **108** an image delay circuit; **109** a horizontal interpolating circuit; **110** a vertical enlarging control circuit; **111** a memory control circuit; **112** a vertical interpolation coefficient generating circuit; **113** a horizontal enlarging control circuit; **114** an image delay control circuit; **115** a horizontal interpolation coefficient generating circuit; **116** a first delay circuit; **117** a second delay circuit; **118** an input terminal for a write clock; **119** a read clock generating circuit; **120** an input terminal for a vertical enlarging ratio preset value; **121** an input terminal for a horizontal enlarging ratio preset value and **122** a combining circuit for a memory control signal.

In FIG. **2**, an image signal which is input from the input terminal **101** is controlled by a write clock from the input terminal **118** on a line-by-line basis so that it is sequentially written into the field memory **103**. The clock generating circuit **119** generates a read clock having a frequency which is about ⅓ times as high as that of the input write clock and supplies it to the field memory **103** via the combining circuit **122**. Accordingly, the video signal in which an image is compressed in a horizontal direction will be read from the field memory **103**. The vertical enlarging control circuit **110** controls the field memory **103** via the combining circuit **122** for reading the video signal from the field memory **103** with a line period corresponding to a magnification factor. The circuit **110** prohibits writing of the one-line memory **105** included in the vertical enlarging circuit **104** with the same period to provide a line delay output of an output signal of the field memory **103**. Manner of this operation is illustrated in FIG. **3**.

FIG. **3** is an explanatory view showing control of a scanning line in case where the scanning line is enlarged ⅓ times in a vertical direction.

FIG. **3**(*b*) shows an output signal of the field memory **103**. The same scanning line is repeatedly read in synchronization with a line reset (FIG. **3**(*a*)) which is conducted by the memory control circuit **111**. The output signal is provided from the one-line memory **105** (FIG. **3**(*d*)) by prohibiting writing of one line before line reset (FIG. **3**(*a*)) in response to a write prohibiting control signal of the one-line memory **105**. As a result, signals for upper and lower adjacent two scanning lines are supplied to the vertical interpolating circuit **106**. That is, the signals shown in FIGS. **3**(*b*) and **3**(*a*) are necessarily signals for adjacent scanning lines.

The vertical interpolating circuit **106** generates a scanning line signal by an interpolating operation (FIG. **3**(*e*)) in accordance with a control signal from the vertical enlarging control circuit **110**.

Configuration of the vertical enlarging control circuit **110** is shown in FIG. **4**. In FIG. **4**, a reference numeral **120** denotes an input terminal for an enlargement preset value which is determined in accordance with the magnification factor; **404** an output terminal for an interpolation coefficient; **403** an output terminal for a memory control signal; **404** an input terminal for a pulse having one line period; **405** an adder for adding the interpolation coefficient to the magnification factor preset value input from the input terminal **120**; **406** a latch circuit for an output signal of the adder **405**; **407** a latch circuit for a carry out signal of the adder **405**.

This circuit configuration is designed for 8 bits of the output interpolation coefficient. A new interpolation coefficient in each line can be serially obtained by repeatedly adding the magnification factor preset value with the fed back interpolation coefficient in the adder **405** in accordance with the pulse input from the input terminal **404**. At this time, the carry signal for the adder **405** will become a memory control signal for repeatedly reading the same line in the field memory **108**. In case of an 8 bit system, the relation between the preset value X of the magnification factor and the actual magnification factor Z can be represented by the formula as follows:

$$Z=256/(256-X)$$

As is apparent from the above mentioned formula, a theoretically desired magnification factor can be obtained by increasing the bit precision.

On the other hand, the scanning line will become a signal having a gravity center in a position of FIG. **3**(*g*) relative to the input video signal shown in FIG. **3**(*f*) (video signal input from the input terminal **101**). By displaying this signal in position of FIG. **3**(*h*) of the actual scanning line, a video signal representing an image which is enlarged in a vertical direction can be obtained.

Enlargement in a horizontal direction can be achieved in the same manner as the enlargement in a vertical direction. A delay control signal which is generated by the horizontal enlargement control circuit **113** is fed to the field memory **103** via the combining circuit **122**. The field memory is controlled to read the same pixel therefrom again with a period corresponding to the magnification factor in response to the delay control signal so that a video signal representing an image which is enlarged in a horizontal direction is obtained. The horizontal enlarging circuit **107** conducts a horizontal interpolation in accordance with a control signal from the horizontal enlargement control circuit **113** to provide a video signal representing an image which is enlarged in a horizontal direction and balanced in gravity center. Delay circuits **116** and **117** are inserted for adjusting the delay time between the control of the field memory **103** and the control of the pixel delay circuit **108**, and the horizontal interpolation circuit **109**.

Temporal compression of an image in a horizontal direction and enlargement of an image in vertical and horizontal directions to display the image having an aspect ratio of 4:3 on a screen having an aspect ratio of 16:9 by using the field memory **103** and one-line memory **105**, etc. in such a manner in the present embodiment can be conducted by a simple circuit configuration. For example, use of a field memory HM 530281 manufactured by Hitachi Ltd. makes it possible to repeatedly read the same line by using a line reset function to provide a simple control.

Another embodiment of the present invention is shown in FIG. **5**. In FIG. **5**, a reference numeral **501** denotes a delay circuit for delaying a control signal for the field memory **103**; **502** a delay circuit for an interpolation coefficient; the other components are identical with those of the embodiment of FIG. **2**. The present embodiment is different from the embodiment of FIG. **2** only in that enlargement of an image in a vertical direction is conducted in a vertical direction after enlargement in a horizontal direction is conducted in the horizontal enlargement circuit **107**. Operation of the circuit in the present embodiment is identical with that of the embodiment of FIG. **2**.

The delay periods of time of the delay circuits **503** and **504** are much shorter than those of **116** and **117** of the embodiment of FIG. **2**. The scale of the circuit can be advantageously reduced. The delay circuits **501** and **502** are controlled on a line-by-line basis. Accordingly, necessity for delay is almost eliminated by considering the timing of the control signal generation of the vertical enlargement control circuit **110**. In other words, adopting of the configuration of the present embodiment provides a circuit having a smaller scale which is capable of compressing and enlarging an image in a desired manner.

A further embodiment of the present invention is shown in FIG. **6**. In FIG. **6**, a reference numeral **601** denotes a second horizontal enlargement control circuit having the same configuration as that of the horizontal enlargement control circuit **113**. The other components are identical with those of the embodiment of FIG. **2**. The present embodiment

is different from the embodiment of FIG. **2** in that it includes a second horizontal enlargement control circuit **601** operating in the same manner as the horizontal enlargement control circuit **113**. Operation of the circuit of the present embodiment is identical with that of the embodiment of FIG. **2**.

A first enlargement control circuit **113** controls the field memory **103** in accordance with a magnification factor preset value fed from an input terminal **121** to provide a video signal representing an image which is enlarged in a horizontal direction. A second horizontal enlargement control circuit **601** is reset with a time lag which is delayed between the field memory **103** and the horizontal interpolation enlargement circuit **107** relative to the reset timing of the first horizontal enlargement control circuit **113** to provide a delay control signal for controlling the pixel delay circuit **108** in the horizontal interpolating enlarging circuit **107** and a coefficient value for controlling the horizontal interpolating circuit **109**.

As a result, the delay circuits **116** and **117** which are necessary in the embodiment of FIG. **2** are eliminated. A most suitable circuit can be formed by choosing a circuit having a smaller scale from either the delay circuits **116** and **117** of FIG. **2** or the second horizontal enlargement control circuit **601** in FIG. **6**.

In the above mentioned embodiments, the whole of the image can be compressed or enlarged to a desired size in both vertical and horizontal directions by the vertical enlargement control circuit **110** and the horizontal enlargement control circuit **113**. This approach is advantageous in reduction in blanking (no signal) areas on a screen when a laterally elongated image such as letter box type movie image represented by the currently available video signals are displayed on a screen of display having an aspect ratio 16:9. However, for an image having a usual aspect ratio of 4:3, the area of the image which is rendered invisible on the screen by the enlargement is large. Further, for the letter box image, the right and left side areas of the image is rendered invisible by the alignment of the image with the upper and lower sides of the screen and blanking areas are formed on the upper and lower areas of the screen by the alignment of the image to the right and left sides of the screen, creating a disparity feeling between the image signal and the display. It is also reported that a sticking problem occurs on the screen.

An embodiment in which the above mentioned problems are overcome will be described with reference to FIG. **7**. The present embodiment is different from the above mentioned embodiment in that the vertical and horizontal enlargement control circuits **110** and **113** are improved.

FIG. **7** is a block diagram showing the configuration of the vertical enlargement control circuit **110**.

In FIG. **7**, a reference numeral **701** denotes a vertical counter for counting the number of lines on the screen; **702** a numerical value converter for converting the value or count of vertical counter **701** in accordance with a predetermined function. The other components are identical with those in FIG. **4**. Since the preset value of the magnification factor from the input terminal **120** in the embodiment of FIG. **4** can be freely converted in accordance with the presetting of the numerical value converter **702** depending upon the location on the screen, a desired area in the image can be enlarged at a desired ratio. The commercial value converter can be formed of logical circuits if the function is simple. For a complicated function, a look-up table system using ROMs, etc. may be adopted. An application in this embodiment is shown in FIG. **8**.

FIG. **8**(A) shows an image which is represented by a video signal of the current format and is compressed in a

horizontal direction and is then displayed on a screen having an aspect ratio of 16:9. The image of the laterally elongated letter box type and its aspect ratio is presumed about 2:1. The whole of the image including blanking areas prior to compression has an aspect ratio of 4:3. FIG. **8**B shows an image of FIG. **8**A which is enlarged ⅔ times in both vertical and horizontal directions. The size of the image in a horizontal direction is equal to that of the screen having an aspect ratio of 16:9. However, blanking areas are left on the upper and lower side of the screen in this case as mentioned above, giving a feeling that the image is not proper.

FIG. **8**C shows a function in the numerical value converter **702** shown in FIG. **7**. Ordinate denotes a value (count) of the vertical counter **701** while abscissa denotes a magnification factor. This function provides a magnification factor of ⅔ in the center of the screen and in the vicinity thereof and increases the magnification factor on the upper and lower side areas of the screen and provides an average magnification factor of ⅔ in a vertical direction. Definition of such a function in the numerical value converter **702** provides an image which is displayed on a screen having an aspect ratio of 16:9 without blanking areas. Since the magnification factor in a horizontal direction is equal to that in a vertical direction in the central area on the screen, the image is displayed with a correct roundness. The roundness is changed only in the edges of screen. This hardly gives a feeling of disparity for the image.

FIG. **8**E shows an image which is enlarged ⅔ times in both vertical and horizontal directions. The size of the image in a vertical direction is equal to that of the screen having an aspect ratio of 16:9. Some areas of the image in a horizontal direction are lost. In this case, concept of the above mentioned numerical value converter **702** is introduced to the horizontal enlargement control circuit **113**. An input signal of the numerical value converter **702** representing the count of the horizontal counter (not shown) and a function determining the magnification factor which decreases on opposite sides of the screen in a horizontal direction will be chosen. If the average magnification factor in a horizontal direction is preset to ⅔ times, the whole of the image can be displayed on a screen having an aspect ratio of 16:9 as shown in FIG. **8**G. Also in this case, the image is distorted only at the opposite side areas of the screen in a horizontal direction.

In such a manner, the image can be partially compressed and enlarged by combination of the numerical value converter **702** shown in FIG. **7** with a circuit which is capable of enlarging the image shown in FIG. **2** to a desired size in the present embodiment. Accordingly, an image having an aspect ratio of 4:3 or letter box size image can be displayed on the screen having an aspect ratio of 16:9 without giving rise to any imaging problems.

A further embodiment of the present invention is shown in FIG. **9**. In FIG. **9**, a reference numeral **901** denotes an input terminal of video signal; **902** a display including a screen having an aspect ratio of 4:3; **903** an image processing circuit for conducting signal processing for input video signal such as Y/C separation and sending the processed signal to the display **902**; **904** a synchronization processing circuit for taking a synchronization signal from a video signal; **905** a mode presetting circuit for presetting the enlargement/compression factor of the video signal; **906** a vertical deflection circuit for outputting a vertical deflecting current for driving the display **902** in accordance with a mode specified by the mode presetting circuit **905** from an output signal of the synchronization processing circuit; **906** a horizontal deflection circuit for outputting a horizontal deflecting current for driving the display **902** in accordance with a mode specified by the mode presetting circuit **905** from the output signal of the synchronization processing circuit **904**; **908** and **909** first and second deflecting current correcting circuits which correct the deflecting current outputs of the vertical and horizontal deflecting circuits **906** and **907**, respectively; and **910** a high voltage generating circuit.

The present embodiment is different from the above mentioned embodiments in that partial compression and enlargement of image is conducted by the deflection circuits and the deflection current correcting circuit. The vertical deflection circuit **906** generates a vertical saw-tooth wave for driving the display **902** in accordance with a vertical deflecting pulse from the synchronization processing circuit **904**. Similarly, the horizontal deflection circuit **907** generates a horizontal saw-tooth wave for driving the display **902** in accordance with a horizontal deflecting pulse from the synchronization processing circuit **904**. At his time, the vertical and horizontal deflection circuits **906** and **907** change the gradient and the phase of the generated saw-tooth wave. Accordingly, the whole of the image is enlarged in vertical and horizontal directions.

On the other hand, the first and second deflection current correcting circuits **906** and **909** correct the operation of the vertical and horizontal deflection circuits **906** and **907**, respectively to give partial distortion to the saw-tooth wave. This correction partially changes the gradient of the saw-tooth wave so that the image have enlargement/compression factor which changes depending upon the location on the screen.

The present embodiment is particularly effective for displaying a letter box type image on a screen having an aspect ratio of 4:3. An application of the embodiment is shown in FIG. **10**.

FIG. **10**A shows a letter box type image which is displayed on a screen having an aspect ratio of 4:3. Letter box type displays will be adopted in the second generation EDTV systems and are expected to become more popular. In the second generation EDTV systems, high definition information is displayed in upper and lower blanking areas on the screen, it is considered that slight artificiality remains on the screen having an aspect ratio of 4:3. FIG. **8**B shows a scheme for reducing the blanking areas by using the vertical and horizontal deflection circuits **906** and **907** to enlarge the whole of image in vertical and horizontal directions. However, there remains a problem that an image is not invisible at the right and left side areas on the screen. FIG. **8**C shows an image which is compressed by decreasing the gradient of the horizontal saw-tooth wave on both right and left side thereof by means of the second deflection current correcting circuit **909** is are enlarged by increasing the gradient of the saw tooth wave on the upper and lower sides thereof by means of the first deflection current correcting circuit **908**. Accordingly, almost all necessary images can be displayed. FIG. **8**D shows the distortion of the displayed image when the display method of FIG. **8**C is adopted. No distortion occurs in the center area (*a*) of the screen and the distortion is largest at the corners (*d*) of the screen. It hardly matters.

The approach of the present embodiment is also effective for the case in which an image is displayed on a screen having an aspect ratio of 16:9. This approach is comparatively more simple in comparison with the enlargement/compression factor variable approach using the above mentioned digital processing and is effective for the analog type displays.

Since the whole of the image can be compressed or enlarged in order to display the image having an aspect ratio of 4:3 on a screen having a ratio of 16:9, an image which

matches the aspect ratio of the screen can be obtained and the image can be displayed on the screen without giving disparity feeling.

Since the image is partially compressed and enlarged, a problem that the image is partially lost by the enlargement of the whole of the image and blanking areas are remained can be solved. An image which matches with the aspect ratio of the screen can be obtained. As a result, sticking problem can be prevented from occurring.

In any cases, the invention can be embodied with a small circuit scale.

What is claimed is:

1. A television receiver capable of enlarging and compressing an image comprising:

a memory having a storage capacity not less than a given value which is controlled with at least a line period;

a clock generator generating a clock having a frequency not less than that of a write clock signal from a writing clock for writing a video signal in said memory and for outputting a read clock for reading said written video signal from said memory;

a vertical enlargement controller generating and outputting a signal for controlling said memory to repeatedly read the same line with a line period depending upon a first preset value when said video signal is read from said memory;

a horizontal enlargement controller generating and outputting a signal for controlling said memory to repeatedly read the same pixel from said memory with a predetermined pixel period depending upon a second preset value when said video signal is read from said memory;

means for combining the output signal from said vertical enlargement controller, the output signal from said horizontal enlargement controller and the read clock from said clock generator and for supplying said memory with a combined signal; to thereby provide a video signal representing an image which is compressed and enlarged in horizontal and vertical directions to a desired size as a video signal read from said memory.

2. A television receiver capable of enlarging and compressing an image as defined in claim **1**, in which said vertical enlargement controller generates and outputs an interpolation coefficient depending upon said first preset value as well as the signal for controlling said memory, said horizontal enlargement controller generates and outputs an interpolation coefficient depending upon said second preset value as well as the signal for controlling said memory, the television receiver further including

a circuit at a stage downstream of said memory, including

a line memory for delaying said video signal read from said memory by one line and outputting it, the operation of said line memory being controlled in accordance with the output signal from said vertical enlargement controller;

vertical interpolator generating and outputting an interpolation signal in accordance with an interpolation coefficient output from said vertical enlargement controller by using said video signal read from said memory and the output signal from said line memory;

means for delaying and outputting the signal and the interpolation coefficient output from said horizontal enlargement controller;

pixel delay means for delaying the output signal from said vertical interpolator, the operation of said pixel delay means being controlled in accordance with the output signal from said means for delaying; and

horizontal interpolator generating and outputting a horizontal interpolation signal in accordance with the interpolation coefficient output from said means for delaying by using output signals from said vertical interpolator and said pixel delay means.

3. A television receiver capable of enlarging and compressing an image as defined in claim **1**, in which said vertical enlargement controller generates and outputs an interpolation coefficient depending upon said first preset value as well as the signal for controlling said memory, said horizontal enlargement controller generates and outputs an interpolation coefficient depending upon said second preset value as well as the signal for controlling said memory, the television receiver further including

a circuit at a stage downstream of said memory, including,

first means for delaying and outputting the signal and the interpolation coefficient output from said horizontal enlargement controller, pixel delay means for delaying by one pixel said video signal read from said memory and for outputting it, the operation of said pixel delay means being controlled in accordance with an output signal from said first means for delaying;

horizontal interpolator generating and outputting an interpolation signal in accordance with the interpolation coefficient output from said first means for delaying by using said video signal read from memory and the output signal from said pixel delay means;

a second means for delaying and outputting the signal and the interpolation coefficient output from said vertical enlargement controller;

a line memory delaying by one line the output signal from said horizontal interpolator, the operation of said line memory being controlled in accordance with the output signal from said second means for delaying; and

a vertical interpolator generating and outputting a vertical interpolation signal in accordance with the interpolation coefficient output from said second means for delaying by using the output signals from said horizontal interpolator and the output signal from said line memory.

4. A television receiver capable of enlarging and compressing an image as defined in claim **1**, in which said vertical enlargement controller generates and outputs an interpolation coefficient depending upon said first preset value as well as the signal for controlling said memory, said receiver further comprising

a line memory delaying said video signal read from said memory by one line and outputting it, the operation of said line memory being controlled in accordance with the output signal from said vertical enlargement controller;

vertical interpolator generating and outputting an interpolation signal in accordance with an interpolation coefficient output from said vertical enlargement controller by using said video signal read from said memory and the output signal from said line memory;

pixel delay means for delaying the output signal from said vertical interpolator;

second horizontal enlargement controller generating and outputting a signal for controlling said pixel delay means at intervals of a pixel period corresponding to said second preset value and for generating and outputting an interpolation coefficient corresponding to said second preset value; and

horizontal interpolator generating and outputting an interpolation signal in accordance with the interpolation coefficient output from said first means for delaying by using output signals from said vertical interpolator and said pixel delay means.

5. A television receiver capable of enlarging and compressing an image according to claim **2**, **3** or **4**, wherein said vertical enlargement controller comprises:

a vertical position generator generating a value in accordance with the vertical position;

value converter consecutively converting the output from said vertical position generator;

a first register;

an adder adding the output from said value converter with the output from said first register to supply the sum to the first register; and

a second register storing a carry output from said adder,

whereby the output of said first register is output as said interpolation coefficient of the vertical enlargement controller and the output of said second register is output as a signal controlling said memory and the line

memory to partially change the magnification rate of said image in a vertical direction.

6. A television receiver capable of enlarging and compressing an image according to claim **2**, **3** or **4**, wherein said horizontal enlargement controller comprises:

a horizontal position generator generating a value in accordance with the horizontal position;

a value converter consecutively converting the count output from said horizontal position;

a first register;

an adder adding the output from said value converter with the output from said first register to supply the sum to said first register; and

a second register storing a carry output from said adder;

whereby the output of said first register is output as said interpolation coefficient of the horizontal enlargement controller and the output of said second register is output as a signal controlling said memory and the pixel delay means to partially change the magnification rate of said image in a horizontal direction.

* * * * *

EXHIBIT C

US006037995A

United States Patent [19]

Ichifuji et al.

[11] **Patent Number: 6,037,995**

[45] **Date of Patent: Mar. 14, 2000**

[54] **BROADCASTING AND COMMUNICATION RECEIVER APPARATUS**

[75] Inventors: **Yasuhisa Ichifuji**, Fujisawa; **Takehito Kishi**, Yokohama; **Naoko Saito**, Tokyo; **Satoru Takashimizu**; **Takanori Eda**, both of Yokohama, all of Japan

[73] Assignee: **Hitachi, Ltd.**, Tokyo, Japan

[21] Appl. No.: **08/844,431**

[22] Filed: **Apr. 18, 1997**

[30] **Foreign Application Priority Data**

Apr. 19, 1996 [JP] Japan 8-097993

[51] **Int. Cl.**[7] **H04N 5/445**

[52] **U.S. Cl.** **348/563**; 348/906; 348/12; 348/13; 348/6; 455/5.1; 455/6.1

[58] **Field of Search** 348/906, 10, 6, 348/7, 13, 12, 563, 564; 455/6.1–6.3, 4.1, 5.1; H04N 7/10, 5/448

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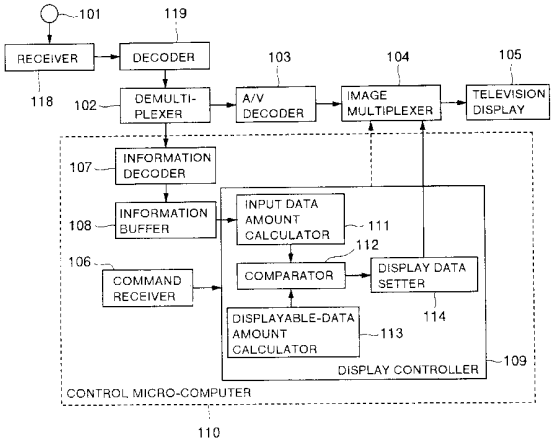
96/07270	3/1996	WIPO .

Primary Examiner—John K. Peng
Assistant Examiner—Linus H. Lo
Attorney, Agent, or Firm—Antonelli, Terry, Stout & Kraus, LLP

[57] **ABSTRACT**

A broadcasting and communication receiver apparatus for displaying program-associated information, in which, in addition to a predetermined display zone, another display zone is provided so that display data of specific information selected by a viewer is wholly displayed and, when the display data is displayed as omitted, a symbol indicative of the information omission is attached to the display data to display the display data within the limited display zone. The apparatus comprises a receiver for receiving the program-associated information including a title, start and end times of a broadcast program together with a video signal and an audio signal, a decoder for decoding the program-associated information, a display unit for displaying the decoded program-associated information thereon, a command receiver for receiving an input signal from a remote controller or from a key or keys provided to the receiver, and a display controller for controlling a display screen on the basis of the input signal.

11 Claims, 7 Drawing Sheets



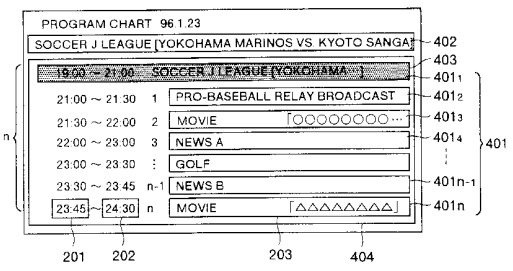


FIG.1

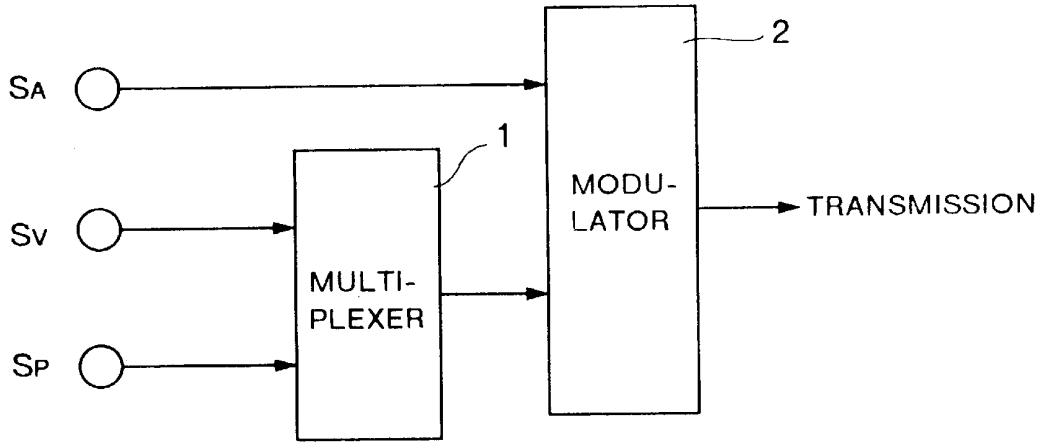

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FIG.2

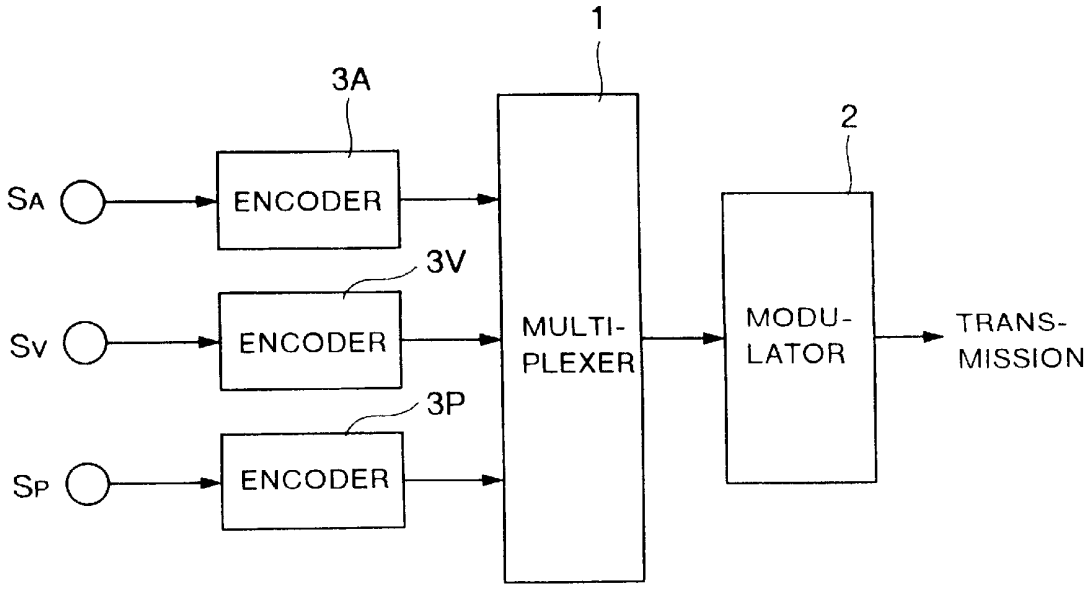
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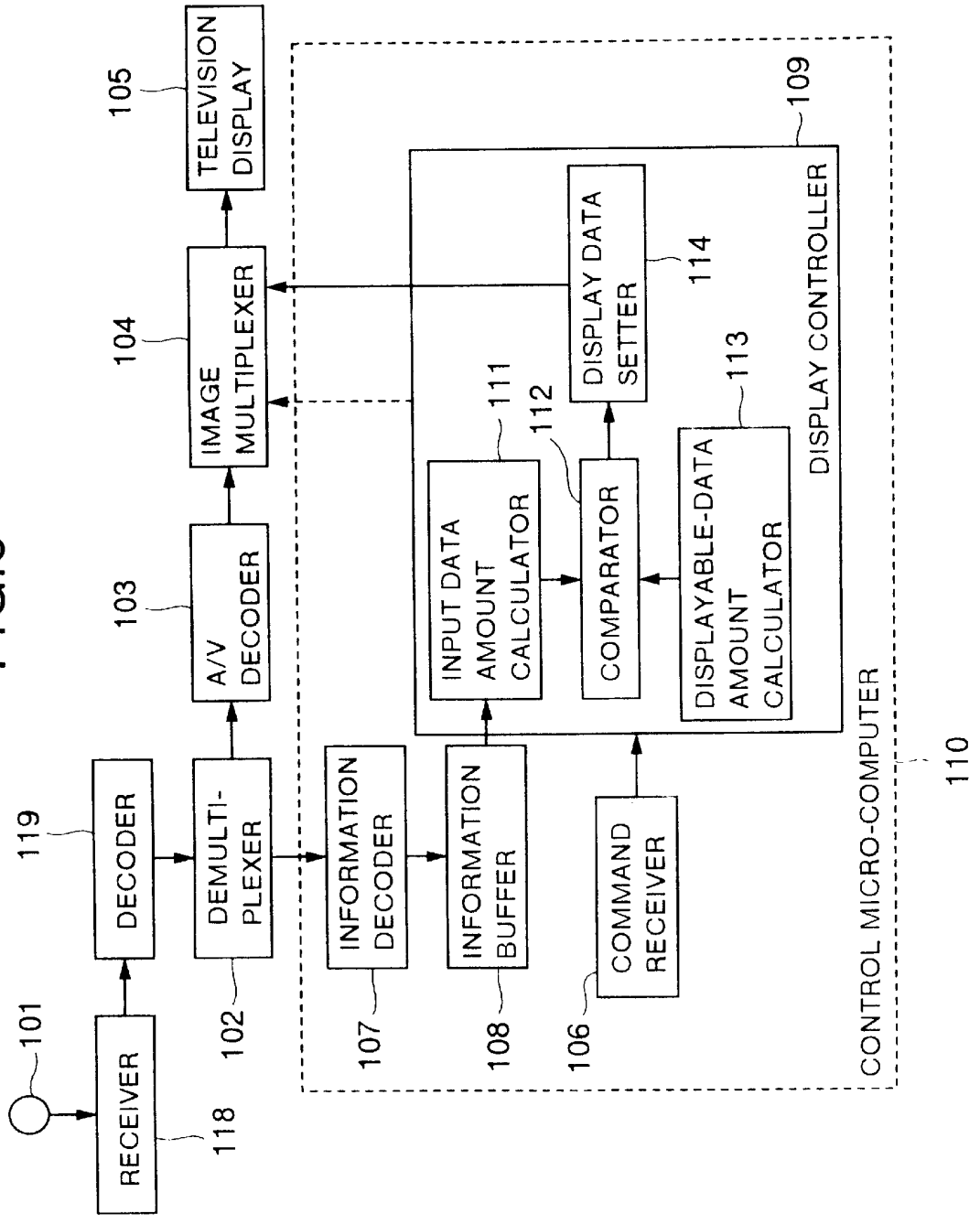
FIG.3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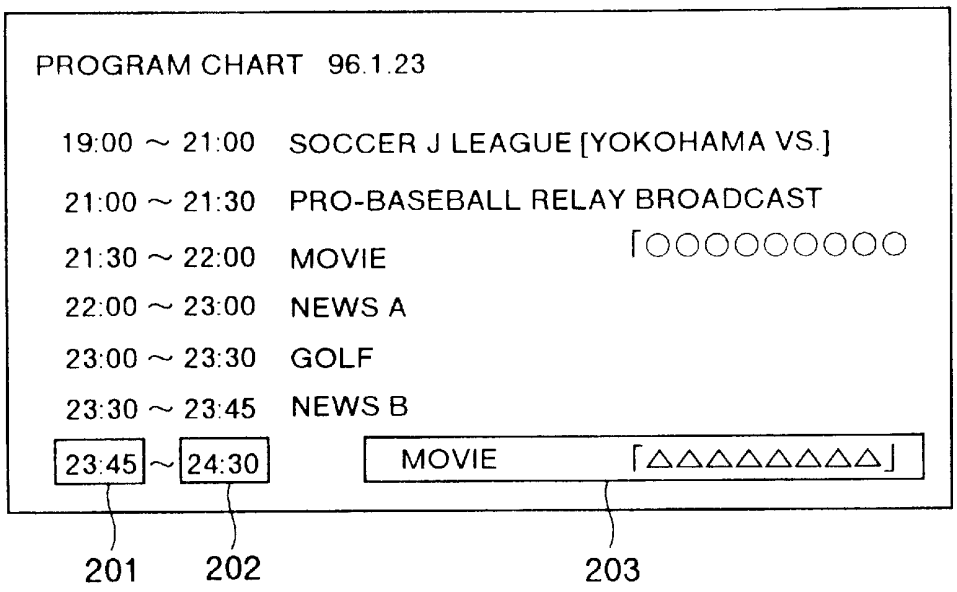
107
INFORMATION DECODER
108
INFORMATION BUFFER
106
COMMAND RECEIVER
109
DISPLAY CONTROLLER
111
INPUT DATA AMOUNT CALCULATOR
112
COMPARATOR
113
DISPLAYABLE-DATA AMOUNT CALCULATOR
114
DISPLAY DATA SETTER
CONTROL MICRO-COMPUTER
110

FIG.4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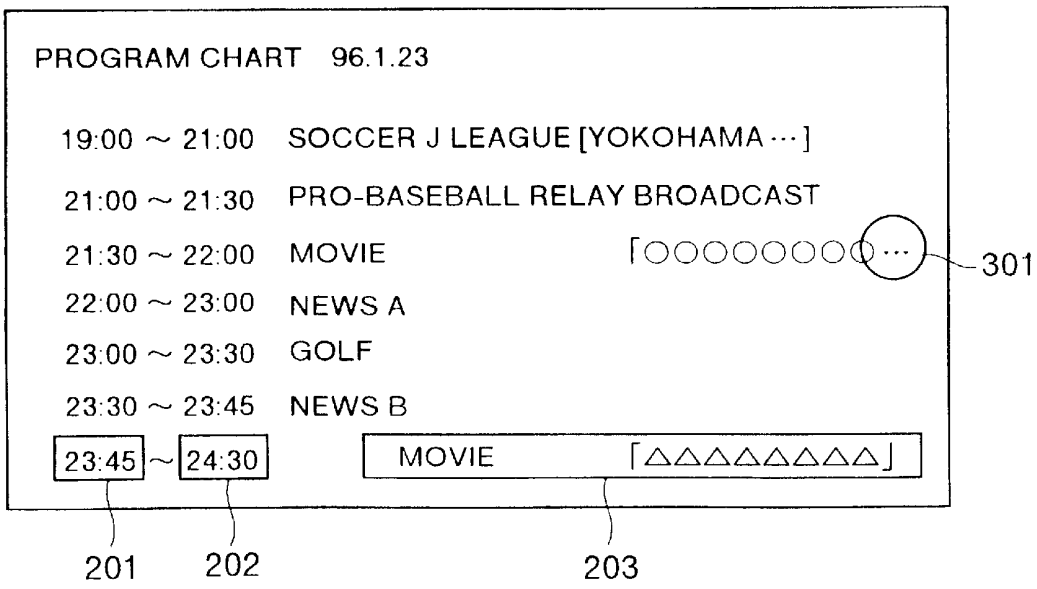
201
202
203

FIG.5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201
202
203

FIG.6

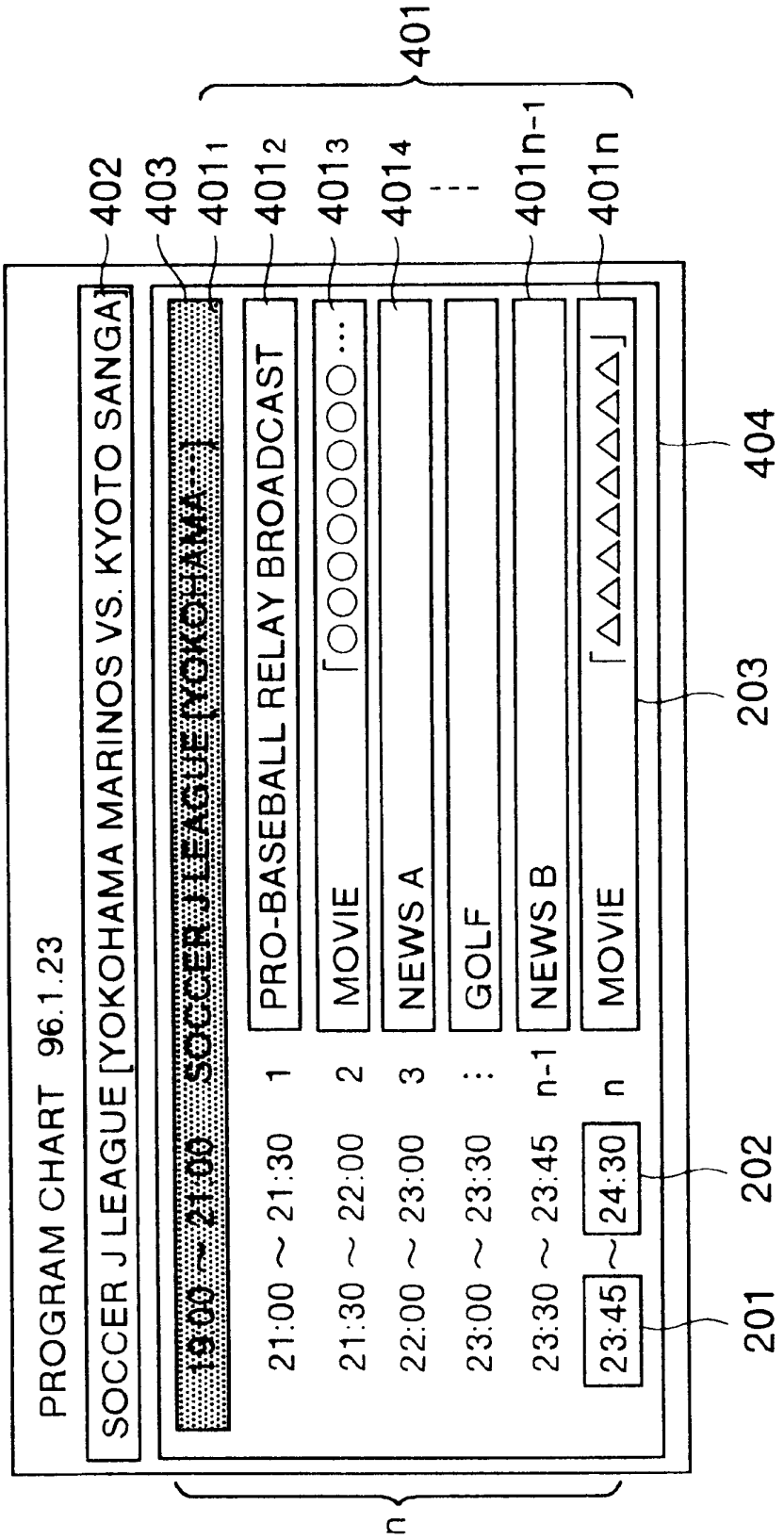

PROGRAM CHART 96.1.23
SOCCER J LEAGUE [YOKOHAMA MARINOS VS. KYOTO SANGA]
19:00 ~ 21:00 SOCCER J LEAGUE [YOKOHAMA ...]
21:00 ~ 21:30 1 PRO-BASEBALL RELAY BROADCAST
21:30 ~ 22:00 2 MOVIE 「○○○○○○○○...
22:00 ~ 23:00 3 NEWS A
23:00 ~ 23:30 : GOLF
23:30 ~ 23:45 n-1 NEWS B
23:45 ~ 24:30 n MOVIE 「△△△△△△△△△」
401
402
403
401 1
401 2
401 3
401 4
401 n-1
401 n
n
201
202
203
404

FIG.7

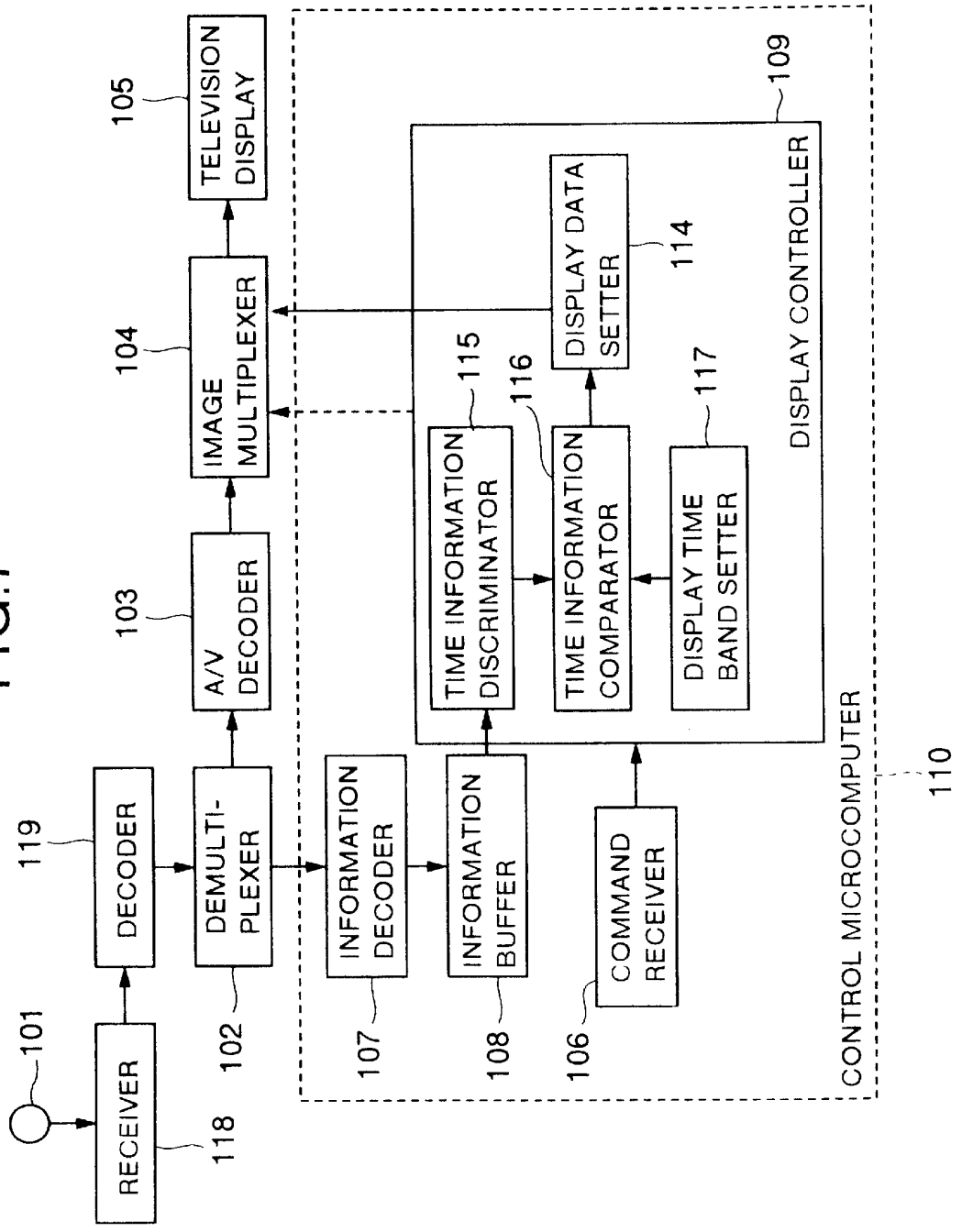

101
RECEIVER
118
102
DEMULTI-PLEXER
119
DECODER
103
A/V DECODER
104
IMAGE MULTIPLEXER
105
TELEVISION DISPLAY
107
INFORMATION DECODER
108
INFORMATION BUFFER
106
COMMAND RECEIVER
109
DISPLAY CONTROLLER
115
TIME INFORMATION DISCRIMINATOR
116
TIME INFORMATION COMPARATOR
117
DISPLAY TIME BAND SETTER
114
DISPLAY DATA SETTER
CONTROL MICROCOMPUTER
110

FIG.8

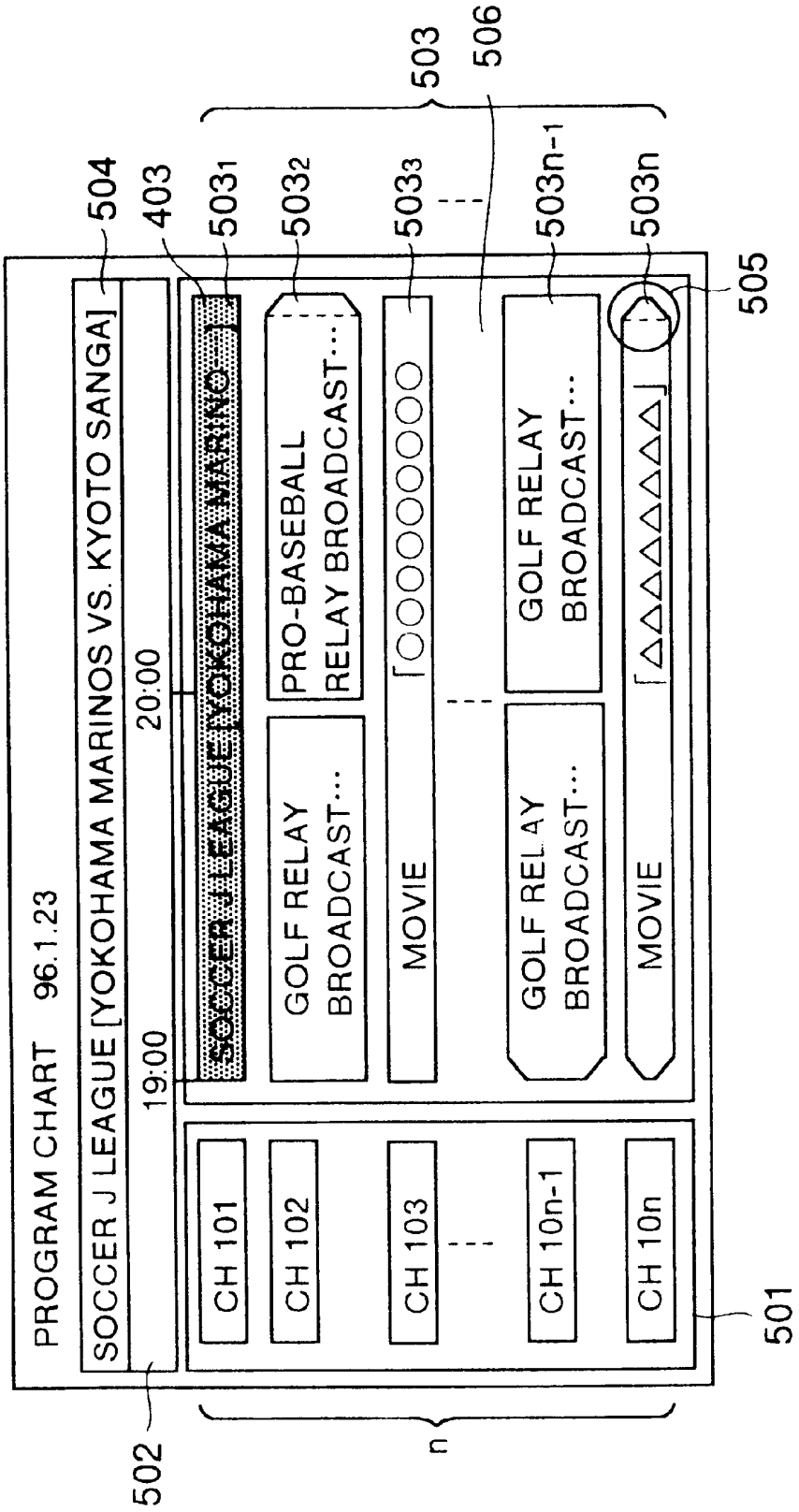
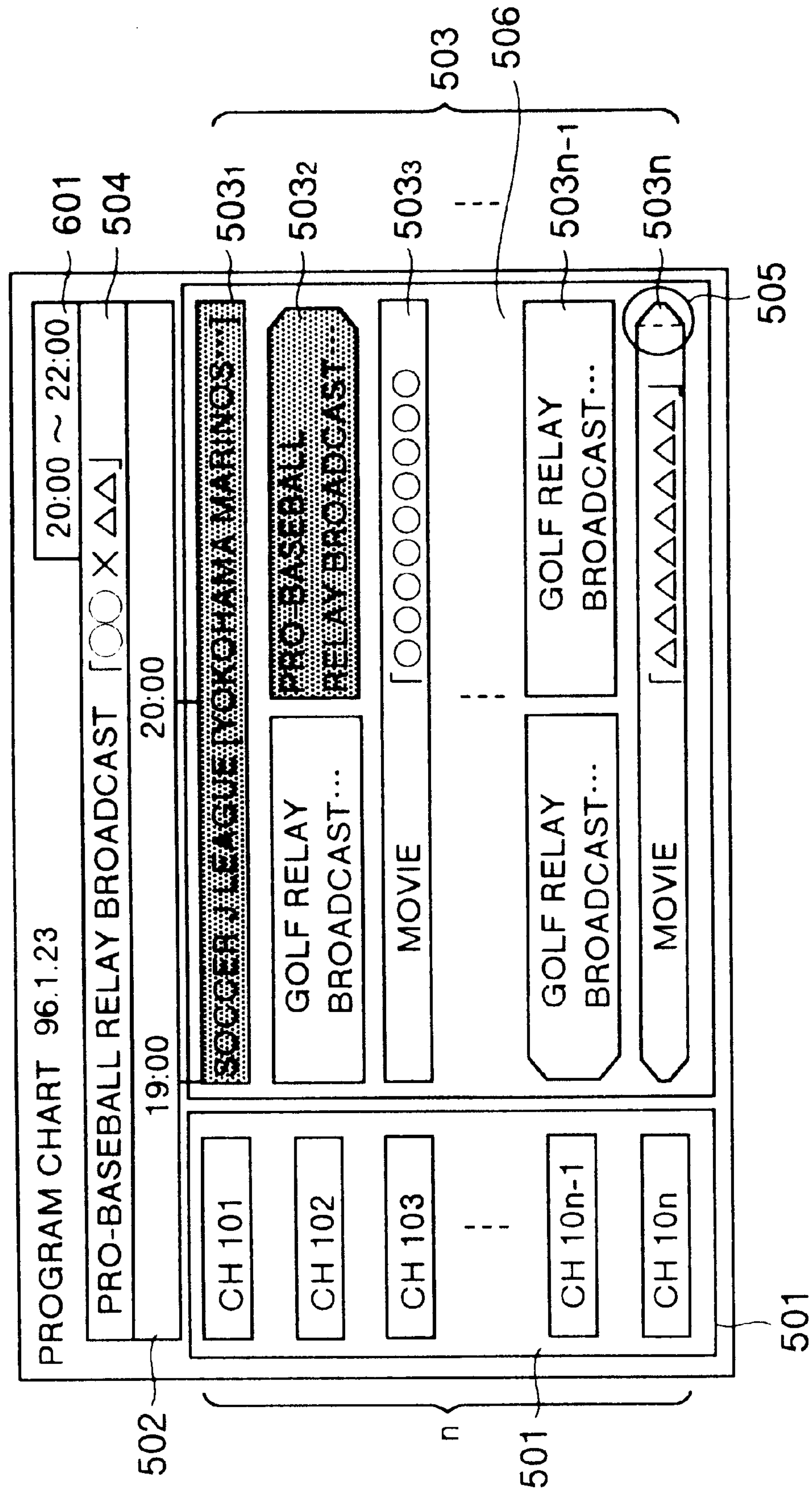

PROGRAM CHART 96.1.23
SOCCER J LEAGUE [YOKOHAMA MARINOS VS. KYOTO SANGA]
19:00
20:00
SOCCER J LEAGUE YOKOHAMA MARINO···
GOLF RELAY BROADCAST···
PRO-BASEBALL RELAY BROADCAST···
MOVIE 「○○○○○○○○○
GOLF RELAY BROADCAST···
GOLF REL AY BROADCAST···
MOVIE 「△△△△△△△△△△
CH 101
CH 102
CH 103
CH 10n-1
CH 10n
501
502
503
503₁
503₂
503₃
503n-1
503n
504
505
506
403
n

FIG.9


PROGRAM CHART 96.1.23
PRO-BASEBALL RELAY BROADCAST 「○○ X △△」
20:00 ~ 22:00
19:00
20:00
SOCCER J LEAGUE 「YOKOHAMA MARINOS・・・」
PRO BASEBALL RELAY BROADCAST・・・
GOLF RELAY BROADCAST・・・
MOVIE
「○○○○○○○○○
GOLF RELAY BROADCAST・・・
GOLF RELAY BROADCAST・・・
MOVIE
「△△△△△△△△△」
CH 101
CH 102
CH 103
CH 10n-1
CH 10n
601
504
503₁
503₂
503₃
503n-1
503n
503
506
505
501
502
n
501

BROADCASTING AND COMMUNICATION RECEIVER APPARATUS

BACKGROUND OF THE INVENTION

The present invention relates to a broadcasting and communication receiver apparatus which receives information about a transmission program together with video and audio data, decodes and displays the program-associated data and more particularly, to a receiver apparatus which can display program-associated information.

In a prior art television signal receiver apparatus, program information such as the title, start and end times of a broadcasting program has not been transmitted together with video and/or audio signal and thus it has been impossible to display these information on a television display screen. For this reason, TV viewers have acquired these information from a program schedule chart run in newspaper.

Further, digital broadcasting has been being started in which digitized signals in place of conventional analog TV signals are transmitted to each home via satellite, cable or land-based broadcasting. Satellite broadcasting has been already realized in such a manner and, even in Japan, plans have been already in the works for start of such service. In the digital broadcasting, various sorts of additional information can be transmitted simultaneously with digitized video and audio signals. When such additional information can be used to prepare a program schedule chart.

Meanwhile, even in the conventional analog broadcasting, when such a system is employed that program-associated information is multiplexed during vertical blanking interval, a program chart similar to that in the digital broadcasting case can be prepared.

FIG. **1** is a block diagram of a multiplex system of an analog broadcasting type, in which S_A denotes an audio signal, S_V a video signal, S_P program-associated information such as a title, start and end times of a broadcasting program. Reference number **1** denotes a multiplexer for multiplexing the video signal S_V and the program-associated information S_P, numeral **2** denotes a modulator for modulating the video signal S_V and the audio signal S_A into broadcasting electromagnetic wave.

In the analog broadcasting system, there is employed a method for multiplexing the program-associated information S_P during the vertical blanking interval. However, the amount of information capable of multiplexing during the vertical blanking interval is small when compared with the amount of information transmittable in the digital broadcasting system. In the analog broadcasting system, further, with respect to its screen displaying function, its screen displaying ability as well as the amount of information to be handled are restricted. Therefore, the display screen implemented based on the analog broadcasting system is inferior in presentation ability to that based on the digital broadcasting system.

FIG. **2** is a block diagram of a multiplex system of a digital broadcasting type, in which reference symbols $\mathbf{3}_A$, $\mathbf{3}_B$ and $\mathbf{3}_P$ denote encoders for encoding the audio and video signals and program-associated information respectively. In the digital broadcasting system, the audio signal S_A, video signal S_V and program-associated information S_P are encoded and compressed respectively by the encoders $\mathbf{3}_A$, $\mathbf{3}_B$ and $\mathbf{3}_P$, and then subjected by the multiplexer **1** to a time division multiplexing operation to obtain a multiplexed signal. The multiplexed signal is modulated by the modulator **2** into broadcasting electromagnetic wave.

The digital broadcasting system is featured in that, since the program-associated information S_P is encoded and compressed by the encoder $\mathbf{3}_P$, more signals can be multiplexed than the program-associated information multiplexable in the analog broadcasting system.

When it is desired to display such program-associated information as program chart on a predetermined display zone of a display screen, e.g., a television display screen, if a display zone necessary for full display of all the display data is larger than the predetermined display zone, then all the display data cannot be fully displayed on the limited display zone. For this reason, there disadvantageously occurs such a situation that part of the originally-displayable information is missing.

SUMMARY OF THE INVENTION

It is therefore a major object of the present invention to display the entire display data on specific information selected by a viewer or to add an information correcting display when the display data is missing to thereby allow the information of the display data to be presented within a limited display zone of a display screen.

Another object of the present invention is to eliminate the need for newspapers and magazines carrying program-associated information.

In accordance with an aspect of the present invention, there is provided a broadcasting and communication receiver apparatus which comprises a receiver means for receiving at least program-associated information including title, start and end times of a broadcast program together with a video signal and a audio signal; a decoder means for decoding the program-associated information from the received signal; a screen display means for processing and displaying the decoded program-associated information on a display screen; a command receiver means for receiving an input signal from a remote controller or from a key or keys provided to a main body of the receiver apparatus; and a display controller means for controlling the display screen based on the input signal.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the present invention will now be described in conjunction with the accompanying drawings, in which;

FIG. **1** is a block diagram of a multiplex system of an analog broadcasting type;

FIG. **2** is a block diagram of a multiplex system of a digital broadcasting type;

FIG. **3** is a block diagram of a broadcasting and communication receiver apparatus in accordance with a first embodiment of the present invention;

FIG. **4** is an example of a display screen for display of program-associated information for explaining the present invention;

FIG. **5** is a first example of the program-associated information display screen in FIG. **3**;

FIG. **6** is a second example of the program-associated information display screen in FIG. **3**;

FIG. **7** is a block diagram of a broadcasting and communication receiver apparatus in accordance with a second embodiment of the present invention;

FIG. **8** is a third example of a display screen for display of program-associated information in FIG. **7**; and

FIG. **9** is a fourth example of the program-associated information display screen in FIG. **7**.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will be explained with reference to the accompanying drawings.

FIG. **3** is a block diagram of a broadcasting and communication receiver apparatus in accordance with an embodiment of the present invention, which includes an input terminal **101** for input of broadcasting and communication signals from an external antenna or the like, a separator or demultiplexer **102** for extracting any one of video and audio signals and program-associated information signal from the received signal, a A/V decoder **103** for decoding the video and audio signals to reproduce original image and original audio, an image multiplexer **104** for multiplexing the video signal and such graphics as characters, a television display **105**, a command receiver **106** for receiving a user input, an information decoder **107** for decoding the transmitted program-associated information, a program-associated information buffer **108** for holding therein the decoded program-associated information, a control micro-computer **110** containing the above elements **106** to **109**, an input data amount calculator **111** for calculating the amount of display data received from the information buffer, displayable-data amount calculator **113** for calculating the number of character rows capable of being displayed on the display screen, a comparator **112** for comparing the amount of input data with the amount of displayable data, a display data setter **114** for setting character rows to be displayed, and a display controller **109** containing the above elements **111** to **114** for controlling the image multiplexer. Further included in the broadcasting and communication receiver apparatus are a receiver **118** for receiving broadcasting and communication signals and a decoder **119** for decoding the received signals.

In FIG. **3**, a signal applied to the input terminal **101** is sent to the demultiplexer **102** through the receiver **118** and decoder **119**. The demultiplexer **102** extracts video and audio signals from the received signal and sends them to the A/V decoder **103**. Similarly, the demultiplexer **102** also extracts program-associated information from the received signal and sends it to the information decoder **107** of the control micro-computer **110**. Program-associated information decoded by the information decoder **107** is sent to the program-associated information buffer **108**.

When a signal indicative of a request of displaying the program-associated information is input to the command receiver **106**, the program-associated information held in the program-associated information buffer **108** is sent to the input data amount calculator **111** of the display controller **109**. The comparator **112** of the display controller **109** compares the number of character rows calculated by the input data amount calculator **111** with the number of displayable character rows calculated by the displayable-data amount calculator **113**, and sends its comparison result and the input data to the display data setter **114** for setting of the display characters. The display controller **109** controls the image multiplexer **104** in such a manner that the image multiplexer **104** multiplexes the display data received from the display data setter **114** and the video signal received from the A/V decoder **103** and displays it on the television display **105**.

When the number of character rows of the input data is larger than the number of displayable character rows, the display data setter **114** sends as display data to the image multiplexer **104** the displayable character rows of the input data with a symbol indicative of omission added to the tail of last one of the character rows thereof.

Shown in FIG. **4** is an example of a display screen for display of program-associated information for explaining the present invention, in which reference numeral **201** denotes a program start time, numeral **202** denotes a program end time, and **203** denotes a program title. In the

example of the program-associated information display screen of FIG. **4**, the start and end times **201** and **202** and title **203** of the program are arranged in a row to express its program broadcasting schedule, but a display zone for displaying the program title **203** is too narrow to display all the program title **203** on the screen until its very end.

In particular, when the system is required to express in Japanese (Kanji), it is necessary to make large the size of Kanji characters for its expression, which results in that the number of character rows displayable within the display zone is decreased and thus all the display data cannot be fully displayed.

FIG. **5** is a first example of the program-associated information display screen in FIG. **3**. In FIG. **5**, numeral **301** denotes an omission symbol indicative of the fact that a tail part of the display data is omitted.

In the case of the program-associated information display screen of FIG. **4**, it is impossible to judge whether the display data such as the program title is fully displayed to its very end or displayable character rows alone of the display data are displayed. In the case of the program-associated information display screen of FIG. **5**, on the other hand, when displayable character rows alone of the display data are displayed, the omission symbol **301** indicative of omission of the tail part of the display data is attached to the last tail of the display character row, whereby a viewer can clearly know it. Although ". . . " has been employed as the omission symbol in the program-associated information data screen of FIG. **5**, another suitable symbol may be used as necessary. Further, contents to be displayed is not limited to such program-associated information as the program start time **201**, program end time **202** and program title **203**, but other information may be allowed.

FIG. **6** shows a second example of the program-associated information display screen in FIG. **3**, in which numeral **401** denotes a first display zone made up of n program display areas $^{401}{}_1$, $\mathbf{401}_2$, . . . , $\mathbf{401}_{n-1}$, and $\mathbf{401}_n$, **402** denotes a second display zone, **403** denotes a cursor for selecting either one of the n program display areas $\mathbf{401}_1$, $\mathbf{401}_2$, . . . , $\mathbf{401}_{n-1}$ in the first display zone, and **404** denotes a display zone in which a plurality (**1**, . . . , and n) of the first display zones **401** are arranged.

Displayed on the first display zone **401** is at least part of display data including program title. Displayed on the second display zone **402** are the same display data including program titles as displayed on the first display zone **401** fully without any omission. The cursor **403**, in response to a user input signal, selects desired one of the n program display areas in the first display zone **401**. In this way, since the operation of the cursor **403** causes the user to arbitrarily select the specific first display zone **401** (for example, **4011**) from the first display zone **401** arranged in the alternative display zone **404**, all the display data including program title required by the user can be fully displayed without any omission.

Since only the display data required by the user are displayed without any omission on the second display zone **402** and display data are displayed with an omission symbol on the first display zone **401**; more first display zones can be displayed within the alternative display zone **404**.

Turning to FIG. **7**, there is shown a block diagram of a broadcasting and communication receiver apparatus in accordance with a second embodiment of the present invention, which includes a time information discriminator **115** for discriminating time information of input data, a display time band setter **117** for setting a time band of a

program chart to be displayed on the display screen, and a time information comparator **116** for comparing the time information of the input data with the time band of the program chart. Other constituent elements are the same as those in FIG. **3**.

When a signal indicative of a request of displaying program-associated information on the display screen is input to the command receiver **106**, the program-associated information hold in the program-associated information buffer **108** is sent therefrom to the time information discriminator **115** of the display controller **109**. The time information comparator **116** of the display controller **109** compares the time information discriminated by the time information discriminator **115** with the display time band set by the display time band setter **117**, and sends its comparison result and the input data to the display data setter **114** where their display format is set. The display controller **109** controls the image multiplexer **104** and composes the display data received from the display data setter and the video signal received from the A/V decoder **103** to display it on the television display **105**.

The above program-associated information display screen has such a display format that uses at least character string in each information field and background, that is, shows such a program chart indicative of program broadcasting schedule that a program start time is given at the left end of each program name field and a program end time is given at the right end of each information field.

When the time information of the input data is judged to be out of a display time band range, the display data setter **114** modifies the shape of the left or right end of the display data and sends it to the image multiplexer **104**. The display data setter **114** modifies the shape of the left or right end of the program name field to clearly indicate that the start or end time of the program is located out of the time band range of the program chart being displayed.

FIG. **8** shows a third example of the program-associated information display screen in FIG. **7**, which includes a channel number column **501**, a time scale column **502**, first program name display column **503** indicative of n-channel program display zones $\mathbf{503}_1$, $\mathbf{503}_2$, . . . $\mathbf{503}_{n-1}$ and $\mathbf{503}_n$, a second program name display column **504**, a continuation display pattern **505** indicative of the fact that a program broadcast start or end time is located out of the program chart being displayed, and a program name alternative column **506** in which a plurality (n=1, . . .) of the first program name display columns **503** are arranged.

In the program display screen, abscissa denotes time, a display start position of the first program name display column **503** in the horizontal direction indicates a broadcast start time, and its horizontal length indicates a program broadcast duration. A measure of time is expressed in the time scale column **502**.

Further, ordinate indicates broadcast channel. Displayed on the channel number column **501** are channel numbers of broadcasting stations, names or logo marks of the broadcasting stations.

The user operates the cursor **403** using a remote controller or a key or keys provided on the main body of the receiver apparatus to select one of the first program name display columns $\mathbf{503}_1$, $\mathbf{503}_2$, . . . and $\mathbf{503}_n$ displayed within the program name alternative column **506**. The selected first program name display column **503** is also displayed in the second program name display column **504**. More specifically, at least part of the program title is displayed on the first program name display column **503**, whereas, all the program title is wholly displayed without any omission on the second program name display column **504**.

The broadcast start time, broadcast duration or broadcast end time of a program is expressed based on a measure of a time displayed in the time scale column **502**. However, when the program broadcast duration is longer than a duration expressible on the program chart screen or when the program broadcast star or end time is located out of the time band expressed in the program chart being displayed, it is impossible to express the program broadcast start or end time within the program chart display screen. For the purpose of expressing that the program broadcasting starts with a time earlier than the time band being displayed or that the program broadcasting ends in a time later than the time band being displayed; the continuation display pattern **505** is used.

By using the continuation display pattern **505**, when the broadcast duration is overlapped as located ahead or behind the time band being displayed, it is possible to express that the broadcast start or end time is out of the time band being displayed.

Shown in FIG. **9** is a fourth example of the program-associated information display screen in FIG. **7**, which includes a third time information display column **601**.

On the program display screen, the third time information display column **601** is provided within the program-associated information display screen to express therein broadcast start and end times of a program. Therefore, when the program broadcast duration is longer than a duration displayable on the program display screen so that the program broadcast start or time cannot be expressed within the time scale column **502** of the program chart screen; it is possible to clearly display the broadcast start and end times, i.e., the time information of the received program-associated information without any omission.

The time information display column **601** may be an independent display zone or may be provided within the second program name display column **504** to be expressed together with the program title.

Although explanation has been made in connection with the program display screen based on the digital broadcasting system in the present embodiment, the present invention is not limited to the specific digital broadcasting system but may be applied to such a broadcasting system that the program-associated information is transmitted as multiplexed to the conventional analog television broadcasting system. Further, the present invention is not restricted to the program chart display screen but may be applied to other general display one.

In accordance with the present invention, there can be provided, when it is desired to display information associated with an item selected condition, a program-associated information display screen of a broadcasting and communication receiver apparatus, on which all display data of the program-associated information received by the receiver apparatus are fully displayed without any omission.

Further, the user can eliminate the need for purchasing newspapers or magazines carrying the program-associated information.

What is claimed is:

1. A broadcasting and communication receiver apparatus comprising:

receiver means for receiving program-associated information including a title, a start time, and an end time of a broadcast program together with a video signal and an audio signal;

decoder means for decoding the program-associated information from the received signal;

display means for displaying the decoded program-associated information on a display screen;

command receiver means for receiving an input signal from a remote controller or from a key or keys provided to a main body of the receiver apparatus; and

display controller means for controlling the display screen based on the input signal;

wherein a first display zone in which a plurality of character strings are displayed is provided in the display screen of the program-associated information; and

wherein the display controller means includes data quantity comparator means for comparing a magnitude of the first display zone with a quantity of display data and, when the display data quantity is judged to be larger than the first display zone, a displayable part of the character string of the display data as well as a symbol indicative of omission and attached to a last tail part of the character string are displayed.

2. A broadcasting and communication receiver apparatus as set forth in claim **1**, wherein, in addition to the first display zone, a second display zone larger in the number of displayable characters than the first display zone is provided; and

wherein the display controller means allows all the display data to be displayed in the second display zone.

3. A broadcasting and communication receiver apparatus as set forth in claim **2**, wherein information displayed in the second display zone is the same as information of a specific first display zone selected based on a user input.

4. A broadcasting and communication receiver apparatus comprising:

receiver means for receiving program-associated information including a title, a start time, and an end time of a broadcast program together with a video signal and an audio signal;

decoder means for decoding the program-associated information from the received signal;

display means for displaying the decoded program-associated information on a display screen;

command receiver means for receiving an input signal from a remote controller or from a key or keys provided to a main body of the receiver apparatus; and

display controller means for controlling the display screen based on the input signal;

wherein the program-associated information display screen having the program-associated information displayed thereon includes at least

a first program name field indicative of a title of a program,

a channel number field indicative of a channel number, and a time scale field indicative of a time being displayed;

wherein each of the first program name field, the channel number field, and the time scale field has a display format that uses at least a character string and a background;

wherein the first program name field, the channel number field, and the time scale field form a program chart indicative of program broadcast schedules;

wherein one end of the first program name field indicates a program start time and another end of the first program name field indicates a program end time; and

wherein the display controller means includes data amount comparator means for comparing a size of the first program name field with an amount of program name data and, when the data amount comparator means judges that the amount of program name data is larger than the size of the first program name field, the display controller means causes a displayable character string of display data as well as a symbol indicative of omission and attached to a last tail part of the character string to be displayed.

5. A broadcasting and communication receiver apparatus as set forth in claim **4**, wherein the program-associated information display screen further includes, in addition to the first program name field, a second program name field larger in the number of displayable characters than the first program name field; and

wherein the display controller means causes all the program name data to be displayed in the second program name field.

6. A broadcasting and communication receiver apparatus as set forth in claim **5**, wherein information displayed in the second program name field is the same as information of a specific first program name field.

7. A broadcasting and communication receiver apparatus as set forth in claim **4**, wherein the display controller means further includes time comparator means for comparing a program broadcast start time and a program broadcast end time to be displayed in the first program name field with a time band to be displayed in the time scale field and, when the time comparator means judges that the program broadcast start time or the program broadcast end time is out of the time band to be displayed in the time scale field, the display controller means changes a shape of a left end or a right end of the background of the first program name field to a continuation display pattern.

8. A broadcasting and communication receiver apparatus as set forth in claim **5**, wherein the program-associated information display screen further includes a time information field for displaying therein time information including a start time and an end time of a selected program.

9. A broadcasting and communication receiver apparatus as set forth in claim **7**, wherein the program-associated information display screen further includes a time information field for displaying therein time information including a start time and an end time of a selected program.

10. A broadcasting and communication receiver apparatus as set forth in claim **8**, wherein the time information field is provided in the second program name field.

11. A broadcasting and communication receiver apparatus as set forth in claim **9**, wherein the time information field is provided as an independent field in the program-associated information display screen.

* * * * *

EXHIBIT D

US006388713B1

(12) **United States Patent**
Saiki et al.

(10) **Patent No.: US 6,388,713 B1**
(45) **Date of Patent: May 14, 2002**

(54) **IMAGE DISPLAY APPARATUS, AND METHOD TO PREVENT OR LIMIT USER ADJUSTMENT OF DISPLAYED IMAGE QUALITY**

(75) Inventors: **Yukimi Saiki**, Tokyo; **Masahisa Tsukahara**, Fujisawa; **Toshimitsu Watanabe**; **Kazuhiko Yoshizawa**, both of Yokohama, all of (JP)

(73) Assignees: **Hitachi, Ltd.**, Tokyo; **Hitachi Video and Information System, Incorporated**, Yokohama, both of (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/114,967**

(22) Filed: **Jul. 14, 1998**

(30) **Foreign Application Priority Data**

Jul. 14, 1997 (JP) 9-188207

(51) **Int. Cl.**[7] **H04N 5/46**; H04N 5/57; H04N 5/58; H04N 17/00

(52) **U.S. Cl.** **348/553**; 348/558; 348/602; 348/603; 348/180; 348/191; 348/564

(58) **Field of Search** 348/180, 189, 348/190, 191, 602, 603, 563, 564, 569, 553, 558, 559, 708, 725, 687

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Primary Examiner—John W. Miller
Assistant Examiner—Paulos Natnael
(74) *Attorney, Agent, or Firm*—Antonelli, Terry, Stout & Kraus, LLP

(57) **ABSTRACT**

A high definition display unit which demodulates, decodes, and processes in relation to chroma and displays a television signal in which a PI (picture) signal and an SI (service information) signal are mixed. A changeover switch **13** connected to an image quality adjusting circuit in a video chroma processing circuit **7** is opened or closed according to an on-off signal S_1, showing the superposed period of both signals detected by a decoder **4**. If the above on-off signal S_1 is on, the changeover switch **13** is opened and the adjustment of image quality is disabled. Therefore, SI display never disappears due to the adjustment of image quality, and the quality of an image can be also adjusted according to an ambient status. Other approaches are also disclosed from preventing image quality adjustment of at least portions of a displayed image containing an information image.

31 Claims, 8 Drawing Sheets

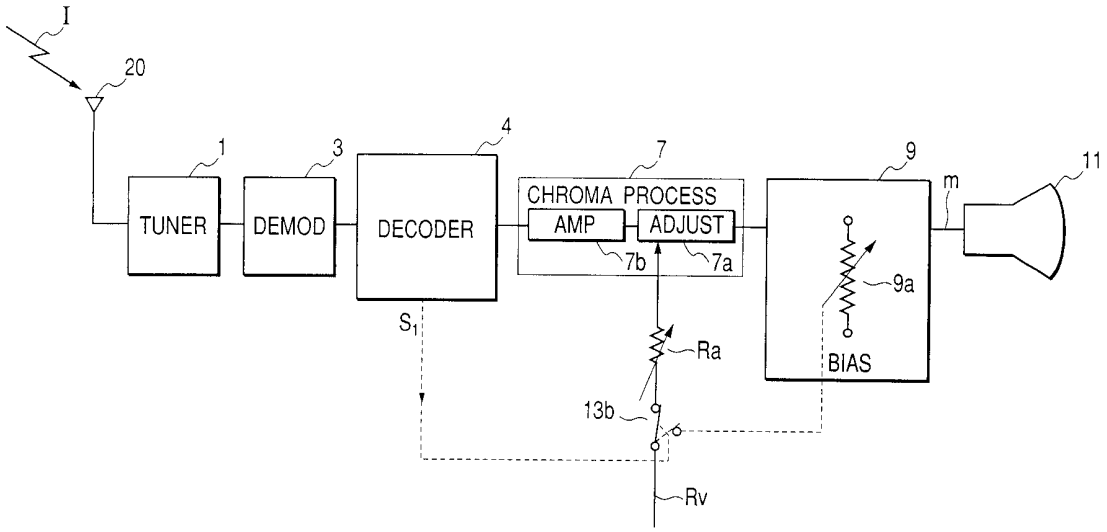

FIG. 1

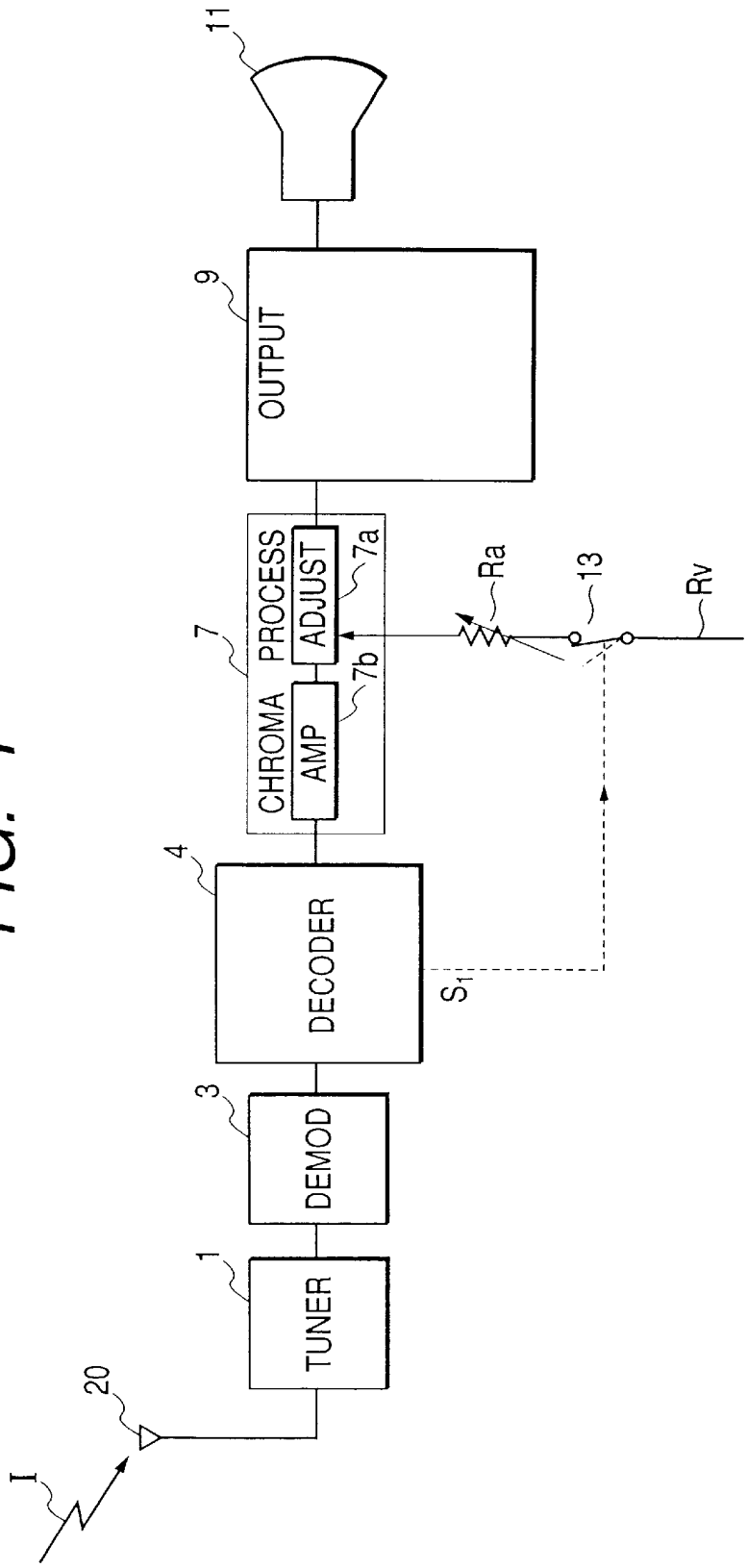
11
9
OUTPUT
7
CHROMA PROCESS
AMP
ADJUST
7a
7b
Ra
13
Rv
4
DECODER
S_1
3
DEMOD
1
TUNER
20
I

FIG. 2

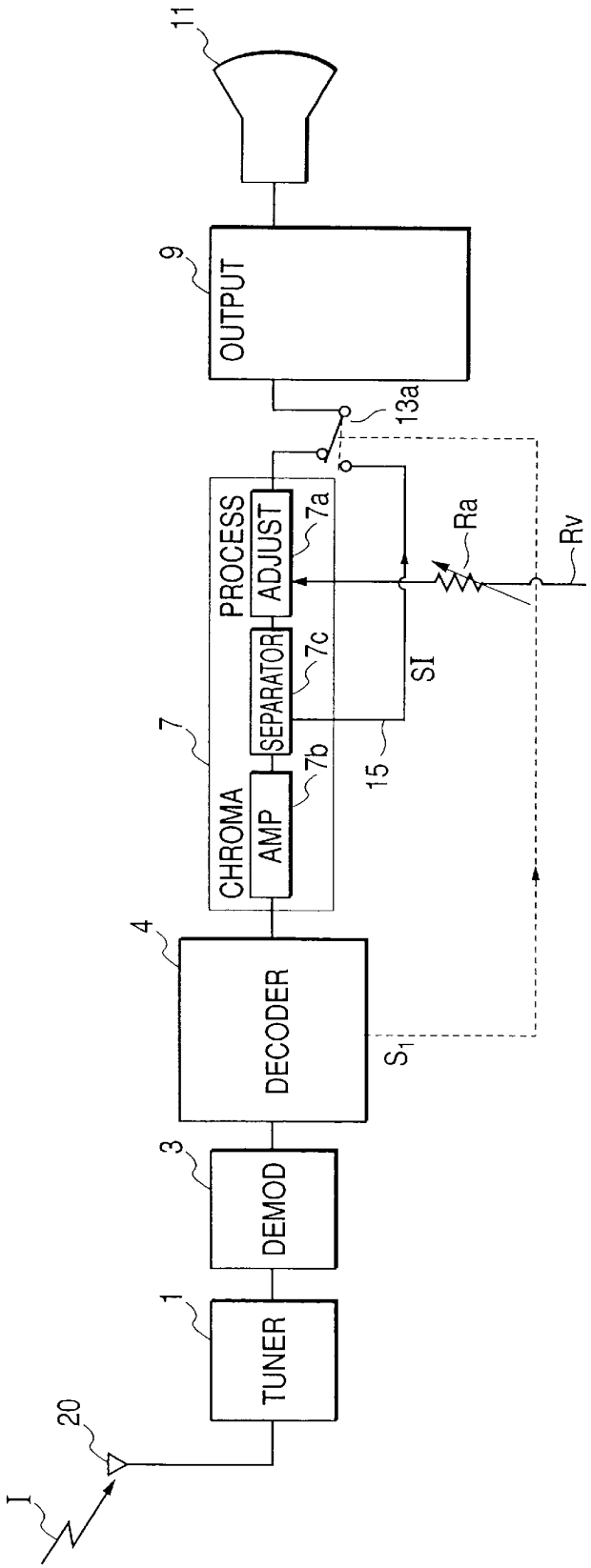
11
9
OUTPUT
13a
PROCESS
ADJUST
7a
SEPARATOR
7c
7
CHROMA
AMP
7b
15
SI
Ra
Rv
4
DECODER
S_1
3
DEMOD
1
TUNER
20
I

FIG. 3

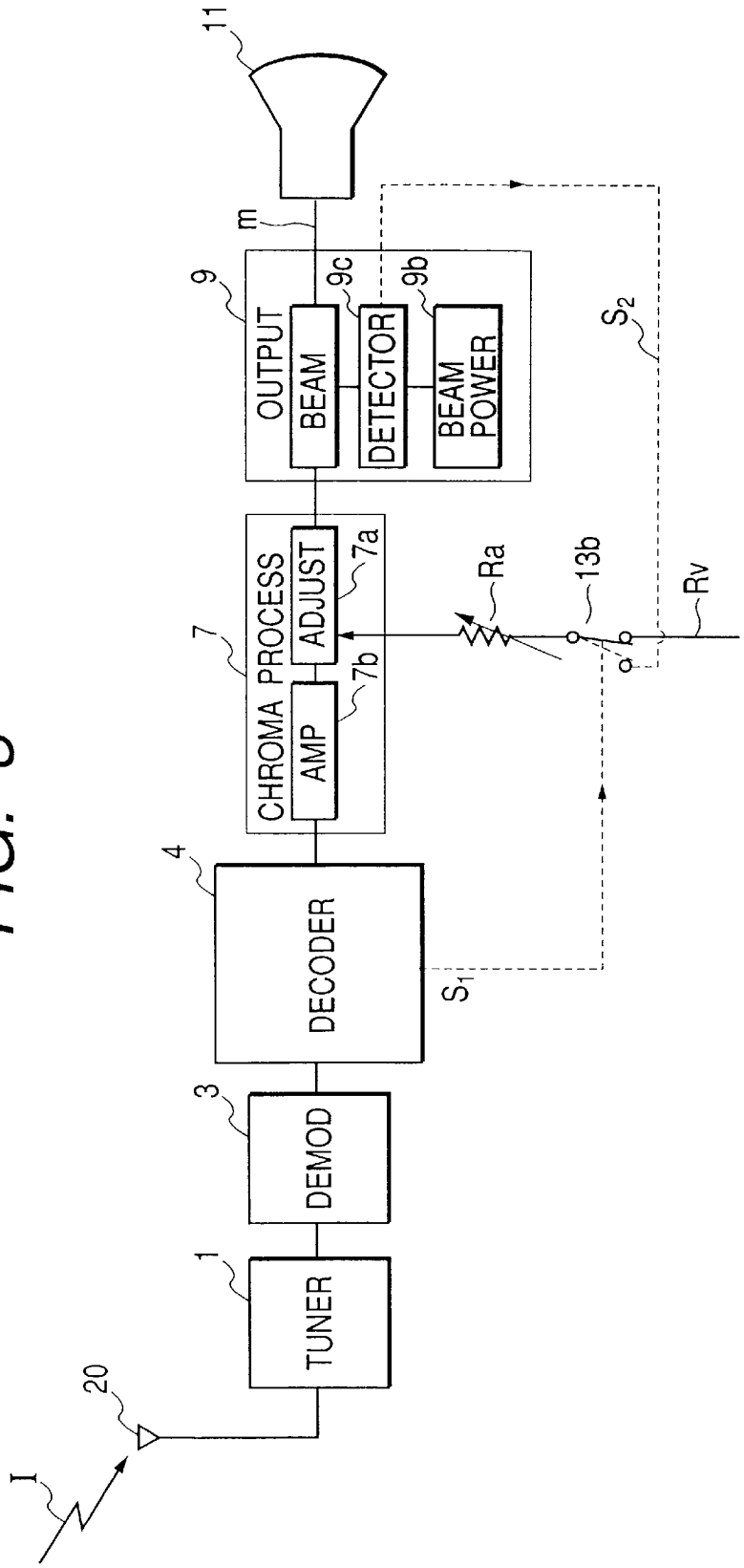
11
m
9
OUTPUT
BEAM
9c
DETECTOR
9b
BEAM POWER
S_2
7
CHROMA PROCESS
ADJUST
7a
AMP
7b
Ra
13b
Rv
4
DECODER
S_1
3
DEMOD
1
TUNER
20
I

FIG. 4

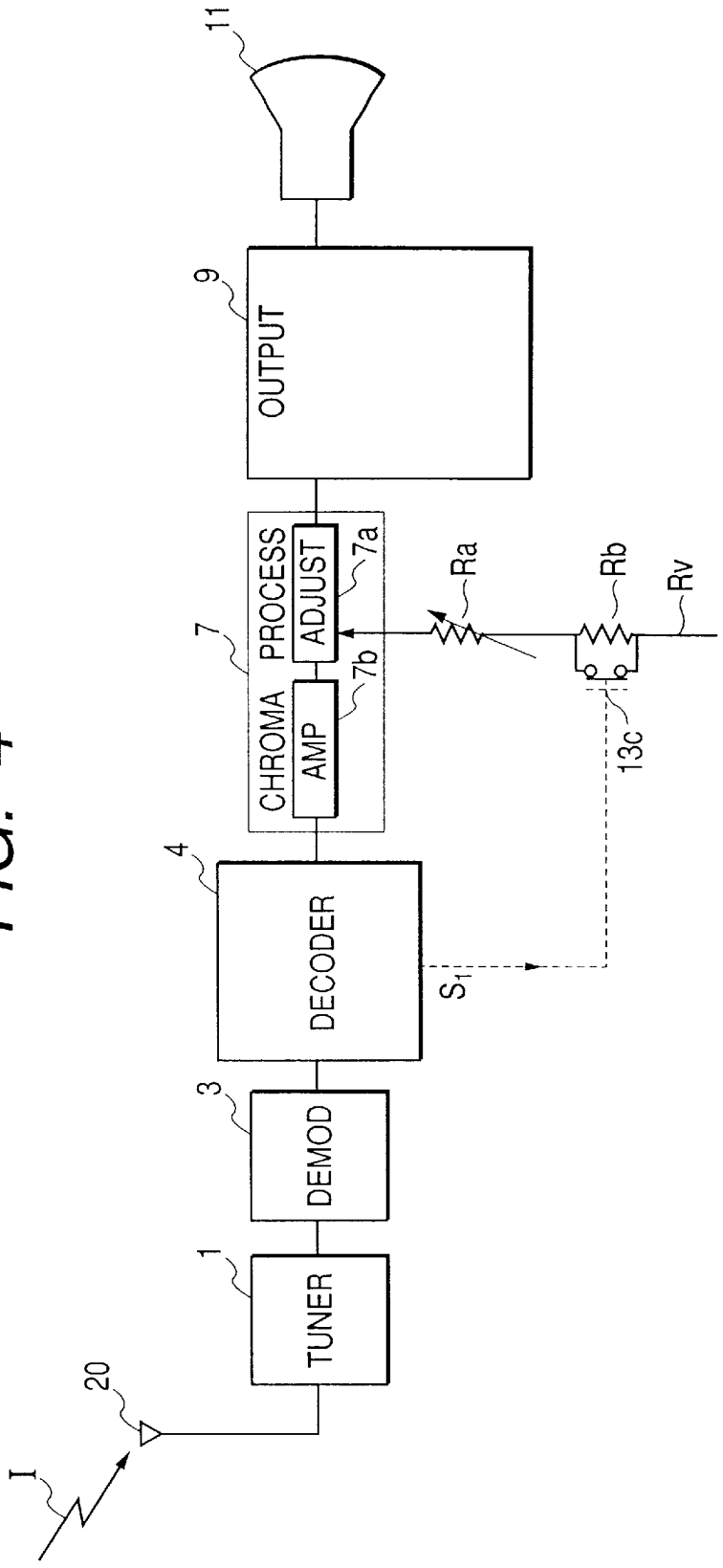
11
9
OUTPUT
7
PROCESS
ADJUST
7a
CHROMA
AMP
7b
Ra
Rb
Rv
13c
4
DECODER
S_1
3
DEMOD
1
TUNER
20
I

FIG. 5

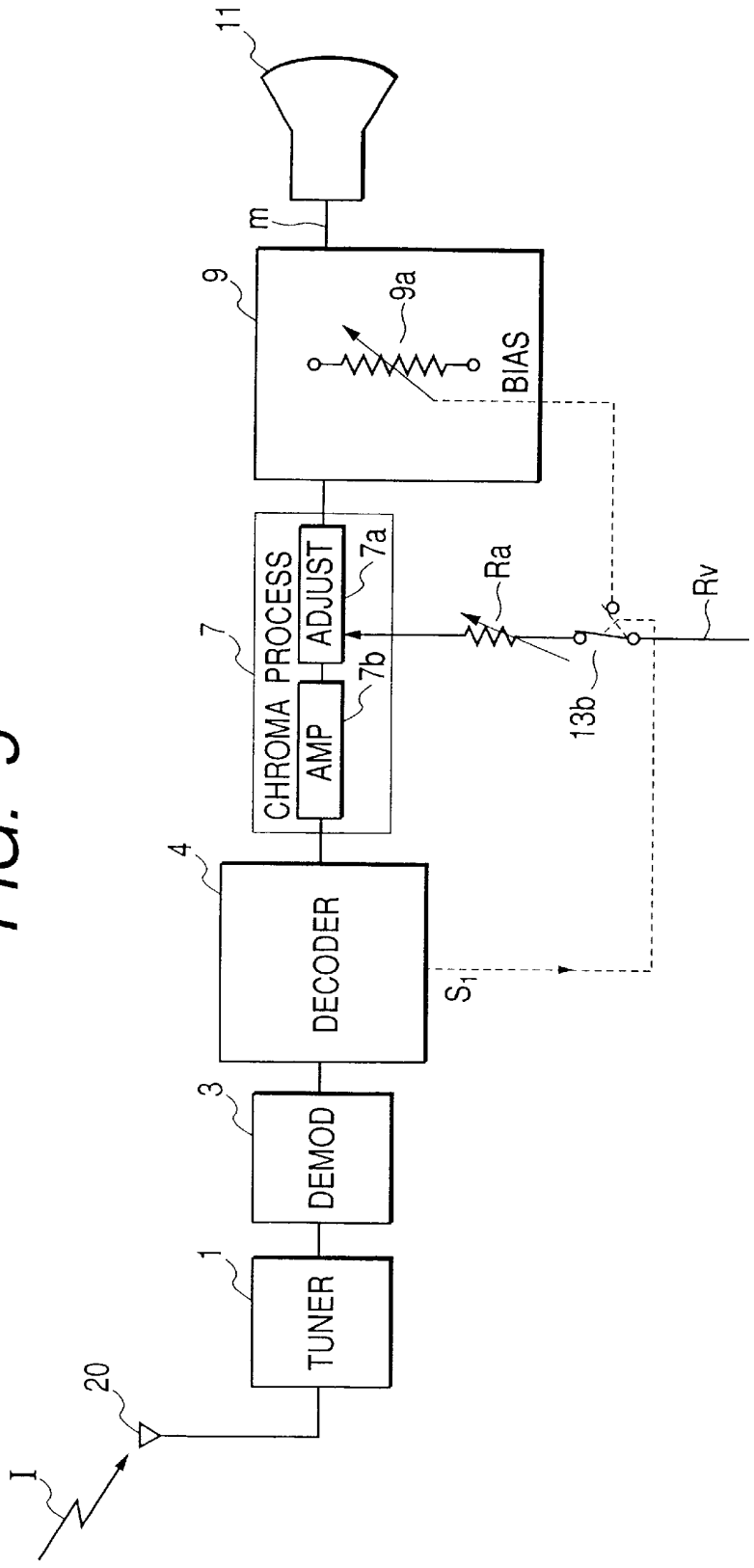
11
m
9
9a
BIAS
CHROMA PROCESS
ADJUST
7a
7
AMP
7b
Ra
Rv
13b
4
DECODER
S_1
3
DEMOD
1
TUNER
20
I

FIG. 6

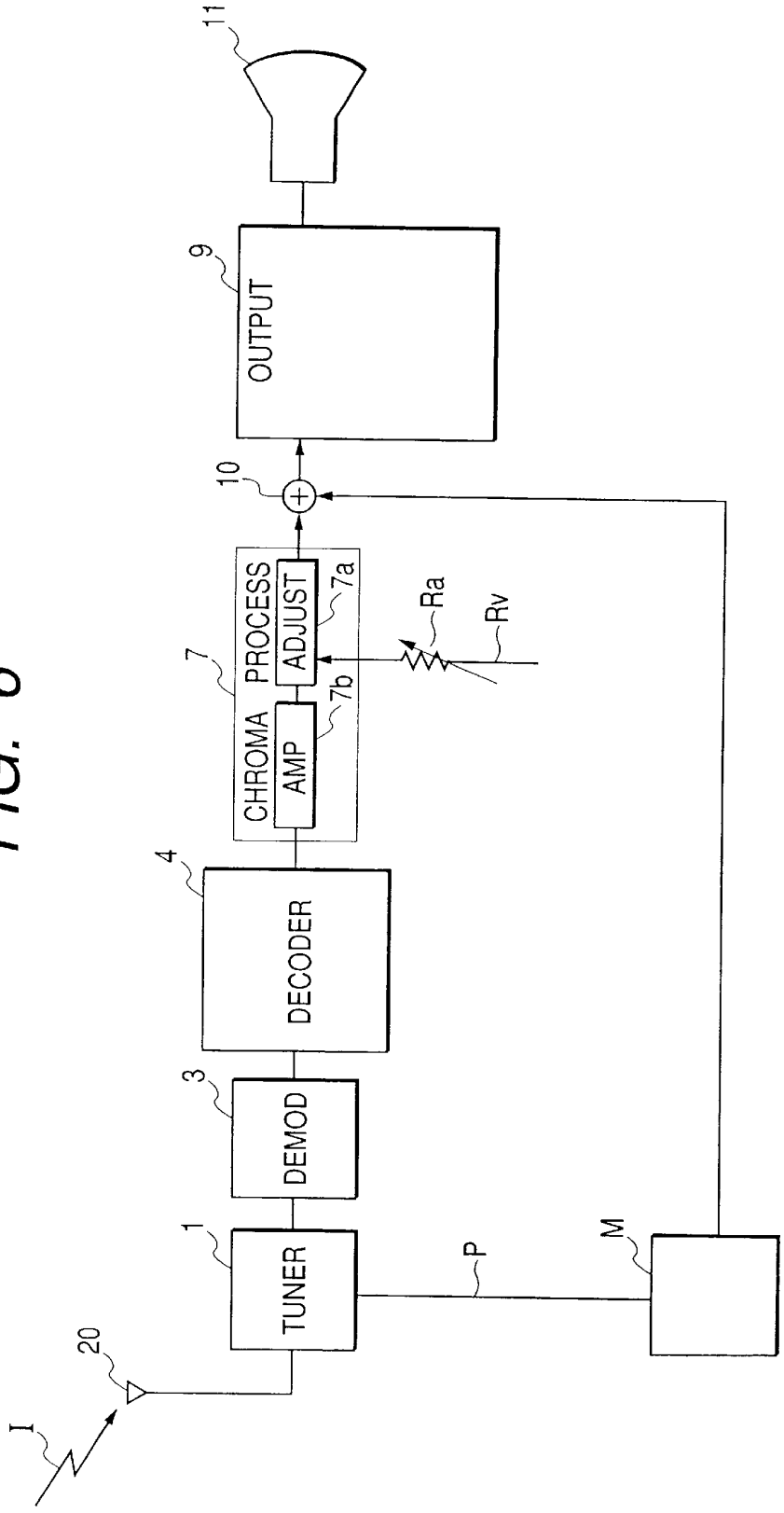
11
9
OUTPUT
10
7
CHROMA PROCESS
AMP
7b
ADJUST
7a
Ra
Rv
4
DECODER
3
DEMOD
1
TUNER
P
M
20
I

FIG. 9

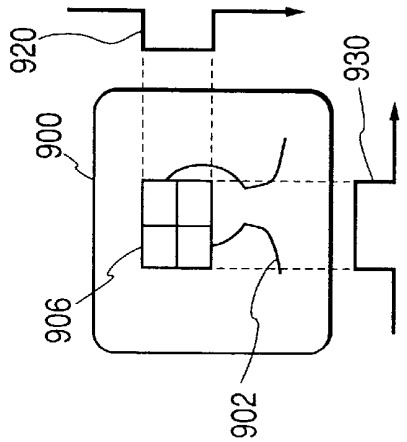

FIG. 7

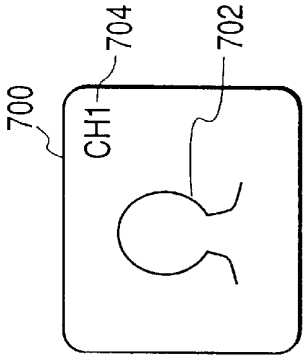

FIG. 8D

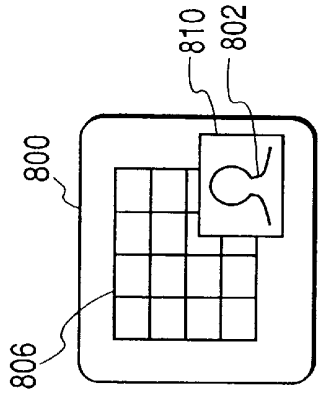

FIG. 8C

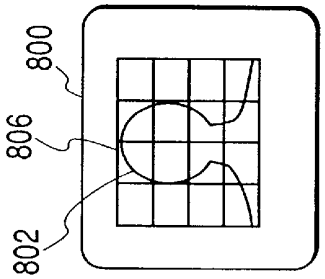

FIG. 8B

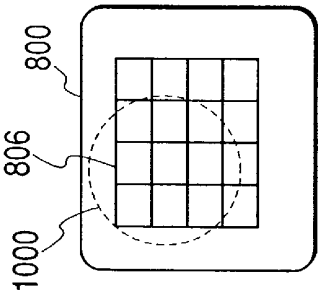

FIG. 8A

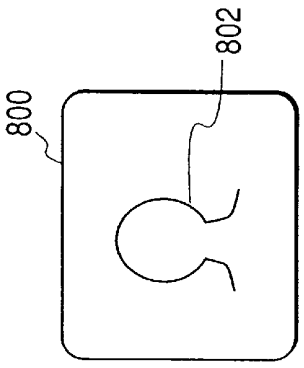

FIG. 11

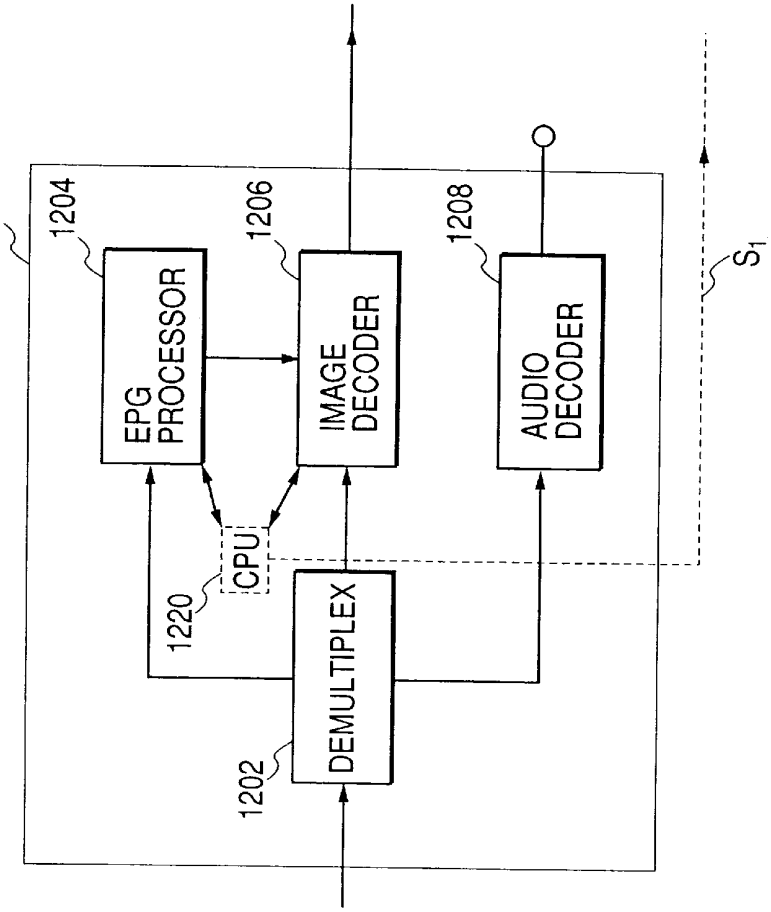
4
1204
EPG PROCESSOR
1206
IMAGE DECODER
1208
AUDIO DECODER
S_1
CPU
1220
DEMULTIPLEX
1202

FIG. 10

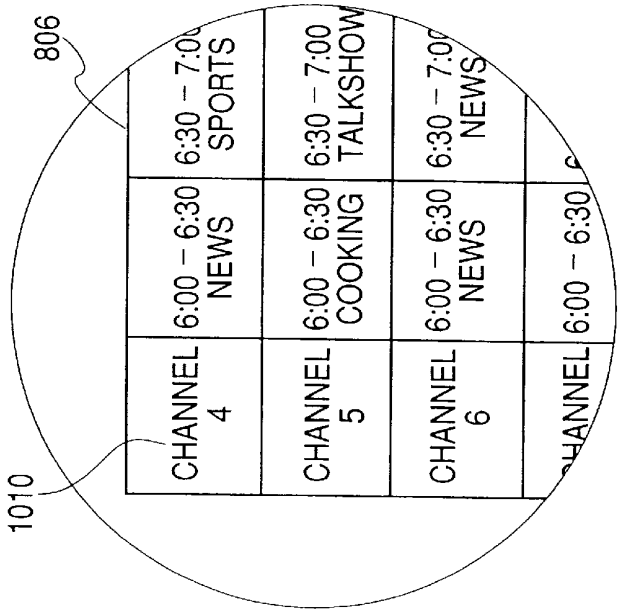
806
6:30 – 7:00 SPORTS
6:30 – 7:00 TALKSHOW
6:30 – 7:00 NEWS
6:00 – 6:30 NEWS
6:00 – 6:30 COOKING
6:00 – 6:30 NEWS
6:00 – 6:30
CHANNEL 4
CHANNEL 5
CHANNEL 6
1010

IMAGE DISPLAY APPARATUS, AND METHOD TO PREVENT OR LIMIT USER ADJUSTMENT OF DISPLAYED IMAGE QUALITY

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to a high definition display unit and method, and more particularly relates to a television receiver having an electronic program guide (EPG) or pay-per-view (PPV) function which is further provided with an arrangement for selectively enabling/disabling image quality adjustment of EPG or PPV menu portions of a display to insure a viewability thereof.

2. Description of Related Art

Referring to FIG. **6**, one type television receiver will be described for background purposes. More particularly, FIG. **6** is a schematic block circuit diagram showing a television receiver arrangement. In FIG. **6**, an analog input signal I including an analog picture signal (hereinafter called a PI signal) corresponding to a television signal, is received by an antenna **20** (or any other appropriate delivery mechanism, e.g., cable, infrared transmission, etc.). Such signal is then input to a demodulating circuit **3** via a tuner I and an IF circuit (not shown), passed through a decoder **5**, and is ultimately processed in a video chroma processing circuit **7**.

In addition, a portion P of information from the input signal is passed from the tuner **1** to a microprocessor M, and image information such as an EPG and/or pay-per-view (PPV) menus, that is, a service information (SI) signal in a form of a digital signal, is generated separately from the above PI signal by the microcomputer M or other separator arrangement. (The microprocessor also provides control signals to ones of the other illustrated components, such control signals not being further illustrated/described for sake of brevity and clarity of illustration/discussion.) Such SI signal is processed, amplified, and transmitted as an on-screen display signal. Therefore, with the FIG. **6** illustrated/described arrangement, a PI signal and an SI signal are demodulated separately.

The above separately demodulated PI signal and SI signal are superposed (e.g., added) with one another by a superposing section **10**, are output to a display **11** via an output device **9**, thus to be displayed. In the FIG. **6** television receiver, a quality of an image is adjusted by an image quality adjusting circuit **7***a*, e.g., within the video chroma processing circuit **7**, using a user-variable adjustment part Ra. More particularly, a user adjusts with a control at a location before superposition by the superposing section **10**, and therefore, the quality of the image and the quality of the image information (e.g., EPG and/or PPV) are completely independent from one another in this background arrangement, i.e., the user-variable adjustment of the display quality of the image does not affect the display quality of the image information owing to the fact that the image information is added to the image after the user-variable adjustment location.

In addition to the FIG. **6** arrangement, there are other methods for displaying an SI signal. For an on-screen circuit for displaying an SI signal, various methods are made practicable, i.e., there are a display character signal inserting circuit method of shunting a color output, and a method of a circuit and others for switching a Y input to a color output to an on-screen RGB and displaying an SI signal. Turning now to problems to be solved by the present invention, as a user cannot control an SI display in a system in which the above display of image information and the adjustment of the quality of an image are completely unrelated, there is a problem that an SI display may be rendered unreadable by luminance adjustment.

As further discussion, superposition of a PI signal and an SI signal in recent digital broadcasting corresponding television, for example, will be described. That is, the above PI signal and SI signal are mixed in a digital compression transmission mode such as in accordance with a Moving Picture Experts Group (MPEG) standard, and the mixed PI and SI signal is simultaneously transmitted or received via the antenna **20**, is decoded by a digital decoder **4**, the tuner **1** and the digital demodulating circuit **3**, is processed by the video chroma processing circuit **7**, is output and displayed. In this mode, the image quality is adjusted according to the above mixed signal by the video chroma processing circuit **7**, i.e., both the PI and SI signal undergo image quality adjustment. There is a problem in this system in that an SI display may disappear or be rendered unreadable by the effect of the image quality adjusting circuit.

As digital broadcasting is tending to be increased in future, it is estimated that the control of SI information resulting in the disappearance of the SI display will be a more and more important problem.

SUMMARY OF THE INVENTION

The present invention is directed toward solving the problems in the above background art. More particularly, the object is to provide a high definition display unit which can prevent or limit a video chroma adjustment circuit from significantly adjusting an image quality of information image portions of a displayed image, such that an information image is never significantly degraded and/or rendered unviewable.

Numerous arrangements are possible for preventing or limiting such adjustment.

More particularly, as one arrangement, a period in which the above both signals (i.e., PI and SI) are superposed is detected, and the image quality adjusting circuit is disabled according to the detection signal. In another arrangement, provided are a section for separating a picture information signal and a bypass circuit with respect to the video chroma processor, a superposed period of the above both signals (PI and SI) is detected, and the bypass circuit is operated according to the detection signal. In yet another arrangement, the superposed period of both signals (PI and SI) is detected and for the superposed period, the image quality adjusting circuit is adjusted according to level or value set according to a detection signal from a detector for detecting a brightness parameter. As a still further embodiment, the superposed period of the above both signals is detected, the image quality adjusting circuit is disabled for the superposed period, and an operating point of an output device is adjusted. Other arrangements are possible as disclosed within the detailed description ahead.

The foregoing and other objects, advantages, manner of operation, novel features and a better understanding of the present invention will become apparent from the following detailed description of the preferred embodiments and claims when read in connection with the accompanying drawings, all forming a part of the disclosure hereof this invention. While the foregoing and following written and illustrated disclosure focuses on disclosing embodiments of the invention which are considered preferred embodiments, it should be clearly understood that the same is by way of illustration and example only and is not to be taken by way

of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

BRIEF DESCRIPTION OF THE DRAWING(S)

The following represents brief descriptions of the drawings, wherein:

FIG. **1** is a schematic block diagram showing a high definition display unit equivalent to an embodiment of the present invention;

FIG. **2** is a schematic block diagram showing a high definition display unit equivalent to an embodiment of the present invention;

FIG. **3** is a schematic block diagram showing a high definition display unit equivalent to an embodiment of the present invention;

FIG. **4** is a schematic block diagram showing a high definition display unit equivalent to an embodiment of the present invention;

FIG. **5** is a schematic block diagram showing a high definition display unit equivalent to an embodiment of the present invention;

FIG. **6** is a schematic block diagram showing a background type television receiver;

FIG. **7** is an illustration of a display containing a picture image and an information image generated internally within an apparatus;

FIGS. **8**A–**8**D are illustrations of a display containing various combinations of a picture image and an information image;

FIG. **9** is an illustration of a display containing a picture image superposed by an information image, and timings related thereto;

FIG. **10** is a magnified illustration of a portion of FIG. **8**B, with respect to an information image; and

FIG. **11** is block diagram illustrating more detailed components of a decoder.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS OF THE INVENTION

Before beginning a detailed description of the subject invention, mention of the following is in order. More particularly, when appropriate, like reference numerals and characters are used to designate identical, corresponding or similar components in differing figure drawings.

As mentioned above, the invention is directed toward avoiding a situation where user adjustment of an image quality (e.g., color density, hue, and/or brightness) of a displayed image renders image (e.g., menu selection) information unviewable. With regard to the image information, the present invention is mainly directed toward improved/guaranteed viewability of image information having its original origin external from the apparatus, such as FIGS. **8**A–**8**Ds' EPG or PPV menu **806** shown in contrast to a picture image **802**. FIG. **7**, on the other hand, is illustrative of image information having its origin within a display apparatus, e.g., internally generated channel image information **704** shown with respect to a picture image **702** within a display **700**.

Turning to more detailed discussion, FIGS. **8**A–**8**D illustrate alternative modes of display possible with displaying picture (i.e., program) images and/or external-origin image (i.e., program menu) information. That is, FIG. **8**A illustrates a display **800** displaying only a picture (i.e., program) image **802**. FIG. **8**B illustrates a display **800** displaying only image (i.e., program menu) information **806** (e.g., an EPG or PPV menu). More particularly, contents within a FIG. **8**B dashed circle **1000** is shown in enlarged form in FIG. **10**, i.e., the image (i.e., program menu) information **806** includes textual image information **1010** such as "CHANNEL 4", "6:00–6:30 NEWS", ETC. FIG. **8**C illustrates a display **800** displaying a picture image **802** and image information overlapped (i.e., superposed). FIG. **8**D illustrates a display **800** displaying a picture-in-picture window **810** (having a picture image **802**) and image information overlapped (i.e., superposed). Accordingly, apparatuses of the present invention are adapted to selectably display at least two of: a picture image without an information image; an information image without a picture image; and, a picture image simultaneously with an information image. That is, the present invention is directed toward preventing user-adjustment of image quality from disadvantageously degrading a viewability of externally-origined image (e.g., program menu) information in any type of display mode, i.e., whether such image information is superposed with a picture image or displayed alone.

Turning now to further detailed description, referring to FIGS. **1** to **5**, each embodiment of the present invention will be described below. More particularly, as an overview, FIG. **1** is a schematic block diagram showing a high definition display unit equivalent to a first embodiment of the present invention, FIG. **2** is a schematic block diagram showing a high definition display unit equivalent to a second embodiment of the present invention, FIG. **3** is a schematic block diagram showing a high definition display unit equivalent to a third embodiment of the present invention, FIG. **4** is a schematic block diagram showing a high definition display unit equivalent to a fourth embodiment of the present invention, and FIG. **5** is a schematic block diagram showing a high definition display unit equivalent to a fifth embodiment of the present invention.

As shown in FIG. **1**, a reference number **1** denotes a tuner, a reference number **3** denotes a digital demodulator, a reference number **4** denotes a digital decoder, a reference number **7** denotes a video chroma processing circuit, a reference number **7***a* denotes an image quality adjusting circuit, a reference number **7***b* denotes an image amplifier, a reference number Ra denotes an adjusting section circuit adjusted by a user (i.e., so as to vary an image quality of a displayed image), a reference number **9** denotes an output circuit, a reference number **13** denotes a circuit changing switch, a reference number **20** denotes an antenna, and a reference number S_1 denotes an on-off (e.g., high-level/low-level) signal indicative of (i.e., corresponding to) superposed/non-superposed periods of a PI signal and an SI signal as detected by an appropriate component, e.g., the digital decoder **4**. The adjusting section circuit, for example, receives a predetermined reference level (e.g., a reference voltage) as indicated by the input arrow Rv, and allows a user (e.g., via a variable resistor) to select a portion of such reference level to be applied to the image quality adjusting circuit **7***a* so as to vary image quality.

As shown in FIG. **1**, an input signal I in which a PI signal and an SI signal (which, for example, have been processed according to discrete cosine transform (DCT), quantized and encoded by a sender) are mixed within an input received by the antenna **20**. As one example of suitable signal transmission/reception, even if a super high frequency (SHF) in the band of 12 GHz is used for a transmission television signal, such can be generally received by a parabolic antenna 20 to 30 cm in diameter. Alternative

acceptable approaches for signal transmission/reception (useable with the present invention) would include cable television (CATV), optical transmission/reception, etc.

A television signal (i.e., channel) of interest is selected from a signal supplied from the antenna **20**, is amplified and the frequency is then converted by the tuner **1**. For the tuner **1**, an electronic tuner for electronically switching a synchronizing frequency using a variable capacity diode of an LC oscillation circuit and a switching diode for switching the level of the LC oscillation circuit, is used.

The synchronization or delay of the above PI signal and SI signal, each frequency of which is converted, is detected by the digital demodulator **3**, and both signals are demodulated with respect to a predetermined transmission digital modulation mode, for example, VSB, ASK, FSK, PSK, QAM, and FDM. In addition, any transmission error caused by a distorting effect from an external device in transmission is also corrected.

As modulated digital signals, both a PI signal and an SI signal are input to the digital decoder **4** in the form of, for example, packet data structure according to an MPEG standard, or any other form such that both can be discriminated. As examples, other types of suitable packet data structures useable with the present invention include: MPEG-2. The digital decoder **4** decodes a PI signal and an SI signal, the frequency of the decoded PI signal is converted for every static signal and every dynamic signal, is converted to an analog signal by a D/A converter (not shown), and is output as signals Y, U, and V (not shown separately).

In the meantime, an SI signal such as an EPG signal is superposed with the PI signal, and is output together therewith. In addition to superposition and outputting, the superposition period of the PI signal and the SI signal is detected by the digital decoder **4** according to a timing and analysis of the packet data structure, and a result of superposed period detection is output to an external device as an on-off signal S_1, e.g., the on-off signal S_1 can be a high-level/low-level signal, with a high-level being indicative of periods of superposition of the PI and SI signals, and with a low-level being indicative of periods of non-superposition of the PI and SI signals.

More particularly, FIG. **11** illustrates one exemplary arrangement of the digital decoder **4**. A demodulated signal from the demodulator **3** is input to the digital decoder, to be demultiplexed within a demultiplexer **1202**. The demultiplexer **1202** demultiplexes the signal into audio data provided to an audio decoder **1208** and then an audio output terminal (not further described within the present disclosure), image data provided to an image decoder **1206**, and EPG data provided to an EPG processor **1204**. The EPG processor **1204** then provides processed EPG data to the image decoder **1206**. The image decoder **1206** decodes the input image data and EPG processed data to generate (in real time), one of a PI signal, an SI signal or a PI signal superposed with an SI signal, and outputs Y, U and V signals.

In addition to the above operations, a central processing unit (CPU) **1220** may be included as an internal component of the digital decoder **4**, but preferably is a CPU external to the decoder and shared in common by several of the FIG. **1** components. The CPU **1220** provides control (e.g., processing, decoding parameters) to the EPG processor **1204** and image decoder **1206** (as well as other circuits), and also receives data (e.g., timing data, etc.) from the EPG processor **1204** and image decoder **1206**. One of the EPG processor **1204**, image decoder **1206** and CPU **1220** generates the on-off signal S_1.

The Y, U and V signals from the digital decoder **4** are input to the video chroma processing circuit **7**. In the video chroma processing circuit **7**, the inputted signals Y, U and V are amplified via amplifier **7***b*, and are ultimately output as signals R, G and B via the image quality adjusting circuit **7***a* composed of a color density adjusting circuit, a hue adjusting circuit, and/or a brightness adjusting circuit, respectively (such circuits not being illustrated individually). A signal from the video chroma processing circuit **7** is further processed (e.g., further amplified) in the output circuit **9**, to be finally delivered to a display **11** such as a cathode ray tube.

The viewing quality of an image is adjusted by adjusting the amplification degree of the color density adjusting circuit, the hue adjusting circuit, and/or the brightness adjusting circuit under user control using the adjusting part Ra. However, in order to avoid a situation where user adjustment can disadvantageously degrade a viewing quality of displayed image information (e.g., a menu, an EPG and/or PPV information), a changeover switch **13** is provided relative to the user control (i.e., adjustment) circuit, and is automatically operated according to the on-off signal S_1 which is indicative of whether or not the PI and SI signals are superposed or not.

After the chroma processing circuit **7**, a color difference signal is converted to a beam current by the output circuit **9**, is delivered to an image receiving circuit via a synchronization/deflection circuit, and an image is thus formed with the display **11**.

The function of the high definition display unit constituted as described above will be described below. More particularly, in the high definition display unit, an on-off signal S_1 indicative of superposed/non-superposed periods of a PI signal and an SI signal is detected under timing control in the digital decoder **4**. As described above, the changeover switch **13** is provided within the user control circuit connected to the image quality adjusting circuit **7***a* in the video chroma processing circuit **7** via an adjustment part Ra. If the above on-off signal S_1 is on (e.g., at a high level) indicating both signals are presently superposed, the above switch **13** is operated on the left side in FIG. **1** (i.e., is opened) such that the user control circuit is disabled to prevent the density of a color, hue and luminance of superposed signals from being controlled by user control. Since user control (i.e., adjustment) of image quality is thus temporarily disabled, image quality is performed at a predetermined level (e.g., preset within the adjustment circuit **7***a*) rather that at a user-adjusted level, so as to guarantee a viewability of the image information (i.e., menu, EPG or PPV). If the above on-off signal S_1 is off (e.g., at a low-level) indicating both signals are not presently superposed, the above switch **13** is operated on the right side in FIG. **1** (i.e., is closed) and the user control arrangement is enabled to allow the density of a color and luminance to be controlled by normal user control.

As described above, if an SI signal exists, user control is disabled. Therefore, since adjustment of image quality by the adjustment is prevented from affecting the image quality of the SI signal, the display of an SI signal on the screen is not disadvantageously affected, i.e., does not become difficult to view and/or disappear altogether. A high definition display unit according to the present invention is not limited to the high definition display unit described in relation to FIG. **1** showing the above first embodiment, i.e., there are many other embodiments and any is included in the tech-

nical concept of the present invention. As non-exhaustive examples, referring to FIGS. **2** to **5**, some of the other embodiments will be described below.

Referring to FIG. **2**, another or second embodiment of a high definition display unit according to the present invention will be described. More particularly, as shown in FIG. **2**, in a high definition display unit, a separator part **7***c* is provided to a front stage of (i.e., before) the image quality adjusting circuit **7***a*, and a PI signal and an SI signal are separated (i.e., further demodulated) in the separation part **7***c*. Further, a changeover switch **13***a* is provided between the video chroma processing circuit **7** and an output circuit **9**, and the bypass circuit **15** of an SI signal is provided between the separation part **7***c* and one terminal of the changeover switch **13***a*.

In the above construction, when an on-off signal S_1 is on (e.g., at a high-level) indicating a superposed period detected in the digital decoder **4** under timing control (note that such on-off signal S_1 can alternatively be detected/generated by other suitable components other than the digital decoder **4**, e.g., by the separator **7***c*), the changeover switch **13***a* is switched to the lower side shown by a dashed line in FIG. **2**, such that the bypass circuit **15** is connected to the output device **9**, and only an SI signal is input to the output device **9** via the bypass circuit **15** and switch **13***a*. Therefore, the SI signal bypasses the adjustment circuit **7***a* so as not to be adjusted thereby, and a display of an SI signal thus is not disadvantageously affected by the adjustment circuit **7***a*, e.g., a menu, EPG or PPV information is never rendered unreadable and/or never disappears.

If the above on-off signal S_1 is off (e.g., at a low-level), the changeover switch **13***a* is switched to the upper side shown by a full line in FIG. **2**, and thus the bypass circuit **15** is disconnected from the output circuit **9** while an output from the adjustment circuit **7***a* is connected, and only a PI signal is input to the output device **9** via the switch **13***a*. Accordingly, while operating in such configuration, the quality of an image can be adjusted under normal user control by adjusting an adjustment part Ra.

FIG. **9** is exemplary of a situation wherein user adjustment is enabled for a major portion of a displayed image, while being disabled for sub-portion of a displayed image, such sub-portion corresponding to an image information portion of the displayed image. More particularly, a display **900** illustrates a picture image **902** being superposed by an information image **906** window. In this embodiment, the user adjustment circuit is normally enabled, unless a predetermined situation is encountered. More particularly, vertical periods **920** and horizontal periods **930** are detected using any well know window period detection method. Such vertical periods **920** and horizontal periods **930** are then used, e.g., via combination with an AND gate, to determine periods when the user adjustment circuit should be disabled. Thus, while the user adjustment circuit is normally enabled during a majority of image display, the user adjustment circuit would be disabled during the information image **906** window.

Referring to FIG. **3**, a further embodiment of a high definition display unit according to the present invention will be described. As shown in FIG. **3**, provided is a detector **9***c* which detects a brightness parameter of a display image signal via an output beam current from a beam power device **9***b* (or some other parameter of the output device), and provides a predetermined detection value S_2 related in level or value to a level or value of the above output beam current m. A changeover switch **13***b* provided within the user adjustment circuit is operated according to an on-off signal S_1 indicative of the superposed/non-superposed periods. If the above on-off signal S_1 is on (e.g., at a high level), the changeover switch **13***b* is switched to the left side shown by a dotted line in FIG. **3**. That is, the switch is selected to a position in which the adjustment part Ra is connected with, and thus adjusted according to, a level of the detection value S_2 as output by the detector **9***c* and related to the above output beam current m. That is, an actual brightness is used in setting an adjustment with the image quality adjusting circuit **7***a*. With such embodiment, an adjustment of a screen according to an ambient status is enabled. Accordingly, since adjustment is limited by and/or takes into account an actual brightness (i.e., via feedback using the S_2 signal), a display of an SI signal thus is not disadvantageously affected (i.e., degraded) by the adjustment circuit **7***a*, e.g., a menu, EPG or PPV information is never rendered unreadable and/or never disappears.

In contrast to the above operation, if the above on-off signal S_1 is off (e.g., at a low level), the changeover switch **13***b* is switched to a selection position shown by a full line in FIG. **3**. That is, is switched to a position in which the adjustment part Ra does not receive the detection value S_2, but instead is connected to allow adjustment solely via user control. More particularly, with such switched configuration the adjustment part Ra for the image quality adjusting circuit **7***a* is adjusted under normal user control.

Referring to FIG. **4**, yet another embodiment of a high definition display unit according to the present invention will be described. That is, as shown in FIG. **4**, an adjustable (resistance) part Ra and a fixed (resistance) part Rb are both provided within a user adjustment circuit, and the adjustment range of the image quality adjusting circuit **7***a* can be selected to any of two different ranges, i.e., one range defined by use of the adjustable (resistance) part Ra solely, and one range defined by use of a series combination of the adjustable (resistance) part Ra and the fixed (resistance) part Rb. As a further construction to facilitate such selection, a short circuiting switch **13***c* is provided with respect to the fixed part Rb, and is operated according to an on-off signal S_1, indicative of the presence/absence of a superposed period.

More particularly, if the above on-off signal S_1, is on (e.g., at a high level, and indicative of superposition), the short-circuiting switch **13***c* is switched to the left side shown by a dashed line in FIG. **4**. That is, is switched to an unconnected (or non-shunting) position, and the adjustment part Ra and the fixed part Rb operate in a series combination. Therefore, the adjustment range of the image quality adjusting circuit **7***a* is limited by the series combination of the adjustment part Ra and the fixed part Rb. With such arrangement, the series combination is chosen such that degradation of superposed information images on a screen by the adjustment of image quality is never caused.

As a contrasting operation, if the above on-off signal S_1, is off (e.g., is at a low level, and indicative of non-superposition), the short circuiting switch **13***c* is switched to the right side shown by a full line in FIG. **4**. That is, is switched to an ON state, to have the fixed part Rb short-circuited such that the image quality adjusting circuit **7***a* is adjusted only by the adjustment part Ra under normal user control.

Referring next to FIG. **5**, another embodiment of a high definition display unit according to the present invention will be described. As shown in FIG. **5**, a changeover switch **13***d* is provided within a user adjustment circuit, the fixed

contact of the changeover switch **13***d* is connected to one terminal of user control, one of switching contacts of the changeover switch **13***d* is connected to the adjustment part Ra, and the other switching contact is connected to a bias circuit **9***a* in an output circuit **9**.

If an on-off signal S_1, is on (i.e., at a high-level) indicative of a superposed period, the changeover switch **13***d* is switched on the right side shown by a dashed line in FIG. **5**, wherein the adjusting resister Ra is disabled, and an operating point of the output device **9** is adjusted by applying a predetermined value (via the switch **13***d*) to a bias circuit **9***a* (within the output device **9**), such that a beam current varies in accordance with the predetermined value, and the whole image (including the PI signal and SI signal) is adjusted. Therefore, with the FIG. **5** embodiment, the display of SI information is never disadvantageously affected or erased by the adjustment of image quality, and the adjustment of a screen according to an ambient status is also enabled.

If, with the FIG. **5** arrangement, the on-off signal S_1 is off (i.e., at a low-level), the changeover switch is switched to the right side shown by a full line in FIG. **5** and the image quality adjusting circuit **7***a* in the video chroma processing circuit **7** is enabled to allow adjusting of the adjustment part Ra and thus image appearance/quality, under normal user control.

The operating point of the output device **9** may also be adjusted using a self-holding mechanism not shown according to an on-off signal S_1 showing a superposed period.

As described in detail above, according to the present invention, if a PI signal and an SI signal are superposed, a high definition display unit which enables controlling (i.e., image appearance/quality adjustment) of an SI signal independent of a PI signal, e.g., according to an ambient status. Thus, a high definition receive arrangement and method can be provided.

This concludes the description of the preferred embodiments. Although the present invention has been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the spirit and scope of the principles of this invention. More particularly, reasonable variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the foregoing disclosure, the drawings and the appended claims without departing from the spirit of the invention. In addition to variations and modifications in the component parts and/or arrangements, uses with alternative components will also be apparent to those skilled in the art.

What is claimed is:

1. An image display apparatus comprising:

a display circuit adapted to selectably display at least two of: a picture image without an information image; said information image without said picture image; and said picture image simultaneously with said information image;

a detector which detects a portion of said displayed image containing said information image and outputs a control signal according to said detected portion;

a user adjustment control circuit allowing user adjustment of an image quality of a displayed image; and

an enabler/disabler adapted to selectively prevent said user adjustment control circuit from adjusting at least said portions of said displayed image containing said information image based on said control signal.

2. An image display apparatus as claimed in claim **1**, wherein said enabler/disabler more specifically disables operation of said user adjustment control circuit to prevent said user adjustment control circuit from adjusting said at least portions of said displayed image containing said information image.

3. An image display apparatus as claimed in claim **1**, wherein said enabler/disabler more specifically bypasses signals of said at least portions of said displayed image containing said information image to prevent said user adjustment control circuit from adjusting said at least portions of said displayed image containing said information image.

4. An image display apparatus as claimed in claim **1**, wherein said enabler/disabler more specifically is adapted to limit an operation of said user adjustment control circuit to a predetermined adjustment range during said at least portions of said displayed image containing said information image, which predetermined adjustment range does not significantly degrade viewability of said information image.

5. An image display apparatus as claimed in claim **1**, wherein said enabler/disabler more specifically utilizes a detected operating parameter of said image display apparatus to select an adjustment range of said user adjustment control circuit during said at least portions of said displayed image containing said information image, which adjustment range does not significantly degrade viewability of said information image.

6. An image display apparatus as claimed in claim **1**, wherein said information image is at least one of an electronic program guide (EPG) and a pay-per-view (PPV) selection menu, and said enabler/disabler is more specifically adapted to selectively prevent said user adjustment control circuit from adjusting at least portions of said displayed image containing said selection menu.

7. An image display apparatus as claimed in claim **1**, wherein said information image is more specifically obtained from at least one of a digital, analog, and a combined analog/digital television signal containing a service information signal.

8. An image display apparatus comprising:

a display means for selectably displaying at least two of: a picture image without an information image; said information image without said picture image; and said picture image simultaneously with said information image;

a detection means for detecting a portion of said displayed image containing said information image and outputting a control signal according to said detected portion;

a user adjustment control means for allowing user adjustment of an image quality of a displayed image; and

an enabler/disabler means for selectively preventing said user adjustment control means from adjusting at least said portions of said displayed image containing said information image based on said control signal.

9. An image display apparatus as claimed in claim **8**, wherein said enabler/disabler means is more specifically for disabling operation of said user adjustment control means to prevent said user adjustment control means from adjusting said at least portions of said displayed image containing said information image.

10. An image display apparatus as claimed in claim **8**, wherein said enabler/disabler means is more specifically for bypassing signals of said at least portions of said displayed image containing said information image, to prevent said user adjustment control means from adjusting said at least portions of said displayed image containing said information image.

11. An image display apparatus as claimed in claim 8, wherein said enabler/disabler means is more specifically for limiting an operation of said user adjustment control means to a predetermined adjustment range during said at least portions of said displayed image containing said information image, which predetermined adjustment range does not significantly degrade viewability of said information image.

12. An image display apparatus as claimed in claim 8, wherein said enabler/disabler means is more specifically for utilizing a detected operating parameter of said image display apparatus to select an adjustment range of said user adjustment control means during said at least portions of said displayed image containing said information image, which adjustment range does not significantly degrade viewability of said information image.

13. An image display apparatus as claimed in claim 8, wherein said information image is at least one of an electronic program guide (EPG) and a pay-per-view (PPV) selection menu, and said enabler/disabler means is more specifically for selectively preventing said user adjustment control means from adjusting at least portions of said displayed image containing said selection menu.

14. An image display apparatus as claimed in claim 8, wherein said information image is more specifically obtained from at least one of a digital, analog, and a combined analog/digital television signal containing a service information signal.

15. An image display method comprising the steps of:

providing a display circuit adapted to selectably display at least two of: a picture image without an information image; said information image without said picture image; and said picture image simultaneously with said information image;

detecting a portion of said displayed image containing said information image;

outputting a control signal according to said detected portion;

allowing, via a user adjustment control circuit, user adjustment of an image quality of a displayed image; and

selectively preventing said user adjustment control circuit from adjusting at least said portions of said displayed image containing said information image based on said control signal.

16. An image display method as claimed in claim 15, wherein said preventing step more specifically disables operation of said user adjustment control circuit to prevent said user adjustment control circuit from adjusting said at least portions of said displayed image containing said information image.

17. An image display method as claimed in claim 15, wherein said preventing step more specifically bypasses signals of said at least portions of said displayed image containing said information image to prevent said user adjustment control circuit from adjusting said at least portions of said displayed image containing said information image.

18. An image display method as claimed in claim 15, wherein said preventing step more specifically limits an operation of said user adjustment control circuit to a predetermined adjustment range during said at least portions of said displayed image containing said information image, which predetermined adjustment range does not significantly degrade viewability of said information image.

19. An image display method as claimed in claim 15, wherein said preventing step more specifically utilizes a detected operating parameter of said image display to select an adjustment range of said user adjustment control circuit during said at least portions of said displayed image containing said information image, which adjustment range does not significantly degrade viewability of said information image.

20. An image display method as claimed in claim 15, wherein said information image is at least one of an electronic program guide (EPG) and a pay-per-view (PPV) selection menu, and said preventing step is more specifically for selectively preventing said user adjustment control circuit from adjusting at least portions of said displayed image containing said selection menu.

21. An image display method as claimed in claim 15, wherein said information image is more specifically obtained from at least one of a digital, analog, and a combined analog/digital television signal containing a service information signal.

22. A high definition display unit, comprising:

a tuner for inputting a television signal having both an information signal and a picture signal;

a digital demodulator for demodulating an output of said tuner;

a digital decoder for decoding an output of said digital demodulator and outputting an analog signal including an information image superposed on a picture image;

a video chroma processor for receiving said analog signal, and having an image quality adjusting circuit;

an output device for outputting a display signal based upon an output from said video chroma processor;

a display for displaying an image according to said display signal; and

a detector for detecting a period of said superposed information signal and picture signal, wherein:

said image quality adjusting circuit is disabled according to said display signal so said information signal is not degraded by image quality adjustment.

23. A high definition display unit, comprising:

a tuner for inputting a mixed television signal in which a picture information signal is superposed on a picture image signal;

a digital demodulator for demodulating an output of said tuner;

a digital decoder for decoding an output of said digital demodulator and outputting it as an analog signal;

a video chroma processor for receiving said analog signal, and having an analog output processing circuit and an image quality adjusting circuit to produce a video chroma processing signal;

an output device for outputting a display signal based upon said video chroma processing signal;

a display for displaying an image according to said display signal;

a section for separating said picture information signal and a bypass circuit of said separated picture information signal are provided to said video chroma processor; and

a detector for detecting a period of said superposed picture information image and picture image signal, and outputting a control signal according to said detected period, wherein:

said bypass circuit is operated according to said control signal so said picture information signal is not degraded by an image quality adjustment.

24. A high definition display unit, comprising:

a tuner for inputting a mixed television signal in which a picture information signal is superposed on a picture image signal;

a digital demodulator for demodulating an output of said tuner;

a digital decoder for decoding an output of said digital demodulator and outputting it as an analog signal;

a video chroma processor for receiving said analog signal, and having an analog output processing circuit and an image quality adjusting circuit for generating a video chroma processing signal;

an output device for outputting a display signal based upon said video chroma processing signal;

a display for displaying an image according to said display signal; and

a detector for detecting a brightness of said image and outputting a signal based on the brightness detected, wherein:

said digital decoder detects a period of said superposed picture information signal and picture image signal; and

for said detected period, said image quality adjusting circuit is operated according to said signal from said detector for detecting said brightness so said picture information signal is not degraded by an image quality adjustment.

25. A high definition display unit, comprising:

a tuner for inputting a mixed television signal in which a picture information signal is superposed on a picture image signal;

a digital demodulator for demodulating an output of said tuner;

a digital decoder for decoding an output of said digital demodulator and outputting it as an analog signal;

a video chroma processor for receiving said analog signal and having an analog output processing circuit and an image quality adjusting circuit to produce a video chroma processing signal;

an output device for outputting a display signal based upon said video chroma processing signal;

a display for displaying an image according to said display signal; and

a detector for detecting a period of said superposed picture information signal and picture image signal, wherein:

for said detected period, said image quality adjusting circuit is disabled, and an operating point of said output device is adjusted so said picture information signal is not degraded by an image quality adjustment.

26. A high definition display unit, comprising:

a tuner for processing a mixed television signal in which a picture information signal is superposed on a picture image signal;

a digital demodulator for demodulating an output of said tuner;

a digital decoder for decoding an output of said digital demodulator and outputting it as an analog signal;

a video chroma processor for receiving said analog signal, and having an analog output processing circuit and an image quality adjusting circuit for producing a video chroma processing signal;

an output device for outputting a display signal based upon said video chroma processing signal;

a display for displaying an image according to said display signal; and

a detector for detecting a period of said superposed picture information signal and picture image signal, and for producing a detection signal, wherein:

said adjustment range limiting circuit is operated according to said detection signal; and

an adjustment range limiting circuit of said image quality adjusting circuit is provided.

27. A high definition signal processing method, comprising the steps of:

inputting a mixed television signal, in which a picture information signal is superposed on a picture image signal, into a tuner;

demodulating an output of said tuner by a digital demodulator;

decoding an output of said digital demodulator by a digital decoder, and processing a decoded output of said digital decoder as an analog signal;

processing said analog signal and adjusting an image quality thereof by a video chroma processor to produce a video chroma processing signal;

outputting a display signal based upon said video chroma processing signal by an output device to a display;

displaying an image on said display according to said display signal;

detecting a period of said superposed picture information signal and picture image signal; and

disabling said adjustment of image quality according to said detected period.

28. A high definition signal processing method, comprising the steps of:

inputting a mixed television signal, in which a picture information signal is superposed on a picture image signal, into a tuner;

demodulating an output of said tuner by a digital demodulator;

decoding an output of said digital demodulator by a digital decoder, and processing a decoded output of said digital decoder as an analog signal;

processing said analog signal and adjusting an image quality thereof by a video chroma processor to produce a video chroma processing signal;

outputting a display signal based upon said video chroma processing signal by an output device to a display;

displaying an image on said display according to said display signal;

detecting a period of said superposed picture information signal and picture image signal;

separating said picture information signal from said picture image signal by said video chroma processor for said detected period; and

bypassing said image quality adjustment of said separated picture information signal to avoid image quality adjustment by said video chroma processing signal.

29. A high definition signal processing method, comprising the steps of:

inputting a mixed television signal, in which a picture information signal is superposed on a picture image signal, into a tuner;

demodulating an output of said tuner by a digital demodulator;

decoding an output of said digital demodulator by a digital decoder, and processing a decoded output of said decoder as an analog signal;

processing said analog signal and adjusting an image quality thereof by a video chroma processor to produce a video chroma processing signal;

outputting a display signal based upon said video chroma processing signal by an output device;

displaying an image on a display according to said display signal;

detecting a brightness of said image to produce a brightness detection signal;

detecting a period of said superposed picture information signal and picture image signal; and

adjusting, for said detected period, said image quality according to said brightness detection signal.

30. A high definition signal processing method, comprising the steps of:

inputting a mixed television signal, in which a picture information signal is superposed on a picture image signal, into a tuner;

demodulating an output of said tuner by a digital demodulator;

decoding an output of said digital demodulator by a digital decoder, and processing said decoded output as an analog signal;

processing said analog signal and adjusting an image quality thereof by a video chroma processor to produce a video chroma processing signal;

outputting a display signal based upon said video chroma processing signal by an output device;

displaying an image on a display according to said display signal;

detecting a period of said superposed picture information signal and said picture image signal; and

for said detected period, an operating point of said output device is adjusted without adjusting said image quality.

31. A high definition signal processing method, comprising the steps of:

inputting a mixed television signal, in which a picture information signal is superposed on a picture image signal, into a tuner;

demodulating an output of said tuner by a digital demodulator;

decoding an output of said digital demodulator by a digital decoder, and processing said decoded output as an analog signal;

processing said analog signal and adjusting an image quality thereof by a video chroma processor to produce a video chroma processing signal;

outputting a display signal based upon said video chroma processing signal by an output device;

displaying an image is on a display according to said display signal;

limiting an image quality adjustment range;

detecting a period of said superposed picture information signal and picture image signal to produce a detection signal; and

said image quality adjustment range is limited according to said detection signal.

* * * * *

EXHIBIT E

US006549243B1

(12) **United States Patent**
Takashimizu et al.

(10) **Patent No.: US 6,549,243 B1**
(45) **Date of Patent: Apr. 15, 2003**

(54) **DIGITAL BROADCAST RECEIVER UNIT**

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(73) Assignee: **Hitachi, Ltd.**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/135,727**

(22) Filed: **Aug. 18, 1998**

(30) **Foreign Application Priority Data**

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(51) **Int. Cl.**[7] **H04N 7/01**; H04N 7/00; H04N 3/27; H04N 5/46; H04N 5/44

(52) **U.S. Cl.** **348/558**; 348/554; 348/555; 348/556; 348/441; 348/469; 348/725

(58) **Field of Search** 348/555, 554, 348/558, 556, 557, 725, 441, 458, 435, 512, 536, 537, 469, 468; H04N 7/01, 5/46, 3/27, 9/475

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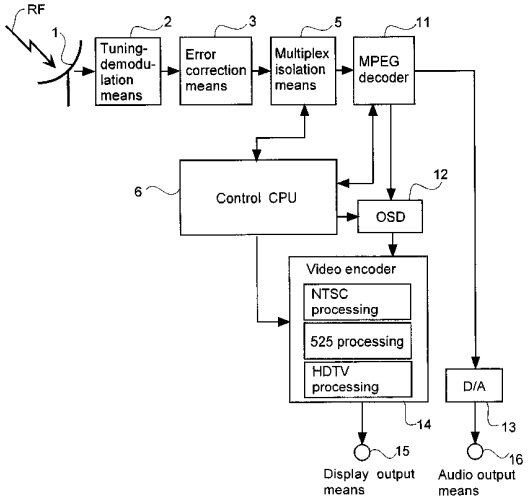
Assistant Examiner—Paulos Natnael
(74) *Attorney, Agent, or Firm*—Antonelli, Terry, Stout & Kraus LLP

(57) **ABSTRACT**

A digital broadcast receiver unit for determining the scanning method of the video signal of the selected program when signals multiplexed through a plurality of different scanning methods are received, processing these video signals by an appropriate video signal processor constituting a video encoder, and then outputting the result. This digital broadcast receiver unit includes a demodulator to tune in the channel of the received signal and perform demodulation, a multiplex isolator to isolate the audio, video and other types of data coded from the multiplex signals output from the demodulator, a decoder to decode the video signal and audio signal from the multiplex isolator, a plurality of video processors performing respectively different corresponding scanning methods and connected to an output of the decoder, an output selector to select from among outputs from the plurality of video processors, and a controller to control the output selector and determine the scanning method of the video signal of the selected program and also perform the appropriate processing based on the scanning method for the selected video signal.

27 Claims, 11 Drawing Sheets



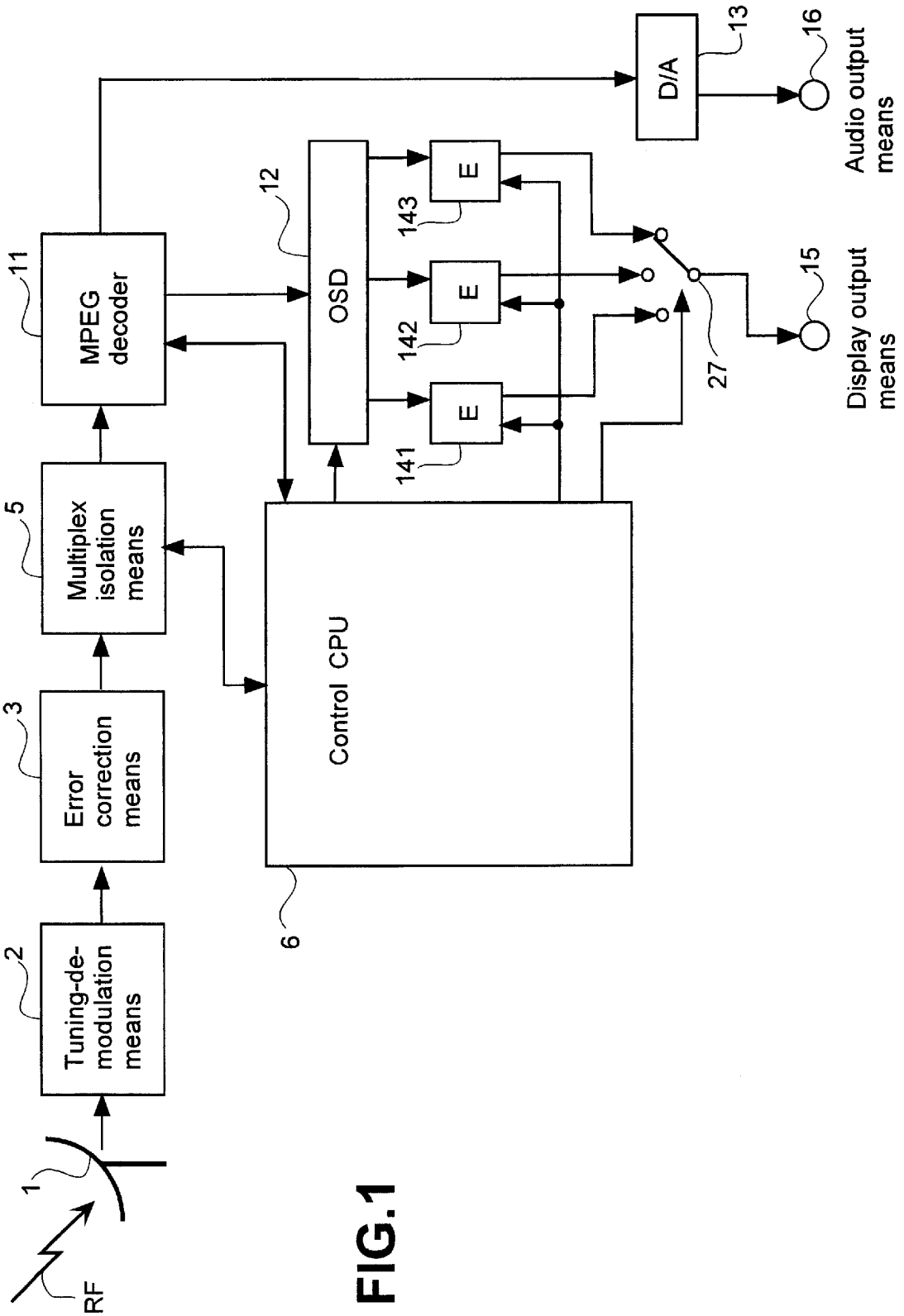

RF
1
Tuning-de-modulation means
2
Error correction means
3
Multiplex isolation means
5
MPEG decoder
11
OSD
12
Control CPU
6
E
143
E
142
E
141
27
D/A
13
Audio output means
16
Display output means
15

FIG.1

FIG.2A

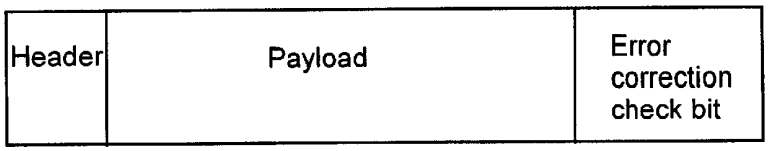


FIG.2B

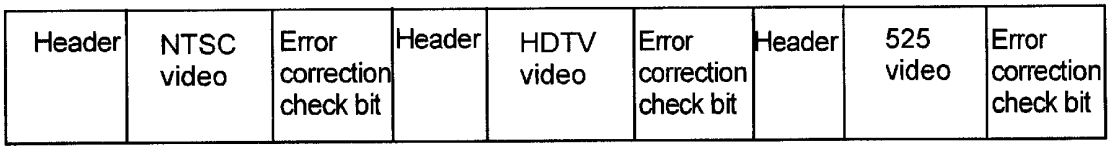


FIG.2C

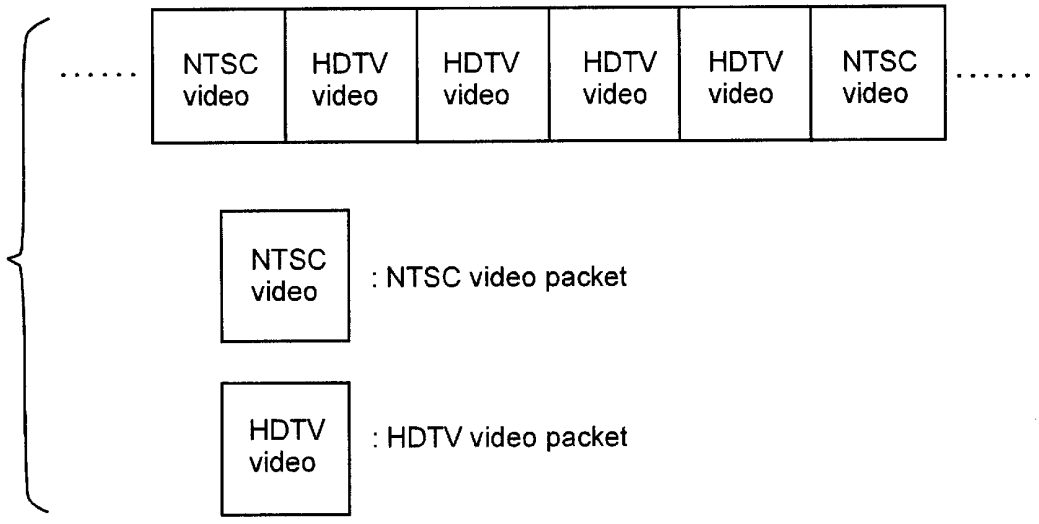


FIG.3

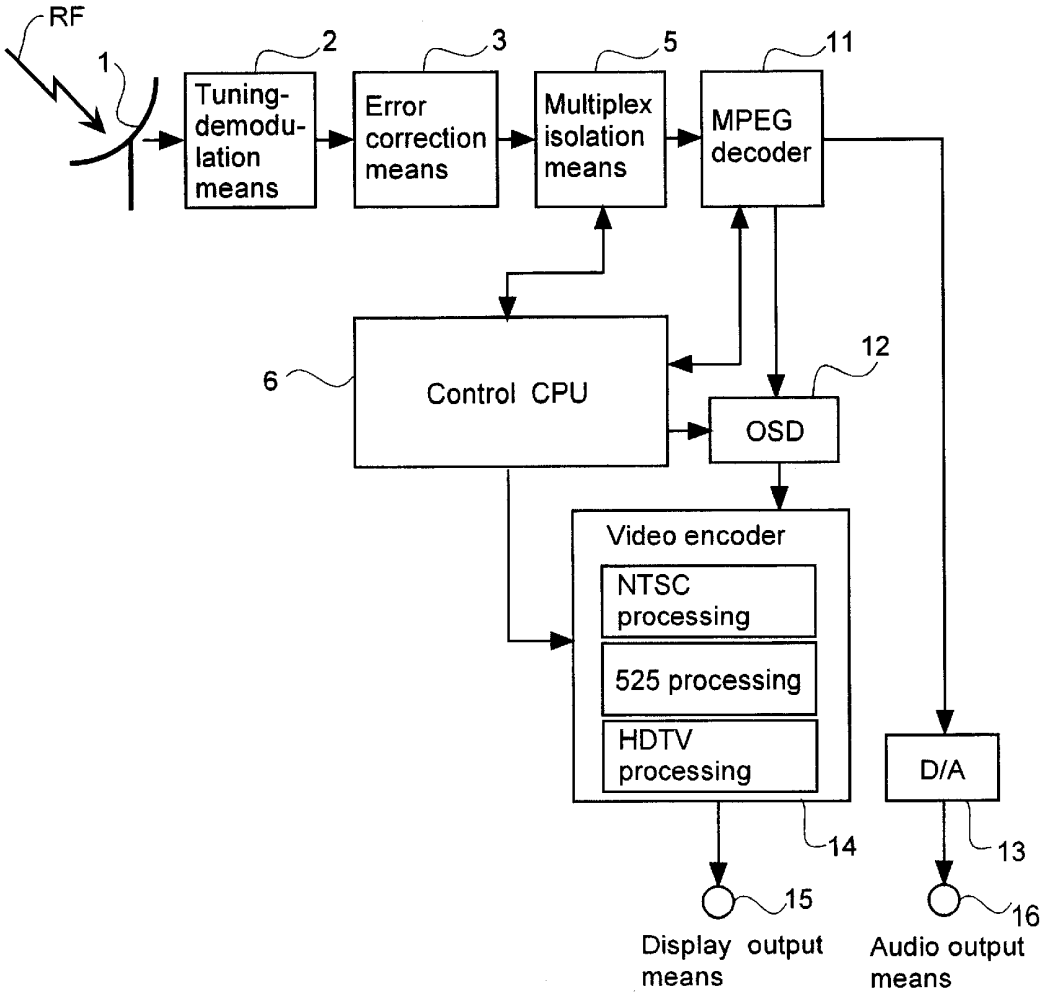


FIG.4A

Header	NTSC video	Error correction check bit	Header	HDTV video	Error correction check bit	Header	Scanning method data	Error correction check bit

FIG.4B

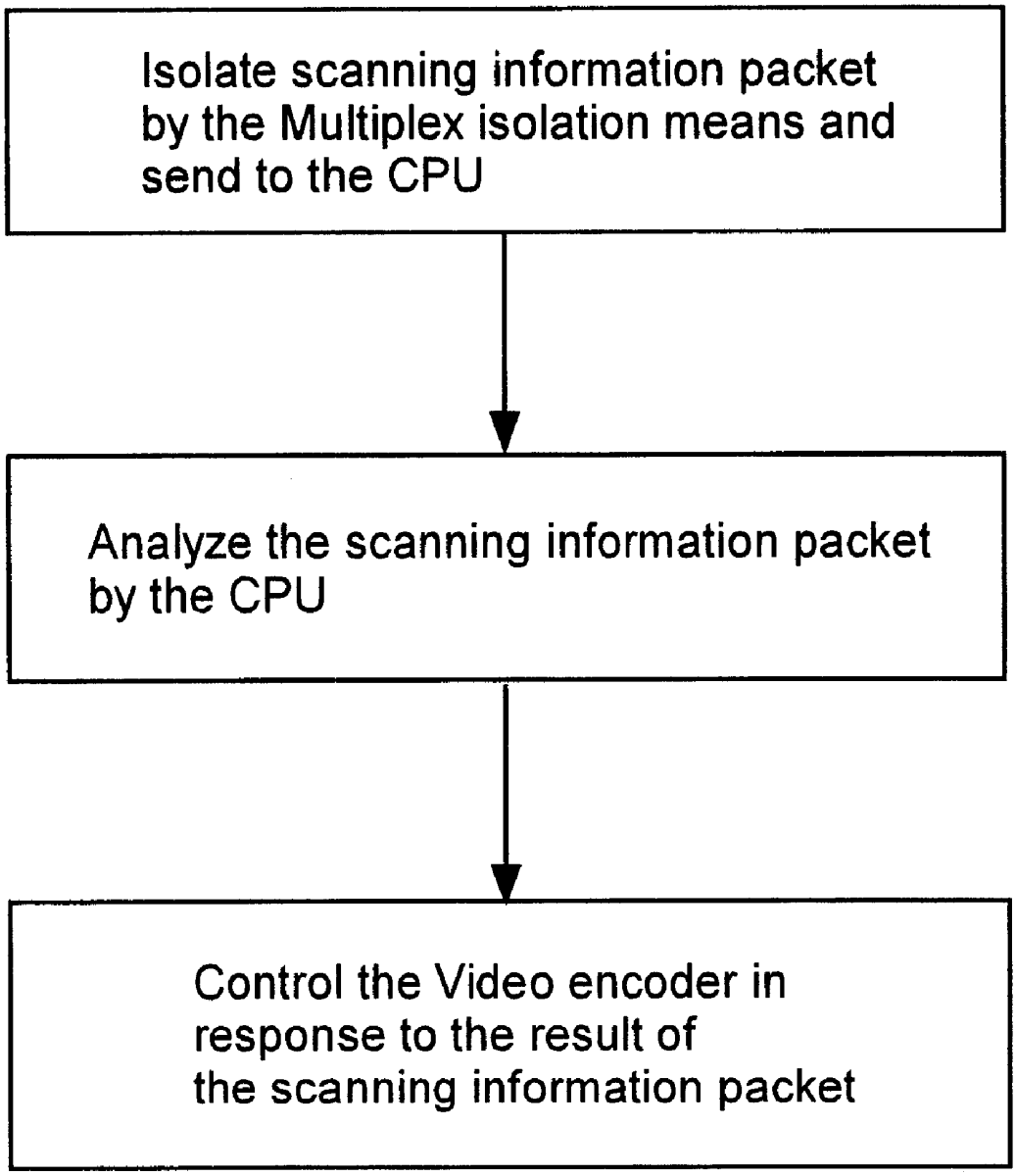

Isolate scanning information packet by the Multiplex isolation means and send to the CPU
Analyze the scanning information packet by the CPU
Control the Video encoder in response to the result of the scanning information packet

FIG.5

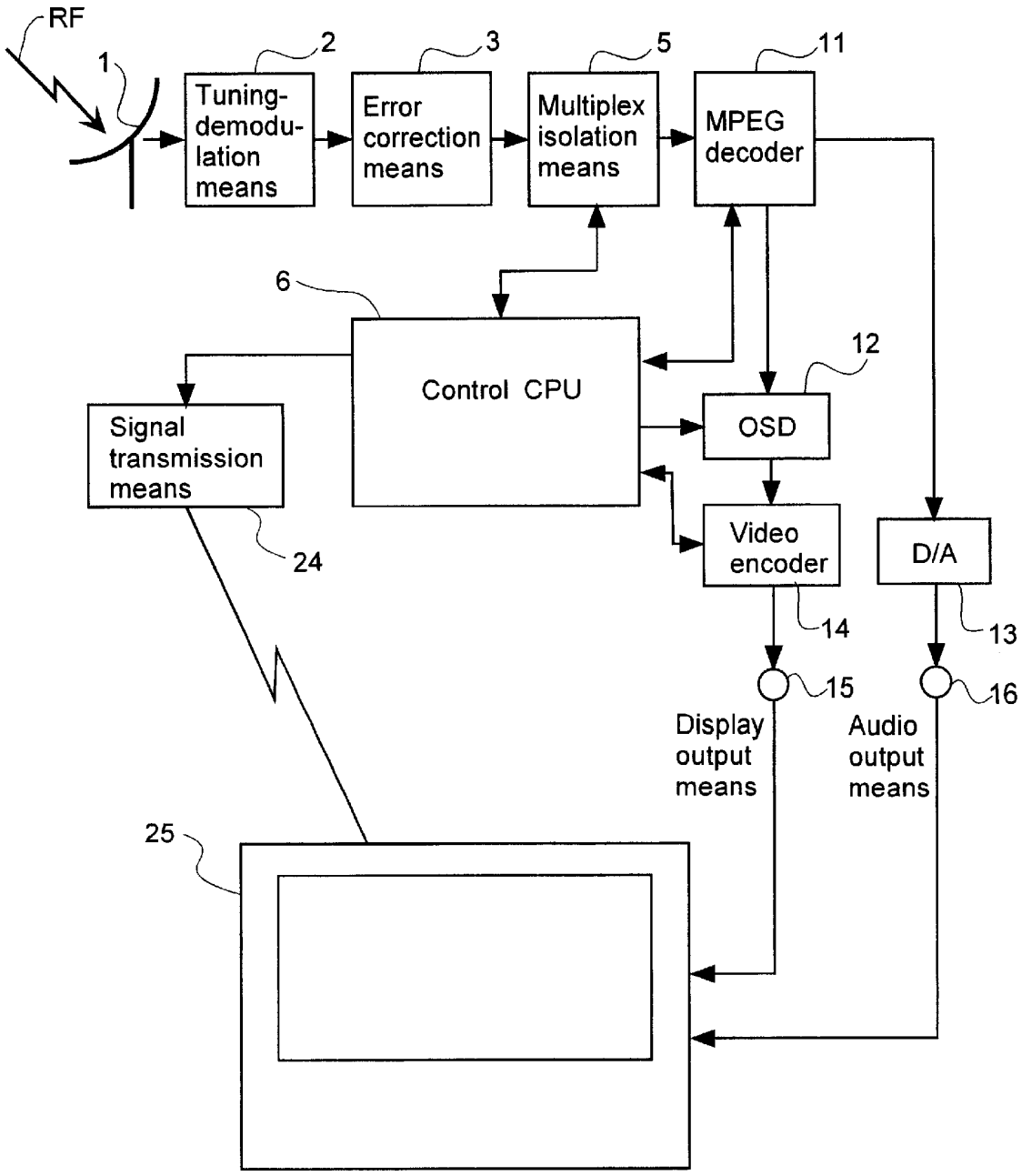

RF
1
2
Tuning-demodulation means
3
Error correction means
5
Multiplex isolation means
11
MPEG decoder
6
Control CPU
12
OSD
Signal transmission means
24
Video encoder
D/A
14
13
15
16
Display output means
Audio output means
25

FIG.6

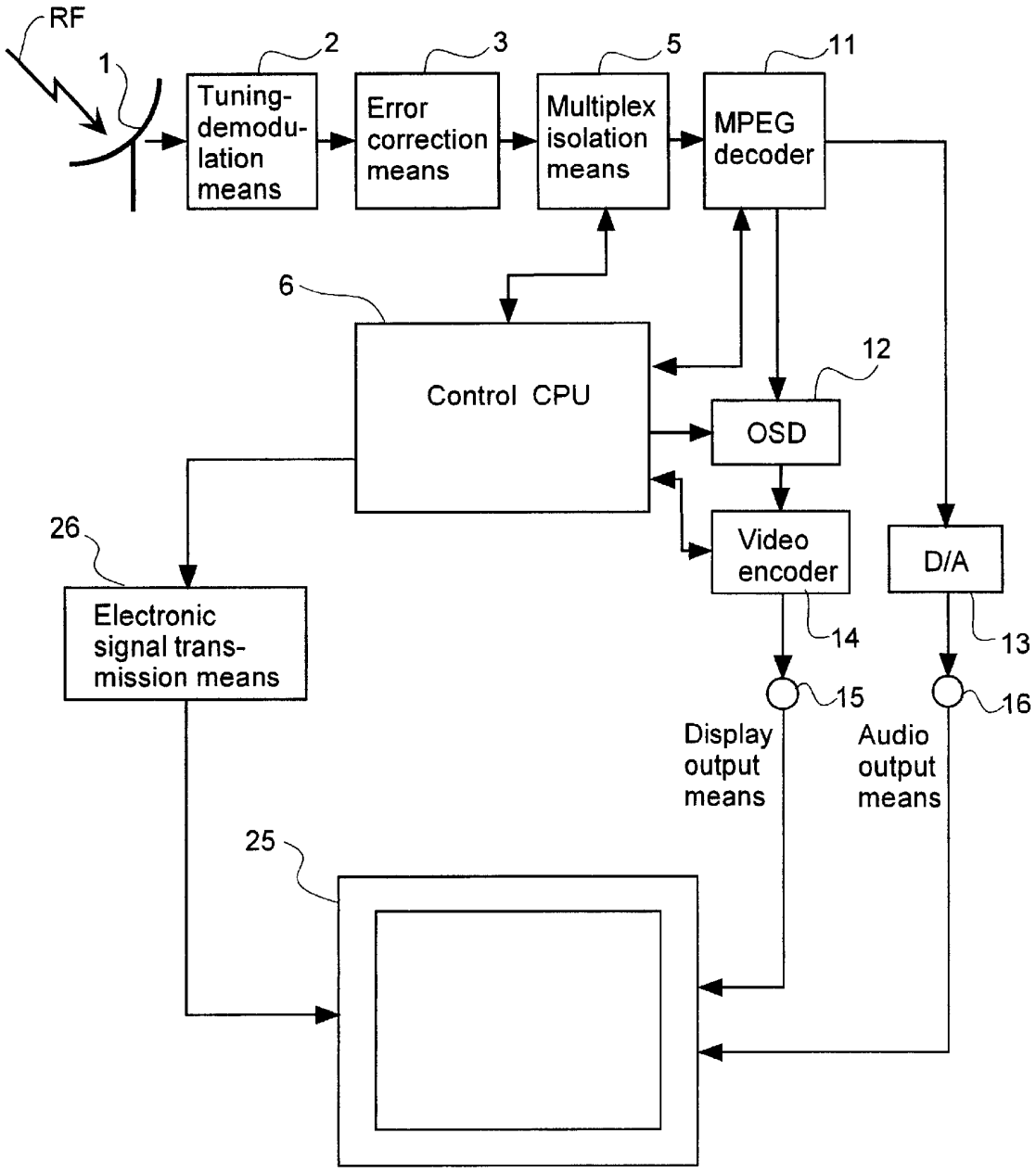

RF
1
2
Tuning-demodulation means
3
Error correction means
5
Multiplex isolation means
11
MPEG decoder
6
Control CPU
12
OSD
Video encoder
D/A
26
Electronic signal transmission means
14
13
15
16
Display output means
Audio output means
25

FIG.7

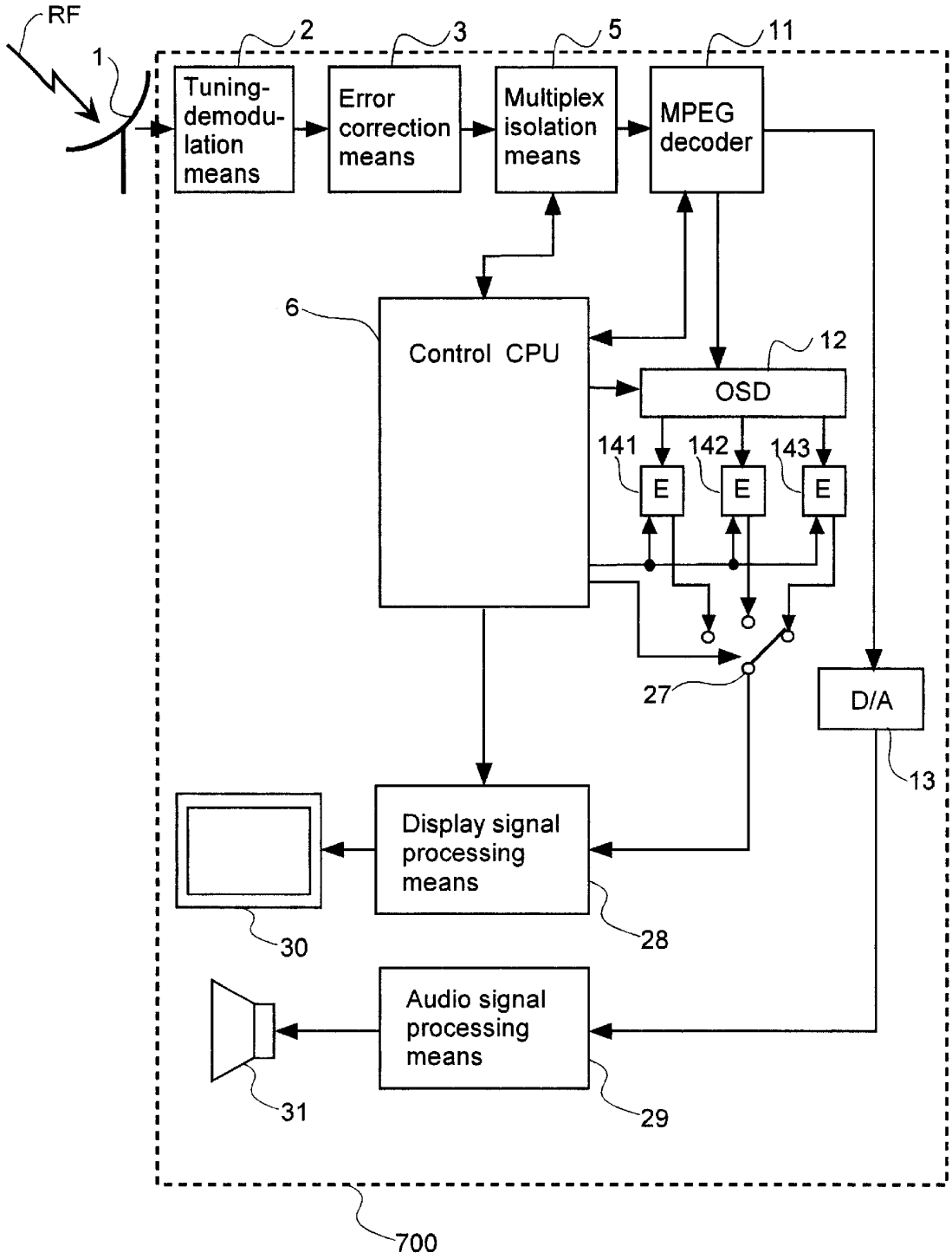

RF
1
2
3
5
11
Tuning-demodu-lation means
Error correction means
Multiplex isolation means
MPEG decoder
6
Control CPU
12
OSD
141
142
143
E
E
E
27
D/A
13
Display signal processing means
28
30
Audio signal processing means
29
31
700

FIG.8

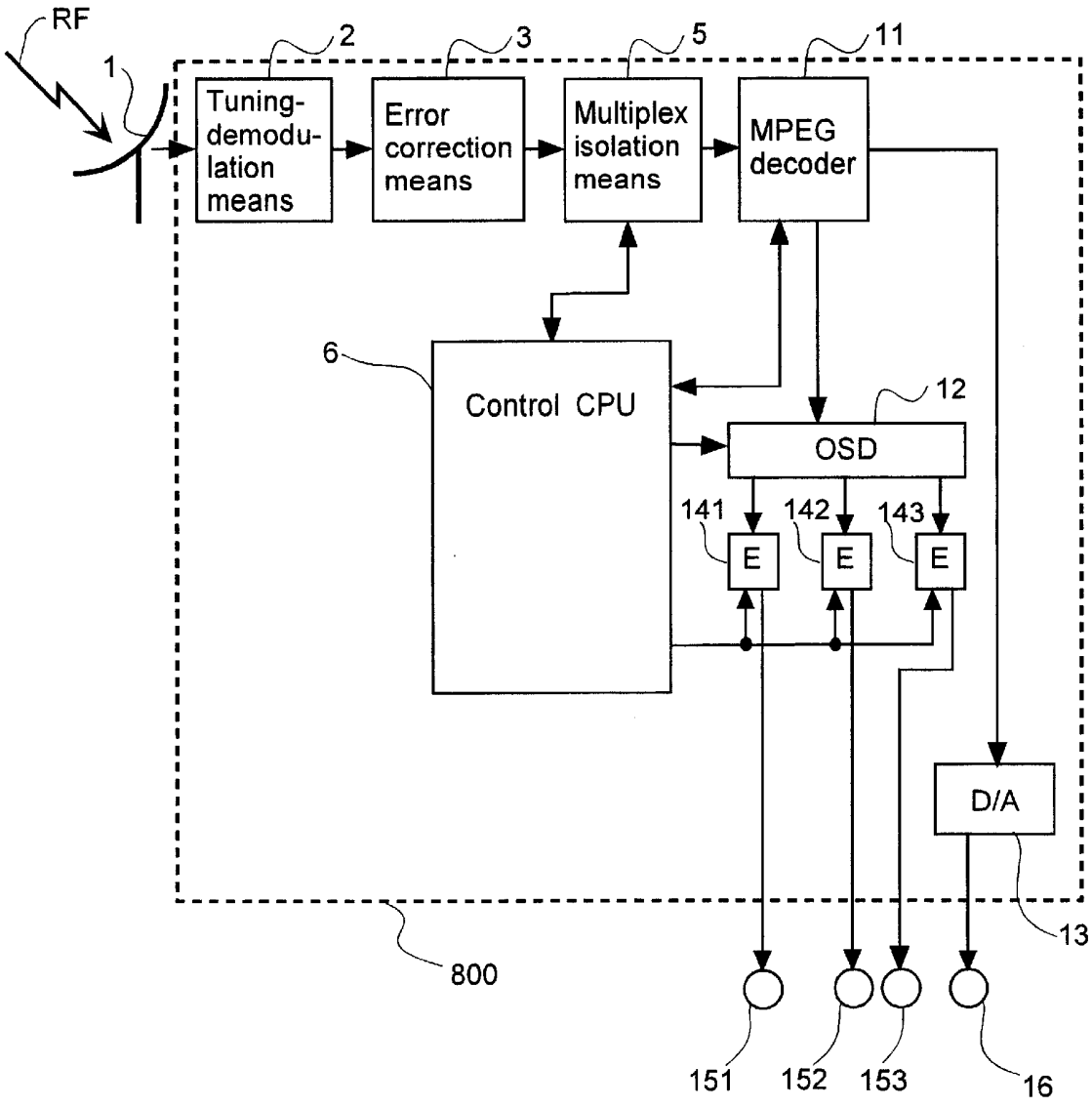

RF
1
2
3
5
11
Tuning-demodulation means
Error correction means
Multiplex isolation means
MPEG decoder
6
Control CPU
12
OSD
141
142
143
E
E
E
D/A
13
800
151
152
153
16

FIG.9

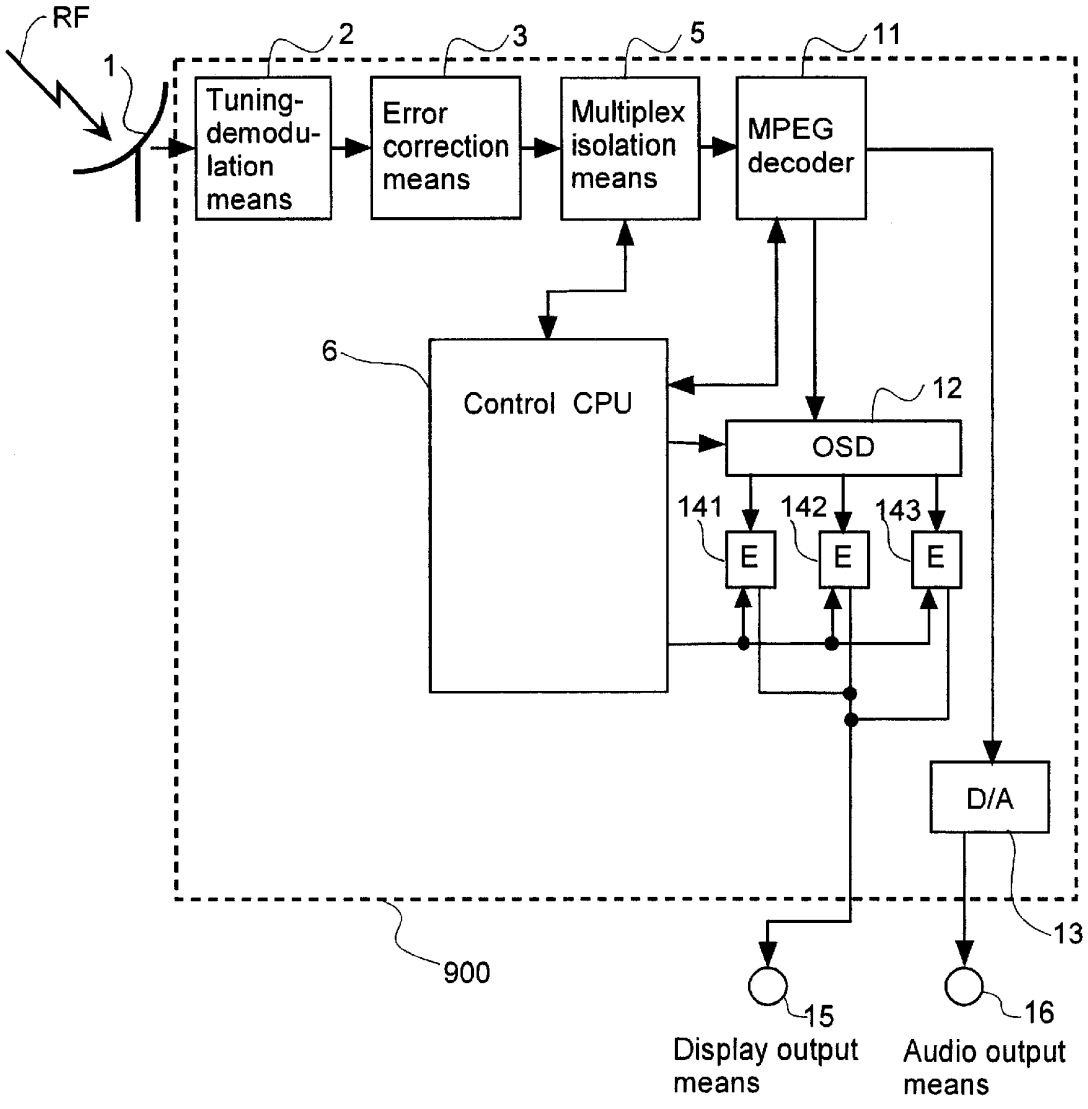

RF
1
2
3
5
11
Tuning-demodulation means
Error correction means
Multiplex isolation means
MPEG decoder
6
Control CPU
12
OSD
141
142
143
E
E
E
D/A
900
13
15
16
Display output means
Audio output means

FIG.10

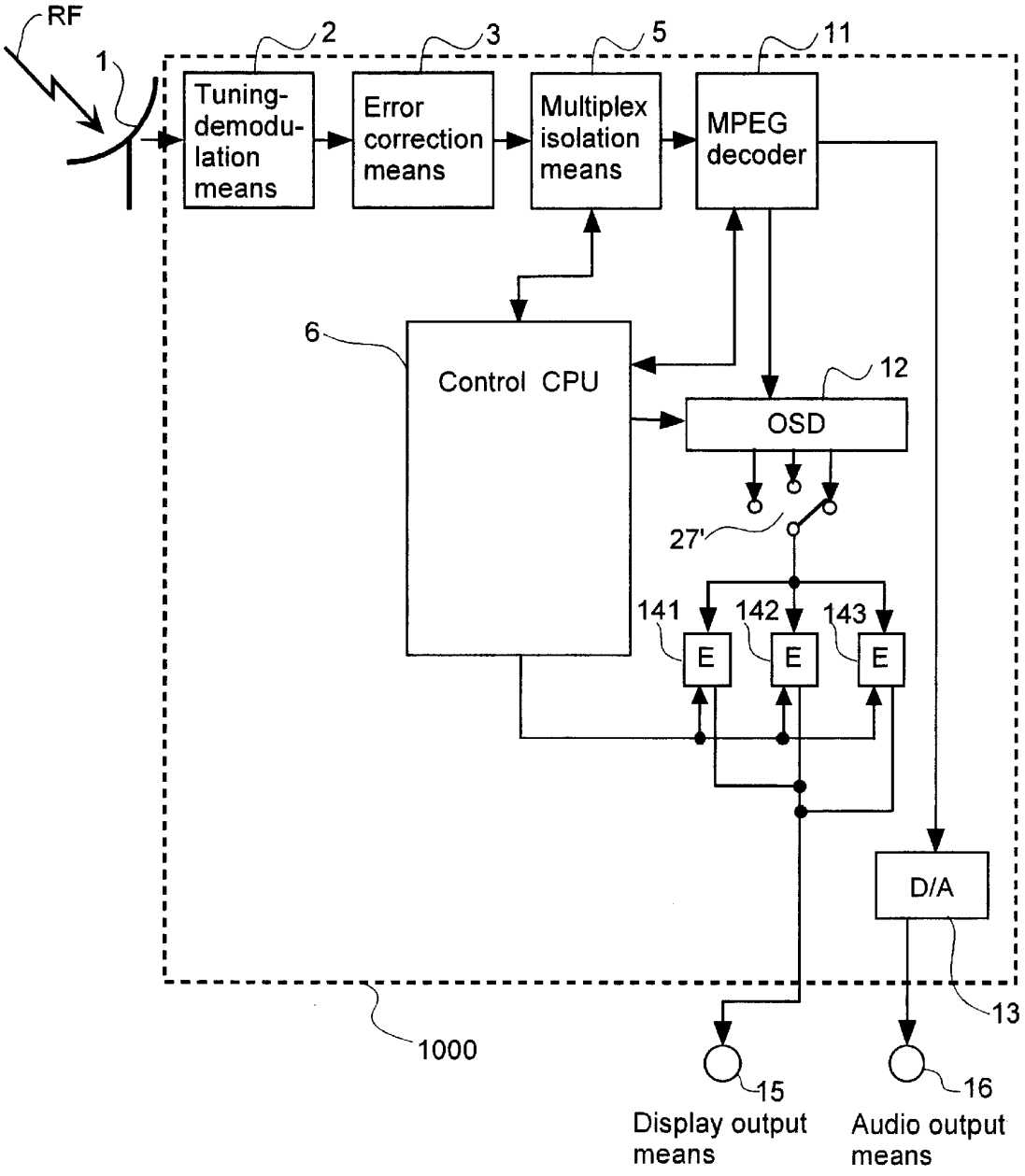
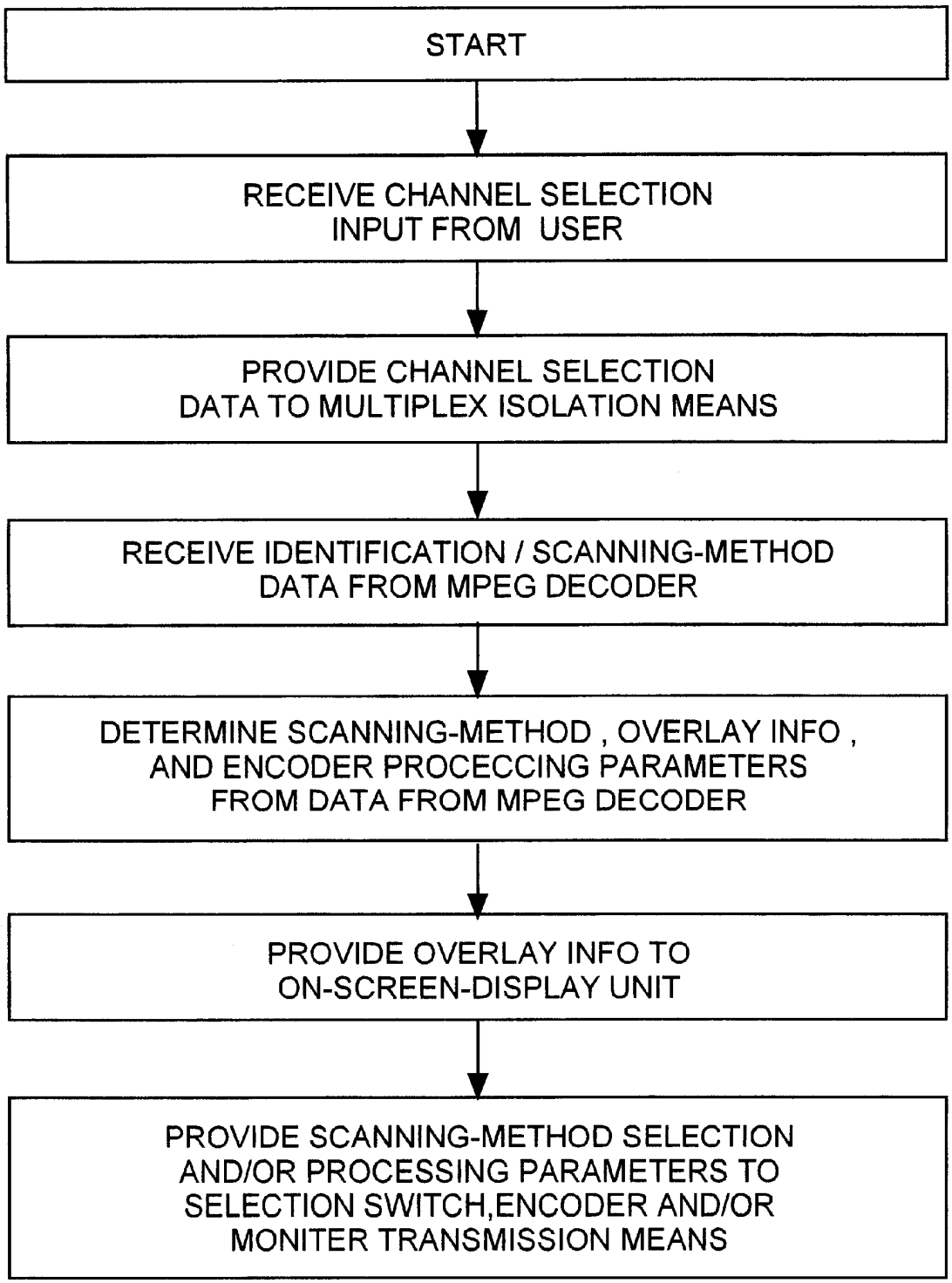

RF
1
2
3
5
11
Tuning-demodulation means
Error correction means
Multiplex isolation means
MPEG decoder
6
Control CPU
12
OSD
27'
141
142
143
E
E
E
D/A
13
1000
15
16
Display output means
Audio output means

FIG.11


START
RECEIVE CHANNEL SELECTION INPUT FROM USER
PROVIDE CHANNEL SELECTION DATA TO MULTIPLEX ISOLATION MEANS
RECEIVE IDENTIFICATION / SCANNING-METHOD DATA FROM MPEG DECODER
DETERMINE SCANNING-METHOD , OVERLAY INFO , AND ENCODER PROCECCING PARAMETERS FROM DATA FROM MPEG DECODER
PROVIDE OVERLAY INFO TO ON-SCREEN-DISPLAY UNIT
PROVIDE SCANNING-METHOD SELECTION AND/OR PROCESSING PARAMETERS TO SELECTION SWITCH,ENCODER AND/OR MONITER TRANSMISSION MEANS

DIGITAL BROADCAST RECEIVER UNIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a digital broadcast receiver unit, and in particular, relates to a digital broadcast receiver unit capable of receiving, in one stream, multiplex video signals formatted according to a plurality of differing scanning methods.

2. Description of Related Art

In digital transmission technology, in addition to video and audio signals, all kinds of information can be multiplexed and broadcast over one common carrier wave, i.e., multi-channel broadcasts utilizing this technology have already commenced. By utilizing this digital transmission technology, video signals for different scanning methods can be coded, multiplexed (i.e., placed on one common carrier wave) and then broadcast.

In contrast, in related art analog broadcast receivers, television receivers are able to receive transmissions from a plurality of analog broadcast systems. In analog broadcasting, however, different kinds of information cannot be multiplexed (or placed together on the same carrier wave) so that the received video signal itself must be analyzed to determine the scanning method. When receiving different video signals having a plurality of scanning systems in the above mentioned related art analog broadcasts, not only was a custom identification means required to analyze and process the received video signal itself, but in order to identify the video signal, video signal processing circuits had to be operated whose operation was not actually necessary.

In contrast, one important feature of digital broadcasting, however, is that a plurality of information such as audio, video and data can be multiplexed and sent as one transmission stream. Utilizing multiplexed data therefore means that various features can be provided.

SUMMARY OF THE INVENTION

In view of the above problems, it is therefore an object of this invention to provide a digital broadcast receiver for identifying video signal scanning methods utilizing different kinds of multiplexed information, and using such identification for selecting an appropriate scanning method for reproduction.

In order to achieve the above, this invention is directed to a digital broadcast receiver unit for receiving a digital multiplexed signal stream having multiplexed signals commonly encoded using a same encoding/decoding standard, the multiplexed signals including video signals corresponding to a plurality of different video signal formats, and isolating and reproducing at least one video signal, the unit including: a selector to select and extract one video signal from a received the digital multiplexed signal; a decoder to decode the video signal from the selector according to the encoding/decoding standard; a plurality of video processor sections, with respective video processor sections providing video processing according to a different video signal format of the plurality of different video signal formats; and a controller using information from the received the digital multiplexed signal to determine a video signal format of the video signal from the decoder, and selecting one video processor section of the video processor sections to perform video processing of the video signal according to a determined video signal format thereof. More particularly, the present invention determines the scanning method of the video signal of the selected program and then performs the appropriate processing based on the scanning method for the selected video signal.

The foregoing and a better understanding of the present invention will become apparent from the following detailed description of the preferred embodiments and claims when read in connection with the accompanying drawings, all forming a part of the disclosure hereof this invention. While the foregoing and following written and illustrated disclosure focuses on disclosing embodiments of the invention which are considered preferred embodiments, it should be clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

BRIEF DESCRIPTION OF THE DRAWING(S)

The following represents brief descriptions of the drawings, wherein:

FIG. **1** shows a block diagram of the first embodiment of this invention;

FIGS. **2**A–C are drawings showing exemplary configurations of the digital multiplex stream;

FIG. **3** is a block diagram showing the configuration of a second embodiment of this invention;

FIGS. **4**A–B are drawings showing the configuration of a digital multiplex stream, and a flowchart showing scanning information packet processing, respectively;

FIG. **5** is a block diagram showing the configuration of a third embodiment of this invention;

FIG. **6** is a block diagram showing the configuration of a fourth embodiment of this invention;

FIG. **7** is a block diagram showing the configuration of a fifth embodiment of this invention;

FIG. **8** is a block diagram showing the configuration of a sixth embodiment of this invention;

FIG. **9** shows a different block diagram showing of this invention;

FIG. **10** shows an another different block diagram showing of this invention; and

FIG. **11** is a flowchart indicative of exemplary processing operations conducted by an application specific integrated circuit (ASIC) or central processing unit (CPU) with respect to the present invention, e.g., via suitable programming.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS OF THE INVENTION

Before beginning a detailed description of the subject invention, mention of the following is in order. When appropriate, like reference numerals and characters are used to designate identical, corresponding or similar components in differing figure drawings.

Hereafter, the embodiment of this inventions will be explained while referring to the accompanying drawings. FIG. **1** is a block diagram showing the structure of the digital broadcast receiver of this invention. An RF carrier wave sent from a communications satellite (not shown) is received at an antenna **1** and then processed by other components. More particularly, in FIG. **1**, the numeral **1** denotes the antenna, the numeral **2** is a tuning-demodulation means, the numeral **3** is an error correction means, the numeral **5** is a multiplex isolation means for treating a multiplexed signal, the

numeral **6** is a control CPU, the numeral **11** is an MPEG decoder for decoding the coded audio and video information. Also in FIG. **1**, the numeral **12** is an OSD (On Screen Display) circuit for adding character information to video signals output from the Moving Picture Experts Group (MPEG) decoder **11**, the numeral **13** is a D/A converter for converting digital audio signals into analog signals. Further, in FIG. **1**, the numeral **141** is a video encoder, for instance, to convert 525 interlaced scanning lines of an NTSC system signal into an analog signal and add synchronizing information, etc. The numeral **142** is a video encoder, for instance, to convert 525 scanning lines of a sequential scanning 525 progressive signal (hereafter abbreviated to 525P signal) into an analog signal and add synchronizing information, etc. The numeral **143** is a video encoder, for instance, to convert the 1080 interlaced scanning lines of an HDTV system signal into an analog signal and add synchronizing information, etc. The numeral **15** in the same figure is a video signal output terminal, the numeral **16** is an audio signal output terminal, and the numeral **27** is an output selection means.

The signal received by the antenna **1** is tuned and demodulated by the tuning-demodulation means **2**. The demodulated signal from the tuning-demodulation means **2** is output to the error correction means **3**. Error correction based on the addition of an error correction code is then performed by the error correction means **3**. Next, according to control provided by the CPU **6**, a signal of a program for viewing is demultiplexed (isolated from the other signals) and output by the multiplex isolation means **5**.

The coded audio data and coded video data isolated by the multiplex isolation means **5** is applied to the MPEG decoder **11**. The MPEG decoder **11** decodes the coded data into the digital signal that was present prior to MPEG coding, i.e., according to control provided by the CPU **6**. The digital video signal output from the MPEG decoder **11** is applied to the OSD means **12** which adds character information according to control by the CPU **6**, and is sent to the video encoders **141**, **142** and **143** which each convert the digital video signal into an analog video signal, again, according to control by the CPU **6**. As a parallel operation, the digital audio signal output from the MPEG decoder **11** is applied to the D/A converter **13**, and converted to an analog audio signal. The output from the video encoders **141**, **142** and **143** is applied to the selection means **27**, wherein an appropriate one of the outputs from the video encoders **141**, **142** and **143** is selected via control by the control CPU **6**, and the selected video signal is output. This process allows the analog video signal and analog audio signal sent from the transmitting side to be played back and output in parallel to the video signal output terminal **15** and the audio signal output terminal **16**, respectively.

The operation when processing video signals for different broadcast systems was explained above. FIG. **2**A shows the structure of one unit of the multiplexed signal referred to as a transport stream packet (hereafter TS packet). The TS packet is comprised of a payload for storing data (e.g., video, audio and other info.), a header for indicating data such as identification (e.g., packet number) and/or scanning approach (e.g., NTSC, PAL, etc.) data, and an error correction check bit for performing error correction. As shown in FIG. **2**B, in a digital broadcast, multiplexing of video signals in one stream for a plurality of differing scanning methods can be performed. FIG. **2**C shows (without headers and error correction check bits) a state of a TS packet in the case where an NTSC signal and an HDTV signal are multiplexed as one example. As is apparent from such Fig., video signals

of different scanning systems do not have to be alternately or periodically provided, but instead, can be provided in any order.

When the viewer selects the desired program from such signals, e.g., through any know remote or switch arrangement (not shown), the multiplex isolation means **5** responds thereto, and only the coded audio data and the coded video data that comprises the selected program is isolated and output from the multiplex isolation means **5**. The coded video data and coded audio data which is output is applied to the MPEG decoder **11**. The coded video data includes data detailing the scanning method. The MPEG decoder **11** detects the data detailing the scanning method from the input coded data and conveys this data to the control CPU **6**. Based on the information conveyed from the MPEG decoder **11**, and the determination of the present scanning method, the CPU **6** (via suitable software programming) controls the video encoders **141**, **142** and **143**, as well as control of the selection means **27**. Thus, only the video encoder matching the video signal selected from among the video encoders **141**, **142** and **143** is utilized and an analog video signal is output from the selection means **27**.

As explained previously, operation of the video encoders **141**, **142** and **143** based on information on the scanning method detected by the MPEG decoder **11** of this invention and the selection means **27** not only allows processing and output of the signal for the correct scanning method, but also allows shutting off of the power to video encoders not currently needed and to stop their operation so that useless expenditure of unnecessary power and generation of unnecessary heat is prevented. Further, the generation of signal interference is also reduced.

Additionally, although in FIG. **1** there is illustrated a configuration in which a signal having a system corresponding to each of the video encoders **141**, **142** and **143** is inputted, it may also be applicable that signals of all the types of scanning systems are connected in common from the same terminal to the video encoders **141**, **142** and **143** as shown in FIG. **9** (implemented a self-contained unit **900**, e.g., a set-top box), and thereby the controlling CPU **6** controls in such a way that only the circuit coinciding with the scanning system of an input signal in the video encoders **141**, **142** and **143** is operated. In addition, as shown in FIG. **10** (implemented as a self-contained unit **1000**, e.g., set-top box), a signal output terminal of each of the scanning systems is connected to the switch **27'** so that the switch **27'** is controlled by the controlling CPU **6**, whereby an output terminal of the OSD means **12** coinciding with a video scanning system of a selected TV program is selected, and the signal is inputted to the video encoder. Concurrently, only the video encoder corresponding to the inputted video signal may be allowed to operate under the control of the CPU **6**. As described above, either configuration shown in FIGS. **9** and **10** provides an effect similar to that exhibited by the configuration shown in FIG. **1**.

The second embodiment of this invention is next explained while referring to FIG. **3**. Reference numeral **14** in FIG. **3** denotes a video encoder. The embodiment of FIG. **3**. differs from the embodiment of FIG. **1** in that the configuration of the video encoder **14** is a singular circuit, e.g., a sub-processor, etc., which versatilely permits processing of any of the NTSC signals, 525 signals or HDTV signals. More particularly, the video encoder **14** can be provided as a sub-processor or singular application specific-integrated circuit (ASIC) chip, having segregated processing subprograms or processing areas which can be selectively enabled/disabled to permit processing according to an

appropriate scanning method. While the FIG. **1** approach of separately provided encoders has the power saving advantage that unneeded encoders can be powered down, a FIG. **3** software implemented approach has the advantage that the encoder **14** can be easily changed/customized via simple software reprogramming. The control CPU **6** operates the video encoder **14** so as to match the scanning method detected by the MPEG decoder **11** with any of the three previously related processing means based on information conveyed from the MPEG decoder **11**.

More specifically, for instance, video filter parameters which limit the available video band are regulated. In addition, in FIG. **3**, the video encoder **14** may be constructed to have a configuration where a parameter is fixed in such a way that it may be adapted only for a predetermined kind of video signal. Alternatively, the parameter may be constructed to have a configuration that it is not fixed by the video encoder **14** by itself, but an optional value is selected by the controlling CPU **6**. For the configuration when the fixed parameter is selected, it is possible to simplify the control to be carried out by the controlling CPU. In the case of the configuration in which an optional value is selected by the controlling CPU **6**, it is possible to cope with video signals of all known scanning systems. With such an arrangement as above, the video signal inputted to the video encoder **14** is correctly encoded and outputted from the output terminal **15** as an analog video signal. This process allows the signals input to the video encoder **14** to be sent from the output terminal **15** as correctly encoded analog video signals. As explained above, processing of signals for the correct scanning method can be performed since this invention controls the video encoder **14** according to the appropriate scanning method, based on information on the scanning method detected by the MPEG decoder **11**.

The embodiments in FIGS. **1** and **3** showed examples of detection with an MPEG decoder **11** of scanning method data containing coded image data. However, as shown for example in FIG. **4**A, when there is a TS packet holding data showing the scanning method for each video signal in the payload, the data in the TS packet listing the scanning methods can be isolated by means of the above multiplex isolation means **5**, and conveyed to the control CPU **6** for subsequent use in control of the selection means **27** and the video encoder. A flowchart of this process is shown in FIG. **4**B. Even in this case, the results will clearly be the same as when detecting the scanning method with the MPEG decoder **11**.

The third embodiment of this invention is shown in FIG. **5**. The embodiment of FIG. **5** differs from the embodiment of FIG. **1** for instance, in that a signal transmission means **24** is provided for sending a signal to a television receiver, e.g., an infrared signal. This signal transmission means **24** sends an infrared signal derived from information from the MPEG decoder **11**, and such infrared signal contains information indicating the scanning method of the video signal. This arrangement for instance allows the scanning method of the video signal detected by the MPEG decoder **11** to be conveyed to a television receiver **25** having a means to receive the aforementioned infrared signal and also able to handle a plurality of scanning methods (e.g., a multi-sync or multi-scan capable television receiver), when this television receiver **25** is connected to the video signal output terminal **15**. The scanning method of the video signal for the television receiver **25** is therefore switched to match the scanning method output from the video signal output terminal **15** so that a viewer need not provide and/or manually manipulate a separate scanning method switcher.

FIG. **5** showed an example using an infrared signal as a signal transmission means **24**, however this invention is not limited to this method and an RF waveform signal sending means may also be utilized to send an RF carrier wave signal without an infrared signal. A television receiver provided with this RF waveform signal receiving capability and connected to the video signal output terminal **15** will achieve the same effect of the invention.

FIG. **6** shows the fourth embodiment of this invention. The embodiment of FIG. **6** differs from the embodiment of FIG. **5** in that rather than using a wireless signal such as infrared to show the scanning method of the video signal, an electrical signal is instead conveyed by a wire utilizing an electrical or electronic signal transmission means **26**. Using the configuration in FIG. **6** will clearly achieve the same effect of the invention as in the embodiment of FIG. **5**.

A fifth embodiment of the invention is shown in FIG. **7**. The embodiment of FIG. **7** differs from the embodiment of FIG. **1** in that the digital broadcast receiver of this invention is housed in a same cabinet **700** with a display unit, or in other words, this embodiment comprises a television with an internal digital broadcast receiver unit. In FIG. **7**, the reference numeral **28** denotes a display signal processing means, **29** denotes an audio signal processing means, **30** denotes a display means such as a CRT or liquid crystal display panel or a plasma display panel, and **31** denotes an audio signal output means such as a speaker. In FIG. **7**, the display processing means **28** and the display means **30** are configured, for example, so that an NTSC signal, a 525P signal or a HDTV signal can be displayed. Also in FIG. **7**, the control CPU **6** detects the video signal scanning method that was selected, operates the video encoders **141**, **142** and **143** and along with switching the selection means **27**, controls the display processing means **28** and functions to allow processing of video signal scanning method that was detected. This arrangement permits correct processing of the video signal for the program selected by the equipment comprising a television with an internal digital broadcast receiver unit and display of the program by means of the display means **30**.

The sixth embodiment of this invention is shown in FIG. **8** (implemented as a self-contained unit **800**, e.g., set-top box). FIG. **1** shows a configuration in which the selector means **27** selects and issues an output from the video encoders **141**, **142** and **143**. As shown in FIG. **8**, however, the sixth embodiment differs in that the selection means **27** is not used and the output from the video encoders **141**, **142** and **143** are respectively output from separate output terminals **151**, **152** and **153**. Using the configuration in FIG. **8** will clearly achieve the same effect of the invention as in the embodiment of FIG. **1**.

FIG. **11** is a flowchart indicative of exemplary processing operations conducted by the CPU **6** with respect to the present invention, e.g., via suitable programming. Such operations are repetitively performed over time.

In the above explanation, the RF carrier wave received by the antenna **1** was sent from an artificial satellite however needless to say, this invention is also applicable in cases where the RF carrier wave is sent from an antenna installed on a ground device. Further, the above explanation described an example of digital broadcast receiver compatible with the three scanning methods consisting of an NTSC signal, a 525P signal and an HDTV signal. However the same effect of the invention can be obtained with a configuration in which other video signal scanning methods are handled by a compatible MPEG encoder or video encoder. Further, as

technology advances further approaches/methods applicable for use with the present invention will be found.

In the digital broadcast receiver of this invention as explained above therefore, video signals can be correctly played back and output even when a plurality of video signals of different scanning methods are received as multiplexed signals in one stream.

This concludes the description of the preferred embodiments. Although the present invention has been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the spirit and scope of the principles of this invention. More particularly, reasonable variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the foregoing disclosure, the drawings and the appended claims without departing from the spirit of the invention. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.

What is claimed is:

1. A digital broadcast receiver unit for receiving a digital multiplexed signal stream having multiplexed signals commonly encoded using a same encoding/decoding standard, said multiplexed signals including video signals corresponding to a plurality of different video signal formats, and isolating and reproducing at least one video signal, said unit comprising:

an isolator to isolate one video signal from a received said digital multiplexed signal;

a decoder to decode the video signal from said isolator according to said encoding/decoding standard;

a plurality of video processor sections, with respective video processor sections providing video processing according to a different video signal format of said plurality of different video signal formats; and

a controller using information from the received said digital multiplexed signal to determine a video signal format of said video signal from said decoder, and selecting one video processor section of said video processor sections to perform video processing of said video signal according to a determined video signal format thereof.

2. A unit as claimed in claim **1**, wherein said digital multiplexed signal is more specifically a packetized digital multiplexed signal with differing groups of packets relating to said different video signal formats, and wherein said isolator isolating a group of packets relating to said one video signal from a received said digital multiplexed signal, and wherein said controller controlling based on information of an isolated said group of packets.

3. A unit as claimed in claim **1**, wherein said plurality of video processor sections is more specifically a plurality of discrete video processors.

4. A unit as claimed in claim **1**, wherein said plurality of video processor sections is more specifically provided via at least one of a common application specific integrated circuit (ASIC) and a common microprocessor adapted to selectively perform processing according to any of said plurality of video processor sections.

5. A unit as claimed in claim **4**, wherein said selecting by said controller is more specifically performed by said controller selectively performing processing with respect to said one video processor section while not performing processing with respect to other ones of said video processor sections.

6. A unit as claimed in claim **1**, wherein said selecting by said controller is more specifically performed by a selector switch controlled to select any output of outputs from said video processor sections, according to said determined video signal format.

7. A unit as claimed in claim **1**, wherein said selecting by said controller is more specifically performed by a selector switch controlled to select any input signal of a plurality of input signals to said video processor sections, said plurality of input signals corresponding to said plurality of different video signal formats, respectively.

8. A unit as claimed in claim **1**, wherein said selecting by said controller is more specifically performed by said controller selectively enabling (said one video processor section) while disabling other ones of said video processor sections.

9. A unit as claimed in claim **1**, further comprising:

a video output display selector controlled by said controller and operable to receive any one of a plurality of outputs of said plurality of video processor sections so as to connect a selected output to a video output display terminal.

10. A unit as claimed in claim **1**, further comprising:

a plurality of video signal output terminals, each terminal providing connection to a differing output of said plurality of video processor sections.

11. A unit as claimed in claim **1**, wherein a scanning method of the video signal is derived from the information from the MPEG decoder and sent to a receiver as one of an infrared signal, a RF signal and an electrical signal, said signal containing information indicating the scanning method used to determine the video signal.

12. A digital broadcast receiver unit for receiving a digital multiplexed signal stream having multiplexed signals commonly encoded using a same encoding/decoding standard, said multiplexed signals including digitally converted audio signals, different kinds of information and video signals corresponding to a plurality of video signal scanning methods, and for isolating and reproducing at least one signal from among said audio signals, said video signals and said different kinds of information, said unit comprising:

a demodulation means for tuning in a channel of a received signal and performing demodulation thereof;

a multiplex isolation means to isolate an audio signal, a video signal and other types of data coded from said multiplexed signals output from said demodulation means;

a decoding means to decode said audio signal and said video signal from said multiplex isolation means;

a plurality of video processing means for performing processing of said video signal from said decoding means, according to said plurality of video signal scanning methods;

an output selection means for selecting an output from said plurality of video processing means; and

a control means for determining a scanning method of said video signal of said channel, and for controlling said output selection means based on a determined said scanning method for said video signal.

13. A unit as claimed in claim **12**, wherein said scanning method is determined by analyzing information provided by said decoding means.

14. A unit as claimed in claim **12**, wherein said control means operates based on information isolated with said multiplex isolation means, such information being used for determining said scanning method of said channel.

15. A unit as claimed in claim 12, wherein signals according to said plurality of video signal scanning methods are output from a common output terminal.

16. A unit as claimed in claim 12, wherein signals according to said plurality of video signal scanning methods are sent from respective different output terminals.

17. A unit as claimed in claim 12, wherein an optical signal output means is provided to output an optical signal containing information designating a determined said scanning method of said video signal for said channel.

18. A unit as claimed in claim 12, wherein an electrical signal output means is provided to output an electrical signal containing information designating a determined said scanning method of said video signal for said channel.

19. A unit as claimed in claim 12, wherein a radio frequency signal output means is provided to output a radio frequency signal containing information designating a determined said scanning method of said video signal for said channel.

20. A unit as claimed in claim 12, further comprising a display means operable according to said plurality of video signal scanning methods, and wherein said control means switches a video signal scanning method for said display means based on a determined said scanning method of said video signal for said channel.

21. A unit as claimed in claim 12, wherein said control means is capable of stopping total or partial operation of said plurality of video processing means.

22. A unit as claimed in claim 12, wherein said output selection means is operable to receive any one of a plurality of outputs of said plurality of video processing means so as to connect a selected said output to a video output display terminal.

23. A unit as claimed in claim 12, wherein a scanning method of the video signal is derived from the information from the MPEG decoder and sent to a receiver as one of an infrared signal, a RF signal and an electrical signal, said signal containing information indicating the scanning method used to determine the video signal.

24. A digital broadcast receiver unit for receiving a digital multiplexed signal stream having multiplexed signals commonly encoded using a same encoding/decoding standard, said multiplexed signals including digitally converted audio signals, different kinds of information and video signals corresponding to at least two video signal scanning methods, and for isolating and reproducing at least one signal from among said audio signals, said video signals and said different kinds of information, said unit comprising:

a demodulation means for tuning in a channel of a received signal and performing demodulation thereof;

a multiplex isolation means to isolate an audio signal, a video signal and other types of data coded from said multiplexed signals output from said demodulation means;

a decoding means to decode said audio signal and said video signal from said multiplex isolation means;

a plurality of video processing means for performing processing of said video signal from said decoding means, according to said at least two video signal scanning methods;

a control means for determining a scanning method of said video signal of said channel, and for operating said plurality of video processing means based on a determined said scanning method for said video signal.

25. A unit as claimed in claim 24, further comprising:

a video output display selector controlled by said control means and operable to receive any one of a plurality of outputs of said plurality of video processing sections so as to connect a selected output to a video output display terminal.

26. A unit as claimed in claim 24, further comprising:

a plurality of video signal output terminals, each terminal providing connection to a differing output of said plurality of video processor sections.

27. A unit as claimed in claim 24, wherein a scanning method of the video signal is derived from the information from the MPEG decoder and sent to a receiver as one of an infrared signal, a RF signal and an electrical signal, said signal containing information indicating the scanning method used to determine the video signal.

* * * * *

EXHIBIT F

US007012769B2

(12) **United States Patent**
Arai et al.

(10) **Patent No.: US 7,012,769 B2**
(45) **Date of Patent: *Mar. 14, 2006**

(54) **DIGITAL INFORMATION RECORDING/REPRODUCING APPARATUS**

(75) Inventors: **Hideo Arai**, Chigasaki (JP); **Hitoaki Owashi**, Yokohama (JP); **Kyoichi Hosokawa**, Yokohama (JP); **Keizo Nishimura**, Yokosuka (JP); **Yoshizumi Watatani**, Fujisawa (JP); **Akira Shibata**, Katsuta (JP)

(73) Assignee: **Hitachi, Ltd.**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 167 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **10/404,452**

(22) Filed: **Apr. 2, 2003**

(65) **Prior Publication Data**

US 2003/0190156 A1 Oct. 9, 2003

Related U.S. Application Data

(60) Continuation of application No. 10/277,830, filed on Oct. 23, 2002, now Pat. No. 6,590,726, which is a continuation of application No. 09/809,047, filed on Mar. 16, 2001, now Pat. No. 6,498,691, which is a continuation of application No. 09/654,962, filed on Sep. 5, 2000, now Pat. No. 6,324,025, which is a continuation of application No. 09/567,005, filed on May 9, 2000, now Pat. No. 6,278,564, which is a continuation of application No. 09/326,595, filed on Jun. 7, 1999, now Pat. No. 6,069,757, which is a continuation of application No. 09/188,303, filed on Nov. 10, 1998, now Pat. No. 6,002,536, which is a continuation of application No. 08/917,176, filed on Aug. 25, 1997, now Pat. No. 5,862,004, which is a continuation of application No. 08/620,879, filed on Mar. 22, 1996, now Pat. No. 5,699,203, and a continuation of application No. 08/620,880, filed on Mar. 22, 1996, now Pat. No. 5,673,154, which is a continuation of application No. 08/457,597, filed on Jun. 1, 1995, now Pat. No. 5,530,598, which is a continuation of application No. 08/457,486, filed on Jun. 1, 1995, now Pat. No. 5,517,368, which is a continuation of application No. 08/238,528, filed on May 5, 1994, now Pat. No. 5,671,095, which is a division of application No. 07/727,059, filed on Jul. 8, 1991, now Pat. No. 5,337,199.

(30) **Foreign Application Priority Data**

Jul. 6, 1990 (JP) 02-177406
Jul. 20, 1990 (JP) 02-190655
Sep. 21, 1990 (JP) 02-250199

(51) **Int. Cl.**
G11B 5/00 (2006.01)

(52) **U.S. Cl.** **360/8**; 386/109

(58) **Field of Classification Search** 360/8, 360/27, 32, 39; 386/6, 7, 37, 33, 68, 84, 386/109, 112
See application file for complete search history.

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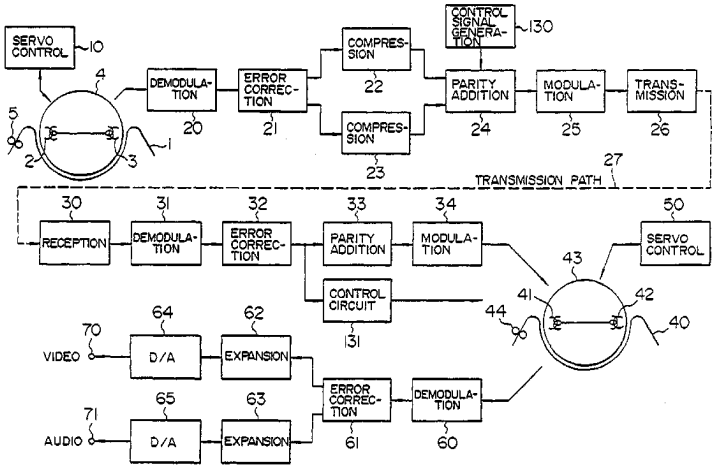

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Primary Examiner—Tan Dinh
(74) *Attorney, Agent, or Firm*—Antonelli, Terry, Stout and Kraus, LLP.

(57) **ABSTRACT**

An apparatus for at least receiving digital information including digital video information bit-compressed by a first compression system plus digital audio information bit-compressed by a second compression system and transmitted to a transmission path. The receiver apparatus includes a receiver which receives the transmitted digital information, a demodulator which demodulates the digital information received by the receiver, an error detector which detects an error of a digital information demodulated by the demodulator by use of a parity signal, a first expander which bit-expands video information among digital information error detected by the error detector corresponding to the first compression system and a second expander which bit-expands audio information among digital information error detected by the error detector corresponding to the second compression system.

9 Claims, 18 Drawing Sheets

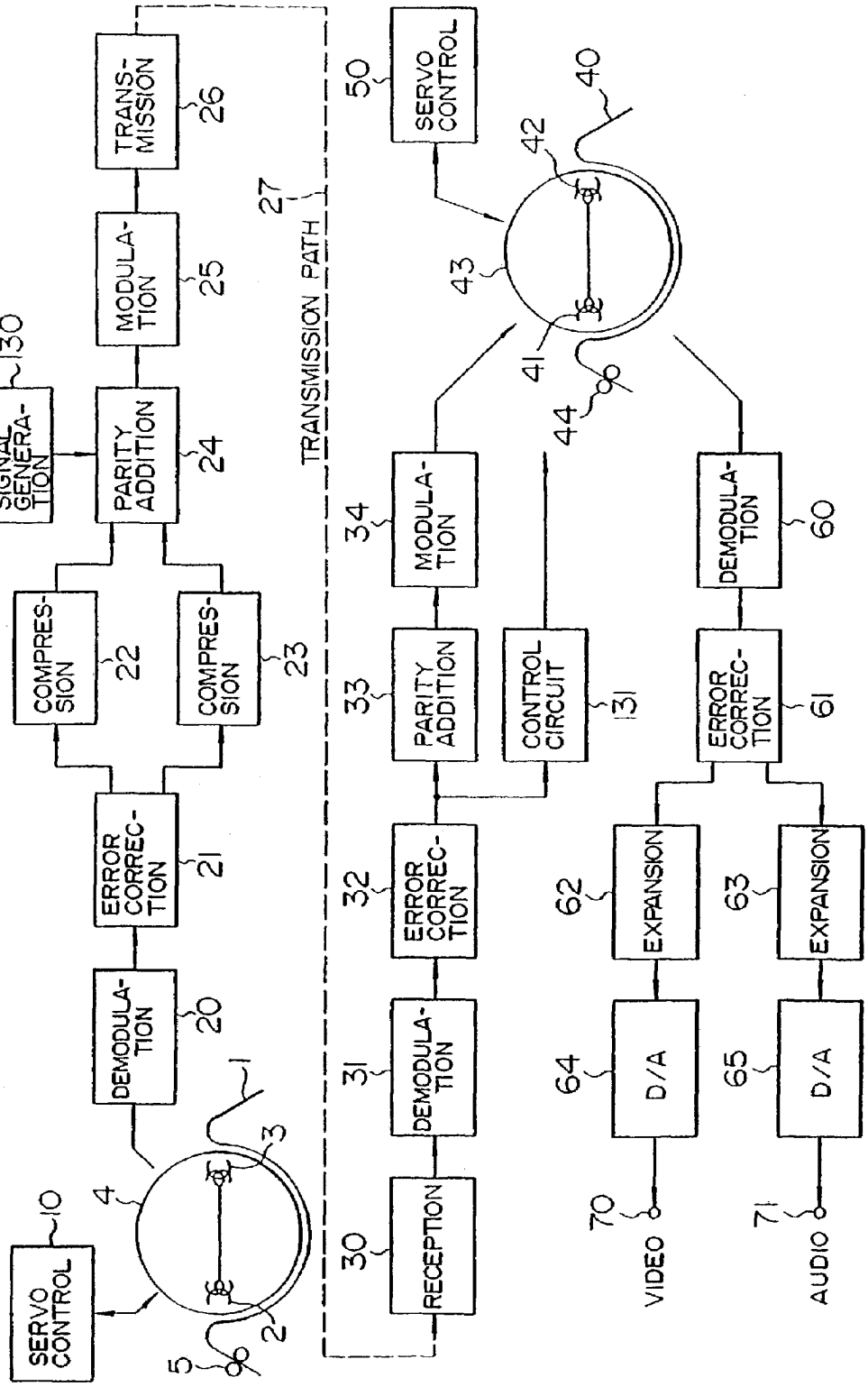

SERVO CONTROL
10
DEMODULA-TION
20
ERROR CORREC-TION
21
COMPRES-SION
22
COMPRES-SION
23
PARITY ADDITION
24
CONTROL SIGNAL GENERA-TION
130
MODULA-TION
25
TRANS-MISSION
26
TRANSMISSION PATH
27
RECEPTION
30
DEMODULA-TION
31
ERROR CORREC-TION
32
PARITY ADDITION
33
MODULA-TION
34
CONTROL CIRCUIT
131
SERVO CONTROL
50
DEMODULA-TION
60
ERROR CORREC-TION
61
EXPANSION
62
EXPANSION
63
D/A
64
D/A
65
VIDEO
70
AUDIO
71
1
2
3
4
5
40
41
42
43
44

FIG. 1

FIG. 2

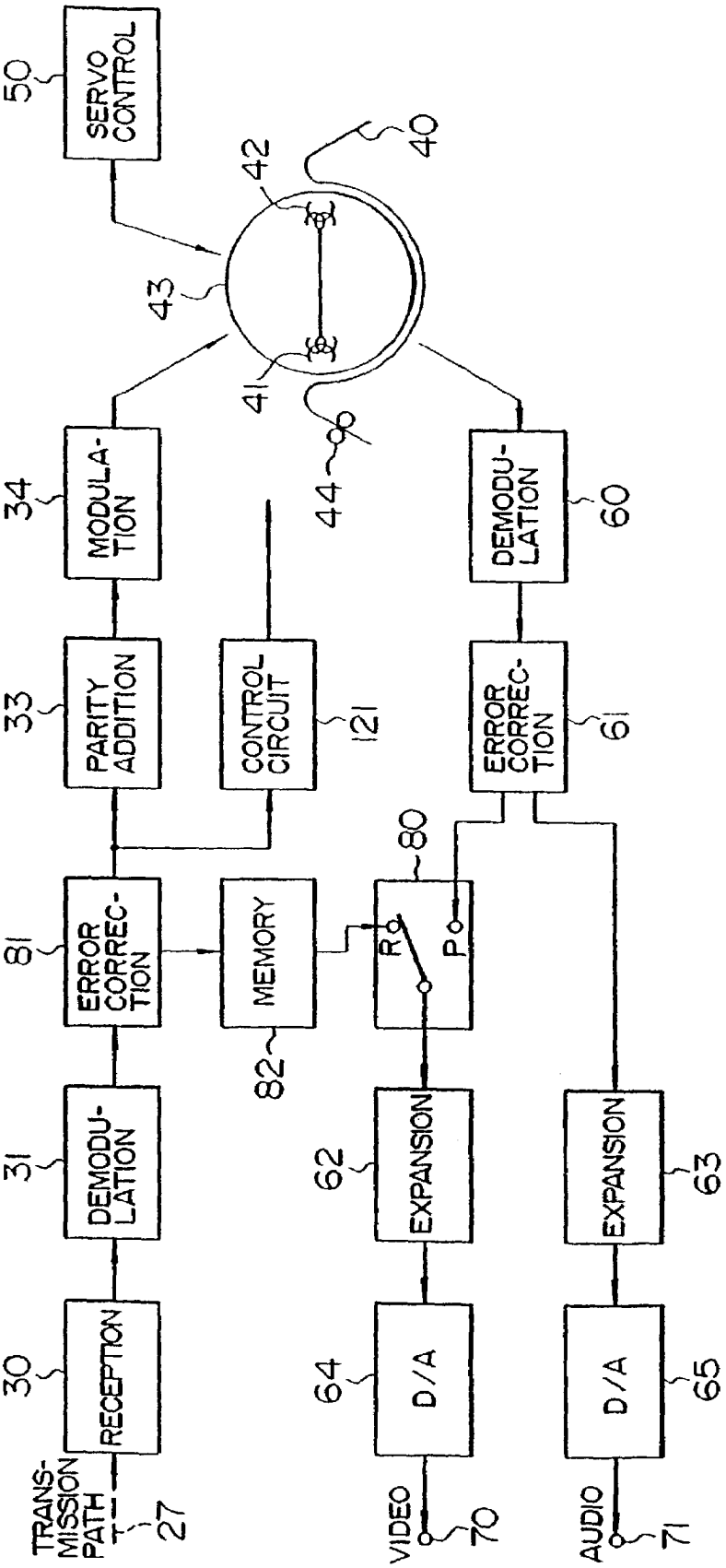

50
SERVO CONTROL
42
40
43
41
44
34
MODULA-TION
DEMODU-LATION
60
33
PARITY ADDITION
CONTROL CIRCUIT
121
ERROR CORREC-TION
61
80
81
ERROR CORREC-TION
MEMORY
R
P
82
31
DEMODU-LATION
62
EXPANSION
EXPANSION
63
30
RECEPTION
64
D/A
D/A
65
TRANS-MISSION PATH
27
VIDEO
70
AUDIO
71

FIG. 3

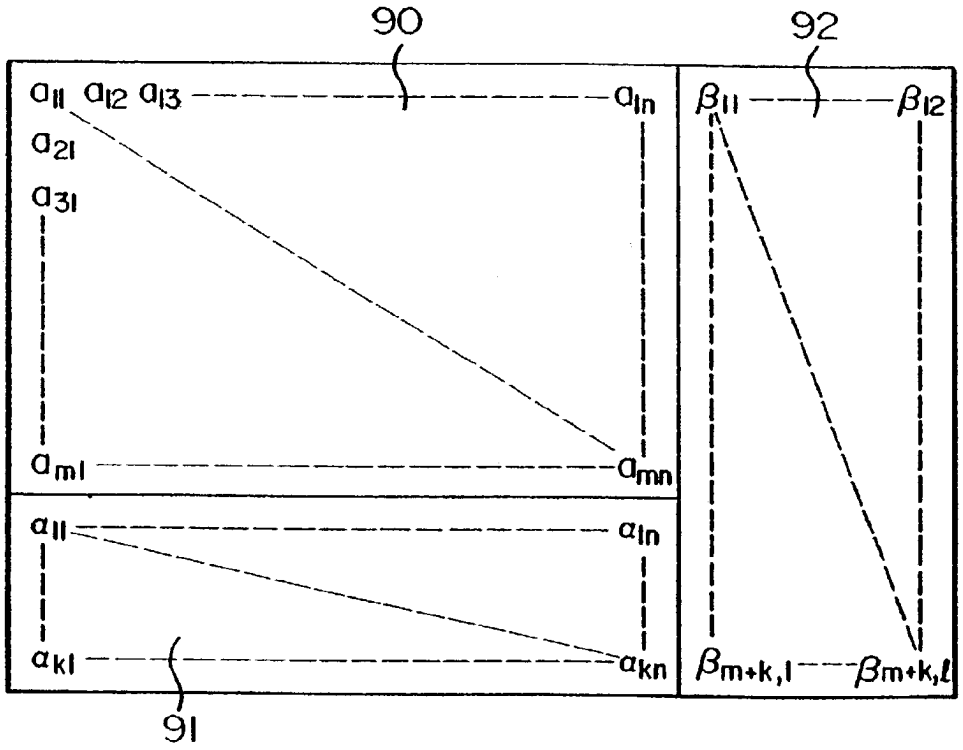
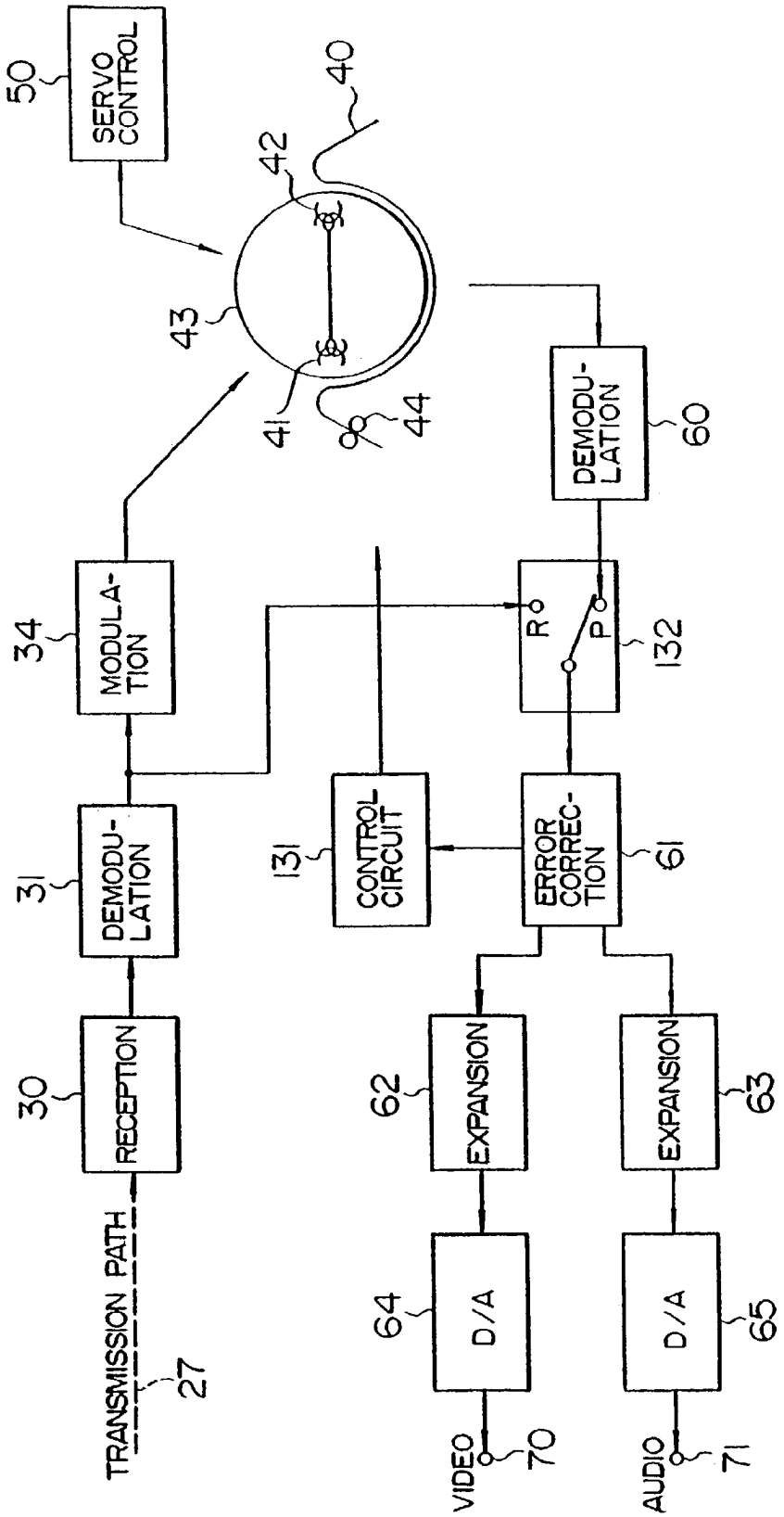

90
92
a_{11} a_{12} a_{13}
a_{1n}
a_{21}
a_{31}
a_{m1}
a_{mn}
β_{11}
β_{12}
a_{11}
a_{1n}
a_{k1}
a_{kn}
$\beta_{m+k,1}$
$\beta_{m+k,l}$
91

FIG. 4


50
SERVO CONTROL
40
42
43
41
44
DEMODU-LATION
60
34
MODULA-TION
R
P
132
31
DEMODU-LATION
131
CONTROL CIRCUIT
ERROR CORREC-TION
61
30
RECEPTION
62
EXPANSION
63
EXPANSION
TRANSMISSION PATH
27
64
D/A
65
D/A
VIDEO
70
AUDIO
71

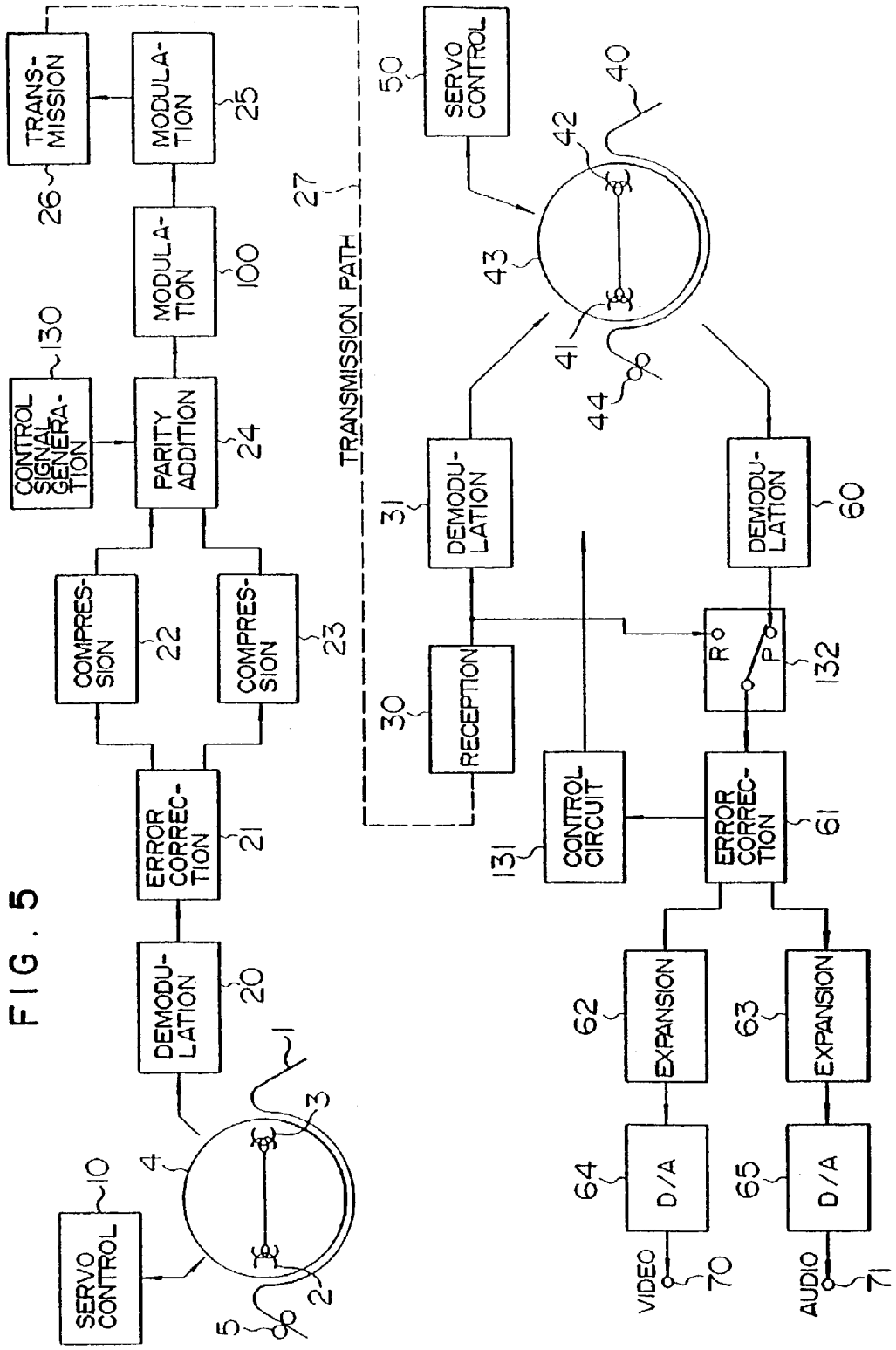

TRANS-MISSION
26
MODULA-TION
25
MODULA-TION
100
CONTROL SIGNAL GENERA-TION
130
PARITY ADDITION
24
COMPRES-SION
22
COMPRES-SION
23
ERROR CORREC-TION
21
DEMODU-LATION
20
SERVO CONTROL
10
TRANSMISSION PATH
27
SERVO CONTROL
50
DEMODU-LATION
31
RECEPTION
30
DEMODU-LATION
60
CONTROL CIRCUIT
131
ERROR CORREC-TION
61
EXPANSION
62
EXPANSION
63
D/A
64
D/A
65
VIDEO
70
AUDIO
71
R
P
132
40
41
42
43
44
1
2
3
4
5

FIG. 5

FIG. 6

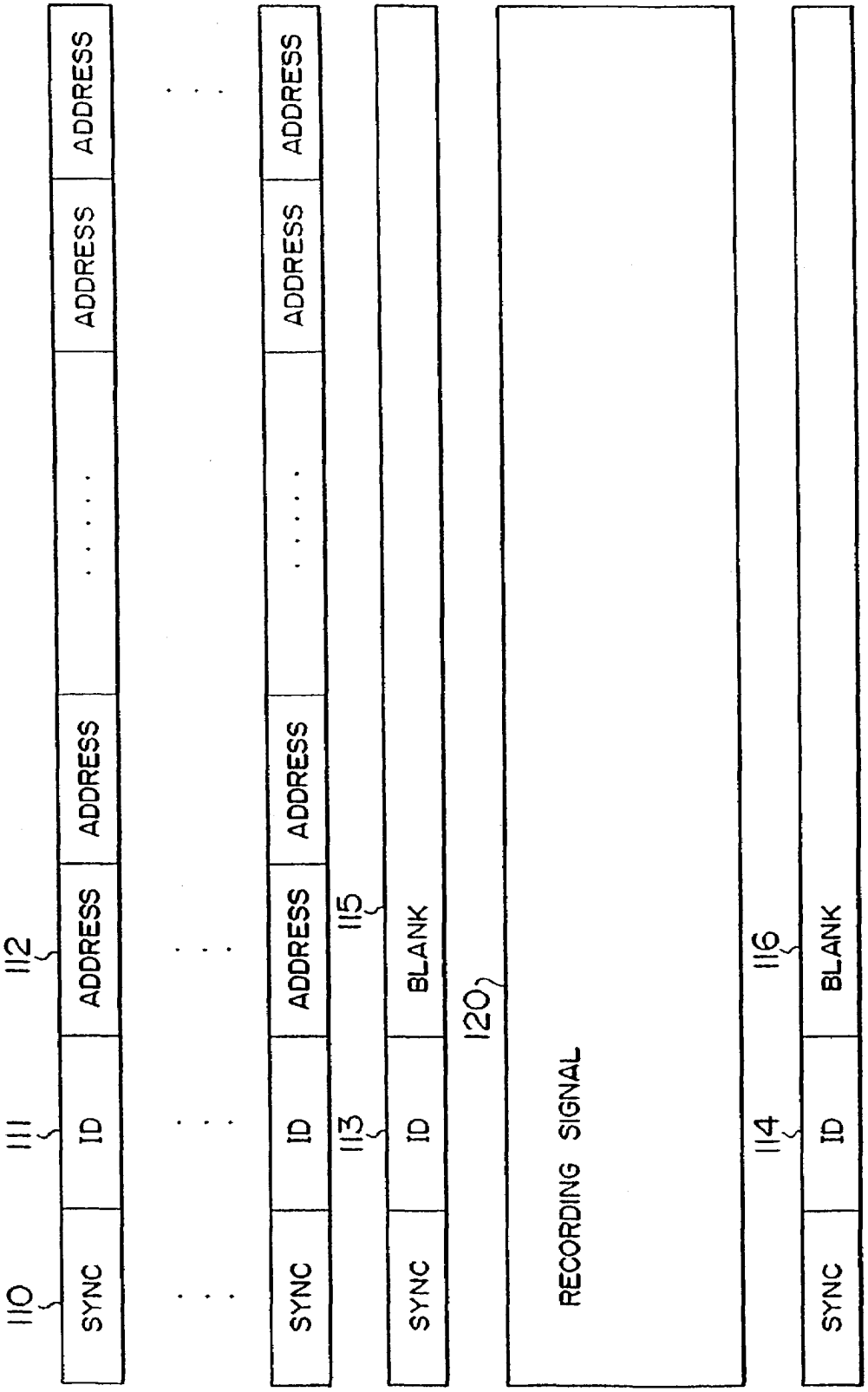

110
111
112
113
114
115
116
120
SYNC
ID
ADDRESS
BLANK
RECORDING SIGNAL

FIG. 7

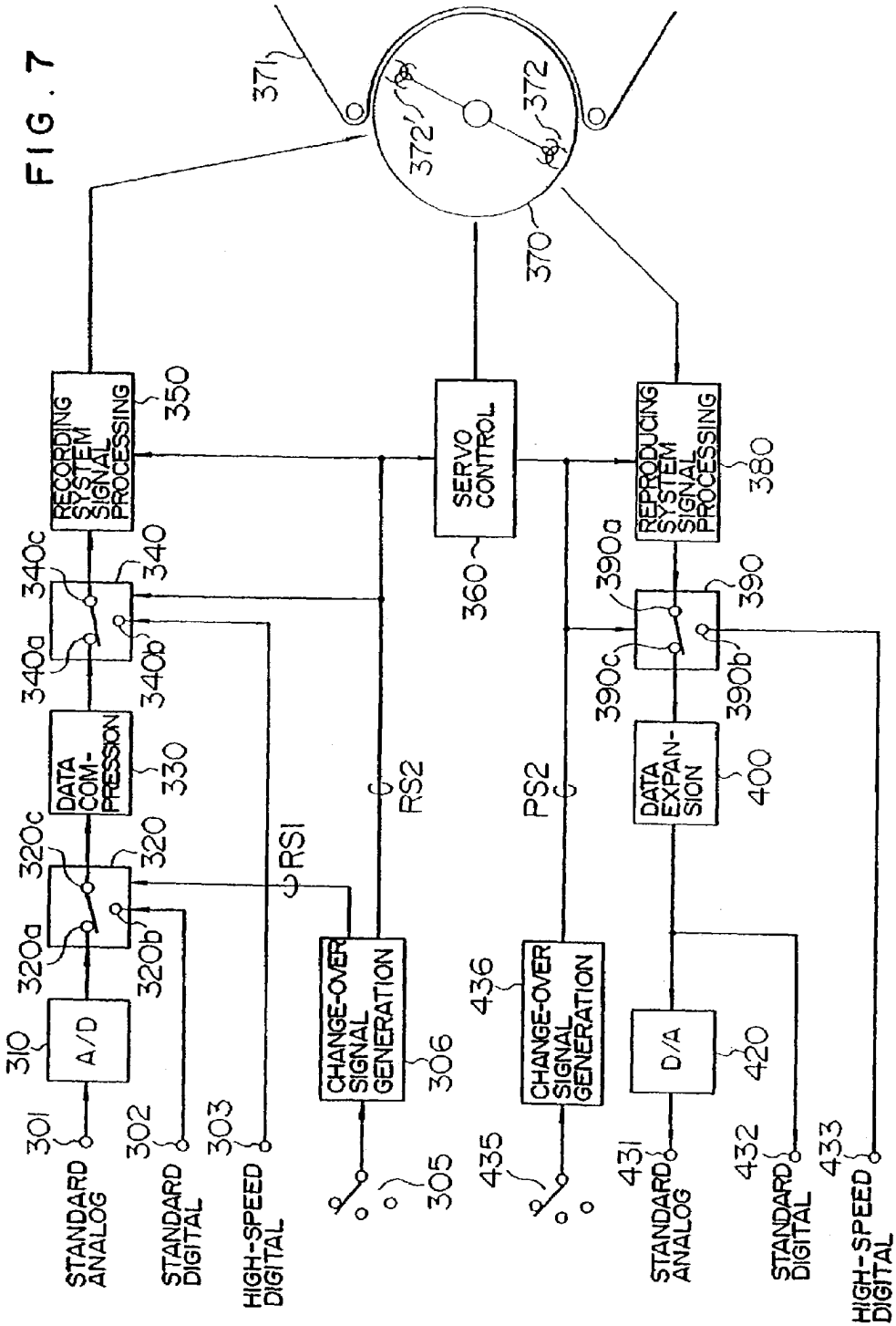

371
372
372'
370
RECORDING SYSTEM SIGNAL PROCESSING
350
SERVO CONTROL
360
REPRODUCING SYSTEM SIGNAL PROCESSING
380
340c
340
340a
340b
DATA COM-PRESSION
330
320c
320
320a
320b
A/D
310
301
302
303
RS1
RS2
CHANGE-OVER SIGNAL GENERATION
306
305
STANDARD ANALOG
STANDARD DIGITAL
HIGH-SPEED DIGITAL
390a
390
390c
390b
PS2
DATA EXPAN-SION
400
436
CHANGE-OVER SIGNAL GENERATION
435
D/A
420
431
432
433
STANDARD ANALOG
STANDARD DIGITAL
HIGH-SPEED DIGITAL

FIG. 8

ITEM / INPUT		FIELD FREQUENCY	TRANSMISSION RATE	DATA COMPRESSION	TIME-BASE COMPRESSION
STANDARD SPEED	ANALOG	59.94 Hz	(AFTER A/D) 114 Mbps	ABSENCE	ABSENCE
	DIGITAL		114 Mbps		
HIGH SPEED	DIGITAL	59.94 Hz	100 Mbps	PRESENCE 1/11.4	PRESENCE 1/10

FIG. 9

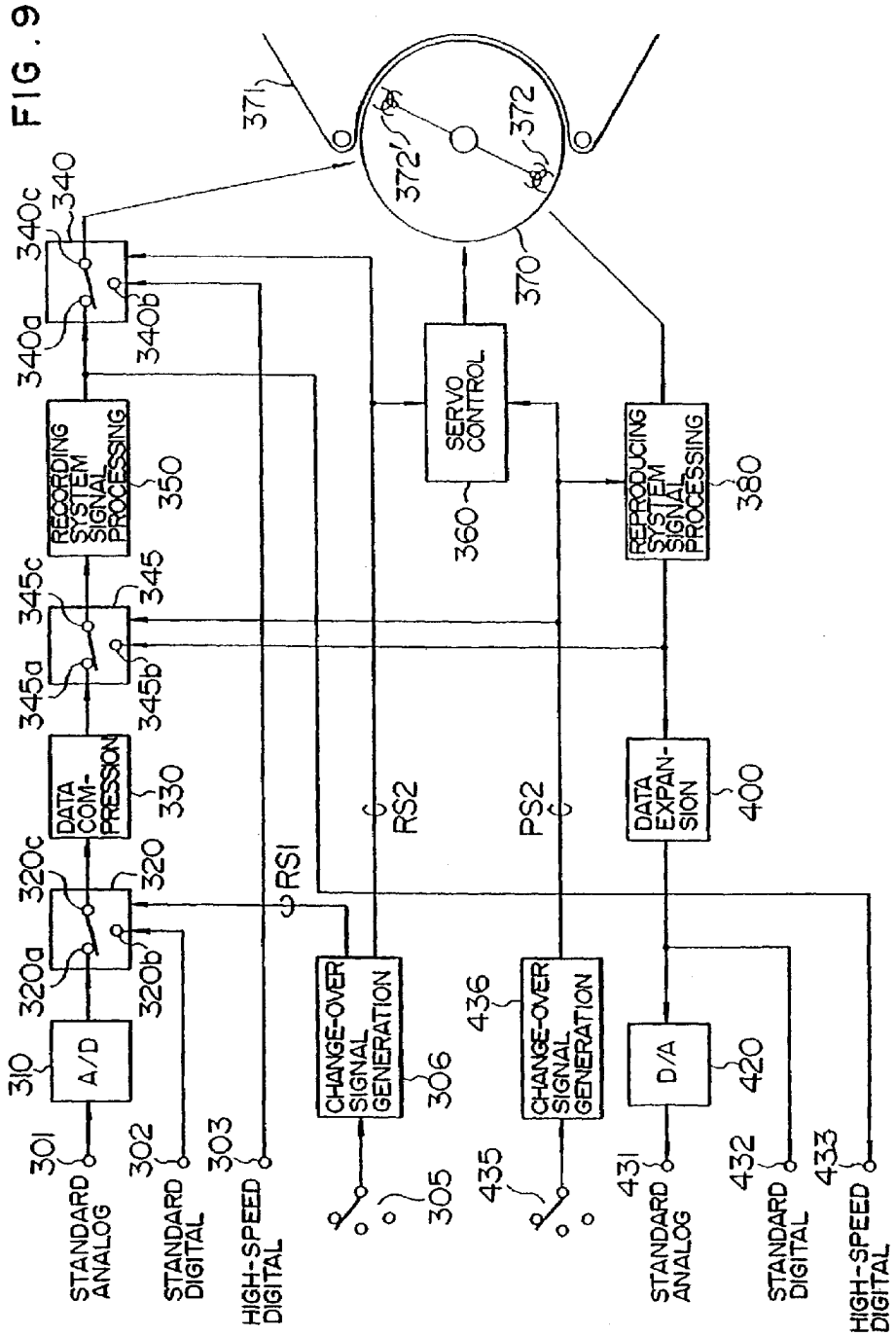

371
372
372'
370
340
340c
340a
340b
SERVO CONTROL
360
RECORDING SYSTEM SIGNAL PROCESSING
350
REPRODUCING SYSTEM SIGNAL PROCESSING
380
345c
345
345a
345b
DATA COM-PRESSION
330
DATA EXPAN-SION
400
320c
320
320a
320b
RS1
RS2
PS2
A/D
310
CHANGE-OVER SIGNAL GENERATION
306
436
D/A
420
301
302
303
305
435
431
432
433
STANDARD ANALOG
STANDARD DIGITAL
HIGH-SPEED DIGITAL
STANDARD ANALOG
STANDARD DIGITAL
HIGH-SPEED DIGITAL

FIG. 10

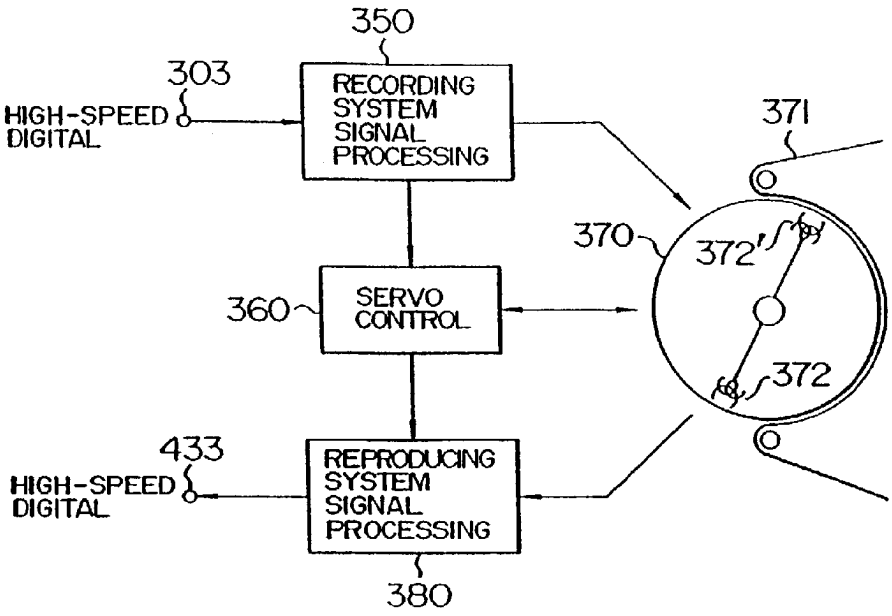

350
303
HIGH-SPEED DIGITAL
RECORDING SYSTEM SIGNAL PROCESSING
371
370
372'
360
SERVO CONTROL
372
433
HIGH-SPEED DIGITAL
REPRODUCING SYSTEM SIGNAL PROCESSING
380

FIG. 11

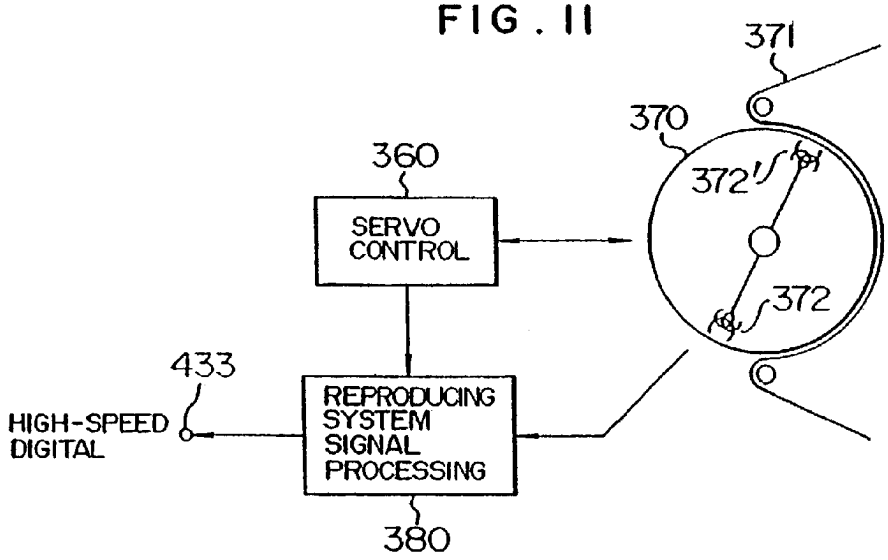

371
370
372'
360
SERVO CONTROL
372
433
HIGH-SPEED DIGITAL
REPRODUCING SYSTEM SIGNAL PROCESSING
380

FIG. 12

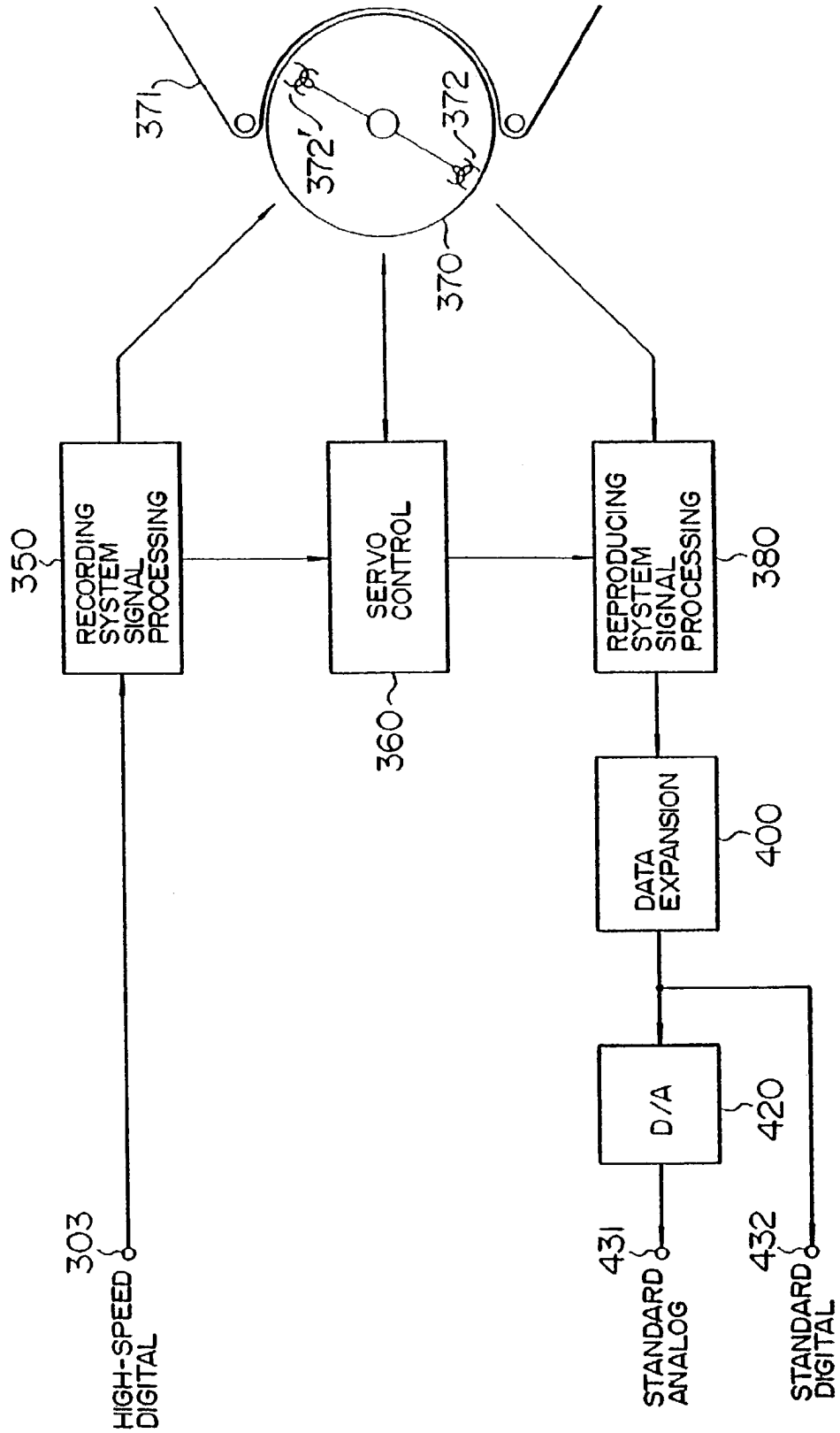

371
372'
372
370
350
RECORDING SYSTEM SIGNAL PROCESSING
SERVO CONTROL
360
REPRODUCING SYSTEM SIGNAL PROCESSING
380
DATA EXPANSION
400
D/A
420
303
HIGH-SPEED DIGITAL
431
STANDARD ANALOG
432
STANDARD DIGITAL

FIG. 13

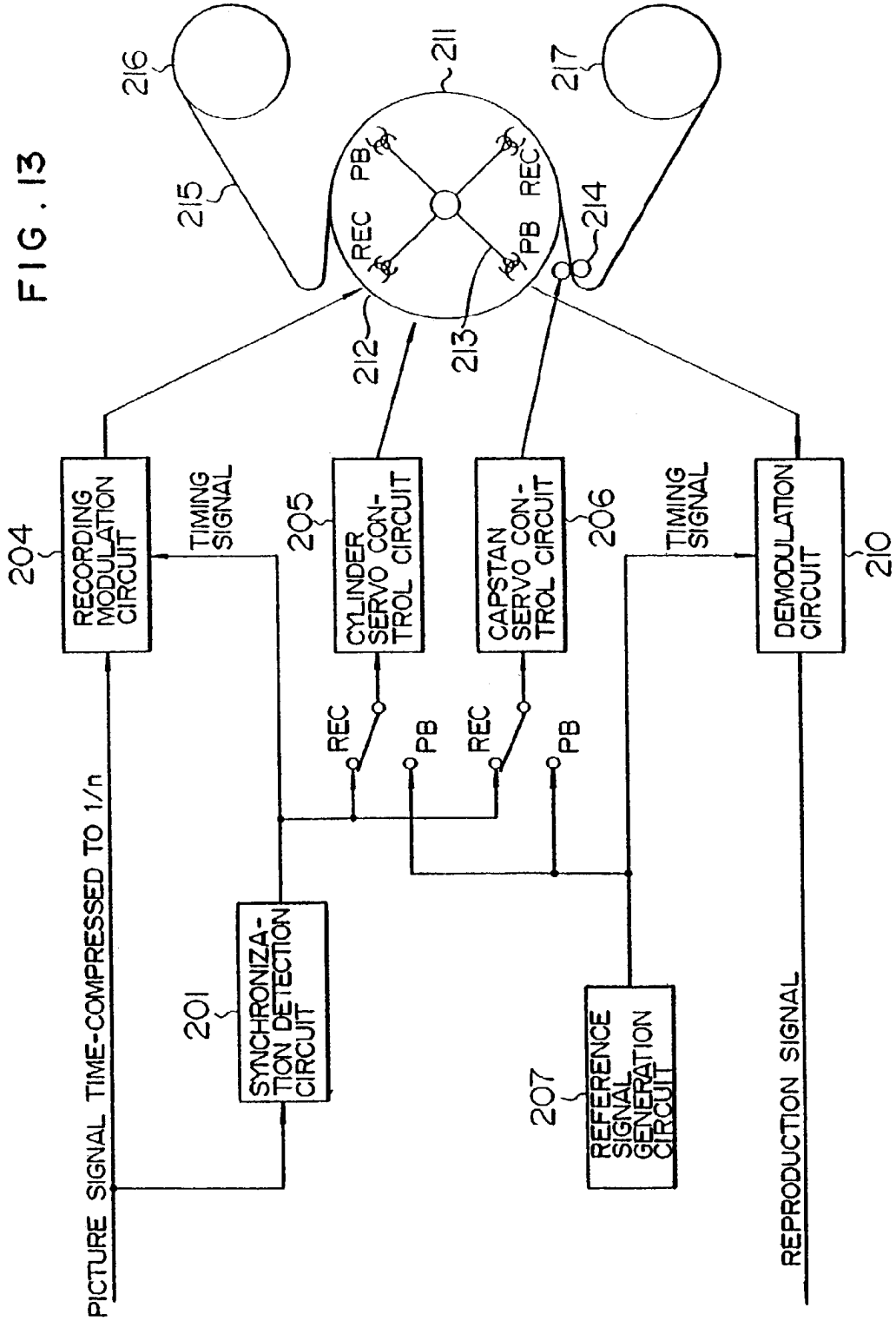

216
211
217
215
REC PB
PB REC
214
212
213
204
RECORDING MODULATION CIRCUIT
TIMING SIGNAL
205
CYLINDER SERVO CONTROL CIRCUIT
CAPSTAN SERVO CONTROL CIRCUIT
206
TIMING SIGNAL
DEMODULATION CIRCUIT
210
REC
PB
REC
PB
PICTURE SIGNAL TIME-COMPRESSED TO 1/n
201
SYNCHRONIZATION DETECTION CIRCUIT
207
REFERENCE SIGNAL GENERATION CIRCUIT
REPRODUCTION SIGNAL

FIG. 14

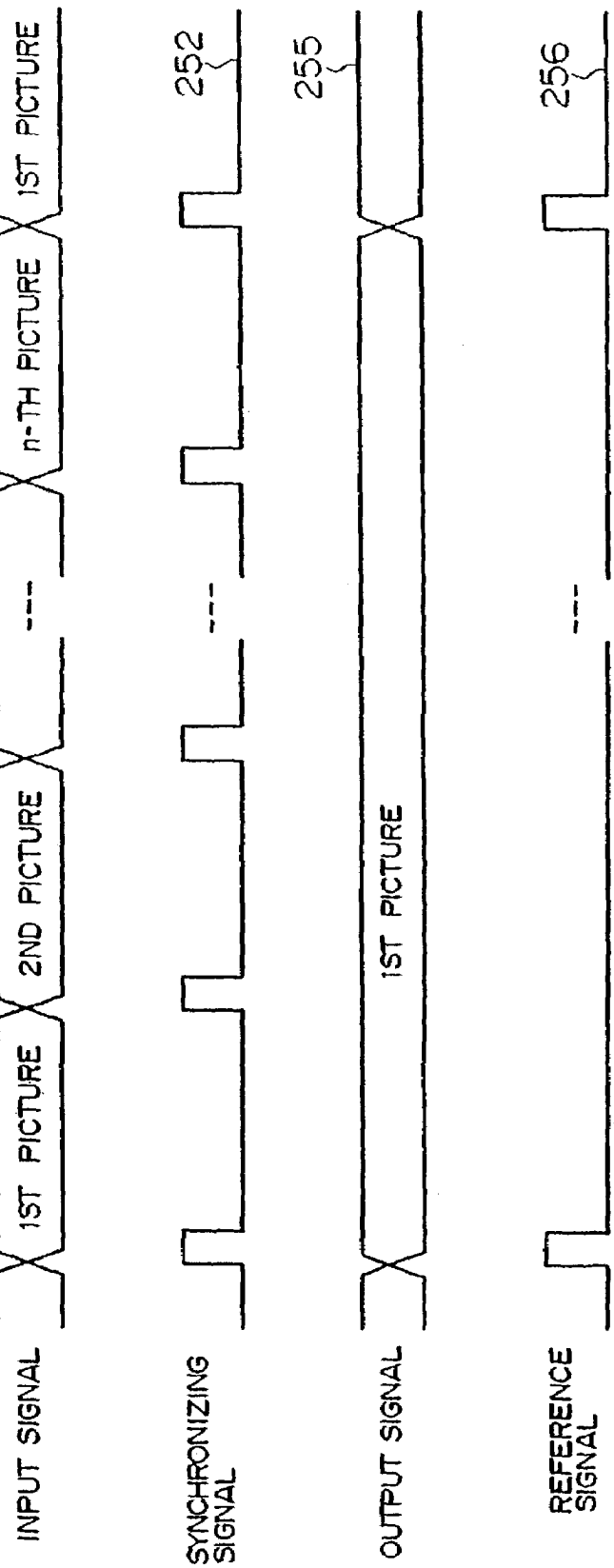

251
252
255
256
1ST PICTURE
2ND PICTURE
---
n-TH PICTURE
1ST PICTURE
INPUT SIGNAL
SYNCHRONIZING SIGNAL
OUTPUT SIGNAL
REFERENCE SIGNAL

FIG. 15

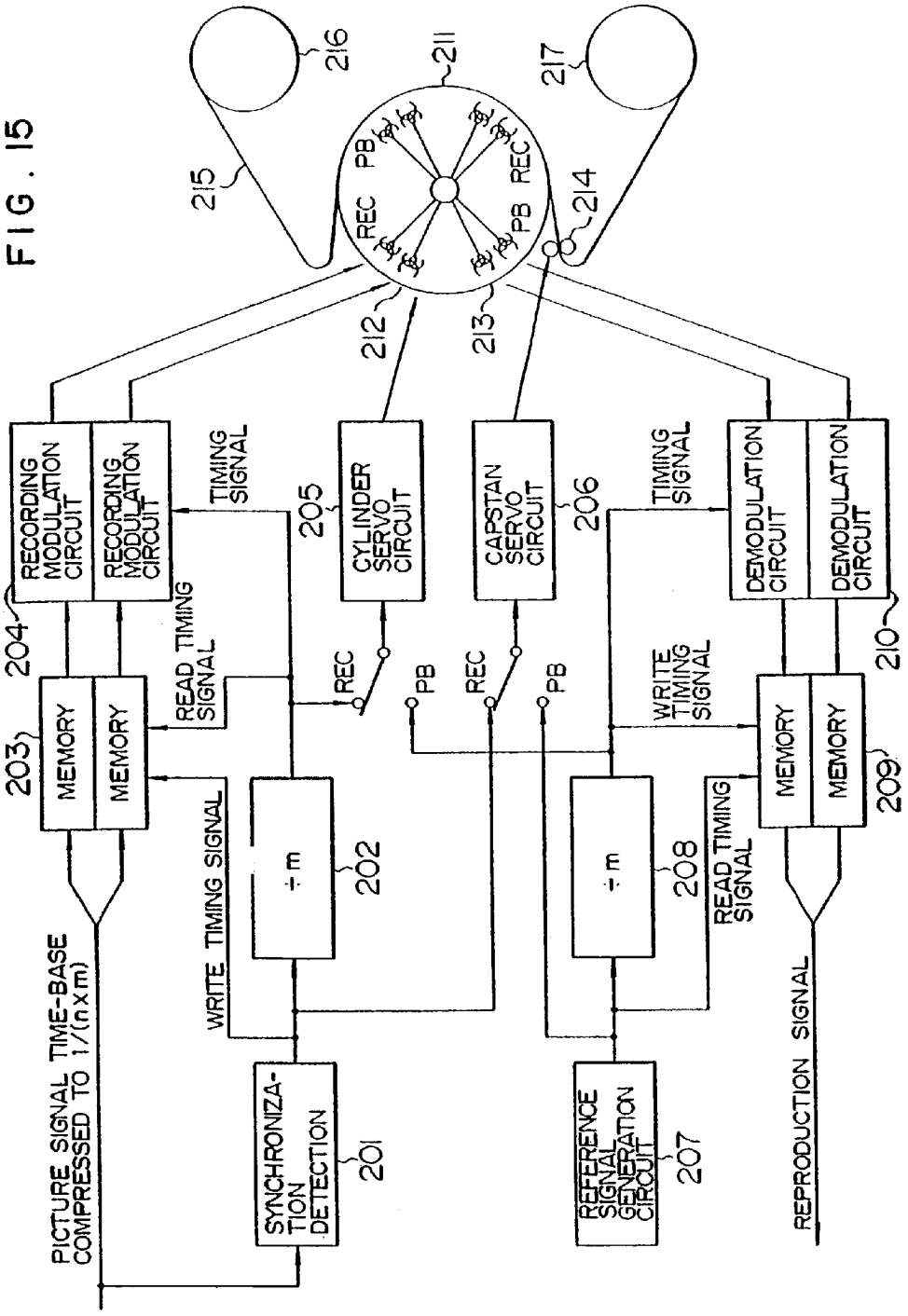

216
211
217
215
PB
REC
REC
PB
214
212
213
RECORDING MODULATION CIRCUIT
RECORDING MODULATION CIRCUIT
TIMING SIGNAL
205
CYLINDER SERVO CIRCUIT
CAPSTAN SERVO CIRCUIT
206
TIMING SIGNAL
DEMODULATION CIRCUIT
DEMODULATION CIRCUIT
204
READ TIMING SIGNAL
REC
PB
REC
PB
WRITE TIMING SIGNAL
210
203
MEMORY
MEMORY
WRITE TIMING SIGNAL
÷m
202
÷m
208
READ TIMING SIGNAL
MEMORY
MEMORY
209
PICTURE SIGNAL TIME-BASE COMPRESSED TO 1/(n x m)
SYNCHRONIZATION DETECTION
201
REFERENCE SIGNAL GENERATION CIRCUIT
207
REPRODUCTION SIGNAL

FIG. 16

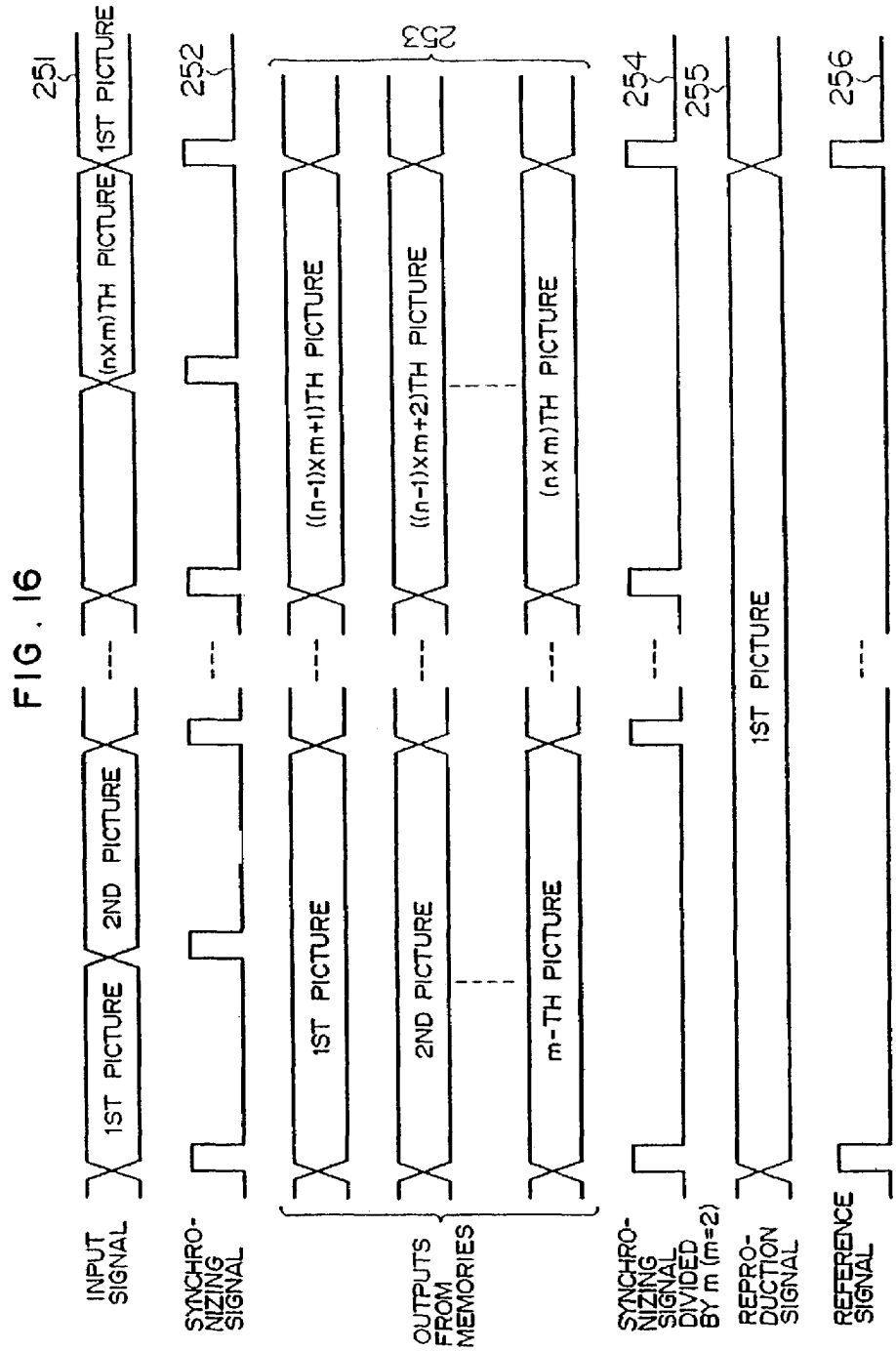
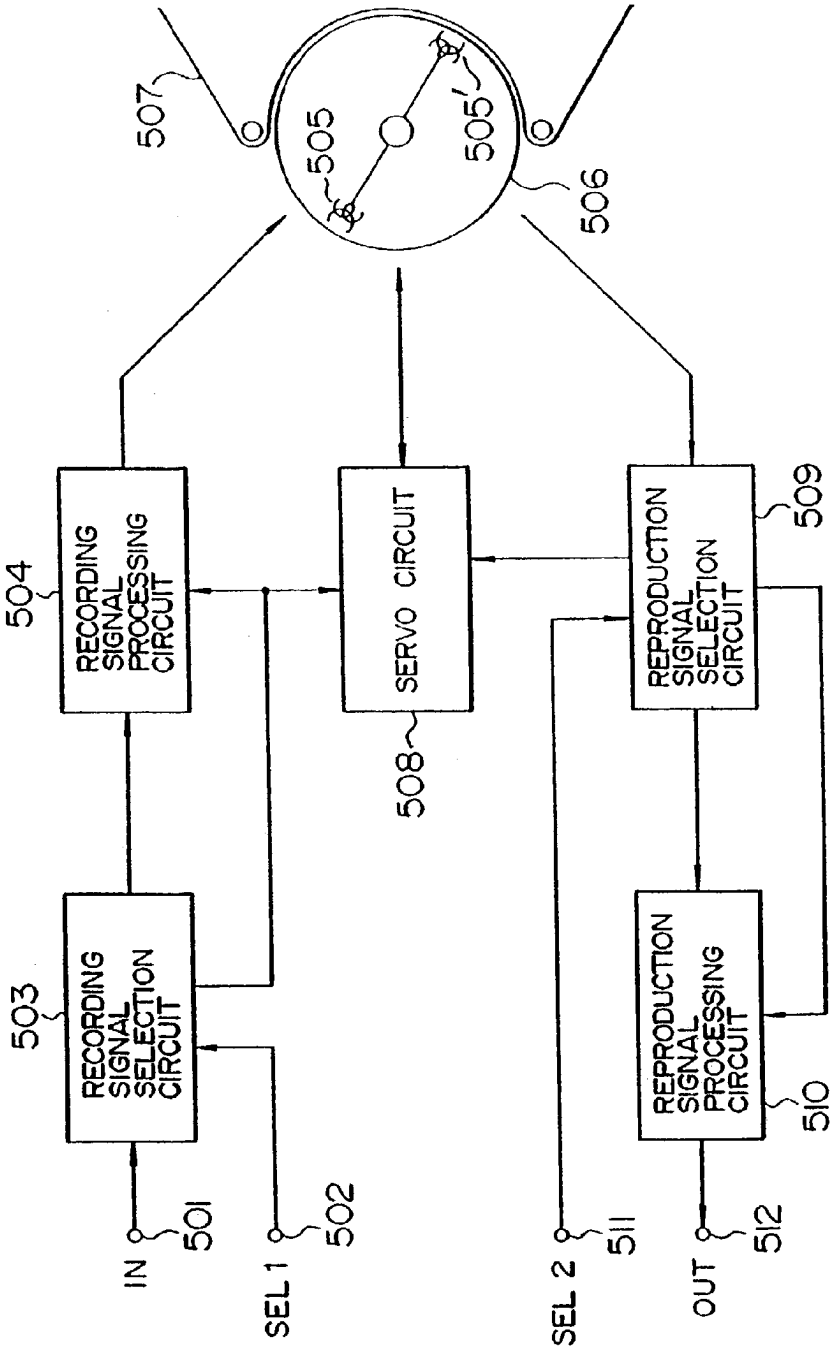

251
252
253
254
255
256
INPUT SIGNAL
SYNCHRO-NIZING SIGNAL
OUTPUTS FROM MEMORIES
SYNCHRO-NIZING SIGNAL DIVIDED BY m (m=2)
REPRO-DUCTION SIGNAL
REFERENCE SIGNAL
1ST PICTURE
2ND PICTURE
(nXm)TH PICTURE
((n-1)Xm+1)TH PICTURE
((n-1)Xm+2)TH PICTURE
m-TH PICTURE

FIG. 17

SYSTEM	MODE		TAPE SPEED (RATIO TO STANDARD SPEED)		CYLINDER ROTATION SPEED (rpm)		NUMBER OF HEAD PAIRS		CYLINDER DIAMETER (mmφ)	CYLINDER CONTACT ANGLE (deg)	NUMBER OF TRACKS REQUIRED FOR ONE PICTURE	REMARKS
	REC	PB	REC	PB	REC	PB	REC	PB				
VHS (NTSC)	NORMAL SPEED	NORMAL SPEED	1	1	1800	1800	1	1	62	180	1	
D2 (NTSC)	NORMAL SPEED	NORMAL SPEED	1	1	5400	5400	2	2	96	180	6	
EXAMPLE ①	HIGH SPEED	NORMAL SPEED	10	1	9000	900	1	1	120	180	1/2	
	HIGH SPEED	HIGH SPEED	10	10	9000	9000						
	NORMAL SPEED	HIGH SPEED	1	10	900	9000						
	HIGH SPEED	NORMAL SPEED	10	1	9000	900						
EXAMPLE ②	HIGH SPEED	HIGH SPEED	10	10	9000	9000	1	1	90	270	1/2	
	NORMAL SPEED	HIGH SPEED	1	10	900	9000						
	HIGH SPEED	NORMAL SPEED	10	1	18000	1800						
EXAMPLE ③	HIGH SPEED	HIGH SPEED	10	10	18000	18000	1	1	60	180	1	
	NORMAL SPEED	HIGH SPEED	1	10	1800	18000						
	HIGH SPEED	NORMAL SPEED	10	1	9000	900						
EXAMPLE ④	HIGH SPEED	HIGH SPEED	10	10	9000	9000	2	2	60	180	1	
	NORMAL SPEED	HIGH SPEED	1	10	900	9000						
	HIGH SPEED	NORMAL SPEED	10	1	9000	1800	2	1				
EXAMPLE ⑤	HIGH SPEED	HIGH SPEED	10	10	9000	9000	2	2	60	180	1	MOVABLE HEADS ARE REQUIRED
	NORMAL SPEED	HIGH SPEED	1	10	1800	9000	1	2				

FIG. 18


507
505
505'
506
504
RECORDING SIGNAL PROCESSING CIRCUIT
SERVO CIRCUIT
508
REPRODUCTION SIGNAL SELECTION CIRCUIT
509
503
RECORDING SIGNAL SELECTION CIRCUIT
REPRODUCTION SIGNAL PROCESSING CIRCUIT
510
IN
501
SEL 1
502
SEL 2
511
OUT
512

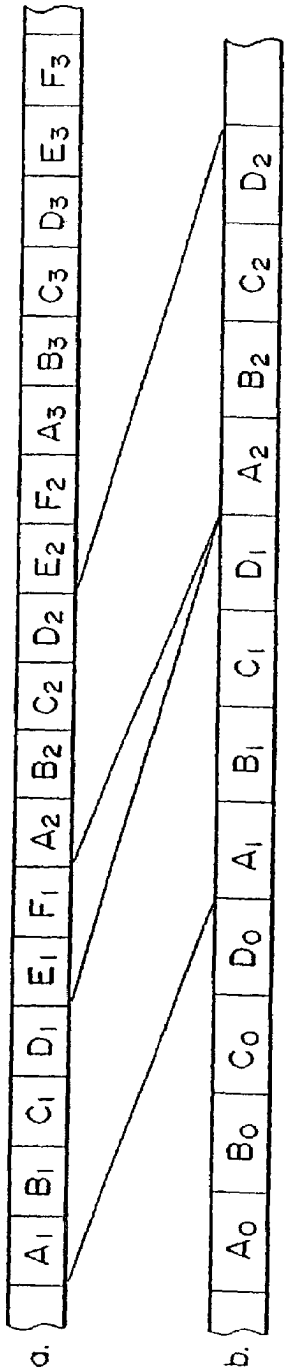

A1 B1 C1 D1 E1 F1 A2 B2 C2 D2 E2 F2 A3 B3 C3 D3 E3 F3
a.
A0 B0 C0 D0 A1 B1 C1 D1 A2 B2 C2 D2
b.

FIG. 19

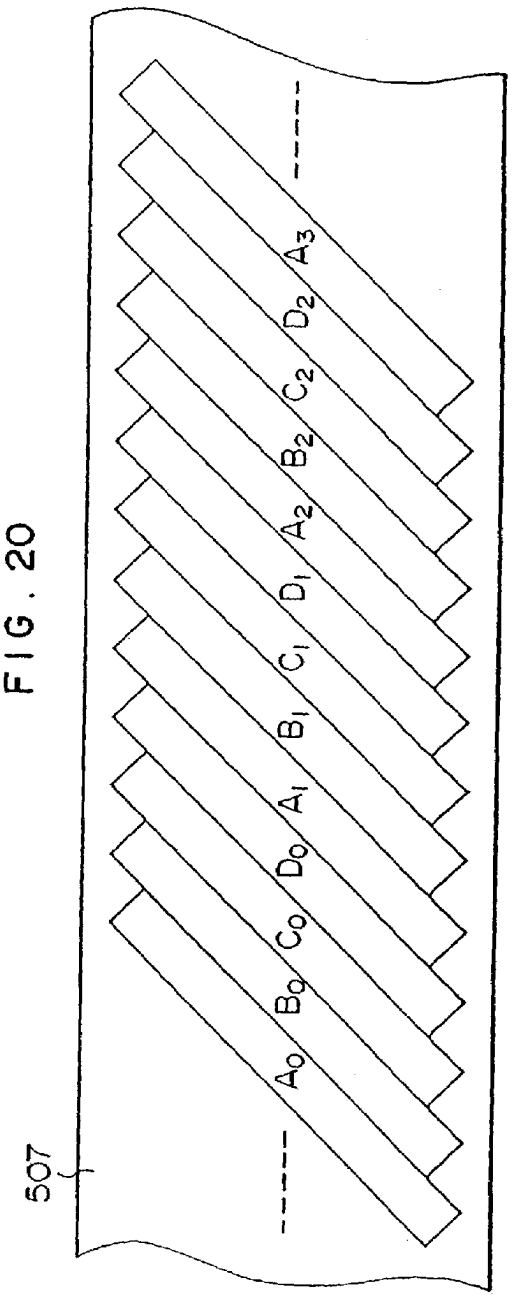

507
A0 B0 C0 D0 A1 B1 C1 D1 A2 B2 C2 D2 A3

FIG. 20

DIGITAL INFORMATION RECORDING/REPRODUCING APPARATUS

CROSS REFERENCE TO RELATED APPLICATIONS

This is a continuation application of U.S. application Ser. No. 10/277,830, filed Oct. 23, 2002, now U.S. Pat. No. 6,590,726, which is a continuation of U.S. Ser. No. 09/809,047, filed Mar. 16, 2001, now U.S. Pat. No. 6,498,691,which is a continuation application of U.S. application Ser. No. 09/654,962, filed Sep. 5, 2000, now U.S. Pat. No. 6,324,025, which is a continuation of U.S. Ser. No. 09/567,005, filed May 9, 2000, now U.S. Pat. No. 6,278,564, which is a continuation application of U.S. Ser. No. 09/326,595, filed Jun. 7,1999, now U.S. Pat. No. 6,069,757, which is a continuation of U.S. application Ser. No. 09/188,303, filed Nov. 10, 1998, now U.S. Pat. No. 6,002,536, which is a continuation of U.S. application Ser. No. 08/917,176, filed Aug. 25, 1997, now U.S. Pat. No. 5,862,004, which is a continuation of U.S. application Ser. No. 08/620,879, filed Mar. 22, 1996, now U.S. Pat. No. 5,699,203, and U.S. application Ser. No. 08/620,880, filed Mar. 22, 1996, now U.S. Pat. No. 5,673,154, which are continuations of U.S. application Ser. No. 08/457,597, filed Jun. 1, 1995, now U.S. Pat. No. 5,530,598, which is a continuation of U.S. application Ser. No. 08/457,486, filed Jun. 1, 1995, now U.S. Pat. No. 5,517,368, which is a continuation of U.S. application Ser. No. 08/238,528, filed May 5, 1994, now U.S. Pat. No. 5,671,095, which is a divisional of U.S. application Ser. No. 07/727,059, filed Jul. 8, 1991, now U.S. Pat. No. 5,337,199, the subject matter of which are incorporated by reference herein.

BACKGROUND OF THE INVENTION

The present invention relates to a system for transmitting a digital video signal and recording the received video signal. More particularly, the present invention relates to great extension of the range of use of a digital signal recording/reproducing system by greatly shortening a recording time through transmission of a video signal in a compressed form, and further relates to great extension of the range of use of a digital signal recording/reproducing system by making the number of signals to be recorded and a recording/reproducing time variable.

As a digital magnetic recording/reproducing system (hereinafter referred to as VTR) is conventionally known, for example, a D2 format VTR. In such a conventional digital VTR, the elongation or shortening of a reproducing time is possible by using variable-speed reproduction. However, the prior art reference does not at all disclose high-speed recording in which a recording time is shortened to 1/m, multiple recording in which a plurality of signals are recorded, and the compression/expansion of a recording/reproducing time.

The above-mentioned conventional digital VTR has a feature that a high quality is attained and there is no deterioration caused by dubbing. However, the shortening of a dubbing time is not taken into consideration. Therefore, for example, in the case where a two-hour program is to be recorded, two hours are required. Thus, there is a drawback that inconveniences are encountered in use. Also, the multiplexing of recording signals is not taken into consideration. Therefore, for example, when two kinds of programs are to be simultaneously recorded or reproduced, two VTR's are required. This also causes inconveniences in use.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a digital VTR in which high-speed recording onto a tape can be made with the same format as that used in standard-speed recording, to provide a transmission signal processing system for transmitting at a high speed a video signal to be recorded by such a digital VTR, and to extend the range of use of the digital VTR by shortening a recording time. For example, the digital VTR can be used in such a manner that a two-hour program is recorded in about ten minutes and is reproduced at a standard speed.

The above object is achieved as follows. A video signal and an audio signal are subjected to time-base compression to 1/m, bit compression to 1/n, addition of a parity signal and modulation, and are thereafter transmitted or outputted. The transmitted signal is received, is subjected to demodulation, error correction, addition of a parity signal and modulation, and is thereafter recorded, onto a magnetic tape which travels at a travel speed m times as high as that upon normal reproduction, by use of a magnetic head on a cylinder which rotates at a frequency m times as high as that upon normal reproduction. The signal on the magnetic tape traveling at a travel speed upon normal reproduction is reproduced by a magnetic head on the cylinder which rotates at a frequency upon normal reproduction. The reproduced signal is subjected to demodulation, error correction, bit expansion of video and audio signals and D/A conversion, and is thereafter outputted. Address signals corresponding to a plurality of VTR's may be transmitted prior to a signal to be recorded. Further, control signals indicative of the start of recording and the stop of recording may be transmitted. The transmitted signals are received and error-corrected, and controls of the standby for recording, the start of recording and the stop of recording are made on the basis of the control signals.

With the above construction, since the video signal and the audio signal are time-base compressed to 1/m and bit-compressed to 1/n, a transmission time is shortened to 1/m and a signal band turns to m/n. The time-base compressed and bit-compressed signal is transmitted after addition of a parity signal for error correction and modulation to a code adapted for a transmission path. The transmitted signal is received and demodulated. The detection of an error produced in a transmitting system and the correction for the error can be made using the added parity signal. The error-corrected signal is added with a parity signal for correction for an error produced in a magnetic recording/reproducing system and is modulated to a code adapted for the magnetic recording/reproducing system. Upon recording, since the rotation frequency of the cylinder and the travel speed of the magnetic tape are increased by m times, the recording onto the magnetic tape can be made at an m-tuple speed. Upon reproduction, by setting the rotation frequency of the cylinder and the travel speed of the magnetic tape to normal ones, the reproduction at a normal speed can be made. The reproduced signal is code-demodulated. The detection of an error produced in the magnetic recording/reproducing system and the correction for the error can be made on the basis of the parity signal. By bit-expanding the video signal and the audio signal compressed by the transmission signal processing system, the original video and audio signal can be restored. The bit-expanded signal is converted into an analog signal by a D/A converter. Simultaneous and selective control of the start/stop of recording for a multiplicity of VTR's can be made in such a manner that the address signals corresponding to the VTR's are transmitted prior to a signal to be recorded, the correction for

an error of the received signal is made, required VTR's are brought into recording standby conditions by the corrected address signals, and the controls of the start of recording and the stop of recording are made by the transmitted control signals.

Another object of the present invention is to provide a digital signal recording/reproducing system in which multiple recording onto a tape can be made with the same format as that used in standard recording and simultaneous multiple reproduction is possible, and to extend the range of use of a digital VTR by compressing/expanding a recording/reproducing time in accordance with the transmission rate of a multiplexed input/output signal and the number of signals in the multiplexed input/output signal.

This object is achieved as follows. There are provided means for selecting one or plural desired signals from a time-base compressed and time-division multiplexed digital input signal, and helical scan recording means for making time-division multiplex recording of the selected signals with a time-base compressed speed after selection being retained. There is further provided means for reproducing the recorded signals with the rotation speed of a cylinder, a tape speed and so on being set to values proportional to the transmission rate of a reproduction signal and the number of signals to be simultaneously reproduced and with the signal being time-base expanded or being retained as time-base compressed.

With the above construction, N kinds of desired signals selected from the multiplexed input digital signal and time-base compressed to 1/K are subjected to time-division multiplex recording with a time-base compressed speed after selection being retained. Upon reproduction, for example, if both the cylinder rotation speed and the tape speed are set to N/K times, a recording track and a reproducing track coincide with each other and the use of a reproducing time K/N times as long as a recording time enables the reproduction of each of the N kinds of signals at a standard speed. Also, if both the cylinder rotation speed and the tape speed are set to (M×N)/K times, a recording track and a reproducing track coincide with each other and the use of a reproducing time as K/(M×N) times as long as the recording time enables the reproduction of each of the N kinds of signals at an M-tuple speed. In the case where L kinds of signals are selected from among the N kinds of reproduced signals and a processing speed at a reproduction signal processing circuit is. set to L×M times as long as a standard reproduction processing speed, each of the L kinds of signals among the N kinds of multiple-recorded signals is outputted at a speed M times as high as a standard speed.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a digital transmission signal processing system and a recording/reproducing system according to an embodiment of. the present invention;

FIG. **2** is a block diagram of a recording/reproducing system according to another embodiment of the present invention;

FIG. **3** is a diagram for explaining the conventional parity adding method;

FIG. **4** is a block diagram of a recording/reproducing system according to still another embodiment of the present invention;

FIG. **5** is a block diagram of a digital transmission signal processing system and a recording/reproducing system according to a further embodiment of the present invention;

FIG. **6** shows the format of control signals used in one of applications of the present invention;

FIG. **7** is a block diagram of a still further embodiment of the present invention;

FIG. **8** shows one example of the specification of signals to be recorded;

FIG. **9** is a block diagram of a furthermore embodiment of the present invention;

FIGS. **10**, **11** and **12** are block diagrams of different examples of applications of the present invention;

FIG. **13** is a block diagram for explaining one example of the operation of the embodiment shown in FIG. **7**;

FIG. **14** is a timing chart showing the waveforms of signals involved in the example shown in FIG. **13**;

FIG. **15** is a block diagram for explaining another example of the operation of the embodiment shown in FIG. **7**;

FIG. **16** is a timing chart showing the waveforms of signals involved in the example shown in FIG. **15**;

FIG. **17** is a table showing some applications of the examples shown in FIGS. **13** and **15**;

FIG. **18** is a block diagram of a still furthermore embodiment of the present invention; and

FIGS. **19** and **20** are signal diagrams for explaining different operations of the embodiment shown in FIG. **18**.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of the present invention will now be explained by use of FIG. **1**. In the figure, reference numerals **1** and **40** denote magnetic tapes, numerals **2**, **3**, **41** and **42** magnetic heads, numerals **4** and **43** cylinders, numerals **5** and **44** capstans, numerals **10** and **50** servo control circuits, numerals **20**, **31** and **60** demodulation circuits, numerals **21**, **32** and **61** error correction circuits, numerals **22** and **23** compression circuits, numerals **24** and **33** parity addition circuits, numerals **25** and **34** modulation circuits, numerals **26** a transmission circuit, numeral **27** a transmission path, numeral **30** a reception circuit, numerals **62** and **63** expansion circuits, numerals **64** and **65** D/A conversion circuits, numeral **70** a video signal output terminal, and numeral **71** an audio signal output terminal.

Firstly, the operation of a transmission signal processing system will be explained. Digital video and audio signals recorded on the magnetic tape **1** are reproduced by the magnetic heads **2** and **3** mounted on the cylinder **4** and are inputted to the demodulation circuit **20**. The magnetic tape **1** travels by virtue of the capstan **5**. The travel speed of the magnetic tape **1** and the rotation frequency of the cylinder **4** are, for example, ten times as high as the tape travel speed and the cylinder rotation speed upon normal reproduction. Accordingly, the signal inputted to the demodulation circuit **20** is a signal time-compressed to one tenth. For example, a 120-minute signal recorded on the magnetic tape **1** can be reproduced in 12 minutes.

Generally, in the case where a digital signal is to be recorded on a magnetic recording medium, the signal is recorded after having been modulated into scrambled NRZ code, M^2 code or the like. The demodulation circuit **20** performs a demodulation processing, that is, a signal processing for restoring the thus modulated signal into original digital data. The signal demodulated by the demodulation circuit **20** is inputted to the error correction circuit **21** in which erroneous data produced in a magnetic recording/reproducing process is detected and the correction for the erroneous data is made. Further, the signal is separated into

a video signal and an audio signal which are in turn inputted to the compression circuits **22** and **23**, respectively. The video signal is bit-compressed through, for example, discrete cosine conversion. The audio signal is bit-compressed through, for example, non-linear quantization or differential PCM. As a result, the transmission rate of the video signal and the audio signal in total is reduced to, for example, one twentieth.

Output signals of the compression circuits **22** and **23** are inputted to the parity addition circuit **24** for performing a signal processing which includes adding a parity signal for error correction and outputting the video signal and the audio signal serially in accordance with a transmission format. A serial output signal of the parity addition circuit **24** is inputted to the modulation circuit **25**. In the modulation circuit **25**, the serial signal is modulated in accordance with the characteristic and the frequency band of the transmission path **27**. For example, in the case where the signal is transmitted in an electric wave form, quadruple phase shift keying (QPSK) is made. The modulated signal is inputted to the transmission circuit **26** from which it is outputted to the transmission path **27**.

As apparent from the foregoing explanation of the operation of the transmission signal processing system, it is possible to transmit a signal at a speed which is ten times as high as a normal speed.

The above embodiment has been shown in conjunction with the case where a signal from the VTR is reproduced. However, a signal source is not limited to the VTR and may include a magnetic disk device, an optical disk device or the like.

Next, explanation will be made of the operation of the VTR for receiving and recording the transmitted signal. The signal transmitted from the transmission signal processing system is received by the reception circuit **30**. The received signal is inputted to the demodulation circuit **31**. The demodulation circuit **31** is provided corresponding to the modulation and demodulates the signal to the original signal. The demodulated signal is inputted to the error correction circuit **32** in which the detection of and the correction for an error produced in the transmission path **27** are made on the basis of the parity signal added by the parity addition circuit **24**. At this time, in the case where the S/N ratio of the transmission system is not sufficient so that complete correction for the error is impossible, correction is made through, for example, signal replacement, by use of the signal correlation.

An output signal of the error correction circuit **32** is inputted to the parity addition circuit **33**. In the parity addition circuit **33**, a parity signal for detecting an error produced in a recording/reproducing process and making correction for the error is added. The parity-added signal is inputted to the modulation circuit **34**. In the modulation circuit **34**, the signal is modulated to scrambled NRZ code, M^2 code or the like as mentioned above. The modulated signal is recorded on the magnetic tape **40** by the magnetic heads **41** and **42** mounted on the cylinder **43**.

Since the signal supplied to the magnetic heads **41** and **42** is a signal which is time-base compressed to one tenth as compared with a signal upon normal operation, the servo control circuit **50** controls the cylinder **43** and the capstan **44** so that the rotation frequency of the cylinder **43** and the travel speed of the magnetic tape **40** become ten times as high as those upon normal recording. Also, in order to record a predetermined signal at a predetermined position on the magnetic, tape **40**, synchronization information is detected from the received signal to control the phase of rotation of the cylinder **41** on the basis of the detected synchronization information.

Next, the operation of the VTR for reproducing the thus recorded signal will be explained. Upon reproduction, the travel speed of the magnetic tape **40** and the rotation frequency of the cylinder **43** are set to those upon normal reproduction. The reproduced signal is inputted to the demodulation circuit **60**. The demodulation circuit **60** is provided corresponding to the modulation circuit **34** and demodulates the modulated signal. The demodulated signal is inputted to the error correction circuit **61** in which the detection of an error produced in the magnetic recording/reproducing system and the correction for the error are made on the basis of the parity signal added by the parity addition circuit **33**. In the case where there is an error which cannot be corrected, the error is properly corrected by use of the signal correlation. Also, the signal is outputted after having been separated into a video signal and an audio signal.

The video signal is inputted to the expansion circuit **62**. The expansion circuit **62** is provided corresponding to the compression circuit **22** and restores the compressed video signal into the original video signal. An output signal of the expansion circuit **62** is inputted to the D/A conversion circuit **64** and is converted thereby into an analog video signal which is in turn outputted from the terminal **70**.

The audio signal is inputted to the expansion circuit **63**. The expansion circuit **63** is provided corresponding to the compression circuit **23** and restores the compressed audio signal into the original audio signal. An output signal of the expansion circuit **63** is inputted to the D/A conversion circuit **65** and is converted thereby into an analog audio signal which is in turn outputted from the terminal **71**.

In the foregoing, the embodiment of the present invention has been shown and the operation thereof has been explained. According to the present invention, a video signal and an audio signal over a long time can be transmitted and recorded in a short time, thereby making it possible to extend the range of use of the digital VTR.

Another embodiment of the present invention is shown in FIG. **2**. FIG. **2** is partially similar to FIG. **1**. The same parts in FIG. **2** as those in FIG. **1** are denoted by the same reference numerals as those used in FIG. **1** and detailed explanation thereof will be omitted. The embodiment shown in FIG. **2** concerns a VTR in which a signal transmitted/received at a high speed can be recorded while being monitored.

In FIG. **2**, reference numeral **80** denotes a change-over switch, numeral **81** an error correction circuit, and numeral **82** a memory circuit. An error-corrected video signal outputted from the error correction circuit **81** is inputted through the memory circuit **82** to a terminal R side of the change over switch **80** which is selected upon recording. The memory circuit **82** has a memory capacity for at least one field. The video signal received at a high speed is stored into a memory of the memory circuit **82** with the number of frames being reduced. The stored signal is read from the memory at a normal speed and is inputted to an expansion circuit **62**.

Upon reproduction, a video signal output of an error correction circuit **61** is inputted to a terminal P side of the change-over switch **80** which is selected upon reproduction. Accordingly, the operation of the embodiment of FIG. **2** upon reproduction is similar to that of the embodiment shown in FIG. **1**.

In the embodiment shown in FIG. **2**, upon recording, the video signal outputted from the error correction circuit **81** is

inputted to the expansion circuit **62** through the memory circuit **82**. Alternatively, an output signal of a modulation circuit **34** may be inputted to a demodulation circuit **60** through a memory circuit. Also, in the case where the operating speed of the demodulation circuit **60** or the error correction circuit **61** leaves a margin, a memory circuit may be properly placed at a post stage. Or, in the case where the storage capacity of the error correction circuit **61** or the expansion circuit **62** leaves a margin, the circuit may be used as a memory circuit or any additional memory circuit may be omitted.

As has been explained in the above, the embodiment shown in FIG. **2** makes it possible to record a received video signal while monitoring it in the form of a picture having a reduced number of frames.

In the embodiment shown in FIG. **1**, the parity signal is added in order to make the detection of and the correction for an error which may be produced in the transmission system or the magnetic recording/reproducing system. One example of a parity adding method is shown in FIG. **3** in conjunction with the case of a D2 format VTR. In the D2 format VTR, a signal for one field is divided into a plurality of segments for signal processing. FIG. **3** shows one segment. In FIG. **3**, reference numeral **90** represents a group of video data, numeral **91** a group of outer code parities, and numeral **92** a group of inner code parities. Firstly, outer code parities are added for data of the matrix-like arranged video data group **90** which lie in a vertical direction in FIG. **3**. Thereafter, inner code parities are added for data of the video data group **90** and the outer code parity group **91** lying in a horizontal direction in FIG. **3**, thereby producing a signal to be recorded. Though detailed explanation of the generation of parities will be omitted herein, the parities are generated in accordance with a generating function G(x).

In the embodiment shown in FIG. **1**, if the same parity generation manner is employed by the parity addition circuits **24** and **33**, the error correction circuits **32** and **61** may hold the most part thereof in common. Namely, since the error correction circuits **32** and **61** are circuits which are respectively used upon recording and upon reproduction, it is possible to reduce the circuit scale or size by using the most part of the circuits **32** and **61** in common.

Further, in the case where the same parity generation manner is employed by the parity addition circuits **24** and **33** in the embodiment shown in FIG. **1**, it is possible to further reduce the circuit scale or-size of the recording/reproducing system. The construction in that case is shown in FIG. **4** as still another embodiment of the present invention. FIG. **4** is partially common to FIG. **1** or **2**. The parts in FIG. **4** common to those in FIG. **1** or **2** are denoted by the same reference numerals as those used in FIG. **1** or **2** and detailed explanation thereof will be omitted.

The embodiment shown in FIG. **4** is based on a concept that an error produced in a transmission system and an error produced in a magnetic recording/reproducing system are simultaneously detected and corrected by an error correction circuit **61**. Accordingly, a signal received by a reception circuit **30** is demodulated by a demodulation circuit **31** and is inputted to a modulation circuit **34** without being subjected to error correction and parity addition. The subsequent processing is the same as that in the embodiment shown in FIG. **1** or **2**. Namely, a reproduced signal is inputted to the error correction circuit **61** after demodulation by a demodulation circuit **60**. As mentioned above, an error produced in the transmission system and an error produced in the magnetic recording/reproducing system are simultaneously detected and corrected by the error correction circuit **61** in the reproducing system.

In the embodiment shown in FIG. **4**, the error correction circuit **32** and the parity addition circuit **33** can be removed as compared with the embodiment shown in FIG. **1** or **2**, thereby making it possible to reduce the circuit scale.

Though having not been mentioned in the foregoing embodiments, in a helical scan VTR as shown, since a signal becomes discontinuous when a track jump is made upon reproduction, the recording is made with an amble signal being added to the heading portion of a signal. Since the addition of an amble signal is employed in the D2 format VTR, detailed explanation thereof will be omitted. Also, in order to define a starting position of a signal, a synchronizing signal is properly added. Since the addition of a synchronizing signal is known in, for example, the D2 format VTR, detailed explanation thereof will be omitted.

In the embodiment shown in FIG. **1**, the addition of an amble signal may be made by the parity addition circuit **24**. Alternatively, it may be made on the recording/reproducing system side in order to enhance the efficiency of use of the transmission path **27**. In this case, the addition of an amble signal can be made by the parity addition circuit **33**. As for the embodiment shown in FIG. **4**, in the case where the addition of an amble signal is to be made on the recording/reproducing system side, the amble signal can be added by the modulation circuit **34**. In the case where the addition of an amble signal is made on the recording/reproducing system side, it is possible to enhance the efficiency of use of the transmission path **27**. On the other hand, in the case where the addition of an amble signal is made on the transmission signal processing system side, the lowering of the cost of a VTR can be attained as a great effect when a signal is sent to a multiplicity of VTR's simultaneously.

FIG. **5** shows a further embodiment of the present invention in which the further reduction of the circuit scale of a VTR on the receiving side and hence the further lowering of the cost can be attained in the case where a signal is sent to a multiplicity of VTR's simultaneously.

FIG. **5** is partially common to FIG. **1**, **2** or **4**. The parts in FIG. **5** common to those in FIG. **1**, **2** or **4** are denoted by the same reference numerals as those used in FIG. **1**, **2** or **4** and detailed explanation thereof will be omitted. In FIG. **5**, reference numeral **100** denotes a modulation circuit. The embodiment shown in FIG. **5** is based on a concept that a signal processing required upon a recording mode of a VTR is performed on the transmitting side. Namely, modulation adapted for magnetic recording/reproduction, for example, a signal processing corresponding to the modulation circuit **34** shown in FIG. **4** is performed on the transmission signal processing system side. After parities have been added by a parity addition circuit **24** of the transmission signal processing system, the modulation adapted for the magnetic recording/reproduction is performed by the modulation circuit **100**. Therefore, modulation adapted for transmission is performed by a modulation circuit **25**. As a modulation system employed by the modulation circuit **100** is suitable a system which does not cause the extension of a frequency band by modulation, for example, scrambled NRZ. A signal modulated by the modulation circuit **25** is transmitted to a transmission path **27** through a transmission circuit **26** in a manner to that in the embodiment shown in FIG. **1**.

The signal received by a reception circuit **30** through the transmission path **27** is inputted to a demodulation circuit **31** in which the signal is subjected to demodulation corresponding to the modulation circuit **25**. Since the signal demodulated by the demodulation circuit **31** is one which has

already been subjected by the modulation circuit **10** to the modulation adapted for the magnetic recording/reproduction, the signal is recorded on a magnetic tape **40** by magnetic heads **41** and **42** as it is. As a result, the same recording as that in the embodiment shown in FIG. **4** is made. An operation upon reproduction is similar to that in the embodiment shown in FIG. **4**.

As apparent from the above, the. present embodiment makes it possible to remarkably reduce the circuit scale of the VTR.

According to one of applications of the present invention, it is possible to transmit a signal from a transmission signal processing system to a multiplicity of VTR's through a transmission path simultaneously and at a high speed, as has already been mentioned. In this case, it is difficult to control a multiplicity of VTR's simultaneously. Further, it is required to make a control which causes specified ones of the VTR's to perform recording operations and specified others of the VTR's not to perform recording operations. A technique for realizing such a control will be shown just below.

For the above purpose, control signals are transmitted prior to transmission of a signal to be recorded. One example of the control signals is shown in FIG. **6**. In the figure, reference numeral **110** denotes a synchronizing signal, numeral **111** an ID signal indicative of a control to be made, numeral **112** an address signal indicative of a VTR to be controlled, numeral **113** a control signal for bringing a VTR designated by the address signal **112** into a recording mode, numeral **114** a control signal for stopping the recording, numerals **115** and **116** blank signals, and numeral **120** a recording signal to be actually recorded.

The ID signal **111** indicating the transmission of the address signals **112** indicative of VTR's in which a signal is to be recorded, is transmitted at a predetermined position relative to the synchronizing signal **110** to bring each VTR into a standby condition. After all the address signals have been transmitted, the ID signal **113** is transmitted to start the recording of the signal **120** in the designated VTR's. After the signal **120** has been transmitted, the ID signal **114** to control the stop of recording is transmitted. Each of the blank signals **115** and **116** is a signal for conforming a signal transmission format to the other transmission signal and is therefore an insignificant signal portion.

In the embodiments shown in FIGS. **1** and **5**, those control signals are produced by a control signal generation circuit **130** and are transmitted with parities which are added by the parity addition circuit **24** for making correction for an error produced during transmission.

In the VTR shown in FIG. **1**, the control signals are detected by a control circuit **131** after the reception by the reception circuit **30**, the demodulation by the demodulation circuit **31** and the correction by the error correction circuit **32** for an error produced during transmission to make a control for the recording and the stop of recording in the recording/reproducing system.

In the case of the VTR's shown in FIGS. **4** and **5**, an output signal of the demodulation circuit **31** is inputted to the error correction circuit **61** for a need of making correction for an error produced during transmission and error-corrected control signals are inputted to a control circuit **131**. In a change-over circuit **132**, the terminal R side for selecting an output signal of the demodulation circuit **31** is selected upon recording and the terminal P side for selecting an output signal of the demodulation circuit **60** is selected upon reproduction.

As apparent from the foregoing, the present embodiment makes it possible to control a multiplicity of VTR's selectively and simultaneously.

Also, the use of the change-over circuit **132** and a memory circuit makes it possible to record a signal while monitoring it in the form of a picture having a reduced number of frames, as explained in conjunction with the embodiment shown in FIG. **2**.

Next, a still further embodiment of the present invention will be explained by use of FIG. **7**. In the figure, reference numeral **301** denotes an input terminal for standard analog video signal, numeral **302** an input terminal for standard digital video signal, numeral **303** an input terminal for high-speed digital video signal, numeral **305** a recording system mode change-over switch, numeral **306** a recording system change-over signal generation circuit, numeral **310** an A/D converter, numeral **320** a change-over circuit, numeral **330** a data compression circuit, numeral **340** a change-over circuit, numeral **350** a recording system signal processing circuit for performing a signal processing which includes addition of error correction code and modulation for recording, numeral **370** a cylinder, numeral **371** a magnetic tape, numerals **372** and **372'** magnetic heads, numeral **380** a reproducing system signal processing circuit for performing a signal processing which includes demodulation for reproduction, error detection and error correction. Numeral **390** a change-over circuit, numeral **400** a data expansion circuit, numeral **420** a D/A converter, numeral **431** an output terminal for standard analog video signal, numeral **432** an output terminal for standard digital video signal, numeral **433** an output terminal for high-speed digital video signal, numeral **435** a reproducing system mode change-over switch, and numeral **436** a reproducing system change-over signal generation circuit.

The present embodiment is an example of a digital magnetic recording/reproducing system which has recording modes of standard-speed recording and high-speed recording and reproduction modes of standard-speed reproduction and high-speed reproduction. FIG. **8** shows one example of the specification of input video signals.

Firstly, explanation will be made of standard-speed recording. A digital signal into which an analog video signal inputted from the input terminal **301** is converted by the A/D converter **310** or an equivalent digital signal which is inputted from the input terminal **302**, is switched or selected by the change-over circuit **320**, is subjected to a predetermined data compression processing by the data compression circuit **330** and is thereafter inputted to a terminal **340***a* of the change-over circuit **340**. In the change-over circuit **340**, a change-over to connect the terminal **340***a* and a terminal **340***c* is made by a change-over signal from the recording system change-over signal generation circuit **306**. Thereby, the data-compressed signal is inputted to the recording system signal processing circuit **350**. In the recording system signal processing circuit **350**, a signal processing such as channel division, addition of error correction code and modulation for recording is performed at a predetermined processing clock adapted for the data-compressed signal. Thereafter, the signal is supplied to the magnetic heads **372** and **372'** mounted on the cylinder **370** so that it is recorded onto the magnetic tape **371**. The cylinder **370** and the magnetic tape **371** are controlled by a servo control circuit **360**. The servo control circuit **360** controls a cylinder motor and a capstan motor so as to provide a cylinder rotation speed and a tape speed for standard speed and so as to be synchronized with the input video signal.

Next, explanation will be made of high-speed recording. A high-speed digital video signal inputted from the input terminal **303** is sent to a terminal **340***b* of the change-over circuit **340**. Since the high-speed digital video signal is a signal which has already been subjected to a data compression processing, it is not necessary to pass the signal through the data compression circuit **330**. A change-over to connect the terminal **340***b* and the terminal **340***c* is made by a change-over signal from the recording system change-over signal generation circuit **306** so that the high-speed digital video signal is inputted to the recording system signal processing circuit **350**. In the recording system signal processing circuit **350**, a signal processing similar to that in the case of the standard-speed recording is performed at a predetermined processing clock adapted for the high-speed digital video signal. Thereafter, the signal is supplied to the magnetic heads **372** and **372**' mounted on the cylinder **370** so that it is recorded onto the magnetic tape **371**. The cylinder **370** and the magnetic tape **371** are controlled by the servo control circuit **360**. The servo control circuit **360** control the cylinder motor and the capstan motor so as to provide a predetermined cylinder rotation speed and a predetermined tape speed and so as to be synchronized with the input video signal.

In the present invention, the recording onto the tape can be made with the quite same format in both the standard-speed recording and the high-speed recording, thereby making it possible to greatly shorten a recording time in the high-speed recording mode.

Next, explanation will be made of a signal processing upon reproduction. In the present embodiment, the recording pattern on the magnetic tape is the same whichever of the standard-speed. recording and the high-speed recording is selected as a recording mode. Therefore, either standard-speed reproduction or high-speed reproduction can be selected irrespective of the recording mode.

Firstly, the standard-speed reproduction will be explained. The servo control circuit **360** controls the cylinder motor and the capstan motor so that a cylinder rotation speed and a tape speed for standard speed are provided. A signal reproduced by the magnetic heads **372** and **372**' is inputted to the reproducing system signal processing circuit **380**. In the reproducing system signal processing circuit **380**, a signal processing such as demodulation for reproduction, channel synthesis, error detection and error correction is performed at a predetermined processing clock adapted for the standard-speed reproduction. Thereafter, the signal is supplied to a terminal **390***a* of the change-over circuit **390**. In the change-over circuit **390**, a changeover to connect the terminal **390***a* and a terminal **390***c* is made upon standard-speed reproduction by a change-over signal from the reproducing system change-over signal generation circuit **436**. Thereby, the reproduced signal is supplied to the data expansion circuit **400**. In the data expansion circuit **400**, a signal processing reverse to the data compression processing upon recording is performed so that the signal is restored to the original signal. Thereby, the original transmission rate is restored. The data-expanded reproduction signal is sent to the D/A converter **420** on one hand to be outputted as an analog video signal from the output terminal **431** after D/A conversion and is sent to the output terminal **432** on the other hand to be outputted as a digital video signal therefrom.

Next, explanation will be made of the high-speed reproduction. The servo control circuit **360** controls the cylinder motor and the capstan motor so that a predetermined cylinder rotation speed and a predetermined tape speed adapted for the high-speed reproduction are provided. A signal reproduced by the magnetic heads **372** and **372**' is inputted to the reproducing system signal processing circuit **380**. In the reproducing system signal processing circuit **380**, a signal processing such as demodulation for reproduction, channel synthesis, error detection and error correction is performed at a predetermined processing clocks adapted for the high-speed reproduction. Thereafter, the high-speed reproduction signal is supplied to the terminal **390***a* of the change-over circuit **390**. In the change-over circuit **390**, a change-over to connect the terminal **390***a* and a terminal **390***b* is made upon high-speed reproduction. Thereby, the high-speed digital video signal is outputted from the output terminal **433**.

A furthermore embodiment of the present invention will be explained by use of FIG. **9**. The construction of the present embodiment is similar to that of the embodiment shown in FIG. **7** but is different therefrom in that the change-over circuit **340** is placed at a different position, the change-over circuit **390** used in FIG. **7** is eliminated and a change-over circuit **345** is newly added.

An input/output signal upon standard-speed recording/reproduction in the present embodiment is the same as that in the embodiment shown in FIG. **7**. As for high-speed recording and high-speed reproduction, however, the present embodiment is different from the embodiment of FIG. **7** in that the transmission of a high-speed digital video signal is made in the form of a recording format. Accordingly, upon high-speed recording, the high-speed digital video signal is not passed through a recording system signal processing circuit **350** but is recorded onto a tape through the change-over circuit **340** as it is. Upon high-speed reproduction, a reproduced signal is subjected to a signal processing for reproduction such as error detection and error correction by a reproducing system signal processing circuit **380** and is thereafter inputted to a terminal **345***b* of the change-over circuit **345**. The signal supplied through the change-over circuit **345** to the recording system side signal processing circuit **350** is subjected to a signal processing for recording such as addition of error correction code and modulation for recording by the signal processing circuit **350** to form a recording format and is thereafter outputted as a high-speed digital video signal from an output terminal **433**.

The embodiments shown in FIGS. **7** and **9** have feature that high-speed recording and high-speed reproduction are possible. The best use of this feature can be made for dubbing or data communication with the result of effective shortening of a dubbing time, a data communication time or a data circuit line occupation time. Also, though those embodiments have been mentioned in conjunction with an example in which all of standard-speed recording, high-speed recording, standard-speed reproduction and high-speed reproduction modes are involved, it is not necessarily required to implement all of those modes. There may be considered an example in which only a necessary mode is provided in compliance with the purpose of use. FIG. **10** shows an embodiment in which a high-speed recording function is provided as a recording mode and at least a high-speed reproduction function is provided as a reproduction mode. Also, there may be considered an embodiment as a system for the exclusive use for reproduction in which at least a high-speed reproduction function is provided, as shown in FIG. **11**. Further, FIG. **12** shows an embodiment in which a high-speed recording function is provided as a recording mode and a standard-speed reproduction function is provided as a reproduction mode.

FIG. **13** is a block diagram of one example of the magnetic recording/reproducing system of the embodiment

of FIG. **7** for explaining processings subsequent to the compression processing. In FIG. **13**, reference numeral **201** denotes a synchronization detection circuit, numeral **204** a recording modulation circuit, numeral **205** a cylinder servo control circuit, numeral **206** a capstan servo (or tape speed) control circuit, numeral **207** a reproduction reference signal generation circuit, numeral **210** a demodulation circuit, numeral **211** a cylinder, numeral **212** a pair of recording heads, numeral **213** a pair of reproducing heads, numeral **214** a capstan which controls the tape speed, numeral **215** a magnetic tape, numeral **216** a delivery reel, and numeral **217** a take-up reel. FIG. **14** is a timing chart of input and output signals in the example shown in FIG. **13** and schematically illustrate a compressed picture signal **251** which is an input signal, a synchronizing signal **252** of the picture signal, a standard-speed reproduction signal **255** which is an output signal, and a reproduction synchronizing signal **256**.

In the shown example, n-tuple speed recording is realized by making a tape speed and a cylinder rotation speed upon recording n times as high as those upon standard-speed reproduction. As shown in FIG. **14**, the compressed video signal as an input signal of the circuit shown in FIG. **13** and the synchronizing signal include information **251** for n pictures and n synchronizing pulses **252** synchronous therewith in a time when one picture is reproduced at a standard speed. The picture information is converted into a predetermined recording format by the recording modulation circuit **204** and is recorded onto the magnetic tape **215** by the recording heads **212**. At this time, a synchronizing signal for the cylinder servo control circuit **205** and the capstan-servo control circuit **206** is increased by n times in compliance with the n-tuple speed video signal, as shown by **252** in FIG. **14**, so that the rotation speed of the cylinder **211** and the feed speed of the magnetic tape **215** are increased by n times. Thereby, the recording onto the tape can be made with the quite same recording format as that in the case of the standard-speed recording. Upon reproduction, a synchronizing signal for the cylinder servo control circuit **205** and the capstan servo control circuit **206** is supplied from the reproduction reference signal generation circuit **207** to restore the cylinder rotation speed and the tape feed speed to those upon standard-speed reproduction, and a signal read. by the reproducing heads **213** is demodulated by the demodulation circuit **210** and is outputted therefrom. In the circuit shown in FIG. **13**, if the input video signal and the synchronizing signal are ones of standard speed, standard-speed recording is possible. Also, n-tuple speed reproduction is possible if the frequency of an output signal from the reproduction reference signal generation circuit is increased by n times.

FIG. **15** is a block diagram of another example of the magnetic recording/reproducing system of the embodiment of FIG. **7** for explaining processings subsequent to the compression processing. FIG. **16** is a timing chart of input and output signals in the example shown in FIG. **15**. In FIG. **15**, the same reference numerals as those used in FIG. **13** denote the same or equivalent components as or to those shown in FIG. **13**. In FIG. **15**, reference numeral **202** denotes a÷m circuit, numeral **203** recording system memories, numeral **208** a÷m circuit, and numeral **209** reproducing system memories. In FIG. **16**, the same reference numerals as those used in FIG. **14** denote the same or equivalent signals as or to those shown in FIG. **14**. In FIG. **16**, reference numeral **253** denotes outputs of the recording system memories **203** and numeral **254** denotes an output of the ÷m circuit **208** or a synchronizing signal divided by m.

The embodiment shown in FIG. **15** is an example in which m pairs of recording heads are used to simultaneously record magnetic signals for m pictures on m tracks, thereby realizing high-speed recording while suppressing an increase in the cylinder rotation speed. Upon reproduction, m pairs of reproducing heads are used. Though FIG. **15** shows the case where two pairs of recording heads **212** are used to simultaneously record information for two pictures on two tracks, three or more pairs of heads can be used in a similar manner.

FIG. **17** is a table showing some examples of the tape speed and the cylinder rotation speed (rpm) in the embodiments shown in FIGS. **13** and **15**. In the table, high-speed recording or reproduction at a speed ten times as high as the standard speed is shown by way of example. Design for implementing another high-speed recording or reproduction is similarly possible. In the table shown in FIG. **17**, examples ①, ② and ③ correspond to the embodiment shown in FIG. **13** and examples ④ and ⑤ correspond to the embodiment shown in FIG. **15**.

A still furthermore embodiment of a digital signal recording/reproducing system of the present invention will be explained by use of a block diagram shown in FIG. **18**.

In FIG. **18**, reference numeral **501** denotes a signal input terminal to which a plurality of video signals are inputted in a time-division multiplex form, numeral **502** a recording selection signal-input terminal to which a recording selection signal for selecting one or plural signals to be recorded from the multiplexed input signal is inputted, numeral **503** a recording signal selection circuit for selecting the signals to be recorded from the multiplexed input signal in accordance with the recording selection signal from the input terminal **502**, numeral **504** a recording signal processing circuit for subjecting the selected signals to a digital processing for recording onto a recording medium, numerals **505** and **505'** magnetic heads, numeral **506** a rotating drum, numeral **507** a magnetic tape or the recording medium, numeral **508** a servo circuit for controlling the rotation of the drum **506** and the travel of the tape **507**, numeral **511** a reproduction selection signal input terminal to which a reproduction selection signal for selecting one or plural signals to be outputted as a reproduction signal from among the multiple-recorded and reproduced signals is inputted, numeral **509** a reproduction signal selection circuit for selecting the signals to be outputted as a reproduction signal from among the multiple-recorded and reproduced signals in accordance with the reproduction selection signal from the input terminal **511**, numeral **510** a reproduction signal processing circuit for subjecting the selected signals to a digital processing, and numeral **512** a reproduction signal output terminal.

The time-division multiplexed input video signal from the signal input terminal **501** is supplied to the recording signal selection circuit **503**. The recording signal selection circuit **503** is also supplied with the recording selection signal from the recording selection signal input terminal **502** to make the selection of signals to be recorded. For example, in the case where six kinds of video signals A, B, C, D, E and F are inputted in a time-division multiplex form as shown in (a) of FIG. **19** and four signals A, B, C and D thereof are to be selected and recorded, an output of the recording signal selection circuit **503** is as shown in (b) of FIG. **19**. Such an output signal of the recording signal selection circuit **503** is inputted to the recording signal processing circuit **504** which in turn performs a signal processing for recording such as addition of error correction code. Also, the recording signal selection circuit **503** produces a speed control signal on the

basis of the number of signals in the time-division multiplexed input video signal, the transmission rate of the input signal and the number of signals to be recorded which are selected by the recording selection signal. The speed control signal is supplied to the recording signal processing circuit **504** and the servo circuit **508**. For example, in the case where the input video signal is time-division multiplexed to sextuplet with each of six signals in the multiplexed input signal being transmitted at a rate time-base compressed to ⅙ and four signals among the six signals in the multiplexed input signal are to be selectively recorded, a signal indicative of a quadruple speed is produced as the speed control signal. Also, in the case where the input video signal is time-division multiplexed to sextuplet with each of six signals in the multiplexed input signal being transmitted at a rate time-base compressed to 1/12 and four signals among the six signals in the multiplexed input signal are to be selectively recorded, a signal indicative of a octuple speed is produced as the speed control signal. Namely, in the case where an input signal is multiplexed to N-plet, the compression rate of each of the N signals in the multiplexed input signal is 1/K and the number of signals to be selectively recorded is L, a speed control signal indicative of an (L×K)/N-tuple speed is produced. The operating speed of the recording signal processing circuit **504** which processes a signal from the recording signal selection circuit **503**, is changed in accordance with the speed control signal. For example, in the case of a speed control signal indicative of a quadruple speed, the recording signal processing circuit **504** performs a signal processing at a speed four times as high as a normal speed and supplies the processed signal to the magnetic heads **505** and **505'**. Here, for example, in the case where the input video signal is time-division multiplexed to sextuplet with each of the six signals in the multiplexed input signal being transmitted at a rate time-base compressed to ⅙ and a speed control signal indicative of a quadruple speed is used to selectively record four signals from among the six signals, the speed of an input signal inputted to the recording signal processing circuit **504** is four times as high as that of one video signal having a normal speed and the recording signal processing circuit **504** processes this quadruple-speed input signal at a quadruple speed and supplies the processed signal to the magnetic heads, thereby making it possible to record all of the four selected signals. Also, if the recording signal selection circuit **503** is constructed so that signals to be selectively recorded are sequentially changed for every one track on the tape, compatibility can be held in regard to the number of signals to be selectively recorded and a processing speed by causing the recording signal processing circuit **504** to perform a completed processing for every one track. In the following, explanation will be made in conjunction with the case where each video signal is recorded in such a form completed for every track. However, it should be noted in advance that the present invention is applicable to another recording system, for example, a system in which signals are recorded in a form changed for every pixel, line or field. On the other hand, the servo circuit **508** supplied with the speed control signal indicative of the quadruple speed controls the rotation speed of the rotating drum **506** so that it becomes four times as high as a normal speed and the travel speed of the magnetic tape **507** so that it becomes four times as high as a normal speed. Thereby, four signals A, B, C and D are alternately recorded on successive tracks of the magnetic tape **507**, as shown in FIG. **20**. According to the control mentioned above, the pattern of recording tracks on the tape becomes the same irrespective of the number of signals in the multiplexed input signal, the transmission rate of each signal and the number of signals to be selectively recorded. In order to make a control upon reproduction easy, it is preferable that the number of selectively recorded signals and the identification codes or signal numbers thereof (for example, A, B, C and D or 0, 1, 2 and 3) are recorded as an ID signal for every track.

In the above example, the recording of the time-division multiplexed signal has been mentioned. However, it is needless to say that the present invention is. also applicable to the case where the number of multipet signal components in an input video signal is 1 or the input video signal is not multiplexed. In such a case, since the recording signal processing circuit **504** and the servo circuit **508** operate at speeds proportional to the transmission rate of the input video signal, an effect is manifested, for example, in high-speed dubbing. As apparent from the foregoing explanation of the operation, it is of course that a multiplexed signal can be recorded at a high speed.

Upon reproduction, a signal reproduced. from the magnetic tape **507** by the magnetic heads **505** and **505'** mounted on the rotating drum **506** is inputted to the reproduction signal selection circuit **509**. The reproduction signal selection circuit **509** produces a speed control signal, for example, by detecting the number of multiple-recorded signals from the ID signal included in the reproduced signal and sends the speed control signal to the servo circuit **508**. The speed control signal is a signal indicative of a speed four times as high as the normal reproduction speed in the case where the number of multiple-recorded signals is 4 and a signal indicative of a sextuple speed in the case where it is 6. In the case of the quadruple speed, the servo control circuit **508** supplied with the speed control signal indicative of the quadruple speed controls the rotation speed of the rotating drum **506** so that it becomes four times as high as a normal speed and the travel speed of the magnetic tape **7** so that it becomes four times as high as a normal speed. Thereby, there can be traced all of signals recorded so that the recording track pattern on the tape becomes the same irrespective of the number of signals to be selectively recorded. In a system which has not a signal indicative of the number of selectively recorded signals, there may be employed a method in which the speed control signal is manually set. In a system in which the number of signals to be recorded on the tape is fixed, the speed control signal has a fixed value. The reproduction signal selection circuit **509** receives a reproduction selection signal inputted from the reproduction selection signal input terminal **511** to select a desired signal(s) from among the signals reproduced by the magnetic heads **505** and **505'** and to output the selected signal as a reproduction signal to the reproduction signal processing circuit **510**. The reproduction signal selection circuit **509** also outputs a selection number signal indicative of the number of selected signals to the reproduction signal processing circuit **510**.

The reproduction signal processing circuit **510** performs a signal processing such as code error correction processing and picture signal processing for the reproduction signal at a processing speed corresponding, to the selection number signal and outputs the processed reproduction signal from the output terminal **512**. For example, in the case where the number indicated by the selection number signal is 2, the signal processing speed is two times as high as a normal speed and various processings are performed for each selected signal. For example, in the case where signals A and C are selected, the signals A and C are outputted alternately for each field. In the case where the number indicated by the selection number signal is 1, for example, when the repro-

duction selection signal from the reproduction selection signal input terminal **511** selects only the signal C, the reproduction signal processing circuit **510** performs the signal processing at the normal speed to output the signal as reproduced at a normal speed. As apparent from the above, the present embodiment makes it possible to simultaneously record any number of signals selected from among a plurality of signals in a multiplexed video signal and to simultaneously reproduce any number of signals from among the recorded signals.

In the case where a plurality of signals are simultaneously reproduced, a construction for outputting the reproduced signals from separate output terminals simultaneously and in parallel may be employed, particularly, in the case of an analog output, as a method other than the construction in which the plurality of reproduced signals are outputted in a time-division multiplex form, as mentioned above. Though in the above-mentioned example the reproduction signal is outputted at a reproduction speed for a usual video signal, the transmission rate of the reproduction signal may be made higher than the reproduction speed for the usual video signal in order to transmit the reproduction signal to another system in an analog or digital signal form at a high rate or to perform high-speed dubbing which is one of effects of the present embodiment. This can be realized in such a manner that the fundamental operating speed of there producing system is set to be higher than a normal reproduction speed and the operating speeds of the servo circuit **508**, the reproduction signal selection circuit **509** and the reproduction signal processing circuit **510** are changed in accordance with the number of multiple-recorded signals and/or the number of signals to be outputted as a reproduction signal with the above fundamental speed being the standard. If the transmission rate of a reproduction signal is made variable so that a rate adapted for a transmission path to which the reproduction signal is to be connected or the performance or function of a recorder by which the reproduction signal is to be recorded, can be selected.

As mentioned above, according to the present embodiment, it is possible to simultaneously record any number of signals selected from among a plurality of signals in a multiplexed video signal and to reproduce any number of signals from among the recorded signals at any speed. Also, in the case where a plurality of signals are selected and reproduced and the plurality of reproduced signals are simultaneously outputted in a time-division multiplex form or from separate output terminals in parallel, it is possible to arbitrarily set the transmission rate of an output signal.

The present embodiment has been explained in conjunction with the case where the present invention is applied to a helical-scan digital-recording VTR. It is of course that a similar effect can be obtained in the case where the present invention is applied to a fixed head VTR. The fixed head system is convenient for the structuring of a system since it has a higher degree of freedom for the setting of the units of division of a signal subjected to time-division multiple recording as compared with the helical scan system. Also, it is of course that the present invention is applicable to a recording/reproducing equipment other than the VTR or is applicable to a digital signal processing and analog recording system.

The present invention can be applied to not only the case where an input signal is time-division multiplexed, as mentioned above, but also the case where a plurality of signals are inputted simultaneously and in parallel. In the latter case, the recording signal selection circuit **503** is constructed to receive the input signals in parallel.

As has been mentioned in the foregoing, according to the present invention, it is possible to realize a digital VTR in which high-speed recording onto a tape can be made with the same format as that used in standard-speed reproduction. Further, there can be realized a transmission signal processing for transmitting at a high rate a video signal to be recorded by such a digital VTR. Also, in the case where a signal transmitted from the transmission signal processing system is to be recorded by a multiplicity of VTR's, it is possible to designate those ones of the multiplicity of VTR's by which recording is to be made and to make a control of the start/stop of recording.

What is claimed is:

1. An apparatus for receiving digital information which is digital video information bit-compressed by a first compression system plus digital audio information bit-compressed by a second compression system and transmitted to a transmission path, comprising:

a receiver which receives the transmitted digital information;

a demodulator which demodulates the digital information received by the receiver;

an error detector which detects an error of digital information demodulated by the demodulator by use of a parity signal;

a first expander which bit-expands video information among digital information error detected by the error detector corresponding to the first compression system; and

a second expander which bit-expands audio information among digital information error detected by the error detector corresponding to the second compression system.

2. An apparatus according to claim **1**, wherein the first compression system and the second compression system are different systems.

3. An apparatus according to claim **1**, wherein the demodulator affects QPSK demodulation.

4. An apparatus according to claim **1**, further comprising:

an output terminal which outputs the digital information error-detected by the error detector to a recording/reproducing apparatus;

an input terminal which inputs a reproduced signal from the recording/reproducing apparatus; and

a selector which selects one of the digital information error-detected by the error detector and the digital information inputted from the input terminal;

wherein the digital information selected by the selector is bit-expanded by the first expander and the second expander.

5. An apparatus for recording digital information which is digital video information bit-compressed by a first compression system using discrete cosine transform plus digital audio information bit-compressed by a second compression system, and which has been error-detected by use of a first parity signal added to the digital information and received from a receiving apparatus, comprising:

an input terminal which inputs the digital information from the receiving apparatus;

a parity signal adder which adds a second parity signal to the inputted digital information which is different from the first parity signal;

a modulator which modulates the second parity signal added digital information added by the parity signal adder; and

a recorder which records the digital information modulated by the modulator on a recording media;

wherein the digital information received from the receiving apparatus is recorded to the recording media with no further expansion and/or compression processing.

6. An apparatus for recording digital information which is digital video information bit-compressed by a first compression system using discrete cosine transform plus a digital audio information bit-compressed by a second compression system, and which has been demodulated corresponding to a first modulation system and received from a receiving apparatus comprising:

an input terminal which inputs the digital information from the receiving apparatus;

a parity signal adder which adds a recording parity signal to the inputted digital information;

a modulator which modulates the recording parity signal added digital information added by the parity signal adder, by using a second modulation system which is different from the first modulation system; and

a recorder which records the digital information modulated by the modulator on a recording media;

wherein the digital information received from the receiving apparatus is recorded to the recording media with no further expansion and/or compression processing.

7. An apparatus according to claim **1**, wherein the first compression system uses a discrete cosine transform, the received digital information is phase-modulated, and the demodulator demodulates the digital information received by the receiver in accordance with the phase-modulation.

8. An apparatus for processing a transmitted digital signal, comprising:

a receiver which receives the transmitted digital signal, wherein the transmitted digital signal includes video signal bit-compressed by a first compression method, an audio signal bit-compressed by a second compression method, and a parity signal for error correction;

a demodulator which demodulates the digital signal received by the receiver;

an error corrector which corrects an error of the digital signal demodulated by the demodulator based on the parity signal;

a first expander which bit-expands the video signal of the digital signal corrected by the error corrector in accordance with the first compression method; and

a second expander which bit-expands the audio signal of the digital signal corrected by the error corrector in accordance with the second compression method.

9. The apparatus according to claim **8**, wherein the first compression method utilizes a discrete cosine transform.

* * * * *

EXHIBIT G

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Arai et al.

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(54) **APPARATUS FOR RECEIVING COMPRESSED DIGITAL INFORMATION**

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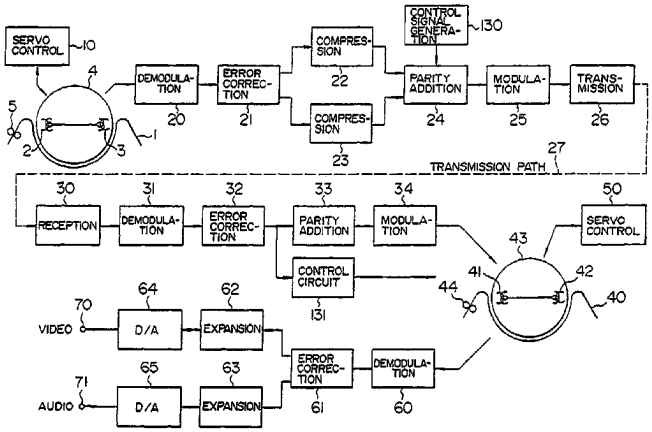
(74) *Attorney, Agent, or Firm*—Antonelli, Terry, Stout & Kraus, LLP.

(57) **ABSTRACT**

An apparatus for receiving digital information including a receiver which receives the digital information that has digital video information bit-compressed by a first compression system, digital audio information bit-compressed by a second compression system, and error-detection information added to both the digital video information and the digital audio information. There is also provided a demodulator which demodulates the digital information received by the receiver, an error detector which detects an error of digital information demodulated by the demodulator by use of the error-detection information, a first expander which bit-expands video information among the digital information error detected by the error detector corresponding system, and a second expander which bit-expands audio information among the digital information error detected by the error detector corresponding to the second compression system.

7 Claims, 18 Drawing Sheets



RELATED U.S. APPLICATION DATA

Mar. 16, 2001, now Pat. No. 6,498,691, which is a continuation of application No. 09/654,962, filed on Sep. 5, 2000, now Pat. No. 6,324,025, which is a continuation of application No. 09/567,005, filed on May 9, 2000, now Pat. No. 6,278,564, which is a continuation of application No. 09/326,595, filed on Jun. 7, 1999, now Pat. No. 6,069,757, which is a continuation of application No. 09/188,303, filed on Nov. 10, 1998, now Pat. No. 6,002,536, which is a continuation of application No. 08/917,176, filed on Aug. 25, 1997, now Pat. No. 5,862,004, which is a continuation of application No. 08/620,879, filed on Mar. 22, 1996, now Pat. No. 5,699,203, and a continuation of application No. 08/620,880, filed on Mar. 22, 1996, now Pat. No. 5,673,154, which is a continuation of application No. 08/457,597, filed on Jun. 1, 1995, now Pat. No. 5,530,598, which is a continuation of application No. 08/457,486, filed on Jun. 1, 1995, now Pat. No. 5,517,368, which is a continuation of application No. 08/238,528, filed on May 5, 1994, now Pat. No. 5,671,095, which is a division of application No. 07/727,059, filed on Jul. 8, 1991, now Pat. No. 5,337,199.

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JP	64-73560	3/1989
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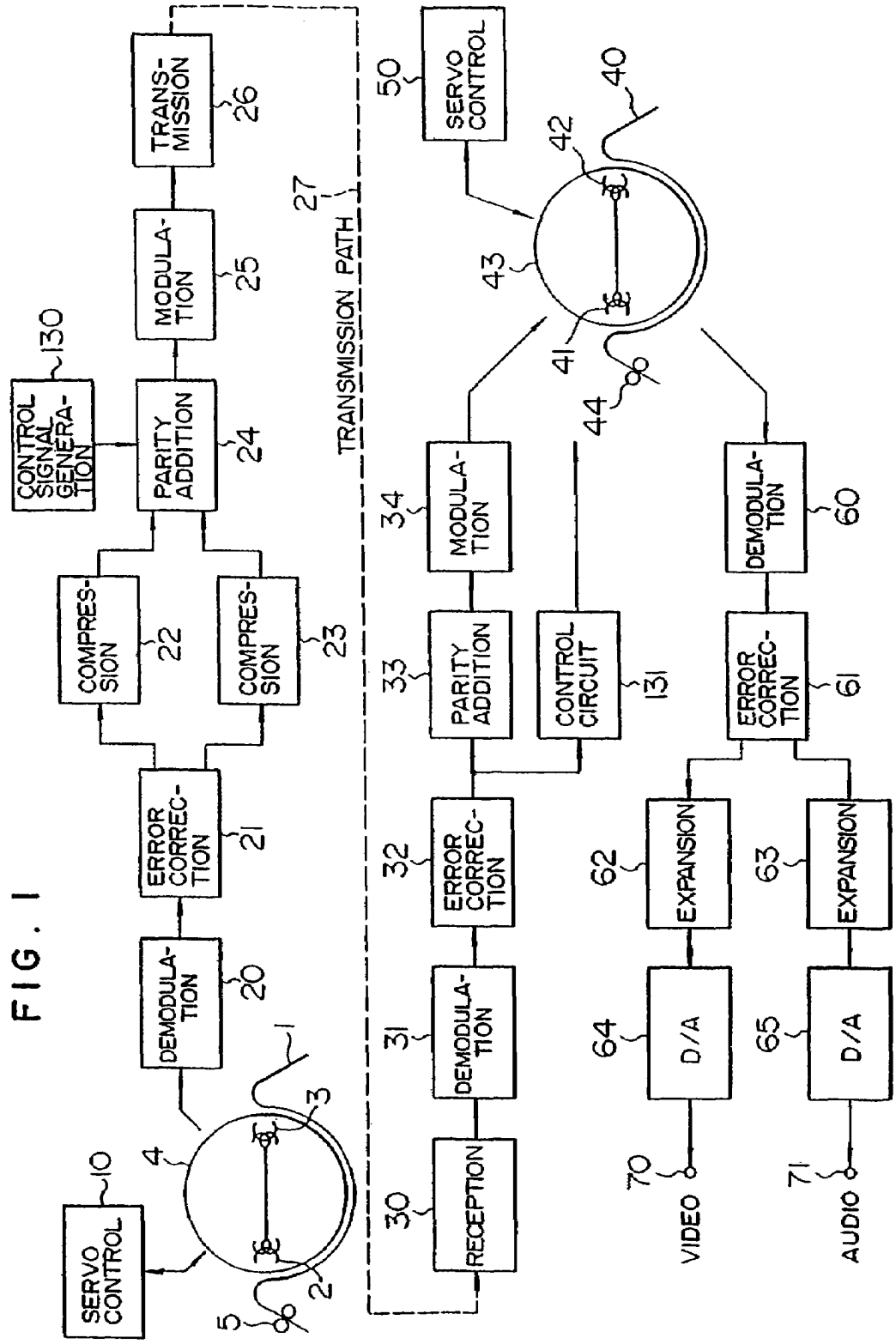

SERVO CONTROL
10
DEMODULATION
20
ERROR CORRECTION
21
COMPRESSION
22
COMPRESSION
23
PARITY ADDITION
24
MODULATION
25
TRANSMISSION
26
CONTROL SIGNAL GENERATION
130
TRANSMISSION PATH
27
RECEPTION
30
DEMODULATION
31
ERROR CORRECTION
32
PARITY ADDITION
33
MODULATION
34
CONTROL CIRCUIT
131
SERVO CONTROL
50
DEMODULATION
60
ERROR CORRECTION
61
EXPANSION
62
EXPANSION
63
D/A
64
D/A
65
VIDEO
70
AUDIO
71
1
2
3
4
5
40
41
42
43
44

FIG. 1

FIG. 2

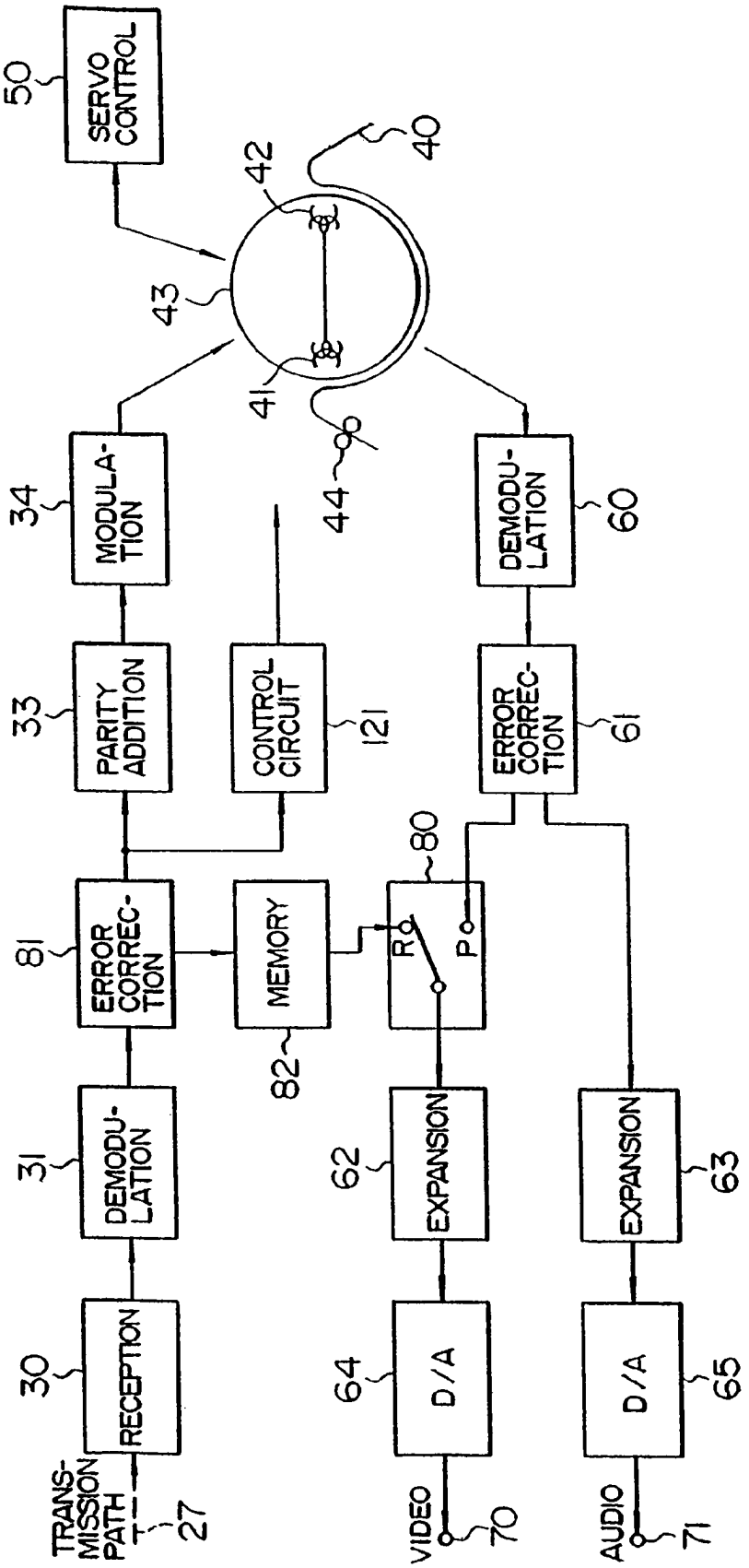

50
SERVO CONTROL
42
40
43
41
44
34
MODULA-TION
DEMODU-LATION
60
33
PARITY ADDITION
CONTROL CIRCUIT
121
ERROR CORREC-TION
61
80
81
ERROR CORREC-TION
MEMORY
R
P
82
31
DEMODU-LATION
62
EXPANSION
63
30
RECEPTION
64
D/A
65
TRANS-MISSION PATH
27
VIDEO
70
AUDIO
71

FIG. 3

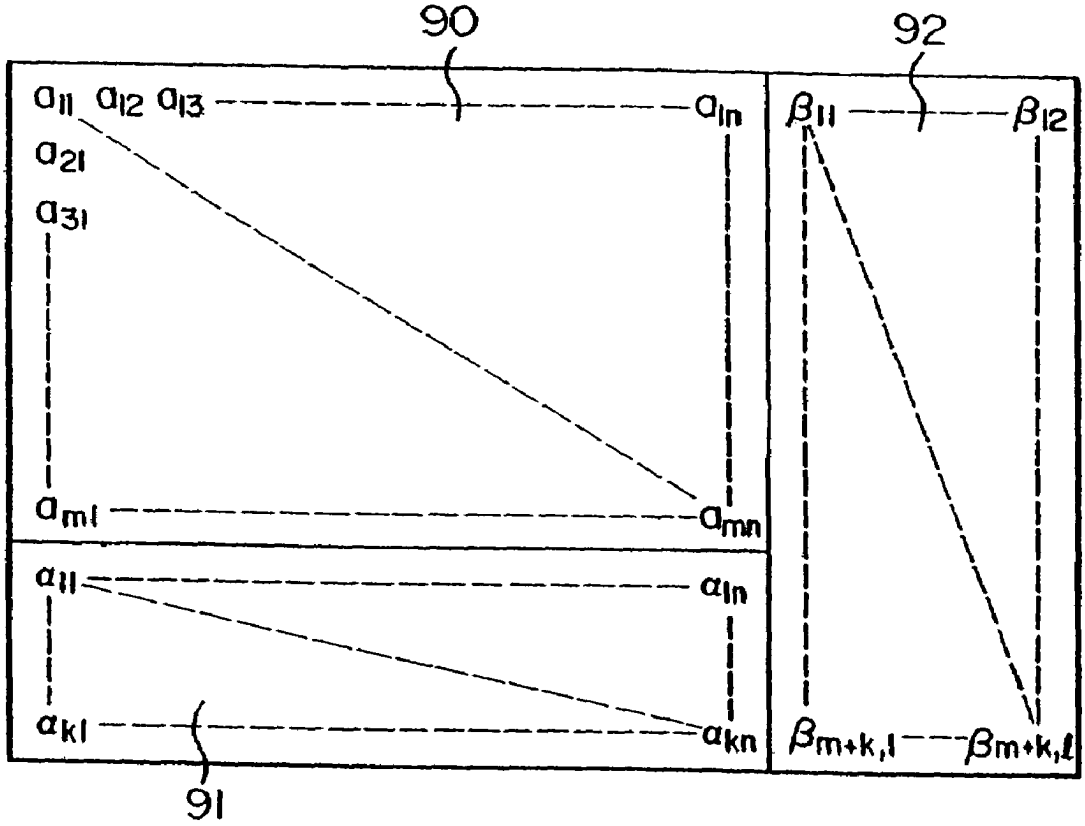
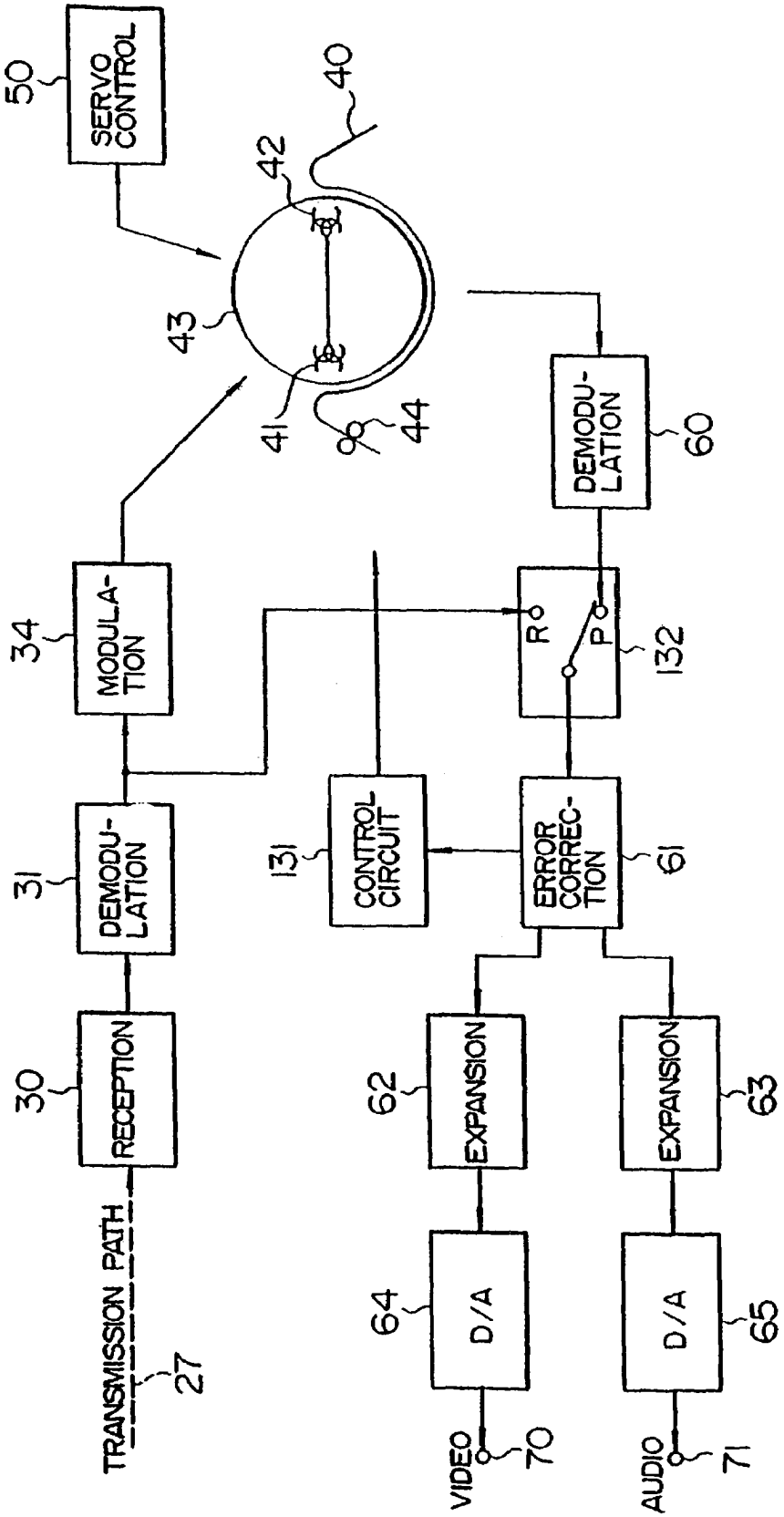

90
92
a_{11} a_{12} a_{13}
a_{1n}
a_{21}
a_{31}
a_{m1}
a_{mn}
β_{11}
β_{12}
a_{11}
a_{1n}
a_{k1}
a_{kn}
$\beta_{m+k,1}$
$\beta_{m+k,l}$
91

FIG. 4


50
SERVO CONTROL
40
42
43
41
44
DEMODU-LATION
60
34
MODULA-TION
R
P
132
31
DEMODU-LATION
131
CONTROL CIRCUIT
ERROR CORREC-TION
61
30
RECEPTION
62
EXPANSION
EXPANSION
63
TRANSMISSION PATH
27
64
D/A
D/A
65
VIDEO
70
AUDIO
71

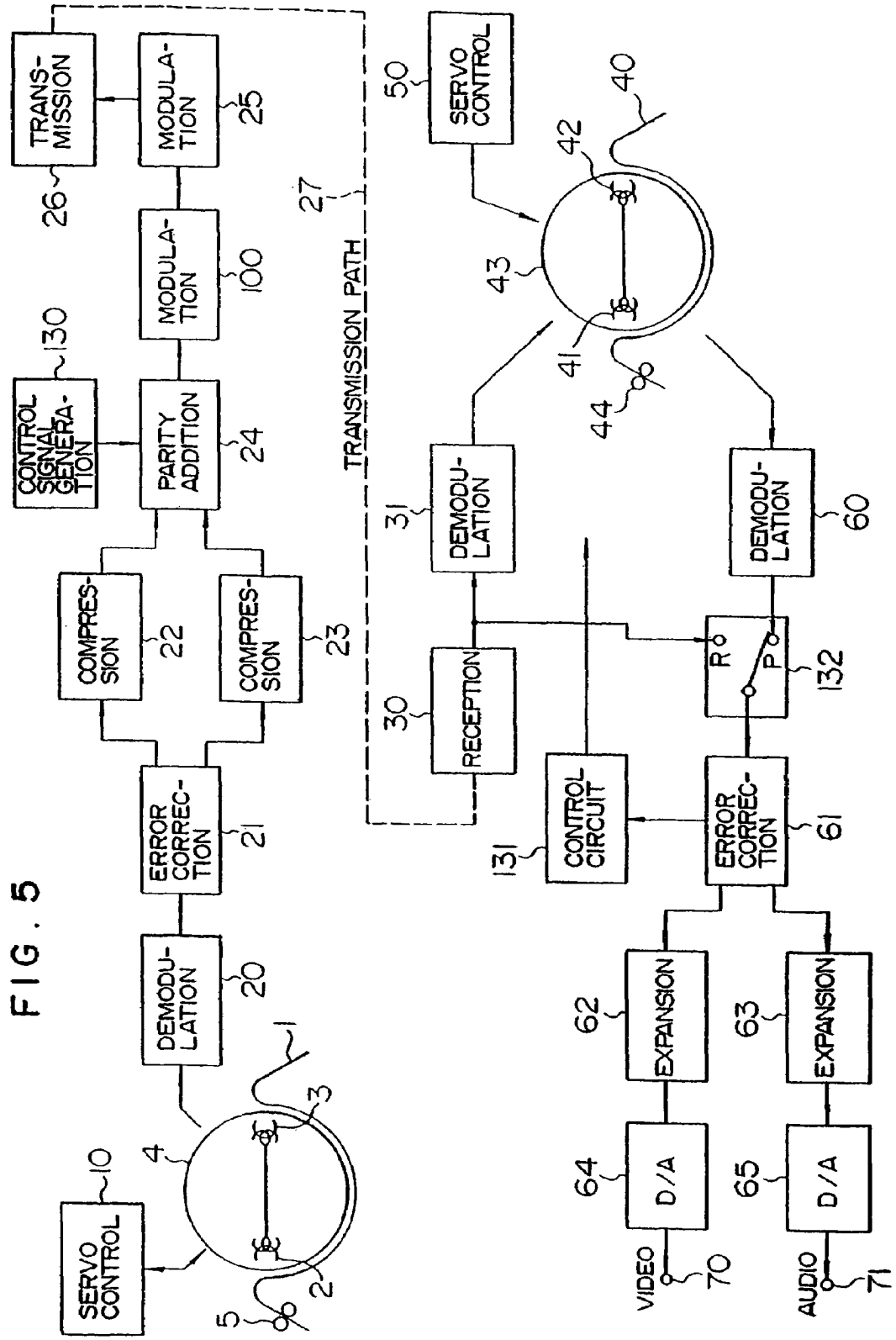

TRANS-MISSION
26
MODULA-TION
25
MODULA-TION
100
CONTROL SIGNAL GENERA-TION
130
PARITY ADDITION
24
COMPRES-SION
22
COMPRES-SION
23
ERROR CORREC-TION
21
DEMODU-LATION
20
SERVO CONTROL
10
TRANSMISSION PATH
27
SERVO CONTROL
50
DEMODU-LATION
31
RECEPTION
30
CONTROL CIRCUIT
131
DEMODU-LATION
60
ERROR CORREC-TION
61
R
P
132
EXPANSION
62
EXPANSION
63
D/A
64
D/A
65
VIDEO
70
AUDIO
71
1
2
3
4
5
40
41
42
43
44

FIG. 5

FIG. 6

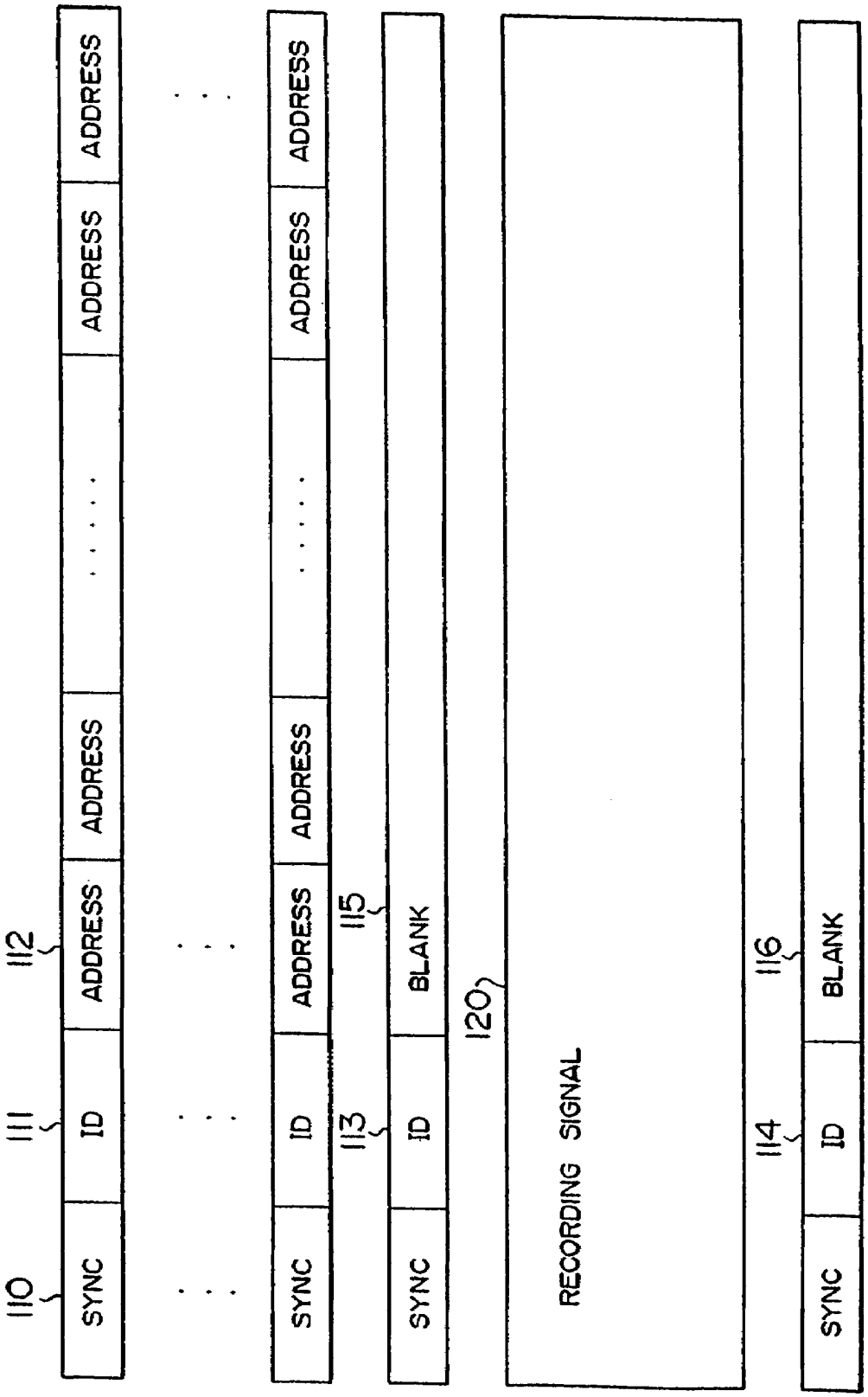

110
111
112
113
114
115
116
120
SYNC
ID
ADDRESS
BLANK
RECORDING SIGNAL

FIG. 7

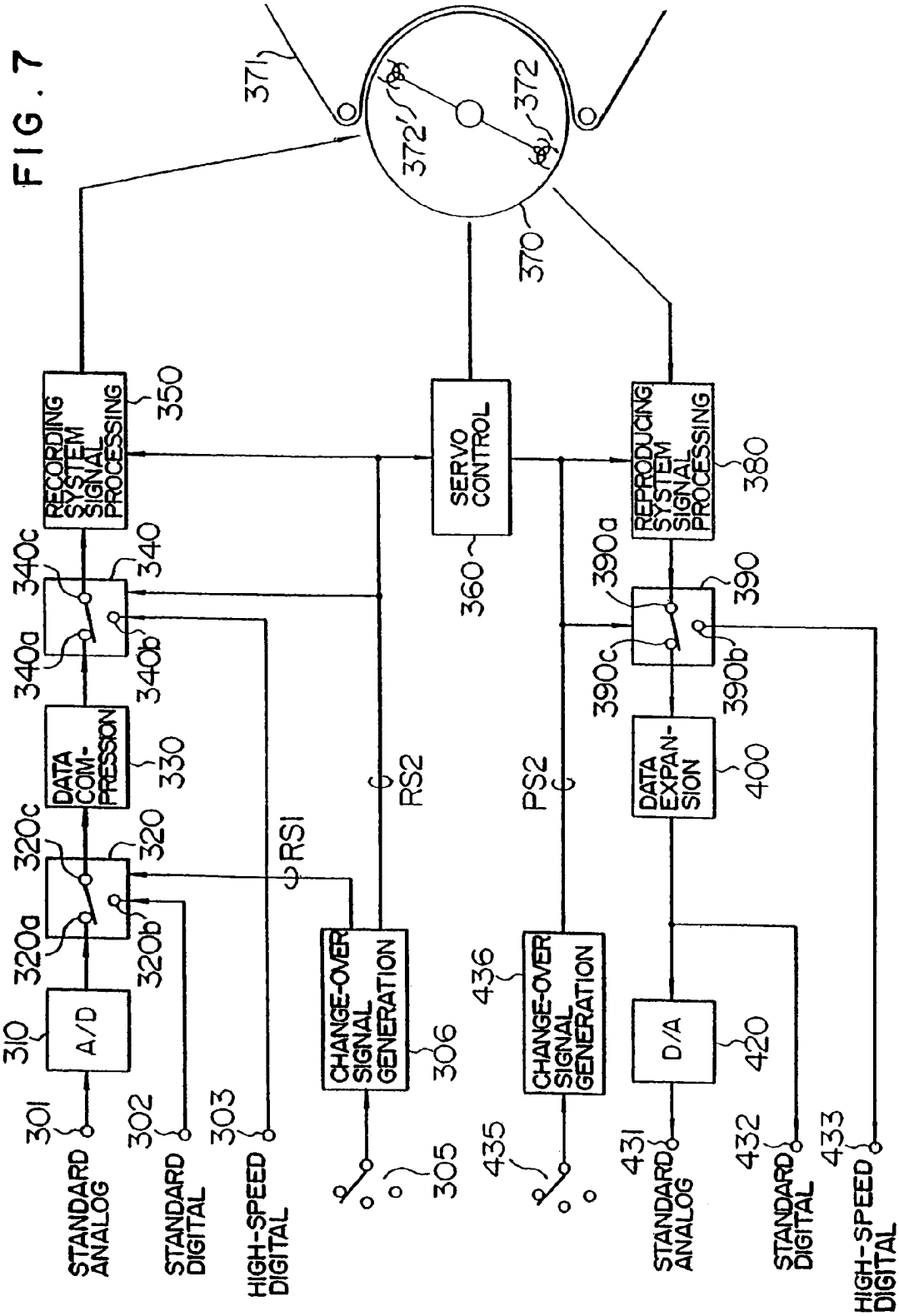

371
372
372'
370
RECORDING SYSTEM SIGNAL PROCESSING
350
SERVO CONTROL
360
REPRODUCING SYSTEM SIGNAL PROCESSING
380
340c
340
340a
340b
DATA COM-PRESSION
330
320c
320
320a
320b
A/D
310
RS1
RS2
PS2
CHANGE-OVER SIGNAL GENERATION
306
436
CHANGE-OVER SIGNAL GENERATION
390a
390
390c
390b
DATA EXPAN-SION
400
D/A
420
301
302
303
305
435
431
432
433
STANDARD ANALOG
STANDARD DIGITAL
HIGH-SPEED DIGITAL
STANDARD ANALOG
STANDARD DIGITAL
HIGH-SPEED DIGITAL

FIG. 8

ITEM / INPUT		FIELD FREQUENCY	TRANSMISSION RATE	DATA COMPRESSION	TIME-BASE COMPRESSION
STANDARD SPEED	ANALOG	59.94 Hz	(AFTER A/D) 114 Mbps	ABSENCE	ABSENCE
	DIGITAL		114 Mbps		
HIGH SPEED	DIGITAL	59.94 Hz	100 Mbps	PRESENCE 1/11.4	PRESENCE 1/10

FIG. 9

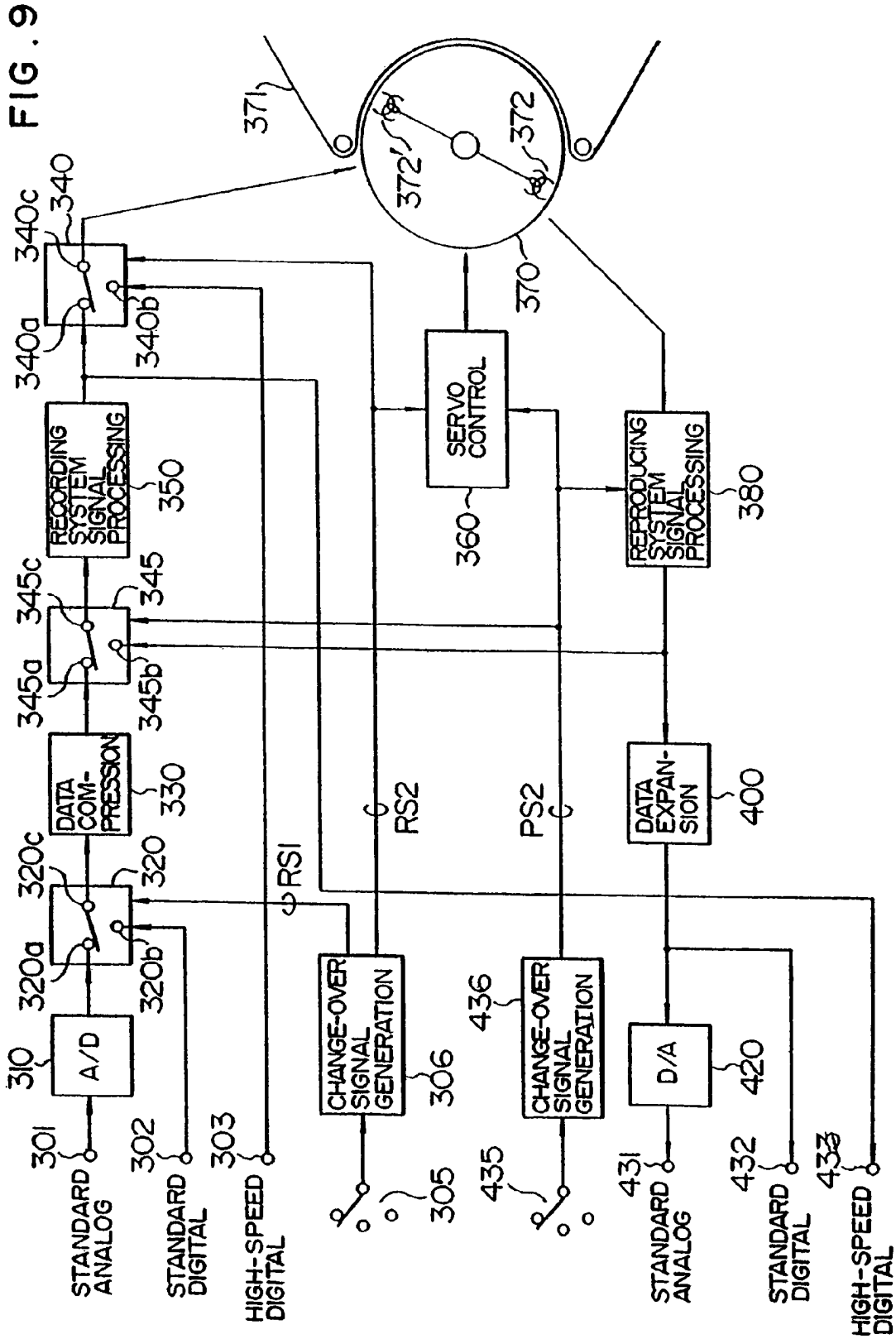

371
372
372'
370
340
340c
340a
340b
SERVO CONTROL
360
RECORDING SYSTEM SIGNAL PROCESSING
350
REPRODUCING SYSTEM SIGNAL PROCESSING
380
345
345c
345a
345b
DATA COM-PRESSION
330
DATA EXPAN-SION
400
320
320c
320a
320b
RS1
RS2
PS2
310
A/D
CHANGE-OVER SIGNAL GENERATION
306
436
CHANGE-OVER SIGNAL GENERATION
D/A
420
301
302
303
305
435
431
432
433
STANDARD ANALOG
STANDARD DIGITAL
HIGH-SPEED DIGITAL
STANDARD ANALOG
STANDARD DIGITAL
HIGH-SPEED DIGITAL

FIG. 10

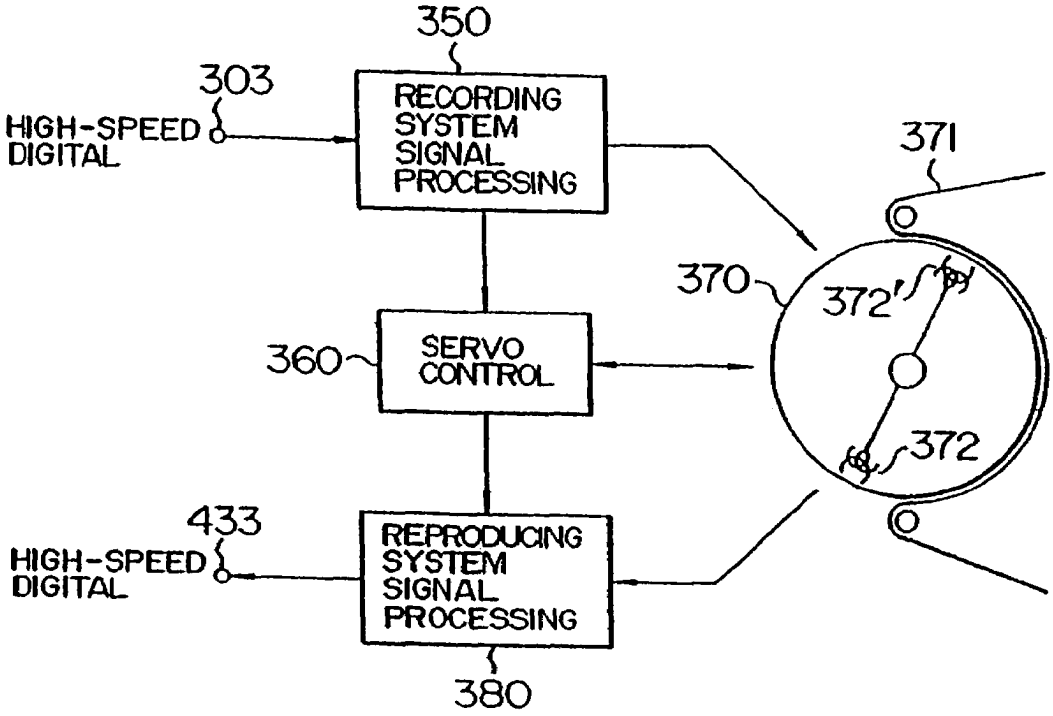

350
303
HIGH-SPEED DIGITAL
RECORDING SYSTEM SIGNAL PROCESSING
371
370
372'
360
SERVO CONTROL
372
433
HIGH-SPEED DIGITAL
REPRODUCING SYSTEM SIGNAL PROCESSING
380

FIG. 11

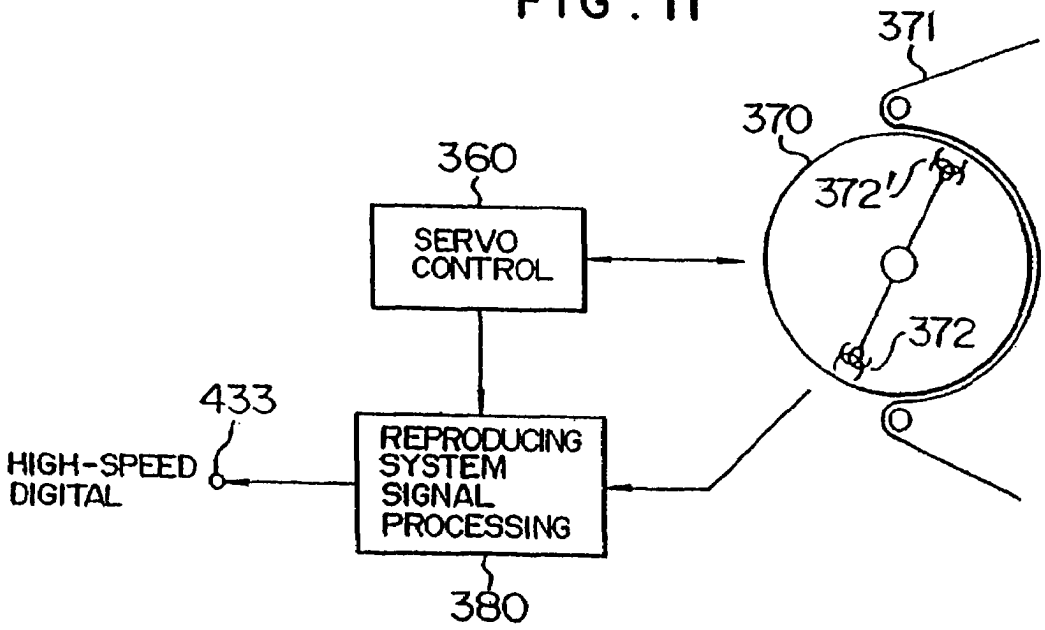

371
370
360
372'
SERVO CONTROL
372
433
HIGH-SPEED DIGITAL
REPRODUCING SYSTEM SIGNAL PROCESSING
380

FIG. 12

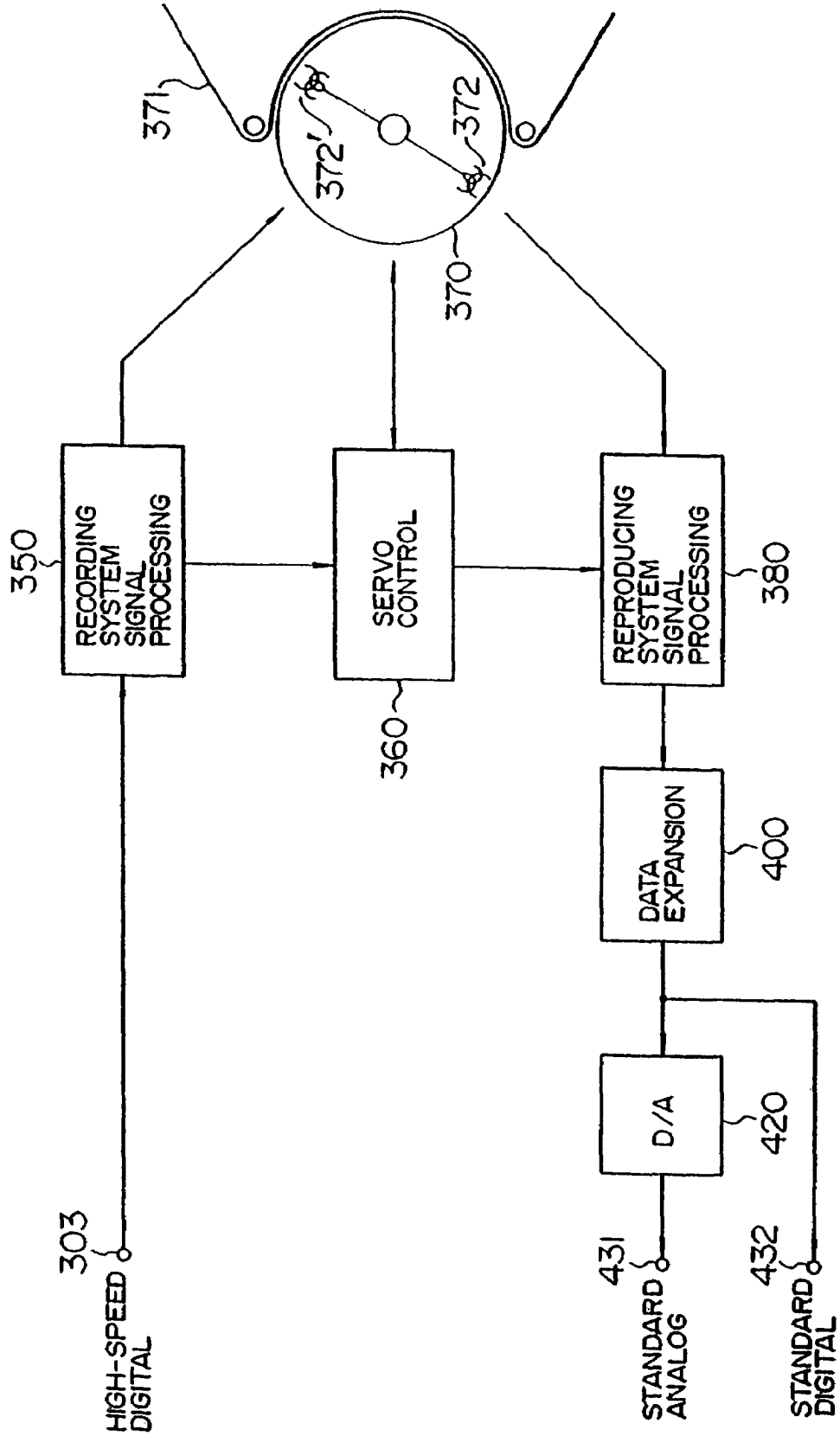

371
372'
372
370
350
RECORDING SYSTEM SIGNAL PROCESSING
SERVO CONTROL
360
REPRODUCING SYSTEM SIGNAL PROCESSING
380
DATA EXPANSION
400
D/A
420
303
HIGH-SPEED DIGITAL
431
STANDARD ANALOG
432
STANDARD DIGITAL

FIG. 13

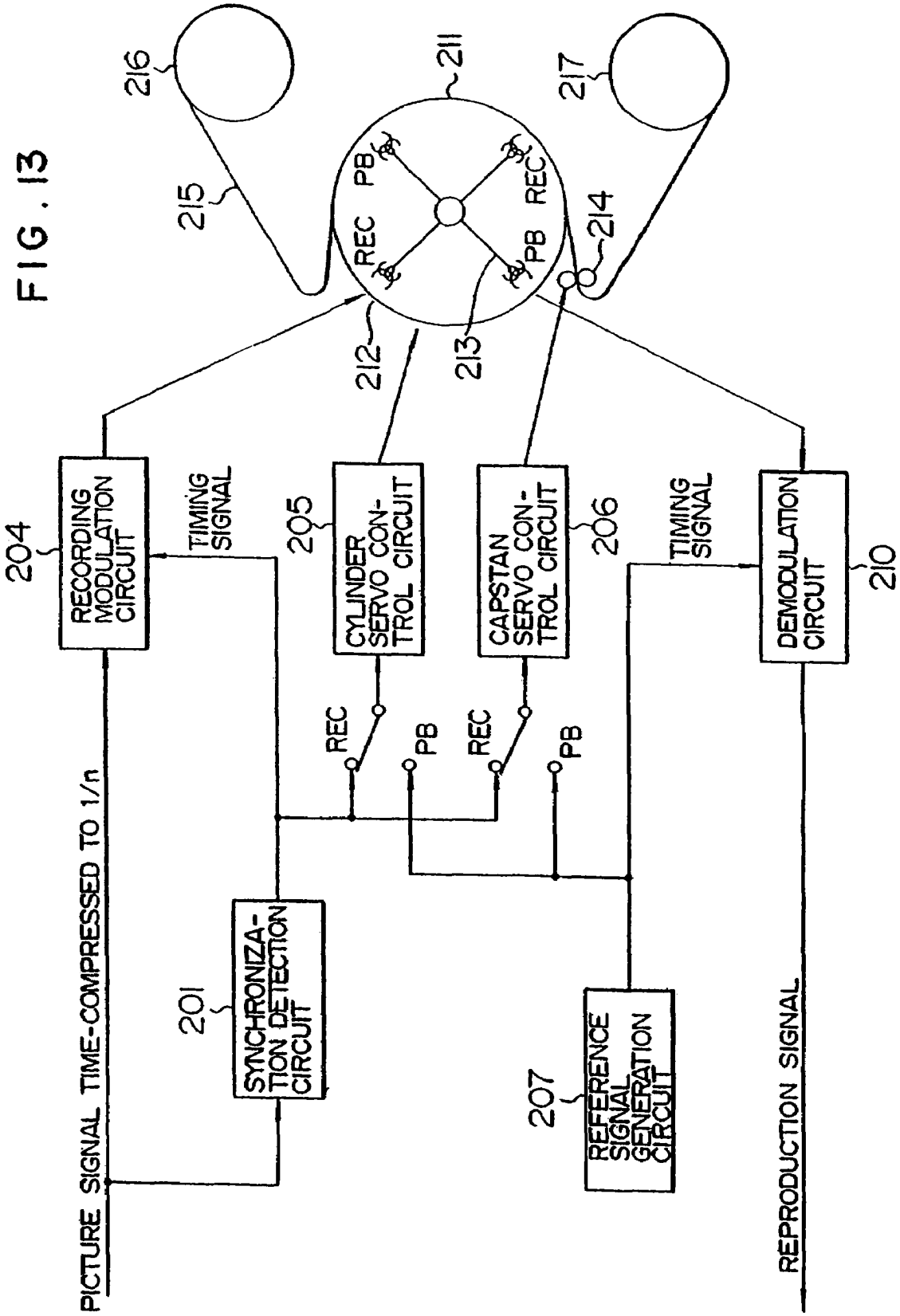

216
211
217
215
214
212
213
REC
PB
PB
REC
204
RECORDING MODULATION CIRCUIT
TIMING SIGNAL
205
CYLINDER SERVO CONTROL CIRCUIT
206
CAPSTAN SERVO CONTROL CIRCUIT
TIMING SIGNAL
DEMODULATION CIRCUIT
210
REC
PB
REC
PB
201
SYNCHRONIZATION DETECTION CIRCUIT
207
REFERENCE SIGNAL GENERATION CIRCUIT
PICTURE SIGNAL TIME-COMPRESSED TO 1/n
REPRODUCTION SIGNAL

FIG. 14

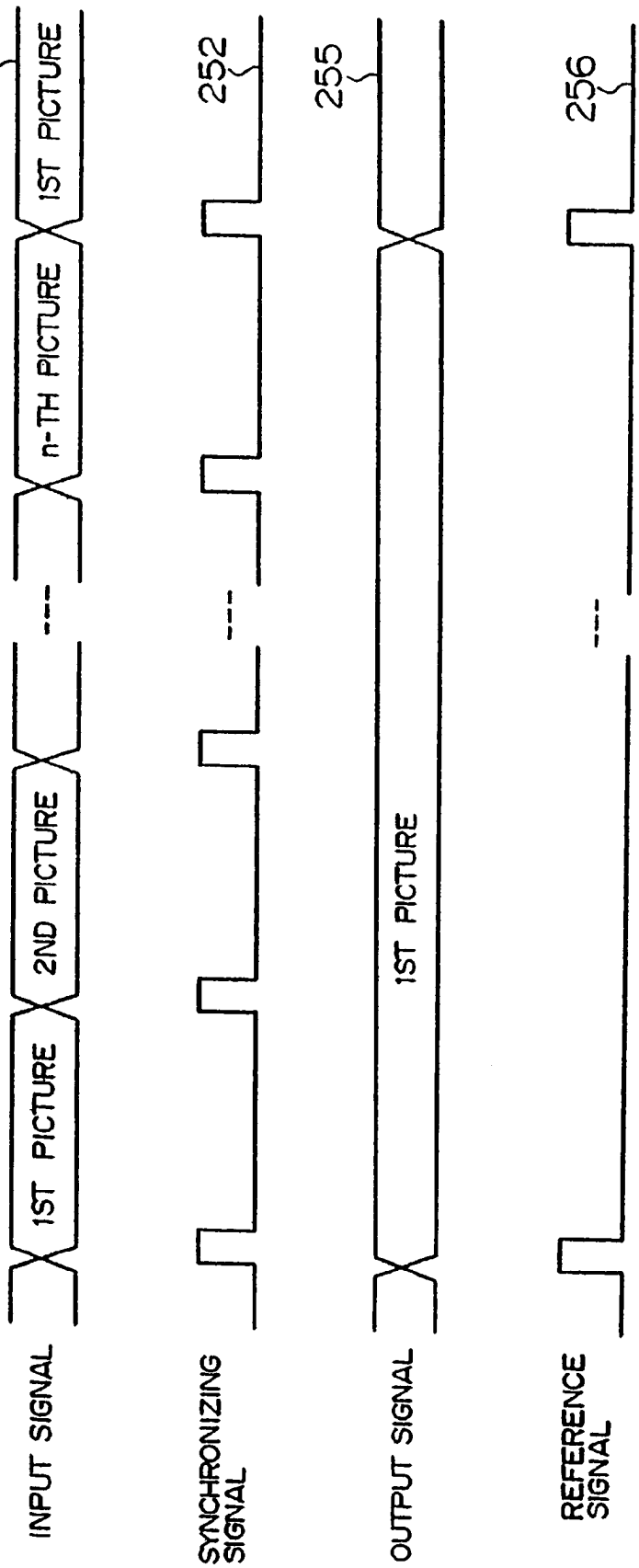

251
252
255
256
1ST PICTURE
2ND PICTURE
n-TH PICTURE
1ST PICTURE
INPUT SIGNAL
SYNCHRONIZING SIGNAL
OUTPUT SIGNAL
REFERENCE SIGNAL

FIG. 15

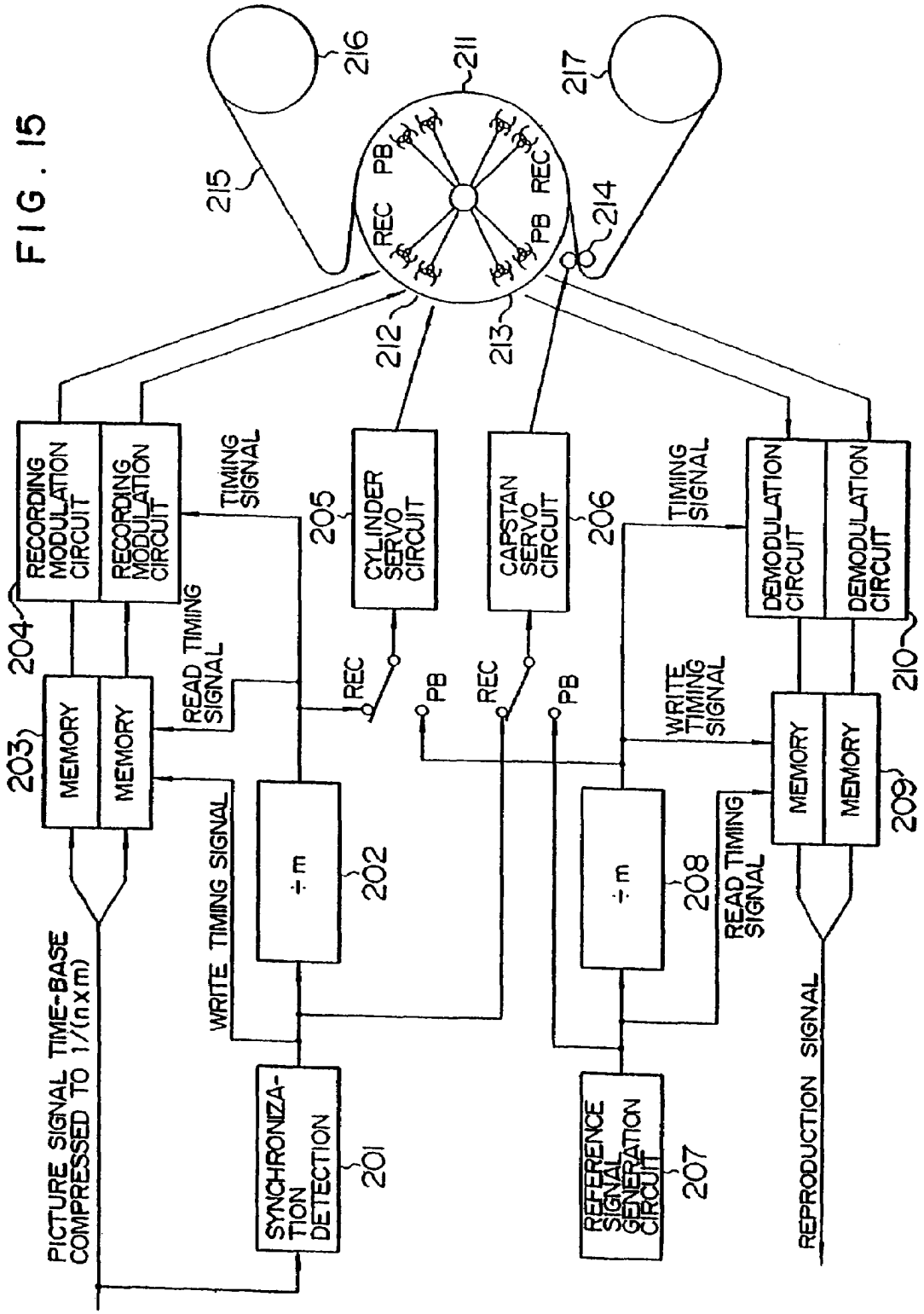

216
211
217
215
REC PB
PB REC
214
212
213
RECORDING MODULATION CIRCUIT
RECORDING MODULATION CIRCUIT
TIMING SIGNAL
205
CYLINDER SERVO CIRCUIT
CAPSTAN SERVO CIRCUIT
206
TIMING SIGNAL
DEMODULATION CIRCUIT
DEMODULATION CIRCUIT
204
READ TIMING SIGNAL
REC
PB
REC
PB
WRITE TIMING SIGNAL
210
203
MEMORY
MEMORY
WRITE TIMING SIGNAL
÷m
202
÷m
208
READ TIMING SIGNAL
MEMORY
MEMORY
209
PICTURE SIGNAL TIME-BASE COMPRESSED TO 1/(n x m)
SYNCHRONIZATION DETECTION
201
REFERENCE SIGNAL GENERATION CIRCUIT
207
REPRODUCTION SIGNAL

FIG. 16

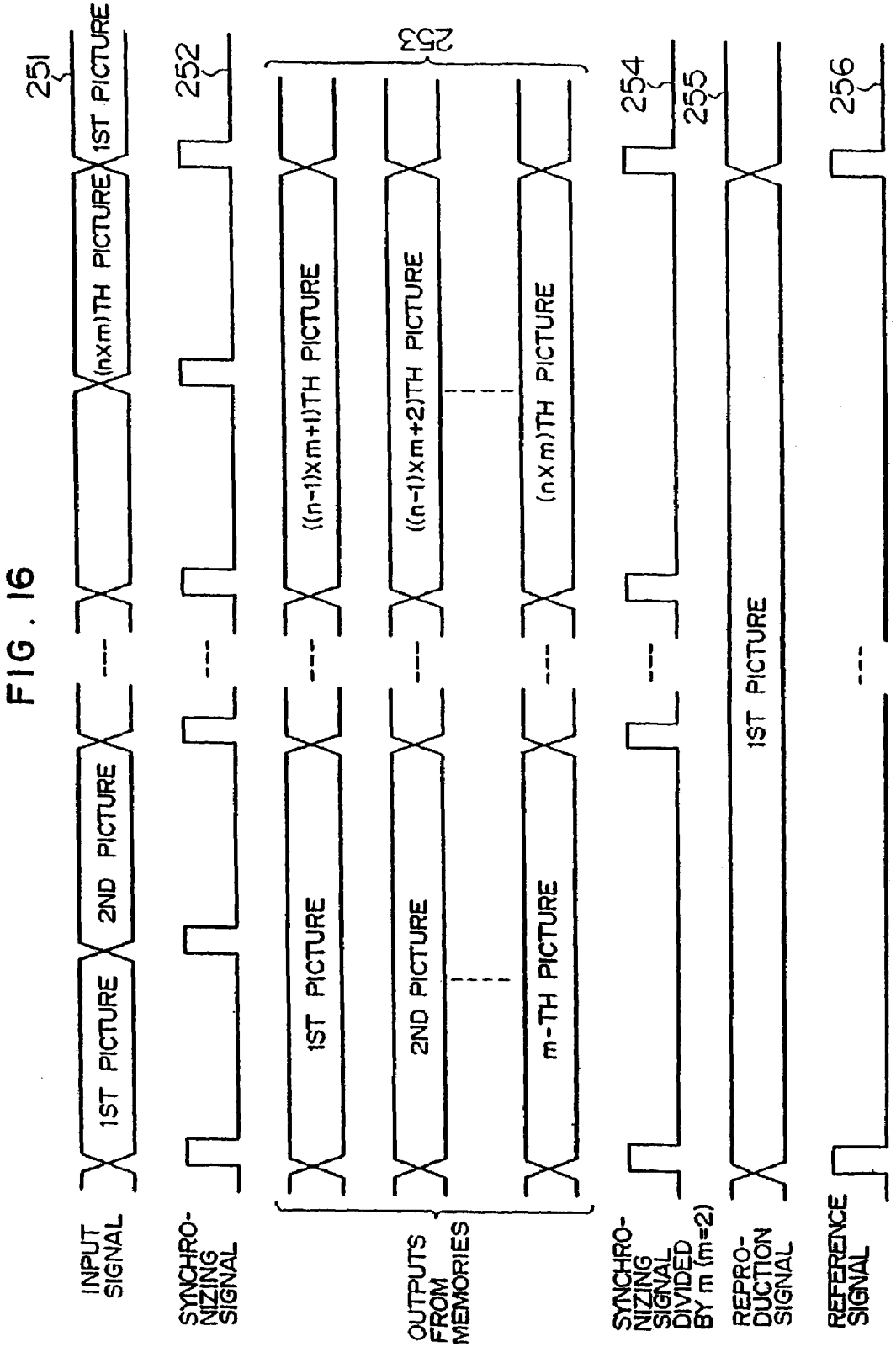

251
252
253
254
255
256
INPUT SIGNAL
SYNCHRONIZING SIGNAL
OUTPUTS FROM MEMORIES
SYNCHRONIZING SIGNAL DIVIDED BY m (m=2)
REPRODUCTION SIGNAL
REFERENCE SIGNAL
1ST PICTURE
2ND PICTURE
(nxm)TH PICTURE
((n-1)xm+1)TH PICTURE
((n-1)xm+2)TH PICTURE
m-TH PICTURE

FIG. 17

SYSTEM	MODE		TAPE SPEED (RATIO TO STANDARD SPEED)		CYLINDER ROTATION SPEED (rpm)		NUMBER OF HEAD PAIRS		CYLINDER DIAMETER (mmφ)	CYLINDER CONTACT ANGLE (deg)	NUMBER OF TRACKS REQUIRED FOR ONE PICTURE	REMARKS
	REC	PB	REC	PB	REC	PB	REC	PB				
VHS (NTSC)	NORMAL SPEED	NORMAL SPEED	1	1	1800	1800	1	1	62	180	1	
D2 (NTSC)	NORMAL SPEED	NORMAL SPEED	1	1	5400	5400	2	2	96	180	6	
EXAMPLE ①	HIGH SPEED	NORMAL SPEED	10	1	9000	900	1	1	120	180	1/2	
	HIGH SPEED	HIGH SPEED	10	10	9000	9000						
	NORMAL SPEED	HIGH SPEED	1	10	900	9000						
EXAMPLE ②	HIGH SPEED	NORMAL SPEED	10	1	9000	900	1	1	90	270	1/2	
	HIGH SPEED	HIGH SPEED	10	10	9000	9000						
	NORMAL SPEED	HIGH SPEED	1	10	900	9000						
EXAMPLE ③	HIGH SPEED	NORMAL SPEED	10	1	18000	1800	1	1	60	180	1	
	HIGH SPEED	HIGH SPEED	10	10	18000	18000						
	NORMAL SPEED	HIGH SPEED	1	10	1800	18000						
EXAMPLE ④	HIGH SPEED	NORMAL SPEED	10	1	9000	900	2	2	60	180	1	
	HIGH SPEED	HIGH SPEED	10	10	9000	9000						
	NORMAL SPEED	HIGH SPEED	1	10	900	9000						
EXAMPLE ⑤	HIGH SPEED	NORMAL SPEED	10	1	9000	1800	2	1	60	180	1	MOVABLE HEADS ARE REQUIRED
	HIGH SPEED	HIGH SPEED	10	10	9000	9000	2	2				
	NORMAL SPEED	HIGH SPEED	1	10	1800	9000	1	2				

FIG. 18

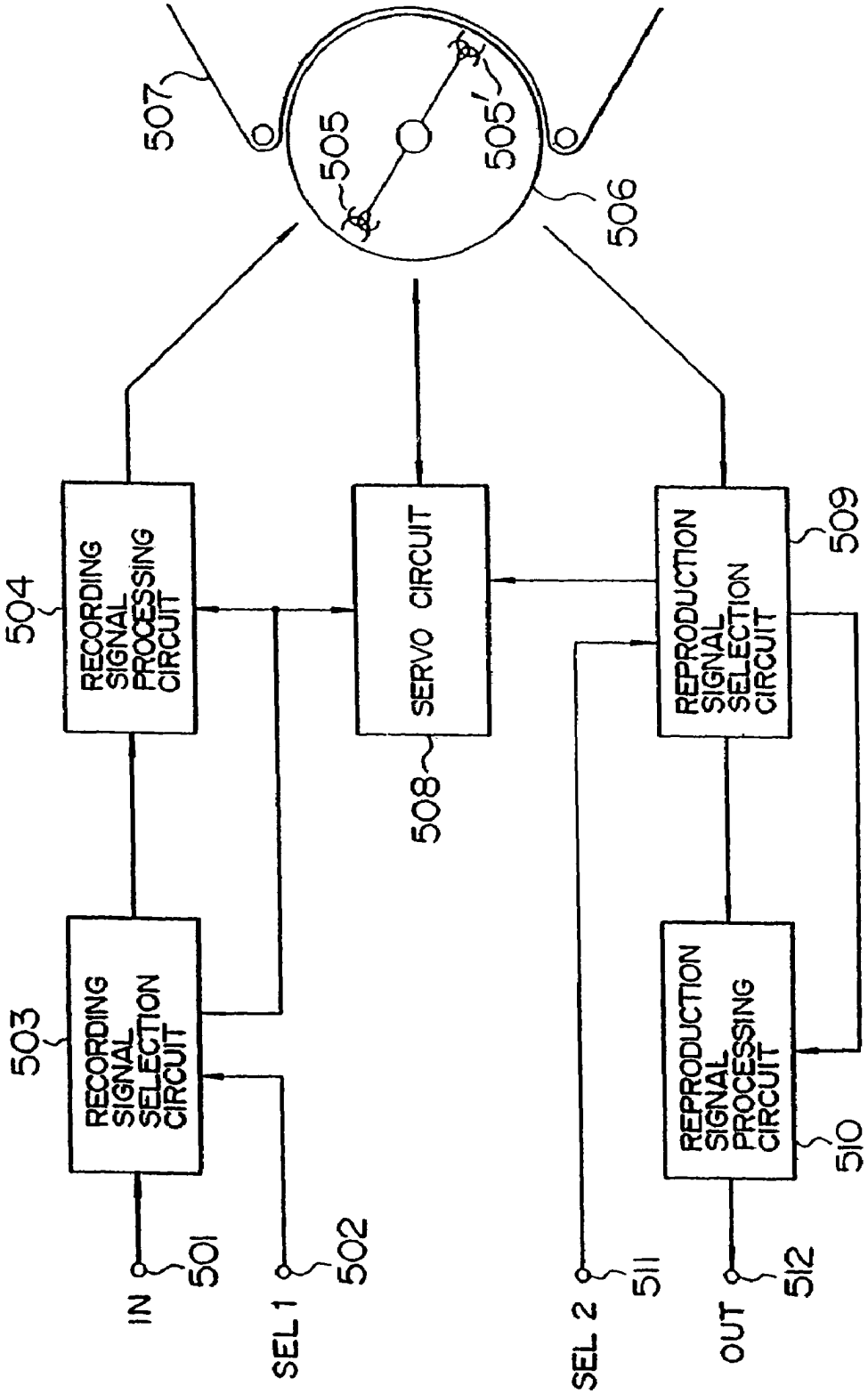

507
505
505'
506
504
RECORDING SIGNAL PROCESSING CIRCUIT
SERVO CIRCUIT
508
REPRODUCTION SIGNAL SELECTION CIRCUIT
509
503
RECORDING SIGNAL SELECTION CIRCUIT
REPRODUCTION SIGNAL PROCESSING CIRCUIT
510
IN
501
SEL 1
502
SEL 2
511
OUT
512

FIG. 19

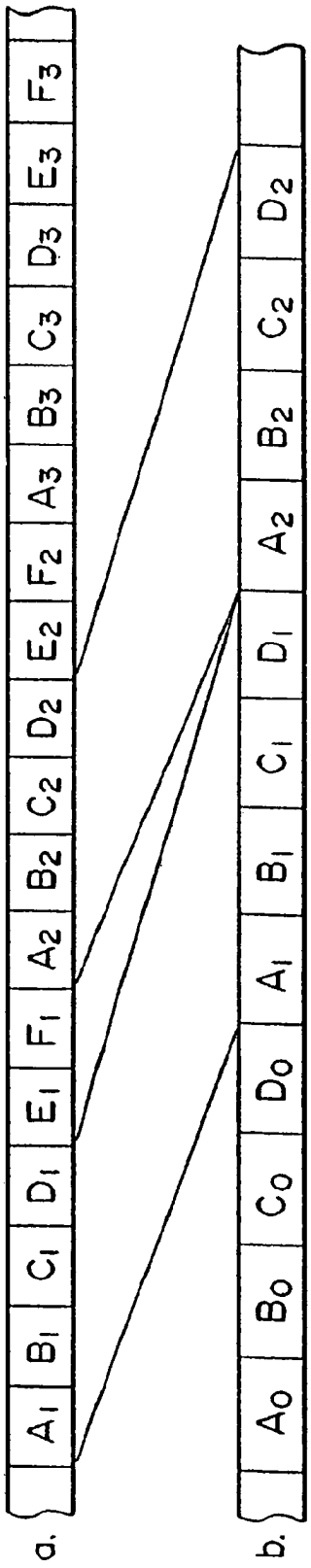
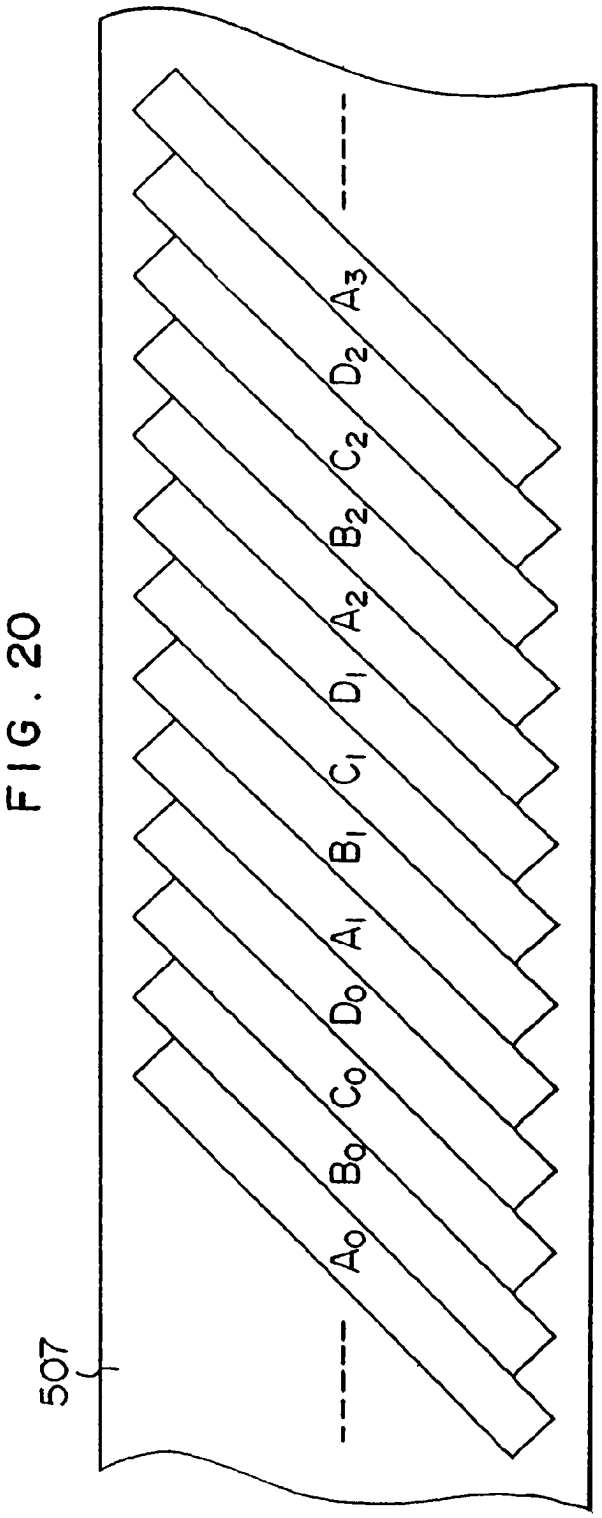

a.
A1 B1 C1 D1 E1 F1 A2 B2 C2 D2 E2 F2 A3 B3 C3 D3 E3 F3
b.
A0 B0 C0 D0 A1 B1 C1 D1 A2 B2 C2 D2

FIG. 20


507
A0 B0 C0 D0 A1 B1 C1 D1 A2 B2 C2 D2 A3

APPARATUS FOR RECEIVING COMPRESSED DIGITAL INFORMATION

CROSS REFERENCE TO RELATED APPLICATIONS

This is a continuation of U.S. application Ser. No. 11/305,229, filed Dec. 19, 2005, now U.S. Pat. No. 7,027,240, which is a continuation of U.S. application Ser. No. 10/404,452, filed Apr. 2, 2003, now U.S. Pat. No. 7,012,769, which is a continuation application of U.S. application Ser. No. 10/277,830, filed Oct. 23, 2002, now U.S. Pat. No. 6,590,726, which is a continuation of U.S. Ser. No. 09/809,047, filed Mar. 16, 2001, now U.S. Pat. No. 6,498,691, which is a continuation application of U.S. application Ser. No. 09/654,962, filed Sep. 5, 2000, now U.S. Pat. No. 6,324,025, which is a continuation of U.S. Ser. No. 09/567,005, filed May 9, 2000, now U.S. Pat. No. 6,278,564, which is a continuation application of U.S. Ser. No. 09/326,595, filed Jun. 7,1999, now U.S. Pat. No. 6,069,757, which is a continuation of U.S. application Ser. No. 09/188,303, filed Nov. 10, 1998, now U.S. Pat. No. 6,002,536, which is a continuation of U.S. application Ser. No. 08/917,176, filed Aug. 25, 1997, now U.S. Pat. No. 5,862,004, which is a continuation of U.S. application Ser. No. 08/620,879, filed Mar. 22, 1996, now U.S. Pat. No. 5,699,203, and copending with U.S. application Ser. No. 08/620,880, filed Mar. 22, 1996, now U.S. Pat. No. 5,673,154, which are continuations of U.S. application Ser. No. 08/457,597, filed Jun. 1, 1995, now U.S. Pat. No. 5,530,598, which is a continuation of U.S. application Ser. No. 08/457,486, filed Jun. 1, 1995, now U.S. Pat. No. 5,517,368, which is a continuation of U.S. application Ser. No. 08/238,528, filed May 5,1994, now U.S. Pat. No. 5,671 ,095, which is a divisional of U.S. application Ser. No. 07/727,059, filed Jul. 8, 1991, now U.S. Pat. No. 5,337,199, the subject matter of which are incorporated by reference herein. This application relates to U.S. Ser. No. 11/305,052, filed Dec. 19, 2005.

BACKGROUND OF THE INVENTION

The present invention relates to a system for transmitting a digital video signal and recording the received video signal. More particularly, the present invention relates to great extension of the range of use of a digital signal recording/reproducing system by greatly shortening a recording time through transmission of a video signal in a compressed form, and further relates to great extension of the range of use of a digital signal recording/reproducing system by making the number of signals to be recorded and a recording/reproducing time variable.

As a digital magnetic recording/reproducing system (hereinafter referred to as VTR) is conventionally known, for example, a D2 format VTR. In such a conventional digital VTR, the elongation or shortening of a reproducing time is possible by using variable-speed reproduction. However, the prior art reference does not at all disclose high-speed recording in which a recording time is shortened to 1/m, multiple recording in which a plurality of signals are recorded, and the compression/expansion of a recording/reproducing time.

The above-mentioned conventional digital VTR has a feature that a high quality is attained and there is no deterioration caused by dubbing. However, the shortening of a dubbing time is not taken into consideration. Therefore, for example, in the case where a two-hour program is to be recorded, two hours are required. Thus, there is a drawback

that inconveniences are encountered in use. Also, the multiplexing of recording signals is not taken into consideration. Therefore, for example, when two kinds of programs are to be simultaneously recorded or reproduced, two VTR's are required. This also causes inconveniences in use.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a digital VTR in which high-speed recording onto a tape can be made with the same format as that used in standard-speed recording, to provide a transmission signal processing system for transmitting at a high speed a video signal to be recorded by such a digital VTR, and to extend the range of use of the digital VTR by shortening a recording time. For example, the digital VTR can be used in such a manner that a two-hour program is recorded in about ten minutes and is reproduced at a standard speed.

The above object is achieved as follows. A video signal and an audio signal are subjected to time-base compression to 1/m, bit compression to 1/n, addition of a parity signal and modulation, and are thereafter transmitted or outputted. The transmitted signal is received, is subjected to demodulation, error correction, addition of a parity signal and modulation, and is thereafter recorded, onto a magnetic tape which travels at a travel speed m times as high as that upon normal reproduction, by use of a magnetic head on a cylinder which rotates at a frequency m times as high as that upon normal reproduction. The signal on the magnetic tape traveling at a travel speed upon normal reproduction is reproduced by a magnetic head on the cylinder which rotates at a frequency upon normal reproduction. The reproduced signal is subjected to demodulation, error correction, bit expansion of video and audio signals and D/A conversion, and is thereafter outputted. Address signals corresponding to a plurality of VTR's may be transmitted prior to a signal to be recorded. Further, control signals indicative of the start of recording and the stop of recording may be transmitted. The transmitted signals are received and error-corrected, and controls of the standby for recording, the start of recording and the stop of recording are made on the basis of the control signals.

With the above construction, since the video signal and the audio signal are time-base compressed to 1/m and bit-compressed to 1/n, a transmission time is shortened to 1/m and a signal band turns to m/n. The time-base compressed and bit-compressed signal is transmitted after addition of a parity signal for error correction and modulation to a code adapted for a transmission path. The transmitted signal is received and demodulated. The detection of an error produced in a transmitting system and the correction for the error can be made using the added parity signal. The error-corrected signal is added with a parity signal for correction for an error produced in a magnetic recording/reproducing system and is modulated to a code adapted for the magnetic recording/reproducing system. Upon recording, since the rotation frequency of the cylinder and the travel speed of the magnetic tape are increased by m times, the recording onto the magnetic tape can be made at an multiple speed. Upon reproduction, by setting the rotation frequency of the cylinder and the travel speed of the magnetic tape to normal ones, the reproduction at a normal speed can be made. The reproduced signal is code-demodulated. The detection of an error produced in the magnetic recording/reproducing system and the correction for the error can be made on the basis of the parity signal. By bit-expanding the video signal and the audio signal compressed by the transmission signal processing system, the original video

and audio signal can be restored. The bit-expanded signal is converted into an analog signal by a D/A converter. Simultaneous and selective control of the start/stop of recording for a multiplicity of VTR's can be made in such a manner that the address signals corresponding to the VTR's are transmitted prior to a signal to be recorded, the correction for an error of the received signal is made, required VTR's are brought into recording standby conditions by the corrected address signals, and the controls of the start of recording and the stop of recording are made by the transmitted control signals.

Another object of the present invention is to provide a digital signal recording/reproducing system in which multiple recording onto a tape can be made with the same format as that used in standard recording and simultaneous multiple reproduction is possible, and to extend the range of use of a digital VTR by compressing/expanding a recording/reproducing time in accordance with the transmission rate of a multiplexed input/output signal and the number of signals in the multiplexed input/output signal.

This object is achieved as follows. There are provided means for selecting one or plural desired signals from a time-base compressed and time-division multiplexed digital input signal, and helical scan recording means for making time-division multiplex recording of the selected signals with a time-base compressed speed after selection being retained. There is further provided means for reproducing the recorded signals with the rotation speed of a cylinder, a tape speed and so on being set to values proportional to the transmission rate of a reproduction signal and the number of signals to be simultaneously reproduced and with the signal being time-base expanded or being retained as time-base compressed.

With the above construction, N kinds of desired signals selected from the multiplexed input digital signal and time-base compressed to 1/K are subjected to time-division multiplex recording with a time-base compressed speed after selection being retained. Upon reproduction, for example, if both the cylinder rotation speed and the tape speed are set to N/K times, a recording track and a reproducing track coincide with each other and the use of a reproducing time K/N times as long as a recording time enables the reproduction of each of the N kinds of signals at a standard speed. Also, if both the cylinder rotation speed and the tape speed are set to (M×N)/K times, a recording track and a reproducing track coincide with each other and the use of a reproducing time as K/(M×N) times as long as the recording time enables the reproduction of each of the N kinds of signals at an M-tuple speed. In the case where L kinds of signals are selected from among the N kinds of reproduced signals and a processing speed at a reproduction signal processing circuit is set to L×M times as long as a standard reproduction processing speed, each of the L kinds of signals among the N kinds of multiple-recorded signals is outputted at a speed M times as high as a standard speed.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a digital transmission signal processing system and a recording/reproducing system according to an embodiment of the present invention;

FIG. **2** is a block diagram of a recording/reproducing system according to another embodiment of the present invention;

FIG. **3** is a diagram for explaining the conventional parity adding method;

FIG. **4** is a block diagram of a recording/reproducing system according to still another embodiment of the present invention;

FIG. **5** is a block diagram of a digital transmission signal processing system and a recording/reproducing system according to a further embodiment of the present invention;

FIG. **6** shows the format of control signals used in one of applications of the present invention;

FIG. **7** is a block diagram of a still further embodiment of the present invention;

FIG. **8** shows one example of the specification of signals to be recorded;

FIG. **9** is a block diagram of a furthermore embodiment of the present invention;

FIGS. **10**, **11** and **12** are block diagrams of different examples of applications of the present invention;

FIG. **13** is a block diagram for explaining one example of the operation of the embodiment shown in FIG. **7**;

FIG. **14** is a timing chart showing the waveforms of signals involved in the example shown in FIG. **13**;

FIG. **15** is a block diagram for explaining another example of the operation of the embodiment shown in FIG. **7**;

FIG. **16** is a timing chart showing the waveforms of signals involved in the example shown in FIG. **15**;

FIG. **17** is a table showing some applications of the examples shown in FIGS. **13** and **15**;

FIG. **18** is a block diagram of a still furthermore embodiment of the present invention; and

FIGS. **19** and **20** are signal diagrams for explaining different operations of the embodiment shown in FIG. **18**.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of the present invention will now be explained by use of FIG. **1**. In the figure, reference numerals **1** and **40** denote magnetic tapes, numerals **2**, **3**, **41** and **42** magnetic heads, numerals **4** and **43** cylinders, numerals **5** and **44** capstans, numerals **10** and **50** servo control circuits, numerals **20**, **31** and **60** demodulation circuits, numerals **21**, **32** and **61** error correction circuits, numerals **22** and **23** compression circuits, numerals **24** and **33** parity addition circuits, numerals **25** and **34** modulation circuits, numerals **26** a transmission circuit, numeral **27** a transmission path, numeral **30** a reception circuit, numerals **62** and **63** expansion circuits, numerals **64** and **65** D/A conversion circuits, numeral **70** a video signal output terminal, and numeral **71** an audio signal output terminal.

Firstly, the operation of a transmission signal processing system will be explained. Digital video and audio signals recorded on the magnetic tape **1** are reproduced by the magnetic heads **2** and **3** mounted on the cylinder **4** and are inputted to the demodulation circuit **20**. The magnetic tape **1** travels by virtue of the capstan **5**. The travel speed of the magnetic tape **1** and the rotation frequency of the cylinder **4** are, for example, ten times as high as the tape travel speed and the cylinder rotation speed upon normal reproduction. Accordingly, the signal inputted to the demodulation circuit **20** is a signal time-compressed to one tenth. For example, a 120-minute signal recorded on the magnetic tape **1** can be reproduced in 12 minutes.

Generally, in the case where a digital signal is to be recorded on a magnetic recording medium, the signal is recorded after having been modulated into scrambled NRZ code, M^2 code or the like. The demodulation circuit **20** performs a demodulation processing, that is, a signal pro-

cessing for restoring the thus modulated signal into original digital data. The signal demodulated by the demodulation circuit **20** is inputted to the error correction circuit **21** in which erroneous data produced in a magnetic recording/reproducing process is detected and the correction for the erroneous data is made. Further, the signal is separated into a video signal and an audio signal which are in turn inputted to the compression circuits **22** and **23**, respectively. The video signal is bit-compressed through, for example, discrete cosine conversion. The audio signal is bit-compressed through, for example, non-linear quantization or differential PCM. As a result, the transmission rate of the video signal and the audio signal in total is reduced to, for example, one twentieth.

Output signals of the compression circuits **22** and **23** are inputted to the parity addition circuit **24** for performing a signal processing which includes adding a parity signal for error correction and outputting the video signal and the audio signal serially in accordance with a transmission format. A serial output signal of the parity addition circuit **24** is inputted to the modulation circuit **25**. In the modulation circuit **25**, the serial signal is modulated in accordance with the characteristic and the frequency band of the transmission path **27**. For example, in the case where the signal is transmitted in an electric wave form, quadruple phase shift keying (QPSK) is made. The modulated signal is inputted to the transmission circuit **26** from which it is outputted to the transmission path **27**.

As apparent from the foregoing explanation of the operation of the transmission signal processing system, it is possible to transmit a signal at a speed which is ten times as high as a normal speed.

The above embodiment has been shown in conjunction with the case where a signal from the VTR is reproduced. However, a signal source is not limited to the VTR and may include a magnetic disk device, an optical disk device or the like.

Next, explanation will be made of the operation of the VTR for receiving and recording the transmitted signal. The signal transmitted from the transmission signal processing system is received by the reception circuit **30**. The received signal is inputted to the demodulation circuit **31**. The demodulation circuit **31** is provided corresponding to the modulation, as provided by the modulation circuit **25**, such as QPSK modulation, for example, and demodulates the modulated signal to the original signal. The demodulated signal is inputted to the error correction circuit **32** in which the detection of and the correction for an error produced in the transmission path **27** are made on the basis of the parity signal added by the parity addition circuit **24**. At this time, in the case where the S/N ratio of the transmission system is not sufficient so that complete correction for the error is impossible, correction is made through, for example, signal replacement, by use of the signal correlation.

An output signal of the error correction circuit **32** is inputted to the parity addition circuit **33**. In the parity addition circuit **33**, a parity signal for detecting an error produced in a recording/reproducing process and making correction for the error is added. The parity-added signal is inputted to the modulation circuit **34**. In the modulation circuit **34**, the signal is modulated to scrambled NRZ code, M^2 code or the like as mentioned above. The modulated signal is recorded on the magnetic tape **40** by the magnetic heads **41** and **42** mounted on the cylinder **43**.

Since the signal supplied to the magnetic heads **41** and **42** is a signal which is time-base compressed to one tenth as compared with a signal upon normal operation, the servo control circuit **50** controls the cylinder **43** and the capstan **44** so that the rotation frequency of the cylinder **43** and the travel speed of the magnetic tape **40** become ten times as high as those upon normal recording. Also, in order to record a predetermined signal at a predetermined position on the magnetic, tape **40**, synchronization information is detected from the received signal to control the phase of rotation of the cylinder **41** on the basis of the detected synchronization information.

Next, the operation of the VTR for reproducing the thus recorded signal will be explained. Upon reproduction, the travel speed of the magnetic tape **40** and the rotation frequency of the cylinder **43** are set to those upon normal reproduction. The reproduced signal is inputted to the demodulation circuit **60**. The demodulation circuit **60** is provided corresponding to the modulation circuit **34** and demodulates the modulated signal. The demodulated signal is inputted to the error correction circuit **61** in which the detection of an error produced in the magnetic recording/reproducing system and the correction for the error are made on the basis of the parity signal added by the parity addition circuit **33**. In the case where there is an error which cannot be corrected, the error is properly corrected by use of the signal correlation. Also, the signal is outputted after having been separated into a video signal and an audio signal.

The video signal is inputted to the expansion circuit **62**. The expansion circuit **62** is provided corresponding to the compression circuit **22** and restores the compressed video signal into the original video signal. An output signal of the expansion circuit **62** is inputted to the D/A conversion circuit **64** and is converted thereby into an analog video signal which is in turn outputted from the terminal **70**.

The audio signal is inputted to the expansion circuit **63**. The expansion circuit **63** is provided corresponding to the compression circuit **23** and restores the compressed audio signal into the original audio signal. An output signal of the expansion circuit **63** is inputted to the D/A conversion circuit **65** and is converted thereby into an analog audio signal which is in turn outputted from the terminal **71**.

In the foregoing, the embodiment of the present invention has been shown and the operation thereof has been explained. According to the present invention, a video signal and an audio signal over a long time can be transmitted and recorded in a short time, thereby making it possible to extend the range of use of the digital VTR.

Another embodiment of the present invention is shown in FIG. **2**. FIG. **2** is partially similar to FIG. **1**. The same parts in FIG. **2** as those in FIG. **1** are denoted by the same reference numerals as those used in FIG. **1** and detailed explanation thereof will be omitted. The embodiment shown in FIG. **2** concerns a VTR in which a signal transmitted/received at a high speed can be recorded while being monitored.

In FIG. **2**, reference numeral **80** denotes a change-over switch, numeral **81** an error correction circuit, and numeral **82** a memory circuit. An error corrected video signal outputted from the error correction circuit **81** is inputted through the memory circuit **82** to a terminal R side of the change over switch **80** which is selected upon recording. The memory circuit **82** has a memory capacity for at least one field. The video signal received at a high speed is stored into a memory of the memory circuit **82** with the number of frames being reduced. The stored signal is read from the memory at a normal speed and is inputted to an expansion circuit **62**.

Upon reproduction, a video signal output of an error correction circuit **61** is inputted to a terminal P side of the

change-over switch **80** which is selected upon reproduction. Accordingly, the operation of the embodiment of FIG. **2** upon reproduction is similar to that of the embodiment shown in FIG. **1**.

In the embodiment shown in FIG. **2**, upon recording, the video signal outputted from the error correction circuit **81** is inputted to the expansion circuit **62** through the memory circuit **82**. Alternatively, an output signal of a modulation circuit **34** may be inputted to a demodulation circuit **60** through a memory circuit. Also, in the case where the operating speed of the demodulation circuit **60** or the error correction circuit **61** leaves a margin, a memory circuit may be properly placed at a post stage. Or, in the case where the storage capacity of the error correction circuit **61** or the expansion circuit **62** leaves a margin, the circuit may be used as a memory circuit or any additional memory circuit may be omitted.

As has been explained in the above, the embodiment shown in FIG. **2** makes it possible to record a received video signal while monitoring it in the form of a picture having a reduced number of frames.

In the embodiment shown in FIG. **1**, the parity signal is added in order to make the detection of and the correction for an error which may be produced in the transmission system or the magnetic recording/reproducing system. One example of a parity adding method is shown in FIG. **3** in conjunction with the case of a D2 format VTR. In the D2 format VTR, a signal for one field is divided into a plurality of segments for signal processing. FIG. **3** shows one segment. In FIG. **3**, reference numeral **90** represents a group of video data, numeral **91** a group of outer code parities, and numeral **92** a group of inner code parities. Firstly, outer code parities are added for data of the matrix-like arranged video data group **90** which lie in a vertical direction in FIG. **3**. Thereafter, inner code parities are added for data of the video data group **90** and the outer code parity group **91** lying in a horizontal direction in FIG. **3**, thereby producing a signal to be recorded. Though detailed explanation of the generation of parities will be omitted herein, the parities are generated in accordance with a generating function G(x).

In the embodiment shown in FIG. **1**, if the same parity generation manner is employed by the parity addition circuits **24** and **33**, the error correction circuits **32** and **61** may hold the most part thereof in common. Namely, since the error correction circuits **32** and **61** are circuits which are respectively used upon recording and upon reproduction, it is possible to reduce the circuit scale or size by using the most part of the circuits **32** and **61** in common.

Further, in the case where the same parity generation manner is employed by the parity addition circuits **24** and **33** in the embodiment shown in FIG. **1**, it is possible to further reduce the circuit scale or-size of the recording/reproducing system. The construction in that case is shown in FIG. **4** as still another embodiment of the present invention. FIG. **4** is partially common to FIG. **1** or **2**. The parts in FIG. **4** common to those in FIG. **1** or **2** are denoted by the same reference numerals as those used in FIG. **1** or **2** and detailed explanation thereof will be omitted.

The embodiment shown in FIG. **4** is based on a concept that an error produced in a transmission system and an error produced in a magnetic recording/reproducing system are simultaneously detected and corrected by an error correction circuit **61**. Accordingly, a signal received by a reception circuit **30** is demodulated by a demodulation circuit **31** and is inputted to a modulation circuit **34** without being subjected to error correction and parity addition. The subsequent processing is the same as that in the embodiment shown in FIG. **1** or **2**. Namely, a reproduced signal is inputted to the error correction circuit **61** after demodulation by a demodulation circuit **60**. As mentioned above, an error produced in the transmission system and an error produced in the magnetic recording/reproducing system are simultaneously detected and corrected by the error correction circuit **61** in the reproducing system.

In the embodiment shown in FIG. **4**, the error correction circuit **32** and the parity addition circuit **33** can be removed as compared with the embodiment shown in FIG. **1** or **2**, thereby making it possible to reduce the circuit scale.

Though having not been mentioned in the foregoing embodiments, in a helical scan VTR as shown, since a signal becomes discontinuous when a track jump is made upon reproduction, the recording is made with an amble signal being added to the heading portion of a signal. Since the addition of an amble signal is employed in the D2 format VTR, detailed explanation thereof will be omitted. Also, in order to define a starting position of a signal, a synchronizing signal is properly added. Since the addition of a synchronizing signal is known in, for example, the D2 format VTR, detailed explanation thereof will be omitted.

In the embodiment shown in FIG. **1**, the addition of an amble signal may be made by the parity addition circuit **24**. Alternatively, it may be made on the recording/reproducing system side in order to enhance the efficiency of use of the transmission path **27**. In this case, the addition of an amble signal can be made by the parity addition circuit **33**. As for the embodiment shown in FIG. **4**, in the case where the addition of an amble signal is to be made on the recording/reproducing system side, the amble signal can be added by the modulation circuit **34**. In the case where the addition of an amble signal is made on the recording/reproducing system side, it is possible to enhance the efficiency of use of the transmission path **27**. On the other hand, in the case where the addition of an amble signal is made on the transmission signal processing system side, the lowering of the cost of a VTR can be attained as a great effect when a signal is sent to a multiplicity of VTR's simultaneously.

FIG. **5** shows a further embodiment of the present invention in which the further reduction of the circuit scale of a VTR on the receiving side and hence the further lowering of the cost can be attained in the case where a signal is sent to a multiplicity of VTR's simultaneously.

FIG. **5** is partially common to FIG. **1**, **2** or **4**. The parts in FIG. **5** common to those in FIG. **1**, **2** or **4** are denoted by the same reference numerals as those used in FIG. **1**, **2** or **4** and detailed explanation thereof will be omitted. In FIG. **5**, reference numeral **100** denotes a modulation circuit. The embodiment shown in FIG. **5** is based on a concept that a signal processing required upon a recording mode of a VTR is performed on the transmitting side. Namely, modulation adapted for magnetic recording/reproduction, for example, a signal processing corresponding to the modulation circuit **34** shown in FIG. **4** is performed on the transmission signal processing system side. After parities have been added by a parity addition circuit **24** of the transmission signal processing system, the modulation adapted for the magnetic recording/reproduction is performed by the modulation circuit **100**. Therefore, modulation adapted for transmission is performed by a modulation circuit **25**. As a modulation system employed by the modulation circuit **100** is suitable a system which does not cause the extension of a frequency band by modulation, for example, scrambled NRZ. A signal modulated by the modulation circuit **25** is transmitted to a transmission path **27** through a transmission circuit **26** in a manner to that in the embodiment shown in FIG. **1**.

The signal received by a reception circuit **30** through the transmission path **27** is inputted to a demodulation circuit **31** in which the signal is subjected to demodulation corresponding to the modulation circuit **25**. Since the signal demodulated by the demodulation circuit **31** is one which has already been subjected by the modulation circuit **10** to the modulation adapted for the magnetic recording/reproduction, the signal is recorded on a magnetic tape **40** by magnetic heads **41** and **42** as it is. As a result, the same recording as that in the embodiment shown in FIG. **4** is made. An operation upon reproduction is similar to that in the embodiment shown in FIG. **4**.

As apparent from the above, the present embodiment makes it possible to remarkably reduce the circuit scale of the VTR.

According to one of applications of the present invention, it is possible to transmit a signal from a transmission signal processing system to a multiplicity of VTR's through a transmission path simultaneously and at a high speed, as has already been mentioned. In this case, it is difficult to control a multiplicity of VTR's simultaneously. Further, it is required to make a control which causes specified ones of the VTR's to perform recording operations and specified others of the VTR's not to perform recording operations. A technique for realizing such a control will be shown just below.

For the above purpose, control signals are transmitted prior to transmission of a signal to be recorded. One example of the control signals is shown in FIG. **6**. In the figure, reference numeral **110** denotes a synchronizing signal, numeral **111** an ID signal indicative of a control to be made, numeral **112** an address signal indicative of a VTR to be controlled, numeral **113** a control signal for bringing a VTR designated by the address signal **112** into a recording mode, numeral **114** a control signal for stopping the recording, numerals **115** and **116** blank signals, and numeral **120** a recording signal to be actually recorded.

The ID signal **111** indicating the transmission of the address signals **112** indicative of VTR's in which a signal is to be recorded, is transmitted at a predetermined position relative to the synchronizing signal **110** to bring each VTR into a standby condition. After all the address signals have been transmitted, the ID signal **113** is transmitted to start the recording of the signal **120** in the designated VTR's. After the signal **120** has been transmitted, the ID signal **114** to control the stop of recording is transmitted. Each of the blank signals **115** and **116** is a signal for conforming a signal transmission format to the other transmission signal and is therefore an insignificant signal portion.

In the embodiments shown in FIGS. **1** and **5**, those control signals are produced by a control signal generation circuit **130** and are transmitted with parities which are added by the parity addition circuit **24** for making correction for an error produced during transmission.

In the VTR shown in FIG. **1**, the control signals are detected by a control circuit **131** after the reception by the reception circuit **30**, the demodulation by the demodulation circuit **31** and the correction by the error correction circuit **32** for an error produced during transmission to make a control for the recording and the stop of recording in the recording/reproducing system.

In the case of the VTR's shown in FIGS. **4** and **5**, an output signal of the demodulation circuit **31** is inputted to the error correction circuit **61** for a need of making correction for an error produced during transmission and error-corrected control signals are inputted to a control circuit **131**. In a change-over circuit **132**, the terminal R side for selecting an output signal of the demodulation circuit **31** is selected upon recording and the terminal P side for selecting an output signal of the demodulation circuit **60** is selected upon reproduction.

As apparent from the foregoing, the present embodiment makes it possible to control a multiplicity of VTR's selectively and simultaneously.

Also, the use of the change-over circuit **132** and a memory circuit makes it possible to record a signal while monitoring it in the form of a picture having a reduced number of frames, as explained in conjunction with the embodiment shown in FIG. **2**.

Next, a still further embodiment of the present invention will be explained by use of FIG. **7**. In the figure, reference numeral **301** denotes an input terminal for standard analog video signal, numeral **302** an input terminal for standard digital video signal, numeral **303** an input terminal for high-speed digital video signal, numeral **305** a recording system mode change-over switch, numeral **306** a recording system change-over signal generation circuit, numeral **310** an A/D converter, numeral **320** a change-over circuit, numeral **330** a data compression circuit, numeral **340** a change-over circuit, numeral **350** a recording system signal processing circuit for performing a signal processing which includes addition of error correction code and modulation for recording, numeral **370** a cylinder, numeral **371** a magnetic tape, numerals **372** and **372'** magnetic heads, numeral **380** a reproducing system signal processing circuit for performing a signal processing which includes demodulation for reproduction, error detection and error correction. Numeral **390** a change-over circuit, numeral **400** a data expansion circuit, numeral **420** a D/A converter, numeral **431** an output terminal for standard analog video signal, numeral **432** an output terminal for standard digital video signal, numeral **433** an output terminal for high-speed digital video signal, numeral **435** a reproducing system mode change-over switch, and numeral **436** a reproducing system change-over signal generation circuit.

The present embodiment is an example of a digital magnetic recording/reproducing system which has recording modes of standard-speed recording and high-speed recording and reproduction modes of standard-speed reproduction and high-speed reproduction. FIG. **8** shows one example of the specification of input video signals.

Firstly, explanation will be made of standard-speed recording. A digital signal into which an analog video signal inputted from the input terminal **301** is converted by the A/D converter **310** or an equivalent digital signal which is inputted from the input terminal **302**, is switched or selected by the change-over circuit **320**, is subjected to a predetermined data compression processing by the data compression circuit **330** and is thereafter inputted to a terminal **340***a* of the changeover circuit **340**. In the change-over circuit **340**, a change-over to connect the terminal **340***a* and a terminal **340***c* is made by a change-over signal from the recording system change-over signal generation circuit **306**. Thereby, the data-compressed signal is inputted to the recording system signal processing circuit **350**. In the recording system signal processing circuit **350**, a signal processing such as channel division, addition of error correction code and modulation for recording is performed at a predetermined processing clock adapted for the data-compressed signal. Thereafter, the signal is supplied to the magnetic heads **372** and **372'** mounted on the cylinder **370** so that it is recorded onto the magnetic tape **371**. The cylinder **370** and the magnetic tape **371** are controlled by a servo control circuit **360**. The servo control circuit **360** controls a cylinder motor

and a capstan motor so as to provide a cylinder rotation speed and a tape speed for standard speed and so as to be synchronized with the input video signal.

Next, explanation will be made of high-speed recording. A high-speed digital video signal inputted from the input terminal **303** is sent to a terminal **340***b* of the change-over circuit **340**. Since the high-speed digital video signal is a signal which has already been subjected to a data compression processing, it is not necessary to pass the signal through the data compression circuit **330**. A change-over to connect the terminal **340***b* and the terminal **340***c* is made by a change-over signal from the recording system change-over signal generation circuit **306** so that the high-speed digital video signal is inputted to the recording system signal processing circuit **350**. In the recording system signal processing circuit **350**, a signal processing similar to that in the case of the standard-speed recording is performed at a predetermined processing clock adapted for the high-speed digital video signal. Thereafter, the signal is supplied to the magnetic heads **372** and **372'** mounted on the cylinder **370** so that it is recorded onto the magnetic tape **371**. The cylinder **370** and the magnetic tape **371** are controlled by the servo control circuit **360**. The servo control circuit **360** control the cylinder motor and the capstan motor so as to provide a predetermined cylinder rotation speed and a predetermined tape speed and so as to be synchronized with the input video signal.

In the present invention, the recording onto the tape can be made with the quite same format in both the standard-speed recording and the high-speed recording, thereby making it possible to greatly shorten a recording time in the high-speed recording mode.

Next, explanation will be made of a signal processing upon reproduction. In the present embodiment, the recording pattern on the magnetic tape is the same whichever of the standard-speed recording and the high-speed recording is selected as a recording mode. Therefore, either standard-speed reproduction or high-speed reproduction can be selected irrespective of the recording mode.

Firstly, the standard-speed reproduction will be explained. The servo control circuit **360** controls the cylinder motor and the capstan motor so that a cylinder rotation speed and a tape speed for standard speed are provided. A signal reproduced by the magnetic heads **372** and **372'** is inputted to the reproducing system signal processing circuit **380**. In the reproducing system signal processing circuit **380**, a signal processing such as demodulation for reproduction, channel synthesis, error detection and error correction is performed at a predetermined processing clock adapted for the standard-speed reproduction. Thereafter, the signal is supplied to a terminal **390***a* of the change-over circuit **390**. In the change-over circuit **390**, a changeover to connect the terminal **390***a* and a terminal **390***c* is made upon standard-speed reproduction by a change-over signal from the reproducing system change-over signal generation circuit **436**. Thereby, the reproduced signal is supplied to the data expansion circuit **400**. In the data expansion circuit **400**, a signal processing reverse to the data compression processing upon recording is performed so that the signal is restored to the original signal. Thereby, the original transmission rate is restored. The data-expanded reproduction signal is sent to the D/A converter **420** on one hand to be outputted as an analog video signal from the output terminal **431** after D/A conversion and is sent to the output terminal **432** on the other hand to be outputted as a digital video signal therefrom.

Next, explanation will be made of the high-speed reproduction. The servo control circuit **360** controls the cylinder motor and the capstan motor so that a predetermined cylinder rotation speed and a predetermined tape speed adapted for the high-speed reproduction are provided. A signal reproduced by the magnetic heads **372** and **372'** is inputted to the reproducing system signal processing circuit **380**. In the reproducing system signal processing circuit **380**, a signal processing such as demodulation for reproduction, channel synthesis, error detection and error correction is performed at a predetermined processing clocks adapted for the high-speed reproduction. Thereafter, the high-speed reproduction signal is supplied to the terminal **390***a* of the change-over circuit **390**. In the change-over circuit **390**, a change-over to connect the terminal **390***a* and a terminal **390***b* is made upon high-speed reproduction. Thereby, the high-speed digital video signal is outputted from the output terminal **433**.

A furthermore embodiment of the present invention will be explained by use of FIG. **9**. The construction of the present embodiment is similar to that of the embodiment shown in FIG. **7** but is different therefrom in that the change-over circuit **340** is placed at a different position, the change-over circuit **390** used in FIG. **7** is eliminated and a change-over circuit **345** is newly added.

An input/output signal upon standard-speed recording/reproduction in the present embodiment is the same as that in the embodiment shown in FIG. **7**. As for high-speed recording and high-speed reproduction, however, the present embodiment is different from the embodiment of FIG. **7** in that the transmission of a high-speed digital video signal is made in the form of a recording format. Accordingly, upon high-speed recording, the high-speed digital video signal is not passed through a recording system signal processing circuit **350** but is recorded onto a tape through the change-over circuit **340** as it is. Upon high-speed reproduction, a reproduced signal is subjected to a signal processing for reproduction such as error detection and error correction by a reproducing system signal processing circuit **380** and is thereafter inputted to a terminal **345***b* of the change-over circuit **345**. The signal supplied through the change-over circuit **345** to the recording system side signal processing circuit **350** is subjected to a signal processing for recording such as addition of error correction code and modulation for recording by the signal processing circuit **350** to form a recording format and is thereafter outputted as a high-speed digital video signal from an output terminal **433**.

The embodiments shown in FIGS. **7** and **9** have feature that high-speed recording and high-speed reproduction are possible. The best use of this feature can be made for dubbing or data communication with the result of effective shortening of a dubbing time, a data communication time or a data circuit line occupation time. Also, though those embodiments have been mentioned in conjunction with an example in which all of standard-speed recording, high-speed recording, standard-speed reproduction and high-speed reproduction modes are involved, it is not necessarily required to implement all of those modes. There may be considered an example in which only a necessary mode is provided in compliance with the purpose of use. FIG. **10** shows an embodiment in which a high-speed recording function is provided as a recording mode and at least a high-speed reproduction function is provided as a reproduction mode. Also, there may be considered an embodiment as a system for the exclusive use for reproduction in which at least a high-speed reproduction function is provided, as shown in FIG. **11**. Further, FIG. **12** shows an embodiment in which a high-speed recording function is provided as a

recording mode and a standard-speed reproduction function is provided as a reproduction mode.

FIG. **13** is a block diagram of one example of the magnetic recording/reproducing system of the embodiment of FIG. **7** for explaining processings subsequent to the compression processing. In FIG. **13**, reference numeral **201** denotes a synchronization detection circuit, numeral **204** a recording modulation circuit, numeral **205** a cylinder servo control circuit, numeral **206** a capstan servo (or tape speed) control circuit, numeral **207** a reproduction reference signal generation circuit, numeral **210** a demodulation circuit, numeral **211** a cylinder, numeral **212** a pair of recording heads, numeral **213** a pair of reproducing heads, numeral **214** a capstan which controls the tape speed, numeral **215** a magnetic tape, numeral **216** a delivery reel, and numeral **217** a take-up reel. FIG. **14** is a timing chart of input and output signals in the example shown in FIG. **13** and schematically illustrate a compressed picture signal **251** which is an input signal, a synchronizing signal **252** of the picture signal, a standard-speed reproduction signal **255** which is an output signal, and a reproduction synchronizing signal **256**.

In the shown example, n-tuple speed recording is realized by making a tape speed and a cylinder rotation speed upon recording ntimes as high as those upon standard-speed reproduction. As shown in FIG. **14**, the compressed video signal as an input signal of the circuit shown in FIG. **13** and the synchronizing signal include information **251** for n pictures and n synchronizing pulses **252** synchronous therewith in a time when one picture is reproduced at a standard speed. The picture information is converted into a predetermined recording format by the recording modulation circuit **204** and is recorded onto the magnetic tape **215** by the recording heads **212**. At this time, a synchronizing signal for the cylinder servo control circuit **205** and the capstan-servo control circuit **206** is increased by n times in compliance with the n-tuple speed video signal, as shown by **252** in FIG. **14**, so that the rotation speed of the cylinder **211** and the feed speed of the magnetic tape **215** are increased by n times. Thereby, the recording onto the tape can be made with the quite same recording format as that in the case of the standard-speed recording. Upon reproduction, a synchronizing signal for the cylinder servo control circuit **205** and the capstan servo control circuit **206** is supplied from the reproduction reference signal generation circuit **207** to restore the cylinder rotation speed and the tape feed speed to those upon standard-speed reproduction, and a signal read by the reproducing heads **213** is demodulated by the demodulation circuit **210** and is outputted therefrom. In the circuit shown in FIG. **13**, if the input video signal and the synchronizing signal are ones of standard speed, standard-speed recording is possible. Also, n-tuple speed reproduction is possible if the frequency of an output signal from the reproduction reference signal generation circuit is increased by n times.

FIG. **15** is a block diagram of another example of the magnetic recording/reproducing system of the embodiment of FIG. **7** for explaining processings subsequent to the compression processing. FIG. **16** is a timing chart of input and output signals in the example shown in FIG. **15**. In FIG. **15**, the same reference numerals as those used in FIG. **13** denote the same or equivalent components as or to those shown in FIG. **13**. In FIG. **15**, reference numeral **202** denotes a ÷m circuit, numeral **203** recording system memories, numeral **208** a ÷m circuit, and numeral **209** reproducing system memories. In FIG. **16**, the same reference numerals as those used in FIG. **14** denote the same or equivalent signals as or to those shown in FIG. **14**. In FIG. **16**, reference numeral **253** denotes outputs of the recording system memories **203** and numeral **254** denotes an output of the ÷m circuit **208** or a synchronizing signal divided by m.

The embodiment shown in FIG. **15** is an example in which m pairs of recording heads are used to simultaneously record magnetic signals for m pictures on m tracks, thereby realizing high-speed recording while suppressing an increase in the cylinder rotation speed. Upon reproduction, m pairs of reproducing heads are used. Though FIG. **15** shows the case where two pairs of recording heads **212** are used to simultaneously record information for two pictures on two tracks, three or more pairs of heads can be used in a similar manner.

FIG. **17** is a table showing some examples of the tape speed and the cylinder rotation speed (rpm) in the embodiments shown in FIGS. **13** and **15**. In the table, high-speed recording or reproduction at a speed ten times as high as the standard speed is shown by way of example. Design for implementing another high-speed recording or reproduction is similarly possible. In the table shown in FIG. **17**, examples (①, ② and ③ correspond to the embodiment shown in FIG. **13** and examples ④ and ⑤ correspond to the embodiment shown in FIG. **15**.

A still furthermore embodiment of a digital signal recording/reproducing system of the present invention will be explained by use of a block diagram shown in FIG. **18**.

In FIG. **18**, reference numeral **501** denotes a signal input terminal to which a plurality of video signals are inputted in a time-division multiplex form, numeral **502** a recording selection signal-input terminal to which a recording selection signal for selecting one or plural signals to be recorded from the multiplexed input signal is inputted, numeral **503** a recording signal selection circuit for selecting the signals to be recorded from the multiplexed input signal in accordance with the recording selection signal from the input terminal **502**, numeral **504** a recording signal processing circuit for subjecting the selected signals to a digital processing for recording onto a recording medium, numerals **505** and **505'** magnetic heads, numeral **506** a rotating drum, numeral **507** a magnetic tape or the recording medium, numeral **508** a servo circuit for controlling the rotation of the drum **506** and the travel of the tape **507**, numeral **511** a reproduction selection signal input terminal to which a reproduction selection signal for selecting one or plural signals to be outputted as a reproduction signal from among the multiple-recorded and reproduced signals is inputted, numeral **509** a reproduction signal selection circuit for selecting the signals to be outputted as a reproduction signal from among the multiple-recorded and reproduced signals in accordance with the reproduction selection signal from the input terminal **511**, numeral **510** a reproduction signal processing circuit for subjecting the selected signals to a digital processing, and numeral **512** a reproduction signal output terminal.

The time-division multiplexed input video signal from the signal input terminal **501** is supplied to the recording signal selection circuit **503**. The recording signal selection circuit **503** is also supplied with the recording selection signal from the recording selection signal input terminal **502** to make the selection of signals to be recorded. For example, in the case where six kinds of video signals A, B, C, D, E and F are inputted in a time-division multiplex form as shown in (a) of FIG. **19** and four signals A, B, C and D thereof are to be selected and recorded, an output of the recording signal selection circuit **503** is as shown in (b) of FIG. **19**. Such an output signal of the recording signal selection circuit **503** is inputted to the recording signal processing circuit **504** which

in turn performs a signal processing for recording such as addition of error correction code. Also, the recording signal selection circuit **503** produces a speed control signal on the basis of the number of signals in the time-division multiplexed input video signal, the transmission rate of the input signal and the number of signals to be recorded which are selected by the recording selection signal. The speed control signal is supplied to the recording signal processing circuit **504** and the servo circuit **508**. For example, in the case where the input video signal is time-division multiplexed to sextuplet with each of six signals in the multiplexed input signal being transmitted at a rate time-base compressed to ⅙ and four signals among the six signals in the multiplexed input signal are to be selectively recorded, a signal indicative of a quadruple speed is produced as the speed control signal. Also, in the case where the input video signal is time-division multiplexed to sextuplet with each of six signals in the multiplexed input signal being transmitted at a rate time-base compressed to 1/12 and four signals among the six signals in the multiplexed input signal are to be selectively recorded, a signal indicative of a octuple speed is produced as the speed control signal. Namely, in the case where an input signal is multiplexed to N-plet, the compression rate of each of the N signals in the multiplexed input signal is 1/K and the number of signals to be selectively recorded is L, a speed control signal indicative of an (L×K)/N-tuple speed is produced. The operating speed of the recording signal processing circuit **504** which processes a signal from the recording signal selection circuit **503**, is changed in accordance with the speed control signal. For example, in the case of a speed control signal indicative of a quadruple speed, the recording signal processing circuit **504** performs a signal processing at a speed four times as high as a normal speed and supplies the processed signal to the magnetic heads **505** and **505'**. Here, for example, in the case where the input video signal is time-division multiplexed to sextuplet with each of the six signals in the multiplexed input signal being transmitted at a rate time-base compressed to ⅙ and a speed control signal indicative of a quadruple speed is used to selectively record four signals from among the six signals, the speed of an input signal inputted to the recording signal processing circuit **504** is four times as high as that of one video signal having a normal speed and the recording signal processing circuit **504** processes this quadruple-speed input signal at a quadruple speed and supplies the processed signal to the magnetic heads, thereby making it possible to record all of the four selected signals. Also, if the recording signal selection circuit **503** is constructed so that signals to be selectively recorded are sequentially changed for every one track on the tape, compatibility can be held in regard to the number of signals to be selectively recorded and a processing speed by causing the recording signal processing circuit **504** to perform a completed processing for every one track. In the following, explanation will be made in conjunction with the case where each video signal is recorded in such a form completed for every track. However, it should be noted in advance that the present invention is applicable to another recording system, for example, a system in which signals are recorded in a form changed for every pixel, line or field. On the other hand, the servo circuit **508** supplied with the speed control signal indicative of the quadruple speed controls the rotation speed of the rotating drum **506** so that it becomes four times as high as a normal speed and the travel speed of the magnetic tape **507** so that it becomes four times as high as a normal speed. Thereby, four signals A, B, C and D are alternately recorded on successive tracks of the magnetic tape **507**, as shown in FIG. **20**. According to the control mentioned above, the pattern of recording tracks on the tape becomes the same irrespective of the number of signals in the multiplexed input signal, the transmission rate of each signal and the number of signals to be selectively recorded. In order to make a control upon reproduction easy, it is preferable that the number of selectively recorded signals and the identification codes or signal numbers thereof (for example, A, B, C and D or 0, 1, 2 and 3) are recorded as an ID signal for every track.

In the above example, the recording of the time-division multiplexed signal has been mentioned. However, it is needless to say that the present invention is also applicable to the case where the number of multipet signal components in an input video signal is 1 or the input video signal is not multiplexed. In such a case, since the recording signal processing circuit **504** and the servo circuit **508** operate at speeds proportional to the transmission rate of the input video signal, an effect is manifested, for example, in high-speed dubbing. As apparent from the foregoing explanation of the operation, it is of course that a multiplexed signal can be recorded at a high speed.

Upon reproduction, a signal reproduced from the magnetic tape **507** by the magnetic heads **505** and **505'** mounted on the rotating drum **506** is inputted to the reproduction signal selection circuit **509**. The reproduction signal selection circuit **509** produces a speed control signal, for example, by detecting the number of multiple-recorded signals from the ID signal included in the reproduced signal and sends the speed control signal to the servo circuit **508**. The speed control signal is a signal indicative of a speed four times as high as the normal reproduction speed in the case where the number of multiple-recorded signals is 4 and a signal indicative of a sextuple speed in the case where it is 6. In the case of the quadruple speed, the servo control circuit **508** supplied with the speed control signal indicative of the quadruple speed controls the rotation speed of the rotating drum **506** so that it becomes four times as high as a normal speed and the travel speed of the magnetic tape **7** so that it becomes four times as high as a normal speed. Thereby, there can be traced all of signals recorded so that the recording track pattern on the tape becomes the same irrespective of the number of signals to be selectively recorded. In a system which has not a signal indicative of the number of selectively recorded signals, there may be employed a method in which the speed control signal is manually set. In a system in which the number of signals to be recorded on the tape is fixed, the speed control signal has a fixed value. The reproduction signal selection circuit **509** receives a reproduction selection signal inputted from the reproduction selection signal input terminal **511** to select a desired signal(s) from among the signals reproduced by the magnetic heads **505** and **505'** and to output the selected signal as a reproduction signal to the reproduction signal processing circuit **510**. The reproduction signal selection circuit **509** also outputs a selection number signal indicative of the number of selected signals to the reproduction signal processing circuit **510**.

The reproduction signal processing circuit **510** performs a signal processing such as code error correction processing and picture signal processing for the reproduction signal at a processing speed corresponding, to the selection number signal and outputs the processed reproduction signal from the output terminal **512**. For example, in the case where the number indicated by the selection number signal is 2, the signal processing speed is two times as high as a normal speed and various processings are performed for each selected signal. For example, in the case where signals A and

C are selected, the signals A and C are outputted alternately for each field. In the case where the number indicated by the selection number signal is 1, for example, when the reproduction selection signal from the reproduction selection signal input terminal **511** selects only the signal C, the reproduction signal processing circuit **510** performs the signal processing at the normal speed to output the signal as reproduced at a normal speed. As apparent from the above, the present embodiment makes it possible to simultaneously record any number of signals selected from among a plurality of signals in a multiplexed video signal and to simultaneously reproduce any number of signals from among the recorded signals.

In the case where a plurality of signals are simultaneously reproduced, a construction for outputting the reproduced signals from separate output terminals simultaneously and in parallel may be employed, particularly, in the case of an analog output, as a method other than the construction in which the plurality of reproduced signals are outputted in a time-division multiplex form, as mentioned above. Though in the above-mentioned example the reproduction signal is outputted at a reproduction speed for a usual video signal, the transmission rate of the reproduction signal may be made higher than the reproduction speed for the usual video signal in order to transmit the reproduction signal to another system in an analog or digital signal form at a high rate or to perform high-speed dubbing which is one of effects of the present embodiment. This can be realized in such a manner that the fundamental operating speed of there producing system is set to be higher than a normal reproduction speed and the operating speeds of the servo circuit **508**, the reproduction signal selection circuit **509** and the reproduction signal processing circuit **510** are changed in accordance with the number of multiple-recorded signals and/or the number of signals to be outputted as a reproduction signal with the above fundamental speed being the standard. If the transmission rate of a reproduction signal is made variable so that a rate adapted for a transmission path to which the reproduction signal is to be connected or the performance or function of a recorder by which the reproduction signal is to be recorded, can be selected.

As mentioned above, according to the present embodiment, it is possible to simultaneously record any number of signals selected from among a plurality of signals in a multiplexed video signal and to reproduce any number of signals from among the recorded signals at any speed. Also, in the case where a plurality of signals are selected and reproduced and the plurality of reproduced signals are simultaneously outputted in a time-division multiplex form or from separate output terminals in parallel, it is possible to arbitrarily set the transmission rate of an output signal.

The present embodiment has been explained in conjunction with the case where the present invention is applied to a helical-scan digital-recording VTR. It is of course that a similar effect can be obtained in the case where the present invention is applied to a fixed head VTR. The fixed head system is convenient for the structuring of a system since it has a higher degree of freedom for the setting of the units of division of a signal subjected to time-division multiple recording as compared with the helical scan system. Also, it is of course that the present invention is applicable to a recording/reproducing equipment other than the VTR or is applicable to a digital signal processing and analog recording system.

The present invention can be applied to not only the case where an input signal is time-division multiplexed, as mentioned above, but also the case where a plurality of signals are inputted simultaneously and in parallel. In the latter case, the recording signal selection circuit **503** is constructed to receive the input signals in parallel.

As has been mentioned in the foregoing, according to the present invention, it is possible to realize a digital VTR in which high-speed recording onto a tape can be made with the same format as that used in standard-speed reproduction. Further, there can be realized a transmission signal processing for transmitting at a high rate a video signal to be recorded by such a digital VTR. Also, in the case where a signal transmitted from the transmission signal processing system is to be recorded by a multiplicity of VTR's, it is possible to designate those ones of the multiplicity of VTR's by which recording is to be made and to make a control of the start/stop of recording.

What is claimed is:

1. An apparatus for receiving digital information including at least one of digital video information and digital audio information, comprising:

a receiver which receives the digital information that has digital video information bit-compressed by a first compression system, digital audio information bit-compressed by a second compression system, and error-detection information added to both the digital video information and the digital audio information;

a demodulator which demodulates the digital information received by the receiver;

an error detector which detects an error of digital information demodulated by the demodulator by use of the error-detection information;

a first expander which bit-expands video information among the digital information error detected by the error detector corresponding system; and

a second expander which bit-expands audio information among the digital information error detected by the error detector corresponding to the second compression system.

2. An apparatus according to claim **1**, wherein the first compression system and the second compression system are different systems.

3. An apparatus according to claim **1**, wherein the demodulator affects QPSK demodulation.

4. An apparatus according to claim **1**, further comprising;

an output terminal which outputs the digital information error-detected by the error detector to a recording/reproducing apparatus;

an input terminal which inputs a reproduced signal from the recording/reproducing apparatus; and

a selector which selects one of the digital information error-detected by the error detector and the digital information inputted from the input terminal;

wherein the digital information selected by the selector is bit-expanded by the first expander and the second expander.

5. An apparatus according to claim **1**, wherein the first compression system uses a discrete cosine transform, the received digital information is phase-modulated, and the demodulator demodulates the digital information received by the receiver in accordance with the phase-modulation.

6. An apparatus for processing a transmitted digital signal including at least one of a video signal and an audio signal, comprising:

a receiver which receives the transmitted digital signal, wherein the transmitted digital signal includes a video

signal bit-compressed by a first compression method, an audio signal bit-compressed by a second compression method, and an error correction signal added commonly to both the video signal and the audio signal;

a demodulator which demodulates the digital signal received by the receiver;

an error corrector which corrects an error of the digital signal demodulated by the demodulator based on the error correction signal;

a first expander which bit-expands the video signal of the digital signal corrected by the error corrector in accordance with the first compression method; and

a second expander which bit-expands the audio signal of the digital signal corrected by the error corrector in accordance with the second compression method.

7. The apparatus according to claim **6**, wherein the first compression method utilizes a discrete cosine transform.

* * * * *

EXHIBIT H

US006144412A

United States Patent [19]

Hirano et al.

[11] **Patent Number: 6,144,412**

[45] **Date of Patent: Nov. 7, 2000**

[54] **METHOD AND CIRCUIT FOR SIGNAL PROCESSING OF FORMAT CONVERSION OF PICTURE SIGNAL**

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[21] Appl. No.: **08/950,666**

[22] Filed: **Oct. 15, 1997**

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[51] **Int. Cl.**[7] **H04N 7/01**

[52] **U.S. Cl.** **348/441**; 348/445; 348/448; 348/452; 348/556

[58] **Field of Search** 348/441, 448, 348/449, 451, 452, 458, 459, 443, 554, 555, 556, 558, 581; H04N 7/01, 11/20

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Attorney, Agent, or Firm—Antonelli, Terry, Stout & Kraus, LLP

[57] **ABSTRACT**

In order to carry out format conversion or scaling processing of picture signal by a memory having a small capacity, picture signals of interlace scanning are converted into picture signals of progressive scanning by interpolation by using an IP convertor **1** and a multiple scan convertor **3**, a scaling processing of expansion and compression in the horizontal direction is firstly performed by using a horizontal scaling unit **5**, processing of expansion, compression, frame rate conversion, synchronization and the like are secondly performed by using a vertical scaling unit **6** and commonly using memories used in scaling processing in the vertical direction and finally, color space conversion or inverse gamma processing is performed by using a picture quality improving unit **8** thereby converting the picture signals into picture signals S**6** having a predetermined format.

35 Claims, 28 Drawing Sheets

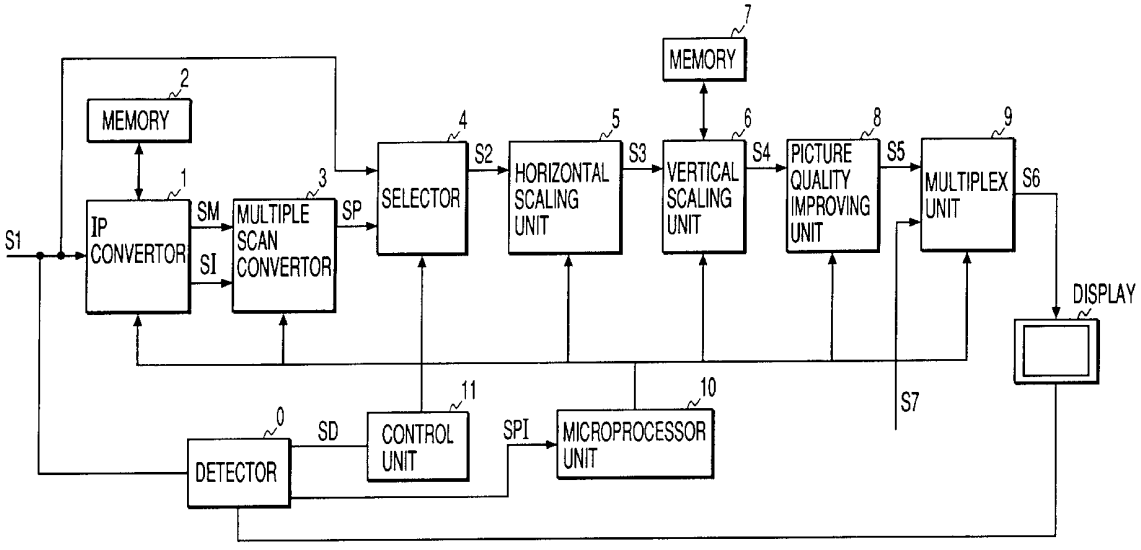


FIG. 1

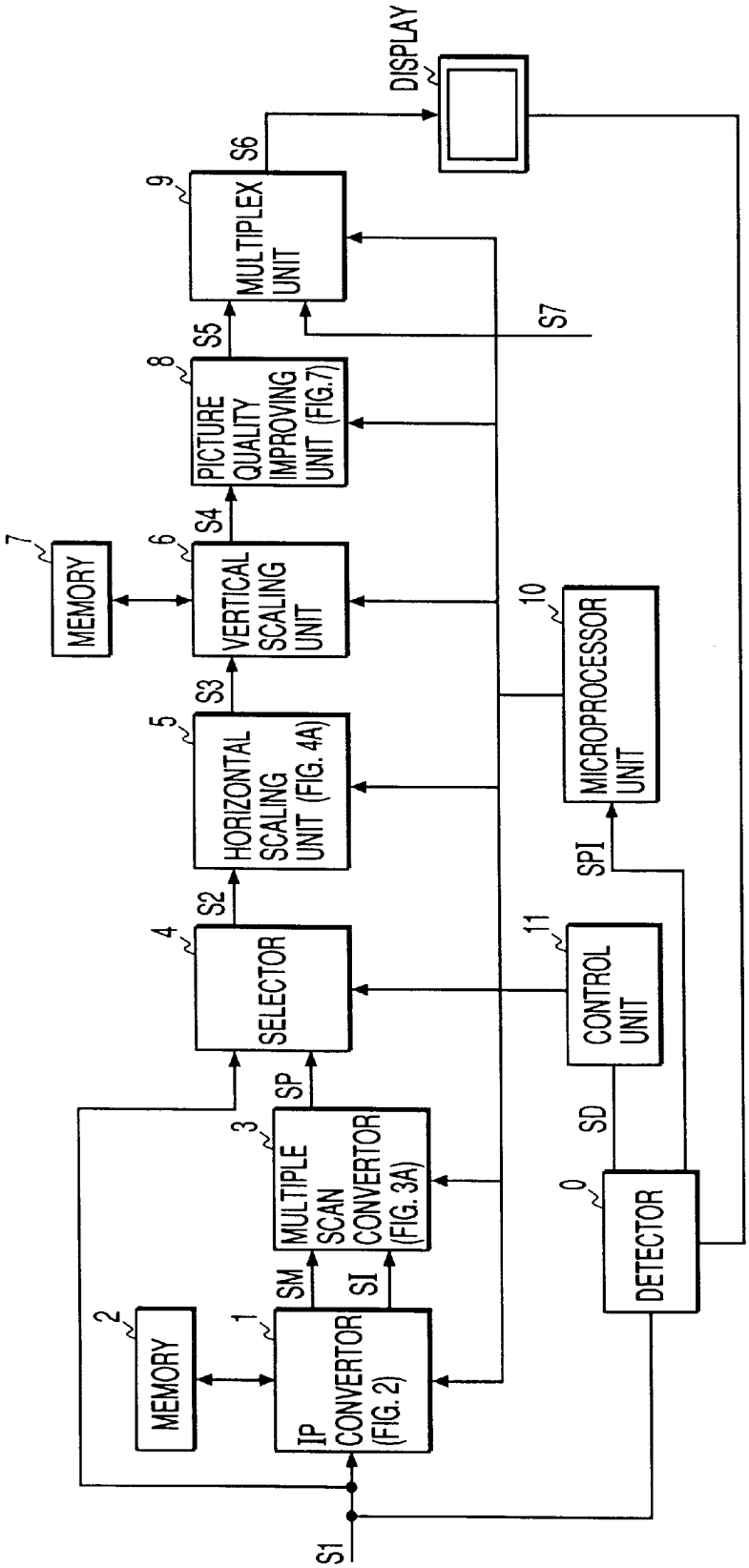

DISPLAY
MULTIPLEX UNIT
PICTURE QUALITY IMPROVING UNIT (FIG.7)
VERTICAL SCALING UNIT
MEMORY
HORIZONTAL SCALING UNIT (FIG. 4A)
MICROPROCESSOR UNIT
SELECTOR
CONTROL UNIT
MULTIPLE SCAN CONVERTOR (FIG. 3A)
DETECTOR
MEMORY
IP CONVERTOR (FIG. 2)
S1
S2
S3
S4
S5
S6
S7
SM
SI
SP
SPI
SD
0
1
2
3
4
5
6
7
8
9
10
11

FIG. 2

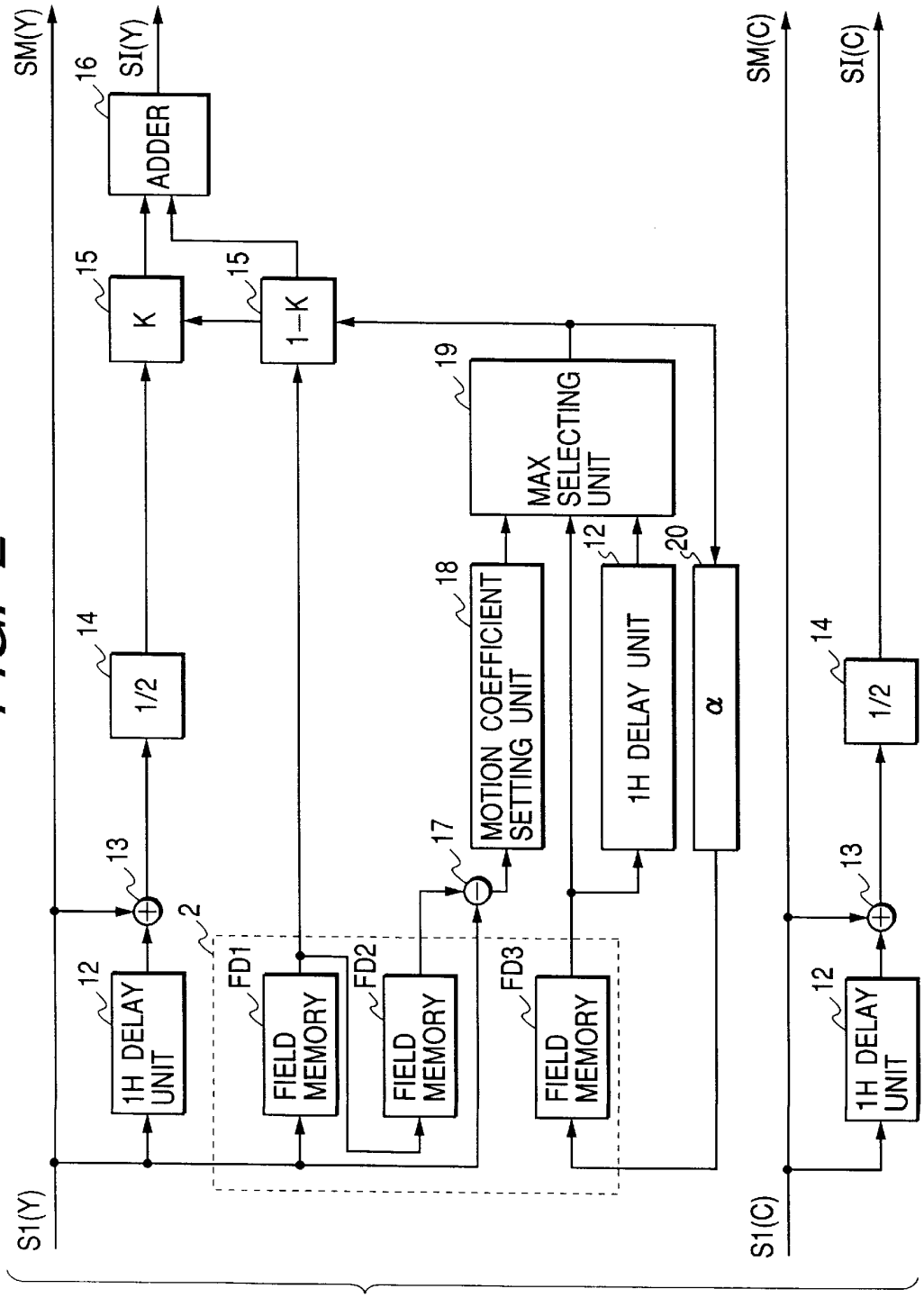

SM(Y)
SI(Y)
16
ADDER
15
K
15
1−K
19
MAX SELECTING UNIT
18
MOTION COEFFICIENT SETTING UNIT
12
1H DELAY UNIT
20
α
14
1/2
13
17
2
FD1
FD2
FD3
FIELD MEMORY
FIELD MEMORY
FIELD MEMORY
12
1H DELAY UNIT
S1(Y)
SM(C)
SI(C)
14
1/2
13
12
1H DELAY UNIT
S1(C)

FIG. 3A

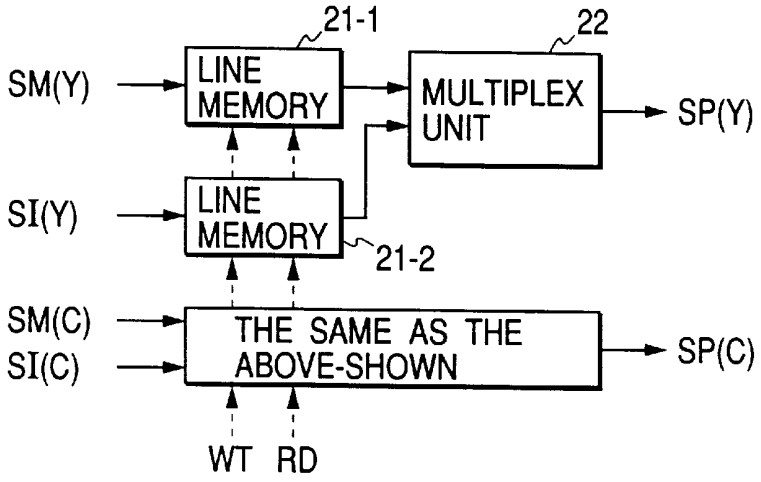
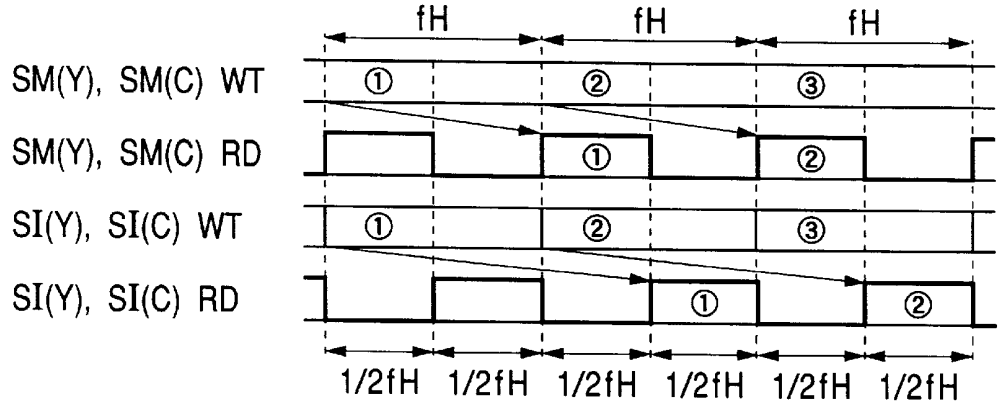


FIG. 3B

[LINE MEMORY OPERATION]



fH : 1H LINE PERIOD OF INTERLACE SCANNING
1/2fH : 1H LINE PERIOD OF PROGRESSIVE SCANNING

FIG. 4A

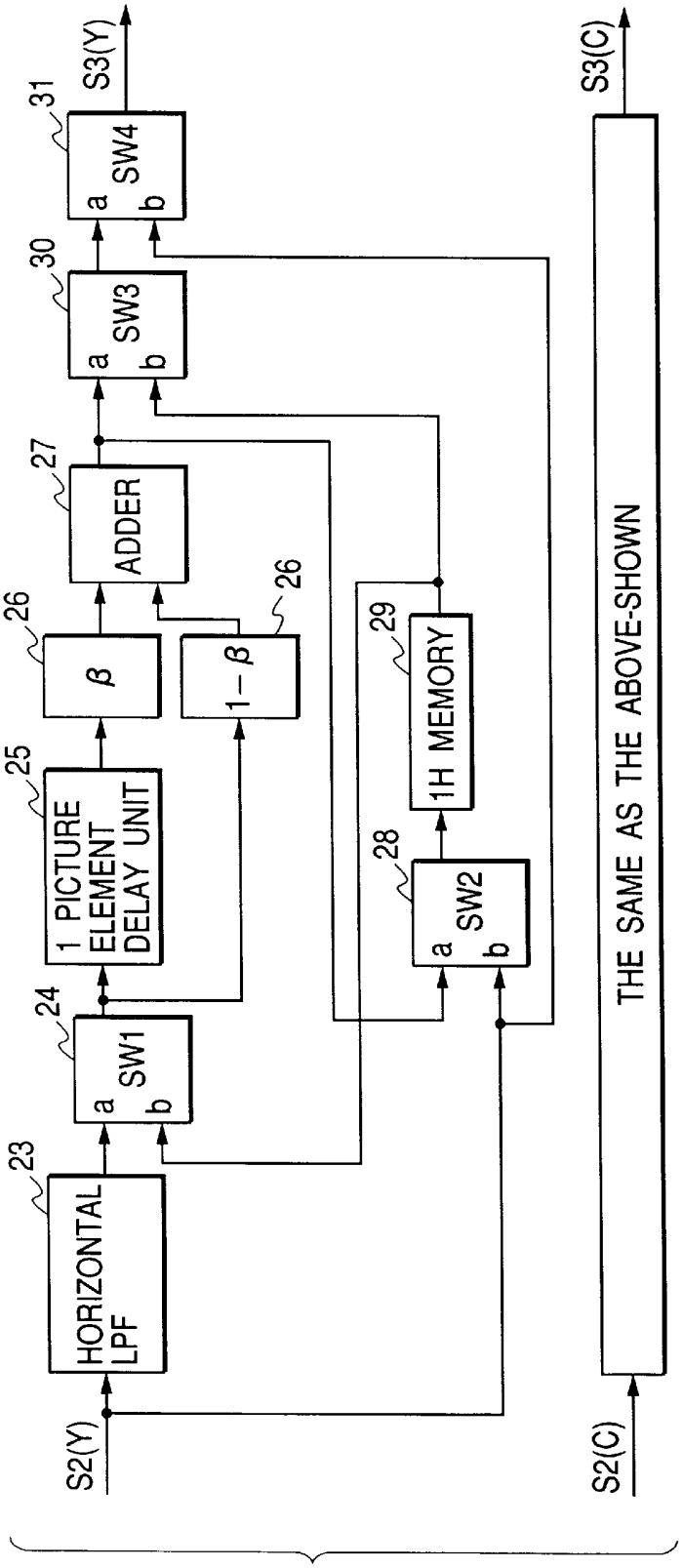

S3(Y)
S3(C)
31
SW4
a
b
30
SW3
27
ADDER
26
β
1 − β
29
1H MEMORY
25
1 PICTURE ELEMENT DELAY UNIT
28
SW2
24
SW1
23
HORIZONTAL LPF
S2(Y)
S2(C)
THE SAME AS THE ABOVE-SHOWN

FIG. 4B

[SWITCH CONTROL]

SIGNAL PROCESSING	SW1	SW2	SW3	SW4
HORIZONTAL COMPRESSION	a	a	b	a
HORIZONTAL EXPANSION	b	b	a	a
THROUGH	–	–	–	b

FIG. 5B

[SWITCH CONTROL]

SIGNAL PROCESSING	SW1	SW2	SW3	SW4
VERTICAL COMPRESSION	a	a	b	a
VERTICAL EXPANSION	b	b	a	a
PAL 100Hz	–	b	b	a
NTSC-PAL 100Hz	b	b	c	a
PAL-NTSC CONVERSION	a	a	b	a
THROUGH	–	–	–	b

FIG. 5A

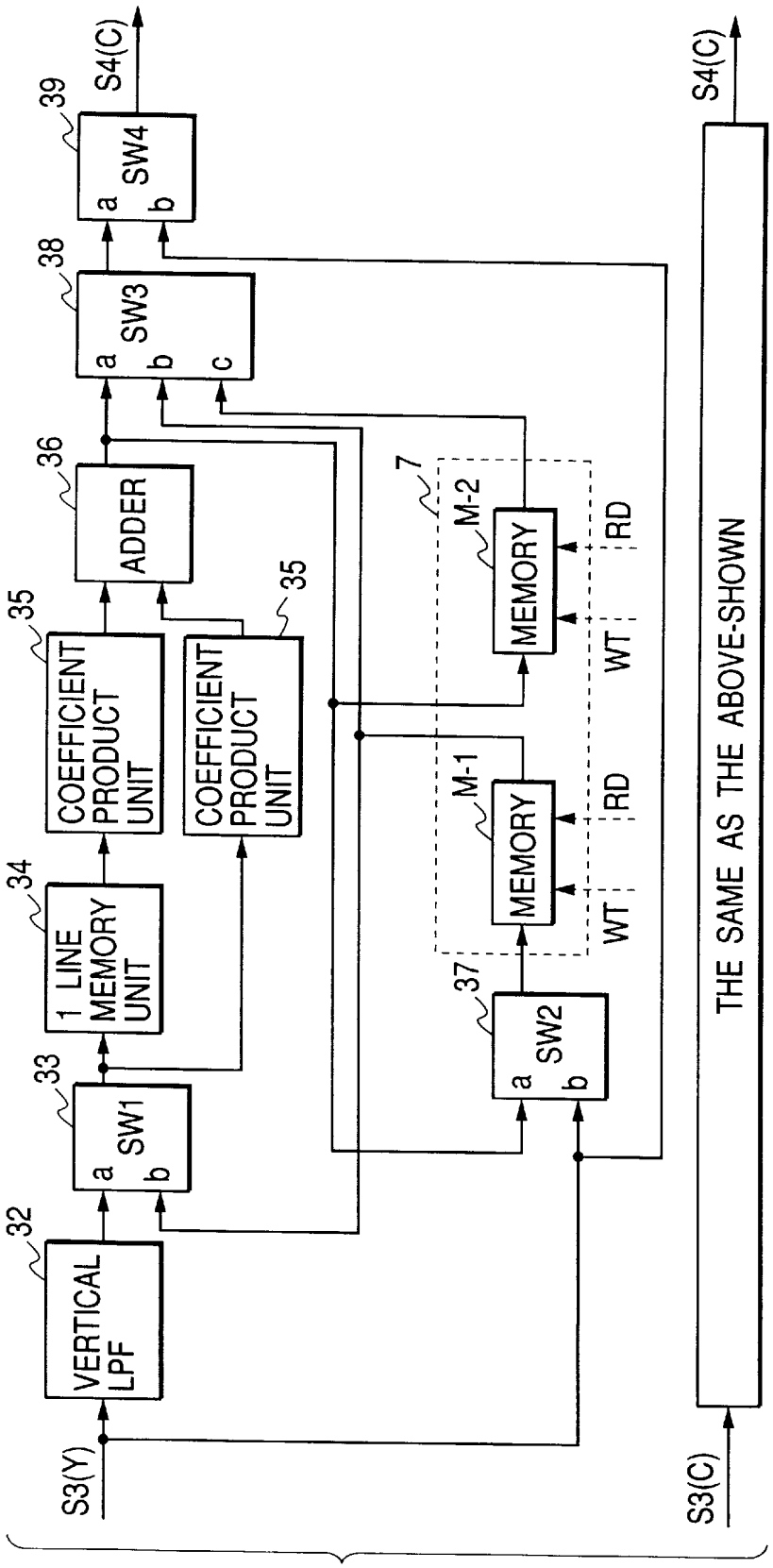

S3(Y)
VERTICAL LPF
32
SW1
33
1 LINE MEMORY UNIT
34
COEFFICIENT PRODUCT UNIT
35
COEFFICIENT PRODUCT UNIT
35
ADDER
36
SW3
38
SW4
39
S4(C)
7
M-2
MEMORY
M-1
MEMORY
RD
WT
RD
WT
37
SW2
THE SAME AS THE ABOVE-SHOWN
S4(C)
S3(C)

FIG. 6A

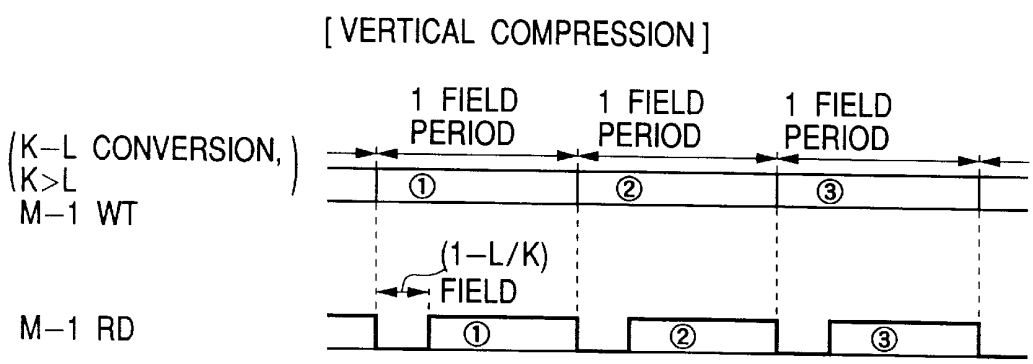


FIG. 6B

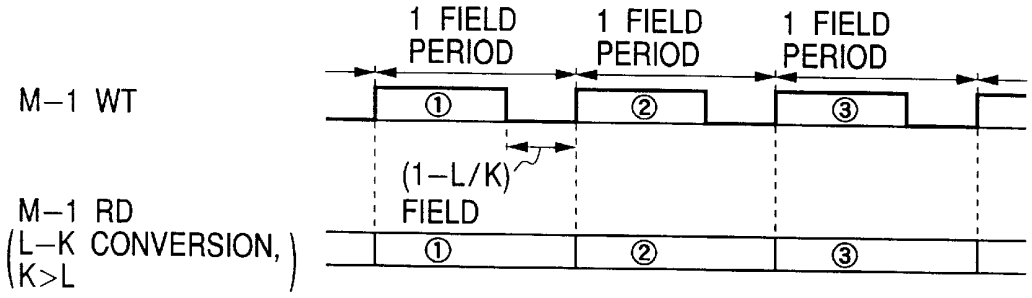


FIG. 6C

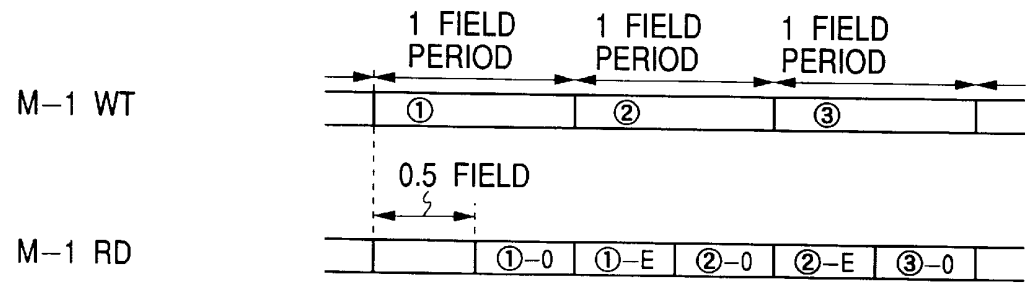


FIG. 6D

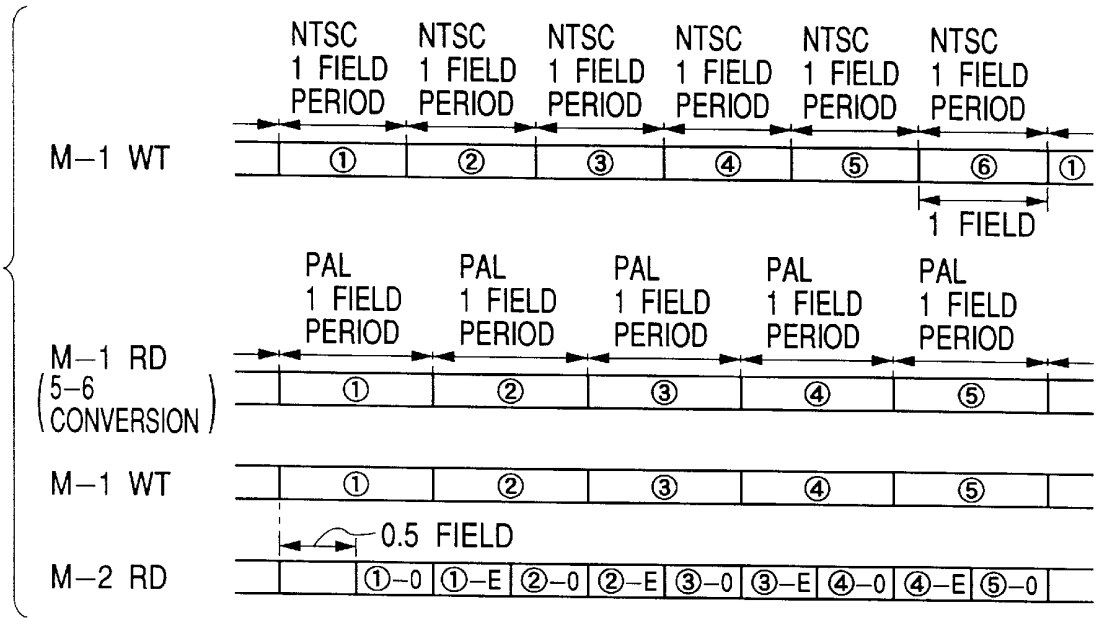

[NTSC–PAL 100Hz]
NTSC 1 FIELD PERIOD
M–1 WT
1 FIELD
PAL 1 FIELD PERIOD
M–1 RD (5–6 CONVERSION)
M–1 WT
0.5 FIELD
M–2 RD

FIG. 6E

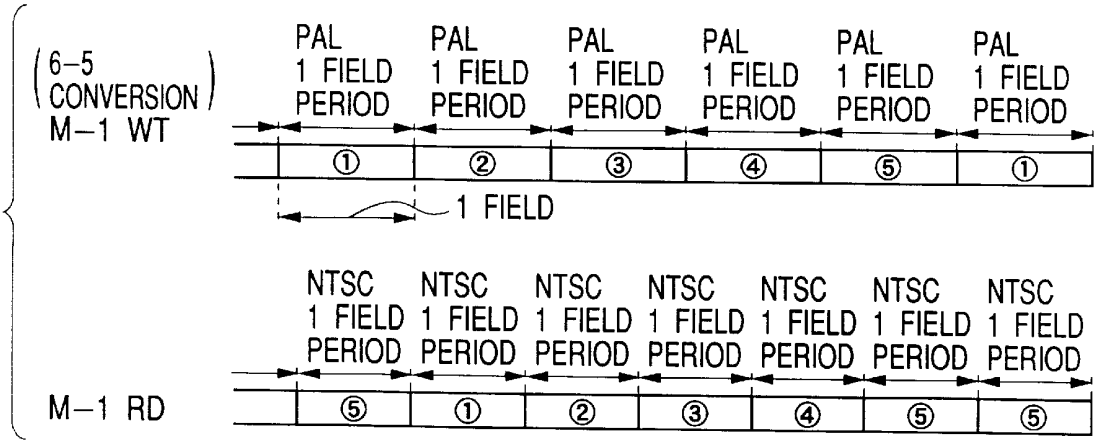

[PAL–NTSC CONVERSION]
(6–5 CONVERSION) M–1 WT
PAL 1 FIELD PERIOD
1 FIELD
NTSC 1 FIELD PERIOD
M–1 RD

FIG. 7

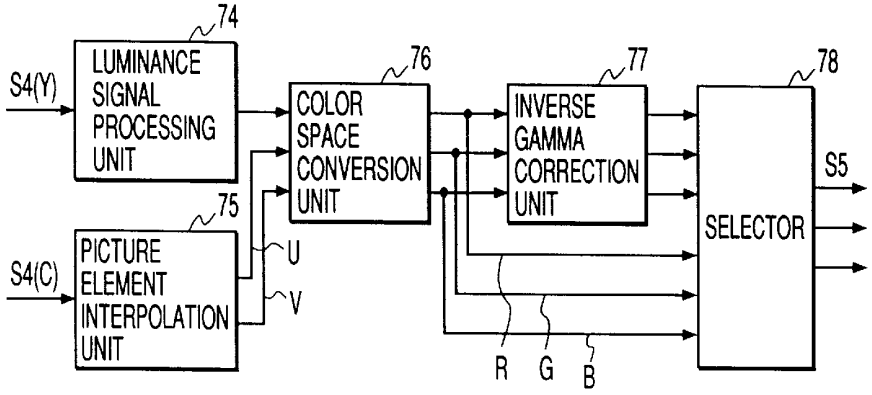

74
LUMINANCE SIGNAL PROCESSING UNIT
S4(Y)
76
COLOR SPACE CONVERSION UNIT
77
INVERSE GAMMA CORRECTION UNIT
78
SELECTOR
S5
75
PICTURE ELEMENT INTERPOLATION UNIT
S4(C)
U
V
R
G
B

FIG. 8

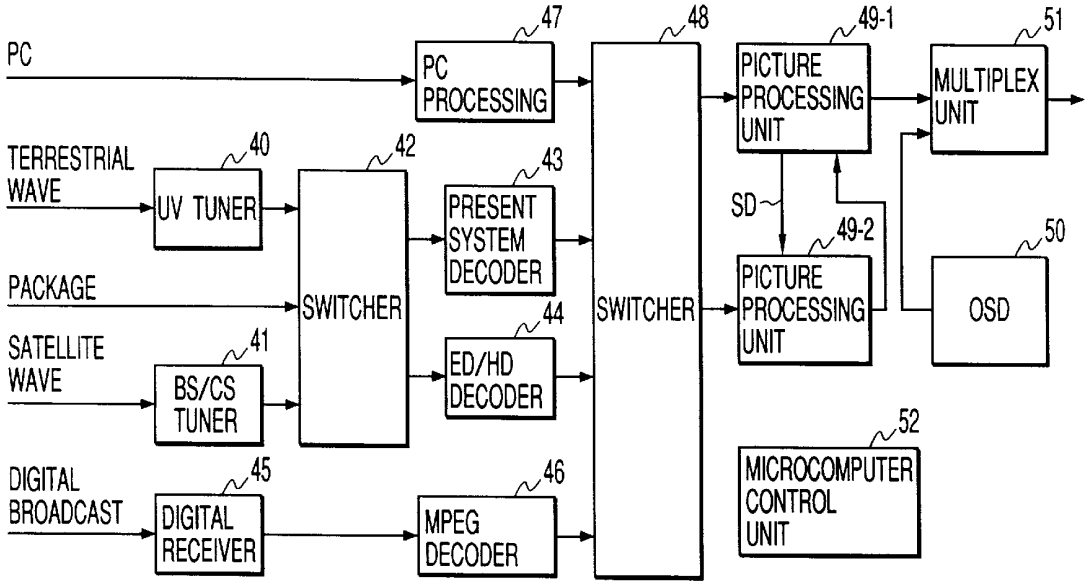

PC
47
PC PROCESSING
48
49-1
PICTURE PROCESSING UNIT
51
MULTIPLEX UNIT
TERRESTRIAL WAVE
40
UV TUNER
42
43
PRESENT SYSTEM DECODER
SD
49-2
50
PACKAGE
SWITCHER
SWITCHER
PICTURE PROCESSING UNIT
OSD
SATELLITE WAVE
41
BS/CS TUNER
44
ED/HD DECODER
52
MICROCOMPUTER CONTROL UNIT
DIGITAL BROADCAST
45
DIGITAL RECEIVER
46
MPEG DECODER

FIG. 9

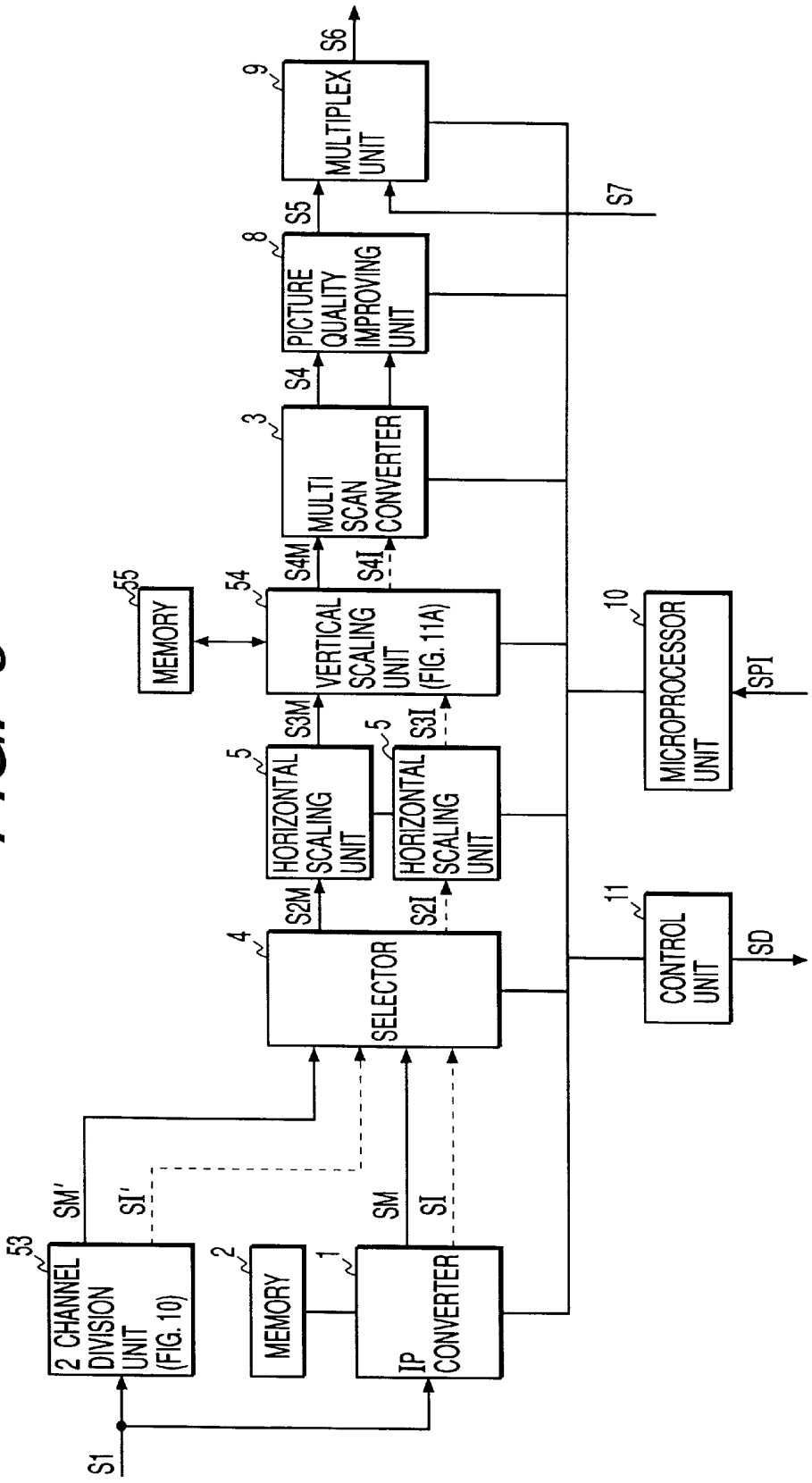

S1
2 CHANNEL DIVISION UNIT (FIG. 10)
53
MEMORY
2
IP CONVERTER
1
SM'
SI'
SM
SI
SELECTOR
4
S2M
S2I
HORIZONTAL SCALING UNIT
5
HORIZONTAL SCALING UNIT
5
S3M
S3I
MEMORY
55
VERTICAL SCALING UNIT (FIG. 11A)
54
S4M
S4I
MULTI SCAN CONVERTER
3
PICTURE QUALITY IMPROVING UNIT
8
S4
S5
MULTIPLEX UNIT
9
S6
S7
MICROPROCESSOR UNIT
10
SPI
CONTROL UNIT
11
SD

FIG. 10A

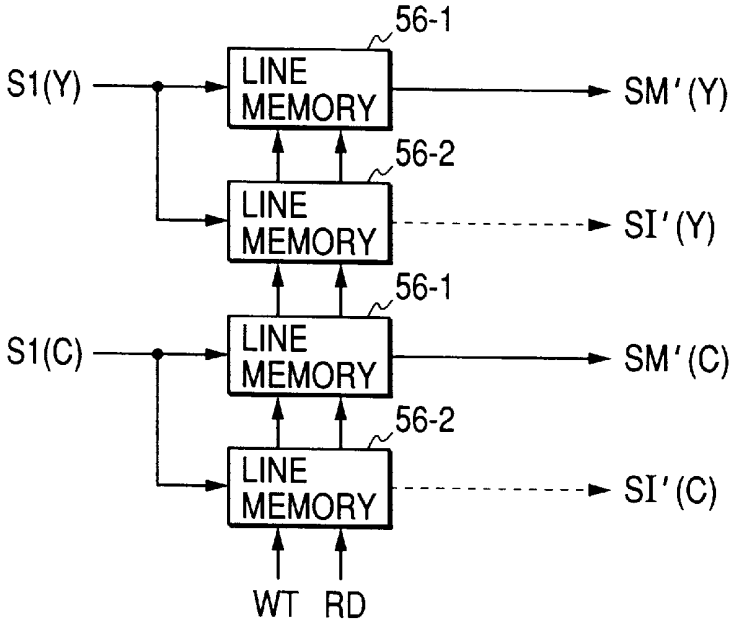


FIG. 10B

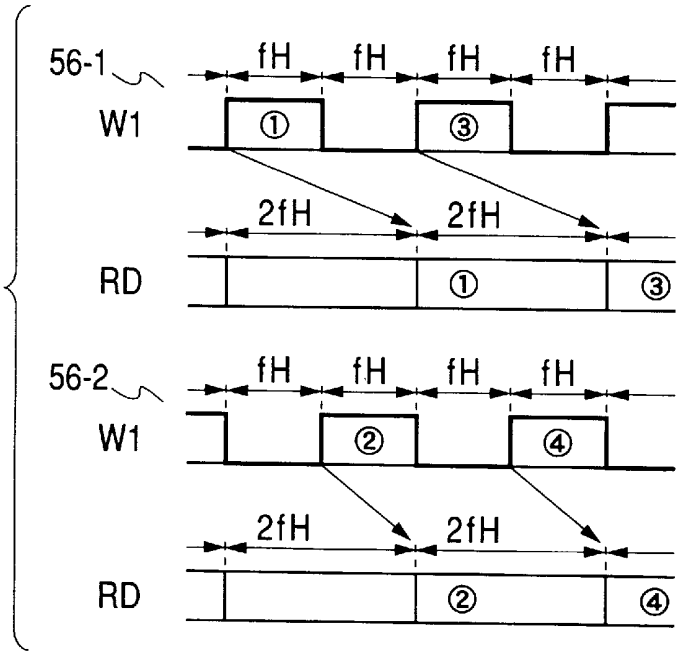


FIG. 11A

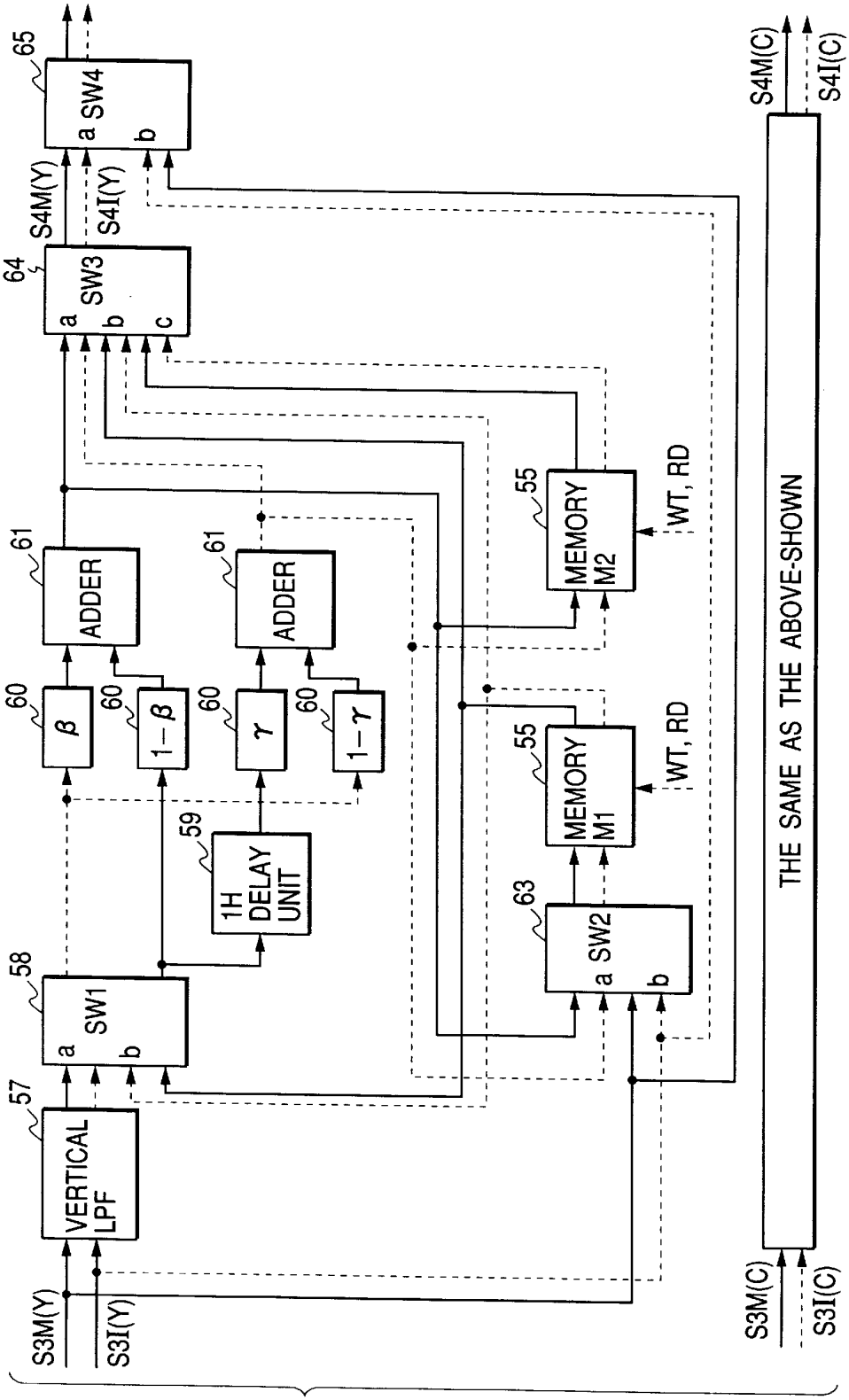

65
SW4
a
b
S4M(Y)
S4I(Y)
64
SW3
a
b
c
61
ADDER
61
ADDER
60
β
60
1−β
60
γ
60
1−γ
59
1H DELAY UNIT
58
SW1
a
b
57
VERTICAL LPF
S3M(Y)
S3I(Y)
55
MEMORY M2
WT, RD
55
MEMORY M1
WT, RD
63
SW2
a
b
S4M(C)
S4I(C)
THE SAME AS THE ABOVE-SHOWN
S3M(C)
S3I(C)

FIG. 11B

[SWITCH CONTROL]

SIGNAL PROCESSING	SW1	SW2	SW3	SW4
VERTICAL COMPRESSION	a	a	b	a
VERTICAL EXPANSION	b	b	a	a
PAL 100Hz	–	b	b	a
NTSC-PAL 100Hz	b	b	c	a
PAL-NTSC CONVERSION	a	a	b	a
THROUGH	–	–	–	b

FIG. 12A

[VERTICAL COMPRESSION]

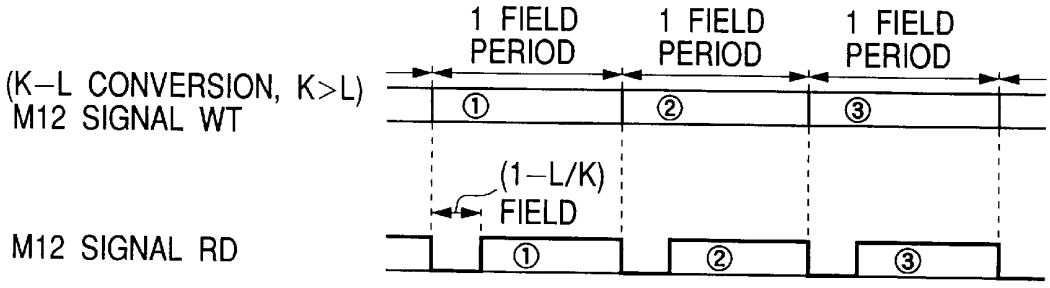


FIG. 12B

[VERTICAL EXPANSION]

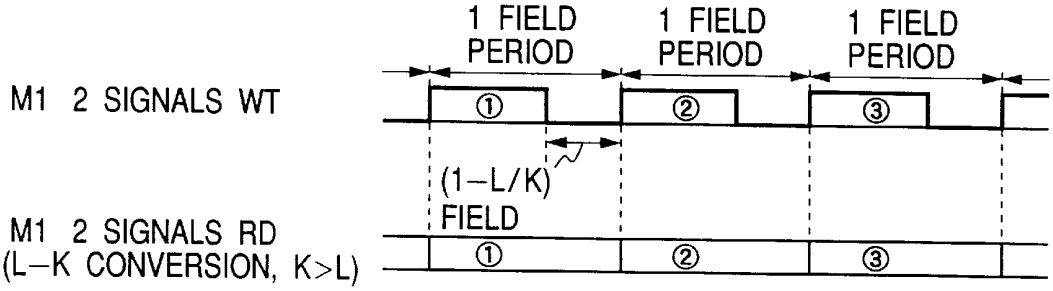


FIG. 12C

[PAL 100Hz]

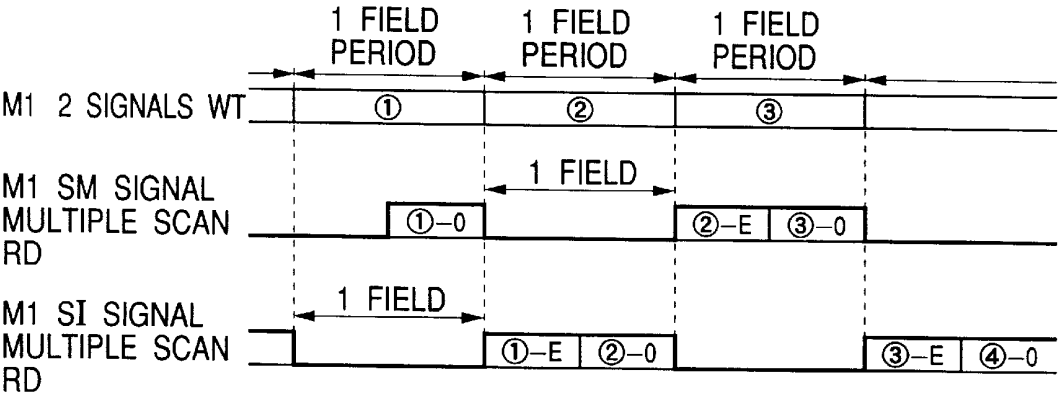


FIG. 12D

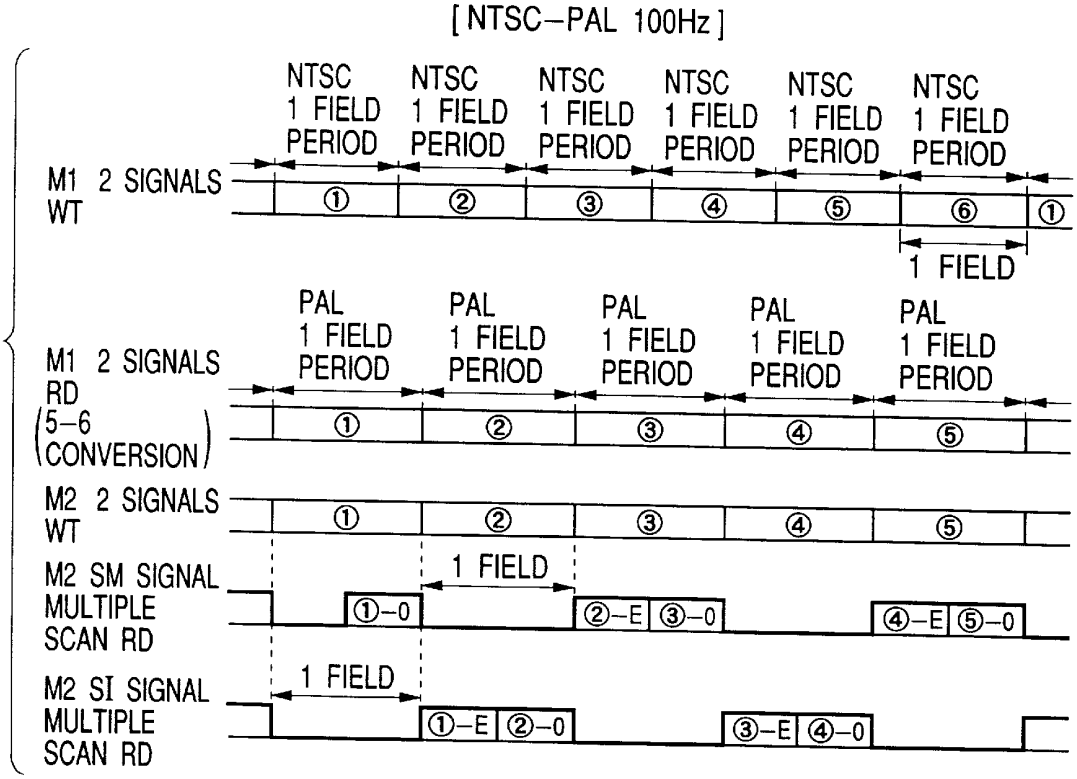


FIG. 12E

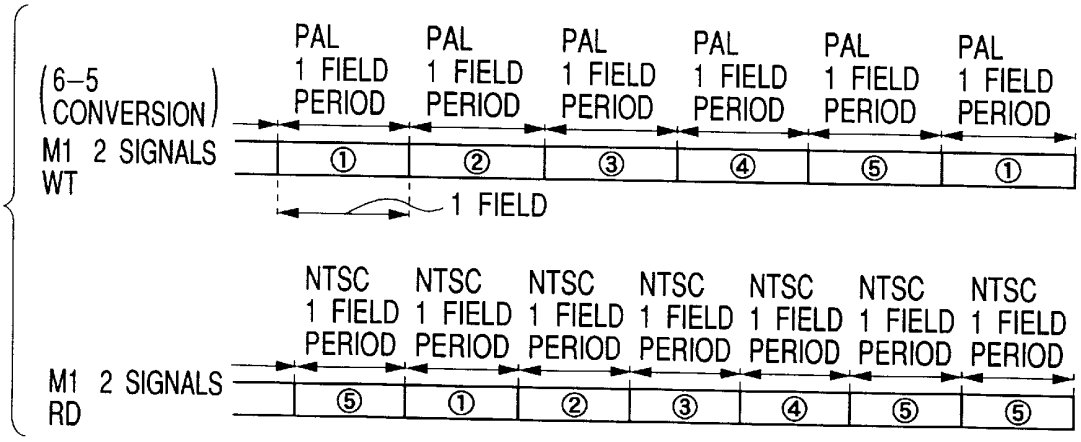


FIG. 13

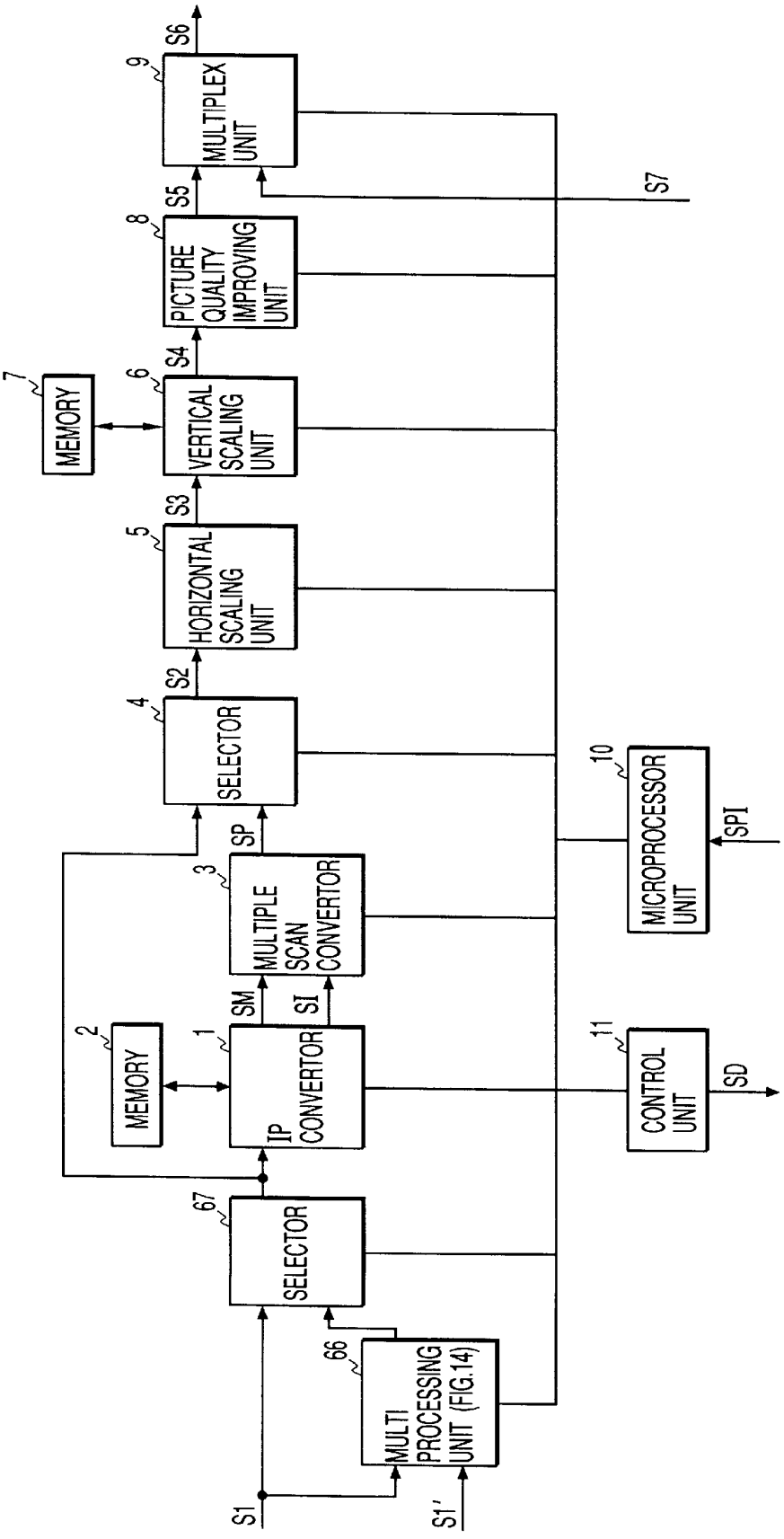

S6
9
MULTIPLEX UNIT
S7
S5
8
PICTURE QUALITY IMPROVING UNIT
S4
7
MEMORY
6
VERTICAL SCALING UNIT
S3
5
HORIZONTAL SCALING UNIT
S2
4
SELECTOR
10
MICROPROCESSOR UNIT
SPI
SP
3
MULTIPLE SCAN CONVERTOR
SM
SI
2
MEMORY
1
IP CONVERTOR
11
CONTROL UNIT
SD
67
SELECTOR
66
MULTI PROCESSING UNIT (FIG.14)
S1
S1'

FIG. 14

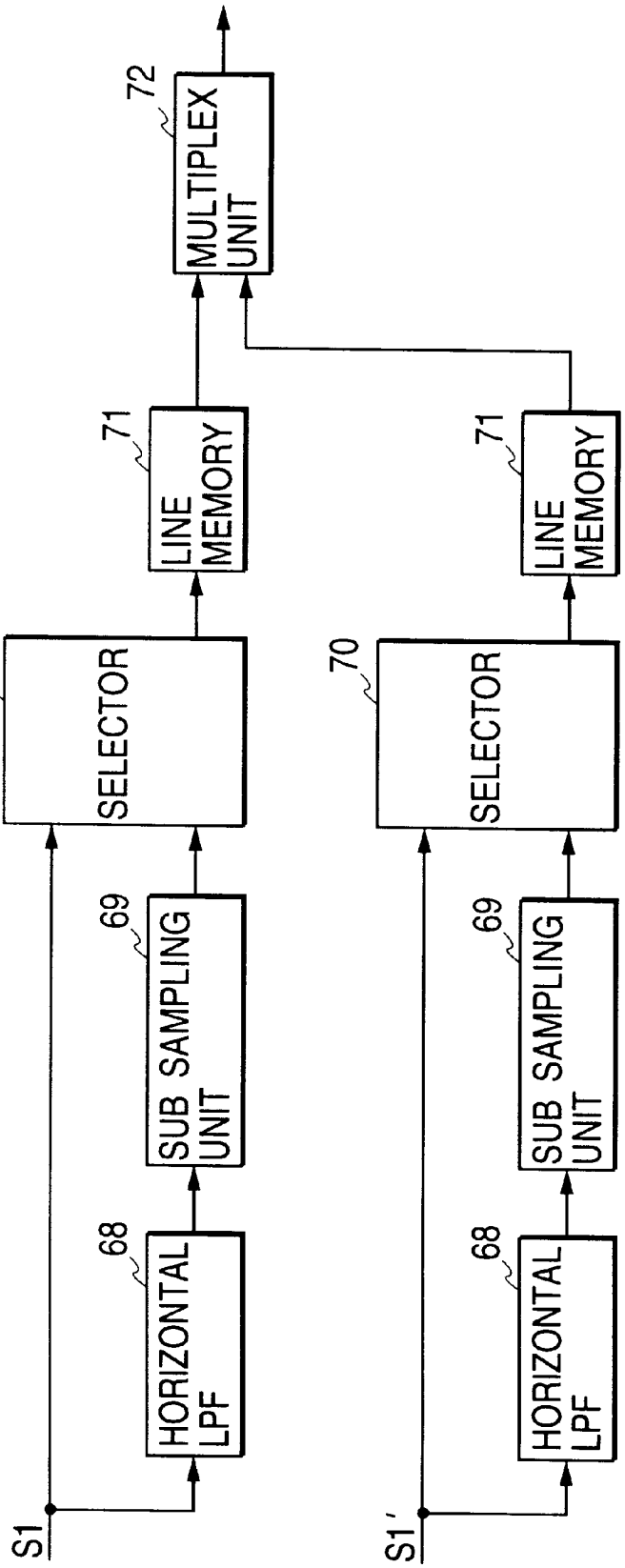

72
MULTIPLEX UNIT
71
LINE MEMORY
71
LINE MEMORY
70
SELECTOR
70
SELECTOR
69
SUB SAMPLING UNIT
69
SUB SAMPLING UNIT
68
HORIZONTAL LPF
68
HORIZONTAL LPF
S1
S1'

FIG. 15A

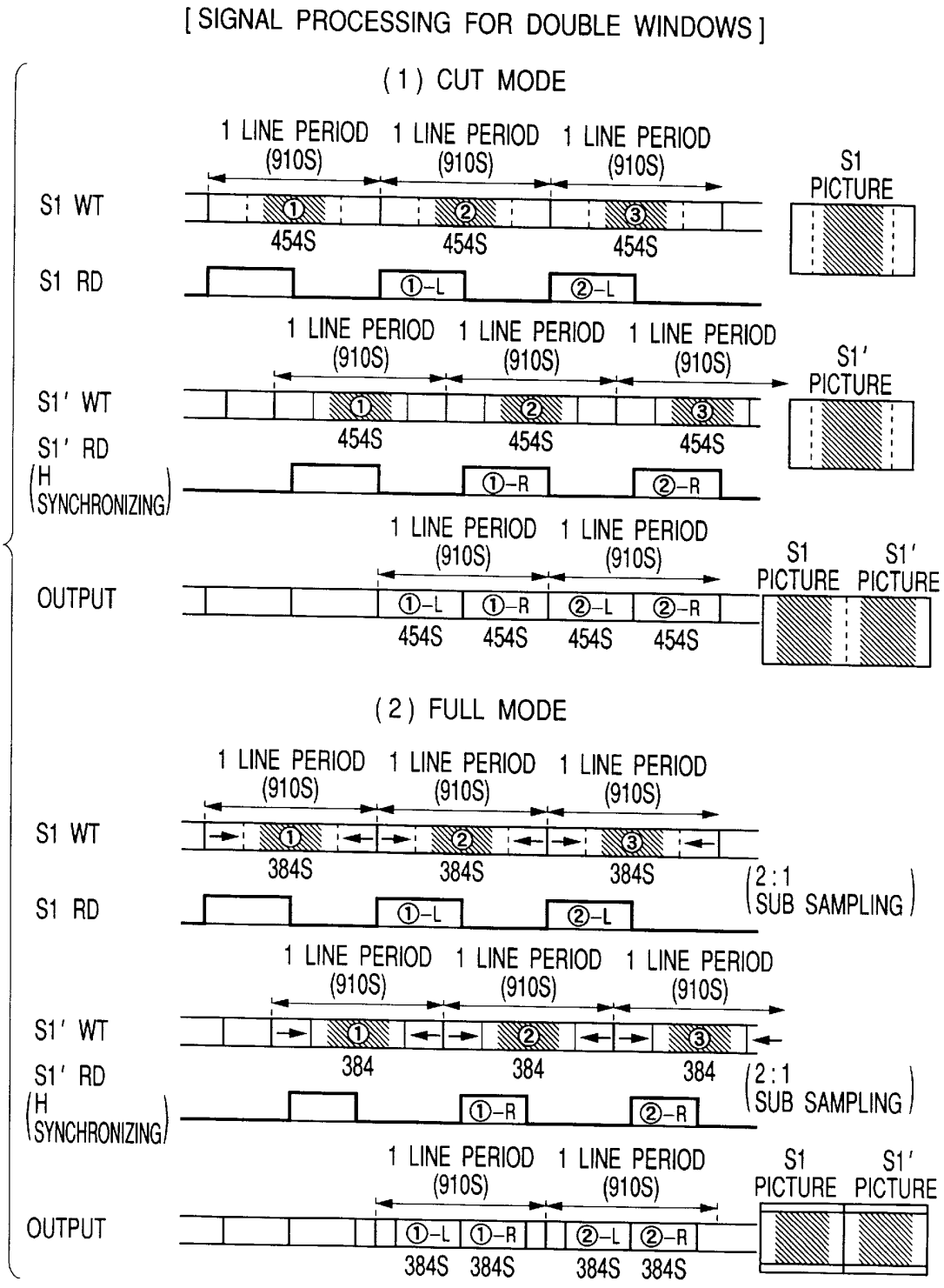

[SIGNAL PROCESSING FOR DOUBLE WINDOWS]
(1) CUT MODE
1 LINE PERIOD (910S)
1 LINE PERIOD (910S)
1 LINE PERIOD (910S)
S1 WT
S1 PICTURE
454S
S1 RD
①-L
②-L
S1' WT
S1' PICTURE
S1' RD
(H SYNCHRONIZING)
①-R
②-R
OUTPUT
S1 PICTURE
S1' PICTURE
(2) FULL MODE
384S
384
(2:1 SUB SAMPLING)

FIG. 15B

[SIGNAL PROCESSING FOR PIP WINDOWS]

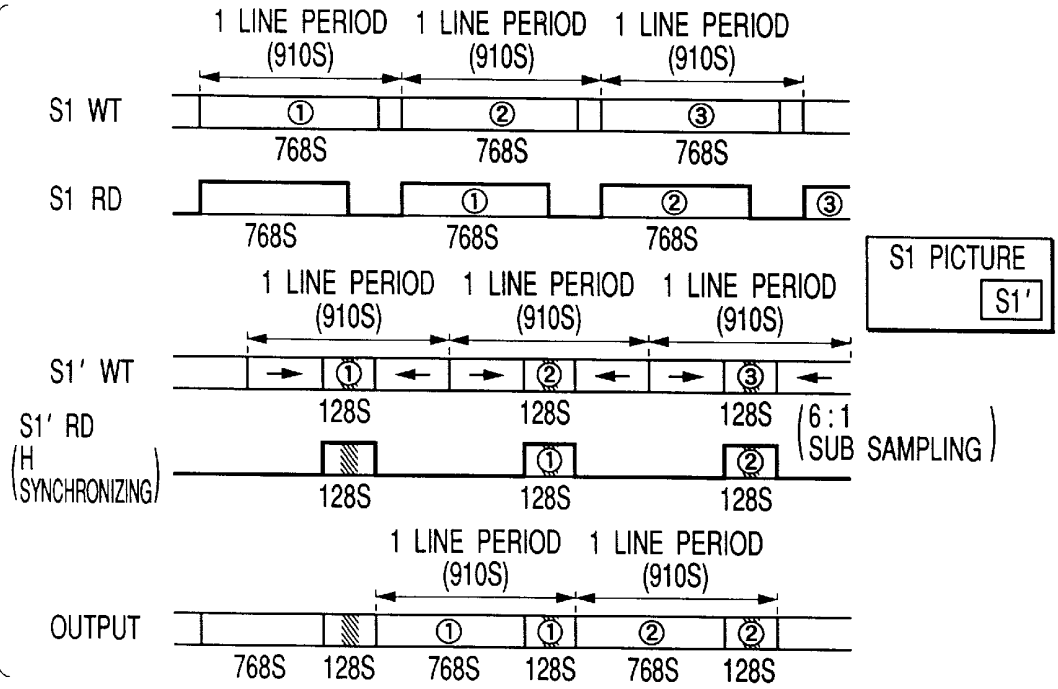


FIG. 16A

[SIGNAL PROCESSING]

DOUBLE WINDOWS MODE	HORIZONTAL SCALING	VERTICAL SCALING
CUT MODE	4–3 COMPRESSION CONVERSION	VERTICAL SYNCHRONIZING
FULL MODE	THROUGH	3–2 COMPRESSION CONVERSION VERTICAL SYNCHRONIZING

PIP WINDOWS MODE	HORIZONTAL SCALING	VERTICAL SCALING
MAIN PICTURE (S1)	4–3 COMPRESSION CONVERSION	THROUGH
SUB PICTURE (S1')	1–2 EXPANSION CONVERSION	9–4 COMPRESSION CONVERSION VERTICAL SYNCHRONIZING

FIG. 16B

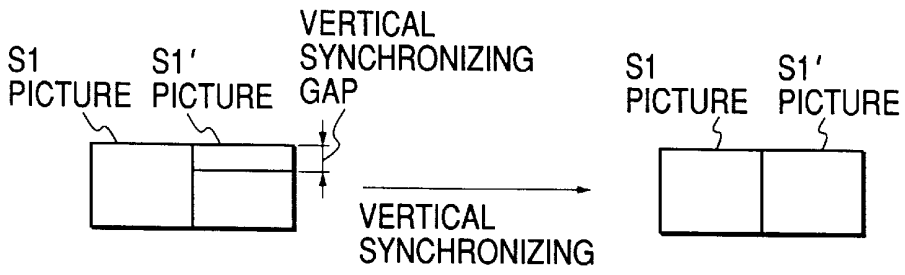


FIG. 16C

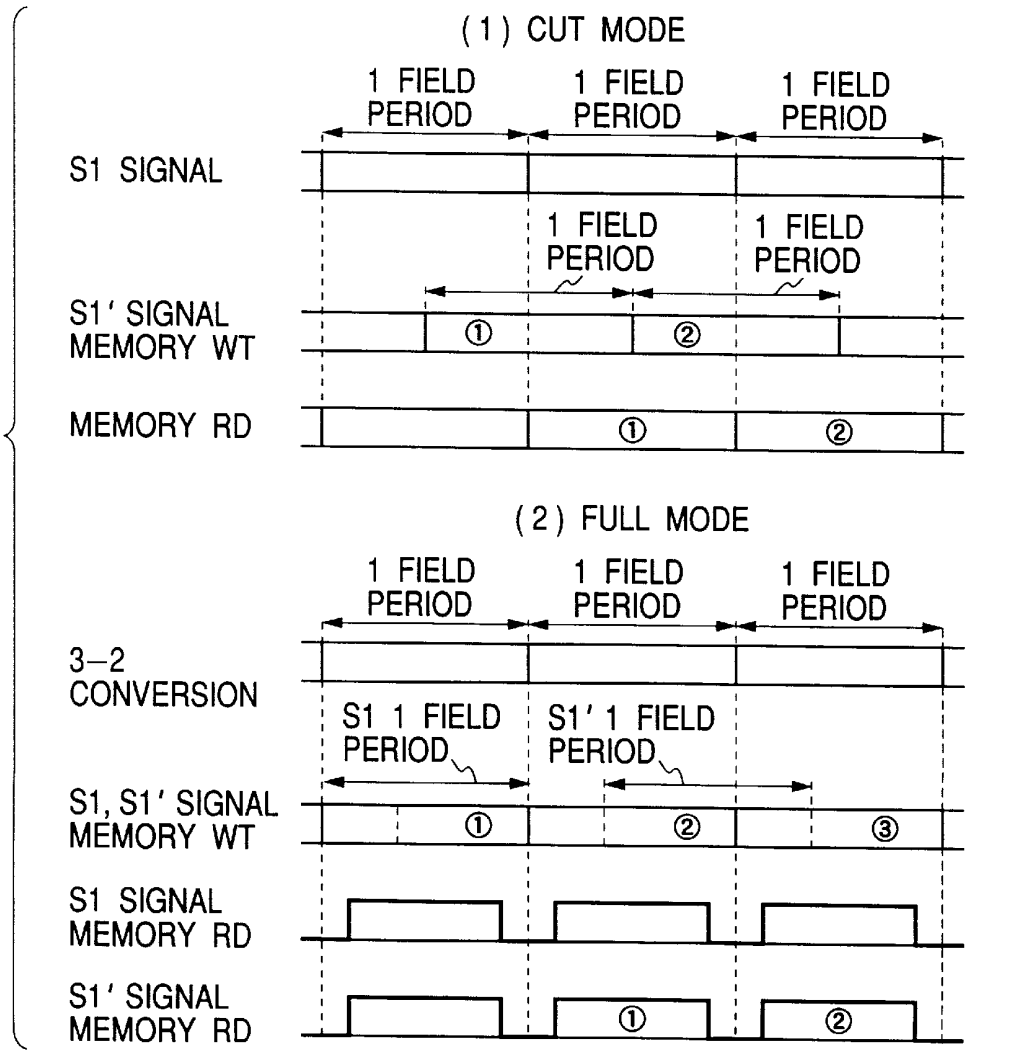


FIG. 17

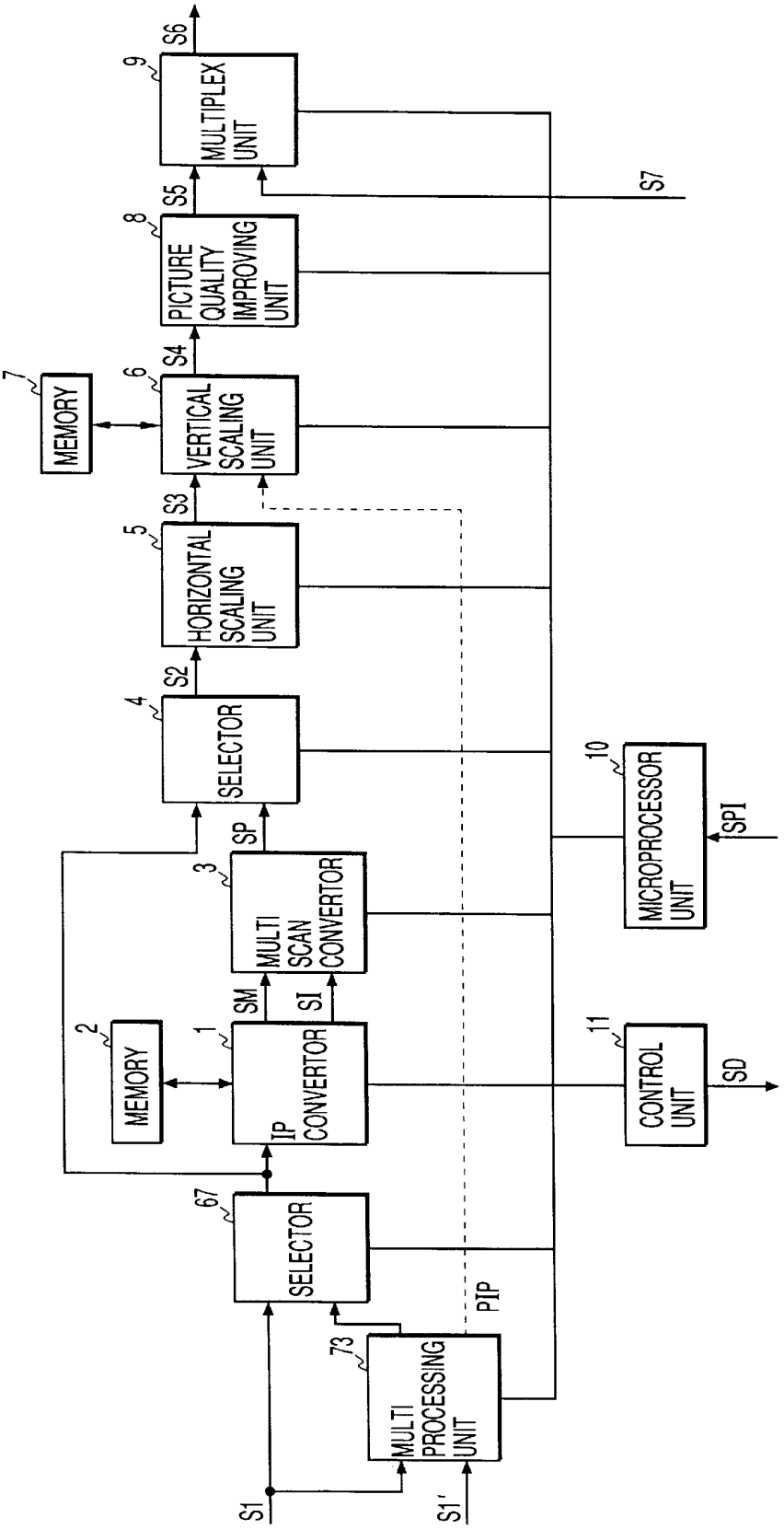

S6
9
MULTIPLEX UNIT
S5
8
PICTURE QUALITY IMPROVING UNIT
S4
6
VERTICAL SCALING UNIT
7
MEMORY
S3
5
HORIZONTAL SCALING UNIT
S2
4
SELECTOR
SP
3
MULTI SCAN CONVERTOR
SM
SI
2
MEMORY
1
IP CONVERTOR
67
SELECTOR
73
MULTI PROCESSING UNIT
S1
S1'
PIP
S7
10
MICROPROCESSOR UNIT
SPI
11
CONTROL UNIT
SD

FIG. 18

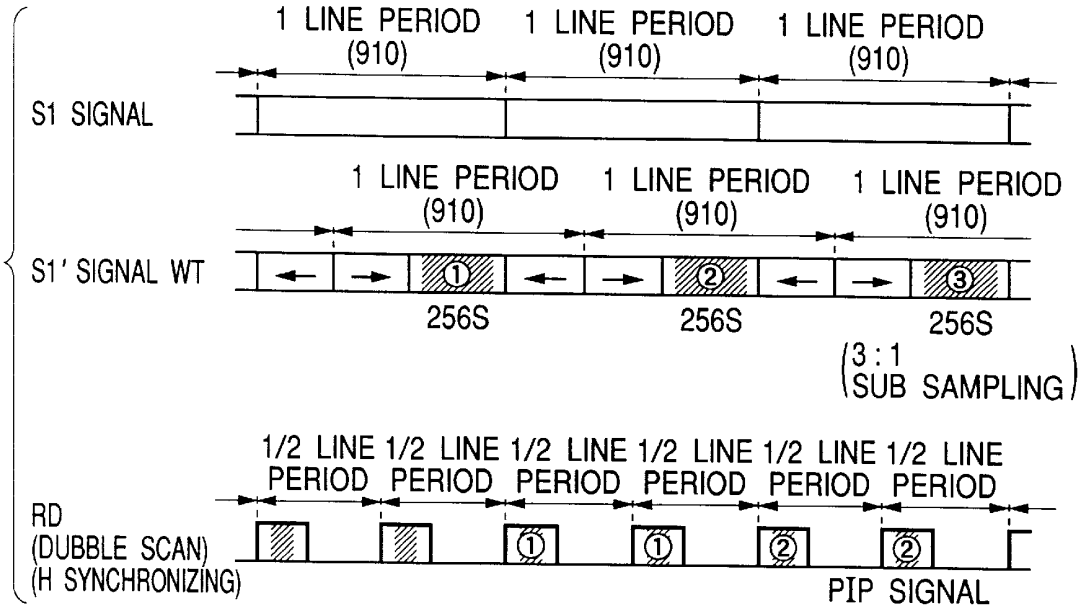


FIG. 19A

[HORIZONTAL COMPRESSION (NORMAL MODE)]

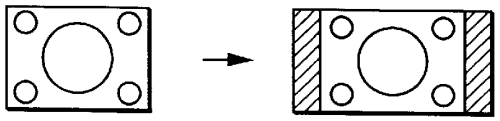


FIG. 19B

[HORIZONTAL EXPANSION (CINEMA MODE)]

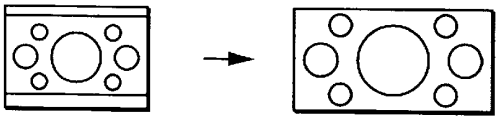


FIG. 19C

[SMOOTH WIDE]

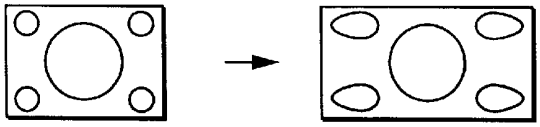


FIG. 19D

[SQUEEZE (FULL MODE)]

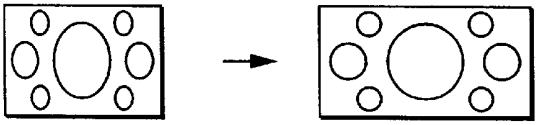


FIG. 19E

[HORIZONTAL AND VERTICAL FLEXIBLE COMPRESSION]

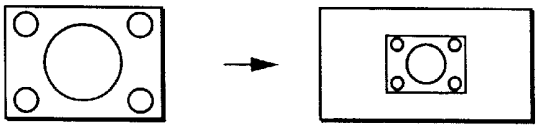


FIG. 19F

[HORIZONTAL AND VERTICAL FLEXIBLE EXPANSION]

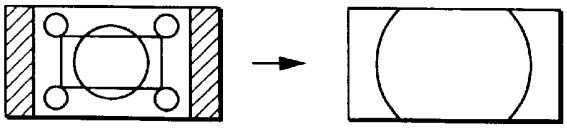


FIG. 20A

[4–3 CONVERSION]

$$\begin{vmatrix} Y1 \\ Y2 \\ Y3 \end{vmatrix} = \begin{vmatrix} 1 & 0 & 0 & 0 \\ 0 & 2/3 & 1/3 & 0 \\ 0 & 0 & 1/3 & 2/3 \end{vmatrix} \begin{vmatrix} X1 \\ X2 \\ X3 \\ X4 \end{vmatrix}$$

FIG. 20B

[3–4 CONVERSION]

$$\begin{vmatrix} Y1 \\ Y2 \\ Y3 \\ Y4 \end{vmatrix} = \begin{vmatrix} 1 & 0 & 0 & 0 \\ 1/4 & 3/4 & 0 & 0 \\ 0 & 2/4 & 2/4 & 0 \\ 0 & 0 & 3/4 & 1/4 \end{vmatrix} \begin{vmatrix} X1 \\ X2 \\ X3 \\ X4 \end{vmatrix}$$

X4 IS THE SAME AS NEXT X1

FIG. 20C

[6–5 CONVERSION]

$$\begin{vmatrix} Y1 \\ Y2 \\ Y3 \\ Y4 \\ Y5 \end{vmatrix} = \begin{vmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 4/5 & 1/5 & 0 & 0 & 0 \\ 0 & 0 & 3/5 & 2/5 & 0 & 0 \\ 0 & 0 & 0 & 2/5 & 3/5 & 0 \\ 0 & 0 & 0 & 0 & 1/5 & 4/5 \end{vmatrix} \begin{vmatrix} X1 \\ X2 \\ X3 \\ X4 \\ X5 \\ X6 \end{vmatrix}$$

FIG. 20D

[5–6 CONVERSION]

$$\begin{vmatrix} Y1 \\ Y2 \\ Y3 \\ Y4 \\ Y5 \\ Y6 \end{vmatrix} = \begin{vmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 1/6 & 5/6 & 0 & 0 & 0 & 0 \\ 0 & 2/6 & 4/6 & 0 & 0 & 0 \\ 0 & 0 & 3/6 & 3/6 & 0 & 0 \\ 0 & 0 & 0 & 4/6 & 2/6 & 0 \\ 0 & 0 & 0 & 0 & 5/6 & 1/6 \end{vmatrix} \begin{vmatrix} X1 \\ X2 \\ X3 \\ X4 \\ X5 \\ X6 \end{vmatrix}$$

X6 IS THE SAME AS NEXT X1

FIG. 21

INPUT SIGNAL		IP CONVERSION	HORIZONTAL SCALING	VERTICAL SCALING	REMARKS
525/60/2 : 1 SYSTEM (NTSC)		○	4–3 CONVERSION	THROUGH	NORMAL MODE
		○	4–3 CONVERSION *	THROUGH	ZOOM WIDE MODE
		○	THROUGH	3–4 CONVERSION	CINEMA MODE
		○	1–N CONVERSION	1–N CONVERSION	N TIMES ZOOM MODE
		○	N–1 CONVERSION	N–1 CONVERSION	1/N COMPRESSION
525/60/1 : 1 SYSTEM (EDTV)		THROUGH	THROUGH	THROUGH	
		THROUGH	1–N CONVERSION	1–N CONVERSION	N TIMES ZOOM MODE
		THROUGH	N–1 CONVERSION	N–1 CONVERSION	1/N COMPRESSION
1125/60/2 : 1 SYSTEM (HDTV)		THROUGH	SUB-SAMPLING ↓	17–16 CONVERSION	
		THROUGH	1–N CONVERSION	1–N CONVERSION	N TIMES ZOOM MODE
		THROUGH	N–1 CONVERSION	N–1 CONVERSION	1/N COMPRESSION
625/50/2 : 1 SYSTEM (PAL)		○	4–3 CONVERSION	6–5 CONVERSION **	NORMAL MODE
		○	4–3 CONVERSION *	6–5 CONVERSION **	ZOOM WIDE MODE
		○	THROUGH	9–10 CONVERSION **	CINEMA MODE
		○	1–N CONVERSION	1–N CONVERSION **	N TIMES ZOOM MODE
		○	N–1 CONVERSION	N–1 CONVERSION **	1/N COMPRESSION
PC	VGA SYSTEM (640×480)	THROUGH	4–3 CONVERSION	THROUGH	NORMAL MODE
		THROUGH	1–N CONVERSION	1–N CONVERSION	N TIMES ZOOM MODE
		THROUGH	N–1 CONVERSION	N–1 CONVERSION	1/N COMPRESSION
	SVGA SYSTEM (800×600)	THROUGH	4–3 CONVERSION	5–4 CONVERSION	NORMAL MODE
		THROUGH	1–N CONVERSION	1–N CONVERSION	N TIMES ZOOM MODE
		THROUGH	N–1 CONVERSION	N–1 CONVERSION	1/N COMPRESSION
	XGA SYSTEM (1024×768)	THROUGH	4–3 CONVERSION	8–5 CONVERSION	NORMAL MODE
		THROUGH	1–N CONVERSION	1–N CONVERSION	N TIMES ZOOM MODE
		THROUGH	N–1 CONVERSION	N–1 CONVERSION	1/N COMPRESSION

* 1–1 CONVERSION AT RIGHT & LEFT CORNER AREA

** INCLUDING FRAME RATE CONVERSION PROCESSING

FIG. 22

INPUT SIGNAL		IP CONVERSION	HORIZONTAL SCALING	VERTICAL SCALING	REMARKS
525/60/2 : 1 SYSTEM (NTSC)		○	4–3 CONVERSION	5–6 CONVERSION **	NORMAL MODE
		○	4–3 CONVERSION *	5–6 CONVERSION **	ZOOM WIDE MODE
		○	THROUGH	5–8 CONVERSION **	CINEMA MODE
		○	1–N CONVERSION	1–N CONVERSION **	N TIMES ZOOM MODE
		○	N–1 CONVERSION	N–1 CONVERSION **	1/N COMPRESSION
525/60/1 : 1 SYSTEM (EDTV)		THROUGH	THROUGH	5–6 CONVERSION **	
		THROUGH	1–N CONVERSION	1–N CONVERSION **	N TIMES ZOOM MODE
		THROUGH	N–1 CONVERSION	N–1 CONVERSION **	1/N COMPRESSION
1125/60/2 : 1 SYSTEM (HDTV)		THROUGH	SUB-SAMPLING ↓	15–16 CONVERSION **	
		THROUGH	1–N CONVERSION	1–N CONVERSION **	N TIMES ZOOM MODE
		THROUGH	N–1 CONVERSION	N–1 CONVERSION **	1/N COMPRESSION
625/50/2 : 1 SYSTEM (PAL)		○	4–3 CONVERSION	THROUTH #	NORMAL MODE
		○	4–3 CONVERSION *	THROUTH #	ZOOM WIDE MODE
		○	THROUGH	3–4 CONVERSION #	CINEMA MODE
		○	1–N CONVERSION	1–N CONVERSION #	N TIMES ZOOM MODE
		○	N–1 CONVERSION	N–1 CONVERSION #	1/N COMPRESSION
PC	VGA SYSTEM (640×480)	THROUGH	4–3 CONVERSION	5–6 CONVERSION **	NORMAL MODE
		THROUGH	1–N CONVERSION	1–N CONVERSION **	N TIMES ZOOM MODE
		THROUGH	N–1 CONVERSION	N–1 CONVERSION **	1/N COMPRESSION
	SVGA SYSTEM (800×600)	THROUGH	4–3 CONVERSION	THROUGH **	NORMAL MODE
		THROUGH	1–N CONVERSION	1–N CONVERSION **	N TIMES ZOOM MODE
		THROUGH	N–1 CONVERSION	N–1 CONVERSION **	1/N COMPRESSION
	XGA SYSTEM (1024×768)	THROUGH	4–3 CONVERSION	4–3 CONVERSION **	NORMAL MODE
		THROUGH	1–N CONVERSION	1–N CONVERSION **	N TIMES ZOOM MODE
		THROUGH	N–1 CONVERSION	N–1 CONVERSION **	1/N COMPRESSION

* 1–1 CONVERSION AT RIGHT & LEFT CORNER AREA

** INCLUDING FRAME RATE CONVERSION & FIELD MULTIPLE SCAN PROCESSING

\# INCLUDING FIELD MULTIPLE SCAN PROCESSING

FIG. 23

INPUT SIGNAL		IP CONVERSION	HORIZONTAL SCALING	VERTICAL SCALING	REMARKS
525/60/2 : 1 SYSTEM (NTSC)		○	4–3 CONVERSION	16–17 CONVERSION #	NORMAL MODE
		○	4–3 CONVERSION *	16–17 CONVERSION #	ZOOM WIDE MODE
		○	THROUGH	12–17 CONVERSION #	CINEMA MODE
		○	1–N CONVERSION	1–N CONVERSION #	N TIMES ZOOM MODE
		○	N–1 CONVERSION	N–1 CONVERSION #	1/N COMPRESSION
525/60/1 : 1 SYSTEM (EDTV)		THROUGH	THROUGH	16–17 CONVERSION #	
		THROUGH	1–N CONVERSION	1–N CONVERSION #	N TIMES ZOOM MODE
		THROUGH	N–1 CONVERSION	N–1 CONVERSION #	1/N COMPRESSION
1125/60/2 : 1 SYSTEM (HDTV)		THROUGH	THROUGH	THROUGH	
		THROUGH	1–N CONVERSION	1–N CONVERSION	N TIMES ZOOM MODE
		THROUGH	N–1 CONVERSION	N–1 CONVERSION	1/N COMPRESSION
625/50/2 : 1 SYSTEM (PAL)		○	4–3 CONVERSION	16–15 CONVERSION ##	NORMAL MODE
		○	4–3 CONVERSION *	16–15 CONVERSION ##	ZOOM WIDE MODE
		○	THROUGH	4–5 CONVERSION ##	CINEMA MODE
		○	1–N CONVERSION	1–N CONVERSION ##	N TIMES ZOOM MODE
		○	N–1 CONVERSION	N–1 CONVERSION ##	1/N COMPRESSION
PC	VGA SYSTEM (640×480)	THROUGH	4–3 CONVERSION	16–17 CONVERSION #	NORMAL MODE
		THROUGH	1–N CONVERSION	1–N CONVERSION #	N TIMES ZOOM MODE
		THROUGH	N–1 CONVERSION	N–1 CONVERSION #	1/N COMPRESSION
	SVGA SYSTEM (800×600)	THROUGH	4–3 CONVERSION	20–17 CONVERSION #	NORMAL MODE
		THROUGH	1–N CONVERSION	1–N CONVERSION #	N TIMES ZOOM MODE
		THROUGH	N–1 CONVERSION	N–1 CONVERSION #	1/N COMPRESSION
	XGA SYSTEM (1024×768)	THROUGH	4–3 CONVERSION	32–21 CONVERSION #	NORMAL MODE
		THROUGH	1–N CONVERSION	1–N CONVERSION #	N TIMES ZOOM MODE
		THROUGH	N–1 CONVERSION	N–1 CONVERSION #	1/N COMPRESSION

* 1–1 CONVERSION AT RIGHT & LEFT CORNER AREA

\# INCLUDING INTERLACE CONVERSION PROCESSING

INCLUDING FRAME RATE CONVERSION & INTERLACE CONVERSION PROCESSING

METHOD AND CIRCUIT FOR SIGNAL PROCESSING OF FORMAT CONVERSION OF PICTURE SIGNAL

BACKGROUND OF THE INVENTION

The present invention relates to signal processing of format conversion of picture signal, particularly to a method and a circuit for signal processing of format conversion of picture signal preferable to converting a plurality of kinds of formats of picture signals into picture signals of predetermined display formats of picture output devices or conversion of flexible compression and flexible expansion of pictures in a horizontal and a vertical direction, or the like.

In recent years, with progress in multimedia, in respect of picture signals, kinds and modes of pictures to be handled increase rapidly and are advancing in a direction of diversification. Further, in respect of picture output devices for displaying pictures, other than CRT (Cathode Ray Tube), planar displays such as a liquid crystal display device, a plasma display panel and the like have frequently been used. Therefore, it is indispensable for information terminal devices in correspondence with multimedia to be provided with a function of receiving many kinds and many modes of picture sources and displaying them.

As representative methods for realizing the function, there are known a method of dealing with by display and a method of dealing with by signal processing. According to the former method, a picture is displayed by widely setting an operational range of a deflection system of a picture output device and performing a scanning operation in a mode in compliance with a signal format of input pictures, which has been reduced into practice as multi scan system. Although this is an effective method which can be realized at a comparatively low cost when a display unit is a CRT, it is difficult to apply in a planar display such as a liquid crystal display device, a plasma display panel or the like having a constant number of display picture elements.

According to the latter method, format conversion is performed by signal processing and pictures are displayed by converting inputted signals of pictures into signals of display formats of picture output devices, which can be applied to all the picture output devices such as a CRT, a liquid crystal display device, a plasma display panel and the like. Therefore, this is a method that is extremely effective in dealing with diversification of input picture sources or picture output devices predicted in the future. According to the method, various signal processing such as conversion of frame rate, compression and expansion of picture size and the like must be performed for format conversion.

For example, when a television signal of PAL system is converted into a television signal of NTSC system and displayed by a CRT or a liquid crystal display device, signal processing such as conversion of frame rate, conversion of number of scanning lines, conversion from interlace scanning into progressive scanning, conversion of aspect ratio or the like, compression and expansion, synchronizing and the like are performed independently each other. Further, memories having a comparatively large capacity such as a line memory, a frame memory are used in many of these signal processing operations. Accordingly, conventionally, a number of memories are needed in a total of signal processing and device cost is increased by using many memories. Further, a variety of input and output interfaces are needed between signal processing and therefore, processing for matching interfaces are often needed, which amounts to an increase in device cost.

Further, in each of signal processing, picture quality is slightly deteriorated, which is caused by, for example, quantization error by AD/DA conversion, band restriction by subjecting signals to a filter or the like. Such a picture quality deterioration is accumulated at each signal processing and the picture quality deterioration cannot be disregarded.

SUMMARY OF THE INVENTION

It is a principal object of the present invention to provide a method and a circuit for signal processing of format conversion of picture signal where deterioration of picture quality accompanied by signal processing of format conversion is inconsiderable, used memory capacity is extremely small and a reduction in fabrication cost is facilitated.

It is other object of the present invention to achieve the above object as well as to provide a signal processing circuit capable of converting a plurality of kinds of systems of input picture signals into signals of predetermined display formats of picture output devices.

In order to achieve the above-described object, according to an aspect of the present invention, there is provided a circuit for signal processing of format conversion of picture signal, comprising a scanning convertor for converting an input picture signal into a picture signal of progressive scanning when the input picture signal is of interlace scanning, a selector for selecting either one of the input picture signal and the picture signal of progressive scanning outputted from the scanning convertor, a scaling unit for performing signal processing of scaling in horizontal and vertical directions in respect of an output signal from the selector for format conversion and a control unit for selecting parameters of signal processing in accordance with a format of the input picture signal and a display format of a picture output device and controlling at least the scanning convertor, the selector and the scaling unit in accordance with the parameters of the signal processing.

Such a constitution is realized by commonly using memories in some signal processing, unifying combinations among signal processing by a common digital interface and a common signal system (progressive scanning system) and adopting a centralized control by the control unit.

Deterioration in picture quality is significantly improved by combining respective signal processing by signals of progressive scanning system. That is, many filtering processing are performed for picture signals in signal processing. In respect of many filters needed in such a picture processing, when progressive scanning system is compared with interlace scanning system, the degree of freedom of design is larger in the progressive scanning system and the filters can be realized with substantially ideal characteristics having high spatial frequencies. Therefore, deterioration in picture quality accompanied by signal processing in format conversion is significantly improved.

The scaling unit is provided with a horizontal scaling unit performing signal processing of the horizontal scaling and a vertical scaling unit performing signal processing of the vertical scaling. When a number of inputted horizontal picture elements of the input picture signal is larger than a number of horizontal picture elements of a displayed picture, the horizontal scaling is performed preferably prior to the vertical scaling and in the converse case, the vertical scaling is preferably performed prior to the horizontal scaling. Further, in the vertical scaling, other than signal processing of compression and expansion, also at least one of signal processing of frame rate conversion for system conversion (for example, PAL-NTSC conversion) of TV

signals, signal processing for PAL 100 Hz, and signal processing of synchronization in multi windows such as double windows, a PIP (Picture In Picture; a small sub picture is displayed in a full main picture) display or the like, is performed. According to the constitution, compared with the case where signal processing of system conversion, compression, expansion, synchronization and the like are independently performed, a memory capacity necessary for signal processing of format conversion can significantly be reduced to one severalth of field (several mega bits).

Further, the circuit structure of each of horizontal scaling and vertical scaling is constituted by a combination of a calculation unit for multiplying a plurality of picture elements or picture elements of a plurality of lines by coefficient values, memories and a plurality of numbers of switches by which compression function, expansion function and through function are realized by switching signals by selectively controlling the switches. According to the calculation unit, linear interpolation process is performed. A plurality of kinds of processing can be performed by a same circuit through the technical means by which circuit scale necessary for signal processing can significantly be reduced.

According to a preferable embodiment of the present invention, the scanning convertor converts the input picture signal into a picture signal of progressive scanning by motion-adaptive process or motion compensative interpolation. Also, an output side of the scaling unit is provided with a picture quality improving unit for executing picture quality improving processing such as color space conversion or inverse gamma conversion to the picture signal which has been subjected to signal processing of format conversion.

As other preferable embodiment of the present invention, there is provided a multi processing unit for performing signal processing of multiplexing a first picture signal and a second picture signal of the same system (for example, NTSC television signals of interlace scanning) to a time-division multiplex signal during 1 scanning line period in which signal processing of format conversion is performed each for the first picture signal in one window and for picture signals outputted from the multi-processing unit in double windows. A further reduction in circuit scale necessary for signal processing can be achieved through the technical means.

As still other preferable embodiment of the present invention, as input picture signals, there are adopted component signals of 4:2:0 system comprising luminance signals and two color difference signals (a system where two color difference signals are divided to every other scanning lines and color signals are sampled at a rate of ½ of that of luminance signal) or 4:2:2 system (a system where both of two color difference signals are present on one scanning line and color difference signals are sampled at a rate of ½ of that of luminance signal). Various sources (for example, present TV signal, HDTV (High Definition Television) signal, EDTV (Extended Definition Television) signal, personal computer picture, package system picture and the like) can be processed in a unified manner through the technical means. Further, signal processing of two color difference signals can be performed by a memory capacity substantially the same as in luminance signal in the case of 4:2:2 system and a memory capacity of ½ of that of luminance signal in the case of 4:2:0 system.

Further, as still other preferable embodiment of the present invention, when an extremely high-speed operation is needed in signal processing (for example, when display is a high definition display or the like), a signal of progressive scanning is divided into two series of signals and signal processing of horizontal and vertical scaling for format conversion are performed to the two series of the signals. The signal processing can be performed at ½ operational speed through the technical means. Incidentally, the memory capacity necessary for the signal processing is substantially the same as in one series.

Further, an output side of the scaling unit is provided with a picture quality improving unit for executing picture quality improving processing such as color space conversion, inverse gamma conversion or the like in respect of the picture signal which has been subjected to signal processing of format conversion. According to the conventional technology, an accuracy of substantially 10 bits/picture element is needed for an output of the picture quality improving processing and therefore, it is necessary to adopt the accuracy of 10 bits/picture element in signal processing at and after the picture quality improvement. According to the present invention, the process of picture quality improvement is arranged after finishing signal processing of format conversion and therefore, respective signal processing after format conversion can be performed by a normal accuracy of 8 bits/picture element and accordingly, capacities of memories and circuit scale can be reduced.

These and other objects and many of the attendant advantages of the invention will be readily appreciated as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a first embodiment of a format conversion circuit of picture signals according to the present invention;

FIG. **2** is a block diagram of an IP convertor **1** of FIG. **1**;

FIG. **3**A is a block diagram of a multiple scan convertor **3** of FIG. **1**;

FIG. **3**B is an explanatory view of the operation of the multiple scan convertor **3** of FIG. **1**;

FIG. **4**A is a block diagram of a horizontal scaling unit **5** of FIG. **1**;

FIG. **4**B is an explanatory view of the operation of the horizontal scaling unit **5**;

FIG. **5**A is a block diagram of a vertical scaling unit **6** of FIG. **1**;

FIG. **5**B is an explanatory view of the operation of the vertical scaling unit **6**;

FIG. **6**A is an outline view of the operation of a memory in the case of a vertical compression processing of the vertical scaling unit **6** of FIG. **1**;

FIG. **6**B is an outline view of the operation of a memory in the case of a vertical expansion processing of the vertical scaling unit **6** of FIG. **1**;

FIG. **6**C is an outline view of the operation of a memory in the case of PAL 100 Hz of the vertical scaling unit **6** of FIG. **1**;

FIG. **6**D is an outline view of the operation of a memory in the case of NTSC-PAL 100 Hz of the vertical scaling unit **6** of FIG. **1**;

FIG. **6**E is an outline view of the operation of a memory in the case of PAL-NTSC conversion processing of the vertical scaling unit **6** of FIG. **1**;

FIG. **7** is a block diagram of a picture quality improving unit **8** of FIG. **1**;

FIG. **8** is a view of an embodiment of a TV receiver using a format conversion circuit of picture signals according to the present invention;

FIG. **9** is a block diagram of a second embodiment of a format conversion circuit of picture signals according to the present invention;

FIG. **10**A is a block diagram of a 2 channel division unit **53** of FIG. **9**;

FIG. **10**B is an explanatory view of the operation of the 2 channel division unit **53** of FIG. **9**;

FIG. **11**A is a block diagram of a vertical scaling unit **54** of FIG. **9**;

FIG. **11**B is an explanatory view of the operation of the vertical scaling unit **54** of FIG. **9**;

FIG. **12**A is an outline view of the operation of a memory in the case of a vertical compression processing of the vertical scaling unit **54** of FIG. **9**;

FIG. **12**B is an outline view of the operation of a memory in the case of the vertical expansion processing of the vertical scaling unit **54** of FIG. **9**;

FIG. **12**C is an outline view of the operation of a memory in the case of PAL 100 Hz of the vertical scaling unit **54** of FIG. **9**;

FIG. **12**D is an outline view of the operation of a memory in the case of NTSC-PAL 100 Hz of the vertical scaling unit **54** of FIG. **9**;

FIG. **12**E is an outline view of the operation of a memory in the case of PAL-NTSC conversion processing of the vertical scaling unit **54** of FIG. **9**;

FIG. **13** is a block diagram of a third embodiment of a format conversion circuit of picture signals according to the present invention;

FIG. **14** is a block diagram of a multi processing unit **66** of FIG. **13**;

FIG. **15**A is an outline view of the operation of the multi processing unit **66** of FIG. **13** in double windows;

FIG. **15**B is an outline view of the operation of the multi processing unit **66** of FIG. **13** in PIP display;

FIG. **16**A is an outline view of signal processing at horizontal and vertical scaling units of FIG. **13**;

FIG. **16**B is an outline view of vertical synchronizing processing of the horizontal and vertical scaling units of FIG. **13**;

FIG. **16**C is an outline view of the operation of a memory in the vertical synchronizing processing at the horizontal and vertical scaling units of FIG. **13**;

FIG. **17** is a block diagram of a fourth embodiment of a format conversion circuit of picture signals according to the present invention;

FIG. **18** is an outline view of signal processing of PIP display at a multi processing unit **73** of FIG. **17**;

FIG. **19**A is a view of picture where a format is converted into horizontal compression (normal mode);

FIG. **19**B is a view of picture where a format is converted into vertical expansion (cinema mode);

FIG. **19**C is a view of picture where a format is converted into smooth wide;

FIG. **19**D is a view of picture where a format is converted into squeeze (full mode);

FIG. **19**E is a view of picture where a format is converted into horizontal and vertical flexible compression;

FIG. **19**F is a view of picture where a format is converted into horizontal and vertical flexible expansion;

FIG. **20**A shows an equation of 4-3 line number conversion in FIG. **1**;

FIG. **20**B shows an equation of 3-4 line number conversion in FIG. **1**;

FIG. **20**C shows an equation of 6-5 line number conversion in FIG. **1**;

FIG. **20**D shows an equation of 5-6 line number conversion in FIG. **1**;

FIG. **21** is an explanatory view of signal processing with an object of 525/60/1:1 (aspect 16:9) display;

FIG. **22** is an explanatory view of signal processing with an object of 625/100/2:1 (aspect 16:9) display; and

FIG. **23** is an explanatory view of signal processing with an object of 1125/60/2:1 (aspect 16:9) display.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

(Embodiment 1)

FIG. **1** is a block diagram showing a first embodiment of a format conversion signal processing circuit of picture signals according to the present invention. A detailed explanation will be given later of detailed structures of respective blocks in reference to drawings of numerals designating the blocks.

An Input picture signal **S1** (comprising component luminance and color difference signals of 4:2:2 system or 4:2:0 system or the like) is inputted to an IP convertor **1** and a selector **4**. The IP convertor **1**, constituting a first convertor which is the front stage of the scanning convertor, forms a signal of scanning lines skipped in interlace scanning by motion-adaptive process or motion compensative interpolation in respect of the input picture signal of interlace scanning, and outputs a transmission scanning line signal SM transmitted in interlace scanning and an interpolation scanning line signal SI formed by the above-described interpolation. A multiple scan convertor **3**, constituting the back stage of the scanning convertor, performs signal processing of ½ compression of time axis in the horizontal direction and time-division multiplex in respect of the signals SM and SI respectively and outputs a picture signal SP of progressive scanning. Thus the scanning convertor is formed with the IP convertor **1** and the multiple scan convertor **3**.

A selector **4** is constituted by a switch circuit for selecting the signal SP when the input picture signal **S1** is the present television (hereinafter, abbreviated as TV) signal of interlace scanning and the input picture signal **S1** when the input picture signal **S1** is an EDTV signal, a personal computer picture signal or a HDTV signal of progressive scanning, respectively and outputting the signal **S1** or the signal SP as a signal **S2**.

A horizontal scaling unit **5** inputs the signal **S2** of progressive scanning outputted from the selector **4**, performs signal processing for converting K picture elements into L picture elements in respect of the horizontal direction of the picture (hereinafter, abbreviated as horizontal K-L conversion), and performs horizontal expansion (K<L) or horizontal compression (K>L) and outputs a converted signal **S3**. A vertical scaling unit **6** performs signal processing for converting K scanning lines into L scanning lines in respect of the vertical direction of the picture (hereinafter, abbreviated as vertical K-L conversion) and performs vertical expansion (K<L) or vertical compression (K>L). Further, depending on the input signals **S1**, system conversion (for example, system conversion between PAL system and NTSC system), signal processing of synchronization

and signal processing of PAL 100 Hz when the field frequency of display is 100 Hz, are also performed. Further, a picture signal S4 with the format of which is converted, are outputted. Further, it is preferable in view of simplifying signal processing to provide the horizontal scaling unit **5** on the input side of the vertical scaling unit **6** when horizontal compression (K>L) is performed and provide the horizontal scaling unit **5** on the output side of the vertical scaling unit **6** when horizontal expansion (K<L) is performed.

A picture quality improving unit **8** inputs the picture signal S4 outputted from the vertical scaling unit **6** that is the final stage of format conversion, performs signal processing of picture quality improvement such as black stretching, white stretching or the like of luminance signals, color space conversion and the like and converts them into RGB signals of three primary colors. Further, signal processing of inverse gamma conversion is performed when a display is a linear property display. Further, a three primary colors picture signal S5 is outputted. A conventionally known one may be used for the picture quality improving unit **8**.

A multiplex unit **9** performs signal processing for multiplexing another three primary colors picture signal S7 for multi pictures displaying (for example, double windows, PIP display, multi windows or the like) in respect of the signal S5. Further, a picture signal S6 in conformity with a format of a display is outputted.

A microprocessor unit **10** sets signal processing parameters based on a picture format signal SPI (information of kind of input picture signals S1, format of display, mode of picture display and the like) and controls the respective blocks **1**, **3**, **4**, **5**, **6**, **8** and **9**. The picture format signal SPI is automatically detected from a frame number, synchronization signal and the like of the input picture signal S1 and from the picture output device at a detector **0**. The picture format signal SPI may naturally be generated manually.

A control unit **11** forms synchronization signal, control signal, clock signal and the like necessary for signal processing at the respective blocks and supplies them to the respective blocks. Further, information SD necessary for synchronizing processing in multi windows is outputted. That is, a control unit for generally controlling the respective blocks is constituted by the microprocessor unit **10** and the control unit **11**.

An explanation will be given of the constitution of the principal blocks of FIG. **1** as follows.

FIG. **2** is a view of a constitution example of the IP convertor **1** and a memory **2** of FIG. **1**. Motion-adaptive interpolation is performed. The circuit is substantially the same as a conventionally known circuit.

A portion of luminance signal S1(Y) of the input picture signal S1 is outputted as a luminance signal SM(Y) of the transmission scanning line signal SM. Meanwhile, an interpolation signal suitable for moving picture is formed by adding at an adder **13** a signal delayed by **1**H period at an **1**H delay unit **12** (notation H designates a period of horizontal scanning line which remains the same in the following explanation) and multiplying a coefficient value ½ at a coefficient product unit **14**.

Further, an interpolation signal suitable for stationary picture is formed by a signal delayed by 1 field period at a field memory FD1 in the memory **2**. Further, a signal formed by delaying the signal by 1 field period at other field memory FD2, is subtracted at a subtracter **17** by which a differential signal at an interval of 1 frame is detected. A motion coefficient setting unit **18** sets a motion information coefficient having a value from 0 to 1 in accordance with an absolute value of the differential signal, that is, a magnitude of motion of picture. A MAX selecting unit **19** sets a final motion coefficient K by also using motion information of previous 1 field to avoid motion detection miss. That is, a maximum value is detected between a signal of motion of previous 1 field formed by delaying a signal at a field memory FD3 that are multiplied by a coefficient α ($0<\alpha<1$) at a coefficient product unit **20** and the motion information coefficient, and the maximum value is outputted as the final motion coefficient K ($0 \leqq K \leqq 1$, stationary: K=0). Thus the MAX selecting unit **19** constitutes a motion detector. Coefficient product units **15** multiply the interpolation signal suitable for moving picture and the interpolation signal suitable for stationary picture by coefficients K and 1−K respectively, and an adder **16** forms a luminance signal SI(Y) of the interpolation scanning line signal SI by adding the both multiplied signals.

In respect of a color difference signal S1(C) of the input picture signal S1, interpolation signals are formed by intrafield interpolation. That is, the signal S1(C) is outputted as a color difference signal SM(C) of the transmission scanning line signal SM, and a color difference signal SI(C) of the interpolation scanning line signal SI is formed by adding a signal delayed by 1 line period in a **1**H delay unit **12** to the color difference signal S1(C) at an adder **13** and multiplying the outputted signal from the adder by a coefficient value ½ at a coefficient product unit **14**.

Incidentally, the bandwidth of each of two color difference signals u and v comprising the color difference signal S1(C) inputted to the above-described IP convertor **1** and selector **4** is ½ of the bandwidth of the luminance signal S1(Y). Therefore, when the input picture signal S1 is of 4:2:2 system, two sets of the circuit having the bandwidth of nearly ½ of the bandwidth of the luminance signal S1(Y) are prepared for processing the two signals u and v. For example, the circuit of the above-described IP convertor **1** has such a constitution. However, the circuit for the color difference signal S1(C) is not limited thereto but one set of a circuit can be prepared by using a color signal multiplex unit which multiplexes the two signals u and v into a time-division multiplex color signal. In this case, the bandwidth of the time-division multiplex color signal becomes double and nearly the same as the bandwidth of the luminance signal S1(Y). Therefore, the circuit for processing the time-division multiplex color signal forms one set of the circuit having nearly the same as the bandwidth of the luminance signal S1(Y). Thereby, the circuit for processing the time-division multiplex color signal can be simplified by reducing the number of circuits. The time-division multiplex color signal outputted from the color signal multiplex unit is inputted to the IP convertor **1** and the selector **4**.

FIG. **3**A and FIG. **3**B are a view of the constitution of a multiple scan convertor **3** of FIG. **1** and a view for explaining the function of a line memory **21** of FIG. **3**A, respectively.

The signals SM(Y) and SM(C) of the transmission scanning line signal SM are stored to line memories **21-1** respectively and the signals SI(Y) and SI(C) of the interpolation scanning line signal SI are stored to line memories **21-2** respectively for 1 line period at an operational speed of interlace scanning by a write operation (hereinafter, abbreviated as WT operation) shown by FIG. **3**B.

According to a read operation (hereinafter, abbreviated as RD operation) from the line memories, the line memories **21-1** and **21-2** are alternately read in 1 line period (½fH) (½ time period of interlace scanning) successively at the operational speed of progressive scanning. Further, the signals from the line memories **21-1**, **21-2** are multiplexed time-

sequentially at a multiplex unit **22** and a luminance signal SP(Y) and a color difference signal SP(C) of the signal SP of progressive scanning are provided as outputs thereof.

FIG. **4**A and FIG. **4**B are a view showing the constitution of the horizontal scaling unit **5** of FIG. **1** and a view showing signal processing parameters for performing selective control of switches in various signal processing, respectively.

According to signal processing of compression in a horizontal direction (hereinafter, abbreviated as horizontal compression), output lines of switches **24**(SW**1**), **28**(SW**2**) and **31**(SW**4**) are connected to terminals "a" and an output line of a switch **30**(SW**3**) is connected to a terminal "b". A luminance signal S**2**(Y) of the signal S**2** of progressive scanning is subjected to band restriction by low pass frequency characteristic at a horizontal LPF **23** to remove horizontal high frequency components constituting an aliasing noise in compression processing. Next, linear interpolation process of horizontal K-L conversion (K>L) of picture elements is performed at a calculation unit constituted by a 1 picture element delay unit **25**, coefficient product units **26** and an adder **27**. That is, an input signal to the delay unit **25** and a signal delayed by 1 picture element by the delay element **25** are respectively multiplied by coefficient values β and $1-\beta$ $(1>\beta\geqq 0)$ at the coefficient product units **26** and the both are added at the adder **27** thereby providing a signal of L picture elements formed from K picture elements by the horizontal K-L conversion. Further, the coefficient values β and $1-\beta$ are changed at the respective picture elements with K picture elements as a period. The signal of L picture elements is stored to a **1**H memory **29** by intermittent WT operation. Further, a signal from the memory **29** is read continuously by RD operation. A signal S**3**(Y) of the signal S**3** which has been subjected to horizontal compression by a multiplication factor of L/K is provided as the output from the switch **31**.

According to signal processing of expansion in a horizontal direction (hereinafter, abbreviated as horizontal expansion), the output lines of the switches **24**(SW**1**) and **28**(SW**2**) are connected to terminals "b" and the output lines of the switches **30**(SW**3**) and **31**(SW**4**) are connected to the terminals "a". The luminance signal S**2**(Y) of progressive scanning is continuously stored to the **1**H memory **29** by WT operation. Further, in RD operation, repetition RD operation is performed at portions of period and a signal of K of picture elements is read in a period of L picture elements. Linear interpolation process of K-L conversion (K<L) of picture elements is performed by the calculation unit constituted by the 1 picture element delay unit **25**, the coefficient product units **26** and the adder **27**. That is, an input signal to the delay unit **25** and a signal delayed by 1 picture element at the delay unit **25** are multiplied by the coefficient values β and $1-\beta$ at the coefficient product units **26** and the both are added at the adder **27** thereby providing a signal of L picture elements formed from K picture elements by K-L conversion. Incidentally, the coefficient values β and $1-\beta$ are changed at the respective picture elements with L picture elements as a period. A signal S**3**(Y) of the signal S**3** which has been subjected to horizontal expansion by a multiplication factor of L/K is provided as the output from the switch **31**(SW**4**). Further, as mentioned above, in respect of signal processing of horizontal expansion, it is preferable to provide the horizontal scaling unit **5** on the output side of the vertical scaling unit **6**.

Through processing is performed when horizontal compression or expansion is not needed in which the switch **31** is connected to the terminal "b" and the input signal S**2**(Y) is provided at the output of the switch **31** as a signal S**3**(Y) of the signal S**3** which has not been subjected to compression or expansion processing.

Also in respect of a color difference signal S**2**(C) of the signal S**2** of progressive scanning, signal processing by the constitution the same as in the case of the luminance signal S**2**(Y) is performed thereby providing a color difference signal S**3**(C) the signal S**3** which has been subjected to horizontal compression, horizontal expansion or through.

FIG. **5**A and FIG. **5**B are a view showing the constitution of the vertical scaling unit **6** of FIG. **1** and a view showing signal processing parameters of selective control of switches in various signal processing, respectively. According to signal processing of compression in a vertical direction (hereinafter, abbreviated as vertical compression), output lines of switches **33**(SW**1**), **37**(SW**2**) and **39**(SW**4**) are connected to terminals "a" and an output line of switch **38**(SW**3**) is connected to a terminal "b", respectively. The luminance signal S**3**(Y) of picture signal of progressive scanning is subjected to band restriction of low pass frequency characteristic at a vertical LPF **32** to remove vertical high frequency components constituting an aliasing noise in compression processing. Linear interpolation process of vertical K-L conversion (K>L) of lines is performed by a calculation unit constituted by a 1 line delay element **34**, coefficient product units **35** and an adder **36**. That is, an input signal to the memory unit **34** and a signal delayed by 1 line at the memory unit **34** are multiplied by coefficient values β and $1-\beta$ at the coefficient product units **35** and the both are added at the adder **36** thereby providing a signal of L lines formed from K lines by vertical K-L conversion as the output. Incidentally, the coefficient values β and $1-\beta$ are changed at the respective lines with K lines as a period. As shown by FIG. **6**A, at a memory M-**1** in a memory **7**, WT operation and RD operation are performed with 1 field period as a period. In WT operation, the signal formed by vertical K-L conversion is intermittently written and stored. Meanwhile, in RD operation, a signal from the memory M-**1** is read continuously from time point delayed by $(1-L/K)$ field period. Thus, a signal S**4**(Y) of the signal S**4** which has been subjected to vertical compression by a multiplication factor of L/K is provided as the output from the switch **39**(SW**4**). As memory capacity necessary for signal processing of vertical compression as described above, a capacity for $(1-L/K)$ field period is sufficient.

According to signal processing of expansion in a vertical direction (hereinafter, abbreviated as vertical expansion), the output lines of the switches **33**(SW**1**) and **37**(SW**2**) are connected to the terminals "b" and the output lines of the switches **38**(SW**3**) and **39**(SW**4**) are connected to the terminals "a", respectively. In the memory M-**1**, WT operation and RD operation are performed with 1 field period as one period as shown by FIG. **6**B. The luminance signal S**3**(Y) of progressive scanning is stored continuously by WT operation. Meanwhile, with respect to RD operation, repetition RD operation is performed at portions of period and a signal of L lines is read in a period of K lines. Next, linear interpolation process of vertical L-K conversion (L<K) of lines is performed by the calculation unit constituted by the 1 line delay element **34**, the coefficient product units **35** and the adder **36**. That is, an input signal to the memory unit **34** and a signal delayed by 1 line at the memory unit **34** are multiplied by the coefficient values β and $1-\beta$ at the coefficient product units **35** and the both are added at the adder **36** thereby providing a signal of K lines formed from L lines by L-K conversion as the output. Incidentally, the coefficient values β and $1-\beta$ are changed at the respective lines with K lines as a period. Thus, a signal S**4**(Y) of the signal S**4** which

has been subjected to vertical expansion at a multiplication factor K/L is provided as the output from the switch **39**(SW). As memory capacity necessary for signal processing of vertical expansion as described above, a capacity of (1−L/K) field period is sufficient.

Signal processing of PAL 100 Hz is for converting a signal having the field frequency of 50 Hz to a signal of interlace scanning of 100 Hz (hereinafter, abbreviated as 625/100/2:1) to remove flickers of PAL television system converted into progressive scanning (hereinafter, abbreviated as 625/50/1:1). The processing is realized by connecting the output lines of the switches **37**(SW2) and **38**(SW3) to the terminals "b" and connecting the output line of the switch **39**(SW4) to the terminal "a". In the memory M-**1**, WT operation and RD operation as shown by FIG. **6**C are performed. The luminance signal S**3**(Y) of the PAL signal of progressive scanning is continuously stored by WT operation with 1 field period as a period. Meanwhile, in RD operation, a signal from the memory M-**1** is read in the order of a signal of odd number scanning lines of progressive scanning (designated by ○-**0** in FIG. **6**C) and a signal of even number scanning lines (designated by ○-E in FIG. **6**C) from time point delayed by 0.5 field period. Thus, a signal S**4**(Y) of the signal S**4** of PAL 100 Hz is provided as the output from the switch **39**(SW4). As memory capacity necessary for signal processing of PAL 100 Hz described above, the capacity of 0.5 field period is sufficient.

According to signal processing of NTSC-PAL 100 Hz, a NTSC signal converted into progressive scanning (hereinafter, abbreviated as 525/60/1:1) is converted into a signal of 625/100/2:1 system. The processing is realized by connecting the output lines of the switches **33**(SW1) and **37**(SW2) to the terminals "b", the output line of the switch **38**(SW3) to a terminal "c" and the output line of the switch **39**(SW4) to the terminal "a", respectively. As shown by FIG. **6**D, the luminance signals S**3**(Y) of the NTSC signal of progressive scanning is stored continuously to the memory M-**1** by WT operation with NTSC 1 field period as a period. Meanwhile, in RD operation, repetition RD operation is performed at portions of period with PAL 1 field period as a period by which a signal of 5 lines is read in a time period of 6 lines.

Next, vertical expansion is performed by linear interpolation process of 5-6 line number conversion by the calculation unit constituted by the 1 line memory unit **34**, the coefficient product units **35** and the adder **36**. That is, an input signal to the memory unit **34** and a signal delayed by 1 line at the memory unit **34** are multiplied by the coefficient values β and 1−β at the coefficient product units **35** and both are added at the adder **36** thereby providing a signal of 6 lines formed from 5 lines by 5-6 line number conversion as the output. Incidentally, the coefficient values β and 1−β are changed at the respective lines with 6 lines as a period. At a memory M-**2** of the memory **7**, the signal outputted from the adder **36** and supplied to the memory M-**2** is stored continuously by WT operation with PAL 1 field period as a period. Meanwhile, in RD operation, a signal outputted from the memory M-**2** is read in the order of a signal of odd number scanning lines (○-**0** in FIG. **6**D) and a signal of even number scanning lines (○-E in FIG. **6**D) from time point delayed by 0.5 field period. Thus, a signal S**4**(Y) of the signal S**4** of NTSC-PAL 100 Hz is provided as the output from the switch **39**(SW4). As memory capacity necessary for signal processing of NTSC-PAL 100 Hz as described above, a capacity of 1 field period for NTSC-PAL conversion and 0.5 field period for field multiple scan conversion is sufficient.

According to signal processing of PAL-NTSC conversion, a signal of 625/50/1:1 system is converted into a signal of 525/60/1:1 system in which the output lines of the switches **33**(SW1) and **37**(SW2) are connected to the terminals "a", the output line of the switch **38**(SW3) is connected to the terminal "b" and the output line of the switch **39**(SW4) is connected to the terminal "a", respectively. The luminance signal S**3**(Y) of PAL system of progressive scanning is subjected to band restriction by low pass frequency characteristic at the vertical LPF **32**. Next, vertical compression is performed by linear interpolation process of 6-5 line number conversion by the calculation unit constituted by the 1 line memory unit **34**, the coefficient product units **35** and the adder **36**. That is, an input signal to the memory unit **34** and a signal delayed by 1 line at the memory unit **34** are multiplied by the coefficient values β and 1−β at the coefficient product units **35** and both are added at the adder **36** thereby providing a signal of 5 lines formed from 6 lines by 6-5 line number conversion as the output. Incidentally, the coefficient values β and 1−β are changed for the respective lines with 6 lines as a period. As shown by FIG. **6**E, at the memory M-**1** a signal formed by 6-5 line number conversion is intermittently written and stored by WT operation with PAL 1 field period as a period. Meanwhile, a signal outputted from the memory M-**1** is read in RD operation with NTSC 1 field period as a period. Thus, a signal S**4**(Y) of the signal S**4** which has been subjected to PAL-NTSC conversion is provided as the output from the switch **39**(SW4). As memory capacity necessary for signal processing of PAL-NTSC conversion as described above, a capacity of 1 field period is sufficient.

Through processing is performed when processing of vertical compression or expansion is not needed in which the output line of the switch **39**(SW4) is connected to the terminal "b" and a signal S**4**(Y) of the signal S**4** which has not been subjected to processing of compression or expansion is provided as the output from the switch **39**.

Also in respect of the color difference signal S**3**(C) of picture signal of progressive scanning, signal processing by the constitution the same as in the luminance signal is performed thereby providing a signal S**4**(C) of the signal S**4** of vertical compression, vertical expansion, PAL 100 Hz, NTSC-PAL 100 Hz, PAL-NTSC conversion or through processing. Incidentally, the parameters and the coefficients of signal processing for driving the switches in FIG. **4**A, FIG. **4**B and FIG. **5**A and FIG. **5**B are provided from the microprocessor of FIG. **1**. The same goes with other embodiments shown below.

As described above, according to the vertical scaling unit, various signal processing necessary for format conversion can be carried out with an extremely small memory capacity.

FIG. **19**A through FIG. **19**F show pictures of representative examples in format conversion of picture signal. In FIG. **19**A, a picture is horizontally compressed to display a picture of aspect ratio of 4:3 on a display screen of aspect ratio of 16:9, which is referred to as normal mode. In FIG. **19**B, a picture is vertically expanded to display a letter box picture in a screen of aspect ratio of 16:9, which is referred to as cinema mode. In FIG. **19**C, the left and right corner areas of a picture of aspect ratio of 4:3 are gradually expanded and are displayed in a full screen of aspect ratio of 16:9, which is referred to as smooth wide. In FIG. **19**D, picture of aspect ratio of 4:3 compressed horizontally is displayed in a full screen of aspect ratio of 16:9, which is referred to as full mode. In FIG. **19**E, picture is displayed by compressing in the horizontal and the vertical directions by an arbitrary magnification. Further, in FIG. **19**F, picture is

displayed by expanding in the horizontal and vertical directions by an arbitrary magnification (referred to as zoom mode).

FIG. **20**A through FIG. **20**D show equations of representative processing of K-L conversion used in signal processing of format conversion.

4-3 conversion of FIG. **20**A is used in normal mode. A matrix shown in FIG. **20**A indicates a corresponding relationship between 4 points of input series X**1**, X**2**, X**3** and X**4**, and 3 points of output series Y**1**, Y**2** and Y**3**. Therefore, in the above-described calculation unit, the coefficient values (β, 1−β) are changed to (1, 0), (2/3, 1/3), (1/3, 2/3) thereby forming the output series. 3-4 conversion of FIG. **20**B is used in cinema mode. A matrix in FIG. **20**B indicates a corresponding relationship between 4 points of input series X**1**, X**2**, X**3** and X**4** (incidentally, X**4** is used also for X**1** of next input series), and 4 points of output series Y**1**, Y**2**, Y**3** and Y**4**. Therefore, in the above-described calculation unit, the coefficient values (β, 1−β) are changed to (0, 1), (1/4, 3/4), (2/4, 2/4), (3/4, 1/4) thereby forming the output series. Further, FIG. **20**C shows an example of 6-5 conversion used in PAL-NTSC conversion and FIG. **20**D shows an example of 5-6 conversion used in NTSC-PAL conversion.

FIG. **21** shows signal processing at the IP convertor **1**, the horizontal and vertical scaling units **5** and **6** with an object of display of a picture signal (526/60/1:1) and aspect ratio of 16:9. In FIG. **21**, circle mark in IP conversion represents an operation of carrying out IP conversion.

In respect of the input signal S**1** of 525/60/2:1 system (corresponding to present NTSC system), format conversion in correspondence with various display modes is carried out to the signal converted to progressive scanning at the IP convertor **1**.

In respect of the input signal S**1** of 525/60/1:1 system (corresponding to EDTV system), the IP conversion is not carried out since it is progressive scanning and through processing, expansion and compression are carried out in accordance with display modes.

In respect of the input signal S**1** of 1125/60/2:1 system (corresponding to HDTV) 17-16 conversion is carried out at the vertical scaling unit **6** and the input signal is converted from interlace scanning to progressive scanning. Further, processing of expansion and compression are carried out in accordance with display modes.

In respect of the input signal S**1** of 625/50/2:1 system (corresponding to present PAL system), frame rate conversion and 6-5 line number conversion are carried out at the vertical scaling unit **6** to the signal converted into progressive scanning at the IP convertor **1**. Also, format conversion in correspondence with various display modes is carried out.

The input signal S**1** of PC system (personal computer picture) is of progressive scanning of 60 frames/second and therefore, the IP conversion is not carried out and processing of normal mode display is performed at horizontal and vertical scaling units **5** and **6**. That is, in VGA system (640×480), horizontal 4-3 line number conversion is performed, in SVGA system (800×600), horizontal 4-3 line number conversion and vertical 5-4 line number conversion are performed and in XGA system (1024×768), horizontal 4-3 line number conversion and vertical 8-5 line number conversion are performed.

FIG. **22** shows signal processing at the IP convertor **1**, the horizontal and the vertical scaling units **5** and **6** with an object of display of 625/100/2:1 and aspect ratio of 16:9.

In respect of the input signal S**1** of 525/60/2:1 system (corresponding to present NTSC system), frame rate conversion, 5-6 line number conversion and field multiple scan conversion are performed at the vertical scaling unit **6** to the signal converted into progressive scanning at the IP convertor **1**. Also, format conversion in correspondence with various display modes is performed.

In respect of the input signal S**1** of 525/60/1:1 system (corresponding to EDTV system), the IP conversion is not carried out since it is progressive scanning and frame rate conversion, 5-6 line number conversion and field multiple scan conversion are performed at the vertical scaling unit **6**. Further, processing of through, expansion and compression are performed in accordance with display modes.

In respect of the input signal S**1** of 1125/60/2:1 system (corresponding to HDTV), frame rate conversion, 15-16 line number conversion and field multiple scan conversion are performed at the vertical scaling unit **6**. Further, processing of expansion and compression are performed in accordance with display modes.

In respect of the input signal S**1** of 625/50/2:1 system (corresponding to present PAL system), field multiple scan conversion is performed at the vertical scaling unit **6** to the signal converted into progressive scanning at the IP convertor **1**. Further, format conversion in correspondence with various display modes is performed.

The input signal of PC system (personal computer picture) is of progressive scanning of 60 frames/second and therefore, the IP conversion is not carried out and frame rate conversion and field multiple scan conversion are performed at the vertical scaling unit **6**. Further, processing for normal mode display is performed. That is, in VGA system (640×480), horizontal 4-3 line number conversion and vertical 5-6 line number conversion are performed, in SVGA system (800×600), horizontal 4-3 line number conversion is performed and in XGA system (1024×768), horizontal 4-3 line number conversion and vertical 4-3 line number conversion are performed.

FIG. **23** shows signal processing at the IP convertor and the horizontal and vertical scaling units with an object of display of 1125/60/2:1 and aspect ratio of 16:9.

In respect of the input signal S**1** of 525/60/2:1 system (corresponding to present NTSC system), format conversion in correspondence with various display modes is carried out to the signal converted into progressive scanning at the IP convertor **1**. Further, 16-17 line number conversion is also carried out at the vertical scaling unit **6** and the signal inputted to the unit **6** is converted into a signal of interlace scanning.

In respect of the input signal S**1** of 525/60/1:1 system (corresponding to EDTV system), the IP conversion is not carried out since it is progressive scanning and processing of through, expansion and compression are performed in accordance with display modes. Incidentally, 16-17 line number conversion is also carried out at the vertical scaling unit **6** and the signal inputted to the unit **6** is converted into a signal of interlace scanning.

In respect of the input signal S**1** of 1125/60/2:1 system (corresponding to HDTV), processing of expansion and compression are carried out in accordance with display modes.

In respect of the input signal S**1** of 625/50/2:1 system (corresponding to present PAL system), frame rate conversion and 16-15 line number conversion are carried out at the vertical scaling unit **6** to the signal converted into progressive scanning at the IP convertor **1** and the signal inputted to the unit **6** is converted into a signal of interlace scanning. Also, format conversion in correspondence with various display modes is performed.

The input signal of PC system (personal computer picture) is of progressive scanning of 60 frames/second and

accordingly, the IP conversion is not performed and a processing of normal mode display is performed at the horizontal and vertical scaling unit **5** and **6**. That is, in VGA system (640×480), horizontal 4-3 line number conversion and vertical 16-17 line number conversion are performed, in SVGA system (800×600), horizontal 4-3 line number conversion and vertical 20-17 line number conversion are performed and in XGA system (1024×768), horizontal 4-3 line number conversion and vertical 32-21 line number conversion are performed.

Next, FIG. **7** shows an example of the constitution of the picture quality improving unit **8** of FIG. **1**. The luminance signal S**4**(Y) of picture signal, which has been subjected to format conversion processing, is inputted to a luminance processing unit **74** where signal processing of image enhancer, black stretching and white stretching are carried out. Further, the color difference signal S**4**(C) of picture signal which has been subjected to format conversion is inputted to a picture element interpolation unit **75** where signal processing for demodulating the color signal S**4**(C) into color difference signals U and V having the structure of sample point the same as in the luminance signal. A color space convertor **76** carries out conversion processing from a luminance and color difference system to a three primary colors RGB system. Further, an inverse gamma processing unit **77** carries out signal processing of inverse gamma correction for a display having a linear characteristic. A selector **78** selects a signal from the color space convertor in a display having a gamma characteristic as in CRT or the like and selects a signal from the inverse gamma processing unit **77** in a display having a linear characteristic as in a liquid crystal display device or a plasma display panel and outputs them as three primary color image signals S**5**.

As mentioned in the above embodiment, according to the present invention, a method and a circuit for signal processing of format conversion of picture signal having inconsiderable deterioration of picture quality accompanied by signal processing and an extremely small memory capacity for use at low cost, can be realized.

Further, FIG. **8** shows an embodiment of a television receiver using a circuit for signal processing of format conversion of picture signal according to the embodiment. Respective blocks shown in FIG. **8** and a picture output device (not illustrated) are integrated into a television receiver. A conventionally known one may be used for the picture output device.

Terrestrial broadcast wave is received by a UV tuner **40** and demodulated into a picture signal of base band. Satellite broadcast wave is received by a BS/CS tuner **41** and is demodulated into a picture signal of base band. Further, a switcher **42** selects and outputs one from the demodulated picture signals and picture signals of the package (CD-ROM, video tape) systems.

A present system decoder **43** performs signal processing of YC (luminance and color) separation and color demodulation in respect of a picture signal of NTSC system or PAL system and demodulates the signal into luminance and color difference signals of component 4:2:2 system (or 4:2:0 system). An ED/HD decoder **44** performs signal processing of demodulation in respect of a picture signal of EDTV system or HDTV system and demodulates the signal into luminance and color difference signals of progressive scanning in EDTV system or component 4:2:2 system (or 4:2:0 system) of interlace scanning in HDTV system.

Digital broadcast wave is received by a digital receiver **45** and is demodulated into a bit stream signal by performing signal processing of descramble, error correction and the like. The bit stream signal is demodulated into luminance and color difference signals of component 4:2:2 system (or 4:2:0 system) by performing demodulation processing at an MPEG decoder **46**.

A PC picture signal (three primary colors RGB signal) is inputted to a PC processing unit **47** and converted into luminance and color difference signals of component 4:2:2 system (or 4:2:0 system) by performing signal processing of color space conversion to luminance and color difference system.

A switcher **48** selects and outputs these signals.

A picture processing unit **49-1** performs signal processing of converting a picture signal into a format of a display in the format conversion signal processing circuit of picture signals shown by FIG. **1**. In one window mode, a signal from the picture processing unit **49-1** is outputted and in multi windows mode, signals formed by multiplexing the signal from the picture processing unit **49-1** as a main picture with a signal as a sub picture from a picture processing unit **49-2** where synchronizing with the main picture is carried out by the information SD.

A multiplex unit **51** performs processing of multiplexing on screen pictures formed by OSD (On Screen Display) **50** (means for forming small other picture in one picture in case of forming pictures of personal computer or the like) to the signal, supplies the output signal to a picture output device (not illustrated in the drawings). In the picture output device, the picture whose format is converted to a predetermined display format is displayed.

A microcomputer control unit **52** sets the input signals or display modes, controls signal processing at respective blocks and the like. Incidentally, connections between the microcomputer control unit **52** and the respective blocks are omitted.

As mentioned above, by adopting the format conversion signal processing circuit of the present invention, a television receiver for receiving and displaying picture signals from various input sources can be realized at low cost by reducing necessary memories. Incidentally, in respect of the picture processing unit **49**, it may also be constituted in a second through a fourth embodiment mentioned below. Further, in the following explanation of embodiments, the same numerals are attached to constitutions or function portions substantially the same as those in the first embodiment and an explanation thereof will be omitted.

(Embodiment 2)

FIG. **9** shows a second embodiment of a format conversion signal processing circuit of picture signal according to the present invention. According to the embodiment, signal processing at horizontal and vertical scaling units is performed under a state of two series of signals of interlace scanning and thereafter, the signals are converted into a signal of progressive scanning. That is, an input picture signal is divided into two series and signal processing of horizontal and vertical scaling units is performed to each of the divided signals.

The input picture signal S**1** (comprising component luminance and color difference signals of 4:2:2 system or 4:2:0 system) is inputted to the IP convertor **1** and a 2 channel division unit **53**. The IP convertor **1** operates to the input picture signal S**1** of interlace scanning and is provided with the constitution and operation the same as those shown by FIG. **2**. The 2 channel division unit **53** forms two series of signals SM' and SI' of interlace scanning from the input picture signal S**1** of progressive scanning. The 2 channel division unit constitutes a second convertor. The selector **4** selects respectively the signals SM and SI when the input

picture signal **S1** is the present TV signal of interlace scanning and the signals SM' and SI' when the signal **S1** is the EDTV signal, the personal computer picture signal or the HDTV signal of progressive scanning and outputs the selected signals as signals **S2M** and **S2I**.

The horizontal scaling units **5** perform horizontal expansion (K<L) or horizontal compression (K>L) by signal processing of horizontal K-L conversion for each of the signals **S2M** and **S2I** and output signals **S3M** and **S3I** expanded or compressed in the horizontal direction. A vertical scaling unit **54** performs vertical expansion (K<L) or vertical compression (K>L) by signal processing of vertical K-L conversion to the signals **S3M** and **S3I**. Further, depending on the kind of the input signal **S1**, similar to Embodiment 1, signal processing of system conversion (for example, PAL-NTSC conversion) or synchronization is performed and depending on a display, signal processing of PAL 100 Hz is performed along therewith. Further, signals **S4M** and **S4I** the format of each of which is converted are outputted.

The multiple scan convertor **3** performs signal processing of ½ compression of time axis and time-division multiplex in the horizontal direction for each of the signals **S4M** and **S4I** and outputs a picture signal **S4** of progressive scanning.

FIG. **10**A and FIG. **10**B are a block diagram of the 2 channel division unit **53** of FIG. **9** and a view for explaining the operation, respectively.

The luminance signal **S1**(Y) and the color difference signal **S1**(C) of the input picture signal **S1** of progressive scanning are respectively inputted to line memories **56-1** and **56-2**. As shown by FIG. **10**B, the line memory **56-1** stores signals (scanning lines ①, ③, . . . in figure) of scanning lines corresponding to first interlace scanning in WT operation for 1 line period of fH. Meanwhile, in RD operation, signals are read for a time period of 2fH twice as much as that in WT operation by which signals SM'(Y) and SM'(C) of interlace scanning are provided.

The line memory **56-2** stores signal (scanning lines ②, ④, . . . in figure) of scanning lines corresponding to second interlace scanning in WT operation for 1 line period of fH. Meanwhile, in RD operation, signals are read for a time period of 2fH twice as much as that in WT operation by which signals SI'(Y) and SI'(C) of interlace scanning are provided.

FIG. **11**A and FIG. **11**B are a block diagram of the vertical scaling unit **54** of FIG. **9** and a view showing the operation of selective control of switches in the vertical scaling unit **54**.

According to signal processing of vertical compression at the vertical scaling unit **54**, output lines of switches **58**(SW1), **63**(SW2) and **65**(SW4) are connected to terminals "a" and an output line of the switch **64**(SW3) is connected to a terminal "b", respectively. Two series of picture signals of luminance signals **S3M**(Y) and **S3I**(Y) are subjected to band restriction by low pass frequency characteristics at a vertical LPF **57** to remove vertical high frequency components constituting an aliasing noise in compression processing. Linear interpolation process of vertical K-L conversion (K>L) is performed by a calculation unit constituted by a 1 line delay element **59**, coefficient product units **60** and adders **61**. That is, in one signal way, the signals **S3M**(Y) and **S3I**(Y) are multiplied by coefficient values β and 1−β at the coefficient product units **60** and both are added at the adder **61**. In the other signal way, a signal formed by delaying the signal **S3M**(Y) by 1 line at the 1 line delay element **59** and the signal **S3I**(Y) are multiplied by coefficient values γ and 1−γ at the coefficient product units **60** and both are added at the adder **61**.

In this method, two series of signals comprising signals of L lines formed from K lines by vertical K-L conversion are provided. Incidentally, the coefficient values β, 1−β, γ and 1−γ are changed at the respective lines. For example, in 4-3 line number conversion, the coefficient values (β, 1−β) are changed for each line such as (1,0), (1/3, 2/3), (2/3, 1/3), (1, 0), . . . , and the coefficient values (γ, 1−γ) are changed for each line such as (2/3, 1/3), (1, 0), (1/3, 2/3), (2/3, 1/3), ... As shown by FIG. **12**A, at a memory **M1** of a memory **55**, WT operation and RD operation are performed with 1 field period as a period. In WT operation, two series of signals formed by K-L conversion are intermittently written and stored. Meanwhile, in RD operation, two series of signals are continuously read from time points delayed by (1−L/K) field period and two series of signals **S4M**(Y) and **S4I**(Y) which have been subjected to vertical compression at a multiplication factor of L/K are provided as outputs of the switch **65**(SW4). As memory capacity necessary for signal processing of vertical compression described above, a capacity of (1−L/K) field period is sufficient.

According to signal processing of vertical expansion, the output lines of the switches **58**(SW1) and **63**(SW2) are connected to the terminals "b" and the output lines of the switches **64**(SW3) and **65**(SW4) are connected to the terminals "a". As shown by FIG. **12**B, at the memory **M1**, WT operation and RD operation are performed with 1 field period as a period. The luminance signals **S3M**(Y) and **S3I**(Y) of two series of picture signals are continuously stored by WT operation. Meanwhile, in RD operation, repetition RD operation is performed at portions of period and two series of signals of L lines are read in a period of K lines. Linear interpolation process of L-K conversion (L<K) of lines is performed by the calculation unit constituted by the 1 line delay element **59**, the coefficient product units **60** and the adders **61**. That is, in one signal way, the signals of **S3M**(Y) and **S3I**(Y) are multiplied by the coefficient values β and 1−β at the coefficient product units **60** and both are added at the adder **61**.

In the other signal way, a signal produced by delaying the signal **S3M**(Y) by 1 line at the 1 line delay element **59** and the signals of **S3I**(Y) are multiplied by coefficient values γ and 1−γ at the coefficient product units **60** and both are added at the adder **61**. Two series of signals comprising signals of K lines formed from L lines by L-K conversion are provided as outputs. Incidentally, the coefficients values β, 1−β, γ and 1−γ are changed at the respective lines. For example, according to 3-4 line number conversion, the coefficient values (β, 1−β) are changed for the respective lines such as (1, 0), (2/4, 2/4), (1, 0), . . . and the coefficient values (γ, 1−γ) are changed for the respective lines such as (1/4, 3/4), (3/4, 1/4), (1/4, 3/4) . . . . Further, two series of signals **S4M**(Y) and **S4I**(Y) which have been vertically expanded by a multiplication factor K/L are provided as outputs of the switch **65**(SW4). As memory capacity necessary for signal processing of vertical expansion described above, a signal of (1−L/K) field period is sufficient.

According to signal processing of PAL 100 Hz, a signal of PAL system (625/50/1:1) converted into progressive scanning is converted into a signal of PAL 100 Hz system (625/100/2:1) of interlace scanning of 100 fields/second, which is realized by respectively connecting the output lines of **SW2** and **SW3** to the terminals "b" and the output line of **SW4** to the terminal "a". At the memory **M1**, WT operation and RD operation shown by FIG. **12**C are performed. The luminance signals **S3M**(Y) and **S3I**(Y) of two series of PAL signals are stored continuously in WT operation with 1 field period as a period. Meanwhile, in RD operation, signals are

read in the order of a signal (○-**0** in figure) and a signal (○-E in figure) from time point delayed by 0.5 field period. Further, two series of signals SM**4**(Y) and S**4**I(Y) of PAL 100 Hz are provided as outputs from the switch **65**(SW**4**). As memory capacity necessary for signal processing of PAL 100 Hz described above, a capacity of 1 field period is sufficient.

According to signal processing of NTSC/PAL 100 Hz, a signal of NTSC system (525/60/1:1) converted into progressive scanning are converted into a signal of 625/100/2:1 system in which the output lines of the switches **58**(SW**1**) and **63**(SW**2**) are connected to the terminals "b", the output line of the switch **64**(SW**3**) is connected to a terminal "c" and the output line of the switch **65**(SW**4**) is connected to the terminal "a", respectively. As shown by FIG. **12**D, the luminance signals S**3**M(Y) and S**3**I(Y) of two series of NTSC system are continuously stored to the memory M**1** by WT operation with NTSC 1 field period as a period. Meanwhile, in RD operation, repetition RD operation is performed at portions of period and two series of signals of 5 lines are read in a period of 6 lines.

Next, vertical expansion is performed by linear interpolation process of 5-6 line number conversion by the calculation unit constituted by the 1 line delay element **59**, the coefficient product units **60** and the adders **61**. That is, in one signal way, the signals S**3**M(Y) and S**3**I(Y) are multiplied by the coefficient values β and 1−β at the coefficient product units **60** respectively and both are added at the adder **61**. In the other signal way, a signal formed by delaying the signal S**3**M(Y) by 1 line at the 1 line delay element **59** and the signal S**3**I(Y) are multiplied by the coefficient values γ and 1-γ at the coefficient product units **60** and both are added at the adder **61**. Two series of signals comprising signals of 6 lines formed from 5 lines by 5-6 line number conversion are provided as the outputs of addition. Incidentally, the coefficient values β, 1−β, γ and 1−γ are respectively changed at the respective lines. Signals are stored continuously in WT operation to a memory M**2** of the memory **55** with PAL 1 field as a period. Meanwhile, in RD operation, signals are read in the order of a signal (○-**0** in figure) and a signal (○-E in figure) from time point delayed by 0.5 field period. Further, two series of signals S**4**M(Y) and S**4**I(Y) of NTSC-PAL 100 Hz are provided as outputs from the switch **65**(SW**4**). As memory capacity necessary for signal processing of NTSC-PAL 100 Hz described above, a capacity of 1 field period for NTSC-PAL conversion and 1 field period for field multiplex scan conversion is sufficient.

According to signal conversion of PAL-NTSC conversion, a signal of 625/50/1:1 system is converted into a signal of 525/60/1:1 system in which the output lines of the switches **58**(SW**1**) and **63**(SW**2**) are connected to the terminals "a", the output line of the switch **64**(SW**3**) is connected to the terminal "b" and the output line of the switch **65**(SW**4**) is connected to the terminal "a", respectively. The luminance signals S**3**M(Y) and S**3**I(Y) of two series of PAL system are subjected to band restriction by low pass frequency characteristic at the vertical LPF **57**. Vertical compression is performed by linear interpolation process of 6-5 line number conversion of lines at the calculation unit constituted by the 1 line delay element **59**, the coefficient product units **60** and the adders **61**. In one signal way, the signal of S**3**M(Y) and S**3**I(Y) are multiplied by the coefficient values β and 1−β at the coefficient product units **60** and both are added at the adder **61**. In the other signal way, a signal formed by delaying the signal S**3**M(Y) by 1 line at the 1 line delay element **59** and the signal S**3**I(Y) are multiplied by the coefficient values γ and 1−γ at the coefficient product units **60** and both are added at the adder **61**. Two series of signals comprising signals of 5 lines formed from 6 lines by 6-5 line number conversion are provided as the outputs. Incidentally, the coefficient values β, 1−β, γ and 1−γ are changed at the respective lines. As shown by FIG. **12**E, at the memory M**1**, two series of signals formed by 6-5 line number conversion are intermittently written and stored by WT operation with PAL 1 field period as a period. Meanwhile, in RD operation, two series of signals are read with NTSC 1 field period as a period. Further, signals S**4**M(Y) and S**4**I(Y) which have been subjected to PAL-NTSC conversion are provided as outputs from the switch **65**. As memory capacity necessary for signal processing of PAL-NTSC conversion described above, a capacity of PAL 1 field period is sufficient.

According to through signal processing, the output line of the switch **65** is connected to the terminal "b". Further, two series of signals S**4**M(Y) and S**4**I(Y) which have not been subjected to processing of compression or expansion are provided as outputs from the switch **65**.

Also in respect of color signals S**3**M(C) and S**3**I(C) of two series of picture signals, signal processing having the constitution the same as that in luminance signals is performed and two series of signals S**4**M(C) and S**4**I(C) of vertical compression, vertical expansion, PAL 100 Hz, NTSC-PAL 100 Hz, PAL-NTSC conversion or through processing are provided.

As described above, according to the vertical scaling unit **54**, various kinds of signal processing necessary for format conversion can be carried out with an extremely small memory capacity. According to the embodiment, in respect of a display such as a high definition display requiring extremely high speed operation for signal processing, a method and a circuit for signal processing of format conversion of picture signal having inconsiderable deterioration of picture quality accompanied by signal processing and an extremely small memory capacity for use can be realized at low cost.

(Embodiment 3)

FIG. **13** shows a third embodiment of a format conversion circuit of picture signal according to the present invention. According to the embodiment, a multi processing unit **66** for synthesizing two series of input picture signals and a selector **67** are added to the constitution shown by FIG. **1**, which is preferable in the case where both of functions of double windows and PIP display are realized. In FIG. **13**, portions having the constitution and function substantially the same as those in FIG. **1** are attached with notations the same as those in FIG. **1** and a detailed explanation thereof will be omitted.

A first input picture signal S**1** (comprising component luminance and color difference signals of 4:2:2 system or 4:2:0 system) is inputted to the multi processing unit **66** and the selector **67**. Further, a second input picture signal S**1**' (comprising component luminance and color difference signals of 4:2:2 system or 4:2:0 system) is inputted to the multi processing unit **66**.

At the multi processing unit **66**, signal processing of multiplexing the first and the second picture signals into a time-division multiplex signal is carried out by which a signal for double windows or PIP display is formed. The selector **67** outputs the first picture signal S**1** in one window mode and a signal from the multi processing unit **66** in double windows or PIP display mode.

FIG. **14** is a block diagram showing the constitution of the multi processing unit **66**, FIG. **15**A is a view for explaining an outline of the operation of the multi processing unit in

double windows according to the embodiment and FIG. **15**B is a view for explaining an outline of the operation of the multi processing unit in PIP display, respectively.

As shown by FIG. **14**, at horizontal LPFs **68**, horizontal high frequency components are removed by low pass characteristic to avoid an aliasing noise accompanied by sub sampling processing. Further, at sub sampling units **69**, signal processing of sub sampling of 2:1 in double windows and 6:1 in PIP display is performed. As mentioned later, selectors **70** select signals of **S1** and **S1'** in double windows of cut mode and signals from the sub sampling units **69** in the other cases.

Line memories **71** perform WT operation and RD operation shown by FIGS. **15**A and **15**B. Output signals from the line memories **71** are subjected to time division multiplex at a multiplex unit **72** by which a signal for double windows or PIP display is formed. A detailed description will be given of the operation of the line memories **71** in reference to FIGS. **15**A and **15**B as follows. Both FIGS. **15**A and **15**B show a case where 1 line is constituted by 910 picture elements and a number of effective picture elements among them is 768.

FIG. **15**A shows the operation of the memories **71** in double windows. In cut mode, each of picture signals **S1** and **S1'** is displayed at ⅜ of screen (hatched region in figure). Accordingly, in WT operation, signals of 454 picture elements shown by dots are stored with 1 line period as a period. Incidentally, phases of horizontal synchronization are shifted normally between the signals **S1** and **S1'**. Meanwhile, RD operation is performed by a synchronizing system of the signal **S1**. A signal (○-L in figure) of the signal **S1** is read in a period of 454 picture elements from the front of 1 line, and a signal (○-R in figure) of the signal **S1'** is read in a period of successive 454 picture elements. In RD operation, horizontal synchronization is performed by which horizontally synchronized output signals are provided. Incidentally, although according to the output signals, phases of vertical synchronization are shifted in the signals **S1** and **S1'**, the shift is corrected by signal processing of vertical (V) synchronization at a vertical scaling unit **6**, mentioned later.

In full mode, full pictures (dot regions in figure) of the picture signals **S1** and **S1'** are displayed respectively. Therefore, in WT operation, signals of 384 picture elements subjected to 2:1 sub sampling are stored with 1 line period as a period. Meanwhile, RD operation is performed by the synchronizing system of the signal **S1**. A signal (○-L in figure) of the signal **S1** is read at an earlier half of 1 line, and a signal (○-R in figure) of the signal **S1'** is read in a later half thereof. Output signals which have been subjected to horizontal (H) synchronization are provided by the RD operation. Incidentally, similar to cut mode, phase shift in vertical synchronization is corrected by signal processing of vertical synchronization at a vertical scaling unit **6**, mentioned later.

FIG. **15**B shows operation of the memories **71** in PIP display. In this case, a main picture is constituted by picture of the signal **S1**, and a sub picture is constituted by picture of cinema mode formed by compressing picture of the signal **S1'** by ⅓. Therefore, according to WT operation, all of 768 effective picture elements of the signal **S1** are stored with 1 line as a period. Further, in respect of the signal **S1'**, a signal of 128 picture elements which has been subjected to 6:1 sub sampling is stored. Meanwhile, RD operation is performed by the synchronizing system of the signal **S1**, in which the 768 picture elements signal of the signal **S1** is read from the front of 1 line and the 128 picture elements signal of the signal **S1'** is read successively. Output signals which have been subjected to horizontal synchronization are provided by the RD operation. Further, phase shift of vertical synchronization is corrected by signal processing of vertical synchronization at a vertical scaling unit **6**, mentioned later.

FIG. **16**A shows content of signal processing of horizontal and vertical scaling units **5** and **6** in double windows and PIP display, FIG. **16**B shows an outline view of vertical synchronization and FIG. **16**C shows an outline of the operation of a memory in vertical synchronization, respectively.

As shown by FIG. **16**A, in cut mode of double windows, the horizontal scaling unit **5** performs processing of 4-3 line number compression conversion and the vertical scaling unit **6** performs processing of vertical synchronization. Further, in full mode, the vertical scaling unit **6** performs processing of 3-2 line number compression conversion and vertical synchronization. Meanwhile, in PIP display, the horizontal scaling unit **5** performs 4-3 line number compression conversion in respect of a main picture, processing of 1-2 line number expansion conversion in respect of a sub picture and the vertical scaling unit **6** performs processing of 9-4 line number compression conversion and vertical synchronization in respect of the sub picture. Further, in respect of one window display, processing similar to that in the first embodiment mentioned above is carried out.

As shown by FIG. **16**B, although the signals which have been subjected to horizontal synchronization are inputted to the horizontal and vertical scaling units **5** and **6**, a phase of vertical synchronization is shifted between the signal **S1** and the signal **S1'** and causes vertical synchronizing gap. Therefore, the phase of vertical synchronization of the signal **S1'** is made to coincide with that of the signal **S1** by processing of vertical synchronization.

As shown by FIG. **16**C, in cut mode, through processing is carried out to a signal (earlier half of each line) of the signal **S1**. Meanwhile, a signal (later half of each line) of the signal **S1'** is stored to the memory **71** by WT operation. Further, RD operation is performed by the synchronization system of the signal **S1** and a signal which has been subjected to vertical synchronization is read. Incidentally, as memory capacity necessary for the signal processing, a capacity of 1 field period is sufficient at maximum.

According to full mode, in WT operation, a signal (earlier half of each line) of the signal **S1** formed by 3-2 line number conversion and a signal (later half of each line) of the signal **S1'** are intermittently written and stored. Meanwhile, in RD operation, both of reading of the signal (earlier half of each line) of the signal **S1** and reading of the signal (later half of each line) of the signal **S1'** are performed by the synchronizing system of the signal **S1**. Thereby, a signal having vertical synchronization is provided. Incidentally, as memory capacity necessary for the signal processing, a capacity of ⅓ (as mentioned before, K=3, L=2 in (1−L/K)) field period is sufficient for vertical compression and 1 field period in vertical synchronization at maximum.

As mentioned above, according to the embodiment, a method and a circuit for signal processing of format conversion of picture signal having both functions of double windows and PIP display, can be realized with inconsiderable deterioration of picture quality accompanied by signal processing and with an extremely small memory capacity for use at low cost.

(Embodiment 4)

FIG. **17** shows a fourth embodiment of a format conversion circuit of picture signal according to the present invention. The embodiment is provided with the constitution similar to that in Embodiment 3. In constituting a sub picture

for PIP display by processing the signal S1', although 6:1 sub sampling is performed in the case of Embodiment 3 in respect of the sampling operation, according to Embodiment 4, the sampling is constituted by 3:1 sub sampling by which a number of picture elements is increased. The embodiment is preferable in the case where the functions of performing double windows and PIP display are also realized similar to Embodiment 3. A multi processing unit **73** is a processing unit for carrying out such a sub sampling. Portions in FIG. **17** having the constitution and function the same as those in FIG. **1** are attached with notations the same as those in FIG. **1** and a detailed explanation will be omitted.

The first input picture signal **S1** (comprising component luminance and color difference signals of 4:2:2 system or 4:2:0 system) is inputted to the multi processing unit **73** and the selector **67**. Further, a second input picture signal **S1'** (comprising component luminance and color difference signals of 4:2:2 system or 4:2:0 system) is inputted to the multi processing unit **73**. The multi processing unit **73** performs signal processing of multiplexing the first and the second picture signals **S1** and **S1'** into a time division multiplex signal which forms a signal for double windows and a signal of the sub picture for PIP display. The selector **67** outputs the first picture signal **S1** in one window mode and a signal outputted from the multi processing unit **73** in double windows.

FIG. **18** is a view for explaining formation of the sub picture signal for PIP display at the multi processing unit **73**.

According to PIP display, a main picture is constituted by the picture of the signal **S1** and the sub picture is constituted by a picture of cinema mode formed by compressing the picture of the signal **S1'** by ⅓. Accordingly, a signal of 256 picture elements provided by performing 3:1 sub sampling to the signal **S1'** is stored to the memory **71** by WT operation with 1 line period as a period in a synchronizing system of the signal **S1'**. Meanwhile, according to RD operation, a signal is read at a speed twice as much as that of WT operation by the synchronizing system of the signal **S1**. Thereby, a sub picture signal PIP in a mode of progressive scanning having horizontal synchronization of the signal **S1** is formed. The signal PIP is subjected to processing of 9-4 line number compression conversion and vertical synchronization at the vertical scaling unit **6** by which the sub picture of cinema mode is constituted. Incidentally, except signal processing in PIP display, the constitution and signal processing of the embodiment are similar to those in Embodiment 3 and an explanation thereof will be omitted.

As mentioned above, according to Embodiment 4, a method and a circuit for signal processing of format conversion of picture signal having both functions of double windows and PIP display, can be realized with inconsiderable deterioration of picture quality accompanied by signal processing and an extremely small memory capacity for use at low cost.

According to the present invention, a method and a circuit for signal processing of format conversion of picture signal for converting a plurality of formats of picture signals into picture signals of predetermined display formats of picture output devices or performing scaling processing of flexible expansion and compression in the horizontal and the vertical directions of picture, can be realized with inconsiderable deterioration of picture quality accompanied by signal processing and an extremely small memory capacity for use at low cost. Therefore, a significant effect is achieved in promoting function of various information device terminals in correspondence with multimedia and reduction in cost.

It is further understood by those skilled in the art that the foregoing description is a preferred embodiment of the disclosed device and that various changes and modifications may be made in the invention without departing from the spirit and scope thereof.

What is claimed is:

1. A circuit for signal processing of format conversion of picture signal which performs signal processing of converting a format of an input picture signal into a predetermined display format of a picture output device, said circuit comprising:

a scanning convertor for performing first local signal processing of converting the input picture signal into a picture signal of progressive scanning when the input picture signal is of interlace scanning;

a first selector for selecting either one of the input picture signal and the picture signal of progressive scanning outputted from the scanning convertor;

a scaling unit comprising a horizontal scaling unit for performing second local signal processing of compression and expansion in a horizontal direction to a signal selected by the first selector and a vertical scaling unit performing third local signal processing of compression and expansion in a vertical direction to thereof; and

a control unit for selecting parameters of the signal processing in accordance with the format of the input picture signal and the display format of the picture output device and controlling at least the scanning convertor, the first selector and the scaling unit in accordance with the parameters of the signal processing.

2. A circuit for signal processing of format conversion of picture signal according to claim **1**, wherein the scanning convertor comprises:

a first convertor for converting the input picture signal into a transmission scanning line signal transmitted in interlace scanning and an interpolation scanning line signal formed by interpolating scanning lines skipped in interlace scanning when the input picture signal is of interlace scanning; and

a multiple scan convertor for multiplexing the transmission scanning line signal and the interpolation scanning line signal to a signal of progressive scanning by fifth local signal processing of time-division multiplex with compressing a time axis by ½.

3. A circuit for signal processing of format conversion of picture signal according to claim **2**, wherein the first convertor comprises:

a motion detector for detecting a motion coefficient of picture of the input picture signal;

a circuit for constituting a first interpolation signal and a second interpolation signal by performing an intrafield calculation and an interfield calculation respectively to the input picture signal; and

a circuit for providing the interpolation scanning line signal by varying a mixture ratio of the first interpolation signal and the second interpolation signal by the motion coefficient.

4. A circuit for signal processing of format conversion of picture signal according to claim **1**, wherein the horizontal scaling unit comprises a calculation unit for multiplying a plurality of picture elements by coefficient values, a line memory and a plurality of switches wherein signal processing of either one of compression in a horizontal direction, expansion in a horizontal direction and through processing is selectively performed by selective control of the switches.

5. A circuit for signal processing of format conversion of picture signal according to claim **1**, wherein the horizontal scaling unit comprises:

a low pass filter for removing an aliasing noise from an input signal to the horizontal scaling unit;

a 1 horizontal scanning line memory;

a first switch for selecting either one of a signal outputted from the 1 horizontal scanning line memory and a signal outputted from the low pass filter;

a calculation unit for delaying a signal outputted from the first switch by one picture element period, forming a first signal by multiplying the delayed signal by a coefficient β ($1>\beta\geqq 0$), forming a second signal by multiplying the signal outputted from the first switch by a coefficient $1-\beta$ and adding the first signal and the second signal;

a second switch for selecting either one of the input signal to the horizontal scaling unit and a signal outputted from the calculation unit and inputting the selected signal to the 1 horizontal scanning line memory;

a third switch for selecting either one of the signal outputted from the 1 horizontal scanning line memory and the signal outputted from the calculation unit;

a fourth switch for selecting either one of a signal outputted from the third switch and the input signal to the horizontal scaling unit; and

wherein signal processing of either one of compression in a horizontal direction, expansion in a horizontal direction and through processing is selectively performed by selective control of the switches.

6. A circuit for signal processing of format conversion of picture signal according to claim **1**, wherein the vertical scaling unit comprises a calculation unit for multiplying picture elements in a plurality of lines by coefficient values, field memories and a plurality of switches, wherein signal processing of either one of compression in a vertical direction, expansion in a vertical direction and through processing is selectively performed by selective control of the switches.

7. A circuit for signal processing of format conversion of picture signal according to claim **1**, wherein the vertical scaling unit comprises:

a low pass filter for removing an aliasing noise from an input signal to the vertical scaling unit;

a first field memory;

a first switch for selecting either one of an output signal read from the first field memory and a signal outputted from the low pass filter;

a calculation unit for forming a first signal by delaying a signal outputted from the first switch by one line period and multiplying the delayed output signal by a coefficient β ($1>\beta\geqq 0$), forming a second signal by multiplying the signal outputted from the first switch by a coefficient $1-\beta$ and adding the first signal and the second signal;

a second switch for selecting either one of the input signal to the vertical scaling unit and a signal outputted from the calculation unit and inputting the selected signal to the first field memory;

a second field memory for delaying the signal outputted from the calculation unit;

a third switch for selecting either one of the signal outputted from the calculation unit, an output signal read from the first field memory and an output signal read from the second field memory;

a fourth switch for selecting either one of a signal outputted from the third switch and the input signal to the vertical scaling unit; and

wherein signal processing of either one of compression in a vertical direction, expansion in a vertical direction, through processing, field multiple scanning and PAL-NTSC system conversion is selectively performed by selective control of the switches.

8. A circuit for signal processing of format conversion of picture signal according to claim **1**, wherein the horizontal scaling unit and the vertical scaling unit comprise circuits for performing the second local signal processing of compression in a horizontal direction and expansion in a horizontal direction, and the third local signal processing of compression in a vertical direction and expansion in a vertical direction respectively by linear interpolation process.

9. A circuit for signal processing of format conversion of picture signal according to claim **1**, wherein the horizontal scaling unit is a circuit for performing only signal processing of compression in a horizontal direction and through processing and the vertical scaling unit is a circuit for performing the third local signal processing to a signal outputted from the horizontal scaling unit.

10. A circuit for signal processing of format conversion of picture signal according to claim **1**, wherein the horizontal scaling unit is a circuit for performing only signal processing of expansion in a horizontal direction and through processing to a signal outputted from the vertical scaling unit.

11. A circuit for signal processing of format conversion of picture signal according to claim **1**, wherein a picture quality improving unit controlled by the control unit for performing signal processing of at least one of color space conversion and inverse gamma conversion to a signal outputted from the scaling unit is connected to an output terminal of the scaling unit.

12. A circuit for signal processing of format conversion of picture signal according to claim **11**, wherein a multiplex unit controlled by the control unit for multiplexing another display picture signal to a signal outputted from the picture quality improving unit is connected to an output terminal of the picture quality improving unit.

13. A circuit for signal processing of format conversion of picture signal according to claim **1**, further comprising:

a color signal multiplex unit for multiplexing two color difference signals of the input picture signal into a time-division multiplex signal; and

wherein the time-division multiplex signal outputted from the color multiplex unit is inputted to the scanning convertor and the first selector.

14. A television receiver comprising:

the circuit for signal processing of format conversion of picture signal according to claim **1**; and

a picture output device for displaying picture of a signal outputted from the circuit for signal processing of format conversion.

15. A method for signal processing of format conversion of a picture signal, which is for converting a format of an input picture signal into a predetermined display format of a picture output device, the method comprising the steps of:

providing a picture signal of progressive scanning directly from the input picture signal when the input picture signal is of progressive scanning, and providing a picture signal of progressive scanning by converting the input picture signal into a picture signal of progressive scanning when the input picture signal is of interlace scanning; and

performing a scaling operation of at least one of compression in a horizontal direction, expansion in a hori-

zontal direction, compression in a vertical direction, expansion in a vertical direction, and frame rate conversion on the provided picture signal of progressive scanning in accordance with the format of the input picture signal and the predetermined display format of the picture output device;

wherein the step of performing a scaling operation includes the step of controlling a scaling unit with signal processing parameters determined in accordance with the format of the input picture signal and the predetermined display format of the picture output device, the scaling unit including

a controllable horizontal scaling unit for selectively performing the compression in the horizontal direction and the expansion in the horizontal direction depending on the signal processing parameters, and

a controllable vertical scaling unit for selectively performing the compression in the vertical direction, the expansion in the vertical direction, and the frame rate conversion depending on the signal processing parameters.

16. A method for signal processing of format conversion of a picture signal according to claim **15**, wherein the compression in the horizontal direction, the expansion in the horizontal direction, the compression in the vertical direction, and the expansion in the vertical direction are performed by a linear interpolation process including the steps of:

multiplying signals of a pair of picture elements contiguously arranged respectively in the horizontal direction and in the vertical direction by coefficients; and

adding together products obtained in the multiplying step.

17. A method for signal processing of format conversion of a picture signal, which is for converting a format of an input picture signal into a predetermined display format of a picture output device, the method comprising the steps of:

providing a picture signal of progressive scanning directly from the input picture signal when the input picture signal is of progressive scanning, and providing a picture signal of progressive scanning by converting the input picture signal into a picture signal of progressive scanning when the input picture signal is of interlace scanning; and

performing a scaling operation of at least one of compression in a horizontal direction, expansion in a horizontal direction, compression in a vertical direction, expansion in a vertical direction, and frame rate conversion on the provided picture signal of progressive scanning in accordance with the format of the input picture signal and the predetermined display format of the picture output device;

wherein in performing the scaling operation,

when the scaling operation of the compression in the horizontal direction is performed, the scaling operation of either one of the compression in the vertical direction and the expansion in the vertical direction is performed after performing the scaling operation in the horizontal direction, and

when the scaling operation of the expansion in the horizontal direction is performed, the scaling operation of the expansion in the horizontal direction is performed after performing the scaling operation of either one of the compression in the vertical direction and the expansion in the vertical direction.

18. A method for signal processing of format conversion of a picture signal, which is for converting a format of an input picture signal into a predetermined display format of a picture output device, the method comprising the steps of:

providing a picture signal of progressive scanning directly from the input picture signal when the input picture signal is of progressive scanning, and providing a picture signal of progressive scanning by converting the input picture signal into a picture signal of progressive scanning when the input picture signal is of interlace scanning; and

performing a scaling operation of at least one of compression in a horizontal direction, expansion in a horizontal direction, compression in a vertical direction, expansion in a vertical direction, and frame rate conversion on the provided picture signal of progressive scanning in accordance with the format of the input picture signal and the predetermined display format of the picture output device;

wherein signal processing of at least one of color space conversion and inverse gamma conversion is performed on a picture signal which has been subjected to the scaling operation.

19. A method for signal processing of format conversion of a picture signal, which is for converting a format of an input picture signal into a predetermined display format of a picture output device, the method comprising the steps of:

providing a picture signal of progressive scanning directly from the input picture signal when the input picture signal is of progressive scanning, and providing a picture signal of progressive scanning by converting the input picture signal into a picture signal of progressive scanning when the input picture signal is of interlace scanning; and

performing a scaling operation of at least one of compression in a horizontal direction, expansion in a horizontal direction, compression in a vertical direction, expansion in a vertical direction, and frame rate conversion on the provided picture signal of progressive scanning in accordance with the format of the input picture signal and the predetermined display format of the picture output device;

wherein the input picture signal is a component signal of either one of 4:2:2 and 4:2:0 including a luminance signal and color difference signals.

20. A circuit for signal processing of format conversion of picture signal which performs signal processing of converting a format of an input picture signal into a predetermined display format of a picture output device, said circuit comprising:

a scanning convertor for performing first local signal processing of converting the input picture signal into a picture signal of progressive scanning when the input picture signal is of interlace scanning;

a first selector for selecting either one of the input picture signal and the picture signal of progressive scanning outputted from the scanning convertor;

a scaling unit comprising a horizontal scaling unit for performing second local signal processing of compression and expansion in a horizontal direction to a signal selected by the first selector and a vertical scaling unit performing third local signal processing of compression and expansion in a vertical direction to thereof; and

a control unit for selecting parameters of the signal processing in accordance with the format of the input picture signal and the display format of the picture

output device and controlling at least the scanning convertor, the first selector and the scaling unit in accordance with the parameters of the signal processing, further comprising:

a multi processing unit for inputting a first picture signal and a second picture signal both having a same format and performing fourth local signal processing of multiplexing the first picture signal and the second picture signal into a time-division multiplex signal during one scanning line period;

a second selector for constituting the input picture signal by selecting either one of the first picture signal and the time-division multiplex signal outputted from the multi processing unit; and

wherein the control unit is constituted to have the scanning convertor, the first selector and the scaling unit perform the signal processing to the first picture signal in case of one window display and perform the signal processing to the time-division multiplex signal outputted from the multi processing unit in case of double windows.

21. A circuit for signal processing of format conversion of picture signal according to claim **20**, wherein the multi processing unit comprising:

a first filter for removing an aliasing noise of the first picture signal;

a first sampling unit for sub-sampling a signal outputted from the filter;

a fourth selector for selecting either one of a signal outputted from the first sampling unit and the first picture signal;

a first line memory connected to an output terminal of the fourth selector;

a second filter for removing an aliasing noise of the second picture signal;

a second sampling unit for sub-sampling a signal outputted from the second filter;

a fifth selector for selecting either one of a signal outputted from the second sampling unit and the second picture signal;

a second line memory connected to an output terminal of the fifth selector; and

a multiplex unit for multiplexing a signal outputted from the first line memory and a signal outputted from the second line memory into a time-division multiplex signal.

22. A circuit for signal processing of format conversion of picture signal according to claim **20**, wherein the scanning convertor comprises:

a first convertor for converting the input picture signal into a transmission scanning line signal transmitted in interlace scanning and an interpolation scanning line signal formed by interpolating scanning lines skipped in interlace scanning when the input picture signal is of interlace scanning; and

a multiple scan convertor for multiplexing the transmission scanning line signal and the interpolation scanning line signal to a signal of progressive scanning by fifth local signal processing of time-division multiplex with compressing a time axis by ½.

23. A circuit for signal processing of format conversion of picture signal according to claim **20**, wherein the horizontal scaling unit comprises a calculation unit for multiplying a plurality of picture elements by coefficient values, a line memory and a plurality of switches wherein signal processing of either one of compression in a horizontal direction, expansion in a horizontal direction and through processing is selectively performed by selective control of the switches.

24. A circuit for signal processing of format conversion of picture signal according to claim **20**, wherein the vertical scaling unit comprises a calculation unit for multiplying picture elements in a plurality of lines by coefficient values, field memories and a plurality of switches, wherein signal processing of either one of compression in a vertical direction, expansion in a vertical direction and through processing is selectively performed by selective control of the switches.

25. A circuit for signal processing of format conversion of picture signal according to claim **20**, wherein the horizontal scaling unit is a circuit for performing only signal processing of compression in a horizontal direction and through processing and the vertical scaling unit is a circuit for performing the third local signal processing to a signal outputted from the horizontal scaling unit.

26. A circuit for signal processing of format conversion of picture signal according to claim **20**, wherein the horizontal scaling unit is a circuit for performing only signal processing of expansion in a horizontal direction and through processing to a signal outputted from the vertical scaling unit.

27. A television receiver comprising:

the circuit for signal processing of format conversion of picture signal according to claim **20**; and

a picture output device for displaying picture of a signal outputted from the circuit for signal processing of format conversion.

28. A method for signal processing of format conversion of picture signal, which is for converting a format of an input picture signal into a predetermined display format of a picture output device, said method comprising the steps of:

performing signal processing of multiplexing a first picture signal and a second picture signal both having a same format to a time-division multiplex signal during one scanning line period;

constituting the input picture signal by selecting either one of the first picture signal and the time-division multiplex signal;

providing a picture signal of progressive scanning directly from the input picture signal when the input picture signal is of progressive scanning and providing a picture signal of progressive scanning by converting the input picture signal into a picture signal of progressive scanning when the input picture signal is of interlace scanning; and

performing a scaling operation of at least one of compression in a horizontal direction, expansion in a horizontal direction, compression in a vertical direction, expansion in a vertical direction and frame rate conversion to the provided picture signal of progressive scanning in accordance with the format of the input picture signal and the predetermined display format of the picture output device.

29. A method for signal processing of format conversion of picture signal according to claim **28**, wherein in performing the scaling operation, when the scaling operation of the compression in the horizontal direction is performed, the scaling operation of either one of the compression in the vertical direction and the expansion in the vertical direction is performed after performing the scaling operation in the horizontal direction and when the scaling operation of the expansion in the horizontal direction is performed, the scaling operation of the expansion in the horizontal direction

is performed after performing the scaling operation of either one of the compression in the vertical direction and the expansion in the vertical direction.

30. A circuit for signal processing of format conversion of picture signal which performs signal processing of converting a format of an input picture signal into a predetermined display format of a picture output device, said circuit comprising:

a first convertor for converting the input picture signal into a transmission scanning line signal transmitted in interlace scanning and an interpolation scanning line signal formed by interpolating scanning lines skipped in interlace scanning when the input picture signal is of interlace scanning;

a second convertor for converting the input picture signal into a transmission scanning line signal transmitted in interlace scanning and an interpolation scanning line signal formed by interpolating scanning lines skipped in interlace scanning when the input picture signal is of progressive scanning;

a third selector for selecting either one of a set of the transmission scanning line signal and the interpolation scanning line signal outputted from the first convertor and a set of the transmission scanning line signal and the interpolation scanning line signal outputted from the second convertor;

a scaling unit comprising a horizontal scaling unit for performing second local signal processing of compression in a horizontal direction and expansion in a horizontal direction to each of signals selected by the third selector and a vertical scaling unit for performing third local signal processing of compression in a vertical direction and expansion in a vertical direction to thereof;

a multiple scan convertor for converting signals outputting from the scaling unit into a signal of progressive scanning by fifth local signal processing of time-division multiplex with compressing a time axis by ½; and

a control unit for selecting parameters of the signal processing in accordance with the format of the input picture signal and the predetermined display format of the picture output device and controlling at least the first convertor, the second convertor, the third selector, the scaling unit and the multiple scan convertor in accordance with the parameters of the signal processing.

31. A circuit for signal processing of format conversion of picture signal according to claim **30**, wherein the horizontal scaling unit comprises a calculation unit for multiplying a plurality of picture elements by coefficient values, a line memory and a plurality of switches, wherein signal processing of either one of compression in a horizontal direction, expansion in a horizontal direction and through processing is selectively performed by selective control of the switches.

32. A circuit for signal processing of format conversion of picture signal according to claim **30**, wherein the vertical scaling unit comprises a calculation unit for multiplying picture elements in a plurality of lines by coefficient values, field memories and a plurality of switches, wherein signal processing of either one of compression in a vertical direction, expansion in a vertical direction and through processing is selectively performed by selective control of the switches.

33. A circuit for signal processing of format conversion of picture signal according to claim **30**, wherein the horizontal scaling unit is a circuit for performing only signal processing of compression in a horizontal direction and through processing and the vertical scaling unit is a circuit for performing the third local signal processing to a signal outputted from the horizontal scaling unit.

34. A circuit for signal processing of format conversion of picture signal according to claim **30**, wherein the horizontal scaling unit is a circuit for performing only signal processing of expansion in a horizontal direction and through processing to a signal outputted from the vertical scaling unit.

35. A television receiver comprising:

the circuit for signal processing of format conversion of picture signal according to claim **30**; and

a picture output device for displaying picture of a signal outputted from the circuit for signal processing of format conversion.

* * * * *

EXHIBIT I

US007889281B2

(12) **United States Patent**
Takashimizu et al.

(10) **Patent No.: US 7,889,281 B2**
(45) **Date of Patent: *Feb. 15, 2011**

(54) **DIGITAL BROADCAST RECEIVER UNIT**

(75) Inventors: **Satoru Takashimizu**, Yokohama (JP); **Kenji Katsumata**, Yokohama (JP); **Yuji Yamamoto**, Yokohama (JP); **Satoshi Iimuro**, Yokohama (JP); **Takanori Eda**, Yokohama (JP); **Shuko Sei**, Yokohama (JP)

(73) Assignee: **Hitachi Consumer Electronics Co., Ltd.**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **12/196,640**

(22) Filed: **Aug. 22, 2008**

(65) **Prior Publication Data**

US 2009/0066856 A1 Mar. 12, 2009

Related U.S. Application Data

(63) Continuation of application No. 11/024,874, filed on Dec. 30, 2004, now Pat. No. 7,436,458, which is a continuation of application No. 10/725,456, filed on Dec. 3, 2003, now Pat. No. 7,173,674, which is a continuation of application No. 10/376,231, filed on Mar. 3, 2003, now abandoned, which is a continuation of application No. 09/135,727, filed on Aug. 18, 1998, now Pat. No. 6,549,243.

(30) **Foreign Application Priority Data**

Aug. 21, 1997 (JP) 9-224605

(51) **Int. Cl.**
H04N 7/01 (2006.01)

(52) **U.S. Cl.** **348/725**

(58) **Field of Classification Search** ..... None
See application file for complete search history.

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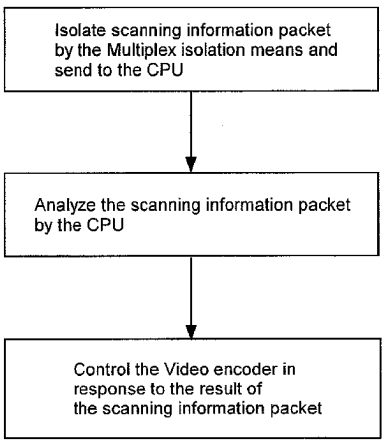
Primary Examiner—Paulos M Natnael
(74) *Attorney, Agent, or Firm*—Antonelli, Terry, Stout & Kraus, LLP.

(57) **ABSTRACT**

A video processing apparatus including: an input device which inputs an encoded video signal; a decoder which decodes the encoded video signal having a video format which is one of a plurality of video formats to produce a decoded video signal; a processor which processes the decoded video signal by using a scanning method information of the decoded video signal, to produce a processed video signal; and an output device which outputs both of the video signal processed by using the scanning method information and scanning method information of the processed video signal, from the video processing apparatus to an external video processing apparatus.

17 Claims, 11 Drawing Sheets



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ISO/IEC 13818-1, MPEG2 Systems, ITU-T Recommendation H.222.0, Jul. 1995.
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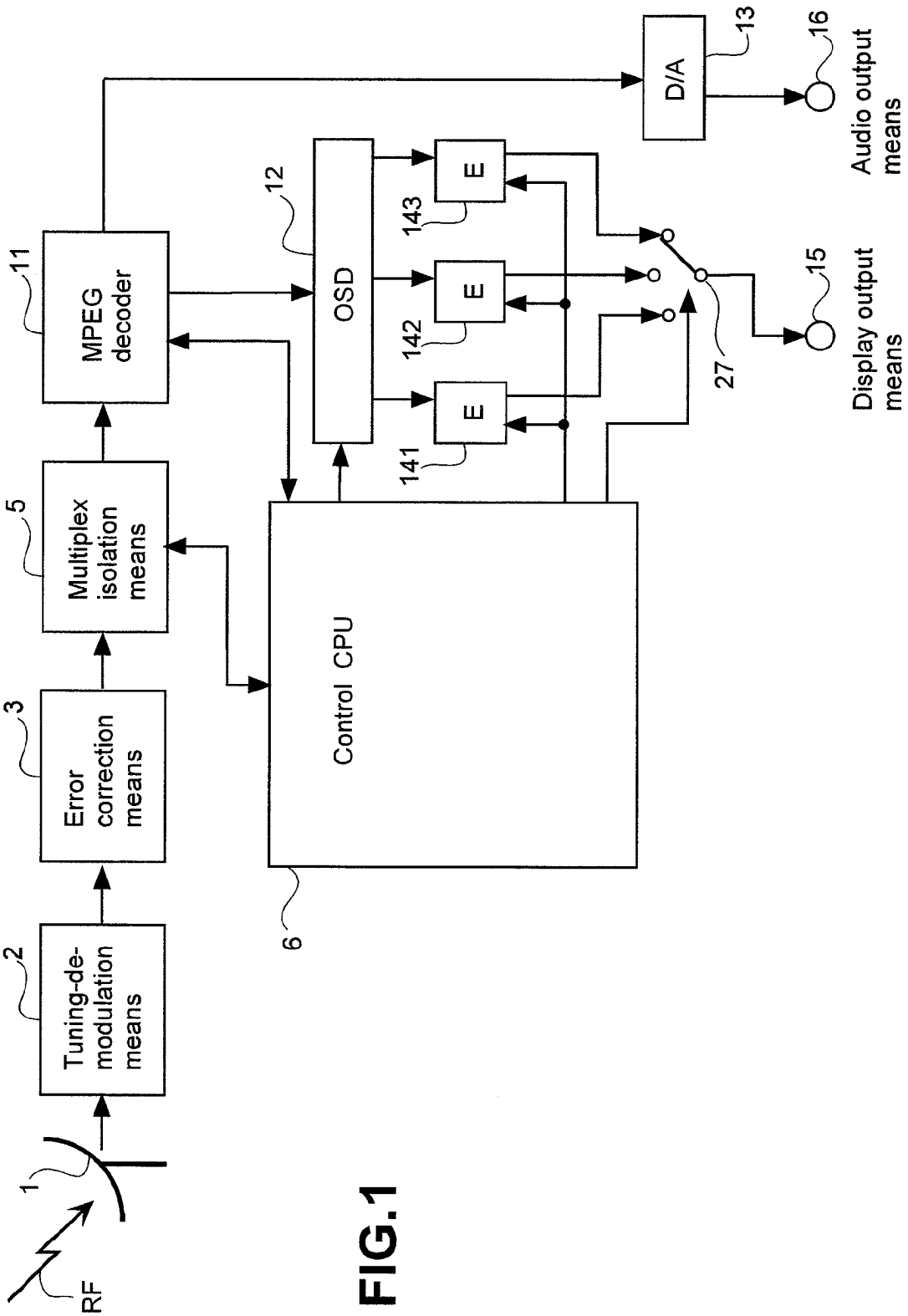

RF
1
Tuning-de-modulation means
2
Error correction means
3
Multiplex isolation means
5
MPEG decoder
11
OSD
12
Control CPU
6
E
143
E
142
E
141
D/A
13
Audio output means
16
Display output means
15
27

FIG.1

FIG.2A

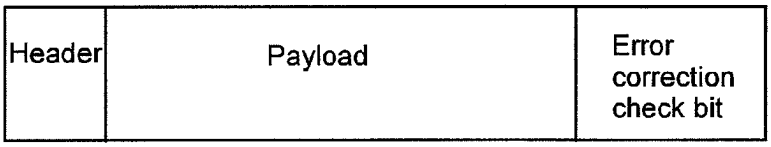


FIG.2B

FIG.2C

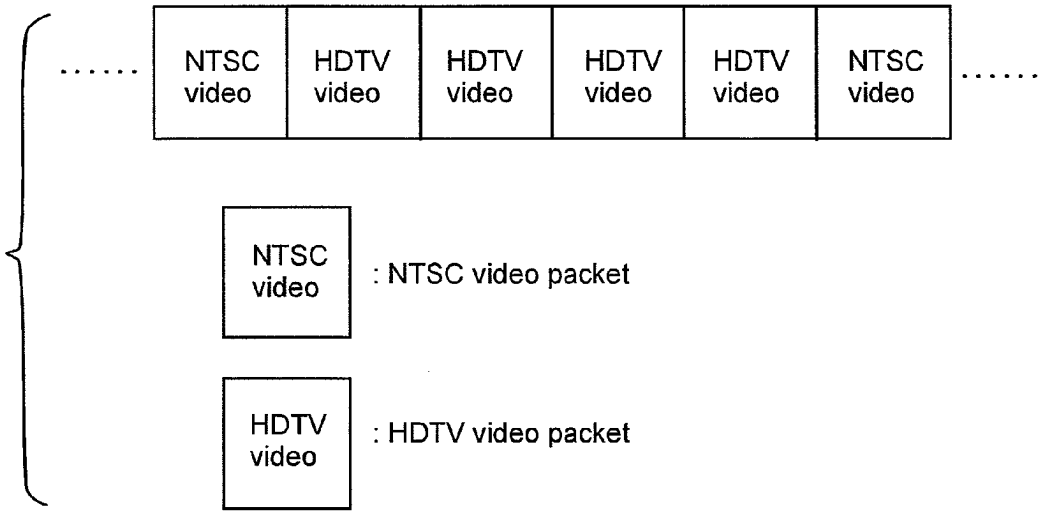


FIG.3

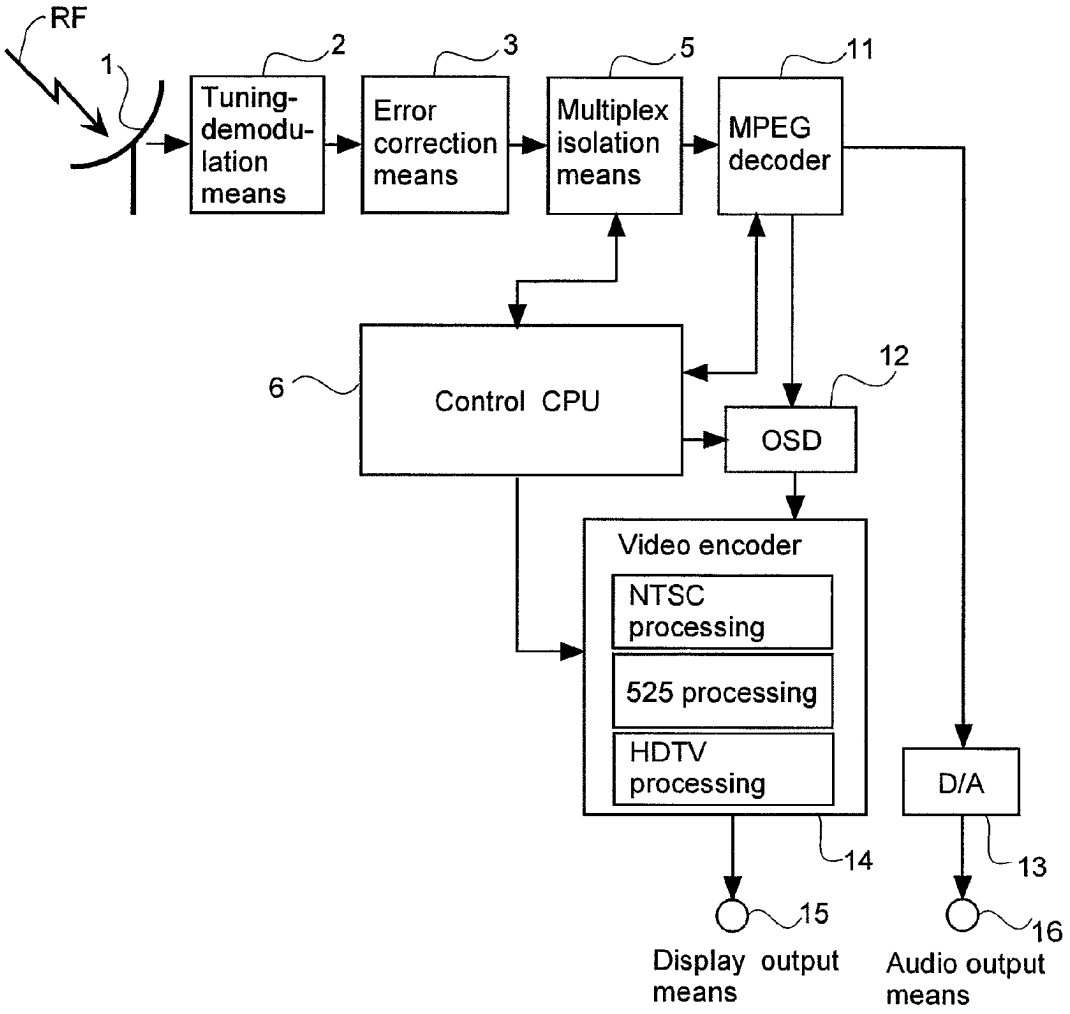


FIG.4A

Header	NTSC video	Error correction check bit	Header	HDTV video	Error correction check bit	Header	Scanning method data	Error correction check bit

FIG.4B

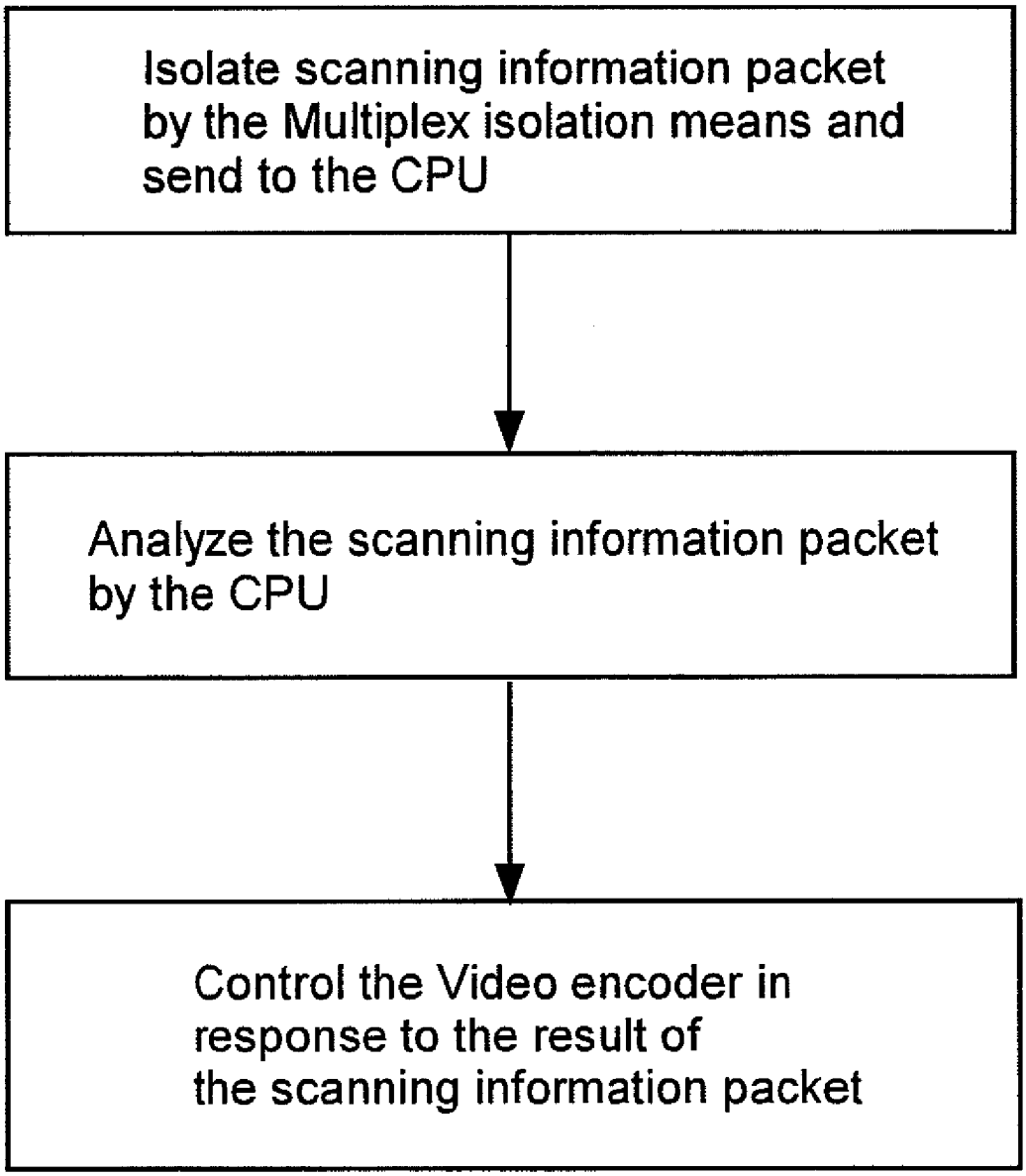

Isolate scanning information packet by the Multiplex isolation means and send to the CPU
Analyze the scanning information packet by the CPU
Control the Video encoder in response to the result of the scanning information packet

FIG.5

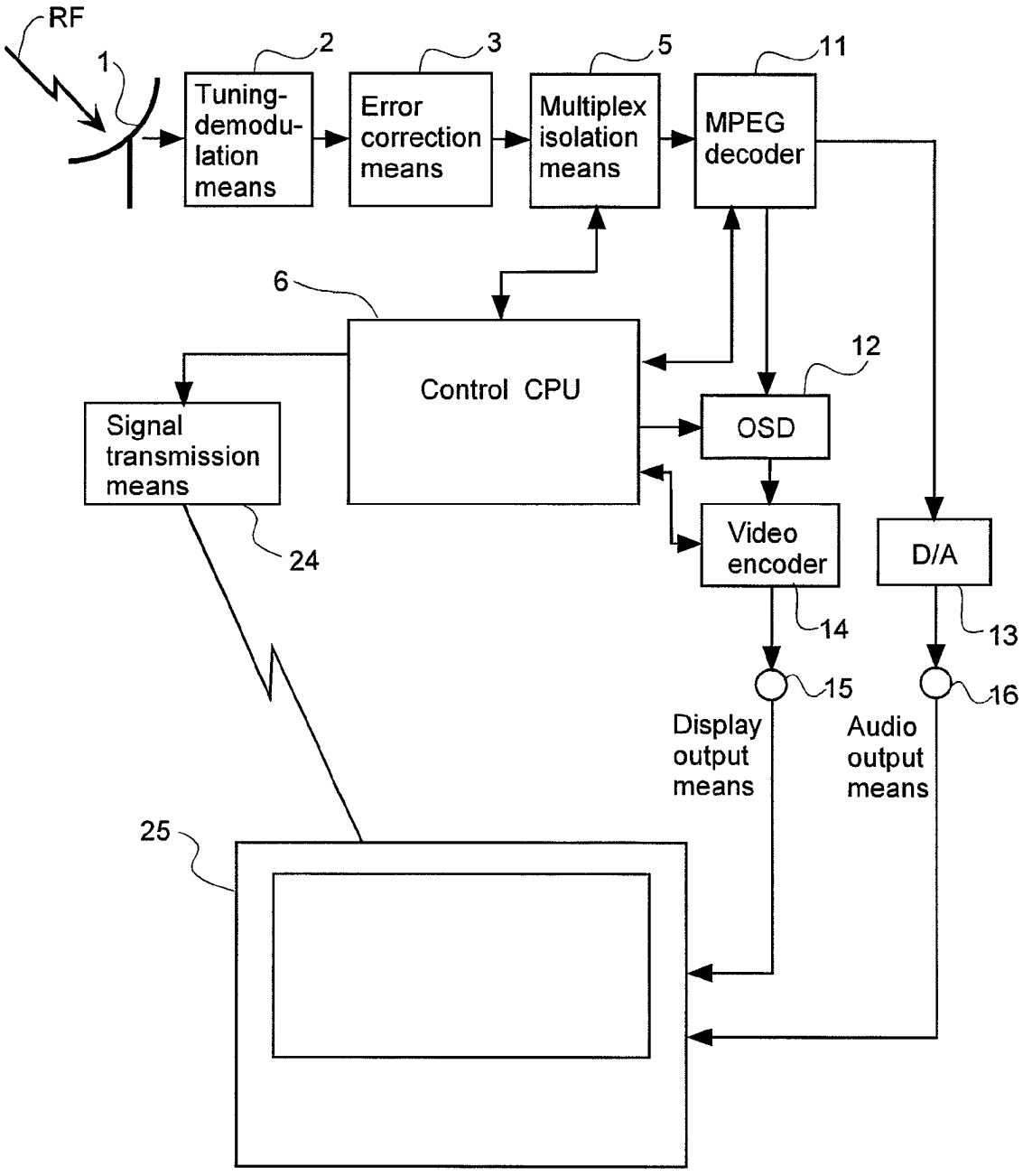

RF
1
2
Tuning-demodulation means
3
Error correction means
5
Multiplex isolation means
11
MPEG decoder
6
Control CPU
12
OSD
Signal transmission means
24
Video encoder
D/A
14
13
15
16
Display output means
Audio output means
25

FIG.6

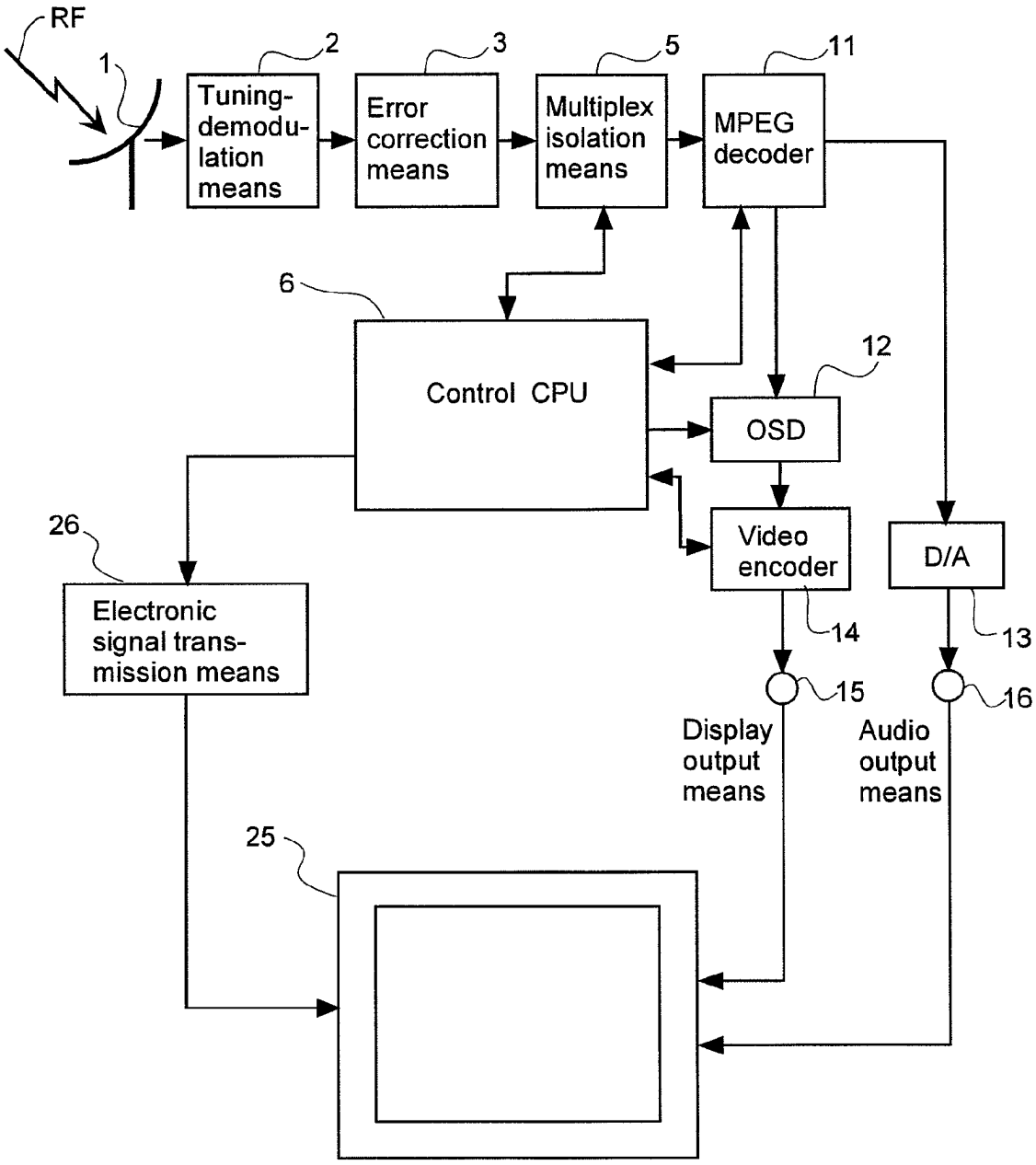

RF
1
2
Tuning-demodu-lation means
3
Error correction means
5
Multiplex isolation means
11
MPEG decoder
6
Control CPU
12
OSD
Video encoder
D/A
26
Electronic signal trans-mission means
14
13
15
16
Display output means
Audio output means
25

FIG.7

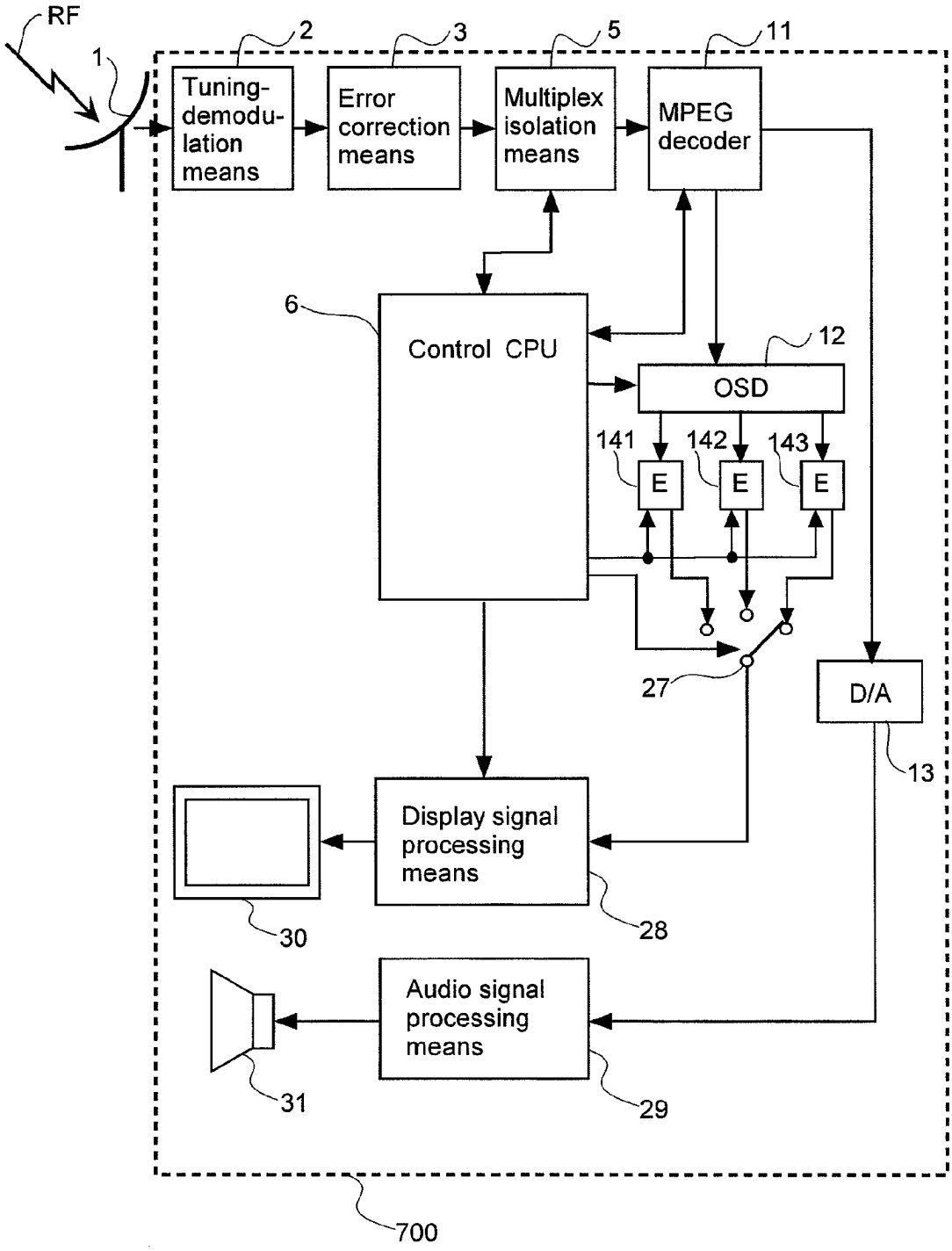

RF
1
2
3
5
11
Tuning-demodulation means
Error correction means
Multiplex isolation means
MPEG decoder
6
Control CPU
12
OSD
141
142
143
E
E
E
27
D/A
13
Display signal processing means
28
30
Audio signal processing means
29
31
700

FIG.8

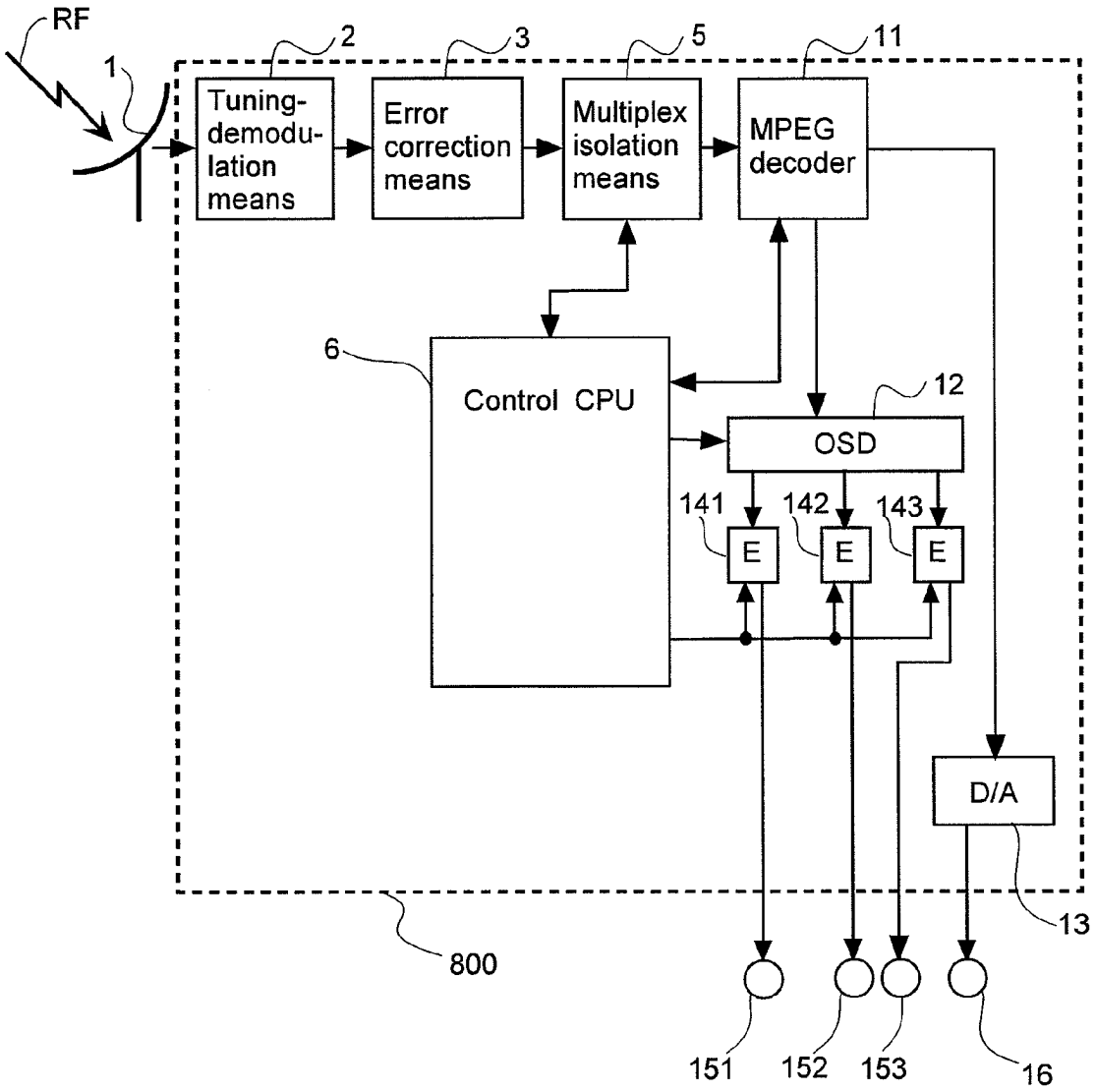

RF
1
2
3
5
11
Tuning-demodulation means
Error correction means
Multiplex isolation means
MPEG decoder
6
Control CPU
12
OSD
141
142
143
E
E
E
D/A
13
800
151
152
153
16

FIG.9

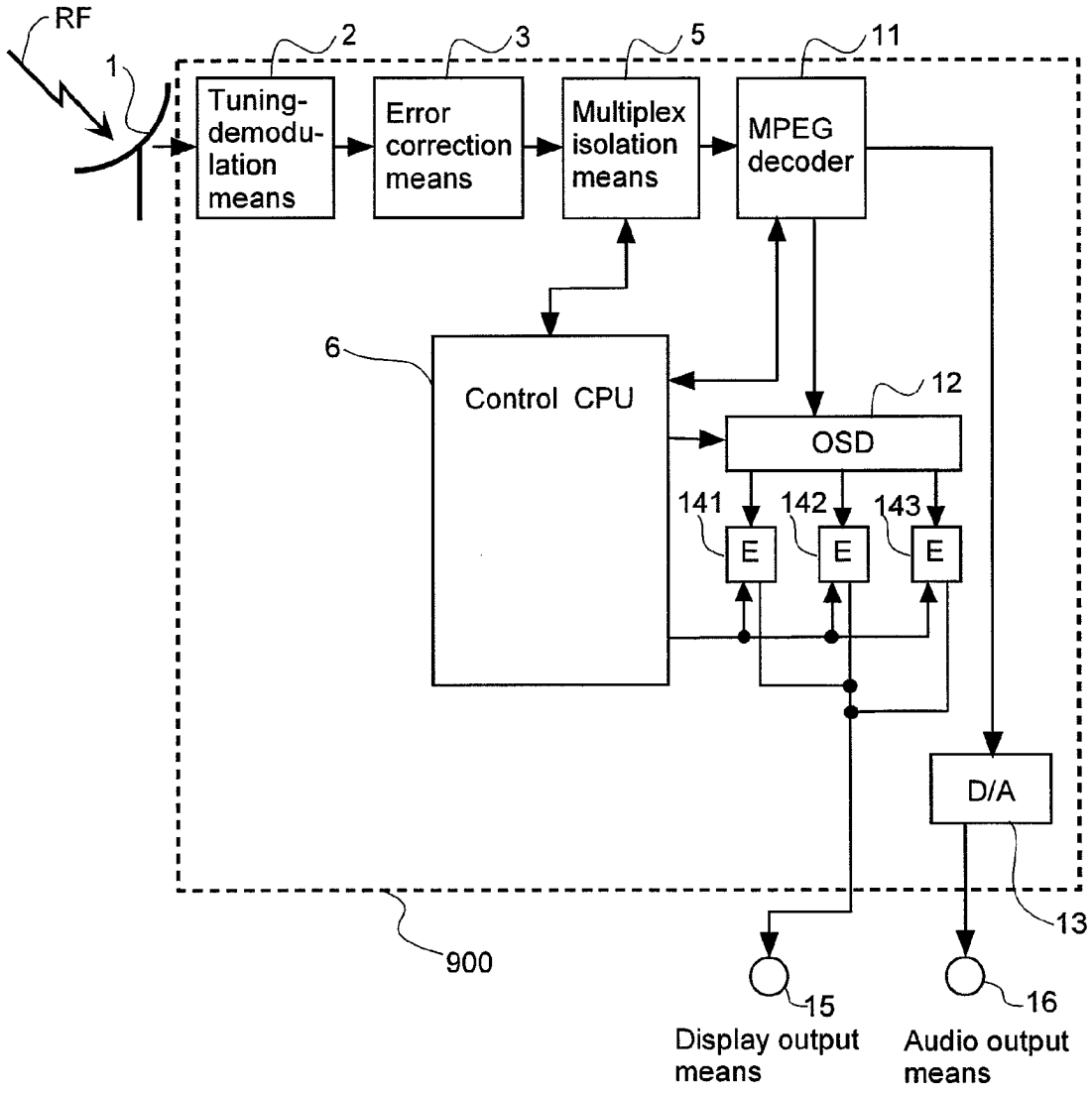

RF
1
2
3
5
11
Tuning-demodulation means
Error correction means
Multiplex isolation means
MPEG decoder
6
Control CPU
12
OSD
141
142
143
E
E
E
D/A
13
900
15
16
Display output means
Audio output means

FIG.10

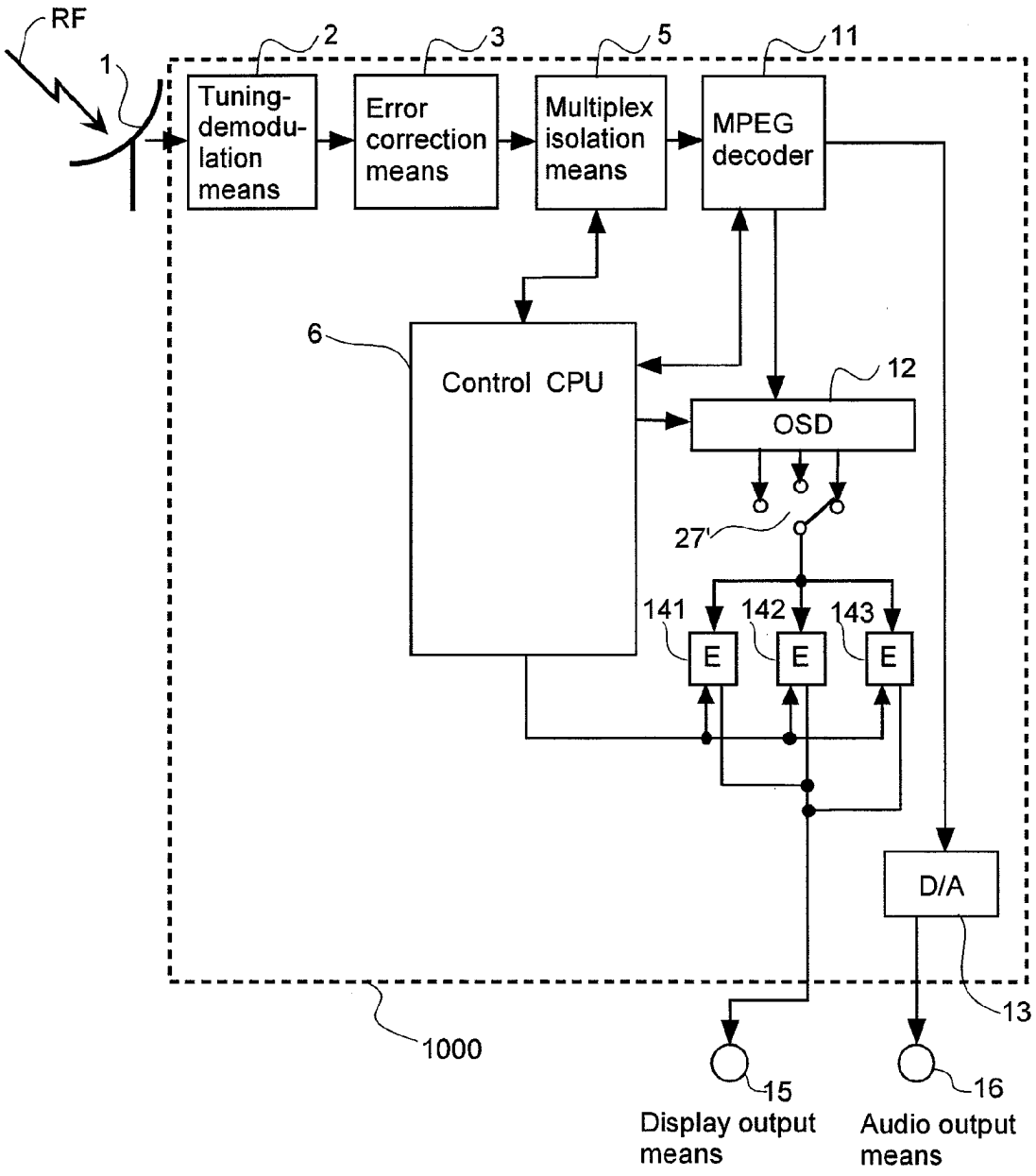
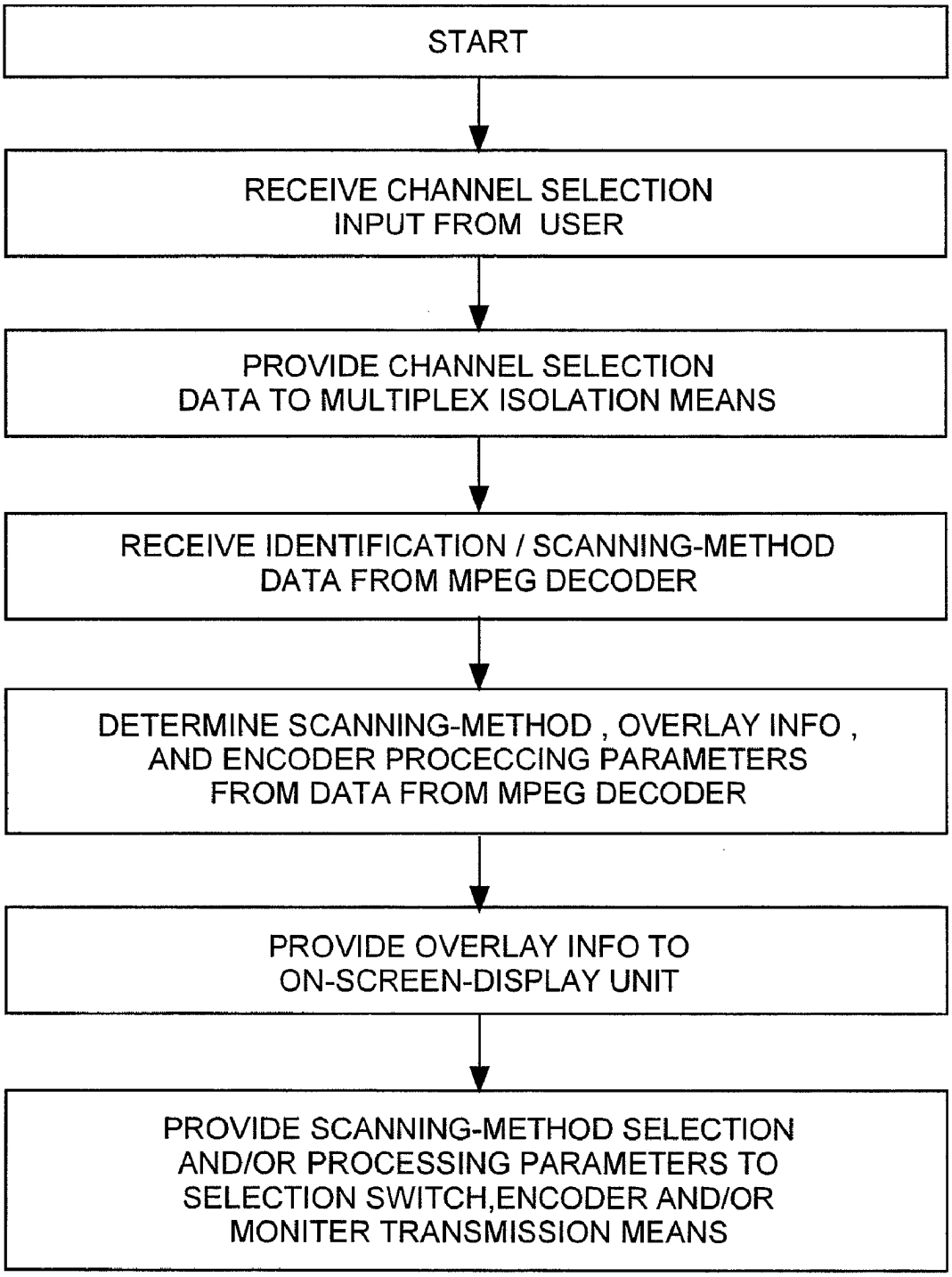

RF
1
2
3
5
11
Tuning-demodulation means
Error correction means
Multiplex isolation means
MPEG decoder
6
Control CPU
12
OSD
27'
141
142
143
E
E
E
D/A
13
1000
15
16
Display output means
Audio output means

FIG.11


START
RECEIVE CHANNEL SELECTION INPUT FROM USER
PROVIDE CHANNEL SELECTION DATA TO MULTIPLEX ISOLATION MEANS
RECEIVE IDENTIFICATION / SCANNING-METHOD DATA FROM MPEG DECODER
DETERMINE SCANNING-METHOD , OVERLAY INFO , AND ENCODER PROCECCING PARAMETERS FROM DATA FROM MPEG DECODER
PROVIDE OVERLAY INFO TO ON-SCREEN-DISPLAY UNIT
PROVIDE SCANNING-METHOD SELECTION AND/OR PROCESSING PARAMETERS TO SELECTION SWITCH,ENCODER AND/OR MONITER TRANSMISSION MEANS

DIGITAL BROADCAST RECEIVER UNIT

CROSS REFERENCE TO RELATED APPLICATION

This is a continuation of U.S. application Ser. No. 11/024,874, filed Dec. 30, 2004 now U.S. Pat. No. 7,436,458, which is a continuation of U.S. application Ser. No. 10/725,456, filed Dec. 3, 2003 (now U.S. Pat. No. 7,173,674), which is a continuation of U.S. application Ser. No. 10/376,231, filed Mar. 3, 2003 (abandoned), which is a continuation of U.S. application Ser. No. 09/135,727, filed Aug. 18, 1998 (now U.S. Pat. No. 6,549,243). This application relates to and claims priority from Japanese Patent Application No. 09-224605, filed on Aug. 21, 1997. The entirety of the contents and subject matter of all of the above is incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a digital broadcast receiver unit, and in particular, relates to a digital broadcast receiver unit capable of receiving, in one stream, multiplex video signals formatted according to a plurality of differing scanning methods.

2. Description of Related Art

In digital transmission technology, in addition to video and audio signals, all kinds of information can be multiplexed and broadcast over one common carrier wave, i.e., multi-channel broadcasts utilizing this technology have already commenced. By utilizing this digital transmission technology, video signals for different scanning methods can be coded, multiplexed (i.e., placed on one common carrier wave) and then broadcast.

In contrast, in related art analog broadcast receivers, television receivers are able to receive transmissions from a plurality of analog broadcast systems. In analog broadcasting, however, different kinds of information cannot be multiplexed (or placed together on the same carrier wave) so that the received video signal itself must be analyzed to determine the scanning method. When receiving different video signals having a plurality of scanning systems in the above mentioned related art analog broadcasts, not only was a custom identification means required to analyze and process the received video signal itself, but in order to identify the video signal, video signal processing circuits had to be operated whose operation was not actually necessary.

In contrast, one important feature of digital broadcasting, however, is that a plurality of information such as audio, video and data can be multiplexed and sent as one transmission stream. Utilizing multiplexed data therefore means that various features can be provided.

SUMMARY OF THE INVENTION

In view of the above problems, it is therefore an object of this invention to provide a digital broadcast receiver for identifying video signal scanning methods utilizing different kinds of multiplexed information, and using such identification for selecting an appropriate scanning method for reproduction.

In order to achieve the above, this invention is directed to a digital broadcast receiver unit for receiving a digital multiplexed signal stream having multiplexed signals commonly encoded using a same encoding/decoding standard, the multiplexed signals including video signals corresponding to a plurality of different video signal formats, and isolating and reproducing at least one video signal, the unit including: a selector to select and extract one video signal from a received the digital multiplexed signal; a decoder to decode the video signal from the selector according to the encoding/decoding standard; a plurality of video processor sections, with respective video processor sections providing video processing according to a different video signal format of the plurality of different video signal formats; and a controller using information from the received the digital multiplexed signal to determine a video signal format of the video signal from the decoder, and selecting one video processor section of the video processor sections to perform video processing of the video signal according to a determined video signal format thereof. More particularly, the present invention determines the scanning method of the video signal of the selected program and then performs the appropriate processing based on the scanning method for the selected video signal.

The foregoing and a better understanding of the present invention will become apparent from the following detailed description of the preferred embodiments and claims when read in connection with the accompanying drawings, all forming a part of the disclosure hereof this invention. While the foregoing and following written and illustrated disclosure focuses on disclosing embodiments of the invention which are considered preferred embodiments, it should be clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

BRIEF DESCRIPTION OF THE DRAWING(S)

The following represents brief descriptions of the drawings, wherein:

FIG. **1** shows a block diagram of the first embodiment of this invention;

FIGS. **2**A-C are drawings showing exemplary configurations of the digital multiplex stream;

FIG. **3** is a block diagram showing the configuration of a second embodiment of this invention;

FIGS. **4**A-B are drawings showing the configuration of a digital multiplex stream, and a flowchart showing scanning information packet processing, respectively;

FIG. **5** is a block diagram showing the configuration of a third embodiment of this invention;

FIG. **6** is a block diagram showing the configuration of a fourth embodiment of this invention;

FIG. **7** is a block diagram showing the configuration of a fifth embodiment of this invention;

FIG. **8** is a block diagram showing the configuration of a sixth embodiment of this invention;

FIG. **9** shows a different block diagram showing of this invention;

FIG. **10** shows an another different block diagram showing of this invention; and

FIG. **11** is a flowchart indicative of exemplary processing operations conducted by an application specific integrated circuit (ASIC) or central processing unit (CPU) with respect to the present invention, e.g., via suitable programming.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS OF THE INVENTION

Before beginning a detailed description of the subject invention, mention of the following is in order. When appro-

priate, like reference numerals and characters are used to designate identical, corresponding or similar components in differing figure drawings.

Hereafter, the embodiment of this inventions will be explained while referring to the accompanying drawings. FIG. **1** is a block diagram showing the structure of the digital broadcast receiver of this invention. An RF carrier wave sent from a communications satellite (not shown) is received at an antenna **1** and then processed by other components. More particularly, in FIG. **1**, the numeral **1** denotes the antenna, the numeral **2** is a tuning-demodulation means, the numeral **3** is an error correction means, the numeral **5** is a multiplex isolation means for treating a multiplexed signal, the numeral **6** is a control CPU, the numeral **11** is an MPEG decoder for decoding the coded audio and video information. Also in FIG. **1**, the numeral **12** is an OSD (On Screen Display) circuit for adding character information to video signals output from the Moving Picture Experts Group (MPEG) decoder **11**, the numeral **13** is a D/A converter for converting digital audio signals into analog signals. Further, in FIG. **1**, the numeral **141** is a video encoder, for instance, to convert **525** interlaced scanning lines of an NTSC system signal into an analog signal and add synchronizing information, etc. The numeral **142** is a video encoder, for instance, to convert **525** scanning lines of a sequential scanning **525** progressive signal (hereafter abbreviated to 525P signal) into an analog signal and add synchronizing information, etc. The numeral **143** is a video encoder, for instance, to convert the 1080 interlaced scanning lines of an HDTV system signal into an analog signal and add synchronizing information, etc. The numeral **15** in the same figure is a video signal output terminal, the numeral **16** is an audio signal output terminal, and the numeral **27** is an output selection means.

The signal received by the antenna **1** is tuned and demodulated by the tuning-demodulation means **2**. The demodulated signal from the tuning-demodulation means **2** is output to the error correction means **3**. Error correction based on the addition of an error correction code is then performed by the error correction means **3**. Next, according to control provided by the CPU **6**, a signal of a program for viewing is demultiplexed (isolated from the other signals) and output by the multiplex isolation means **5**.

The coded audio data and coded video data isolated by the multiplex isolation means **5** is applied to the MPEG decoder **11**. The MPEG decoder **11** decodes the coded data into the digital signal that was present prior to MPEG coding, i.e., according to control provided by the CPU **6**. The digital video signal output from the MPEG decoder **11** is applied to the OSD means **12** which adds character information according to control by the CPU **6**, and is sent to the video encoders **141**, **142** and **143** which each convert the digital video signal into an analog video signal, again, according to control by the CPU **6**. As a parallel operation, the digital audio signal output from the MPEG decoder **11** is applied to the D/A converter **13**, and converted to an analog audio signal. The output from the video encoders **141**, **142** and **143** is applied to the selection means **27**, wherein an appropriate one of the outputs from the video encoders **141**, **142** and **143** is selected via control by the control CPU **6**, and the selected video signal is output. This process allows the analog video signal and analog audio signal sent from the transmitting side to be played back and output in parallel to the video signal output terminal **15** and the audio signal output terminal **16**, respectively.

The operation when processing video signals for different broadcast systems was explained above. FIG. **2**A shows the structure of one unit of the multiplexed signal referred to as a transport stream packet (hereafter TS packet). The TS packet is comprised of a payload for storing data (e.g., video, audio and other info.), a header for indicating data such as identification (e.g., packet number) and/or scanning approach (e.g., NTSC, PAL, etc.) data, and an error correction check bit for performing error correction. As shown in FIG. **2**B, in a digital broadcast, multiplexing of video signals in one stream for a plurality of differing scanning methods can be performed. FIG. **2**C shows (without headers and error correction check bits) a state of a TS packet in the case where an NTSC signal and an HDTV signal are multiplexed as one example. As is apparent from such Fig., video signals of different scanning systems do not have to be alternately or periodically provided, but instead, can be provided in any order.

When the viewer selects the desired program from such signals, e.g., through any know remote or switch arrangement (not shown), the multiplex isolation means **5** responds thereto, and only the coded audio data and the coded video data that comprises the selected program is isolated and output from the multiplex isolation means **5**. The coded video data and coded audio data which is output is applied to the MPEG decoder **11**. The coded video data includes data detailing the scanning method. The MPEG decoder **11** detects the data detailing the scanning method from the input coded data and conveys this data to the control CPU **6**. Based on the information conveyed from the MPEG decoder **11**, and the determination of the present scanning method, the CPU **6** (via suitable software programming) controls the video encoders **141**, **142** and **143**, as well as control of the selection means **27**. Thus, only the video encoder matching the video signal selected from among the video encoders **141**, **142** and **143** is utilized and an analog video signal is output from the selection means **27**.

As explained previously, operation of the video encoders **141**, **142** and **143** based on information on the scanning method detected by the MPEG decoder **11** of this invention and the selection means **27** not only allows processing and output of the signal for the correct scanning method, but also allows shutting off of the power to video encoders not currently needed and to stop their operation so that useless expenditure of unnecessary power and generation of unnecessary heat is prevented. Further, the generation of signal interference is also reduced.

Additionally, although in FIG. **1** there is illustrated a configuration in which a signal having a system corresponding to each of the video encoders **141**, **142** and **143** is inputted, it may also be applicable that signals of all the types of scanning systems are connected in common from the same terminal to the video encoders **141**, **142** and **143** as shown in FIG. **9** (implemented a self-contained unit **900**, e.g., a set-top box), and thereby the controlling CPU **6** controls in such a way that only the circuit coinciding with the scanning system of an input signal in the video encoders **141**, **142** and **143** is operated. In addition, as shown in FIG. **10** (implemented as a self-contained unit **1000**, e.g., set-top box), a signal output terminal of each of the scanning systems is connected to the switch **27'** so that the switch **27'** is controlled by the controlling CPU **6**, whereby an output terminal of the OSD means **12** coinciding with a video scanning system of a selected TV program is selected, and the signal is inputted to the video encoder. Concurrently, only the video encoder corresponding to the inputted video signal may be allowed to operate under the control of the CPU **6**. As described above, either configuration shown in FIGS. **9** and **10** provides an effect similar to that exhibited by the configuration shown in FIG. **1**.

The second embodiment of this invention is next explained while referring to FIG. **3**. Reference numeral **14** in FIG. **3** denotes a video encoder. The embodiment of FIG. **3** differs

from the embodiment of FIG. **1** in that the configuration of the video encoder **14** is a singular circuit, e.g., a sub-processor, etc., which versatilely permits processing of any of the NTSC signals, 525 signals or HDTV signals. More particularly, the video encoder **14** can be provided as a sub-processor or singular application specific-integrated circuit (ASIC) chip, having segregated processing sub-programs or processing areas which can be selectively enabled/disabled to permit processing according to an appropriate scanning method. While the FIG. **1** approach of separately provided encoders has the power saving advantage that unneeded encoders can be powered down, a FIG. **3** software implemented approach has the advantage that the encoder **14** can be easily changed/customized via simple software reprogramming. The control CPU **6** operates the video encoder **14** so as to match the scanning method detected by the MPEG decoder **11** with any of the three previously related processing means based on information conveyed from the MPEG decoder **11**.

More specifically, for instance, video filter parameters which limit the available video band are regulated. In addition, in FIG. **3**, the video encoder **14** may be constructed to have a configuration where a parameter is fixed in such a way that it may be adapted only for a predetermined kind of video signal. Alternatively, the parameter may be constructed to have a configuration that it is not fixed by the video encoder **14** by itself, but an optional value is selected by the controlling CPU **6**. For the configuration when the fixed parameter is selected, it is possible to simplify the control to be carried out by the controlling CPU. In the case of the configuration in which an optional value is selected by the controlling CPU **6**, it is possible to cope with video signals of all known scanning systems. With such an arrangement as above, the video signal inputted to the video encoder **14** is correctly encoded and outputted from the output terminal **15** as an analog video signal. This process allows the signals input to the video encoder **14** to be sent from the output terminal **15** as correctly encoded analog video signals. As explained above, processing of signals for the correct scanning method can be performed since this invention controls the video encoder **14** according to the appropriate scanning method, based on information on the scanning method detected by the MPEG decoder **11**.

The embodiments in FIGS. **1** and **3** showed examples of detection with an MPEG decoder **11** of scanning method data containing coded image data. However, as shown for example in FIG. **4**A, when there is a TS packet holding data showing the scanning method for each video signal in the payload, the data in the TS packet listing the scanning methods can be isolated by means of the above multiplex isolation means **5**, and conveyed to the control CPU **6** for subsequent use in control of the selection means **27** and the video encoder. A flowchart of this process is shown in FIG. **4**B. Even in this case, the results will clearly be the same as when detecting the scanning method with the MPEG decoder **11**.

The third embodiment of this invention is shown in FIG. **5**. The embodiment of FIG. **5** differs from the embodiment of FIG. **1** for instance, in that a signal transmission means **24** is provided for sending a signal to a television receiver, e.g., an infrared signal. This signal transmission means **24** sends an infrared signal derived from information from the MPEG decoder **11**, and such infrared signal contains information indicating the scanning method of the video signal. This arrangement for instance allows the scanning method of the video signal detected by the MPEG decoder **11** to be conveyed to a television receiver **25** having a means to receive the aforementioned infrared signal and also able to handle a plurality of scanning methods (e.g., a multi-sync or multi-scan capable television receiver), when this television receiver **25** is connected to the video signal output terminal **15**. The scanning method of the video signal for the television receiver **25** is therefore switched to match the scanning method output from the video signal output terminal **15** so that a viewer need not provide and/or manually manipulate a separate scanning method switcher.

FIG. **5** showed an example using an infrared signal as a signal transmission means **24**, however this invention is not limited to this method and an RF waveform signal sending means may also be utilized to send an RF carrier wave signal without an infrared signal. A television receiver provided with this RF waveform signal receiving capability and connected to the video signal output terminal **15** will achieve the same effect of the invention.

FIG. **6** shows the fourth embodiment of this invention. The embodiment of FIG. **6** differs from the embodiment of FIG. **5** in that rather than using a wireless signal such as infrared to show the scanning method of the video signal, an electrical signal is instead conveyed by a wire utilizing an electrical or electronic signal transmission means **26**. Using the configuration in FIG. **6** will clearly achieve the same effect of the invention as in the embodiment of FIG. **5**.

A fifth embodiment of the invention is shown in FIG. **7**. The embodiment of FIG. **7** differs from the embodiment of FIG. **1** in that the digital broadcast receiver of this invention is housed in a same cabinet **700** with a display unit, or in other words, this embodiment comprises a television with an internal digital broadcast receiver unit. In FIG. **7**, the reference numeral **28** denotes a display signal processing means, **29** denotes an audio signal processing means, **30** denotes a display means such as a CRT or liquid crystal display panel or a plasma display panel, and **31** denotes an audio signal output means such as a speaker. In FIG. **7**, the display processing means **28** and the display means **30** are configured, for example, so that an NTSC signal, a 525P signal or a HDTV signal can be displayed. Also in FIG. **7**, the control CPU **6** detects the video signal scanning method that was selected, operates the video encoders **141**, **142** and **143** and along with switching the selection means **27**, controls the display processing means **28** and functions to allow processing of video signal scanning method that was detected. This arrangement permits correct processing of the video signal for the program selected by the equipment comprising a television with an internal digital broadcast receiver unit and display of the program by means of the display means **30**.

The sixth embodiment of this invention is shown in FIG. **8** (implemented as a self-contained unit **800**, e.g., set-top box). FIG. **1** shows a configuration in which the selector means **27** selects and issues an output from the video encoders **141**, **142** and **143**. As shown in FIG. **8**, however, the sixth embodiment differs in that the selection means **27** is not used and the output from the video encoders **141**, **142** and **143** are respectively output from separate output terminals **151**, **152** and **153**. Using the configuration in FIG. **8** will clearly achieve the same effect of the invention as in the embodiment of FIG. **1**.

FIG. **11** is a flowchart indicative of exemplary processing operations conducted by the CPU **6** with respect to the present invention, e.g., via suitable programming. Such operations are repetitively performed over time.

In the above explanation, the RF carrier wave received by the antenna **1** was sent from an artificial satellite however needless to say, this invention is also applicable in cases where the RF carrier wave is sent from an antenna installed on a ground device. Further, the above explanation described an example of digital broadcast receiver compatible with the three scanning methods consisting of an NTSC signal, a 525P

signal and an HDTV signal. However the same effect of the invention can be obtained with a configuration in which other video signal scanning methods are handled by a compatible MPEG encoder or video encoder. Further, as technology advances further approaches/methods applicable for use with the present invention will be found.

In the digital broadcast receiver of this invention as explained above therefore, video signals can be correctly played back and output even when a plurality of video signals of different scanning methods are received as multiplexed signals in one stream.

This concludes the description of the preferred embodiments. Although the present invention has been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the spirit and scope of the principles of this invention. More particularly, reasonable variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the foregoing disclosure, the drawings and the appended claims without departing from the spirit of the invention. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.

What is claimed is:

1. A display system comprising:

digital broadcast receiver unit for receiving a digital multiplexed signal stream having digital multiplexed signals encoded using an encoding/decoding standard, the digital multiplexed signals including video signals corresponding to a plurality of different video signal formats, the unit including:

an isolator to isolate one video signal from the digital multiplexed signal;

a decoder to decode the video signal from the isolator according to the encoding/decoding standard;

a processor to execute a plurality of video processing sub-programs, with respective video processing sub-programs providing video processing according to a different video signal format of the plurality of different video signal formats; and

a controller using information obtained from the digital multiplexed signal to determine a video signal format of the video signal decoded by the decoder, and selecting one video processing of the video processing sub-programs to perform video processing of the video signal decoded by the decoder according to the determined video signal format pertaining to a designated number of scanning lines; and

a display apparatus coupleable with the digital broadcast receiver unit, including:

an input unit which inputs both: a processed video signal processed by the decoder according to the determined video signal format pertaining to a the designated number of scanning lines, and the determined video signal format of the processed video signal, which are outputted from the digital broadcast receiver unit,

a display which is able to display signals having any of a plurality of differing designated numbers of scanning lines, and which displays said processed video signal inputted by said input unit,

wherein a scanning method of the video signal for said display is switched to match a scanning method indicated by the determined video signal format inputted by said input unit.

2. A digital broadcast receiver unit for receiving a digital multiplexed signal stream having digital multiplexed signals encoded using an encoding/decoding standard, the digital multiplexed signals including video signals corresponding to a plurality of different video signal formats, the unit comprising:

an isolator to isolate one video signal from the digital multiplexed signal;

a decoder to decode the video signal from the isolator according to the encoding/decoding standard;

a processor to execute a plurality of video processing sub-programs, with respective video processing sub-programs providing video processing according to a different video signal format of the plurality of different video signal formats; and

a controller using information obtained from the digital multiplexed signal to determine a video signal format of the video signal decoded by the decoder, and selecting one video processing of the video processing sub-programs to perform video processing of the video signal decoded by the decoder according to the determined video signal format.

3. A unit as claimed in claim **2**, wherein

the digital multiplexed signal includes a data indicating the video signal format; and

the controller obtains the data from the digital multiplexed signal as the information to determine the video signal format of the video signal.

4. A unit as claimed in claim **2**, wherein

the digital multiplexed signal includes a data indicating the video signal format;

the decoder obtains the data from the digital multiplexed signal; and

the controller obtains the data from the decoder as the information to determine the video signal format of the video signal.

5. A unit as claimed in claim **2**, wherein

the digital multiplexed signal includes a data indicating the video signal format;

the isolator obtains the data from the digital multiplexed signal; and

the controller obtains the data from the isolator as the information to determine the video signal format of the video signal.

6. A digital broadcast receiver unit for receiving a digital multiplexed signal stream having digital multiplexed signals encoded using an encoding/decoding standard, the digital multiplexed signals including video signals corresponding to a plurality of different video signal formats, the unit comprising:

an isolator to isolate one video signal from the digital multiplexed signal;

a decoder to decode the video signal from the isolator according to the encoding/decoding standard;

a processor to execute a plurality of video processing sub-programs, with respective video processing sub-programs providing video processing according to a different video signal format of the plurality of different video signal formats;

a controller using information obtained from the digital multiplexed signal to determine a video signal format of the video signal decoded by the decoder, and selecting one video processing of the video processing sub-programs to perform video processing of the video signal decoded by the decoder according to the determined video signal format; and

a display to display the video signal processed by the processor.

7. A unit as claimed in claim **6**, wherein

the digital multiplexed signal includes a data indicating the video signal format; and

the controller obtains the data from the digital multiplexed signal as the information to determine the video signal format of the video signal.

8. A unit as claimed in claim **6**, wherein

the digital multiplexed signal includes a data indicating the video signal format;

the decoder obtains the data from the digital multiplexed signal; and

the controller obtains the data from the decoder as the information to determine the video signal format of the video signal.

9. A unit as claimed in claim **6**, wherein

the digital multiplexed signal includes a data indicating the video signal format;

the isolator obtains the data from the digital multiplexed signal; and

the controller obtains the data from the isolator as the information to determine the video signal format of the video signal.

10. A digital broadcast receiver unit for receiving a digital multiplexed signal stream having digital multiplexed signals encoded using an encoding/decoding standard, the digital multiplexed signals including video signals corresponding to a plurality of different video signal formats, the unit comprising:

an isolator to isolate one video signal from the digital multiplexed signal;

a decoder to decode the video signal from the isolator according to the encoding/decoding standard;

a plurality of video processor sections, with respective video processor sections providing video processing according to a different video signal format of the plurality of different video signal formats; and

a controller using information obtained from the digital multiplexed signal to determine a video signal format of the video signal decoded by the decoder, and selecting one video processor section of the video processor sections to perform video processing of the video signal decoded by the decoder according to the determined video signal format.

11. A unit as claimed in claim **10**, wherein

the digital multiplexed signal includes a data indicating the video signal format; and

the controller obtains the data from the digital multiplexed signal as the information to determine the video signal format of the video signal.

12. A unit as claimed in claim **10**, wherein

the digital multiplexed signal includes a data indicating the video signal format;

the decoder obtains the data from the digital multiplexed signal; and

the controller obtains the data from the decoder as the information to determine the video signal format of the video signal.

13. A unit as claimed in claim **10**, wherein

the digital multiplexed signal includes a data indicating the video signal format;

the isolator obtains the data from the digital multiplexed signal; and

the controller obtains the data from the isolator as the information to determine the video signal format of the video signal.

14. A digital broadcast receiver unit for receiving a digital multiplexed signal stream having digital multiplexed signals encoded using an encoding/decoding standard, the digital multiplexed signals including video signals corresponding to a plurality of different video signal formats, the unit comprising:

an isolator to isolate one video signal from the digital multiplexed signal;

a decoder to decode the video signal from the isolator according to the encoding/decoding standard;

a plurality of video processor sections, with respective video processor sections providing video processing according to a different video signal format of the plurality of different video signal formats;

a controller using information obtained from the digital multiplexed signal to determine a video signal format of the video signal decoded by the decoder, and selecting one video processor section of the video processor sections to perform video processing of the video signal decoded by the decoder according to the determined video signal format; and

a display to display the video signal processed by the processor.

15. A unit as claimed in claim **14**, wherein

the digital multiplexed signal includes a data indicating the video signal format; and

the controller obtains the data from the digital multiplexed signal as the information to determine the video signal format of the video signal.

16. A unit as claimed in claim **14**, wherein

the digital multiplexed signal includes a data indicating the video signal format;

the decoder obtains the data from the digital multiplexed signal; and

the controller obtains the data from the decoder as the information to determine the video signal format of the video signal.

17. A unit as claimed in claim **14**, wherein

the digital multiplexed signal includes a data indicating the video signal format;

the isolator obtains the data from the digital multiplexed signal; and

the controller obtains the data from the isolator as the information to determine the video signal format of the video signal.

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EXHIBIT J

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(12) **United States Patent**
Arai et al.

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(54) **APPARATUS AND METHOD FOR RECEIVING AND RECORDING DIGITAL INFORMATION**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 1187 days.

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Related U.S. Application Data

(60) Continuation of application No. 10/404,452, filed on Apr. 2, 2003, now Pat. No. 7,012,769, which is a continuation of application No. 10/277,830, filed on Oct. 23, 2002, now Pat. No. 6,590,726, which is a continuation of application No. 09/809,047, filed on Mar. 16, 2001, now Pat. No. 6,498,691, which is a continuation of application No. 09/654,962, filed on Sep. 5, 2000, now Pat. No. 6,324,025, which is a continuation of application No. 09/567,005, filed on May 9, 2000, now Pat. No. 6,278,564, which is a continuation of application No. 09/326,595, filed on Jun. 7, 1999, now Pat. No. 6,069,757, which is a continuation of application No. 09/188,303, filed on Nov. 10, 1998, now Pat. No. 6,002,536, which is a continuation of application No. 08/917,176, filed on Aug. 25, 1997, now Pat. No. 5,862,004, which is a continuation of application No. 08/620,879, filed on Mar. 22, 1996, now Pat. No. 5,699,203, which is a continuation of application No. 08/457,597, filed on Jun. 1, 1995, now Pat. No. 5,530,598, which is a continuation of application No. 08/457,486, filed on Jun. 1, 1995, now Pat. No. 5,517,368, which is a continuation of application No. 08/238,528, filed on May 5, 1994, now Pat. No. 5,671,095, which is a division of application No. 07/727,059, filed on Jul. 8, 1991, now Pat. No. 5,337,199.

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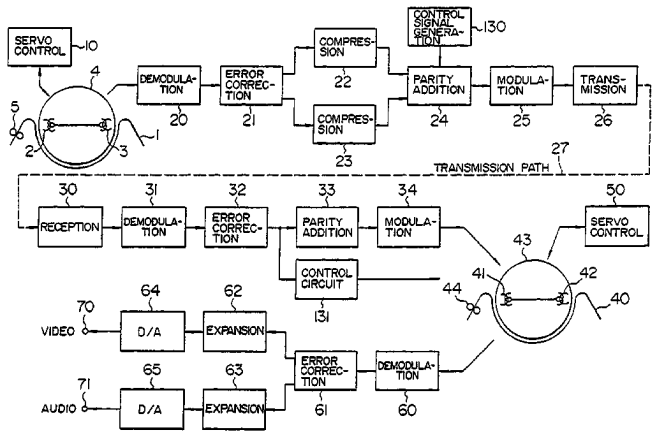
(74) *Attorney, Agent, or Firm* — Antonelli, Terry, Stout & Kraus, LLP.

(57) **ABSTRACT**

A digital information receiving apparatus and method in which a receiver receives a digital signal including a video signal and an audio signal, wherein the received video signal is bit-compressed by a first compression method and the received audio signal is bit-expanded by a second compression method which is different from the first compression method, a demodulator demodulates the received digital signal, and an expander bit-expands the demodulated digital signal.

32 Claims, 18 Drawing Sheets



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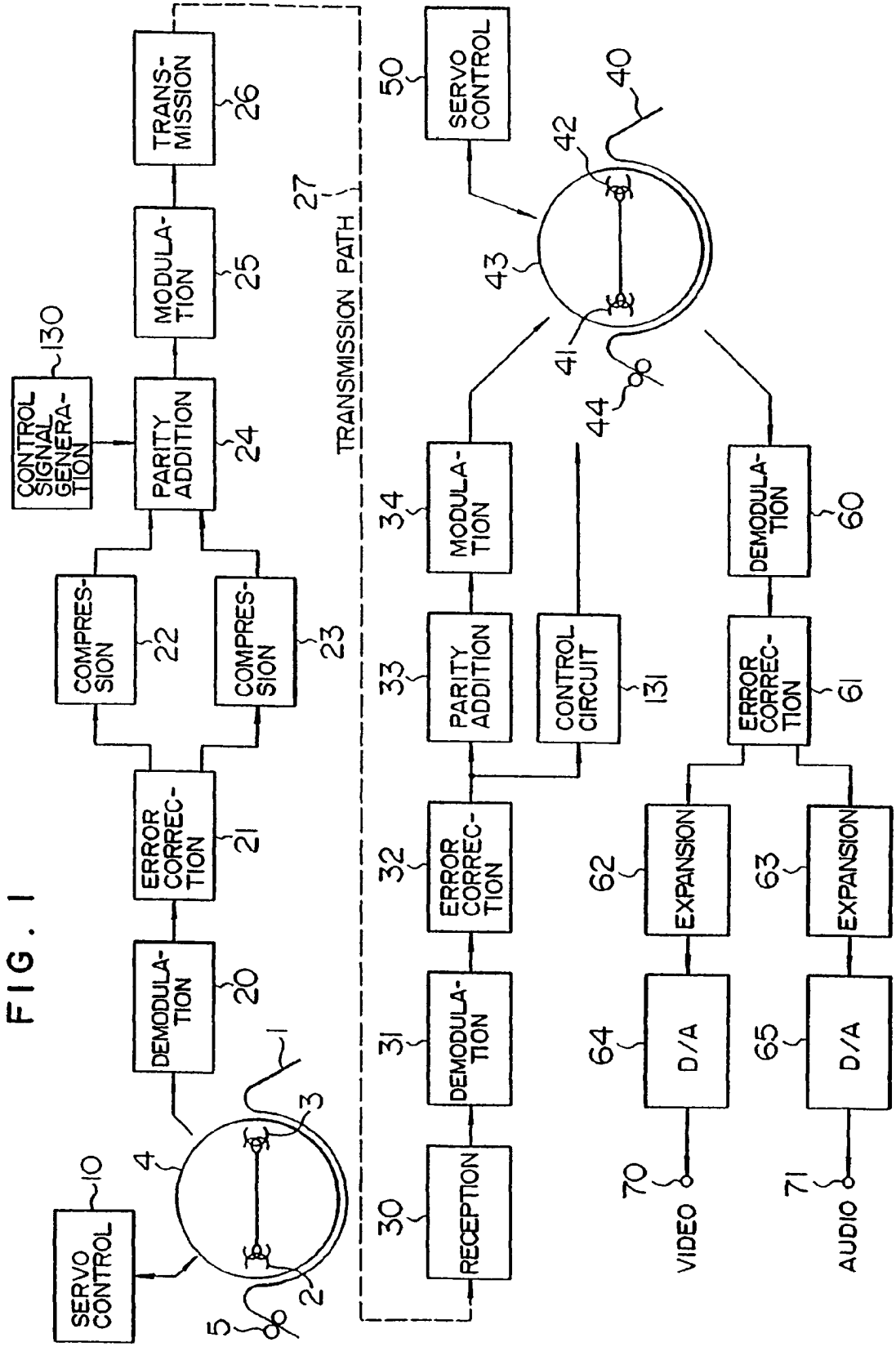
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10
DEMODULATION
20
ERROR CORRECTION
21
COMPRESSION
22
COMPRESSION
23
PARITY ADDITION
24
MODULATION
25
TRANSMISSION
26
CONTROL SIGNAL GENERATION
130
TRANSMISSION PATH
27
RECEPTION
30
DEMODULATION
31
ERROR CORRECTION
32
PARITY ADDITION
33
MODULATION
34
CONTROL CIRCUIT
131
SERVO CONTROL
50
DEMODULATION
60
ERROR CORRECTION
61
EXPANSION
62
EXPANSION
63
D/A
64
D/A
65
VIDEO
70
AUDIO
71
1
2
3
4
5
40
41
42
43
44

FIG. 1

FIG. 2

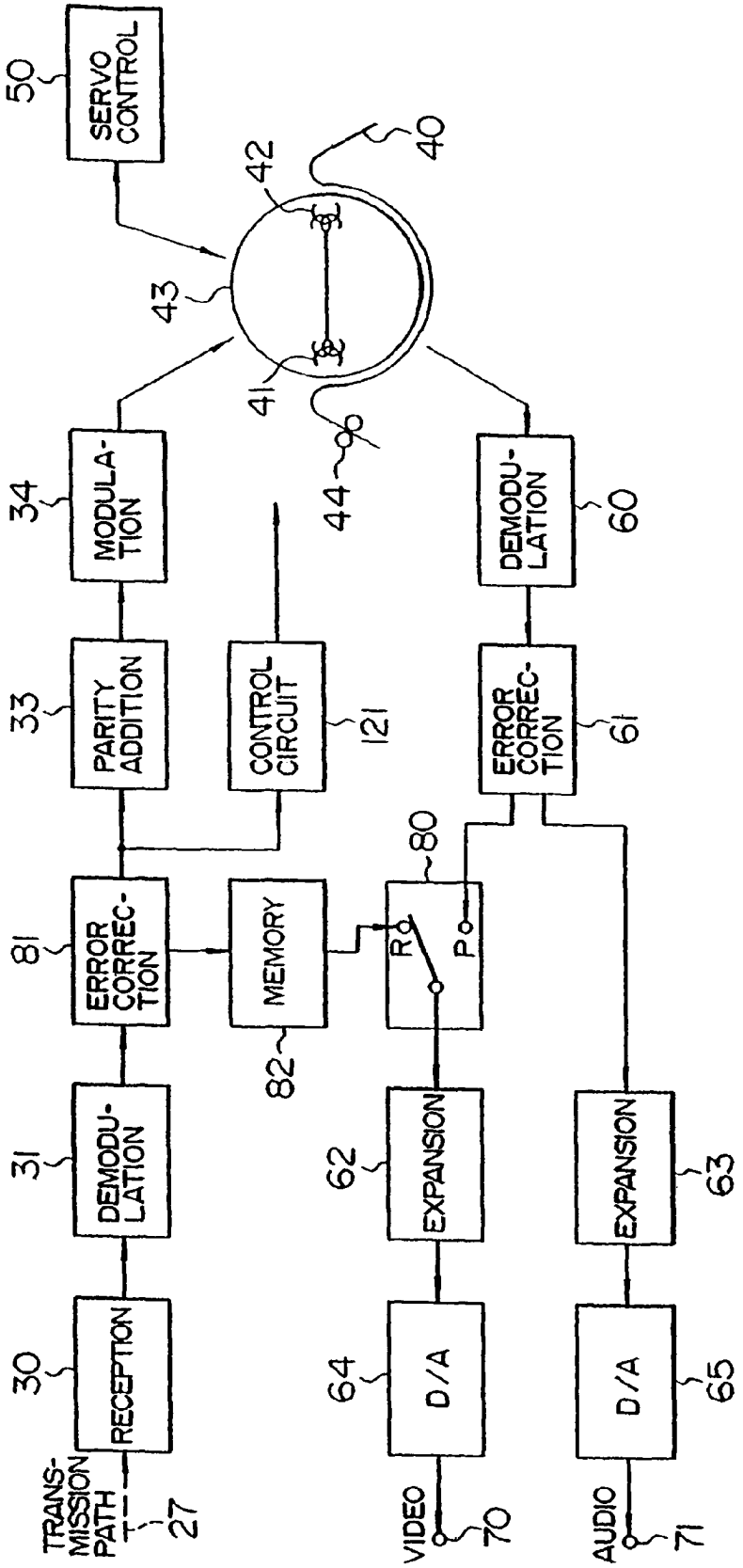

50
SERVO CONTROL
42
40
43
41
44
34
MODULATION
60
DEMODULATION
33
PARITY ADDITION
CONTROL CIRCUIT
121
ERROR CORRECTION
61
80
81
ERROR CORRECTION
MEMORY
R
P
82
31
DEMODULATION
62
EXPANSION
63
EXPANSION
30
RECEPTION
64
D/A
65
D/A
TRANSMISSION PATH
27
VIDEO
70
AUDIO
71

FIG. 3

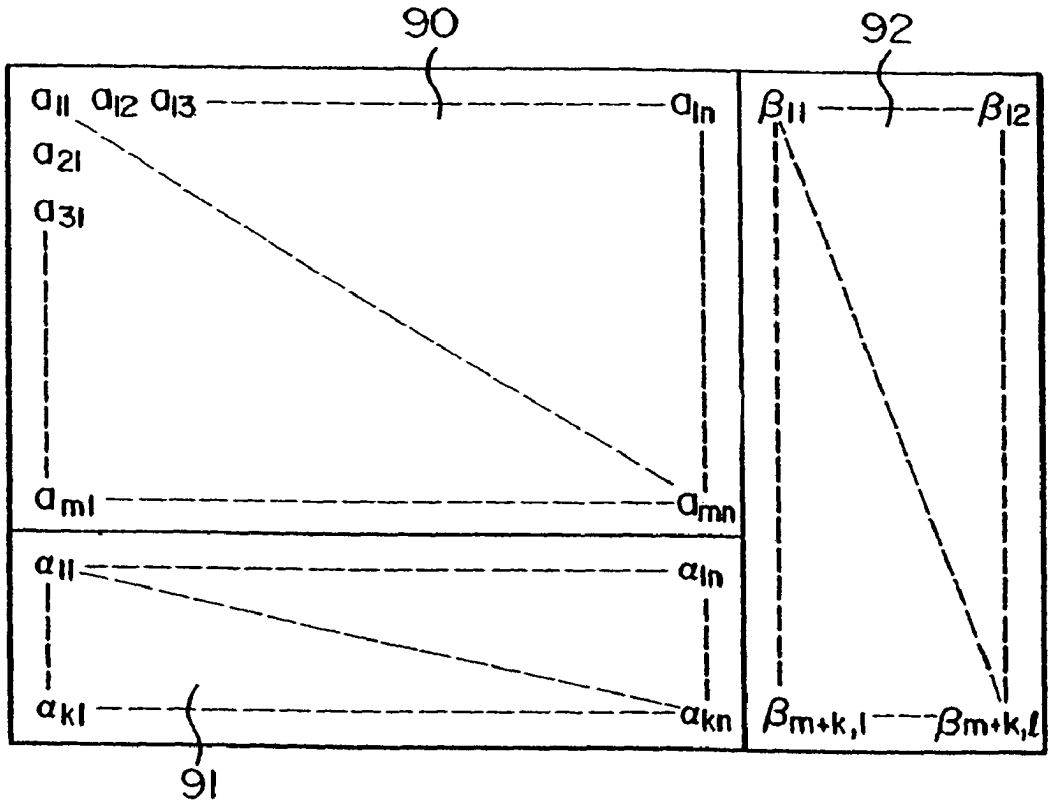
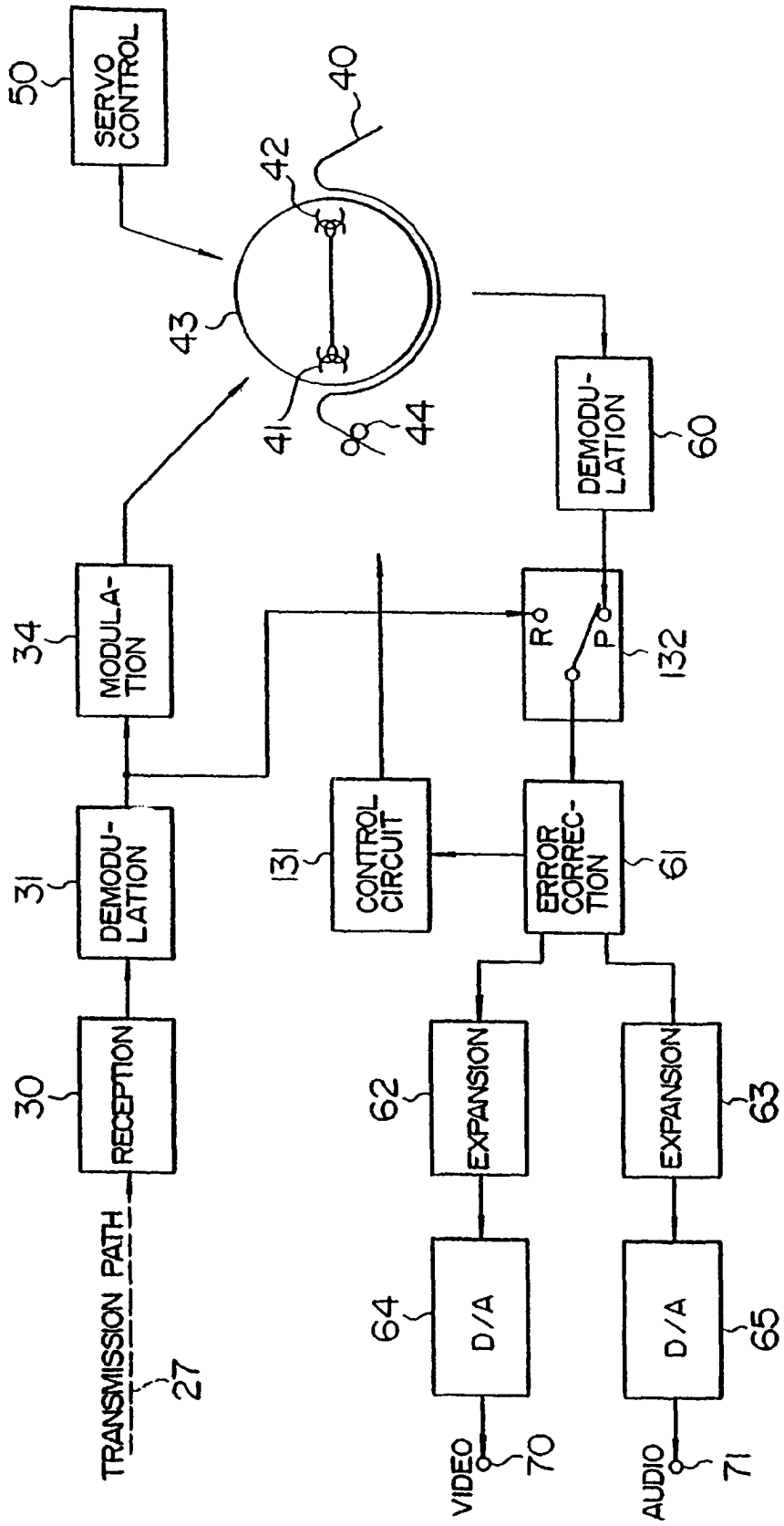

90
92
a_{11} a_{12} a_{13}
a_{1n}
a_{21}
a_{31}
a_{m1}
a_{mn}
β_{11}
β_{12}
α_{11}
α_{1n}
α_{k1}
α_{kn}
$\beta_{m+k,1}$
$\beta_{m+k,l}$
91

FIG. 4


50
SERVO CONTROL
40
42
43
41
44
DEMODU-LATION
60
34
MODULA-TION
R
P
132
31
DEMODU-LATION
131
CONTROL CIRCUIT
ERROR CORREC-TION
61
30
RECEPTION
62
EXPANSION
63
EXPANSION
TRANSMISSION PATH
27
64
D/A
65
D/A
VIDEO
70
AUDIO
71

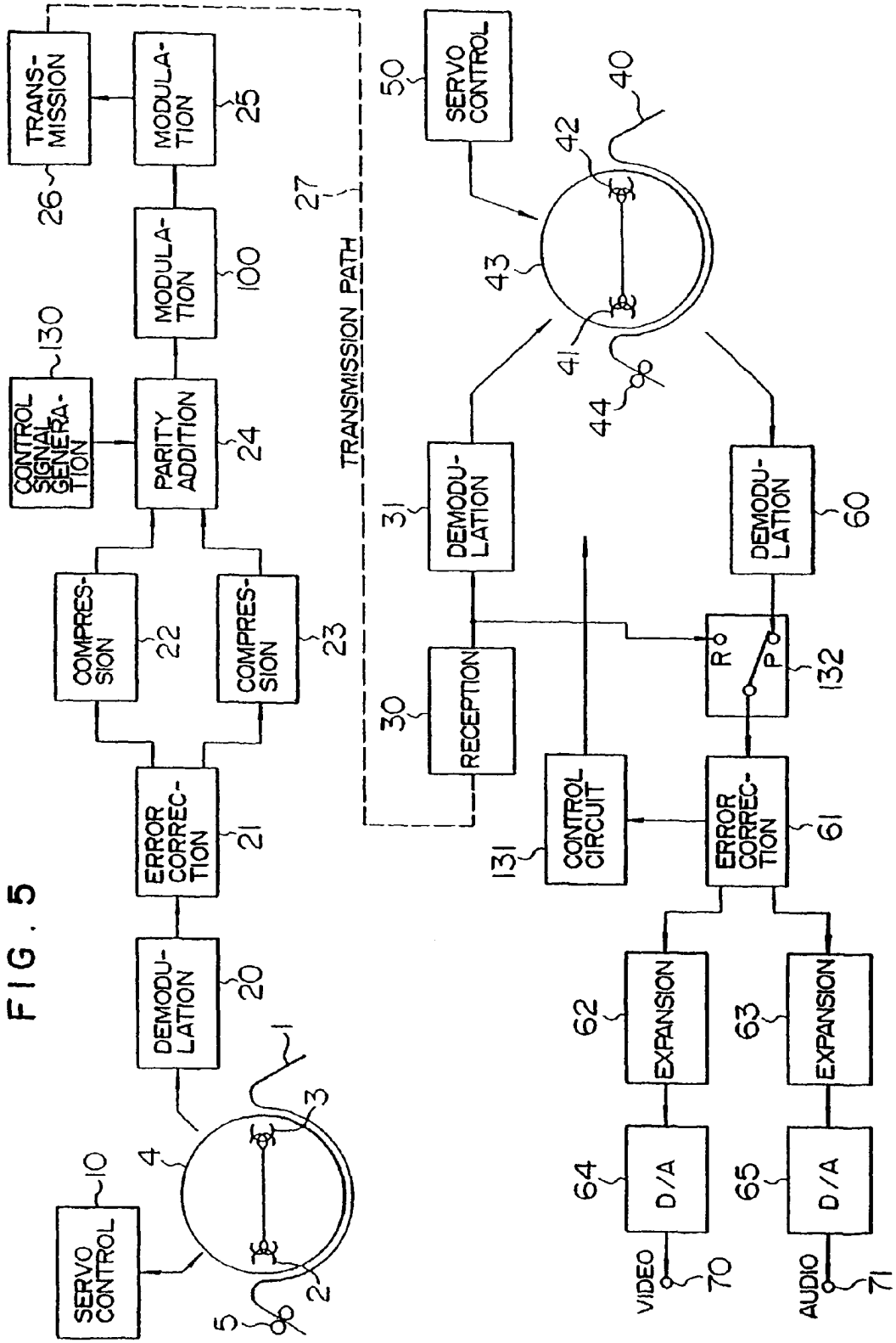

TRANS-MISSION
26
MODULA-TION
25
27
TRANSMISSION PATH
SERVO CONTROL
50
40
42
43
41
44
MODULA-TION
100
130
CONTROL SIGNAL GENERA-TION
PARITY ADDITION
24
DEMODU-LATION
31
DEMODU-LATION
60
COMPRES-SION
22
COMPRES-SION
23
RECEPTION
30
R
P
132
ERROR CORREC-TION
21
CONTROL CIRCUIT
131
ERROR CORREC-TION
61
DEMODU-LATION
20
1
3
4
2
5
SERVO CONTROL
10
62
EXPANSION
63
EXPANSION
64
D/A
65
D/A
VIDEO
70
AUDIO
71

FIG. 5

FIG. 6

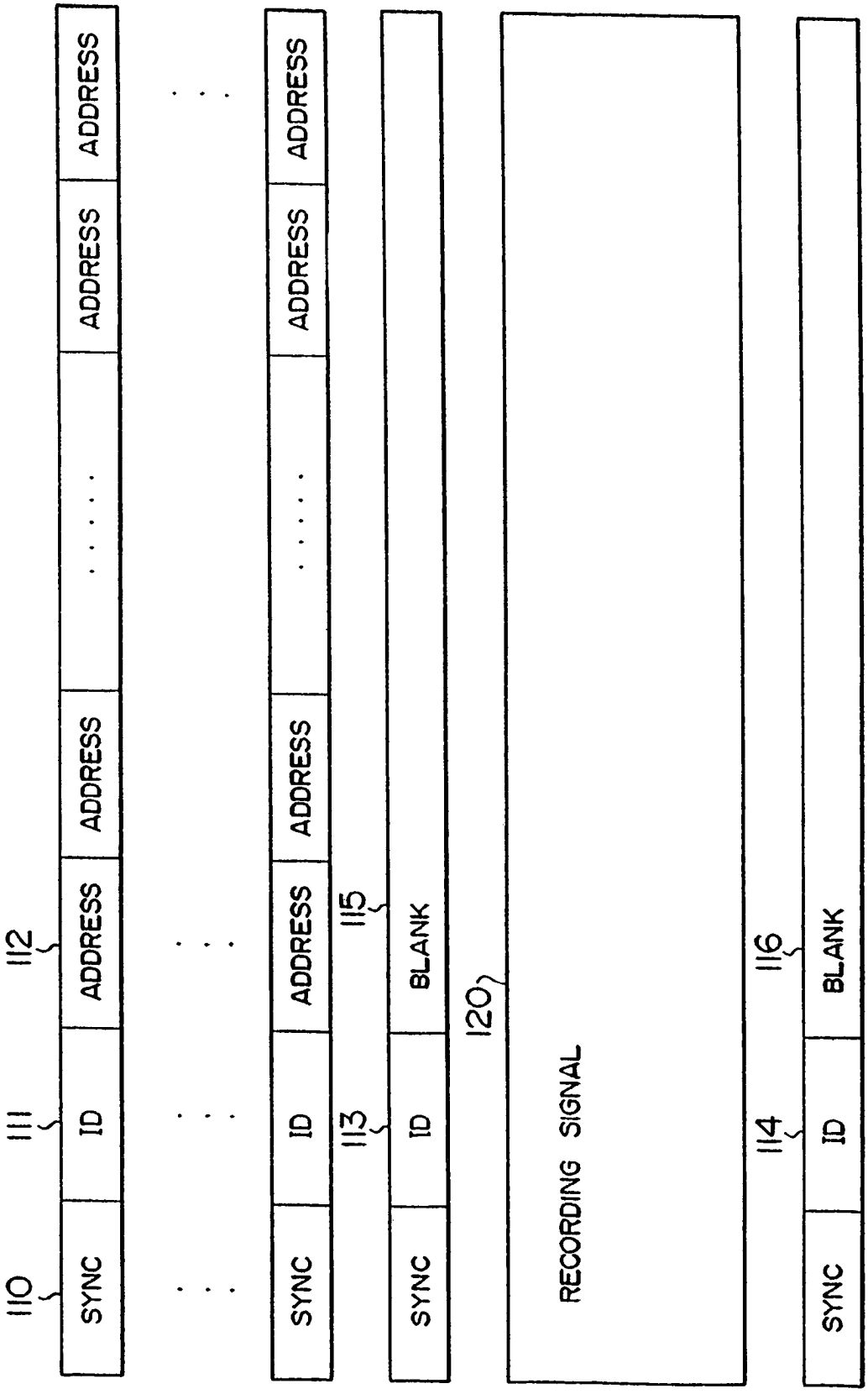

110
111
112
113
115
116
120
SYNC
ID
ADDRESS
BLANK
RECORDING SIGNAL

FIG. 7

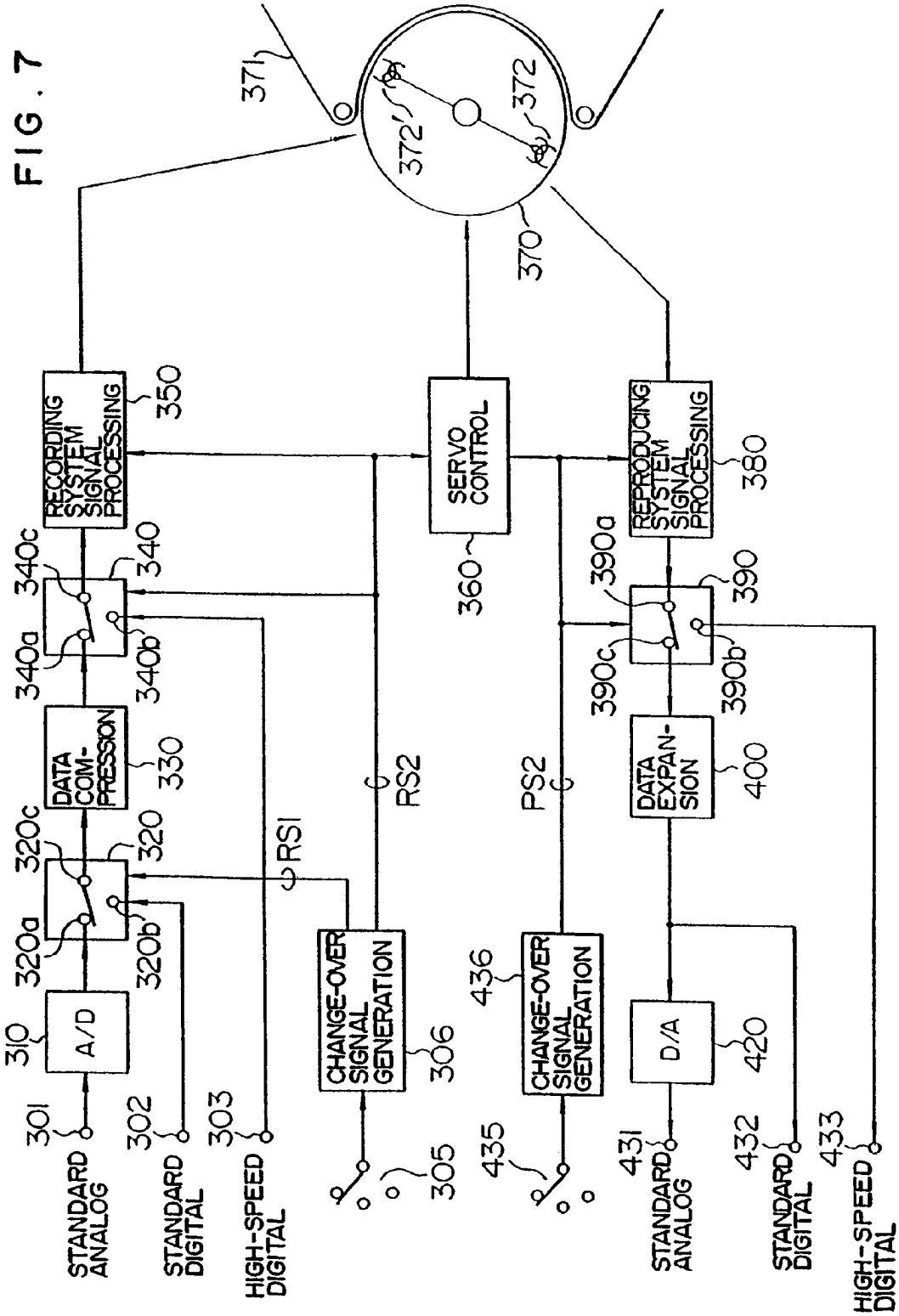

371
372
372
370
RECORDING SYSTEM SIGNAL PROCESSING
350
SERVO CONTROL
360
REPRODUCING SYSTEM SIGNAL PROCESSING
380
340c
340
340a
340b
390a
390
390c
390b
DATA COM-PRESSION
330
DATA EXPAN-SION
400
320c
320
320a
320b
RS1
RS2
PS2
310
A/D
CHANGE-OVER SIGNAL GENERATION
306
436
CHANGE-OVER SIGNAL GENERATION
D/A
420
301
302
303
305
435
431
432
433
STANDARD ANALOG
STANDARD DIGITAL
HIGH-SPEED DIGITAL
STANDARD ANALOG
STANDARD DIGITAL
HIGH-SPEED DIGITAL

FIG. 8

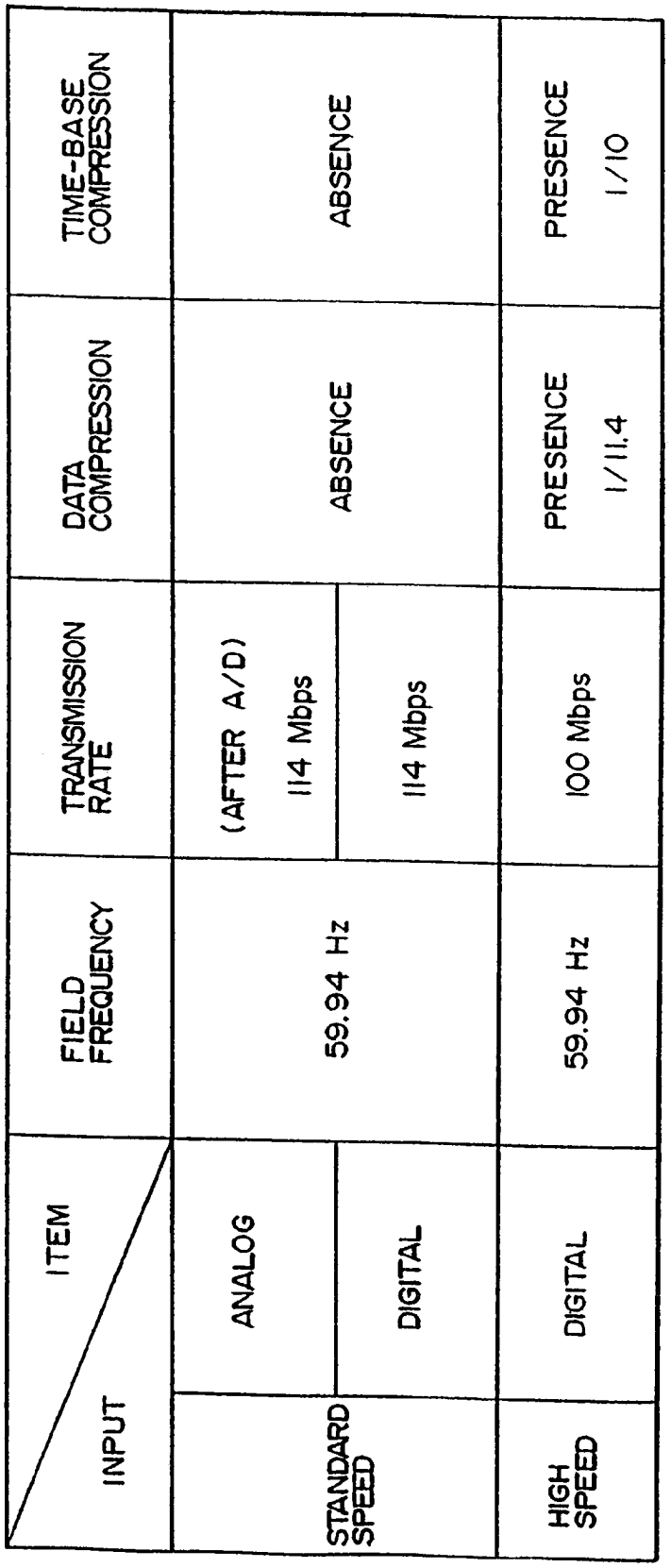

ITEM
INPUT
FIELD FREQUENCY
TRANSMISSION RATE
DATA COMPRESSION
TIME-BASE COMPRESSION
STANDARD SPEED
ANALOG
(AFTER A/D)
114 Mbps
ABSENCE
ABSENCE
DIGITAL
114 Mbps
59.94 Hz
HIGH SPEED
DIGITAL
100 Mbps
59.94 Hz
PRESENCE
1/11.4
PRESENCE
1/10

FIG. 9

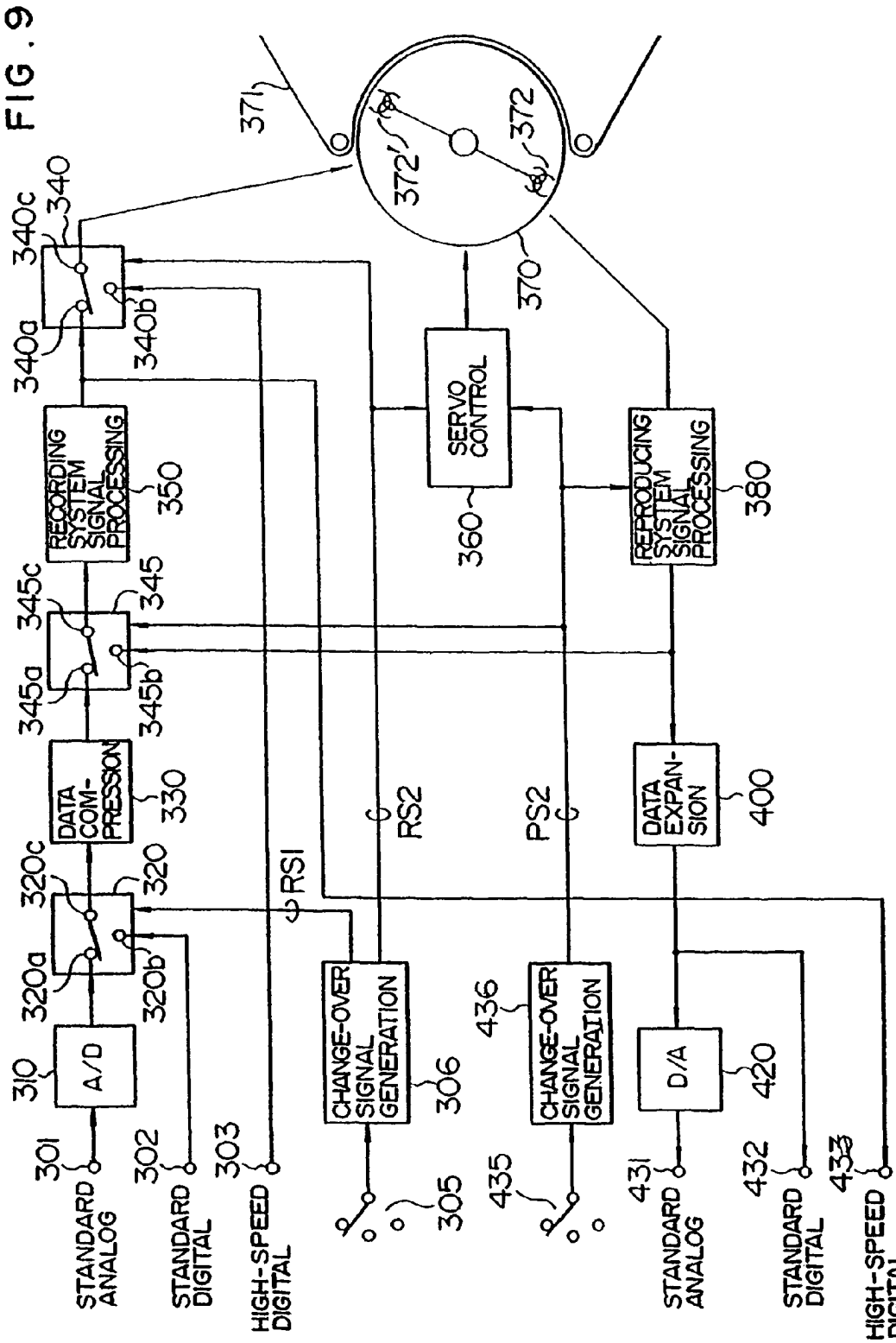

371
372
372
370
340
340c
340a
340b
SERVO CONTROL
360
RECORDING SYSTEM SIGNAL PROCESSING
350
REPRODUCING SYSTEM SIGNAL PROCESSING
380
345
345c
345a
345b
DATA COM-PRESSION
330
DATA EXPAN-SION
400
320
320c
320a
320b
RS1
RS2
PS2
A/D
310
CHANGE-OVER SIGNAL GENERATION
306
436
CHANGE-OVER SIGNAL GENERATION
D/A
420
301
302
303
305
435
431
432
433
STANDARD ANALOG
STANDARD DIGITAL
HIGH-SPEED DIGITAL
STANDARD ANALOG
STANDARD DIGITAL
HIGH-SPEED DIGITAL

FIG. 10

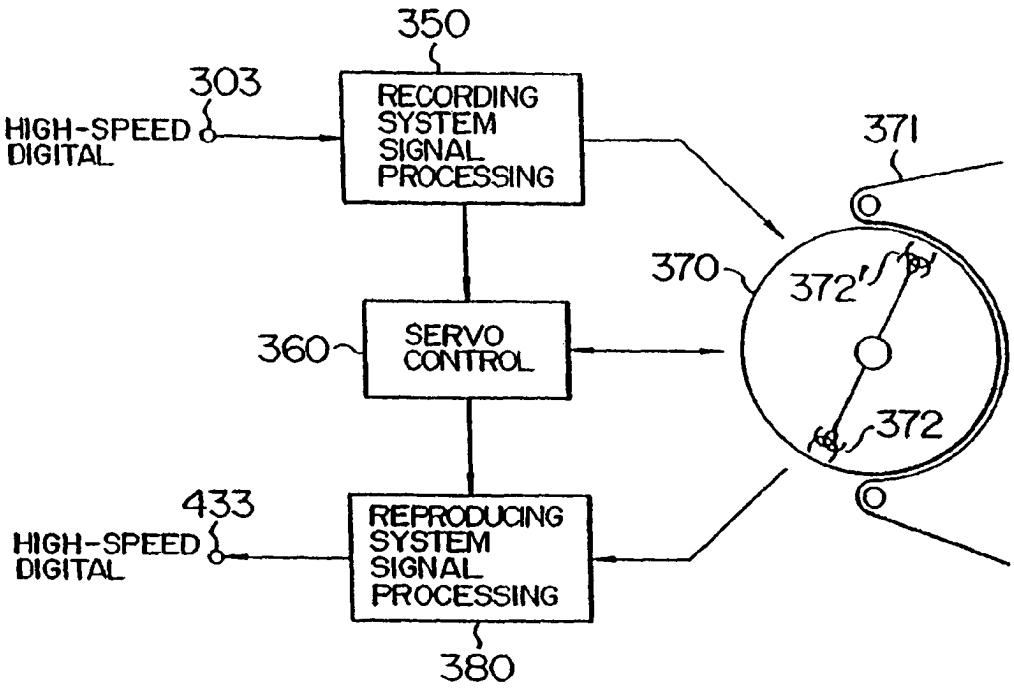

350
303
HIGH-SPEED DIGITAL
RECORDING SYSTEM SIGNAL PROCESSING
371
370
372'
360
SERVO CONTROL
372
433
HIGH-SPEED DIGITAL
REPRODUCING SYSTEM SIGNAL PROCESSING
380

FIG. 11

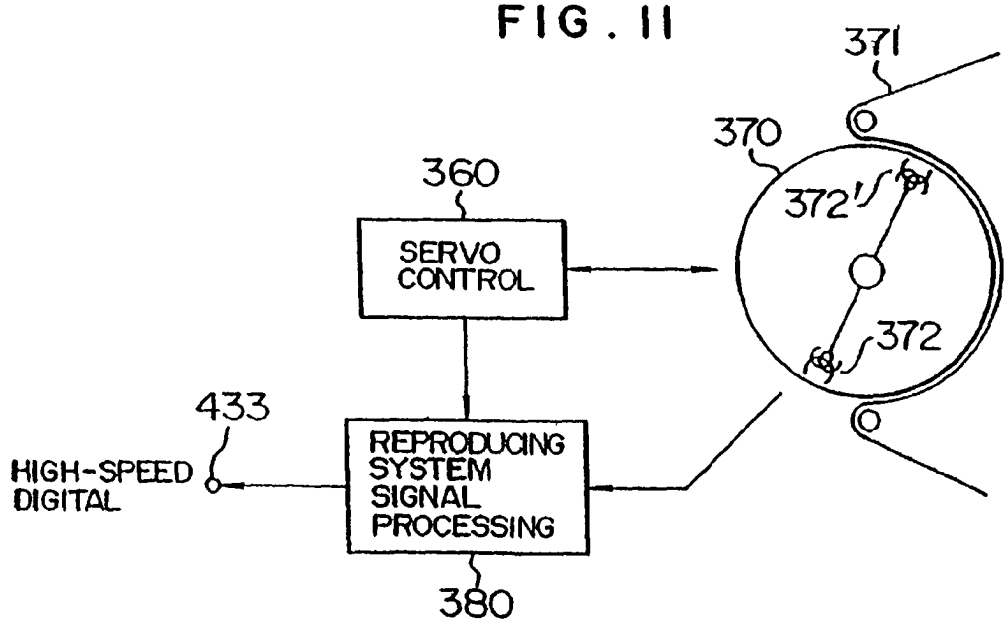

371
370
360
372'
SERVO CONTROL
372
433
HIGH-SPEED DIGITAL
REPRODUCING SYSTEM SIGNAL PROCESSING
380

FIG. 12

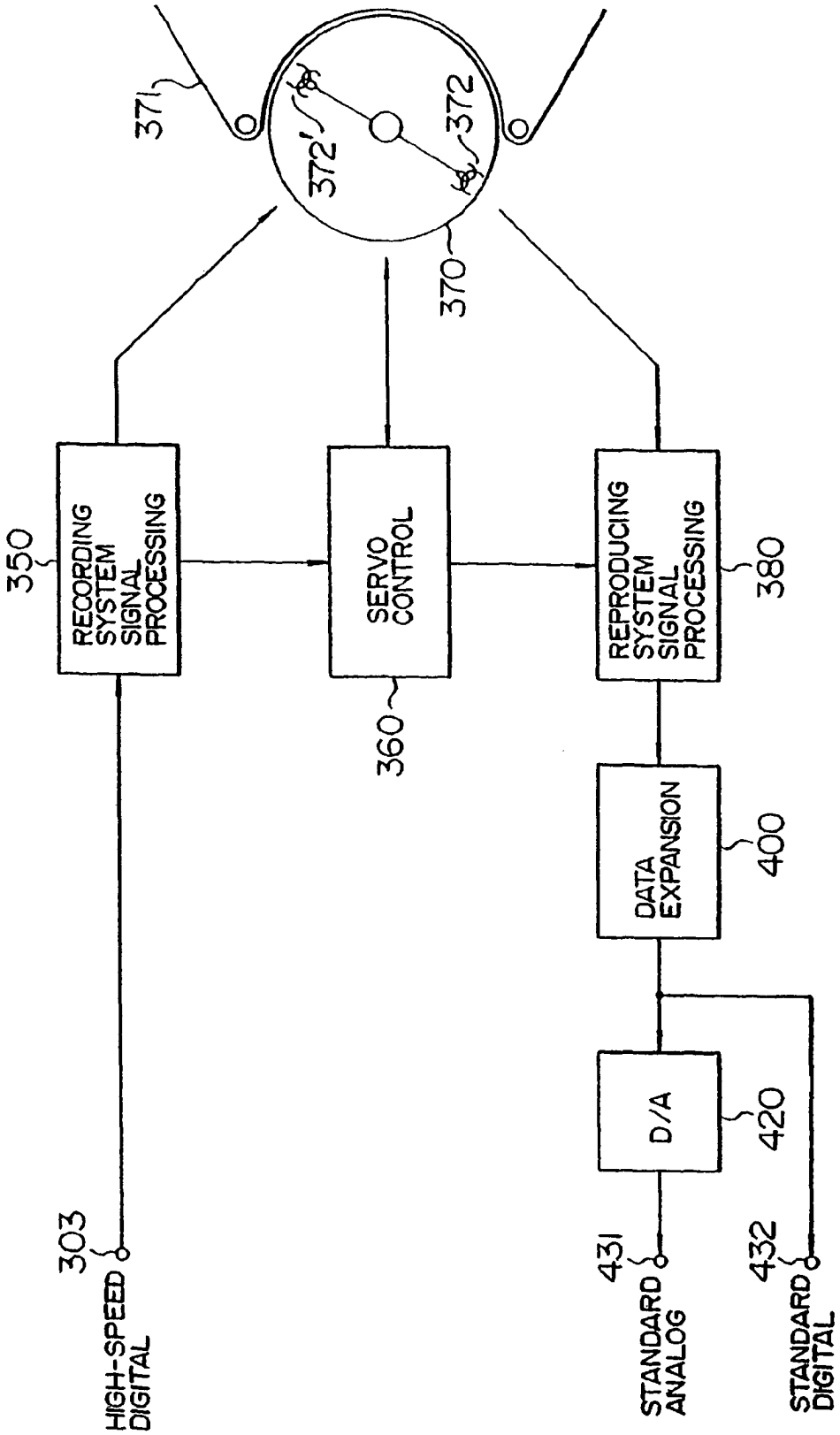

371
372'
372
370
350
RECORDING SYSTEM SIGNAL PROCESSING
SERVO CONTROL
360
REPRODUCING SYSTEM SIGNAL PROCESSING
380
DATA EXPANSION
400
D/A
420
303
HIGH-SPEED DIGITAL
431
STANDARD ANALOG
432
STANDARD DIGITAL

FIG. 13

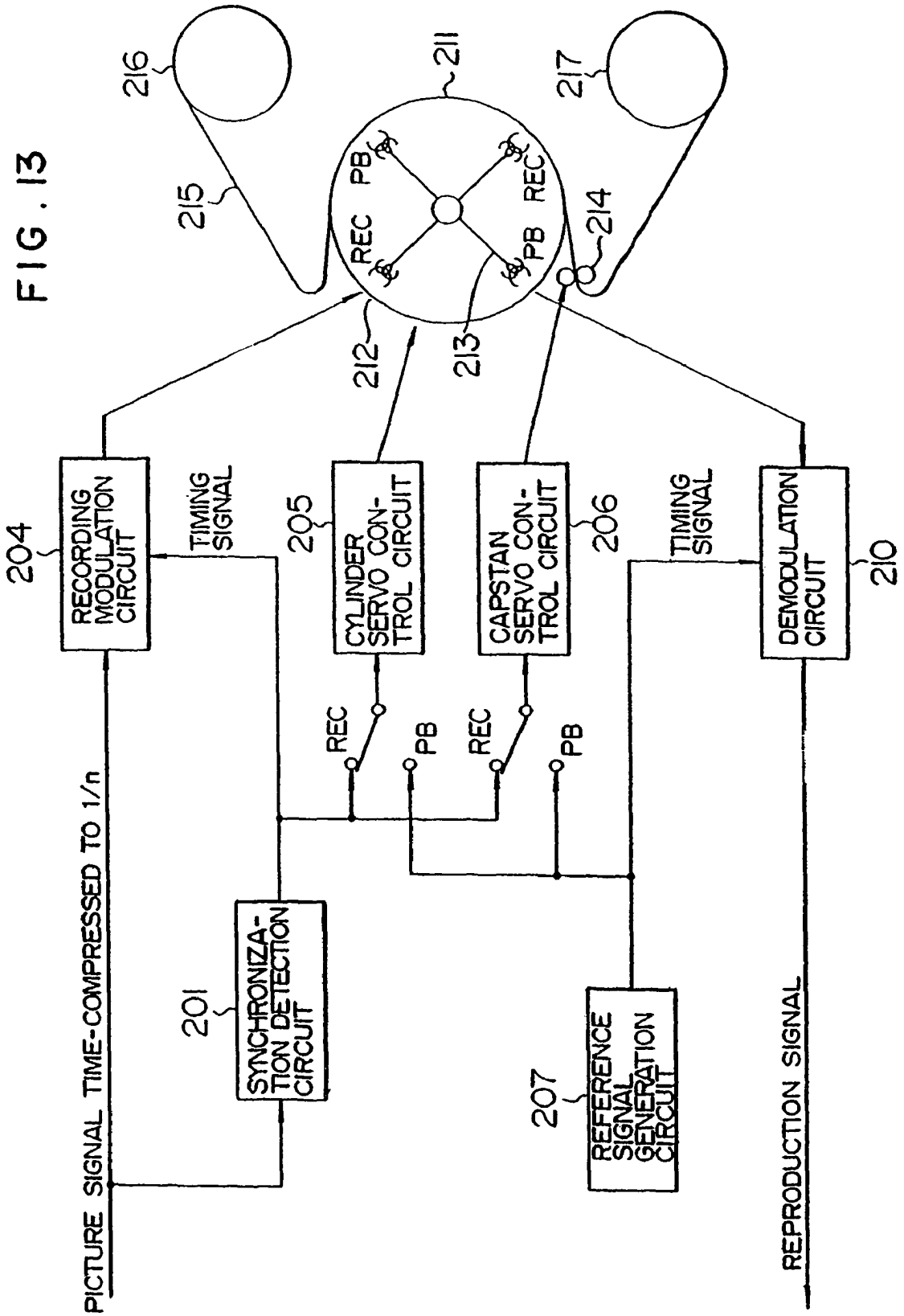

216
211
217
215
214
REC PB
PB REC
212
213
204
RECORDING MODULATION CIRCUIT
TIMING SIGNAL
205
CYLINDER SERVO CONTROL CIRCUIT
206
CAPSTAN SERVO CONTROL CIRCUIT
TIMING SIGNAL
DEMODULATION CIRCUIT
210
REC
PB
REC
PB
PICTURE SIGNAL TIME-COMPRESSED TO 1/n
201
SYNCHRONIZATION DETECTION CIRCUIT
207
REFERENCE SIGNAL GENERATION CIRCUIT
REPRODUCTION SIGNAL

FIG. 14

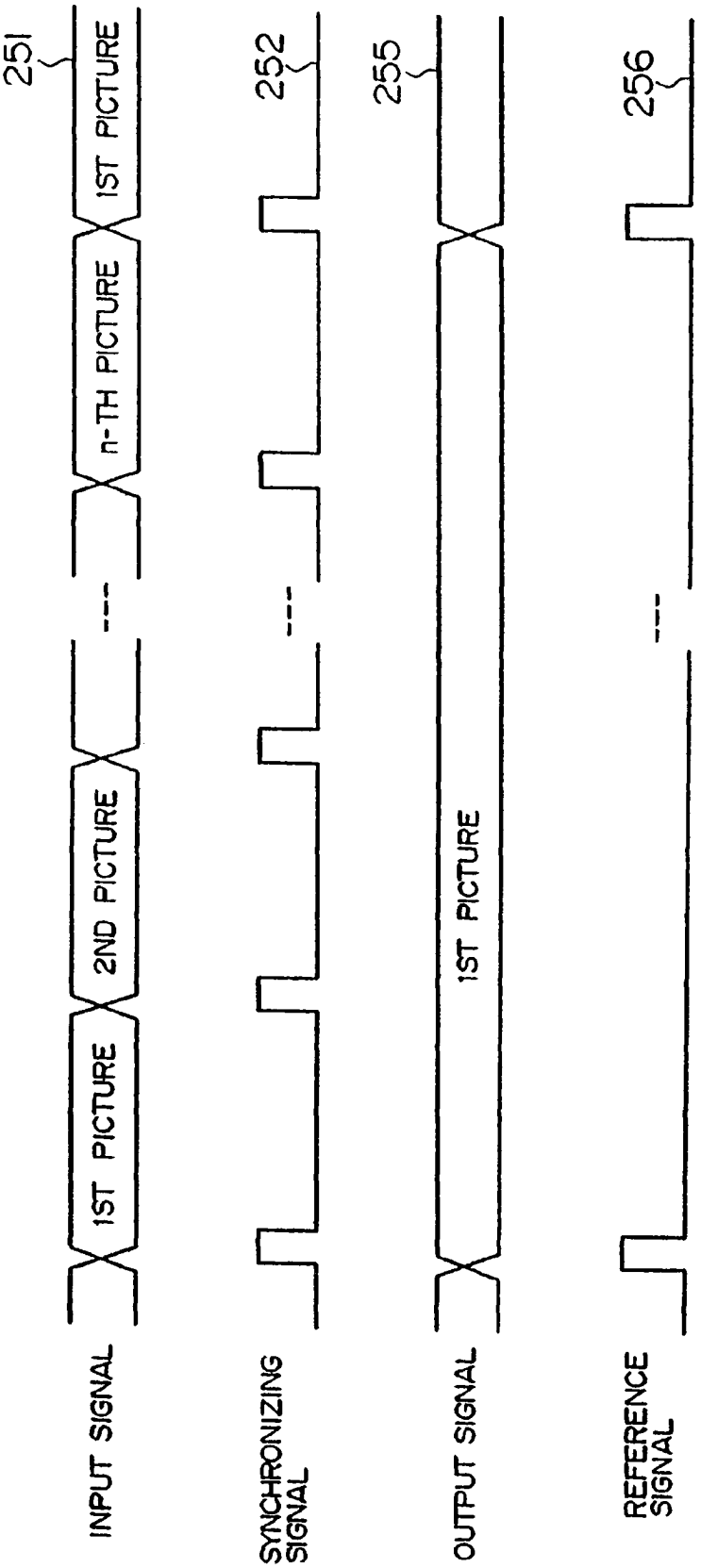

251
252
255
256
1ST PICTURE
2ND PICTURE
n-TH PICTURE
1ST PICTURE
INPUT SIGNAL
SYNCHRONIZING SIGNAL
OUTPUT SIGNAL
REFERENCE SIGNAL

FIG. 15

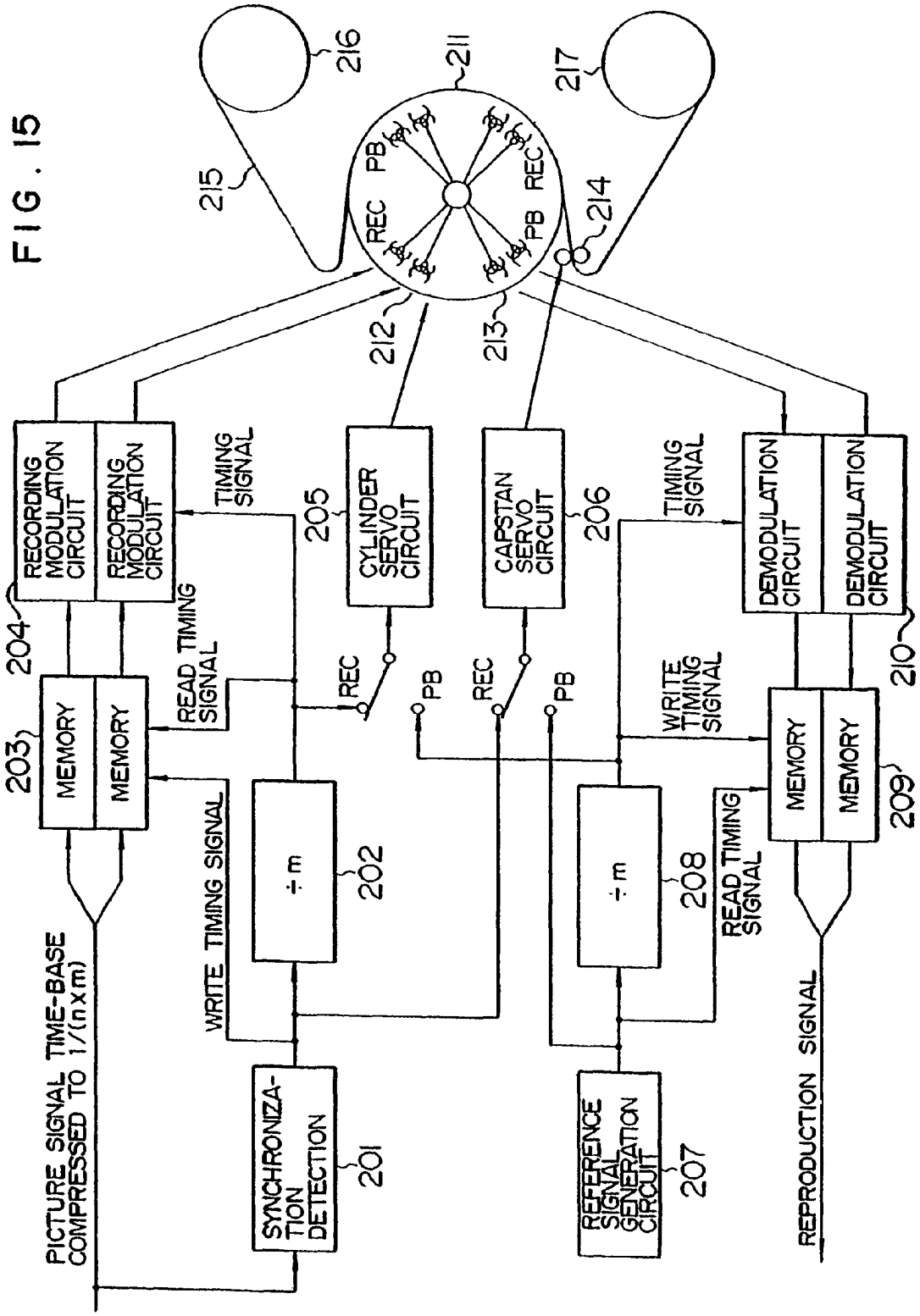

216
211
217
215
REC PB
PB REC
214
212
213
RECORDING MODULATION CIRCUIT
RECORDING MODULATION CIRCUIT
TIMING SIGNAL
205
CYLINDER SERVO CIRCUIT
CAPSTAN SERVO CIRCUIT
206
TIMING SIGNAL
DEMODULATION CIRCUIT
DEMODULATION CIRCUIT
204
READ TIMING SIGNAL
REC
PB
REC
PB
WRITE TIMING SIGNAL
210
203
MEMORY
MEMORY
MEMORY
MEMORY
209
WRITE TIMING SIGNAL
÷ m
202
÷ m
208
READ TIMING SIGNAL
PICTURE SIGNAL TIME-BASE COMPRESSED TO 1/(n x m)
SYNCHRONIZATION DETECTION
201
REFERENCE SIGNAL GENERATION CIRCUIT
207
REPRODUCTION SIGNAL

FIG. 16

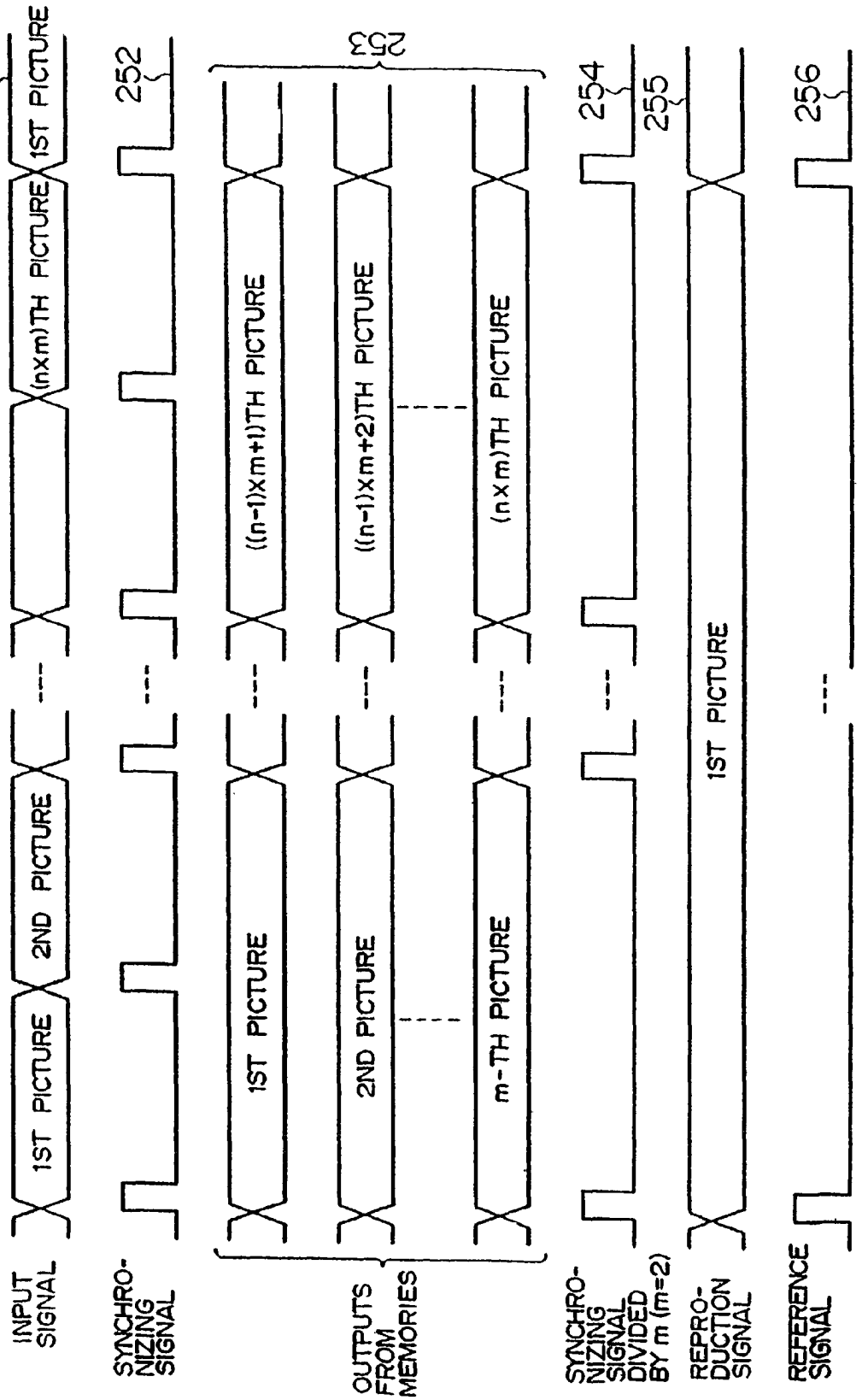
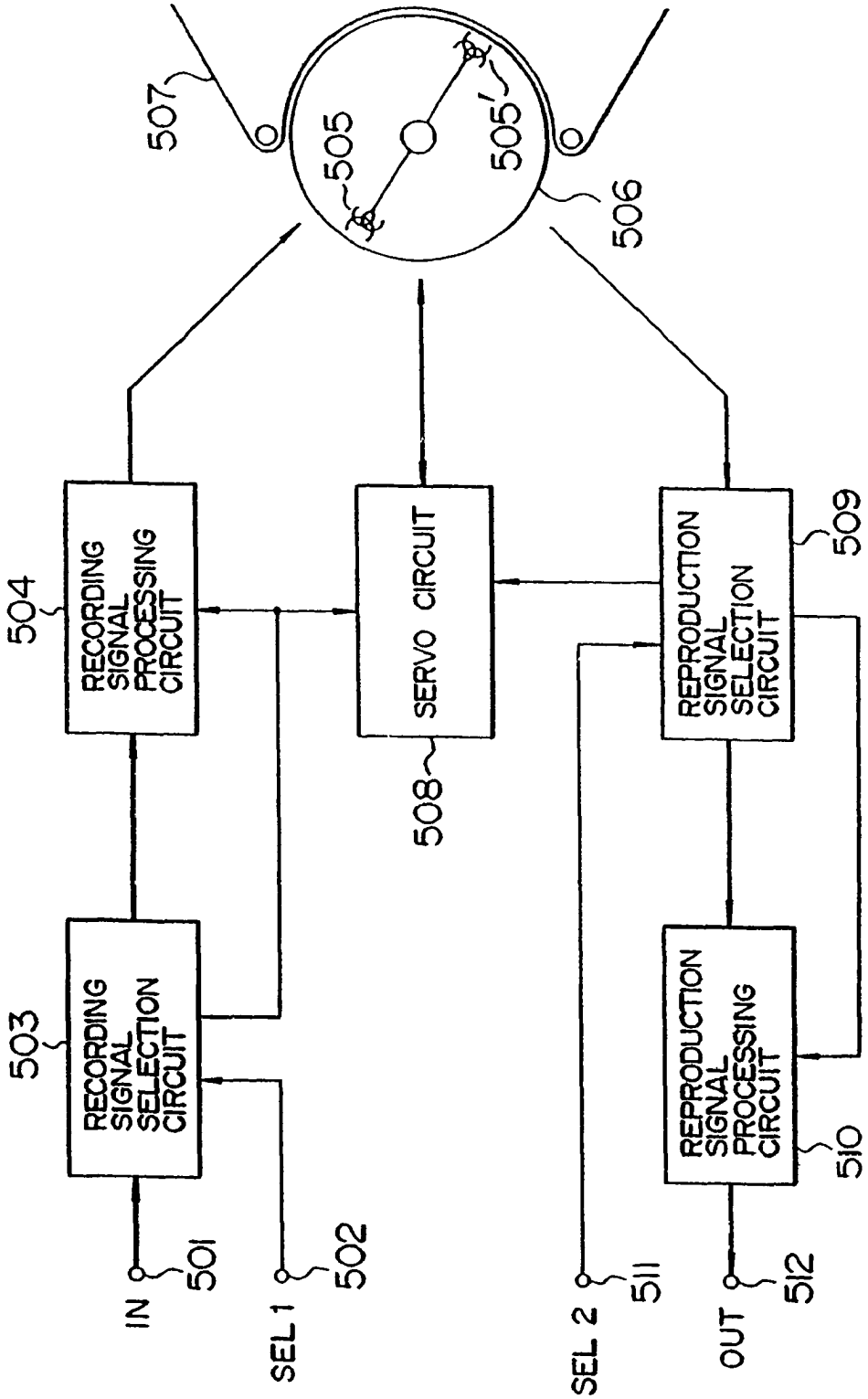

251
252
253
254
255
256
INPUT SIGNAL
SYNCHRO-NIZING SIGNAL
OUTPUTS FROM MEMORIES
SYNCHRO-NIZING SIGNAL DIVIDED BY m (m=2)
REPRO-DUCTION SIGNAL
REFERENCE SIGNAL
1ST PICTURE
2ND PICTURE
(nxm)TH PICTURE
((n-1)xm+1)TH PICTURE
((n-1)xm+2)TH PICTURE
m-TH PICTURE

FIG. 17

SYSTEM	MODE		TAPE SPEED (RATIO TO STANDARD SPEED)		CYLINDER ROTATION SPEED (rpm)		NUMBER OF HEAD PAIRS		CYLINDER DIAMETER (mmφ)	CYLINDER CONTACT ANGLE (deg)	NUMBER OF TRACKS REQUIRED FOR ONE PICTURE	REMARKS
	REC	PB	REC	PB	REC	PB	REC	PB				
VHS (NTSC)	NORMAL SPEED	NORMAL SPEED	1	1	1800	1800	1	1	62	180	1	
D2 (NTSC)	NORMAL SPEED	NORMAL SPEED	1	1	5400	5400	2	2	96	180	6	
EXAMPLE ①	HIGH SPEED	NORMAL SPEED	10	1	9000	900	1	1	120	180	1/2	
	HIGH SPEED	HIGH SPEED	10	10	9000	9000						
	NORMAL SPEED	HIGH SPEED	1	10	900	9000						
EXAMPLE ②	HIGH SPEED	NORMAL SPEED	10	1	9000	900	1	1	90	270	1/2	
	HIGH SPEED	HIGH SPEED	10	10	9000	9000						
	NORMAL SPEED	HIGH SPEED	1	10	900	9000						
EXAMPLE ③	HIGH SPEED	NORMAL SPEED	10	1	18000	1800	1	1	60	180	1	
	HIGH SPEED	HIGH SPEED	10	10	18000	18000						
	NORMAL SPEED	HIGH SPEED	1	10	1800	18000						
EXAMPLE ④	HIGH SPEED	NORMAL SPEED	10	1	9000	900	2	2	60	180	1	
	HIGH SPEED	HIGH SPEED	10	10	9000	9000						
	NORMAL SPEED	HIGH SPEED	1	10	900	9000						
EXAMPLE ⑤	HIGH SPEED	NORMAL SPEED	10	1	9000	1800	2	1	60	180	1	MOVABLE HEADS ARE REQUIRED
	HIGH SPEED	HIGH SPEED	10	10	9000	9000	2	2				
	NORMAL SPEED	HIGH SPEED	1	10	1800	9000	1	2				

FIG. 18


507
505
505'
506
504
RECORDING SIGNAL PROCESSING CIRCUIT
SERVO CIRCUIT
508
509
REPRODUCTION SIGNAL SELECTION CIRCUIT
503
RECORDING SIGNAL SELECTION CIRCUIT
REPRODUCTION SIGNAL PROCESSING CIRCUIT
510
IN
501
SEL 1
502
SEL 2
511
OUT
512

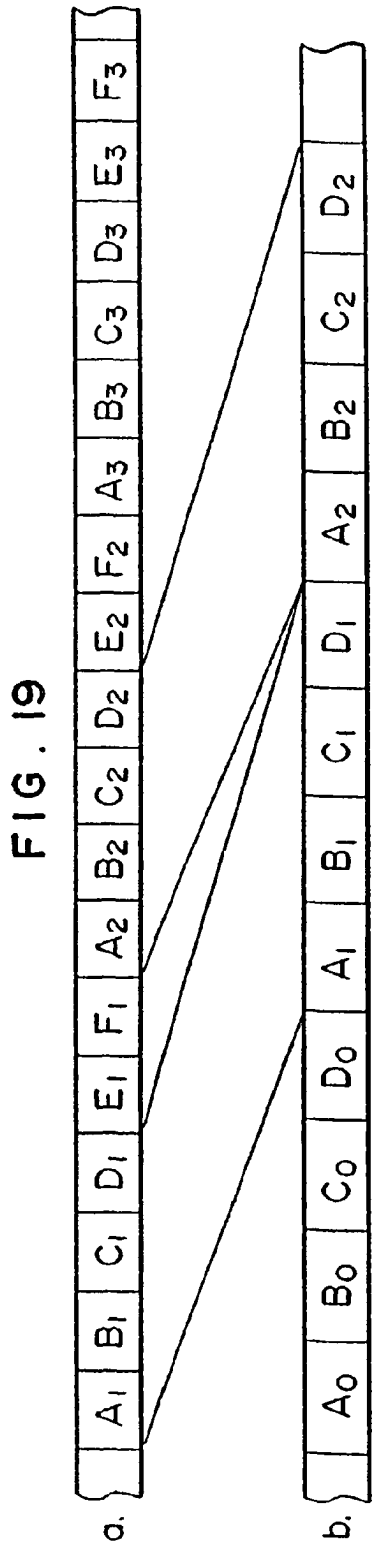

a.
b.
A1 B1 C1 D1 E1 F1 A2 B2 C2 D2 E2 F2 A3 B3 C3 D3 E3 F3
A0 B0 C0 D0 A1 B1 C1 D1 A2 B2 C2 D2

FIG. 19

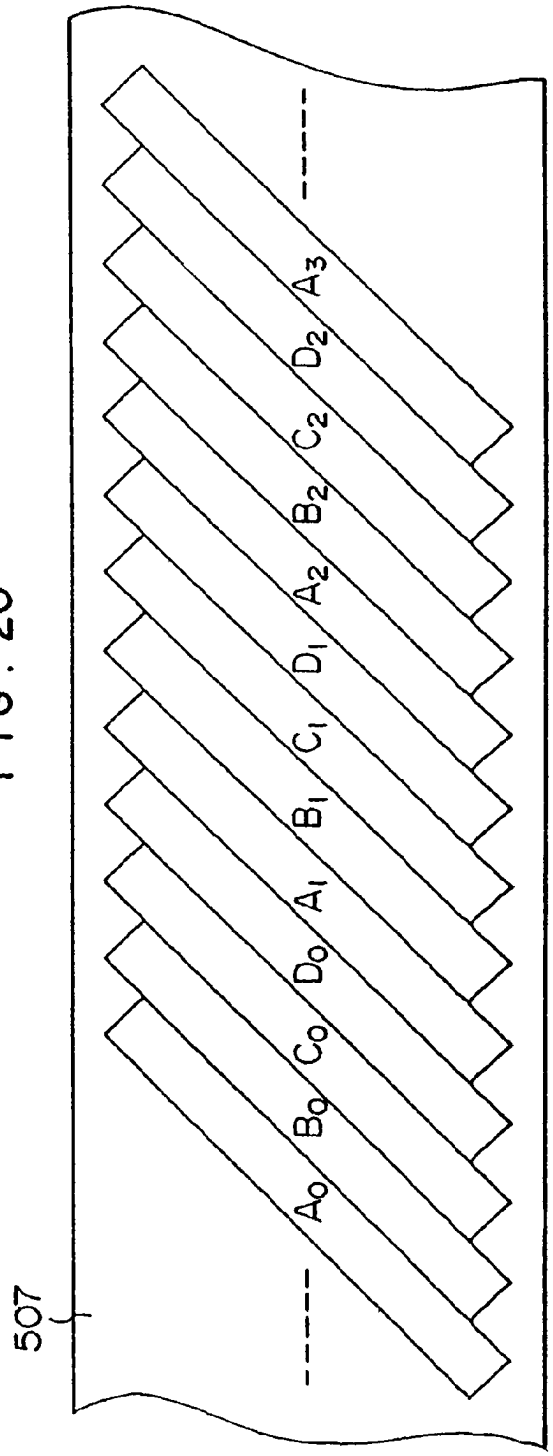

507
A0 B0 C0 D0 A1 B1 C1 D1 A2 B2 C2 D2 A3

FIG. 20

APPARATUS AND METHOD FOR RECEIVING AND RECORDING DIGITAL INFORMATION

CROSS REFERENCE TO RELATED APPLICATIONS

This is a continuation of U.S. application Ser. No. 10/404,452, filed Apr. 2, 2003, now U.S. Pat. No. 7,012,769, which is a continuation application of U.S. application Ser. No. 10/277,830, filed Oct. 23, 2002, now U.S. Pat. No. 6,590,726, which is a continuation of U.S. Ser. No. 09/809,047, filed Mar. 16, 2001, now U.S. Pat. No. 6,498,691, which is a continuation application of U.S. application Ser. No. 09/654,962, filed Sep. 5, 2000, now U.S. Pat. No. 6,324,025, which is a continuation of U.S. Ser. No. 09/567,005, filed May 9, 2000, now U.S. Pat. No. 6,278,564, which is a continuation application of U.S. Ser. No. 09/326,595, filed Jun. 7, 1999, now U.S. Pat. No. 6,069,757, which is a continuation of U.S. application Ser. No. 09/188,303, filed Nov. 10, 1998, now U.S. Pat. No. 6,002,536, which is a continuation of U.S. application Ser. No. 08/917,176, filed Aug. 25, 1997, now U.S. Pat. No. 5,862,004, which is a continuation of U.S. application Ser. No. 08/620,879, filed Mar. 22, 1996, now U.S. Pat. No. 5,699,203, and with U.S. application Ser. No. 08/620,880, filed Mar. 22, 1996, now U.S. Pat. No. 5,673,154, which are continuations of U.S. application Ser. No. 08/457,597, filed Jun. 1, 1995, now U.S. Pat. No. 5,530,598, which is a continuation of U.S. application Ser. No. 08/457,486, filed Jun. 1, 1995, now U.S. Pat. No. 5,517,368, which is a continuation of U.S. application Ser. No. 08/238,528, filed May 5, 1994, now U.S. Pat. No. 5,671,095, which is a divisional of U.S. application Ser. No. 07/727,059, filed Jul. 8, 1991, now U.S. Pat. No. 5,337,199, the subject matter of which are incorporated by reference herein.

BACKGROUND OF THE INVENTION

The present invention relates to a system for transmitting a digital video signal and recording the received video signal. More particularly, the present invention relates to great extension of the range of use of a digital signal recording/reproducing system by greatly shortening a recording time through transmission of a video signal in a compressed form, and further relates to great extension of the range of use of a digital signal recording/reproducing system by making the number of signals to be recorded and a recording/reproducing time variable.

As a digital magnetic recording/reproducing system (hereinafter referred to as VTR) is conventionally known, for example, a D2 format VTR. In such a conventional digital VTR, the elongation or shortening of a reproducing time is possible by using variable-speed reproduction. However, the prior art reference does not at all disclose high-speed recording in which a recording time is shortened to 1/m, multiple recording in which a plurality of signals are recorded, and the compression/expansion of a recording/reproducing time.

The above-mentioned conventional digital VTR has a feature that a high quality is attained and there is no deterioration caused by dubbing. However, the shortening of a dubbing time is not taken into consideration. Therefore, for example, in the case where a two-hour program is to be recorded, two hours are required. Thus, there is a drawback that inconveniences are encountered in use. Also, the multiplexing of recording signals is not taken into consideration. Therefore, for example, when two kinds of programs are to be simultaneously recorded or reproduced, two VTR's are required. This also causes inconveniences in use.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a digital VTR in which high-speed recording onto a tape can be made with the same format as that used in standard-speed recording, to provide a transmission signal processing system for transmitting at a high speed a video signal to be recorded by such a digital VTR, and to extend the range of use of the digital VTR by shortening a recording time. For example, the digital VTR can be used in such a manner that a two-hour program is recorded in about ten minutes and is reproduced at a standard speed.

The above object is achieved as follows. A video signal and an audio signal are subjected to time-base compression to 1/m, bit compression to 1/n, addition of a parity signal and modulation, and are thereafter transmitted or outputted. The transmitted signal is received, is subjected to demodulation, error correction, addition of a parity signal and modulation, and is thereafter recorded, onto a magnetic tape which travels at a travel speed m times as high as that upon normal reproduction, by use of a magnetic head on a cylinder which rotates at a frequency m times as high as that upon normal reproduction. The signal on the magnetic tape traveling at a travel speed upon normal reproduction is reproduced by a magnetic head on the cylinder which rotates at a frequency upon normal reproduction. The reproduced signal is subjected to demodulation, error correction, bit expansion of video and audio signals and D/A conversion, and is thereafter outputted. Address signals corresponding to a plurality of VTR's may be transmitted prior to a signal to be recorded. Further, control signals indicative of the start of recording and the stop of recording may be transmitted. The transmitted signals are received and error-corrected, and controls of the standby for recording, the start of recording and the stop of recording are made on the basis of the control signals.

With the above construction, since the video signal and the audio signal are time-base compressed to 1/m and bit-compressed to 1/n, a transmission time is shortened to 1/m and a signal band turns to m/n. The time-base compressed and bit-compressed signal is transmitted after addition of a parity signal for error correction and modulation to a code adapted for a transmission path. The transmitted signal is received and demodulated. The detection of an error produced in a transmitting system and the correction for the error can be made using the added parity signal. The error-corrected signal is added with a parity signal for correction for an error produced in a magnetic recording/reproducing system and is modulated to a code adapted for the magnetic recording/reproducing system. Upon recording, since the rotation frequency of the cylinder and the travel speed of the magnetic tape are increased by m times, the recording onto the magnetic tape can be made at an m-tuple speed. Upon reproduction, by setting the rotation frequency of the cylinder and the travel speed of the magnetic tape to normal ones, the reproduction at a normal speed can be made. The reproduced signal is code-demodulated. The detection of an error produced in the magnetic recording/reproducing system and the correction for the error can be made on the basis of the parity signal. By bit-expanding the video signal and the audio signal compressed by the transmission signal processing system, the original video and audio signal can be restored. The bit-expanded signal is converted into an analog signal by a D/A converter. Simultaneous and selective control of the start/stop of recording for a multiplicity of VTR's can be made in such a manner

that the address signals corresponding to the VTR's are transmitted prior to a signal to be recorded, the correction for an error of the received signal is made, required VTR's are brought into recording standby conditions by the corrected address signals, and the controls of the start of recording and the stop of recording are made by the transmitted control signals.

Another object of the present invention is to provide a digital signal recording/reproducing system in which multiple recording onto a tape can be made with the same format as that used in standard recording and simultaneous multiple reproduction is possible, and to extend the range of use of a digital VTR by compressing/expanding a recording/reproducing time in accordance with the transmission rate of a multiplexed input/output signal and the number of signals in the multiplexed input/output signal.

This object is achieved as follows. There are provided means for selecting one or plural desired signals from a time-base compressed and time-division multiplexed digital input signal, and helical scan recording means for making time-division multiplex recording of the selected signals with a time-base compressed speed after selection being retained. There is further provided means for reproducing the recorded signals with the rotation speed of a cylinder, a tape speed and so on being set to values proportional to the transmission rate of a reproduction signal and the number of signals to be simultaneously reproduced and with the signal being time-base expanded or being retained as time-base compressed.

With the above construction, N kinds of desired signals selected from the multiplexed input digital signal and time-base compressed to 1/K are subjected to time-division multiplex recording with a time-base compressed speed after selection being retained. Upon reproduction, for example, if both the cylinder rotation speed and the tape speed are set to N/K times, a recording track and a reproducing track coincide with each other and the use of a reproducing time K/N times as long as a recording time enables the reproduction of each of the N kinds of signals at a standard speed. Also, if both the cylinder rotation speed and the tape speed are set to (M×N)/K times, a recording track and a reproducing track coincide with each other and the use of a reproducing time as K/(M×N) times as long as the recording time enables the reproduction of each of the N kinds of signals at an M-tuple speed. In the case where L kinds of signals are selected from among the N kinds of reproduced signals and a processing speed at a reproduction signal processing circuit is set to L×M times as long as a standard reproduction processing speed, each of the L kinds of signals among the N kinds of multiple-recorded signals is outputted at a speed M times as high as a standard speed.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a digital transmission signal processing system and a recording/reproducing system according to an embodiment of the present invention;

FIG. **2** is a block diagram of a recording/reproducing system according to another embodiment of the present invention;

FIG. **3** is a diagram for explaining the conventional parity adding method;

FIG. **4** is a block diagram of a recording/reproducing system according to still another embodiment of the present invention;

FIG. **5** is a block diagram of a digital transmission signal processing system and a recording/reproducing system according to a further embodiment of the present invention;

FIG. **6** shows the format of control signals used in one of applications of the present invention;

FIG. **7** is a block diagram of a still further embodiment of the present invention;

FIG. **8** shows one example of the specification of signals to be recorded;

FIG. **9** is a block diagram of a furthermore embodiment of the present invention;

FIGS. **10**, **11** and **12** are block diagrams of different examples of applications of the present invention;

FIG. **13** is a block diagram for explaining one example of the operation of the embodiment shown in FIG. **7**;

FIG. **14** is a timing chart showing the waveforms of signals involved in the example shown in FIG. **13**;

FIG. **15** is a block diagram for explaining another example of the operation of the embodiment shown in FIG. **7**;

FIG. **16** is a timing chart showing the waveforms of signals involved in the example shown in FIG. **15**;

FIG. **17** is a table showing some applications of the examples shown in FIGS. **13** and **15**;

FIG. **18** is a block diagram of a still furthermore embodiment of the present invention; and

FIGS. **19** and **20** are signal diagrams for explaining different operations of the embodiment shown in FIG. **18**.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of the present invention will now be explained by use of FIG. **1**. In the figure, reference numerals **1** and **40** denote magnetic tapes, numerals **2**, **3**, **41** and **42** magnetic heads, numerals **4** and **43** cylinders, numerals **5** and **44** capstans, numerals **10** and **50** servo control circuits, numerals **20**, **31** and **60** demodulation circuits, numerals **21**, **32** and **61** error correction circuits, numerals **22** and **23** compression circuits, numerals **24** and **33** parity addition circuits, numerals **25** and **34** modulation circuits, numerals **26** a transmission circuit, numeral **27** a transmission path, numeral **30** a reception circuit, numerals **62** and **63** expansion circuits, numerals **64** and **65** D/A conversion circuits, numeral **70** a video signal output terminal, and numeral **71** an audio signal output terminal.

Firstly, the operation of a transmission signal processing system will be explained. Digital video and audio signals recorded on the magnetic tape **1** are reproduced by the magnetic heads **2** and **3** mounted on the cylinder **4** and are inputted to the demodulation circuit **20**. The magnetic tape **1** travels by virtue of the capstan **5**. The travel speed of the magnetic tape **1** and the rotation frequency of the cylinder **4** are, for example, ten times as high as the tape travel speed and the cylinder rotation speed upon normal reproduction. Accordingly, the signal inputted to the demodulation circuit **20** is a signal time-compressed to one tenth. For example, a 120-minute signal recorded on the magnetic tape **1** can be reproduced in 12 minutes.

Generally, in the case where a digital signal is to be recorded on a magnetic recording medium, the signal is recorded after having been modulated into scrambled NRZ code, M^2 code or the like. The demodulation circuit **20** performs a demodulation processing, that is, a signal processing for restoring the thus modulated signal into original digital data. The signal demodulated by the demodulation circuit **20** is inputted to the error correction circuit **21** in which erroneous data produced in a magnetic recording/reproducing process is detected and the correction for the erroneous data is made. Further, the signal is separated into a video signal and an audio signal which are in turn inputted to the compression

circuits **22** and **23**, respectively. The video signal is bit-compressed through, for example, discrete cosine conversion. The audio signal is bit-compressed through, for example, non-linear quantization or differential PCM. As a result, the transmission rate of the video signal and the audio signal in total is reduced to, for example, one twentieth.

Output signals of the compression circuits **22** and **23** are inputted to the parity addition circuit **24** for performing a signal processing which includes adding a parity signal for error correction and outputting the video signal and the audio signal serially in accordance with a transmission format. A serial output signal of the parity addition circuit **24** is inputted to the modulation circuit **25**. In the modulation circuit **25**, the serial signal is modulated in accordance with the characteristic and the frequency band of the transmission path **27**. For example, in the case where the signal is transmitted in an electric wave form, quadruple phase shift keying (QPSK) is made. The modulated signal is inputted to the transmission circuit **26** from which it is outputted to the transmission path **27**.

As apparent from the foregoing explanation of the operation of the transmission signal processing system, it is possible to transmit a signal at a speed which is ten times as high as a normal speed.

The above embodiment has been shown in conjunction with the case where a signal from the VTR is reproduced. However, a signal source is not limited to the VTR and may include a magnetic disk device, an optical disk device or the like.

Next, explanation will be made of the operation of the VTR for receiving and recording the transmitted signal. The signal transmitted from the transmission signal processing system is received by the reception circuit **30**. The received signal is inputted to the demodulation circuit **31**. The demodulation circuit **31** is provided corresponding to the modulation and demodulates the signal to the original signal. The demodulated signal is inputted to the error correction circuit **32** in which the detection of and the correction for an error produced in the transmission path **27** are made on the basis of the parity signal added by the parity addition circuit **24**. At this time, in the case where the S/N ratio of the transmission system is not sufficient so that complete correction for the error is impossible, correction is made through, for example, signal replacement, by use of the signal correlation.

An output signal of the error correction circuit **32** is inputted to the parity addition circuit **33**. In the parity addition circuit **33**, a parity signal for detecting an error produced in a recording/reproducing process and making correction for the error is added. The parity-added signal is inputted to the modulation circuit **34**. In the modulation circuit **34**, the signal is modulated to scrambled NRZ code, M^2 code or the like as mentioned above. The modulated signal is recorded on the magnetic tape **40** by the magnetic heads **41** and **42** mounted on the cylinder **43**.

Since the signal supplied to the magnetic heads **41** and **42** is a signal which is time-base compressed to one tenth as compared with a signal upon normal operation, the servo control circuit **50** controls the cylinder **43** and the capstan **44** so that the rotation frequency of the cylinder **43** and the travel speed of the magnetic tape **40** become ten times as high as those upon normal recording. Also, in order to record a predetermined signal at a predetermined position on the magnetic, tape **40**, synchronization information is detected from the received signal to control the phase of rotation of the cylinder **41** on the basis of the detected synchronization information.

Next, the operation of the VTR for reproducing the thus recorded signal will be explained. Upon reproduction, the travel speed of the magnetic tape **40** and the rotation frequency of the cylinder **43** are set to those upon normal reproduction. The reproduced signal is inputted to the demodulation circuit **60**. The demodulation circuit **60** is provided corresponding to the modulation circuit **34** and demodulates the modulated signal. The demodulated signal is inputted to the error correction circuit **61** in which the detection of an error produced in the magnetic recording/reproducing system and the correction for the error are made on the basis of the parity signal added by the parity addition circuit **33**. In the case where there is an error which cannot be corrected, the error is properly corrected by use of the signal correlation. Also, the signal is outputted after having been separated into a video signal and an audio signal.

The video signal is inputted to the expansion circuit **62**. The expansion circuit **62** is provided corresponding to the compression circuit **22** and restores the compressed video signal into the original video signal. An output signal of the expansion circuit **62** is inputted to the D/A conversion circuit **64** and is converted thereby into an analog video signal which is in turn outputted from the terminal **70**.

The audio signal is inputted to the expansion circuit **63**. The expansion circuit **63** is provided corresponding to the compression circuit **23** and restores the compressed audio signal into the original audio signal. An output signal of the expansion circuit **63** is inputted to the D/A conversion circuit **65** and is converted thereby into an analog audio signal which is in turn outputted from the terminal **71**.

In the foregoing, the embodiment of the present invention has been shown and the operation thereof has been explained. According to the present invention, a video signal and an audio signal over a long time can be transmitted and recorded in a short time, thereby making it possible to extend the range of use of the digital VTR.

Another embodiment of the present invention is shown in FIG. **2**. FIG. **2** is partially similar to FIG. **1**. The same parts in FIG. **2** as those in FIG. **1** are denoted by the same reference numerals as those used in FIG. **1** and detailed explanation thereof will be omitted. The embodiment shown in FIG. **2** concerns a VTR in which a signal transmitted/received at a high speed can be recorded while being monitored.

In FIG. **2**, reference numeral **80** denotes a change-over switch, numeral **81** an error correction circuit, and numeral **82** a memory circuit. An error corrected video signal outputted from the error correction circuit **81** is inputted through the memory circuit **82** to a terminal R side of the change over switch **80** which is selected upon recording. The memory circuit **82** has a memory capacity for at least one field. The video signal received at a high speed is stored into a memory of the memory circuit **82** with the number of frames being reduced. The stored signal is read from the memory at a normal speed and is inputted to an expansion circuit **62**.

Upon reproduction, a video signal output of an error correction circuit **61** is inputted to a terminal P side of the change-over switch **80** which is selected upon reproduction. Accordingly, the operation of the embodiment of FIG. **2** upon reproduction is similar to that of the embodiment shown in FIG. **1**.

In the embodiment shown in FIG. **2**, upon recording, the video signal outputted from the error correction circuit **81** is inputted to the expansion circuit **62** through the memory circuit **82**. Alternatively, an output signal of a modulation circuit **34** may be inputted to a demodulation circuit **60** through a memory circuit. Also, in the case where the operating speed of the demodulation circuit **60** or the error cor-

rection circuit **61** leaves a margin, a memory circuit may be properly placed at a post stage. Or, in the case where the storage capacity of the error correction circuit **61** or the expansion circuit **62** leaves a margin, the circuit may be used as a memory circuit or any additional memory circuit may be omitted.

As has been explained in the above, the embodiment shown in FIG. **2** makes it possible to record a received video signal while monitoring it in the form of a picture having a reduced number of frames.

In the embodiment shown in FIG. **1**, the parity signal is added in order to make the detection of and the correction for an error which may be produced in the transmission system or the magnetic recording/reproducing system. One example of a parity adding method is shown in FIG. **3** in conjunction with the case of a D2 format VTR. In the D2 format VTR, a signal for one field is divided into a plurality of segments for signal processing. FIG. **3** shows one segment. In FIG. **3**, reference numeral **90** represents a group of video data, numeral **91** a group of outer code parities, and numeral **92** a group of inner code parities. Firstly, outer code parities are added for data of the matrix-like arranged video data group **90** which lie in a vertical direction in FIG. **3**. Thereafter, inner code parities are added for data of the video data group **90** and the outer code parity group **91** lying in a horizontal direction in FIG. **3**, thereby producing a signal to be recorded. Though detailed explanation of the generation of parities will be omitted herein, the parities are generated in accordance with a generating function G(x).

In the embodiment shown in FIG. **1**, if the same parity generation manner is employed by the parity addition circuits **24** and **33**, the error correction circuits **32** and **61** may hold the most part thereof in common. Namely, since the error correction circuits **32** and **61** are circuits which are respectively used upon recording and upon reproduction, it is possible to reduce the circuit scale or size by using the most part of the circuits **32** and **61** in common.

Further, in the case where the same parity generation manner is employed by the parity addition circuits **24** and **33** in the embodiment shown in FIG. **1**, it is possible to further reduce the circuit scale or-size of the recording/reproducing system. The construction in that case is shown in FIG. **4** as still another embodiment of the present invention. FIG. **4** is partially common to FIG. **1** or **2**. The parts in FIG. **4** common to those in FIG. **1** or **2** are denoted by the same reference numerals as those used in FIG. **1** or **2** and detailed explanation thereof will be omitted.

The embodiment shown in FIG. **4** is based on a concept that an error produced in a transmission system and an error produced in a magnetic recording/reproducing system are simultaneously detected and corrected by an error correction circuit **61**. Accordingly, a signal received by a reception circuit **30** is demodulated by a demodulation circuit **31** and is inputted to a modulation circuit **34** without being subjected to error correction and parity addition. The subsequent processing is the same as that in the embodiment shown in FIG. **1** or **2**. Namely, a reproduced signal is inputted to the error correction circuit **61** after demodulation by a demodulation circuit **60**. As mentioned above, an error produced in the transmission system and an error produced in the magnetic recording/reproducing system are simultaneously detected and corrected by the error correction circuit **61** in the reproducing system.

In the embodiment shown in FIG. **4**, the error correction circuit **32** and the parity addition circuit **33** can be removed as compared with the embodiment shown in FIG. **1** or **2**, thereby making it possible to reduce the circuit scale.

Though having not been mentioned in the foregoing embodiments, in a helical scan VTR as shown, since a signal becomes discontinuous when a track jump is made upon reproduction, the recording is made with an amble signal being added to the heading portion of a signal. Since the addition of an amble signal is employed in the D2 format VTR, detailed explanation thereof will be omitted. Also, in order to define a starting position of a signal, a synchronizing signal is properly added. Since the addition of a synchronizing signal is known in, for example, the D2 format VTR, detailed explanation thereof will be omitted.

In the embodiment shown in FIG. **1**, the addition of an amble signal may be made by the parity addition circuit **24**. Alternatively, it may be made on the recording/reproducing system side in order to enhance the efficiency of use of the transmission path **27**. In this case, the addition of an amble signal can be made by the parity addition circuit **33**. As for the embodiment shown in FIG. **4**, in the case where the addition of an amble signal is to be made on the recording/reproducing system side, the amble signal can be added by the modulation circuit **34**. In the case where the addition of an amble signal is made on the recording/reproducing system side, it is possible to enhance the efficiency of use of the transmission path **27**. On the other hand, in the case where the addition of an amble signal is made on the transmission signal processing system side, the lowering of the cost of a VTR can be attained as a great effect when a signal is sent to a multiplicity of VTR's simultaneously.

FIG. **5** shows a further embodiment of the present invention in which the further reduction of the circuit scale of a VTR on the receiving side and hence the further lowering of the cost can be attained in the case where a signal is sent to a multiplicity of VTR's simultaneously.

FIG. **5** is partially common to FIG. **1**, **2** or **4**. The parts in FIG. **5** common to those in FIG. **1**, **2** or **4** are denoted by the same reference numerals as those used in FIG. **1**, **2** or **4** and detailed explanation thereof will be omitted. In FIG. **5**, reference numeral **100** denotes a modulation circuit. The embodiment shown in FIG. **5** is based on a concept that a signal processing required upon a recording mode of a VTR is performed on the transmitting side. Namely, modulation adapted for magnetic recording/reproduction, for example, a signal processing corresponding to the modulation circuit **34** shown in FIG. **4** is performed on the transmission signal processing system side. After parities have been added by a parity addition circuit **24** of the transmission signal processing system, the modulation adapted for the magnetic recording/reproduction is performed by the modulation circuit **100**. Therefore, modulation adapted for transmission is performed by a modulation circuit **25**. As a modulation system employed by the modulation circuit **100** is suitable a system which does not cause the extension of a frequency band by modulation, for example, scrambled NRZ. A signal modulated by the modulation circuit **25** is transmitted to a transmission path **27** through a transmission circuit **26** in a manner to that in the embodiment shown in FIG. **1**.

The signal received by a reception circuit **30** through the transmission path **27** is inputted to a demodulation circuit **31** in which the signal is subjected to demodulation corresponding to the modulation circuit **25**. Since the signal demodulated by the demodulation circuit **31** is one which has already been subjected by the modulation circuit **10** to the modulation adapted for the magnetic recording/reproduction, the signal is recorded on a magnetic tape **40** by magnetic heads **41** and **42** as it is. As a result, the same recording as that in the embodiment shown in FIG. **4** is made. An operation upon reproduction is similar to that in the embodiment shown in FIG. **4**.

As apparent from the above, the present embodiment makes it possible to remarkably reduce the circuit scale of the VTR.

According to one of applications of the present invention, it is possible to transmit a signal from a transmission signal processing system to a multiplicity of VTR's through a transmission path simultaneously and at a high speed, as has already been mentioned. In this case, it is difficult to control a multiplicity of 'VTR's simultaneously. Further, it is required to make a control which causes specified ones of the VTR's to perform recording operations and specified others of the VTR's not to perform recording operations. A technique for realizing such a control will be shown just below.

For the above purpose, control signals are transmitted prior to transmission of a signal to be recorded. One example of the control signals is shown in FIG. **6**. In the figure, reference numeral **110** denotes a synchronizing signal, numeral **111** an ID signal indicative of a control to be made, numeral **112** an address signal indicative of a VTR to be controlled, numeral **113** a control signal for bringing a VTR designated by the address signal **112** into a recording mode, numeral **114** a control signal for stopping the recording, numerals **115** and **116** blank signals, and numeral **120** a recording signal to be actually recorded.

The ID signal **111** indicating the transmission of the address signals **112** indicative of VTR's in which a signal is to be recorded, is transmitted at a predetermined position relative to the synchronizing signal **110** to bring each VTR into a standby condition. After all the address signals have been transmitted, the ID signal **113** is transmitted to start the recording of the signal **120** in the designated VTR's. After the signal **120** has been transmitted, the ID signal **114** to control the stop of recording is transmitted. Each of the blank signals **115** and **116** is a signal for conforming a signal transmission format to the other transmission signal and is therefore an insignificant signal portion.

In the embodiments shown in FIGS. **1** and **5**, those control signals are produced by a control signal generation circuit **130** and are transmitted with parities which are added by the parity addition circuit **24** for making correction for an error produced during transmission.

In the VTR shown in FIG. **1**, the control signals are detected by a control circuit **131** after the reception by the reception circuit **30**, the demodulation by the demodulation circuit **31** and the correction by the error correction circuit **32** for an error produced during transmission to make a control for the recording and the stop of recording in the recording/reproducing system.

In the case of the VTR's shown in FIGS. **4** and **5**, an output signal of the demodulation circuit **31** is inputted to the error correction circuit **61** for a need of making correction for an error produced during transmission and error-corrected control signals are inputted to a control circuit **131**. In a change-over circuit **132**, the terminal R side for selecting an output signal of the demodulation circuit **31** is selected upon recording and the terminal P side for selecting an output signal of the demodulation circuit **60** is selected upon reproduction.

As apparent from the foregoing, the present embodiment makes it possible to control a multiplicity of VTR's selectively and simultaneously.

Also, the use of the change-over circuit **132** and a memory circuit makes it possible to record a signal while monitoring it in the form of a picture having a reduced number of frames, as explained in conjunction with the embodiment shown in FIG. **2**.

Next, a still further embodiment of the present invention will be explained by use of FIG. **7**. In the figure, reference numeral **301** denotes an input terminal for standard analog video signal, numeral **302** an input terminal for standard digital video signal, numeral **303** an input terminal for high-speed digital video signal, numeral **305** a recording system mode change-over switch, numeral **306** a recording system change-over signal generation circuit, numeral **310** an A/D converter, numeral **320** a change-over circuit, numeral **330** a data compression circuit, numeral **340** a change-over circuit, numeral **350** a recording system signal processing circuit for performing a signal processing which includes addition of error correction code and modulation for recording, numeral **370** a cylinder, numeral **371** a magnetic tape, numerals **372** and **372'** magnetic heads, numeral **380** a reproducing system signal processing circuit for performing a signal processing which includes demodulation for reproduction, error detection and error correction. Numeral **390** a change-over circuit, numeral **400** a data expansion circuit, numeral **420** a D/A converter, numeral **431** an output terminal for standard analog video signal, numeral **432** an output terminal for standard digital video signal, numeral **433** an output terminal for high-speed digital video signal, numeral **435** a reproducing system mode change-over switch, and numeral **436** a reproducing system change-over signal generation circuit.

The present embodiment is an example of a digital magnetic recording/reproducing system which has recording modes of standard-speed recording and high-speed recording and reproduction modes of standard-speed reproduction and high-speed reproduction. FIG. **8** shows one example of the specification of input video signals.

Firstly, explanation will be made of standard-speed recording. A digital signal into which an analog video signal inputted from the input terminal **301** is converted by the A/D converter **310** or an equivalent digital signal which is inputted from the input terminal **302**, is switched or selected by the change-over circuit **320**, is subjected to a predetermined data compression processing by the data compression circuit **330** and is thereafter inputted to a terminal **340***a* of the changeover circuit **340**. In the change-over circuit **340**, a change-over to connect the terminal **340***a* and a terminal **340***c* is made by a change-over signal from the recording system change-over signal generation circuit **306**. Thereby, the data-compressed signal is inputted to the recording system signal processing circuit **350**. In the recording system signal processing circuit **350**, a signal processing such as channel division, addition of error correction code and modulation for recording is performed at a predetermined processing clock adapted for the data-compressed signal. Thereafter, the signal is supplied to the magnetic heads **372** and **372'** mounted on the cylinder **370** so that it is recorded onto the magnetic tape **371**. The cylinder **370** and the magnetic tape **371** are controlled by a servo control circuit **360**. The servo control circuit **360** controls a cylinder motor and a capstan motor so as to provide a cylinder rotation speed and a tape speed for standard speed and so as to be synchronized with the input video signal.

Next, explanation will be made of high-speed recording. A high-speed digital video signal inputted from the input terminal **303** is sent to a terminal **340***b* of the change-over circuit **340**. Since the high-speed digital video signal is a signal which has already been subjected to a data compression processing, it is not necessary to pass the signal through the data compression circuit **330**. A change-over to connect the terminal **340***b* and the terminal **340***c* is made by a change-over signal from the recording system change-over signal generation circuit **306** so that the high-speed digital video signal is inputted to the recording system signal processing circuit **350**. In the recording system signal processing circuit **350**, a signal processing similar to that in the case of the standard-

speed recording is performed at a predetermined processing clock adapted for the high-speed digital video signal. Thereafter, the signal is supplied to the magnetic heads **372** and **372'** mounted on the cylinder **370** so that it is recorded onto the magnetic tape **371**. The cylinder **370** and the magnetic tape **371** are controlled by the servo control circuit **360**. The servo control circuit **360** control the cylinder motor and the capstan motor so as to provide a predetermined cylinder rotation speed and a predetermined tape speed and so as to be synchronized with the input video signal.

In the present invention, the recording onto the tape can be made with the quite same format in both the standard-speed recording and the high-speed recording, thereby making it possible to greatly shorten a recording time in the high-speed recording mode.

Next, explanation will be made of a signal processing upon reproduction. In the present embodiment, the recording pattern on the magnetic tape is the same whichever of the standard-speed recording and the high-speed recording is selected as a recording mode. Therefore, either standard-speed reproduction or high-speed reproduction can be selected irrespective of the recording mode.

Firstly, the standard-speed reproduction will be explained. The servo control circuit **360** controls the cylinder motor and the capstan motor so that a cylinder rotation speed and a tape speed for standard speed are provided. A signal reproduced by the magnetic heads **372** and **372'** is inputted to the reproducing system signal processing circuit **380**. In the reproducing system signal processing circuit **380**, a signal processing such as demodulation for reproduction, channel synthesis, error detection and error correction is performed at a predetermined processing clock adapted for the standard-speed reproduction. Thereafter, the signal is supplied to a terminal **390***a* of the change-over circuit **390**. In the change-over circuit **390**, a changeover to connect the terminal **390***a* and a terminal **390***c* is made upon standard-speed reproduction by a change-over signal from the reproducing system change-over signal generation circuit **436**. Thereby, the reproduced signal is supplied to the data expansion circuit **400**. In the data expansion circuit **400**, a signal processing reverse to the data compression processing upon recording is performed so that the signal is restored to the original signal. Thereby, the original transmission rate is restored. The data-expanded reproduction signal is sent to the D/A converter **420** on one hand to be outputted as an analog video signal from the output terminal **431** after D/A conversion and is sent to the output terminal **432** on the other hand to be outputted as a digital video signal therefrom.

Next, explanation will be made of the high-speed reproduction. The servo control circuit **360** controls the cylinder motor and the capstan motor so that a predetermined cylinder rotation speed and a predetermined tape speed adapted for the high-speed reproduction are provided. A signal reproduced by the magnetic heads **372** and **372'** is inputted to the reproducing system signal processing circuit **380**. In the reproducing system signal processing circuit **380**, a signal processing such as demodulation for reproduction, channel synthesis, error detection and error correction is performed at a predetermined processing clocks adapted for the high-speed reproduction. Thereafter, the high-speed reproduction signal is supplied to the terminal **390***a* of the change-over circuit **390**. In the change-over circuit **390**, a change-over to connect the terminal **390***a* and a terminal **390***b* is made upon high-speed reproduction. Thereby, the high-speed digital video signal is outputted from the output terminal **433**.

A furthermore embodiment of the present invention will be explained by use of FIG. **9**. The construction of the present embodiment is similar to that of the embodiment shown in FIG. **7** but is different therefrom in that the change-over circuit **340** is placed at a different position, the change-over circuit **390** used in FIG. **7** is eliminated and a change-over circuit **345** is newly added.

An input/output signal upon standard-speed recording/reproduction in the present embodiment is the same as that in the embodiment shown in FIG. **7**. As for high-speed recording and high-speed reproduction, however, the present embodiment is different from the embodiment of FIG. **7** in that the transmission of a high-speed digital video signal is made in the form of a recording format. Accordingly, upon high-speed recording, the high-speed digital video signal is not passed through a recording system signal processing circuit **350** but is recorded onto a tape through the change-over circuit **340** as it is. Upon high-speed reproduction, a reproduced signal is subjected to a signal processing for reproduction such as error detection and error correction by a reproducing system signal processing circuit **380** and is thereafter inputted to a terminal **345***b* of the change-over circuit **345**. The signal supplied through the change-over circuit **345** to the recording system side signal processing circuit **350** is subjected to a signal processing for recording such as addition of error correction code and modulation for recording by the signal processing circuit **350** to form a recording format and is thereafter outputted as a high-speed digital video signal from an output terminal **433**.

The embodiments shown in FIGS. **7** and **9** have feature that high-speed recording and high-speed reproduction are possible. The best use of this feature can be made for dubbing or data communication with the result of effective shortening of a dubbing time, a data communication time or a data circuit line occupation time. Also, though those embodiments have been mentioned in conjunction with an example in which all of standard-speed recording, high-speed recording, standard-speed reproduction and high-speed reproduction modes are involved, it is not necessarily required to implement all of those modes. There may be considered an example in which only a necessary mode is provided in compliance with the purpose of use. FIG. **10** shows an embodiment in which a high-speed recording function is provided as a recording mode and at least a high-speed reproduction function is provided as a reproduction mode. Also, there may be considered an embodiment as a system for the exclusive use for reproduction in which at least a high-speed reproduction function is provided, as shown in FIG. **11**. Further, FIG. **12** shows an embodiment in which a high-speed recording function is provided as a recording mode and a standard-speed reproduction function is provided as a reproduction mode.

FIG. **13** is a block diagram of one example of the magnetic recording/reproducing system of the embodiment of FIG. **7** for explaining processings subsequent to the compression processing. In FIG. **13**, reference numeral **201** denotes a synchronization detection circuit, numeral **204** a recording modulation circuit, numeral **205** a cylinder servo control circuit, numeral **206** a capstan servo (or tape speed) control circuit, numeral **207** a reproduction reference signal generation circuit, numeral **210** a demodulation circuit, numeral **211** a cylinder, numeral **212** a pair of recording heads, numeral **213** a pair of reproducing heads, numeral **214** a capstan which controls the tape speed, numeral **215** a magnetic tape, numeral **216** a delivery reel, and numeral **217** a take-up reel. FIG. **14** is a timing chart of input and output signals in the example shown in FIG. **13** and schematically illustrate a compressed picture signal **251** which is an input signal, a synchronizing signal **252** of the picture signal, a standard-

speed reproduction signal **255** which is an output signal, and a reproduction synchronizing signal **256**.

In the shown example, n-tuple speed recording is realized by making a tape speed and a cylinder rotation speed upon recording n times as high as those upon standard-speed reproduction. As shown in FIG. **14**, the compressed video signal as an input signal of the circuit shown in FIG. **13** and the synchronizing signal include information **251** for n pictures and n synchronizing pulses **252** synchronous therewith in a time when one picture is reproduced at a standard speed. The picture information is converted into a predetermined recording format by the recording modulation circuit **204** and is recorded onto the magnetic tape **215** by the recording heads **212**. At this time, a synchronizing signal for the cylinder servo control circuit **205** and the capstan-servo control circuit **206** is increased by n times in compliance with the n-tuple speed video signal, as shown by **252** in FIG. **14**, so that the rotation speed of the cylinder **211** and the feed speed of the magnetic tape **215** are increased by n times. Thereby, the recording onto the tape can be made with the quite same recording format as that in the case of the standard-speed recording. Upon reproduction, a synchronizing signal for the cylinder servo control circuit **205** and the capstan servo control circuit **206** is supplied from the reproduction reference signal generation circuit **207** to restore the cylinder rotation speed and the tape feed speed to those upon standard-speed reproduction, and a signal read by the reproducing heads **213** is demodulated by the demodulation circuit **210** and is outputted therefrom. In the circuit shown in FIG. **13**, if the input video signal and the synchronizing signal are ones of standard speed, standard-speed recording is possible. Also, n-tuple speed reproduction is possible if the frequency of an output signal from the reproduction reference signal generation circuit is increased by n times.

FIG. **15** is a block diagram of another example of the magnetic recording/reproducing system of the embodiment of FIG. **7** for explaining processings subsequent to the compression processing. FIG. **16** is a timing chart of input and output signals in the example shown in FIG. **15**. In FIG. **15**, the same reference numerals as those used in FIG. **13** denote the same or equivalent components as or to those shown in FIG. **13**. In FIG. **15**, reference numeral **202** denotes a ÷m circuit, numeral **203** recording system memories, numeral **208** a ÷m circuit, and numeral **209** reproducing system memories. In FIG. **16**, the same reference numerals as those used in FIG. **14** denote the same or equivalent signals as or to those shown in FIG. **14**. In FIG. **16**, reference numeral **253** denotes outputs of the recording system memories **203** and numeral **254** denotes an output of the ÷m circuit **208** or a synchronizing signal divided by m.

The embodiment shown in FIG. **15** is an example in which m pairs of recording heads are used to simultaneously record magnetic signals for m pictures on m tracks, thereby realizing high-speed recording while suppressing an increase in the cylinder rotation speed. Upon reproduction, m pairs of reproducing heads are used. Though FIG. **15** shows the case where two pairs of recording heads **212** are used to simultaneously record information for two pictures on two tracks, three or more pairs of heads can be used in a similar manner.

FIG. **17** is a table showing some examples of the tape speed and the cylinder rotation speed (rpm) in the embodiments shown in FIGS. **13** and **15**. In the table, high-speed recording or reproduction at a speed ten times as high as the standard speed is shown by way of example. Design for implementing another high-speed recording or reproduction is similarly possible. In the table shown in FIG. **17**, examples ①, ② and ③ correspond to the embodiment shown in FIG. **13** and examples ④ and ⑤ correspond to the embodiment shown in FIG. **15**.

A still furthermore embodiment of a digital signal recording/reproducing system of the present invention will be explained by use of a block diagram shown in FIG. **18**.

In FIG. **18**, reference numeral **501** denotes a signal input terminal to which a plurality of video signals are inputted in a time-division multiplex form, numeral **502** a recording selection signal-input terminal to which a recording selection signal for selecting one or plural signals to be recorded from the multiplexed input signal is inputted, numeral **503** a recording signal selection circuit for selecting the signals to be recorded from the multiplexed input signal in accordance with the recording selection signal from the input terminal **502**, numeral **504** a recording signal processing circuit for subjecting the selected signals to a digital processing for recording onto a recording medium, numerals **505** and **505'** magnetic heads, numeral **506** a rotating drum, numeral **507** a magnetic tape or the recording medium, numeral **508** a servo circuit for controlling the rotation of the drum **506** and the travel of the tape **507**, numeral **511** a reproduction selection signal input terminal to which a reproduction selection signal for selecting one or plural signals to be outputted as a reproduction signal from among the multiple-recorded and reproduced signals is inputted, numeral **509** a reproduction signal selection circuit for selecting the signals to be outputted as a reproduction signal from among the multiple-recorded and reproduced signals in accordance with the reproduction selection signal from the input terminal **511**, numeral **510** a reproduction signal processing circuit for subjecting the selected signals to a digital processing, and numeral **512** a reproduction signal output terminal.

The time-division multiplexed input video signal from the signal input terminal **501** is supplied to the recording signal selection circuit **503**. The recording signal selection circuit **503** is also supplied with the recording selection signal from the recording selection signal input terminal **502** to make the selection of signals to be recorded. For example, in the case where six kinds of video signals A, B, C, D, E and F are inputted in a time-division multiplex form as shown in (a) of FIG. **19** and four signals A, B, C and D thereof are to be selected and recorded, an output of the recording signal selection circuit **503** is as shown in (b) of FIG. **19**. Such an output signal of the recording signal selection circuit **503** is inputted to the recording signal processing circuit **504** which in turn performs a signal processing for recording such as addition of error correction code. Also, the recording signal selection circuit **503** produces a speed control signal on the basis of the number of signals in the time-division multiplexed input video signal, the transmission rate of the input signal and the number of signals to be recorded which are selected by the recording selection signal. The speed control signal is supplied to the recording signal processing circuit **504** and the servo circuit **508**. For example, in the case where the input video signal is time-division multiplexed to sextuplet with each of six signals in the multiplexed input signal being transmitted at a rate time-base compressed to ⅙ and four signals among the six signals in the multiplexed input signal are to be selectively recorded, a signal indicative of a quadruple speed is produced as the speed control signal. Also, in the case where the input video signal is time-division multiplexed to sextuplet with each of six signals in the multiplexed input signal being transmitted at a rate time-base compressed to 1/12 and four signals among the six signals in the multiplexed input signal are to be selectively recorded, a signal indicative of a octuple speed is produced as the speed control

signal. Namely, in the case where an input signal is multiplexed to N-plet, the compression rate of each of the N signals in the multiplexed input signal is 1/K and the number of signals to be selectively recorded is L, a speed control signal indicative of an (L×K)/N-tuple speed is produced. The operating speed of the recording signal processing circuit **504** which processes a signal from the recording signal selection circuit **503**, is changed in accordance with the speed control signal. For example, in the case of a speed control signal indicative of a quadruple speed, the recording signal processing circuit **504** performs a signal processing at a speed four times as high as a normal speed and supplies the processed signal to the magnetic heads **505** and **505'**. Here, for example, in the case where the input video signal is time-division multiplexed to sextuplet with each of the six signals in the multiplexed input signal being transmitted at a rate time-base compressed to ⅙ and a speed control signal indicative of a quadruple speed is used to selectively record four signals from among the six signals, the speed of an input signal inputted to the recording signal processing circuit **504** is four times as high as that of one video signal having a normal speed and the recording signal processing circuit **504** processes this quadruple-speed input signal at a quadruple speed and supplies the processed signal to the magnetic heads, thereby making it possible to record all of the four selected signals. Also, if the recording signal selection circuit **503** is constructed so that signals to be selectively recorded are sequentially changed for every one track on the tape, compatibility can be held in regard to the number of signals to be selectively recorded and a processing speed by causing the recording signal processing circuit **504** to perform a completed processing for every one track. In the following, explanation will be made in conjunction with the case where each video signal is recorded in such a form completed for every track. However, it should be noted in advance that the present invention is applicable to another recording system, for example, a system in which signals are recorded in a form changed for every pixel, line or field. On the other hand, the servo circuit **508** supplied with the speed control signal indicative of the quadruple speed controls the rotation speed of the rotating drum **506** so that it becomes four times as high as a normal speed and the travel speed of the magnetic tape **507** so that it becomes four times as high as a normal speed. Thereby, four signals A, B, C and D are alternately recorded on successive tracks of the magnetic tape **507**, as shown in FIG. **20**. According to the control mentioned above, the pattern of recording tracks on the tape becomes the same irrespective of the number of signals in the multiplexed input signal, the transmission rate of each signal and the number of signals to be selectively recorded. In order to make a control upon reproduction easy, it is preferable that the number of selectively recorded signals and the identification codes or signal numbers thereof (for example, A, B, C and D or 0, 1, 2 and 3) are recorded as an ID signal for every track.

In the above example, the recording of the time-division multiplexed signal has been mentioned. However, it is needless to say that the present invention is also applicable to the case where the number of multipet signal components in an input video signal is 1 or the input video signal is not multiplexed. In such a case, since the recording signal processing circuit **504** and the servo circuit **508** operate at speeds proportional to the transmission rate of the input video signal, an effect is manifested, for example, in high-speed dubbing. As apparent from the foregoing explanation of the operation, it is of course that a multiplexed signal can be recorded at a high speed.

Upon reproduction, a signal reproduced from the magnetic tape **507** by the magnetic heads **505** and **505'** mounted on the rotating drum **506** is inputted to the reproduction signal selection circuit **509**. The reproduction signal selection circuit **509** produces a speed control signal, for example, by detecting the number of multiple-recorded signals from the ID signal included in the reproduced signal and sends the speed control signal to the servo circuit **508**. The speed control signal is a signal indicative of a speed four times as high as the normal reproduction speed in the case where the number of multiple-recorded signals is 4 and a signal indicative of a sextuple speed in the case where it is 6. In the case of the quadruple speed, the servo control circuit **508** supplied with the speed control signal indicative of the quadruple speed controls the rotation speed of the rotating drum **506** so that it becomes four times as high as a normal speed and the travel speed of the magnetic tape **7** so that it becomes four times as high as a normal speed. Thereby, there can be traced all of signals recorded so that the recording track pattern on the tape becomes the same irrespective of the number of signals to be selectively recorded. In a system which has not a signal indicative of the number of selectively recorded signals, there may be employed a method in which the speed control signal is manually set. In a system in which the number of signals to be recorded on the tape is fixed, the speed control signal has a fixed value. The reproduction signal selection circuit **509** receives a reproduction selection signal inputted from the reproduction selection signal input terminal **511** to select a desired signal(s) from among the signals reproduced by the magnetic heads **505** and **505'** and to output the selected signal as a reproduction signal to the reproduction signal processing circuit **510**. The reproduction signal selection circuit **509** also outputs a selection number signal indicative of the number of selected signals to the reproduction signal processing circuit **510**.

The reproduction signal processing circuit **510** performs a signal processing such as code error correction processing and picture signal processing for the reproduction signal at a processing speed corresponding, to the selection number signal and outputs the processed reproduction signal from the output terminal **512**. For example, in the case where the number indicated by the selection number signal is 2, the signal processing speed is two times as high as a normal speed and various processings are performed for each selected signal. For example, in the case where signals A and C are selected, the signals A and C are outputted alternately for each field. In the case where the number indicated by the selection number signal is 1, for example, when the reproduction selection signal from the reproduction selection signal input terminal **511** selects only the signal C, the reproduction signal processing circuit **510** performs the signal processing at the normal speed to output the signal as reproduced at a normal speed. As apparent from the above, the present embodiment makes it possible to simultaneously record any number of signals selected from among a plurality of signals in a multiplexed video signal and to simultaneously reproduce any number of signals from among the recorded signals.

In the case where a plurality of signals are simultaneously reproduced, a construction for outputting the reproduced signals from separate output terminals simultaneously and in parallel may be employed, particularly, in the case of an analog output, as a method other than the construction in which the plurality of reproduced signals are outputted in a time-division multiplex form, as mentioned above. Though in the above-mentioned example the reproduction signal is outputted at a reproduction speed for a usual video signal, the transmission rate of the reproduction signal may be made

higher than the reproduction speed for the usual video signal in order to transmit the reproduction signal to another system in an analog or digital signal form at a high rate or to perform high-speed dubbing which is one of effects of the present embodiment. This can be realized in such a manner that the fundamental operating speed of there producing system is set to be higher than a normal reproduction speed and the operating speeds of the servo circuit **508**, the reproduction signal selection circuit **509** and the reproduction signal processing circuit **510** are changed in accordance with the number of multiple-recorded signals and/or the number of signals to be outputted as a reproduction signal with the above fundamental speed being the standard. If the transmission rate of a reproduction signal is made variable so that a rate adapted for a transmission path to which the reproduction signal is to be connected or the performance or function of a recorder by which the reproduction signal is to be recorded, can be selected.

As mentioned above, according to the present embodiment, it is possible to simultaneously record any number of signals selected from among a plurality of signals in a multiplexed video signal and to reproduce any number of signals from among the recorded signals at any speed. Also, in the case where a plurality of signals are selected and reproduced and the plurality of reproduced signals are simultaneously outputted in a time-division multiplex form or from separate output terminals in parallel, it is possible to arbitrarily set the transmission rate of an output signal.

The present embodiment has been explained in conjunction with the case where the present invention is applied to a helical-scan digital-recording VTR. It is of course that a similar effect can be obtained in the case where the present invention is applied to a fixed head VTR. The fixed head system is convenient for the structuring of a system since it has a higher degree of freedom for the setting of the units of division of a signal subjected to time-division multiple recording as compared with the helical scan system. Also, it is of course that the present invention is applicable to a recording/reproducing equipment other than the VTR or is applicable to a digital signal processing and analog recording system.

The present invention can be applied to not only the case where an input signal is time-division multiplexed, as mentioned above, but also the case where a plurality of signals are inputted simultaneously and in parallel. In the latter case, the recording signal selection circuit **503** is constructed to receive the input signals in parallel.

As has been mentioned in the foregoing, according to the present invention, it is possible to realize a digital VTR in which high-speed recording onto a tape can be made with the same format as that used in standard-speed reproduction. Further, there can be realized a transmission signal processing for transmitting at a high rate a video signal to be recorded by such a digital VTR. Also, in the case where a signal transmitted from the transmission signal processing system is to be recorded by a multiplicity of VTR's, it is possible to designate those ones of the multiplicity of VTR's by which recording is to be made and to make a control of the start/stop of recording.

What is claimed is:

1. A digital information receiving apparatus, comprising:

a receiver configured to receive digital information from a transmission path, wherein the digital information includes video information bit-compressed by a first compression method, audio information bit-compressed by a second compression method which is different from the first compression method, and error detection information added to the video information and separately added to the audio information, respectively;

a demodulator configured to demodulate the digital information received by the receiver;

an error detector configured to detect an error which occurs in the transmission path of the digital information demodulated by the demodulator based on the error detection information, the error being the error which occurs in the transmission path having no recording process of the digital information therein;

a first expander configured to bit-expand the video information of the digital information error detected by the error detector in accordance with a first expansion method corresponding to the first compression method; and

a second expander configured to bit-expand the audio information of the digital information error detected by the error detector in accordance with a second expansion method corresponding to the second compression method.

2. A digital information receiving apparatus, according to claim **1**, wherein the first compression method utilizes a discrete cosine transform.

3. A digital information receiving apparatus, comprising;

a receiver configured to receive digital information from a transmission path, wherein the digital information includes video information bit-compressed by a first compression method, audio information bit-compressed by a second compression method which is different from the first compression method, and error correction information added to the video information and separately added to the audio information, respectively;

a demodulator configured to demodulate the digital information received by the receiver;

an error corrector configured to correct an error which occurs in the transmission path of the digital information demodulated by the demodulator based on the error correction information, the error being the error which occurs in the transmission path having no recording process of the digital information therein;

a first expander configured to bit-expand the video information of the digital information error corrected by the error corrector in accordance with a first expansion method corresponding to the first compression method; and

a second expander configured to bit-expand the audio information of the digital information error corrected by the error corrector in accordance with a second expansion method corresponding to the second compression method.

4. A digital information receiving apparatus, according to claim **3**, wherein the first compression method utilizes a discrete cosine transform.

5. A digital information receiving and recording apparatus comprising:

a receiver configured to receive digital information from a transmission path, wherein the digital information includes video information bit-compressed by a first compression method, audio information bit-compressed by a second compression method which is different from the first compression method, and transmission error correction information added to the video information and separately added to the audio information, respectively;

an error corrector configured to correct an error of the digital information received by the receiver based on the transmission error correction information, the error

being the error which occurs in the transmission path having no recording process of the digital information therein;

a record error correction information adder configured to add record error correction information to the video information and the audio information error corrected by the error corrector, the record error correction information being different from the transmission error correction information; and

a recorder configured to record the digital information added the record correction information by the record error correction information adder to the recording medium.

6. A digital information receiving and recording apparatus, according to claim **5**, wherein the first compression method utilizes a discrete cosine transform.

7. A method for receiving digital information of a digital information receiving apparatus, comprising the steps of:

receiving the digital information from a transmission path, wherein the digital information includes video information bit-compressed by a first compression method, audio information bit-compressed by a second compression method which is different from the first compression method, and error detection information added to the video information and separately added to the audio information, respectively;

demodulating the digital information received by the receiving step;

detecting an error of the digital information demodulated by the demodulating step based on the error detection information, the error being the error which occurs in the transmission path having no recording process of the digital information therein;

bit-expanding the video information of the digital information error detected by the error detecting step in accordance with a first expansion method corresponding to the first compression method; and

bit-expanding the audio information of the digital information error detected by the error detecting step in accordance with a second expansion method corresponding to the second compression method.

8. A method for receiving digital information of a digital information receiving apparatus, according to claim **7**, wherein the first compression method utilizes a discrete cosine transform.

9. A method for receiving a digital information of a digital information receiving apparatus, comprising the steps of:

receiving digital information from a transmission path, wherein the digital information includes video information bit-compressed by a first compression method, audio information bit-compressed by a second compression method which is different from the first compression method, and error correction information added to the video information and separately added to the audio information, respectively;

demodulating the digital information received by the receiving step;

correcting an error of the digital information demodulated by the demodulating step based on the error correction information, the error being the error which occurs in the transmission path having no recording process of the digital information therein;

bit-expanding the video information of the digital information by the error correcting step in accordance with a first expansion method corresponding to the first compression method; and

bit-expanding the audio information of the digital information error corrected by the error correcting step in accordance with a second expansion method corresponding to the second compression method.

10. A method for receiving a digital information of a digital information receiving apparatus, according to claim **9**, wherein the first compression method utilizes a discrete cosine transform.

11. A method for receiving a digital information of a digital information receiving apparatus, comprising the steps of:

receiving digital information from a transmission path, wherein the digital information includes video information bit-compressed by a first compression method, audio information bit-compressed by a second compression method which is different from the first compression method, and transmission error correction information added to the video information and separately added to the audio information, respectively;

correcting an error of the digital information received by the receiving step based on the transmission error correction information, the error being the error which occurs in the transmission path having no recording process of the digital information therein;

adding record error correction information to the video information and the audio information error corrected by the error correcting step, the record error correction information being different from the transmission error correction information; and

recording the digital information having the record correction information added by the adding step to the recording medium.

12. A method for receiving a digital information of a digital information receiving apparatus, according to claim **11**, wherein the first compression method utilizes a discrete cosine transform.

13. A digital information receiving apparatus, comprising:

receiving means for receiving digital information from a transmission path, wherein the digital information includes video information bit-compressed by a first compression method, audio information bit-compressed by a second compression method which is different from the first compression method, and error detection information added to the video information and separately added to the audio information, respectively;

demodulating means for demodulating the digital information received by the receiving means;

error detecting means for detecting an error of the digital information demodulated by the demodulating means based on the error detection information, the error being the error which occurs in the transmission path having no recording process of the digital information therein;

first expanding means for bit-expanding the video information of the digital information error detected by the error detecting means in accordance with a first expansion method corresponding to the first compression method; and

second expanding means for bit-expanding the audio information of the digital information error detected by the error detecting means in accordance with a second expansion method corresponding to the second compression method.

14. A digital information receiving apparatus, according to claim **13**, wherein the first compression method utilizes a discrete cosine transform.

15. A digital information receiving apparatus, comprising;

receiving means for receiving digital information from a transmission path, wherein the digital information

includes video information bit-compressed by a first compression method, audio information bit-compressed by a second compression method which is different from the first compression method, and error correction information added to the video information and separately added to the audio information, respectively;

demodulating means for demodulating the digital information received by the receiving means;

error correcting means for correcting an error of the digital information demodulated by the demodulating means based on the error correction information, the error being the error which occurs in the transmission path having no recording process of the digital information therein;

first expanding means for bit-expanding the video information of the digital information error corrected by the error correcting means in accordance with a first expansion method corresponding to the first compression method; and

second expanding means for bit-expanding the audio information of the digital information error corrected by the error correcting means in accordance with a second expansion method corresponding to the second compression method.

16. A digital information receiving apparatus, according to claim **15**, wherein the first compression method utilizes a discrete cosine transform.

17. A digital information receiving apparatus, comprising:

a receiver configured to receive digital information from a transmission path, wherein the digital information includes video information bit-compressed by a first compression method, audio information bit-compressed by a second compression method which is different from the first compression method, and error detection information added to the video information and separately added to the audio information, respectively;

a demodulator configured to demodulate a digital information which is previously received by the receiver;

an error detector configured to detect an error of a digital information which is previously demodulated by the demodulator based on the error detection information, the error being the error which occurs in the transmission path having no recording process of a digital information therein;

a first expander configured to bit-expand the video information of a digital information which is previously error detected by the error detector in accordance with a first expansion method corresponding to the first compression method; and

a second expander configured to bit-expand the audio information of a digital information which is previously error detected by the error detector in accordance with a second expansion method corresponding to the second compression method.

18. A digital information receiving apparatus, according to claim **17**, wherein the first compression method utilizes a discrete cosine transform.

19. A digital information receiving apparatus, comprising;

a receiver configured to receive digital information from a transmission path, wherein the digital information includes video information bit-compressed by a first compression method, audio information bit-compressed by a second compression method which is different from the first compression method, and error correction information added to the video information and separately added to the audio information, respectively;

a demodulator configured to demodulate a digital information which is previously received by the receiver;

an error corrector configured to correct an error of a digital information which is previously demodulated by the demodulator based on the error correction information, the error being the error which occurs in the transmission path having no recording process of a digital information therein;

a first expander configured to bit-expand the video information of a digital information which is previously error corrected by the error corrector in accordance with a first expansion method corresponding to the first compression method; and

a second expander configured to bit-expand the audio information of a digital information which is previously error corrected by the error corrector in accordance with a second expansion method corresponding to the second compression method.

20. A digital information receiving apparatus, according to claim **19**, wherein the first compression method utilizes a discrete cosine transform.

21. A digital information receiving apparatus, comprising:

receiving means for receiving digital information from a transmission path, wherein the digital information includes video information bit-compressed by a first compression method, audio information bit-compressed by a second compression method which is different from the first compression method, and error detection information added to the video information and separately added to the audio information, respectively;

demodulating means for demodulating a digital information which is previously received by the receiving means;

error detecting means for detecting an error of a digital information which is previously demodulated by the demodulating means based on the error detection information, the error being the error which occurs in the transmission path having no recording process of a digital information therein;

first expanding means for bit-expanding the video information of a digital information which is previously error detected by the error detecting means in accordance with a first expansion method corresponding to the first compression method; and

second expanding means for bit-expanding the audio information of a digital information which is previously error detected by the error detecting means in accordance with a second expansion method corresponding to the second compression method.

22. A digital information receiving apparatus, according to claim **21**, wherein the first compression method utilizes a discrete cosine transform.

23. A digital information receiving apparatus, comprising;

receiving means for receiving digital information from a transmission path, wherein the digital information includes video information bit-compressed by a first compression method, audio information bit-compressed by a second compression method which is different from the first compression method, and error correction information added to the video information and separately added to the audio information, respectively;

demodulating means for demodulating a digital information which is previously received by the receiving means;

error correcting means for correcting an error of a digital information which is previously demodulated by the demodulating means based on the error correction infor-

mation, the error being the error which occurs in the transmission path having no recording process of a digital information therein;

first expanding means for bit-expanding the video information of a digital information which is previously error corrected by the error correcting means in accordance with a first expansion method corresponding to the first compression method; and

second expanding means for bit-expanding the audio information of a digital information which is previously error corrected by the error correcting means in accordance with a second expansion method corresponding to the second compression method.

24. A digital information receiving apparatus, according to claim **23**, wherein the first compression method utilizes a discrete cosine transform.

25. A digital information receiving apparatus, comprising;

a receiver configured to receive digital information transmitted in electric wave form from a transmission path, wherein the digital information includes video information bit-compressed by a first compression method, audio information bit-compressed by a second compression method which is different from the first compression method, and error correction information added to the video information and separately added to the audio information, respectively;

a demodulator configured to demodulate the digital information received by the receiver;

an error corrector configured to correct an error of the digital information demodulated by the demodulator based on the error correction information, the error being the error which occurs in the transmission path having no recording process of the digital information therein;

a first expander configured to bit-expand the video information of the digital information error corrected by the error corrector in accordance with a first expansion method corresponding to the first compression method; and

a second expander configured to bit-expand the audio information of the digital information error corrected by the error corrector in accordance with a second expansion method corresponding to the second compression method.

26. A digital information receiving apparatus, according to claim **25**, wherein the first compression method utilizes a discrete cosine transform.

27. A method for receiving a digital information of a digital information receiving apparatus, comprising the steps of:

receiving digital information transmitted in electric wave form from a transmission path, wherein the digital information includes video information bit-compressed by a first compression method, audio information bit-compressed by a second compression method which is different from the first compression method, and error correction information added to the video information and separately added to the audio information, respectively;

demodulating the digital information received by the receiving step;

correcting an error of the digital information demodulated by the demodulating step based on the error correction information, the error being the error which occurs in the transmission path having no recording process of the digital information therein;

bit-expanding the video information of the digital information by the error correcting step in accordance with a first expansion method corresponding to the first compression method; and

bit-expanding the audio information of the digital information error corrected by the error correcting step in accordance with a second expansion method corresponding to the second compression method.

28. A method for receiving a digital information of a digital information receiving apparatus, according to claim **27**, wherein the first compression method utilizes a discrete cosine transform.

29. A digital information receiving apparatus, comprising;

a receiver configured to receive digital information transmitted in electric wave form from a transmission path, wherein the digital information includes video information bit-compressed by a first compression method, audio information bit-compressed by a second compression method which is different from the first compression method, and error correction information added to the video information and separately added to the audio information, respectively;

a demodulator configured to demodulate a digital information which is previously received by the receiver;

an error corrector configured to correct an error of a digital information which is previously demodulated by the demodulator based on the error correction information, the error being the error which occurs in the transmission path having no recording process of a digital information therein;

a first expander configured to bit-expand the video information of a digital information which is previously error corrected by the error corrector in accordance with a first expansion method corresponding to the first compression method; and

a second expander configured to bit-expand the audio information of a digital information which is previously error corrected by the error corrector in accordance with a second expansion method corresponding to the second compression method.

30. A digital information receiving apparatus, according to claim **29**, wherein the first compression method utilizes a discrete cosine transform.

31. A digital information receiving apparatus, according to claim **1**, further comprising:

a control signal detector configured to detect control signal information generated by a control signal generator.

32. A digital information receiving apparatus, according to claim **31**, further comprising:

a parity addition circuit configured to add parities to the control signal information.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 8,009,375 B2
APPLICATION NO. : 11/305229
DATED : August 30, 2011
INVENTOR(S) : H. Arai et al.

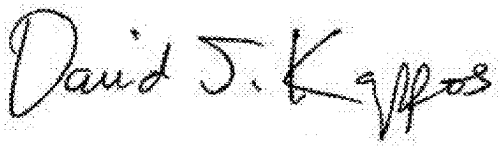
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title Page

Under the head (*) Notice:

Please **delete** the sentence "This patent is subject to a Terminal Disclaimer."

Signed and Sealed this
Eighteenth Day of October, 2011



David J. Kappos
Director of the United States Patent and Trademark Office