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(54) **SEMICONDUCTOR DEVICE HAVING METAL GATE AND MANUFACTURING METHOD THEREOF**

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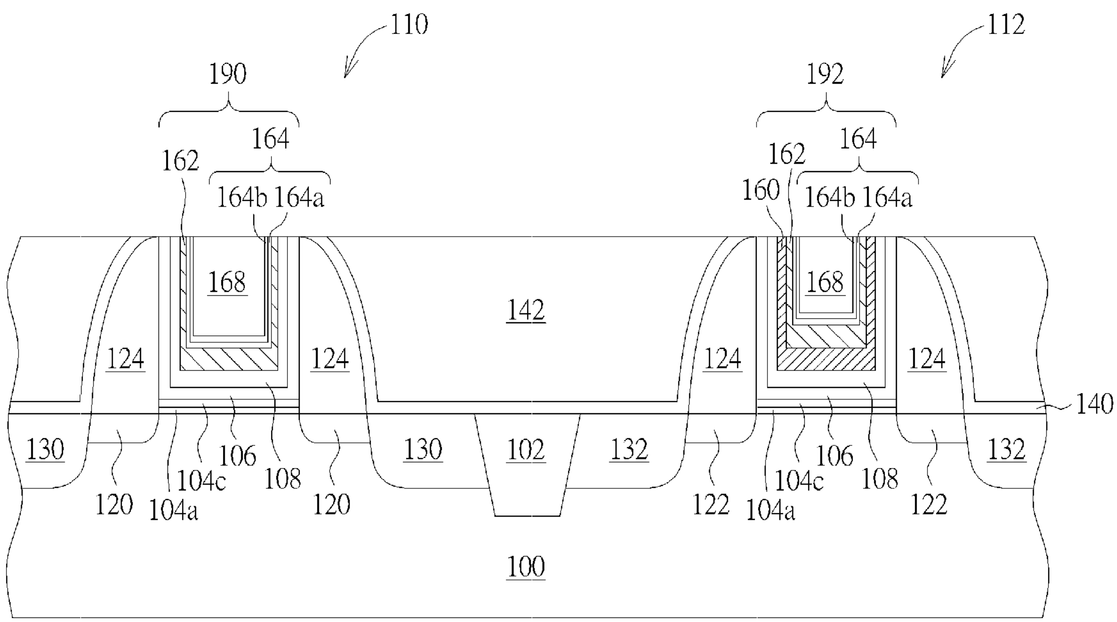
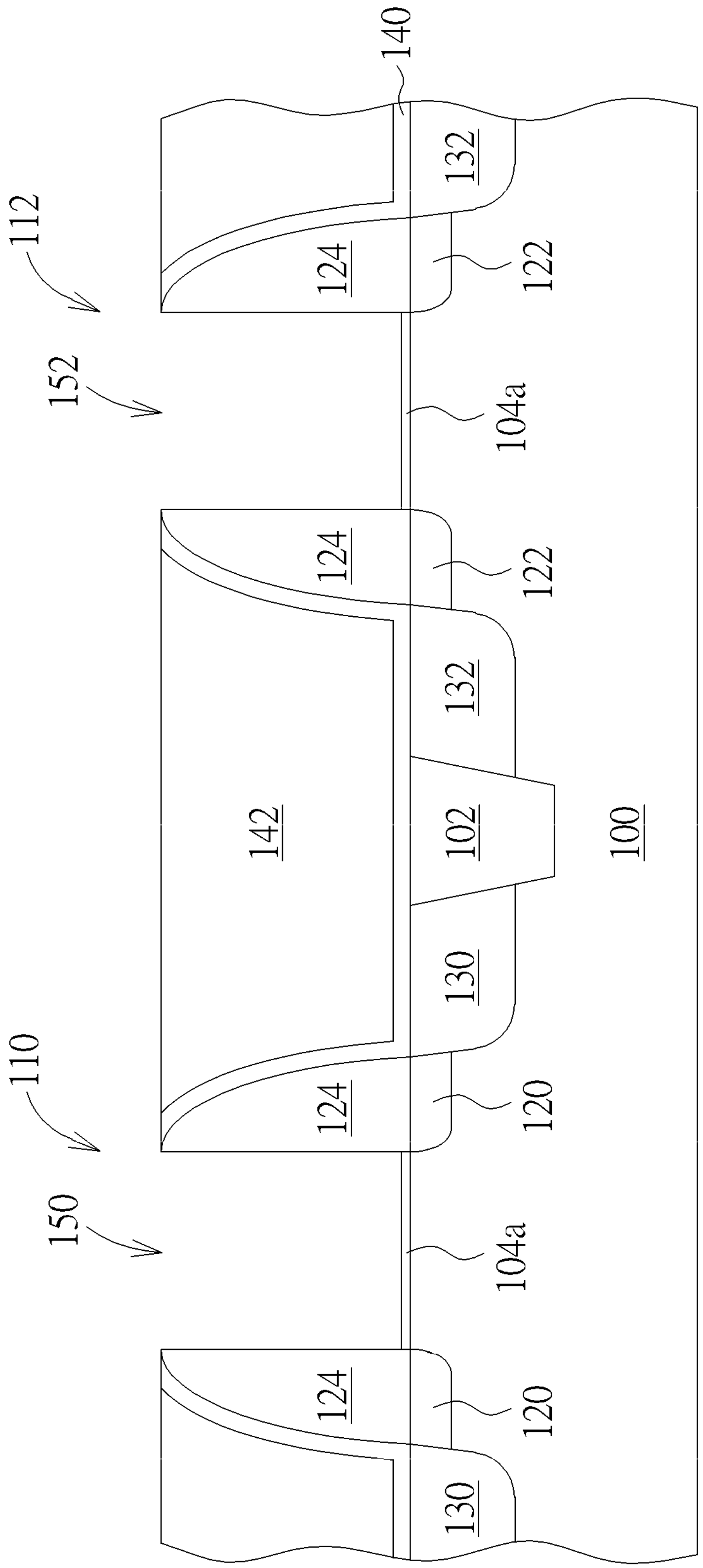
(57) **ABSTRACT**

A method for manufacturing a semiconductor device having metal gate includes following steps. A substrate having at least a first semiconductor device formed thereon is provided. The first semiconductor device includes a first gate trench formed therein. Next, an n-typed work function metal layer is formed in the first gate trench. After forming the n-typed work function metal layer, a nitridation process is performed to form a first protecting layer on the n-typed work function metal layer. After forming the first protecting layer, an oxidation process is performed to the first protecting layer to form a second protecting layer on the n-typed work function metal layer. Then, a gap filling metal layer is formed to fill up the first gate trench.

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112
124
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142
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150
104a
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120
130

FIG. 1

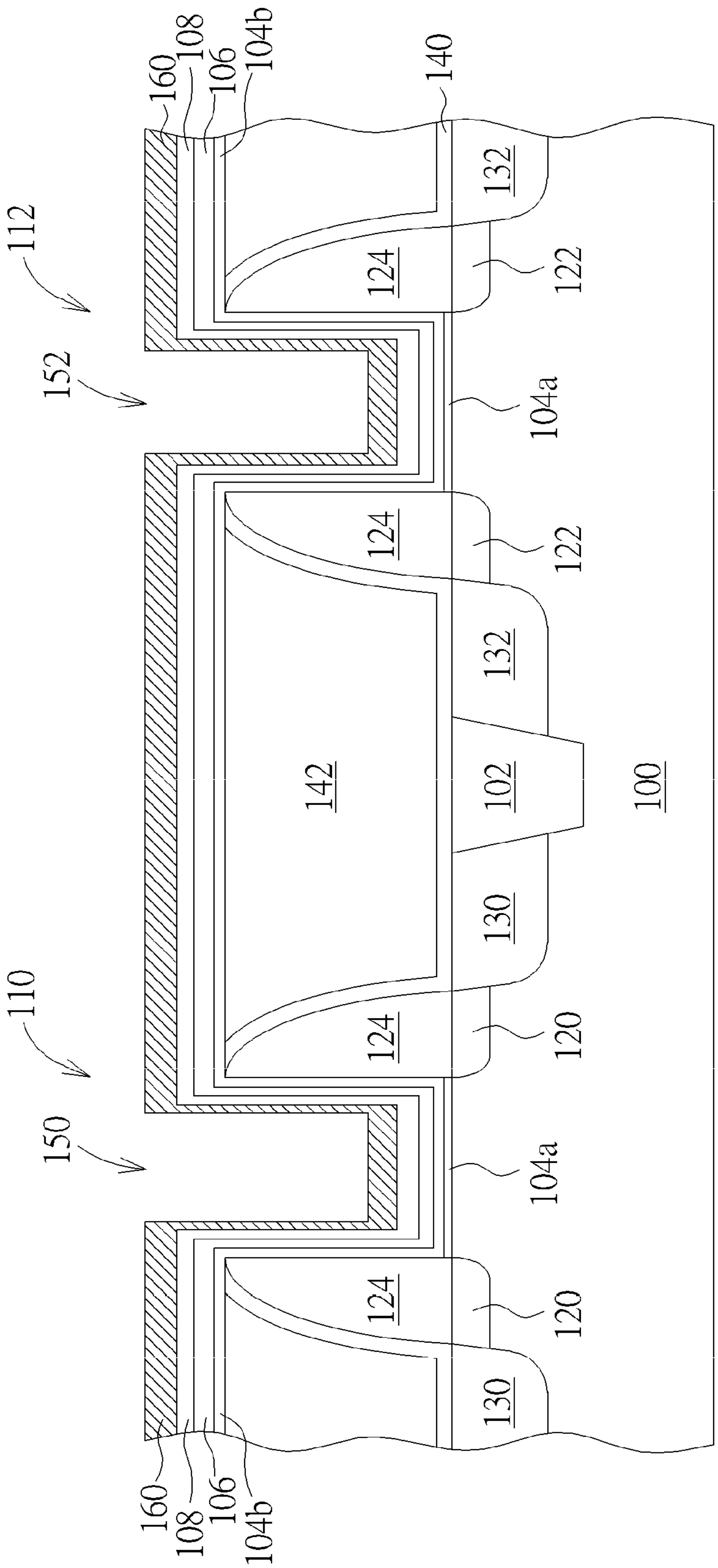
160
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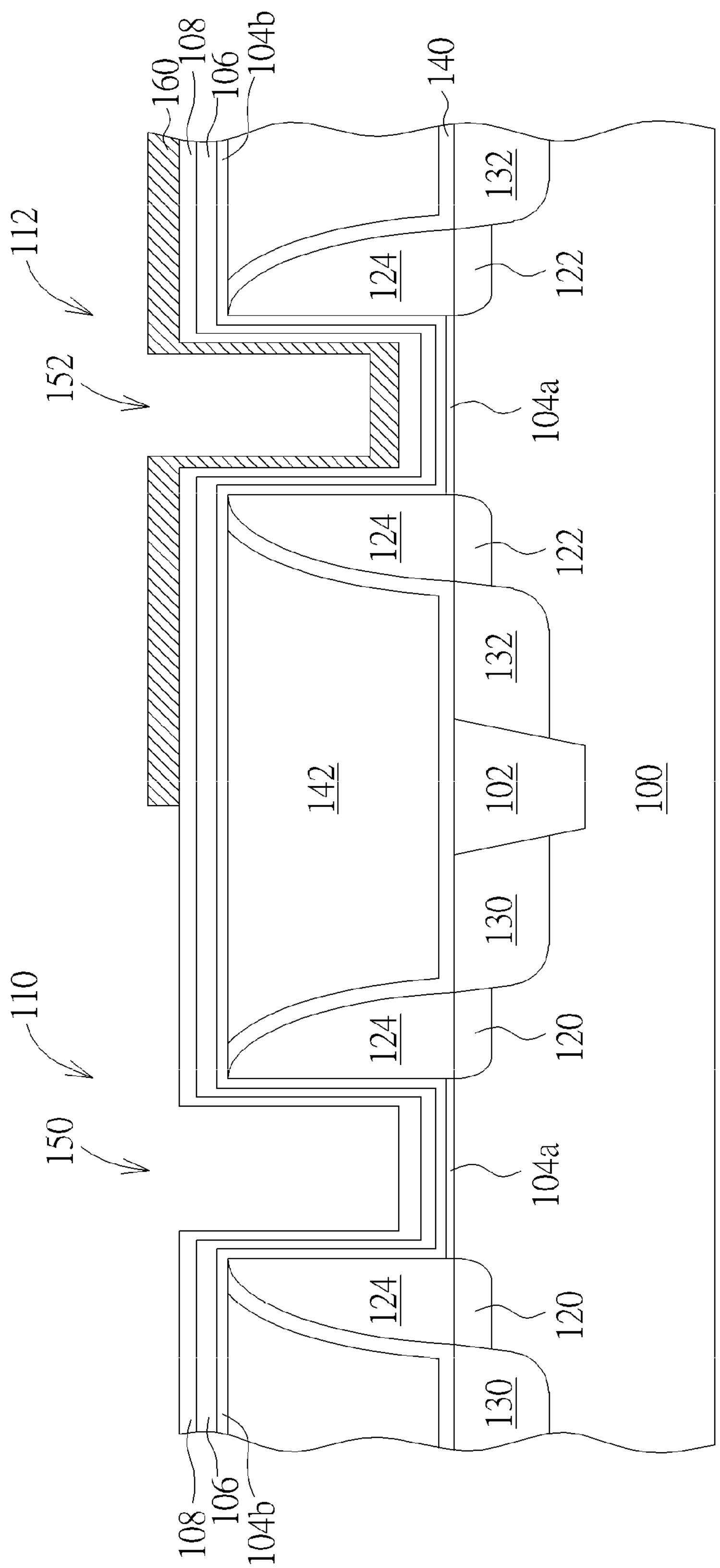
FIG. 2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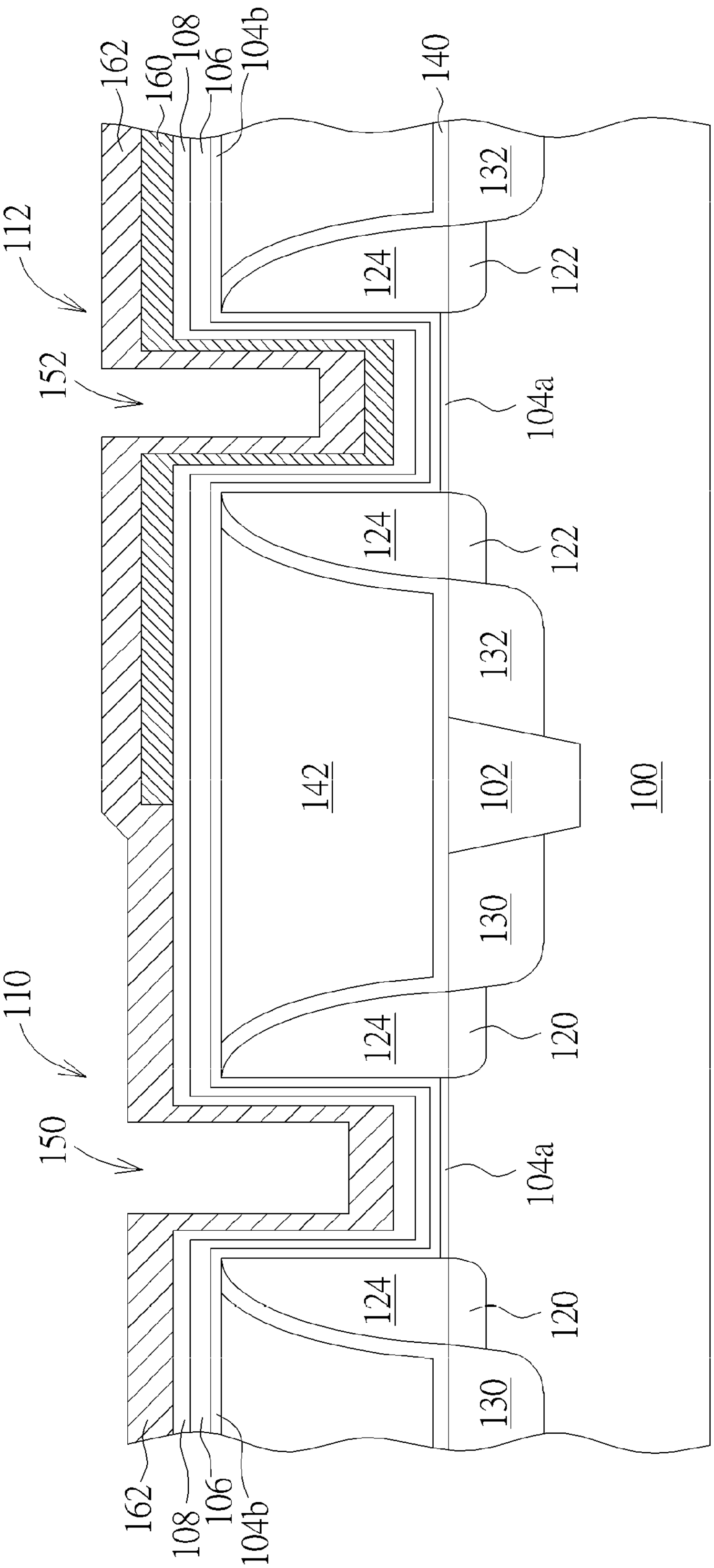
104b

FIG. 3


162
160
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104b
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152
104a
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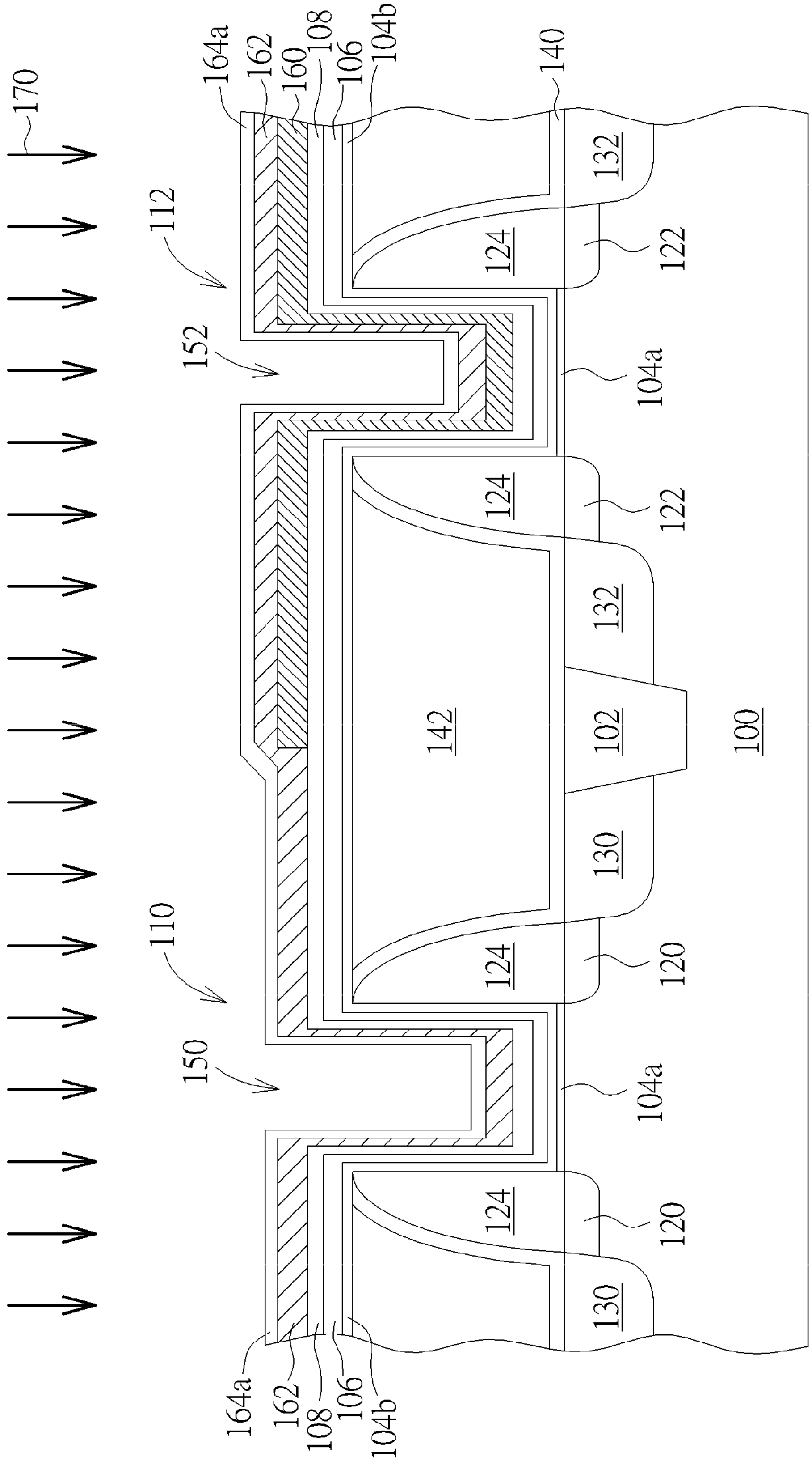
150
120

FIG. 4


170
164a
162
160
108
106
104b
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122
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104a
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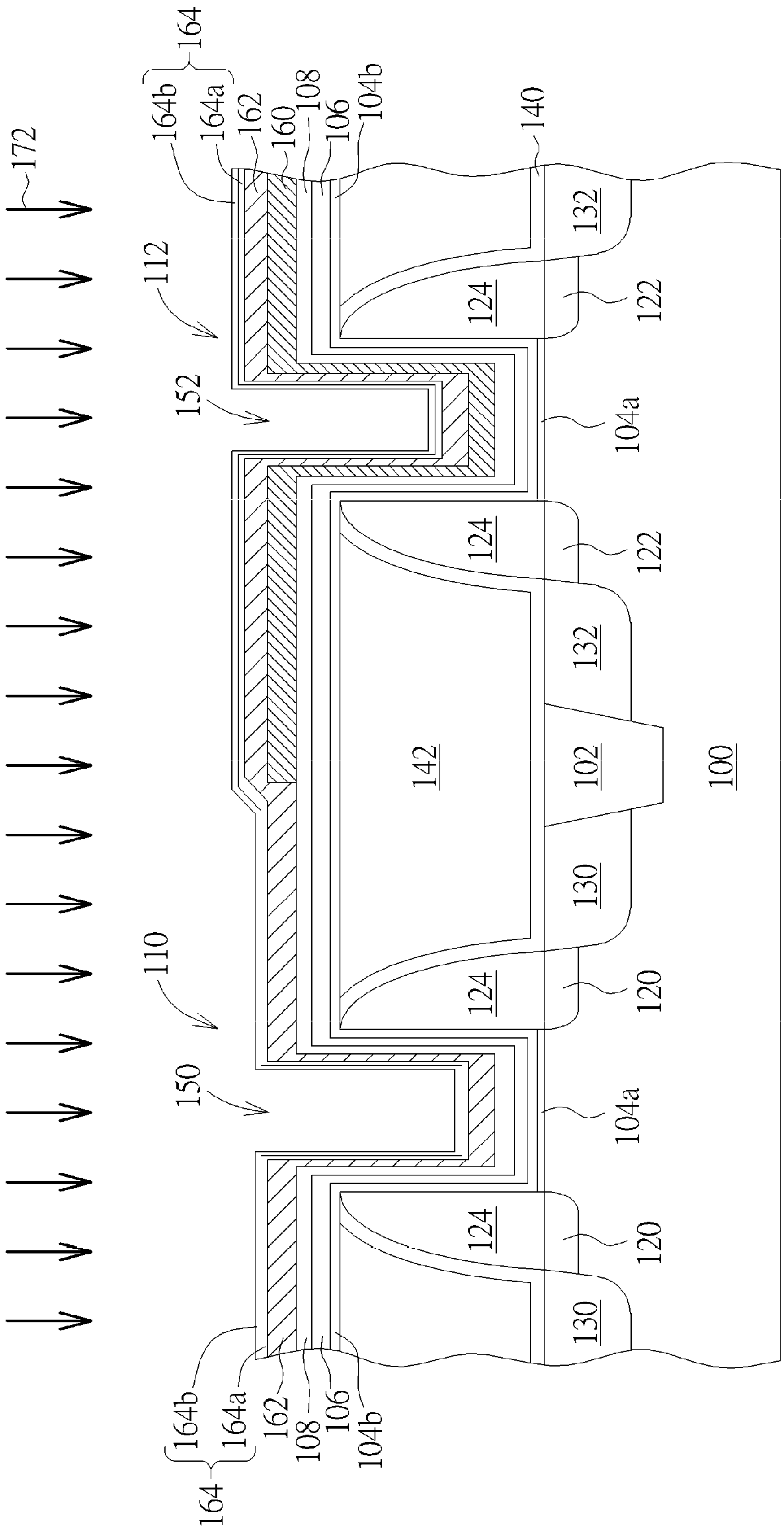
120
110
150

FIG. 5



172
164
164b
164a
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104b
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104a
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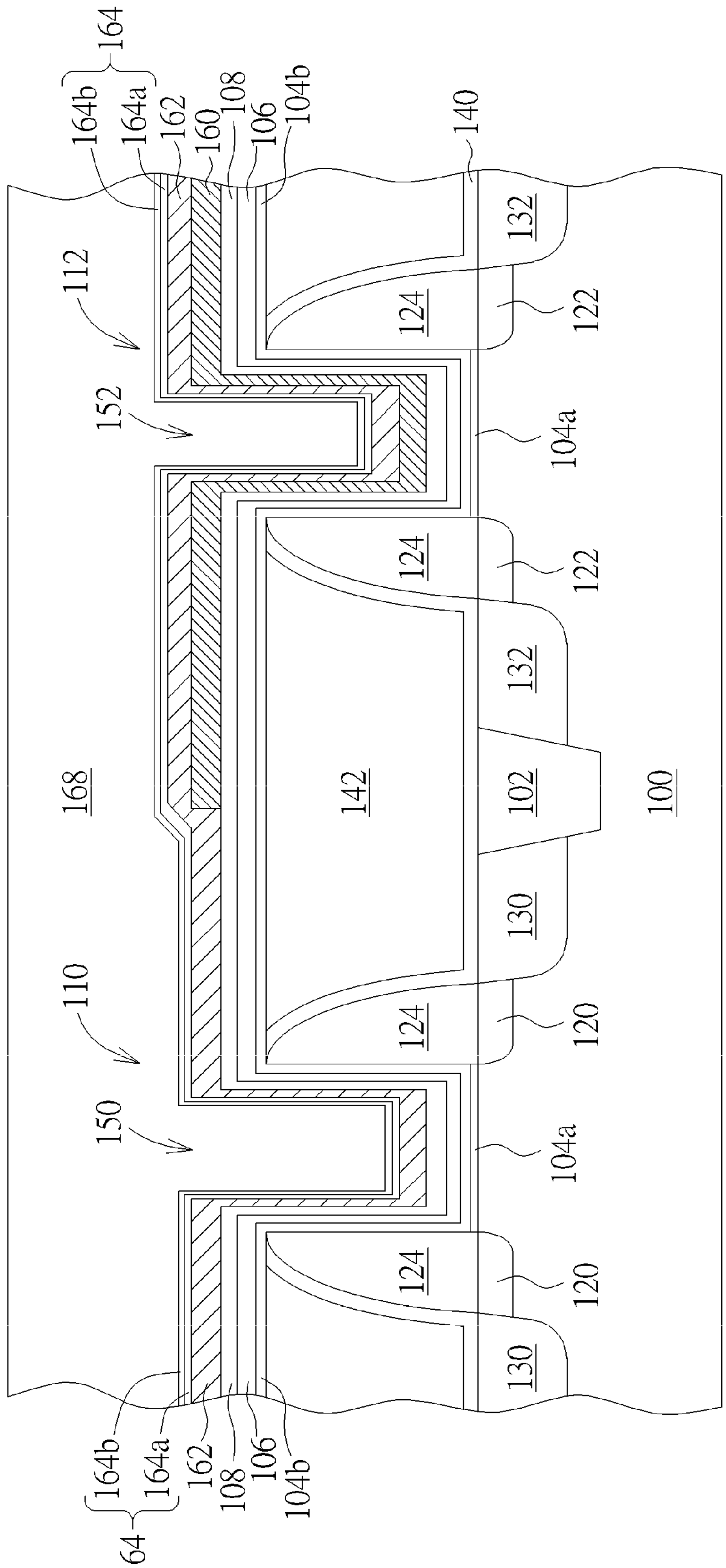
150

FIG. 6


164
164b
164a
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104b
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104a
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168
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150
104a
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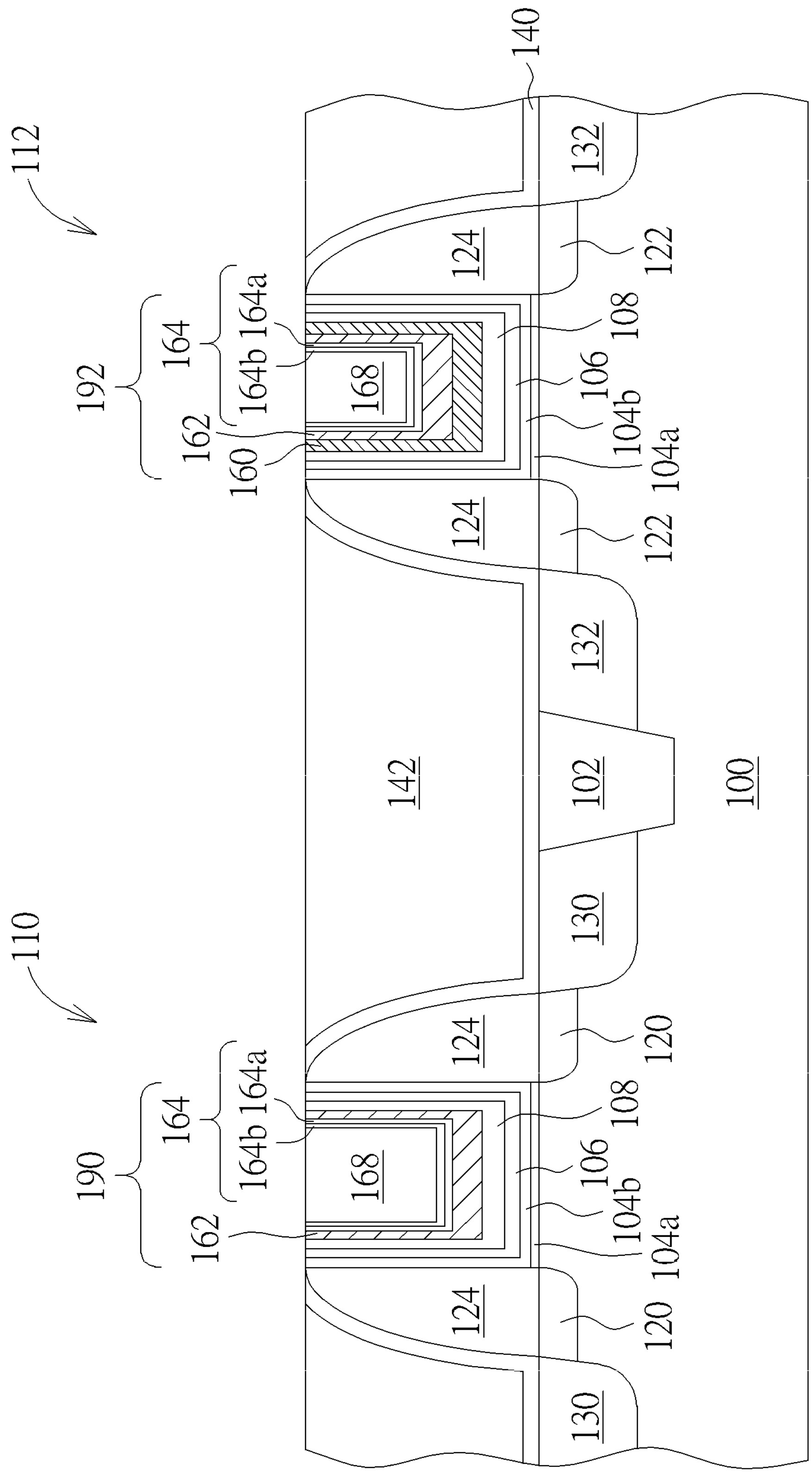
130
164b
164a
162
108
106
104b
164

FIG. 7


112
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164a
164b
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104b
104a
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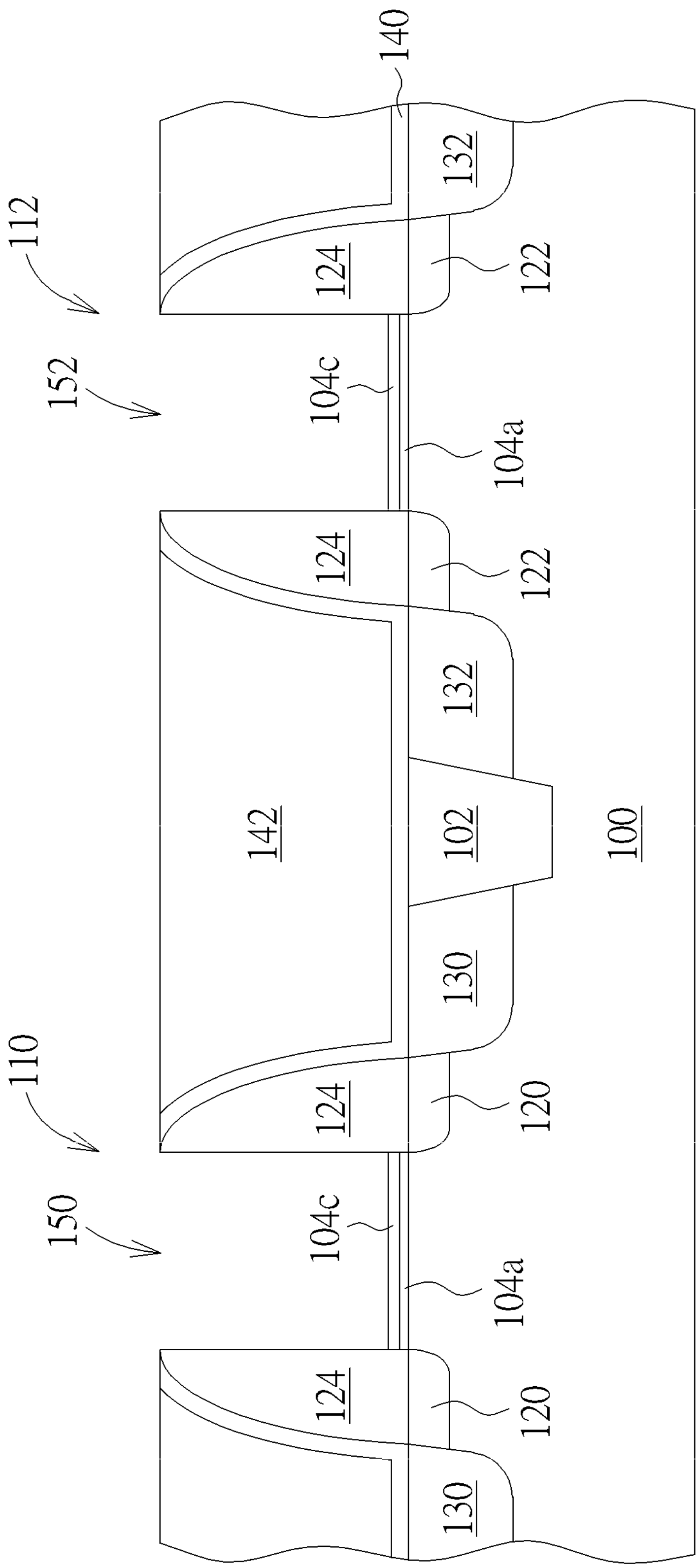
120
190

FIG. 8


140
112
132
124
122
152
104c
104a
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122
132
142
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110
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120
150
104c
104a
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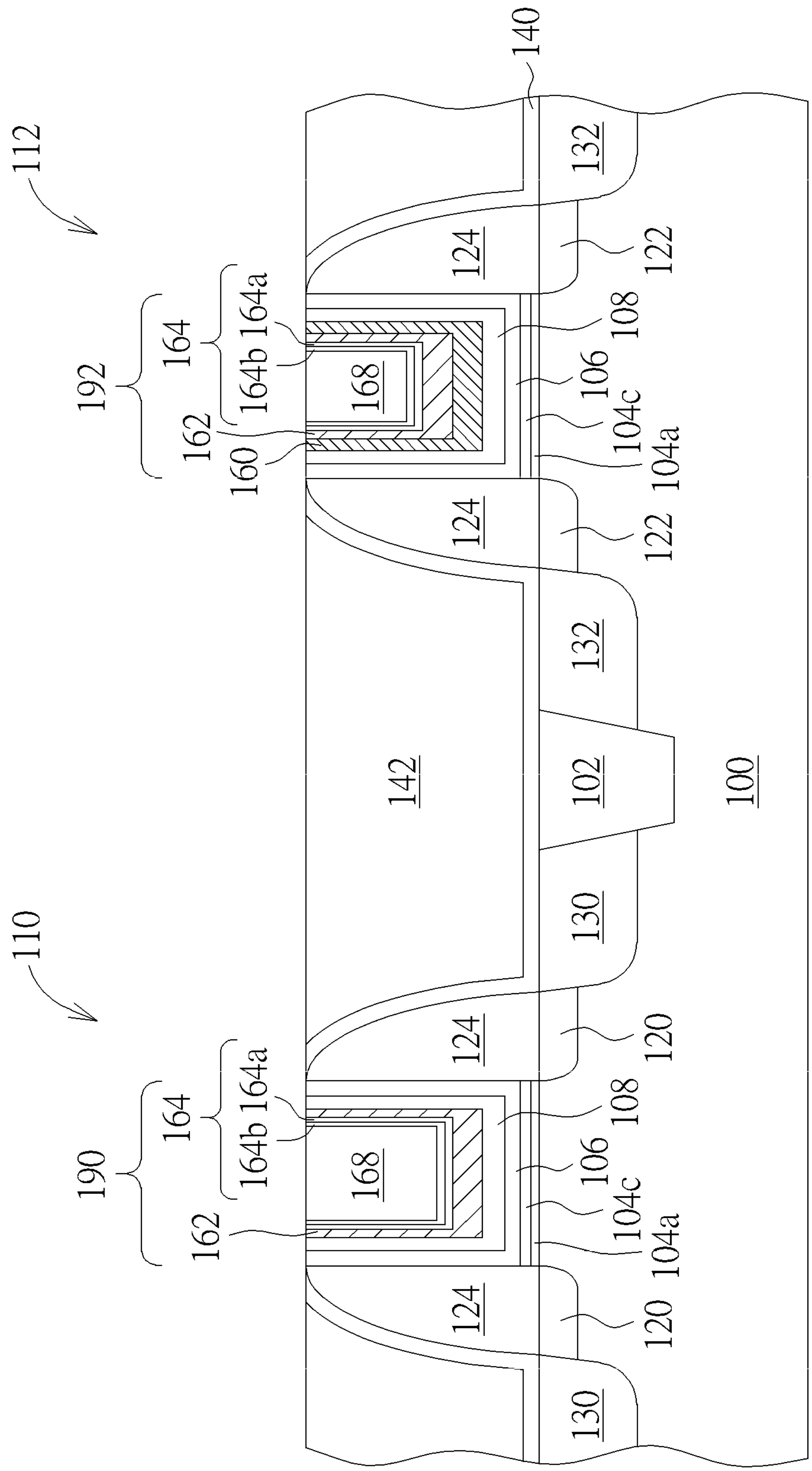
130

FIG. 9



112
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164a
164b
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104c
104a
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142
102
100
130
110
124
120
164
164a
164b
190
168
108
106
104c
104a
162
124
120
130

FIG. 10

SEMICONDUCTOR DEVICE HAVING METAL GATE AND MANUFACTURING METHOD THEREOF

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The invention relates to a semiconductor device having metal gate and a manufacturing method thereof, and more particularly, to a semiconductor device having metal gate and a manufacturing method capable of prevention metal diffusion and improving gap-fill result.

[0003] 2. Description of the Prior Art

[0004] With a trend toward scaling down the size of the semiconductor device, work function metals are used to replace the conventional polysilicon gate to be the control electrode that competent to the high dielectric constant (herein after abbreviated as high-k) gate dielectric layer. The conventional metal gate methods are categorized into the gate first process and the gate last process. Among the two main processes, the gate last process is able to avoid processes of high thermal budget and to provide wider material choices for the high-k gate dielectric layer and the metal gate, and thus the gate last process gradually replaces the gate first process.

[0005] In the conventional gate last process, a dummy gate or a replacement gate is formed on a substrate and followed by steps of forming a conventional metal-oxide semiconductor (MOS) transistor device. Subsequently, the dummy/replacement gate is removed to form a gate trench. Then the gate trench is filled with work function metals required by different conductivity types and gap filling metals. Often, it may employ material such as aluminum (Al) as the gap filling metal. It has been observed that Al may diffuse into the work function metals, and thus the electrical property of the work function metal is adversely influenced. As a countermeasure against to the problems, there has been proposed the barrier layers to prevent the Al diffusion.

[0006] To provide prevention to the Al diffusion, multi-layered barrier structure including at least a titanium nitride (hereinafter abbreviated as TiN) layer or a tantalum nitride (hereinafter abbreviated as TaN) is developed. However, it is found the multi-layered barrier structure is still insufficient to prevent the Al diffusion. Furthermore, the multi-layered barrier structure narrows the opening of the gate trench and thus causes gap-filling issue.

[0007] Accordingly, though the gate last process is able to avoid processes of high thermal budget and to provide wider material choices for the high-k gate dielectric layer and the metal gate, the gate last process still faces material requirements for the complicated processes and reliability requirement for the layers filling in the gate trench.

SUMMARY OF THE INVENTION

[0008] According to an aspect of the present invention, a method for manufacturing a semiconductor device having metal gate is provided. According to the method, a substrate having at least a first semiconductor device formed thereon is provided. The first semiconductor device includes a first gate trench formed therein. Next, an n-typed work function metal layer is formed in the first gate trench. After forming the n-typed work function metal layer, a nitridation process is performed to form a first protecting layer on the n-typed work function metal layer. After forming the first protecting layer, an oxidation process is performed to the first protecting layer to form a second protecting layer on the n-typed work function metal layer. Then, a gap filling metal layer is formed to fill up the first gate trench.

[0009] According to another aspect of the present invention, a semiconductor device having metal gate is provided. The semiconductor device having metal gate includes a substrate, a high-k gate dielectric layer formed on the substrate, an n-typed work function metal layer formed on the high-k gate dielectric layer, a first protecting layer formed on the n-typed work function metal layer, a second protecting layer formed on the first protecting layer, and a gap filling metal layer directly formed on the second protecting layer. It is noteworthy that the first protecting layer includes a nitrified material of the n-typed work function metal layer, and the second protecting layer includes an oxidized material of the first protecting layer.

[0010] According to the method for manufacturing the semiconductor device having metal gate provided by the present invention, the protecting layer is formed by sequentially performing the nitridation process and the oxidation process to the n-typed work function metal layer. Therefore no additional protecting/barrier layer is deposited on the n-typed work function metal layer in the gate trench. In other words, fewer layers are deposited in the gate trench and thus gap filling result of the ensuing layers formed in the gate trench is improved.

[0011] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIGS. **1-8** are drawings illustrating a manufacturing method for a semiconductor device having metal gate provided by a first preferred embodiment of the present invention, wherein

[0013] FIG. **2** is a schematic drawing in a step subsequent to FIG. **1**,

[0014] FIG. **3** is a schematic drawing in a step subsequent to FIG. **2**,

[0015] FIG. **4** is a schematic drawing in a step subsequent to FIG. **3**,

[0016] FIG. **5** is a schematic drawing in a step subsequent to FIG. **4**,

[0017] FIG. **6** is a schematic drawing in a step subsequent to FIG. **5**,

[0018] FIG. **7** is a schematic drawing in a step subsequent to FIGS. **6**, and

[0019] FIG. **8** is a schematic drawing in a step subsequent to FIG. **7**.

[0020] FIGS. **9-10** are drawings illustrating a manufacturing method for a semiconductor device having metal gate provided by a second preferred embodiment, wherein

[0021] FIG. **10** is a schematic drawing in a step subsequent to FIG. **9**.

DETAILED DESCRIPTION

[0022] Please refer to FIGS. **1-8**, which are drawings illustrating a manufacturing method for a semiconductor device having metal gate provided by a first preferred embodiment of the present invention. As shown in FIG. **1**, the preferred embodiment first provides a substrate **100** such as a silicon substrate, a silicon-containing substrate, or a silicon-on-insulator (SOI) substrate. The substrate **100** includes a first semiconductor device **110** and a second semiconductor device **112** formed thereon. A shallow trench isolation (STI) **102** is formed in the substrate **100** between the first semiconductor device **110** and the second semiconductor device **112** for providing electrical isolation. The first semiconductor device **110** includes a first conductivity type, the second semiconductor device **112** includes a second conductivity type, and the first conductivity type and the second conductivity type are complementary. In the preferred embodiment, the first semiconductor device **110** is an n-typed semiconductor device and the second semiconductor device **112** is a p-typed semiconductor device.

[0023] Please still refer to FIG. **1**. The first semiconductor device **110** and the second semiconductor device **112** respectively include a dielectric layer **104***a* and a dummy gate such as a polysilicon layer (not shown), and a patterned hard mask (not shown) formed on the polysilicon layer for defining the dummy gate. The first semiconductor device **110** and the second semiconductor device **112** further respectively include first lightly-doped drains (hereinafter abbreviated as LDDs) **120** and second LDDs **122**, a spacer **124**, a first source/drain **130** and a second source/drain **132**. Salicides (not shown) are respectively formed on surfaces of the first source/drain **130** and the second source/drain **132**. On the first semiconductor device **110** and the second semiconductor device **112**, a contact etch stop layer (hereinafter abbreviated as CESL) **140** and an inter-layer dielectric (hereinafter abbreviated as ILD) layer **142** are sequentially formed.

[0024] Please still refer to FIG. **1**. Subsequently, a planarization process is performed to remove a portion of the CESL **140** and a portion of the ILD layer **142** and followed by performing a suitable etching process to remove the patterned hard mask layers and the dummy gates of the first semiconductor device **110** and the second semiconductor device **112**. Consequently, a first gate trench **150** is formed in the first semiconductor device **110** and a second gate trench **152** is formed in the second semiconductor device **112**, simultaneously. And the dielectric layer **104***a* is exposed at bottoms of both of the first gate trench **150** and the second gate trench **152**.

[0025] Please refer to FIG. **2**. After forming the first gate trench **150** and the second gate trench **152**, a high-k gate dielectric layer **104***b* is formed on the substrate **100**. It is noteworthy that the preferred embodiment is integrated with the high-k last process, therefore the dielectric layer **104***a* exposed in the gate trenches **150**/**152** can be used as an interfacial layer **104***a*. The high-k gate dielectric layer **104***b* includes high-k materials such as rare earth metal oxide. For example but not limited to, the high-k gate dielectric layer **104***b* can include material selected from the group consisting of hafnium oxide (HfO_2), hafnium silicon oxide ($HfSiO_4$), hafnium silicon oxynitride (HfSiON), aluminum oxide (Al_2O_3), lanthanum oxide (La_2O_3), tantalum oxide (Ta_2O_5), yttrium oxide (Y_2O_3), zirconium oxide (ZrO_2), strontium titanate oxide ($SrTiO_3$), zirconium silicon oxide ($ZrSiO_4$), hafnium zirconium oxide ($HfZrO_4$), strontium bismuth tantalate, ($SrBi_2Ta_2O_9$, SBT), lead zirconate titanate ($PbZr_xTi_{1-x}O_3$, PZT), and barium strontium titanate ($Ba_xSr_{1-x}TiO_3$, BST).

[0026] Please still refer to FIG. **2**. After forming the high-k gate dielectric layer **104***b*, a bottom barrier layer **106**, an etch stop layer **108**, and a p-typed work function metal layer **160** are sequentially formed in the gate trenches **150**/**152** and on the substrate **100**. Typically, the bottom barrier layer **106** includes TiN, and the etch stop layer **108** includes TaN, but not limited to this. The p-typed work function metal layer **160** includes metal material having a work function of about 4.85 eV, for example but not limited to TiN.

[0027] Please refer to FIG. **3**. After forming the first work function metal layer **160**, a patterned protecting layer (not shown) is formed on the substrate **100** to protect the second semiconductor device **112** and expose the first semiconductor device **110**, particularly to expose the first work function metal layer **160** in the first gate trench **150**. Subsequently, an etching process is performed to remove the exposed first work function metal layer **160** from the first gate trench **150**. It is noteworthy that this instant etching process stops at the etch stop layer **108**. In other words, the bottom barrier layer **106** and the high-k dielectric layer **104***b* in the first gate trench **150** are protected by the etch stop layer **108** during removing the first work function metal layer **160** from the first gate trench **150**.

[0028] Please refer to FIG. **4**. Next, an n-typed work function metal layer **162** is formed in the first gate trench **150** and the second gate trench **152**. The n-typed work function metal layer **162** includes metal materials having a work function of about 3.95 eV, for example but not limited to titanium aluminide (hereinafter abbreviated as TiAl). A thickness of the n-typed work function metal layer **162** is about 100 Angstroms (Å), but not limited to this.

[0029] Please refer to FIG. **5**. After forming the n-typed work function metal layer **162**, a nitridation process **170** is performed to the n-typed work function metal layer **162**. Accordingly, a portion of the n-typed work function metal layer **162** is nitrified, and a first protecting layer **164***a* is therefore formed on the n-typed work function metal layer **162**. The first protecting layer **164***a* includes a nitrified material of the n-typed work function metal layer **162**. For example, when the n-typed work function metal layer **164** includes TiAl, the first protecting layer **164***a* includes a titanium aluminum nitride (hereinafter abbreviated as TiAlN). In the preferred embodiment, the nitridation process **170** includes nitrogen (N_2) or ammonia (NH_3). The nitridation process **170** can be, for example but not limited to, a N_2 plasma treatment or a NH_3 plasma treatment. In accordance with the preferred embodiment, a low frequency (LF) power of the N_2 plasma treatment is about 0-100W, a high frequency (HF) power of the N_2 plasma treatment is about 200-600W. A flow rate of nitrogen in the N_2 plasma treatment is about 5-200 standard cubic centimeters per minute (sccm). A process pressure of the N_2 plasma treatment is smaller than 15 Torr, a process temperature of the N_2 plasma treatment is lower than 350° C., and a process duration of the N_2 plasma treatment is greater than 60 seconds (sec.).

[0030] Please refer to FIG. **6**. After forming the TiAlN layer **162** by performing the nitridation process **170**, an oxidation process **172** is performed to the TiAlN layer **162**. In the preferred embodiment, the oxidation process **172** includes dinitrogen monoxide (N_2O) or oxygen (O_2). The oxidation process **172** can be, for example but not limited to, a N_2O treatment or an O_2 treatment. In accordance with the preferred embodiment, a LF power of the N_2O plasma treatment is about 250-1000W, a HF power of the N_2O plasma treatment is about 200-600W. A flow rate of N_2O in the N_2O plasma treatment is about 100-3000 sccm. A process pressure of the N_2O plasma treatment is smaller than 15 Torr, a process temperature of the N_2O plasma treatment is lower than 350° C., and a process duration of the N_2O plasma treatment is between 40 sec. and 120 sec. Consequently, a second protecting layer **164***b* is formed on the first protecting layer **164***a*. The second protecting layer **164***b* includes an oxidized material of the first protecting layer **164***a*. For example, when the first protecting layer **164***a* includes TiAlN, the second protecting layer **164***b* includes TiAlNO. The first protecting layer **164***a* and the second protecting layer **164***b* cooperatively serve as a barrier layer **164**. More important, an overall thickness of the second protecting layer **164***b* (that is the TiAlNO layer **164***b*) and of the first protecting layer **164***a* (That is the TiAlN layer **164***a*) is smaller than one-third of an original thickness of the n-typed work function metal layer **162**. In other words, the overall thickness of the first protecting layer **164***a* and the second protecting layer **164***b* is smaller than a half of the thickness of a final thickness of the n-typed work function metal layer **162**. Accordingly, the overall thickness of the first protecting layer **164***a* and the second protecting layer **164***b* is between 20 Å and 30 Å.

[0031] Please refer to FIG. **7**. After forming the second protecting layer **164***b*, a gap-filling metal layer **168** is formed on the substrate **100**. The gap filling metal layer **168** includes materials with low resistance and superior gap-filling characteristic such as Al, but not limited to this. It is noteworthy that the gap-filling metal layer **168** is directly formed on the second protecting layer **164***b*. In other words, the gap-filling metal layer **168** contacts the second protecting layer **164***b*.

[0032] Please refer to FIG. **8**. After forming the gap-filling metal layer **168**, a planarization process, such as a CMP process, is performed to remove the superfluous gap-filling metal layer **168**, barrier layer **164**, n-typed work function metal layer **162**, p-typed work function metal layer **160**, etch stop layer **108**, bottom barrier layer **106** and high-k gate dielectric layer **104***b*. Consequently, a first metal gate **190** and a second metal gate **192** are obtained. In addition, the ILD layer **142** and the CESL **140** can be selectively removed and sequentially reformed on the substrate **100** for improving performance of the semiconductor devices **110/112** in the preferred embodiment. Since the abovementioned CMP process is well-known to those skilled in the art, those details are omitted in the interest of brevity.

[0033] According to the method for manufacturing the semiconductor device having metal gate provided by the preferred embodiment, the high-k gate dielectric layer **104***b* includes a U shape since the preferred embodiment adopts high-k last approach. More important, the barrier layer **164** (including the first protecting layer **164***a* and the second protecting layer **164***b*), which is formed by transferring an upper portion of the n-typed work function layer **162**, provides superior prevention for Al diffusion and thus no more top barrier layer is required in the preferred embodiment. Accordingly, the following formed gap-filling metal layer **168** is to fill the gate trenches **150/152** with wider opening and thus gap-filling result is improved.

[0034] Please refer to FIGS. **9-10**, which are drawings illustrating a method for manufacturing a semiconductor device having metal gate provided by a second preferred embodiment of the present invention. The method for manufacturing a semiconductor device having metal gate provided by the second preferred embodiment includes steps almost the same as mentioned in the first preferred embodiment, therefore those identical steps are omitted in the interest of brevity, and elements the same in both of the first and second preferred embodiments are designated by the same numerals. The difference between the first and second embodiments is that the second preferred embodiment adopts the high-k first approach.

[0035] Please refer to FIG. **9**. According to the method for manufacturing a semiconductor device having metal gate provided by the second preferred embodiment, a substrate **100** have a first semiconductor device **110** and a second semiconductor device **112** formed thereon is provided. As mentioned above, the first semiconductor device **110** is an n-typed semiconductor device and the second semiconductor device **112** is a p-typed semiconductor device. The first semiconductor device **110** and the second semiconductor device **112** respectively include an interfacial layer **104***a*, a high-k gate dielectric layer **104***c*, a dummy gate (not shown) such as a polysilicon layer, and a patterned hard mask (not shown) formed on the polysilicon layer for defining the dummy gate. It is noteworthy that because the preferred embodiment is integrated with high-k first process, the high-k gate dielectric layer **104***c* includes a flap shape.

[0036] Please still refer to FIG. **9**. For forming the metal gate, the hard mask layers and the dummy gates are removed to form a first gate trench **150** and a second gate trench **152**. As shown in FIG. **9**, the flat shaped high-k gate dielectric layer **104***c* is therefore exposed in the bottom of the gate trenches **150/152**.

[0037] Please refer to FIG. **10**. After forming the gate trenches **150/152**, steps as mentioned above are performed. Those details are the same with the first preferred embodiment and thus omitted for simplicity. Consequently, a first metal gate **190** and a second metal gate **192** are obtained as shown in FIG. **10**.

[0038] According to the method for manufacturing the semiconductor device having metal gate provided by the second preferred embodiment, the high-k gate dielectric layer **104***c* includes a flat shape since the preferred embodiment adopts high-k first approach. More important, the barrier layer **164** (including the first protecting layer **164***a* and the second protecting layer **164***b*), which is formed by transferring an upper portion of the n-typed work function layer **162**, provides superior prevention for Al diffusion and thus no more top barrier layer is required in the preferred embodiment. Accordingly, the following formed gap-filling metal layer **168** is to fill the gate trenches **150/152** with wider opening and thus gap-filling result is improved.

[0039] Additionally, in another preferred embodiment of the present invention, the method for manufacturing the semiconductor device provided by the invention can be integrated with gate first approach. According to the preferred embodiment, a high-k gate dielectric layer is formed on the substrate, an n-typed work function metal layer is formed on the high-k gate dielectric layer, an nitridation process is performed to the n-typed work function metal layer to form a first protecting layer and an oxidation process is performed to the first protecting layer to form a second protecting layer. The nitridation process and the oxidation process include the same parameters as mentioned above and thus those details are omitted for simplicity. Next, gate patterning process is performed and followed by steps for forming LDDs, spacers, and source/drain, and any other required elements. Since those steps for forming the elements are well known to those skilled in the art, the details are omitted for simplicity.

[0040] Briefly speaking, according to the method for manufacturing the semiconductor device having metal gate provided by the present invention, the barrier layer is formed by sequentially performing the nitridation process and the oxidation process to the n-typed work function metal layer and thus transferring the upper portion of the n-typed work function metal layer. Therefore, no additional protecting/barrier layer is deposited on the n-typed work function metal layer in the gate trench. In other words, less layers are deposited in the gate trench and thus gap filling result of the ensuing layers formed in the gate trench is improved. Additionally, the method for manufacturing a semiconductor device having metal gate provided by the present invention can be integrated into high-k first approach and high-k last approach, even the gate-first approach, and thus provides superior manufacturability.

[0041] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

What is claimed is:

1. A method for manufacturing a semiconductor device having metal gate, comprising:

providing a substrate having at least a first semiconductor device formed thereon, and the first semiconductor device comprising a first gate trench formed therein;

forming an n-typed work function metal layer in the first gate trench;

performing a nitridation process to form a first protecting layer on the n-typed work function metal layer;

performing an oxidation process to the first protecting layer to form a second protecting layer on the n-typed work function metal layer after the nitridation; and

forming a gap-filling metal layer to fill up the first gate trench.

2. The method for manufacturing a semiconductor device having metal gate according to claim **1**, further comprising forming a high-k gate dielectric layer in the first gate trench before forming the n-type work function metal layer.

3. The method for manufacturing a semiconductor device having metal gate according to claim **1**, further comprising a high-k gate dielectric layer, and the high-k gate dielectric layer is exposed in the first gate trench.

4. The method for manufacturing a semiconductor device having metal gate according to claim **1**, wherein the nitridation process comprises N_2 or NH_3.

5. The method for manufacturing a semiconductor device having metal gate according to claim **1**, wherein the oxidation process comprises N_2O or O_2.

6. The method for manufacturing a semiconductor device having metal gate according to claim **1**, further comprising a second semiconductor device formed on the substrate, and the second semiconductor device comprises a second gate trench formed therein.

7. The method for manufacturing a semiconductor device having metal gate according to claim **6**, further comprising sequentially forming a bottom barrier layer, an etch stop layer, and a p-type work function metal layer on the substrate before forming the n-typed work metal layer.

8. The method for manufacturing a semiconductor device having metal gate according to claim **7**, further comprising removing the p-typed work function metal layer from the first gate trench before forming the n-typed work function metal layer.

9. A semiconductor device having metal gate comprising:

a substrate;

a high-k gate dielectric layer formed on the substrate;

an n-typed work function metal layer formed on the high-k gate dielectric layer;

a first protecting layer formed on the n-typed work function metal layer, the first protecting layer comprising a nitrified material of the n-typed work function metal layer;

a second protecting layer formed on the first protecting layer, the second protecting layer comprising an oxidized material of the first protecting layer; and

a gap-filling metal layer directly formed on the second protecting layer.

10. The semiconductor device having metal gate according to claim **9**, wherein the high-k gate dielectric layer comprises a flat shape or a U shape.

11. The semiconductor device having metal gate according to claim **9**, wherein the n-typed work function metal layer comprises TiAl layer.

12. The semiconductor device having metal gate according to claim **11**, wherein the first protecting layer is a TiAlN layer.

13. The semiconductor device having metal gate according to claim **12**, wherein the second protecting layer is a TiAlNO layer.

14. The semiconductor device having metal gate according to claim **9**, wherein an overall thickness of the first protecting layer and the second protecting layer is smaller than a half of a thickness of the n-typed work function metal layer.

15. The semiconductor device having metal gate according to claim **9**, further comprising at least a bottom barrier layer and an etch stop layer formed between the high-k gate dielectric layer and the n-typed work function metal layer.

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