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(54) METHOD OF FABRICATING A SEMICONDUCTOR DEVICE

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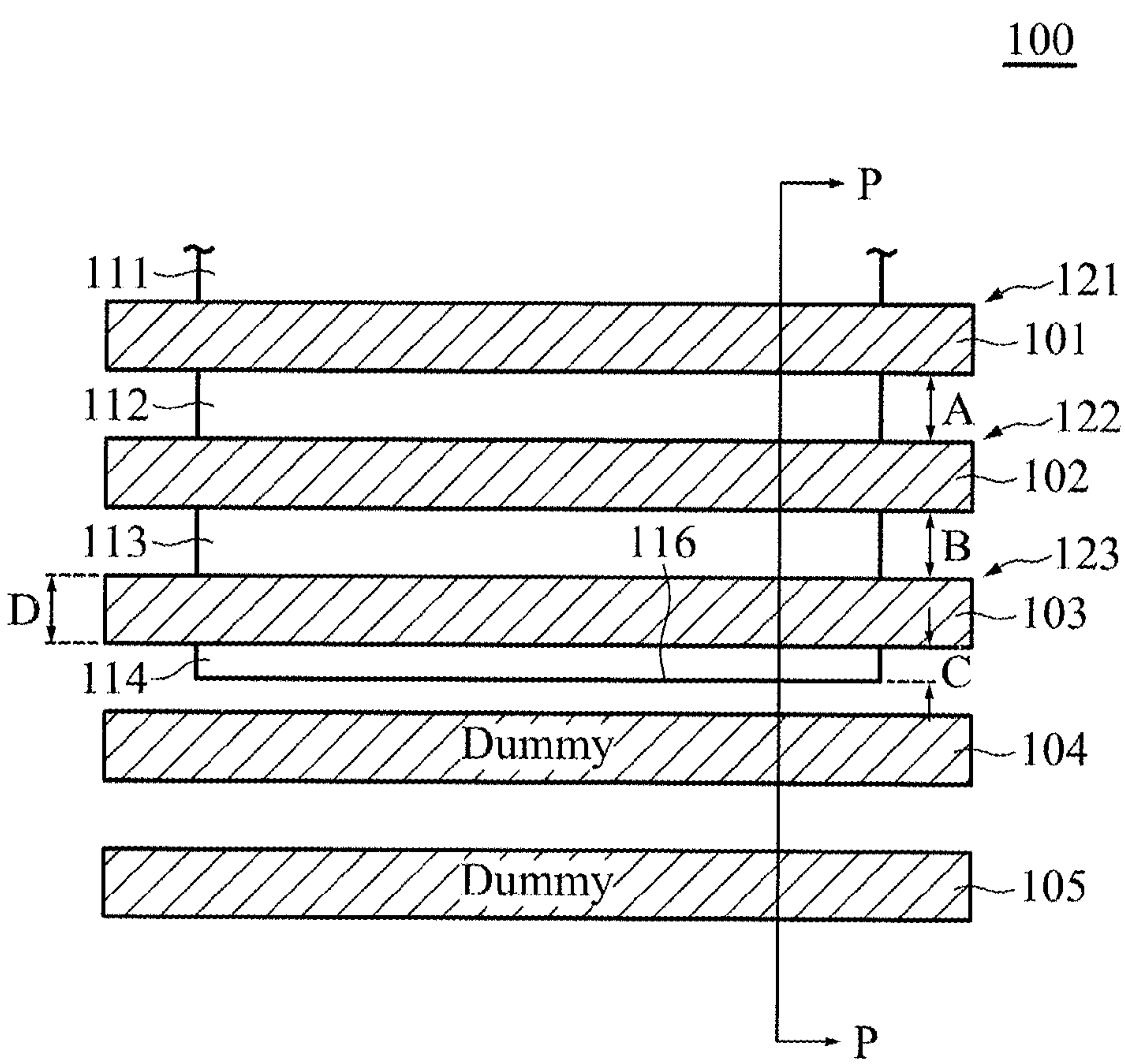
(57) **ABSTRACT**

A method includes designing a first layout of gate structures and diffusion regions of a plurality of active devices, identifying an edge device of the plurality of active devices, modifying the first layout resulting in a second layout, performing a design rule check on the second layout, and fabricating, based on the second layout, at least one of a photolithography mask or at least one component in a layer of a semiconductor device. Modifying the first layout includes adding a dummy device next to the edge device, adding a dummy gate structure next to the dummy device and extending a shared diffusion region to at least the dummy device. The dummy device and the edge device have the shared diffusion region. Performing the design rule check considers a gate structure of the dummy device as one of two dummy gate structures next to the edge device.



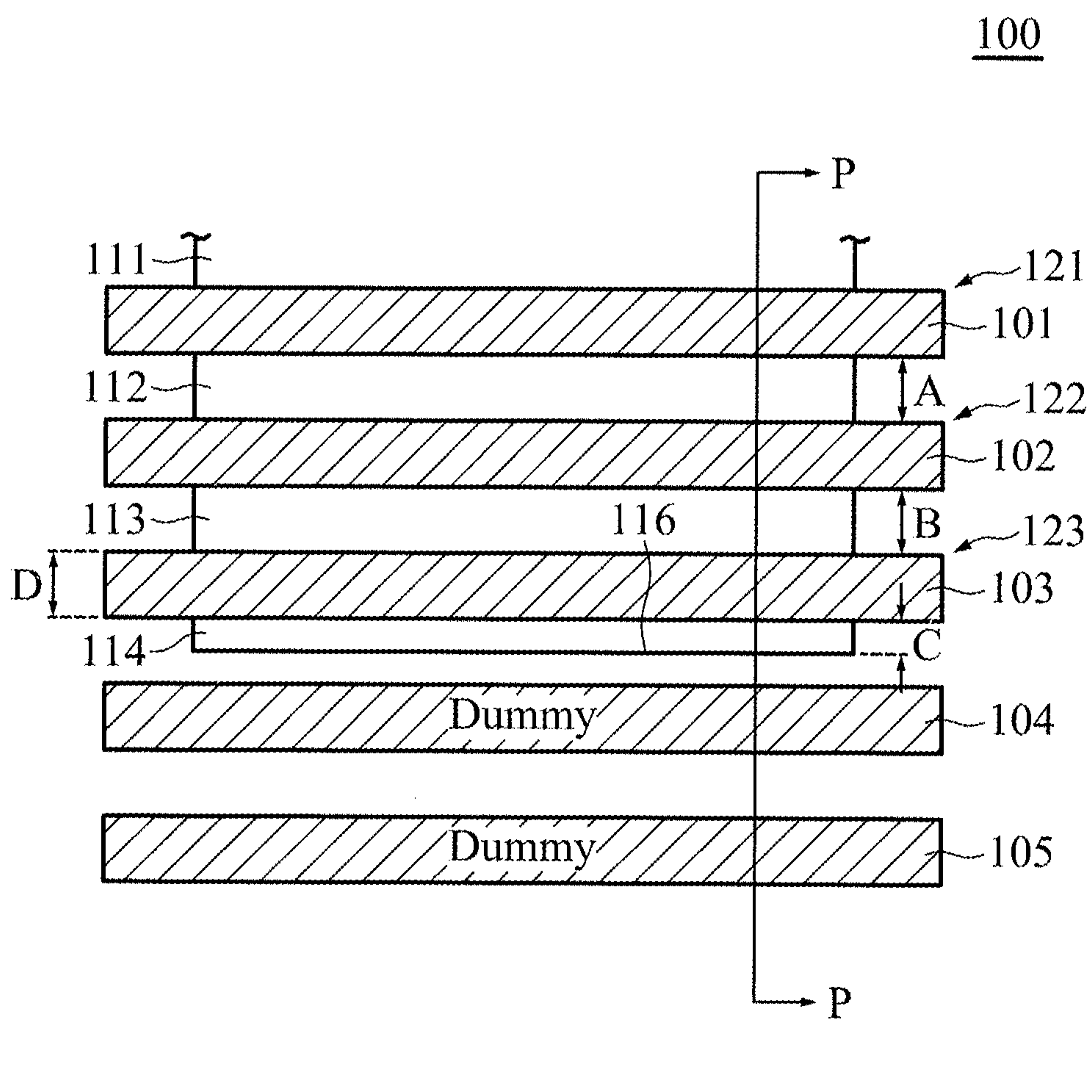

100
P
111
121
101
112
A
122
102
113
116
B
123
D
103
114
C
Dummy
104
Dummy
105
P

FIG. 1A

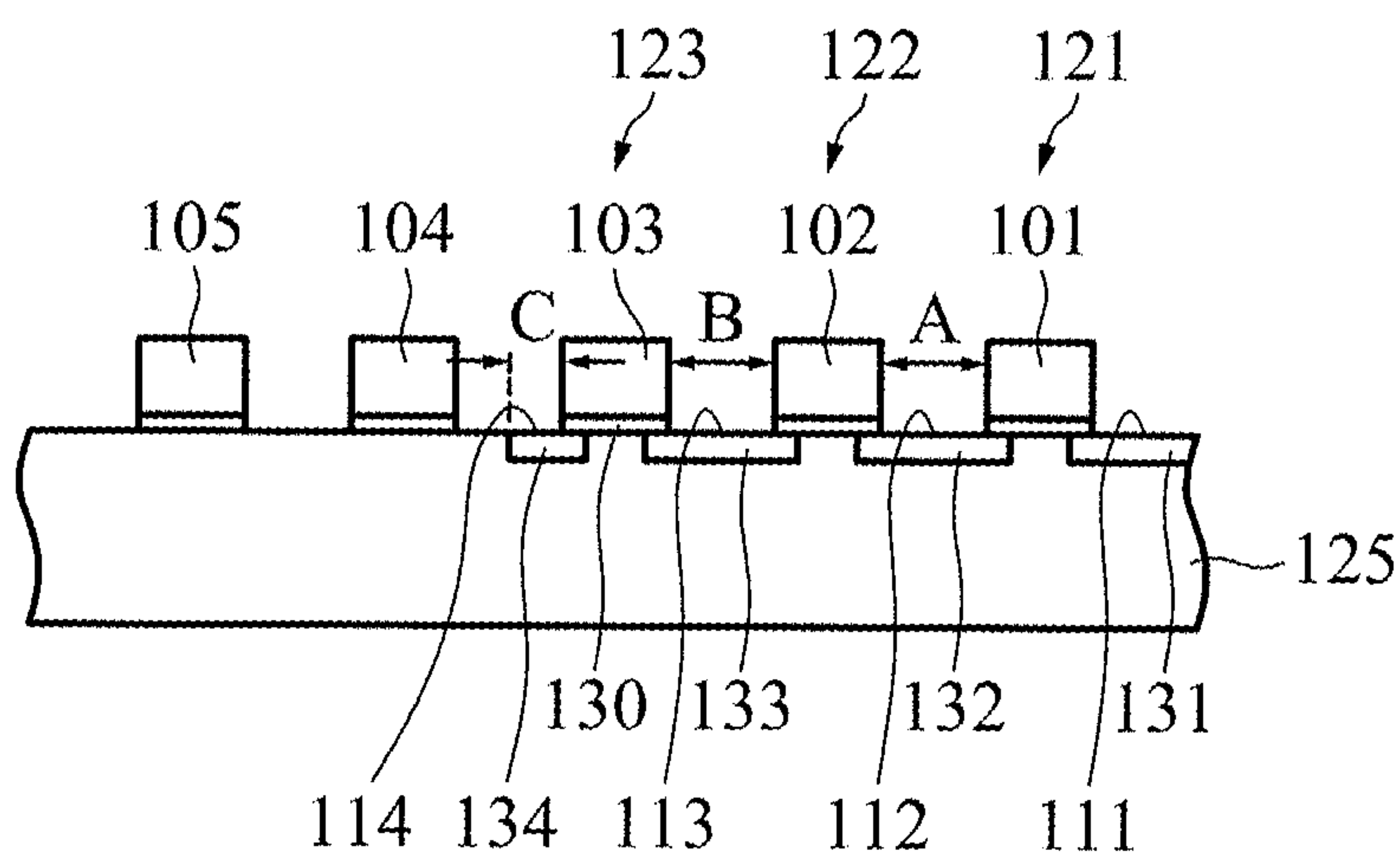

123
122
121
105
104
103
102
101
C
B
A
125
130
133
132
131
114
134
113
112
111

FIG. 1B

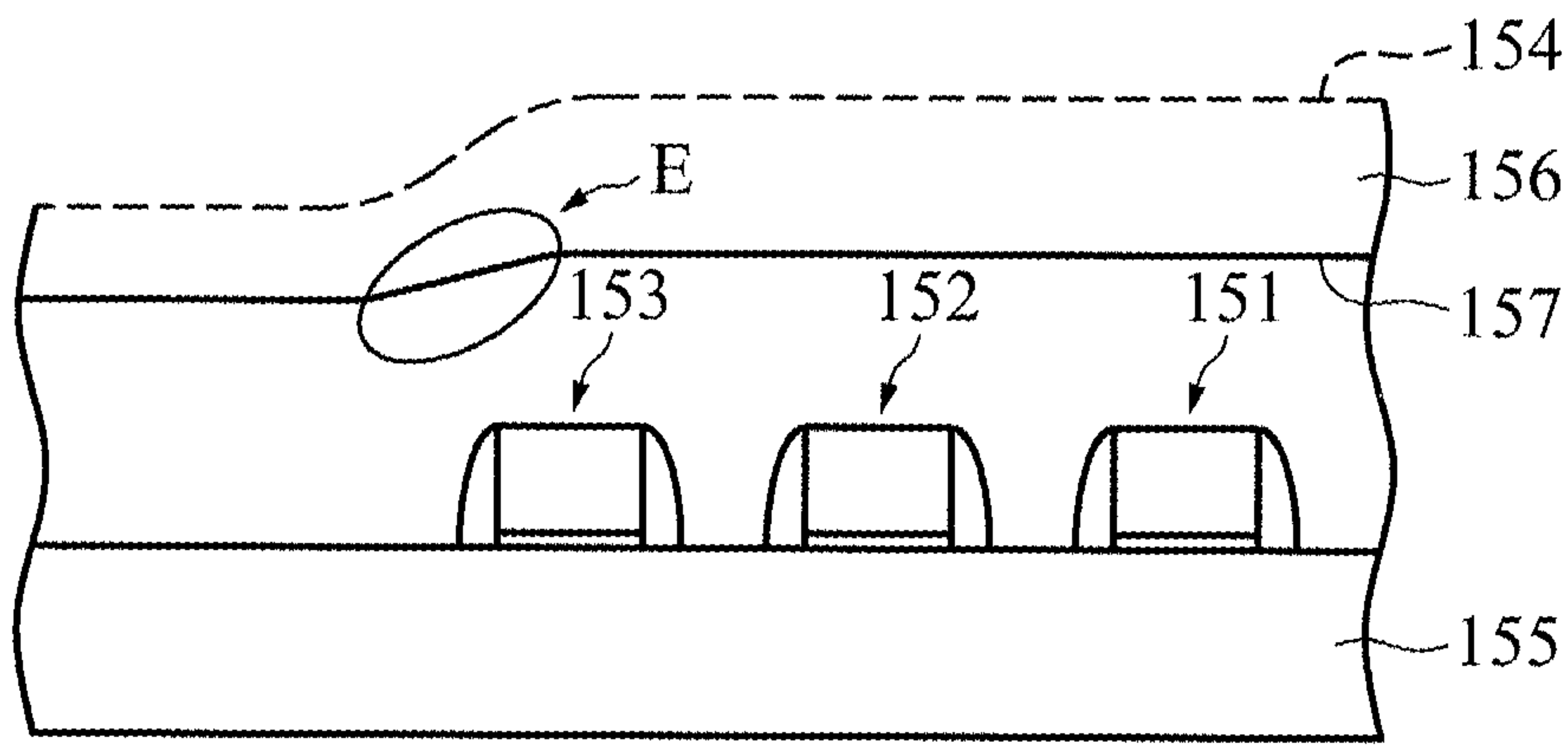


FIG. 1C

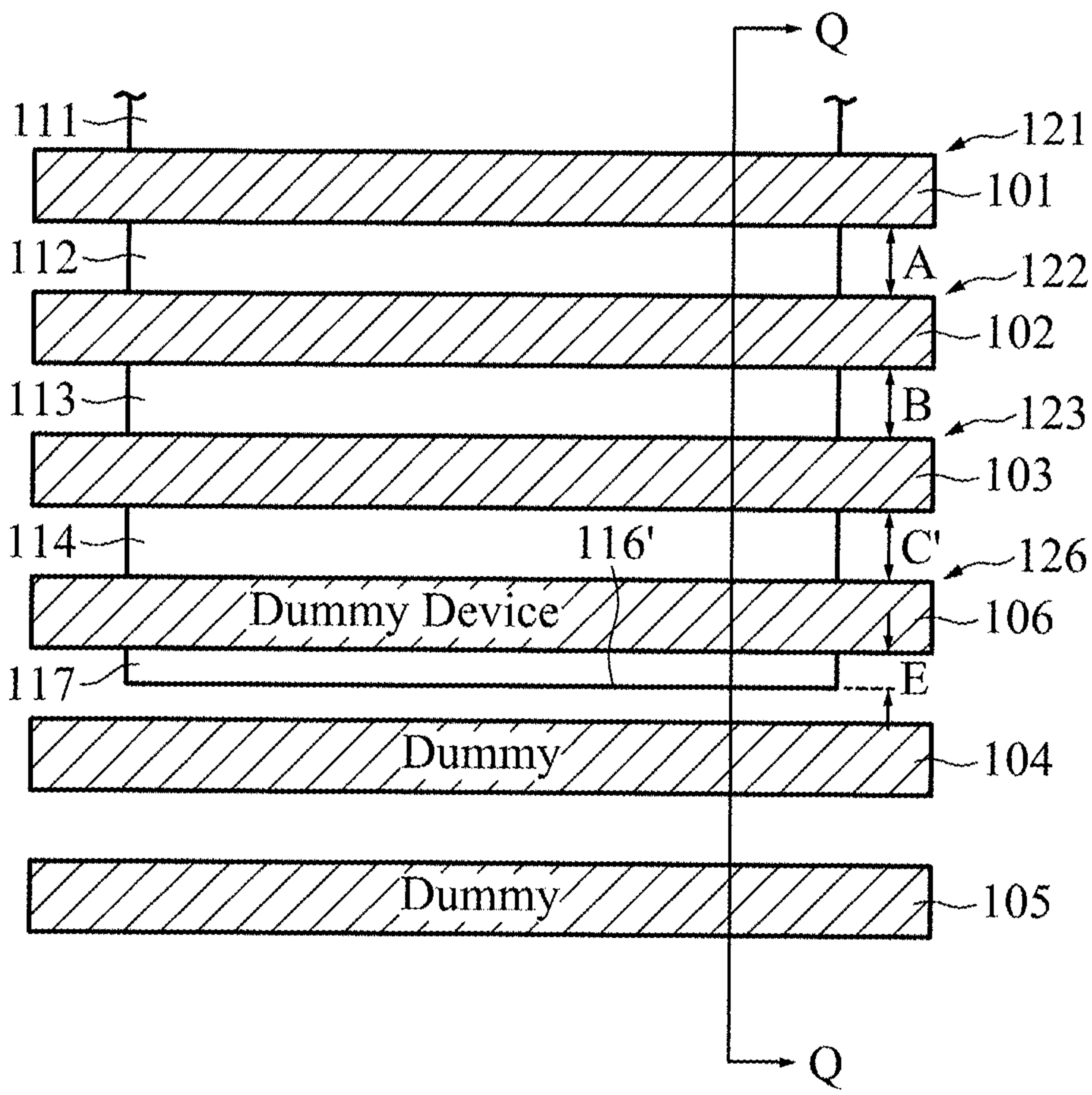

Q
111
121
101
112
A
122
102
113
B
123
103
114
116'
C'
126
Dummy Device
106
117
E
Dummy
104
Dummy
105
Q

FIG. 1D

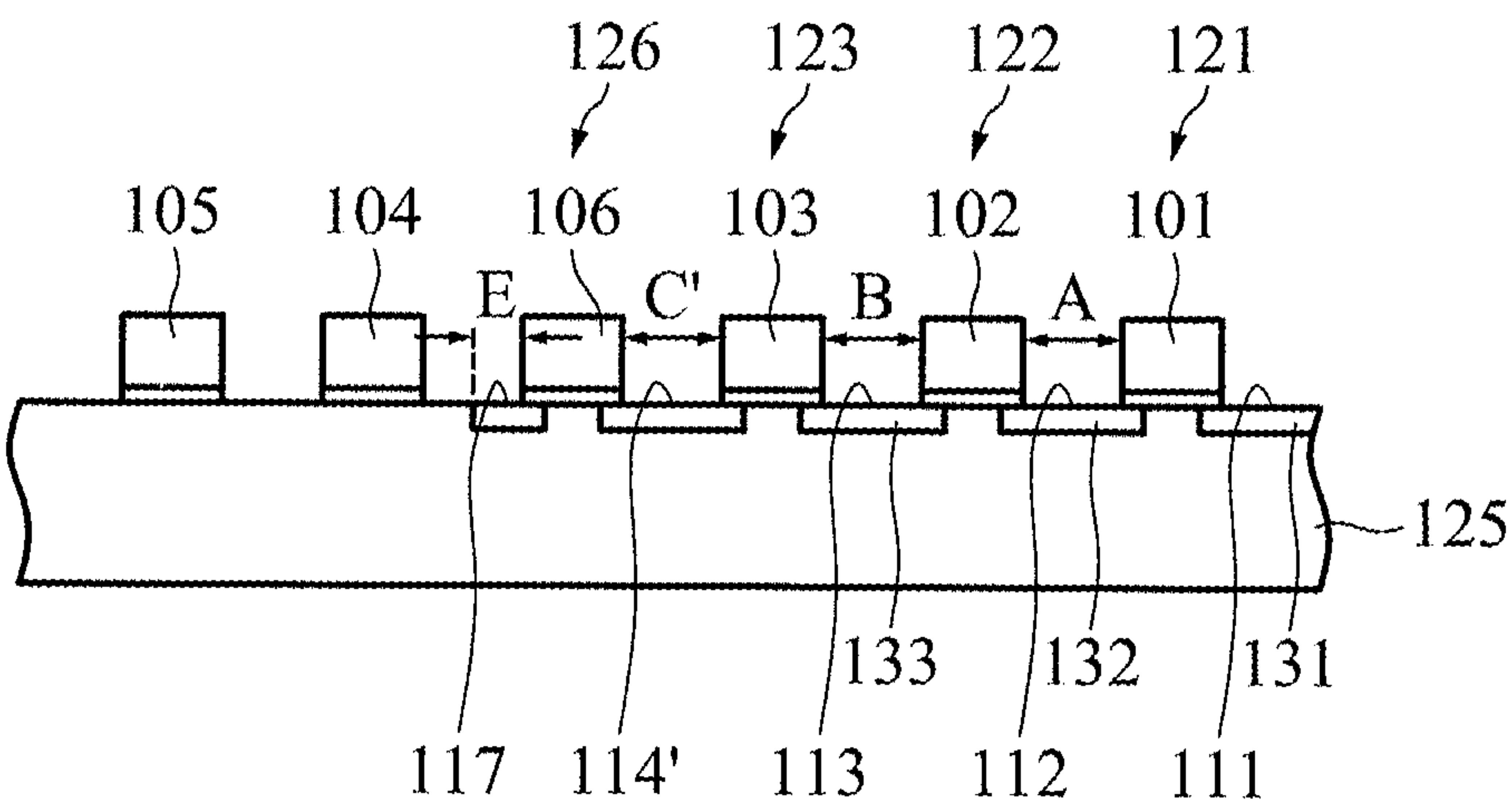

126
123
122
121
105
104
106
103
102
101
E
C'
B
A
125
133
132
131
117
114'
113
112
111

FIG. 1E

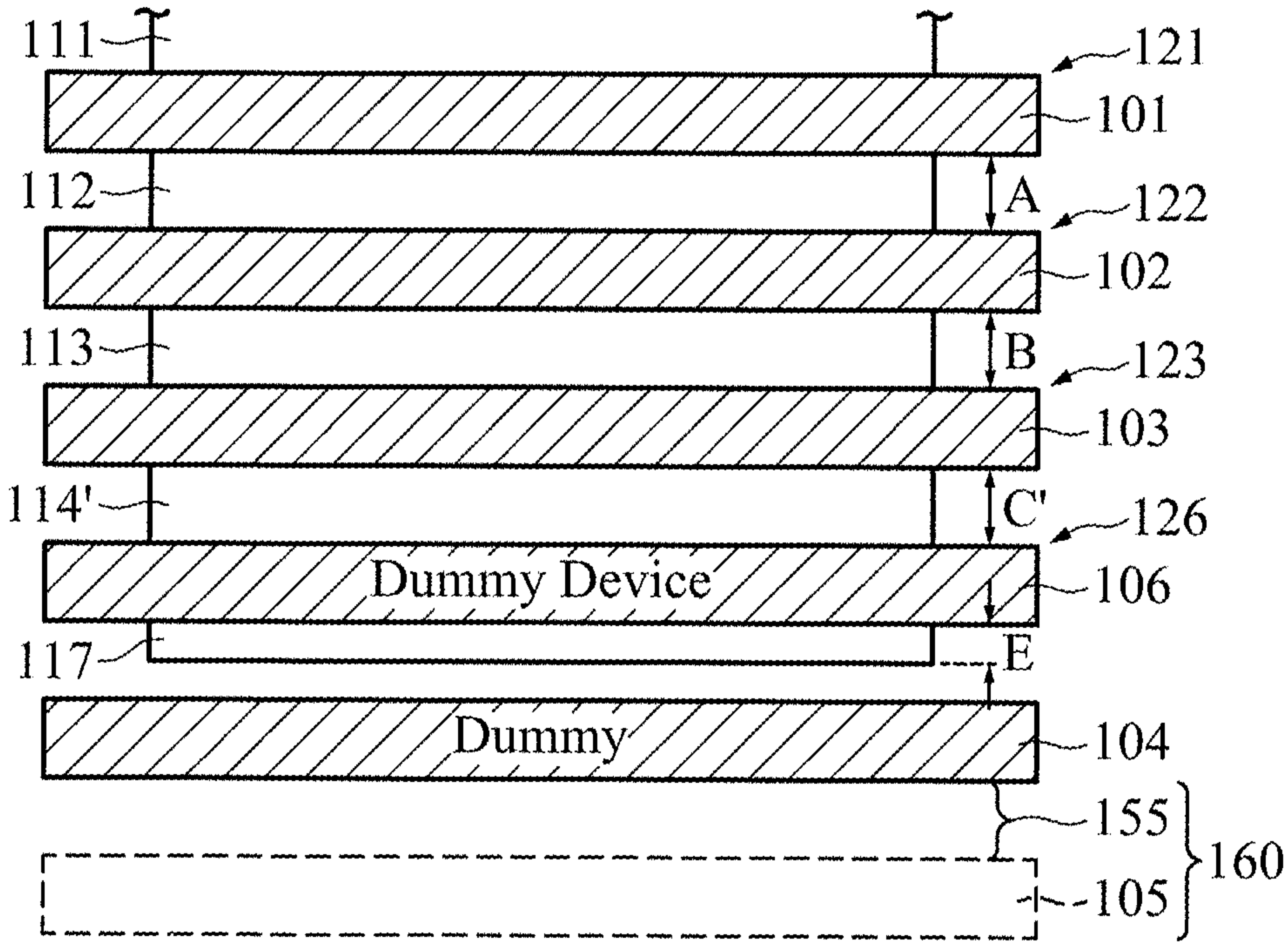

111
121
101
112
A
122
102
113
B
123
103
114'
C'
126
Dummy Device
106
117
E
Dummy
104
155
160
105

FIG. 1F

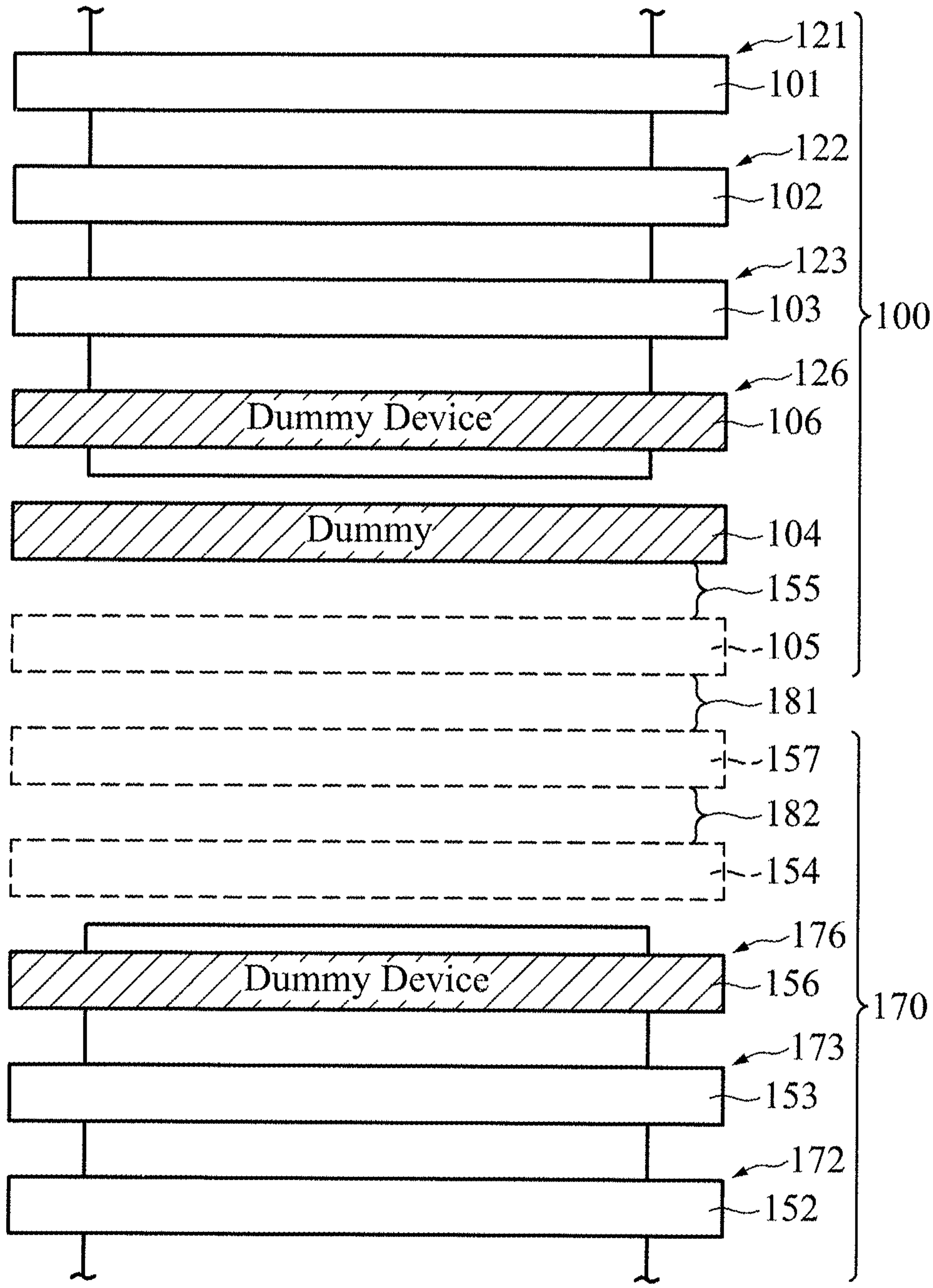

121
101
122
102
123
103
126
Dummy Device
106
100
Dummy
104
155
105
181
157
182
154
176
Dummy Device
156
170
173
153
172
152

FIG. 1G

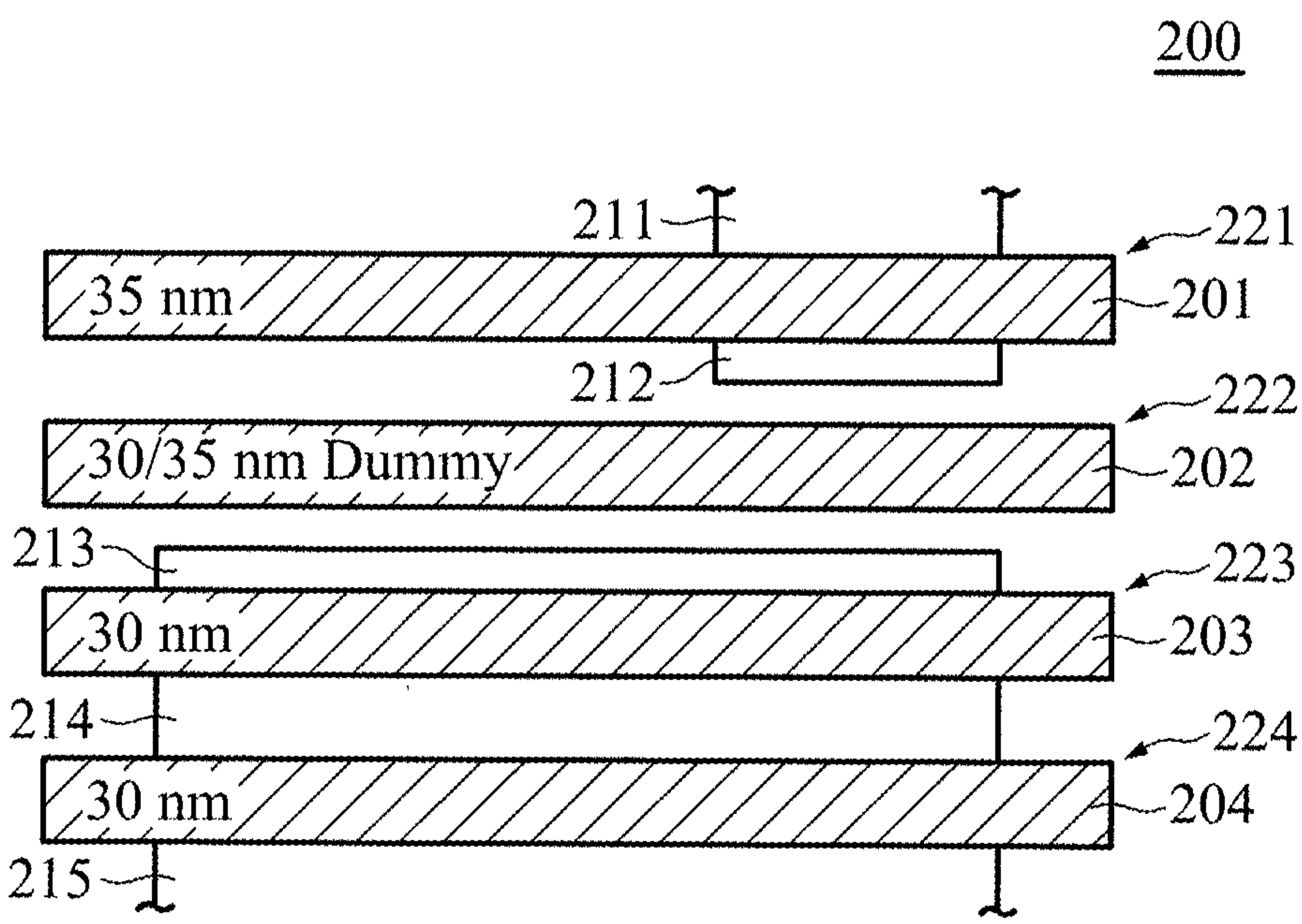

200
211
221
35 nm
201
212
222
30/35 nm Dummy
202
213
223
30 nm
203
214
224
30 nm
204
215

FIG. 2A

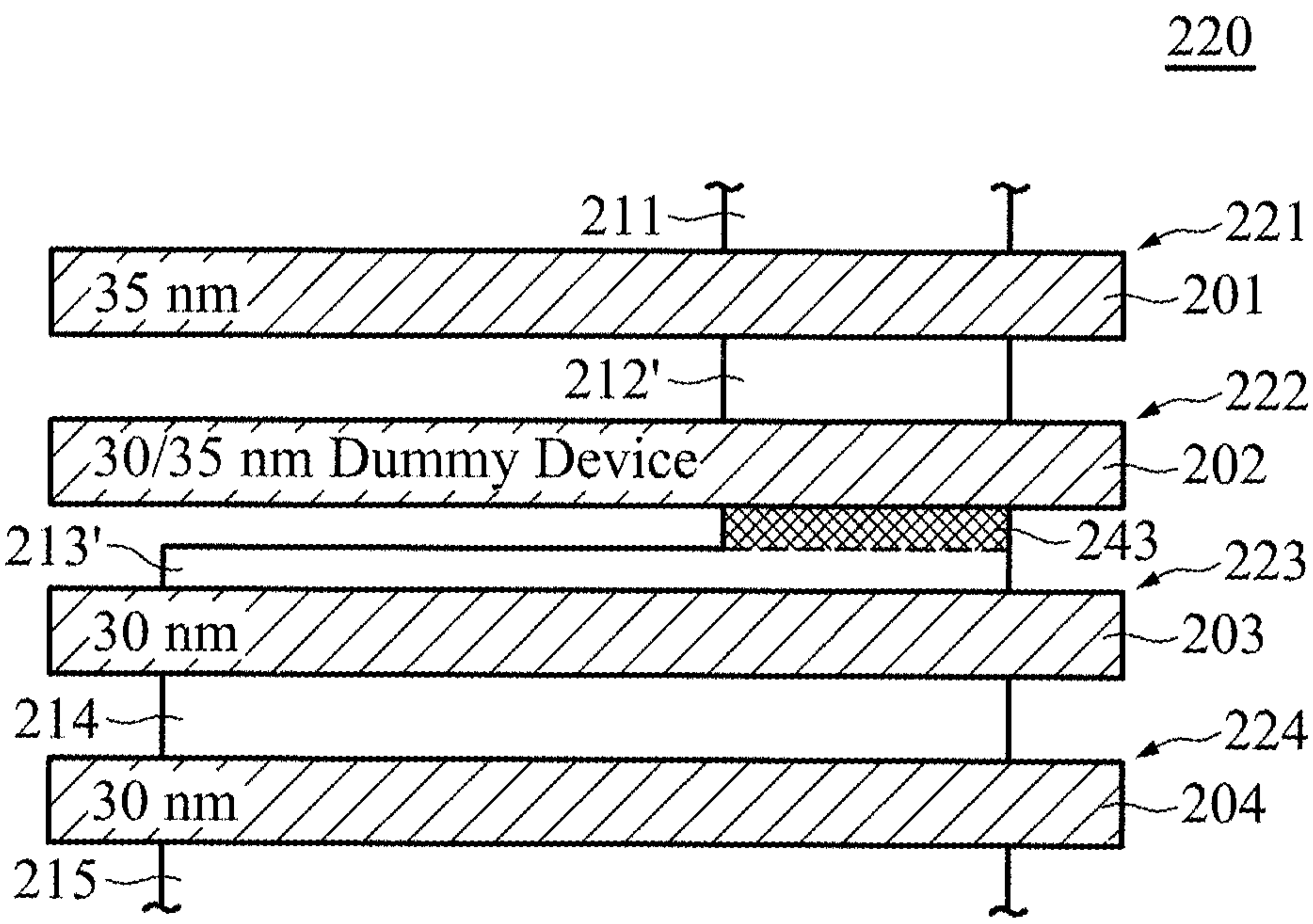

220
211
221
35 nm
201
212'
222
30/35 nm Dummy Device
202
213'
243
223
30 nm
203
214
224
30 nm
204
215

FIG. 2B

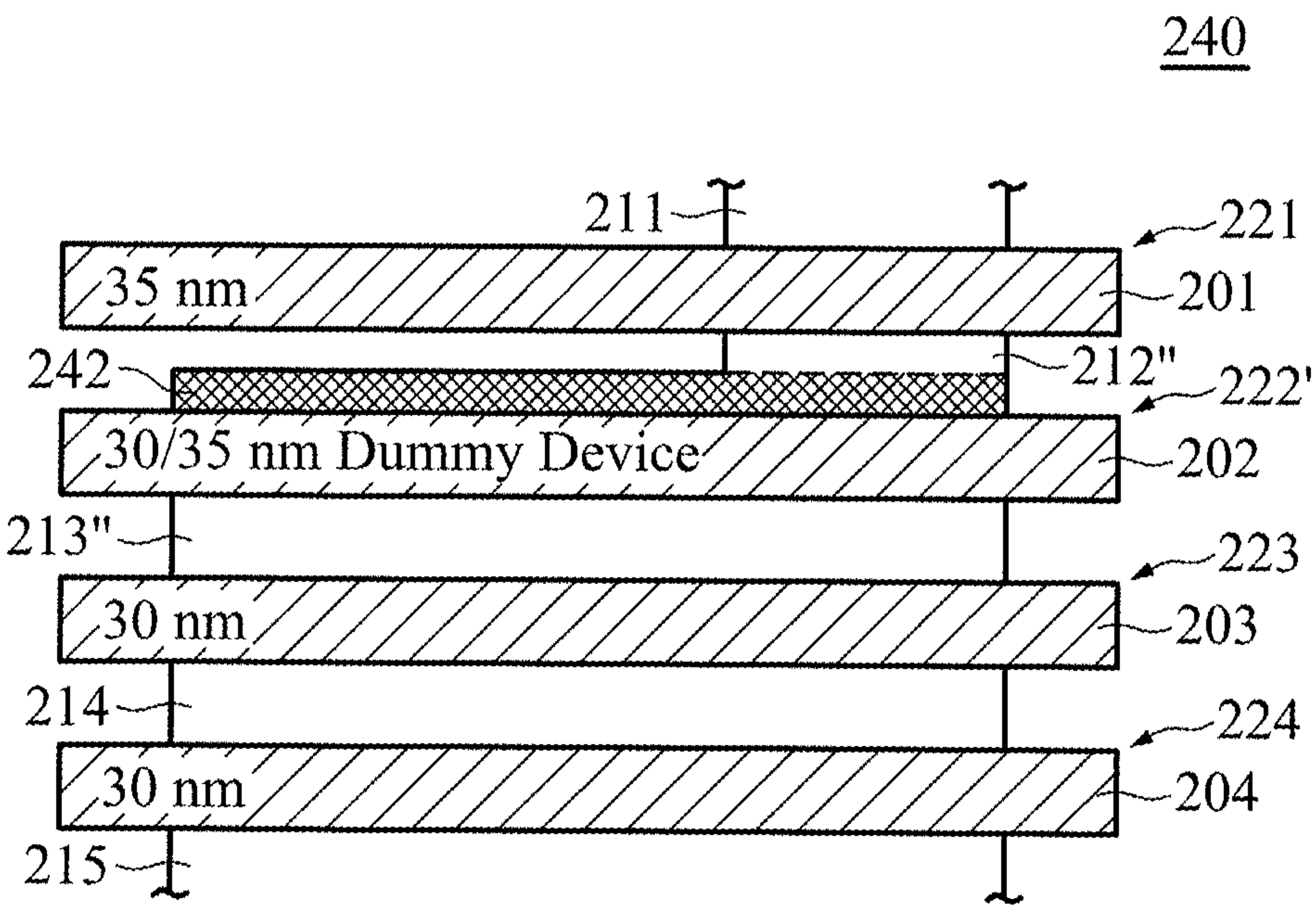

240
211
221
35 nm
201
242
212"
222'
30/35 nm Dummy Device
202
213"
223
30 nm
203
214
224
30 nm
204
215

FIG. 2C

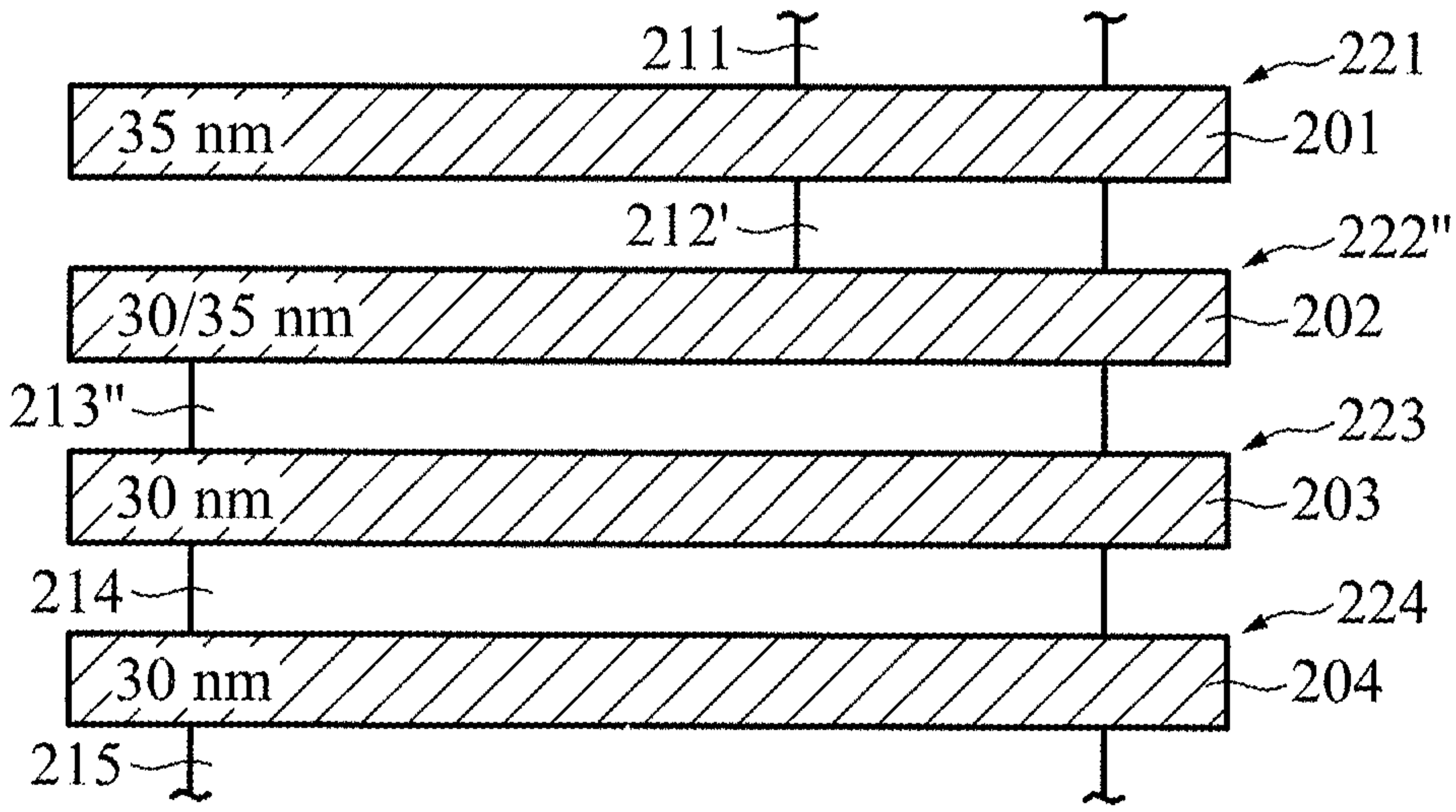

211
221
35 nm
201
212'
222"
30/35 nm
202
213"
223
30 nm
203
214
224
30 nm
204
215

FIG. 2D

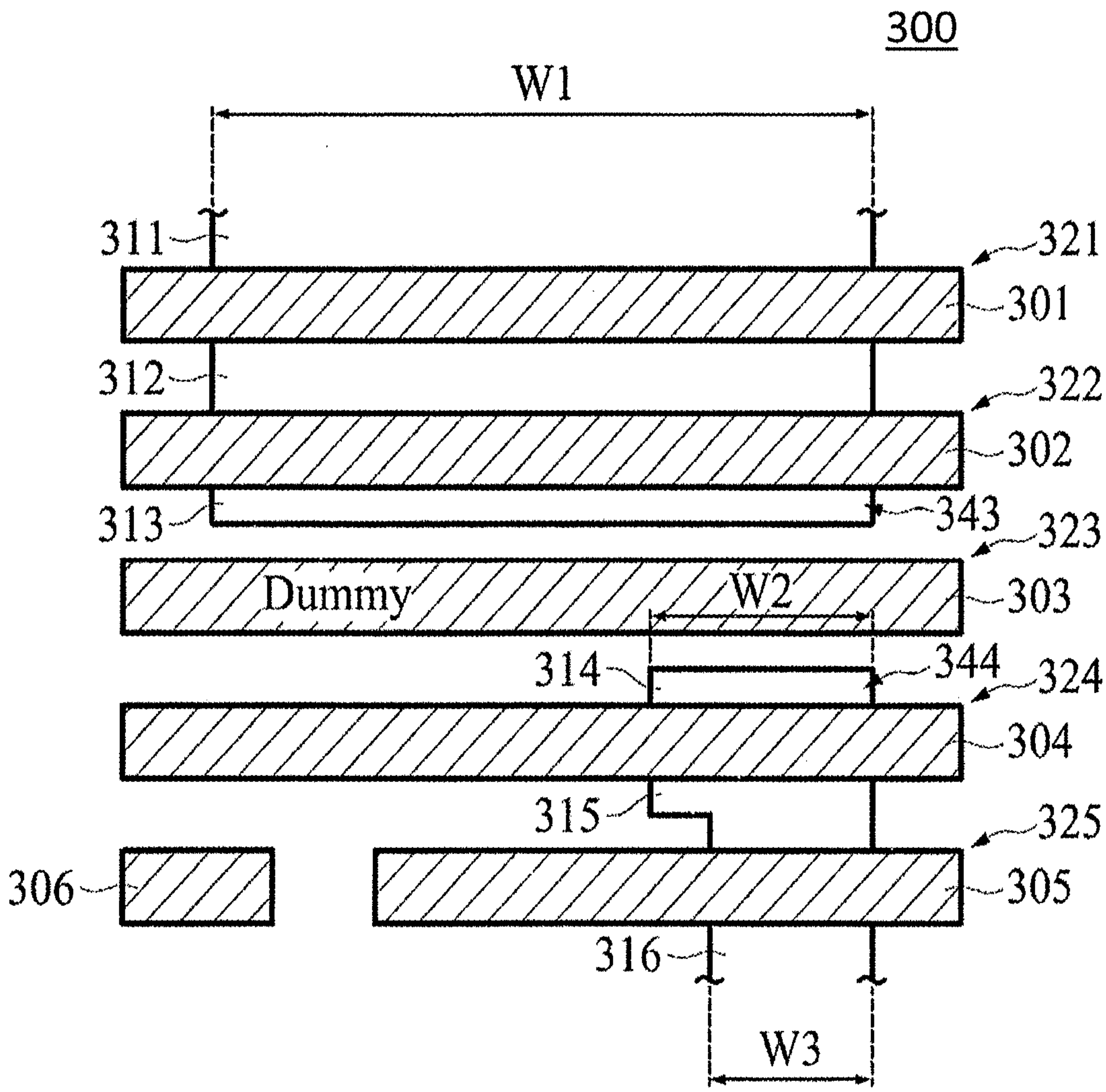

300
W1
311
321
301
312
322
302
313
343
323
Dummy
W2
303
314
344
324
304
315
325
306
305
316
W3

FIG. 3A

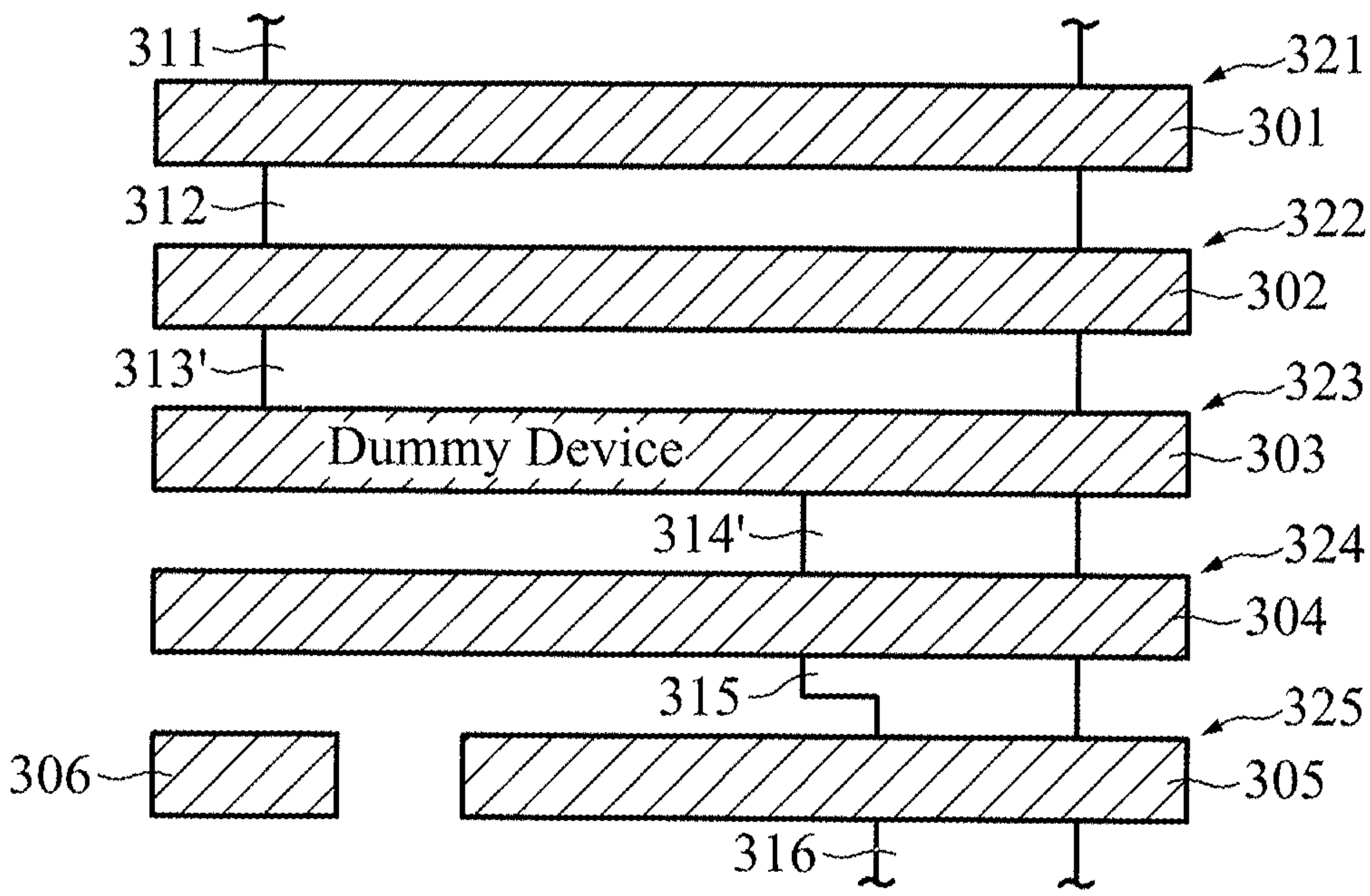

311
312
313'
Dummy Device
314'
315
316
306
321
301
322
302
323
303
324
304
325
305

FIG. 3B

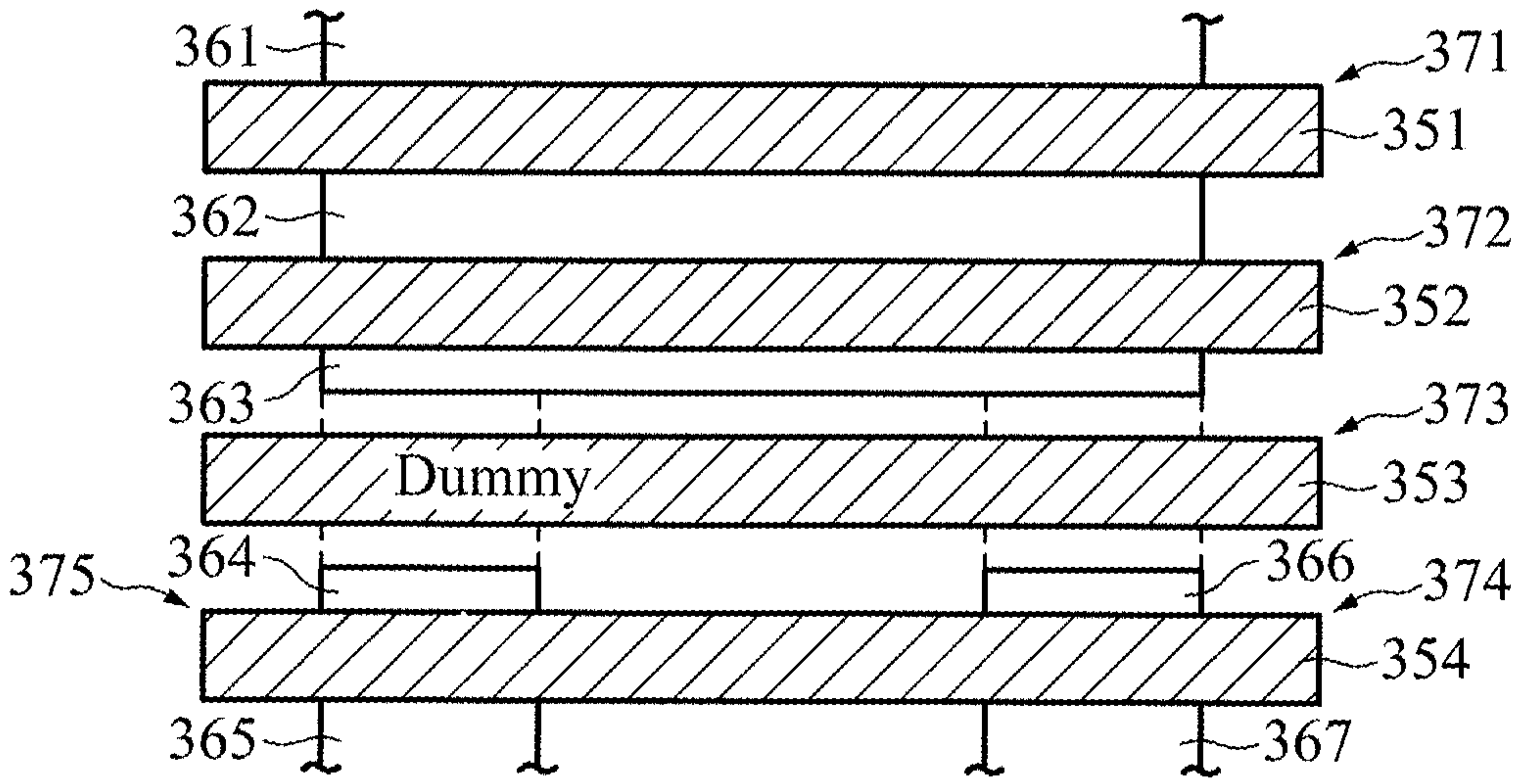

361
371
351
362
372
352
363
373
Dummy
353
375
364
366
374
354
365
367

FIG. 3C

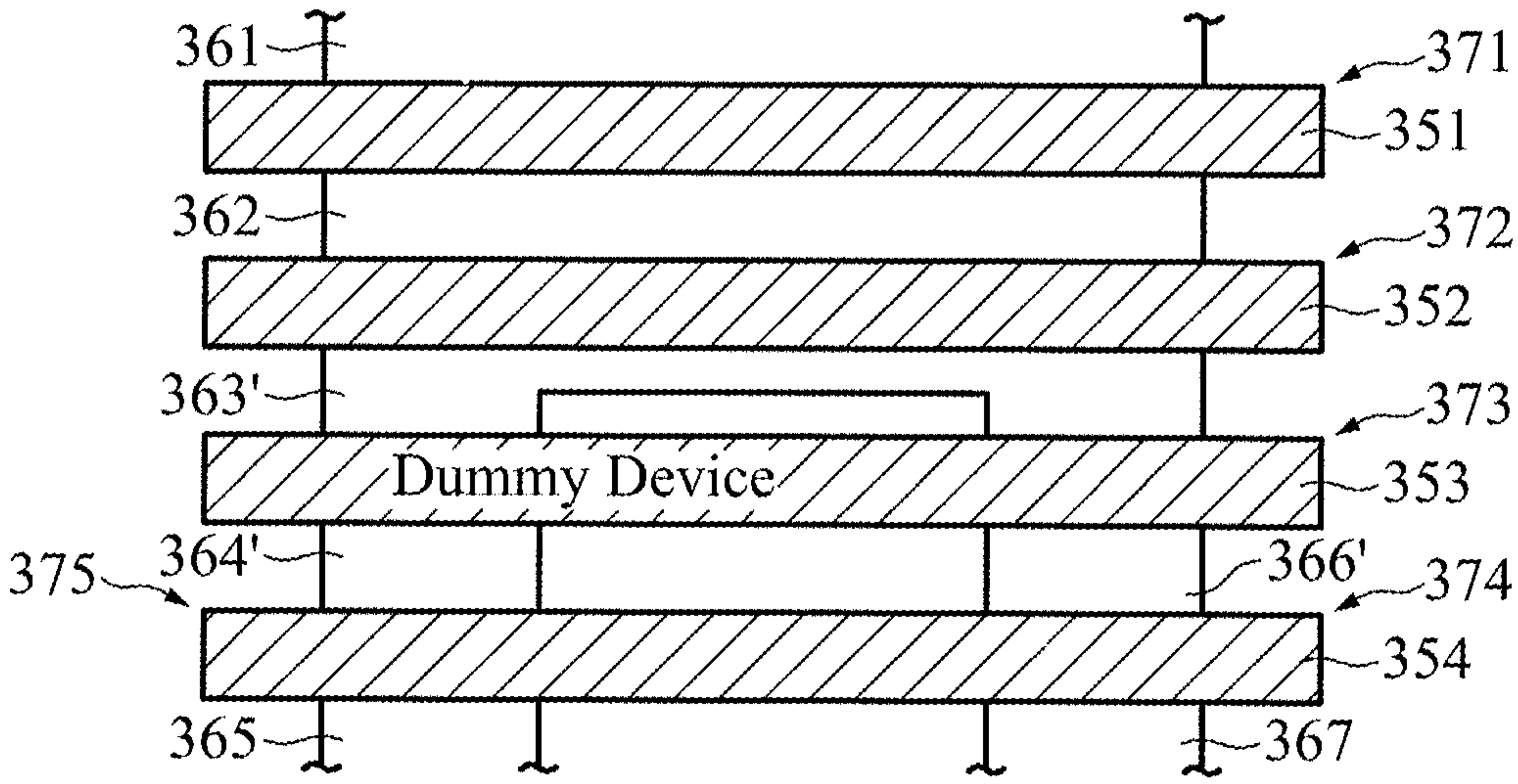

361
371
351
362
372
352
363'
373
Dummy Device
353
375
364'
366'
374
354
365
367

FIG. 3D

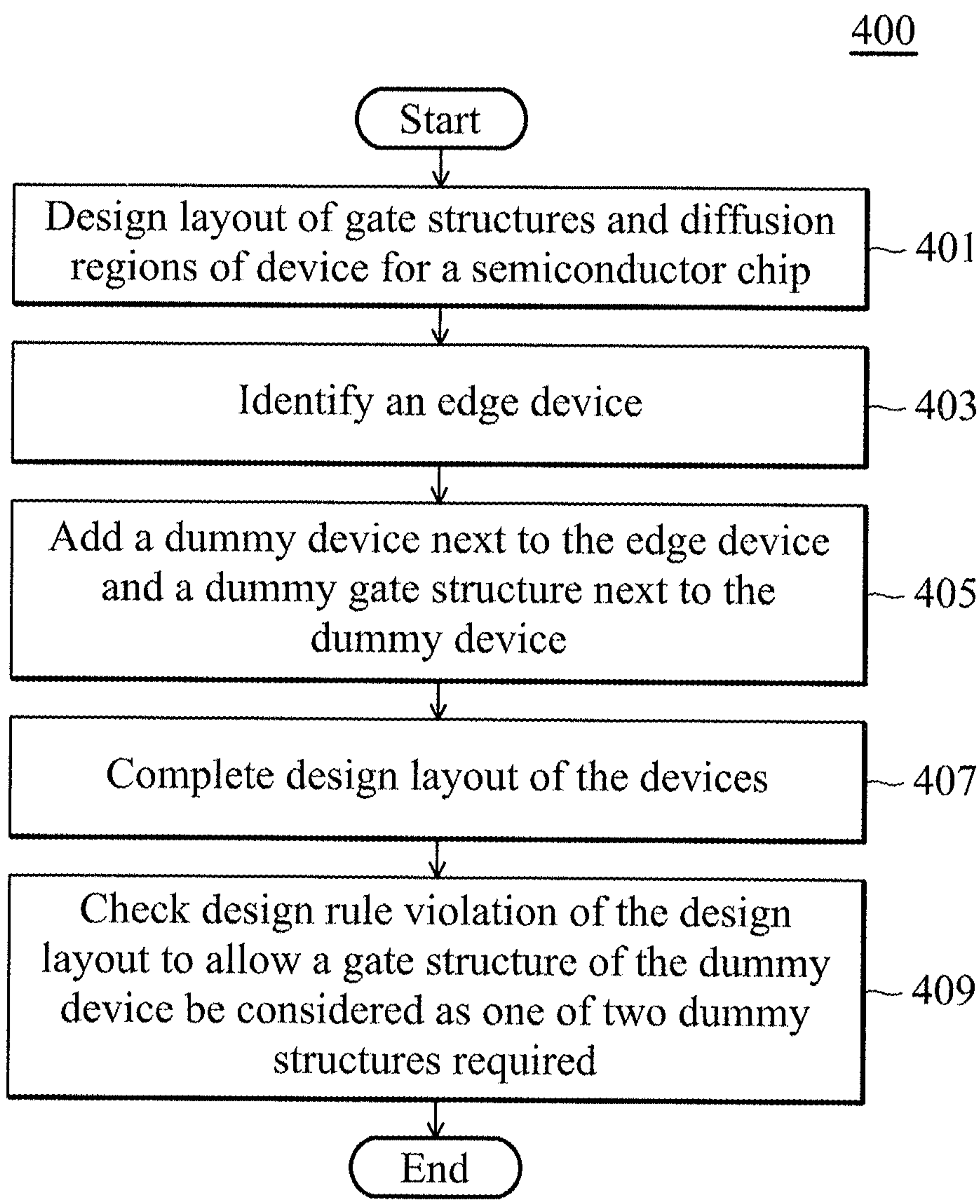

400
Start
Design layout of gate structures and diffusion regions of device for a semiconductor chip
401
Identify an edge device
403
Add a dummy device next to the edge device and a dummy gate structure next to the dummy device
405
Complete design layout of the devices
407
Check design rule violation of the design layout to allow a gate structure of the dummy device be considered as one of two dummy structures required
409
End

FIG. 4A

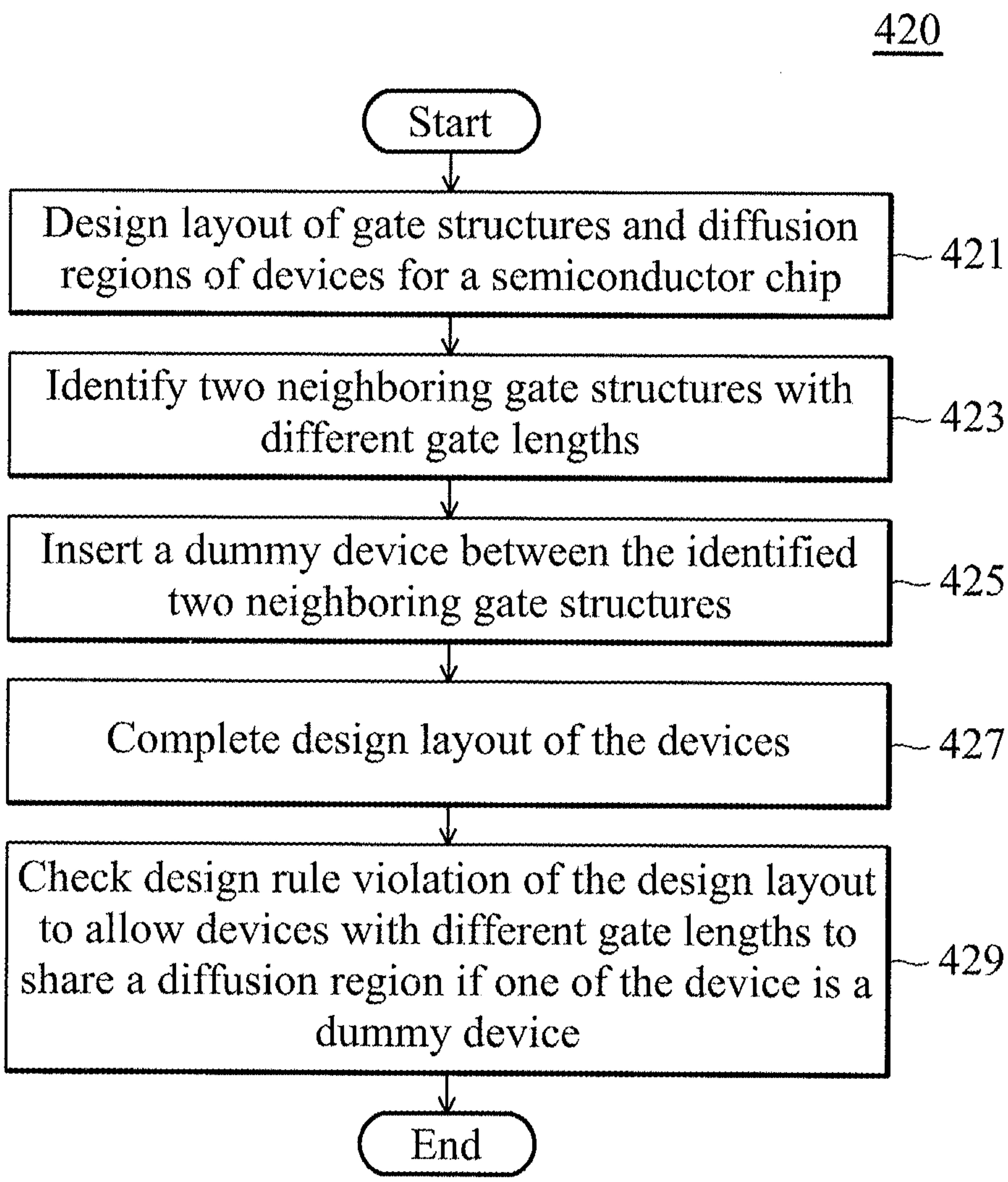

420
Start
Design layout of gate structures and diffusion regions of devices for a semiconductor chip
421
Identify two neighboring gate structures with different gate lengths
423
Insert a dummy device between the identified two neighboring gate structures
425
Complete design layout of the devices
427
Check design rule violation of the design layout to allow devices with different gate lengths to share a diffusion region if one of the device is a dummy device
429
End

FIG. 4B

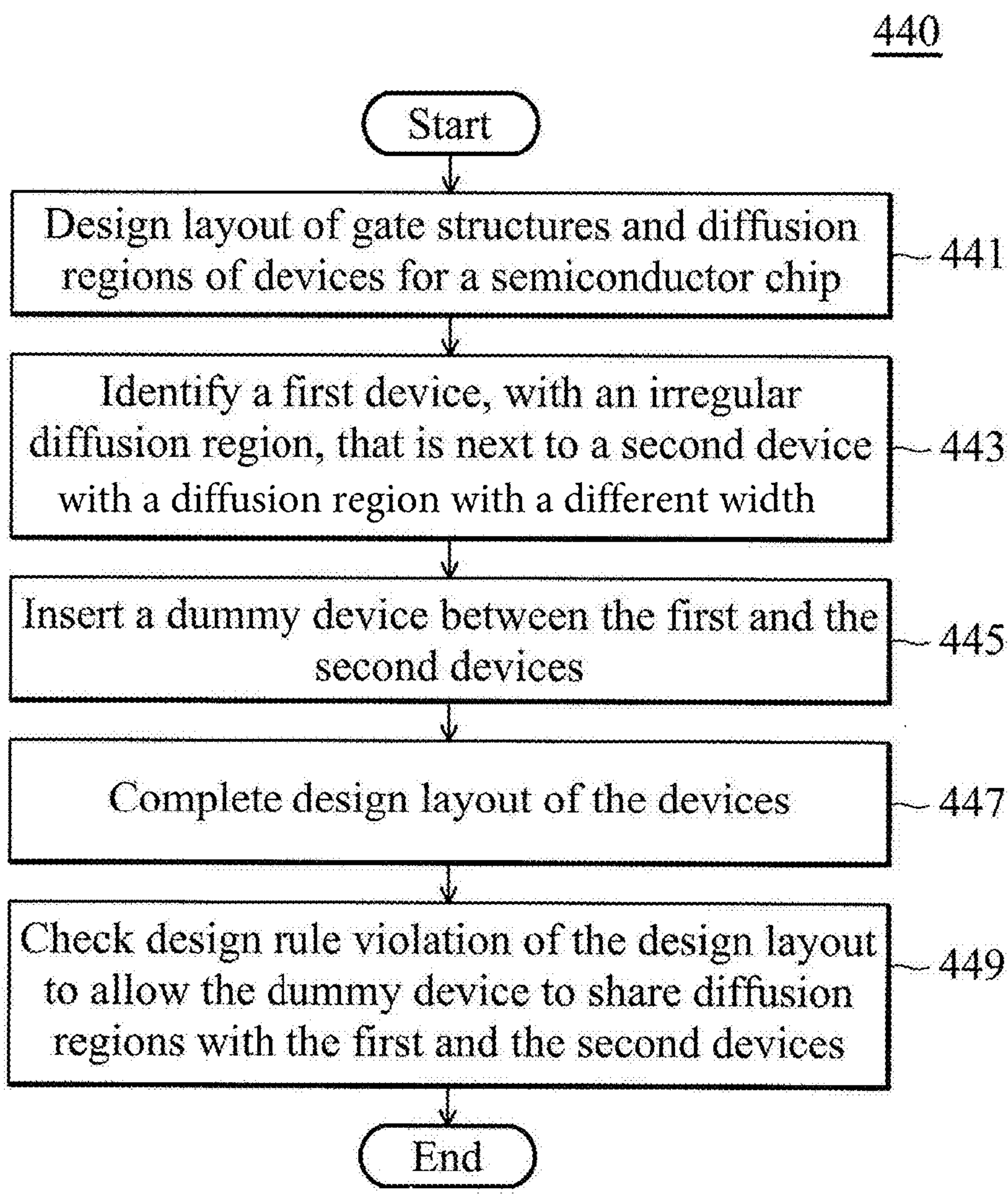

440
Start
Design layout of gate structures and diffusion regions of devices for a semiconductor chip
441
Identify a first device, with an irregular diffusion region, that is next to a second device with a diffusion region with a different width
443
Insert a dummy device between the first and the second devices
445
Complete design layout of the devices
447
Check design rule violation of the design layout to allow the dummy device to share diffusion regions with the first and the second devices
449
End

FIG. 4C

METHOD OF FABRICATING A SEMICONDUCTOR DEVICE

PRIORITY CLAIM

[0001] The present application is a continuation of U.S. application Ser. No. 15/848,333, filed Dec. 20, 2017, which is a divisional of U.S. application Ser. No. 13/949,683, filed Jul. 24, 2013, now U.S. Pat. No. 9,852,249, issued Dec. 26, 2017, which is a divisional of U.S. application Ser. No. 12/879,447, filed Sep. 10, 2010, now U.S. Pat. No. 8,519, 444, issued Aug. 27, 2013, each of which are incorporated by reference herein in their entireties.

FIELD

[0002] This application relates to design rules and, more particularly, to design rules of dummy devices.

BACKGROUND

[0003] The semiconductor integrated circuit (IC) industry has experienced rapid growth.

[0004] Technological advances in IC processing and design have produced generations of ICs where each generation has smaller and more complex circuits than the previous one. As integrated circuit manufacturing technology has developed, and VLSI (very large scale integration) has increased the density of features on a wafer, the process of designing the circuits becomes separated from the process of manufacturing them.

[0005] In recent years, it has been realized that it is important, at the design stage, to take into account the particularities of the processes that will be used to manufacture the integrated circuits. More particularly, it is desirable to design the integrated circuits so that the various processes involved in manufacturing the devices are optimized, while at the same time ensuring low cost, acceptable product quality, reliability, and safety, etc. This is referred to as applying "design for manufacture" (DFM) techniques or principles. When applying DFM techniques in designing semiconductor integrated circuits, the designer is concerned about how the various aspects of the circuit design affect the yield. Different factors can introduce yield loss and/or device performance. People in charge of manufacturing the ICs could specify design rules that integrated circuit designers must comply with in order to produce a useable final product with good yield. It is within this context the following disclosure arises.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The present disclosure will be readily understood by the following detailed description in conjunction with the accompanying drawings, and like reference numerals designate like structural elements.

[0007] FIG. **1**A shows a top layout view of a device area **100**, in accordance with some embodiments.

[0008] FIG. **1**B shows a cross-sectional and schematic view of the device area of FIG. **1**A after the layout is used to manufacture devices, in accordance with some embodiments.

[0009] FIG. **1**C shows a cross section of a device region with an edge gate structure, in accordance with some embodiments.

[0010] FIGS. **1**D-**1**G show different embodiments of design layout and device structures with a dummy device next to an edge device.

[0011] FIGS. **2**A-**2**D show different embodiments of design layout of neighboring devices with different gate lengths.

[0012] FIGS. **3**A-**3**D show different embodiments of a device with an irregular-shaped diffusion region near a device with different gate width.

[0013] FIGS. **4**A-**4**C various process flows of designing and verifying a design layout, in accordance with some embodiments.

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

[0014] It is to be understood that the following disclosure provides many different embodiments, or examples, for implementing different features of the disclosure. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0015] As mentioned above, people in charge of manufacturing the ICs could specify design rules that integrated circuit designers must comply with in order to produce a useable final product with good yield. One of such design rules is related to gate structures. FIG. **1**A shows a top layout view of a device area **100**, in accordance with some embodiments. FIG. **1**A shows a number of gate structures, **101**, **102**, **103**, **104**, and **105**, placed above a number of diffusion regions, **111** (not completely shown), **112**, **113**, and **114**. After manufacturing, the gate structures are at least made of a gate layer(s) over a gate dielectric layer(s), in accordance with some embodiments. The gate layer can be made of polysilicon. Even for replacement gates, the gate layer is first deposited with polysilicon, which is later removed and replaced with another type of gate material(s). For simplicity of discussion, we will call the gate structures, **101**, **102**, **103**, **104**, and **105**, of FIG. **1**A polysilicon lines.

[0016] Diffusion region **111** is at the edge of the drawing and is not completely shown. The widths of the diffusion regions (or implant regions), **112**, **113**, and **114**, are "A", "B", and "C" respectively. In some embodiments, the space between two neighboring polysilicon lines, such as between **101** and **102**, between **102** and **103**, between **103** and **104**, and between **104** and **105**, are equal. In some embodiments, the width of polysilicon lines **101**, **102**, **103**, **104**, **105**, is equal to be "D". Gate structures **101**, **102**, and **103** form transistors, **121**, **122**, and **123** with diffusion regions **111**, **112**, **113**, and **114**.

[0017] FIG. **1**B shows a cross-sectional and schematic view of the device area **100** cut along PP line in FIG. **1**A after the layout is used to manufacture devices, in accordance with some embodiments. FIG. **1**B shows cross sections of polysilicon lines, **101**, **102**, **103**, **104**, and **105**, with a dielectric layer **130** underneath. The diffusion regions **111**, **112**, **113**, **114** define regions that are implanted with N-type or P-type dopants, which can be thermally treated afterwards and diffuse to (and extend to) areas under portions of polysiliocn lines **101**, **102**, and **103** to become actual diffusion regions **131**, **132**, **133**, and **134**. The type of dopants used for implant in regions **111**, **112**, **113**, **114** depends on the type of devices **121**, **122**, and **123**. If devices (or transistors) **121**, **122**, and **123** are NMOS (or N-type metal-oxide-semiconductor), the dopants implanted in regions **111**, **112**, **113**, **114** are N-type dopants. Similarly, if the devices are PMOS (P-type MOS), the dopants are P-type. The gate dielectric layer **130** can be made of a single dielectric material or be made of a composite layer (more than one layer) with more than one dielectric material.

[0018] In FIGS. **1**A and **1**B, polysilicon lines (or structures) **104** and **105** are dummy structures, which are placed next to polysilicon structure **103** according to a design rule. The polysilicon structure **103** defines the gate of transistor **123** and is the last (or end) transistor gate structure in a row of transistors, **101**, **102**, and **103**. To ensure good process uniformity, the design rule specifies that two dummy polysilicon structures, such as structure **104** and **105**, need to be placed next to polysilicon structure **103**. Without the two dummy polysilicon structures, the edge polysilicon structure **103** could suffer patterning and etching non-uniformity due to edge effects. Further, pre-metal dielectric (PMD) layer near the end polysilicon structure could also suffer from local non-uniformity issue. For example, FIG. **1**C shows a substrate **155** with **3** gate structures **151**, **152**, and **153** covered by a PMD layer **156**, with the edge of the PMD layer shown by dotted line **154**. After chemical-mechanical planarization (CMP) (shown by edge line **157**), there is a local slope near edge gate structure **153** in region "E", which could be a result of local stress experienced by the polishing pad due to the end of polysilicon structures. The slope in region E can make contact patterning more challenging. For advanced technologies, such as 65 nm, 40 nm, 28 nm, 20 nm, or below, the contact size become smaller and smaller. If a contact needs to be made on or near region E, the slope could make patterning of contact problematic and could affect the yield of contacts. Therefore, the design rule specifies that two extra dummy polysilicon structures be added next to the edge structure to overcome (or prevent) process uniformity issues.

[0019] According to the design rule, two dummy polysilicon structures **104** and **105** are added next to structure **103**. Transistor **123** is at the edge of a number of transistors, including structures **121**, **122**, and **123**. If the spacing between polysilicon lines, **101**, **102**, **103**, and **104**, is the same, the length of diffusion "C" would be shorter than length of diffusion "A" and "B", as shown in FIGS. **1**A and **1**B. The shorter length of diffusion (LOD) and additional diffusion edge effect along edge **116** of diffusion region **114**, compared to diffusion regions such as **111**, **112** and **113**, could make transistor **123** behave less well than expected, in comparison to transistors **101**, **102** and **103**. Even if the spacing between lines, **101**, **102**, **103**, and **104**, is not the same and "C" is about the same as either "A" or "C", the diffusion edge issue related to edge **116** still exists.

[0020] To resolve the LOD and edge effect issues related to diffusion region **114** (or region **134**) of transistor **123**, a dummy device **126** can be inserted between device **123** and dummy gate structure (or polysilicon line) **104**, as shown in FIGS. **1**D and **1**E in accordance with some embodiments. FIG. **1**E shows a cross-sectional view of structures of FIG. **1**D after the layout of FIG. **1**D is used to create device structures, in accordance with some embodiment. The dummy device **126** includes a gate polysilicon structure **106** and a diffusion region **114'**, which is shared with transistor **123**, and a diffusion region **107** with an edge **116'**. The diffusion region **114** of FIGS. **1**A and **1**B with a length "C" is extended to diffusion region **114'** with a length "C", which does not have an edge **116**. In some embodiments, the diffusion region **114'** has a length "C" equal to or greater than length "A" or "B". Since transistor **126** is a dummy device, the shorter diffusion length "E" of diffusion region **117** and the additional edge (with edge effect) **116'** would not affect overall device performance or yield of the chip. The dummy transistor **126** needs to be inactivated. If transistor **126** is an NMOS, the gate of transistor **126** is connected to Vss to deactivate the device. If transistor **126** is a PMOS, the gate of transistor **126** is connected to Vdd to deactivate the device.

[0021] By inserting a dummy transistor (or device) **126**, the LOD and edge effect issues related to transistor **123** are resolved. However, transistor **126** introduces an extra polysilicon structure **106** and a region between polysilicon structures **106** and **104**, which includes an extra diffusion region **117**. The polysilicon structure **106** and the region between polysilicon structures **106** and **104** take extra space (or real estate) on the substrate.

[0022] As mentioned above, transistor **126** is a dummy device and its performance is not important. Therefore, the polysilicon structure **106** could be treated as a dummy polysilicon. As a result, only one additional polysilicon structure needs to be placed next to dummy polysilicon structure **106**. FIG. **1**F shows the dummy polysilicon structure **105** being removed, in accordance with some embodiments, and only dummy polysilicon structure **104** remains. FIG. **1**F shows that the surface area **160** previously occupied by polysilicon structure **105** and the space (region **155**) between polysilicon structures **104** and **105** are freed up (or saved).

[0023] FIG. **1**G shows two device regions **100** and **170**, in accordance with some embodiments. Device region **100** has been described above. Device region **170** is similar to device region **100**, with transistor **173** being a transistor at the edge of an area of devices, including transistors **172**, and **173**. Transistor **153** has a gate structure **153**. To resolve the LOD and edge effect issues related to edge transistor **173**, a dummy device **176** is placed next to transistor **173**. Dummy device **176** has a gate structure (polysilicon) **176**. To follow the design rule of two dummy polysilicon structures placed next to an edge gate structure, device region **170** also includes dummy polysilicon structures **154** and **157**, placed next to gate structure **156**. As described above, since the gate structures **106** and **156** of dummy devices **126** and **176** can be considered as dummy polysilicon structures, dummy polysilicon structures **105** and **157** are not needed and the spaces **155** and **181** between these dummy structures and neighboring dummy polysilicon structure **104** that would have been needed according to the existing design rules could have been saved.

[0024] A further application of the concept can be seen in FIG. **1**G. If device regions **100** and **170** are placed next to each other, only one dummy polysilicon structure, such as structure **104**, is needed between dummy gate structures **106** and **156** of dummy devices **126** and **176**. Dummy structure **104** can be used as a dummy structure for edge device **173**. Therefore, dummy structure **154** and space **182** are not needed and space can be saved.

[0025] For advanced technologies, more devices are needed to perform more tasks in a single chip and the real estate on the chip is very valuable. By treating gate polysilicon structures of dummy devices as dummy polysilicon structures placed next to edge devices to resolve processing and device concerns, precious space on chips can be saved.

[0026] Another design rule is related to diffusion regions (or implant regions). The design rule specifies that transistors with different gate lengths (or widths) cannot share diffusion regions. FIG. 2A shows a top layout view of a device area **200**, in accordance with some embodiments. FIG. 2A shows a transistor **221** with a polysilicon structure **201** with a gate length "L" of 35 nm. The polysiliocn structure **201** is placed between a diffusion region **211** and another diffusion region **212**. FIG. 2A also shows a transistor **223** near transistor **221**. The transistor **223** has a polysilicon structure **203** with a gate length of 30 nm. The polysilicon structure **203** is placed between a diffusion region **213** and another diffusion region **214**. The design rules specify that gate structures with different gate lengths (30 nm for gate poly **203** and 35 nm for gate poly **201**) cannot be place next to each other. If transistors with different gate lengths are placed next to each other, during the lithography process, the gate lengths of these two neighboring gate structures might not yield the desired respective values (30 nm and 35 nm respectively). By placing a dummy polysilicon structure between these two gate structures with different lengths, more accurate dimensions of these two gate structures can be achieved.

[0027] Due to the requirement of separation, a dummy polysilicon structure **202** is placed between polysilicon structure **201** and polysilicon structure **203**. The dummy polysilicon structure **202** has a length of 35 nm or 30 nm, in accordance with some embodiments. After patterning process, the gate length of dummy polysilicon structure **202** might not be at the target value. However, with the insertion of the dummy polysilicon structure **202**, the lengths of gate poly **201** and gate poly **203** would more likely to be at their respective target values.

[0028] As described above in FIGS. 1A and 1B, edge diffusion regions, such as region **114** has LOD and edge effect issues. Similarly, diffusion regions **212** and **213** also have LOD and edge effect issues. To resolve or reduce such issues, polysilicon structure **202** can be turned into a gate structure and become part of a dummy device **222**, as shown in FIG. 2B (layout **220**) in accordance with some embodiments. As mentioned above, since device **222** is a dummy device, it would be tied to either to Vdd or Vss depending on whether it's an NMOS or a PMOS. Device **222** is formed by extending the diffusion region **212** all the way to polysilicon structure **202** to become region **212'**. Diffusion region **213** is changed to diffusion region **213'** to allow a new diffusion region **243** to be next to polysilicon structure **202**. By expanding the diffusion region **212** to become diffusion region **212'**, the LOD and edge effect issues related to diffusion region **212** (or transistor **201**) are resolved. However, the LOD and edge effect issues for diffusion region **213** (or transistor **223**) are not completely resolved.

[0029] FIG. 2C shows another layout design **240** that can resolve LOD and edge effect issues for diffusion region **213**, in accordance with some embodiments. In the layout design **240** shown in FIG. 2C, the diffusion region **213"** next to transistor **223** is extended completely to the edge of polysilicon structure **202**; therefore, the LOD and edge effect issues related to diffusion region **213"** are resolved. However, the diffusion region **212"** has an extra diffusion region **242** in comparison to diffusion region **212**. The extra diffusion region **242** could impact the device performance for transistor **221**. Whether to choose design (or layout) **220** or **240** depends on which device (transistor **221** or **223**) is more important. If the performance of transistor **221** is more important, design **220** should be chosen. On the other hand, if the performance of transistor **223** is more important, design **240** should be chosen. Since transistor **222** is a dummy device, its performance is not important; modifying the design rule to allow a diffusion region to be shared with diffusion region(s) of a dummy device with a different width should not affect the device performance. In some embodiments, the width of polysilicon structure **202** of dummy device **222** is drawn at 30 nm or 35 nm.

[0030] As mentioned above, transistor **222** is a dummy device and its performance is not important. Another option of resolving LOD and edge effect issues for transistors **221** and **223** (or diffusion regions **212** and **213**) is shown in FIG. 2D, in accordance with some embodiments. FIG. 2D shows that diffusion region **212** of FIG. 2A is extended to become region **212'** and diffusion **213** of FIG. 2A is extended to become **213"**. Both regions **212'** and **213"** maintain the length of diffusion regions of the original design. As a result, both transistors **221** and **223** have LOD and edge effect issues of their respective diffusion regions **212** and **213** resolved.

[0031] Another design rule is related to restriction on shapes of diffusion regions (or implant regions). The design rule specifies that in shared diffusion regions of devices cannot have more than one shared diffusion region that has an irregular shape (or L shape, or non-rectangular shape, or odd shape). FIG. 3A shows a top layout view of a device area **300**, in accordance with some embodiments. Device area **300** includes transistors **321**, **322**, **324**, and **325**. Transistors **321** and **322** are made of gate structures **301** and **302** respectively, and include diffusion regions **311**, **312** and **313** on either side of transistors **321** and **322** respectively. Transistors **324** and **325** are made of gate structures **304** and **305** respectively, and include diffusion regions **314**, **315** and **316** on either side of transistors **324** and **325** respectively. The width of the diffusion regions **311**, **312**, and **313** is "W_1", which is different from the widths of diffusion regions **314** (W_2) and **316** (W_3). The width of diffusion region **315** is hard to define due to the odd shape (or L shape) of the diffusion region. The shape of diffusion region **315** is allowed according to the design rule. However, the design rule allows only one such region in a device region, such as the region with transistors **324** and **325**, with shared diffusion regions, such as diffusion regions **314**, **315**, and **316**. Irregular shaped diffusion region, such as diffusion region **315**, makes device simulation difficult and hard to match the real performance of the devices, including devices **324** and **325**. However, a single "L" shaped diffusion region is considered manageable and allowed according to the design rules. Although an "L" shaped (or irregular shaped) diffusion region is allowed, the design rule specifies that another irregular shaped diffusion region in the same device region is not allowed. As a result, diffusion region **314** is separated from diffusion region **313** by a dummy gate structure **303**.

[0032] As mentioned above, there are LOD and edge effect issues associated with diffusion regions, such as region **313** and **314**, which are shortened and have long edges, **343** and **344** respectively. The issues can be solved (or reduced) by turning dummy structure **303** into a dummy device **323** and extending the diffusion regions **313** and **314** to each side of dummy gate structure **303**. The extended diffusion regions **313** and **314** would become regions **313'** and **314'**, as shown in FIG. **3**B, in accordance with some embodiments. Since dummy transistor **323** is not important, the different widths of diffusion regions **313'** and **314'** are of no concern. However, with the creation of dummy device **323**, the extended diffusion regions **313'** and **314'** resolve the LOD and edge effect concerns (or issues) of transistor **322** and **324**. The way to extend diffusion regions **313** and **314** to diffusion regions **313'** and **314'** is only an example. Other ways of extending the diffusion regions, such as the ones shown in FIGS. **2**B and **2**C to focus on the performance of one of the two transistors next to the dummy device **323**, are also possible. As noted above, the gate of dummy device **323** needs to be inactivated by being tied to Vdd or Vss, depending on the type of device **323**.

[0033] FIG. **3**C shows another example of placing a dummy structure **353** between devices **372**, **374**, and **375**, in accordance with some embodiments. If the diffusion region **364** of device **375** and device region **366** of device **374** are extended to diffusion region **363** (see dotted lines in FIG. **3**C), the diffusion region **363*** would become "U" shaped, which is considered an irregular shape (not a rectangular shape, or with a single L shape) according to the design rule. As mentioned above, the devices involving diffusion regions **363**, **364**, and **366** would suffer from LOD and edge effect issues. In order to resolve such issues, the dummy polysilicon structure **353** can be turned into a dummy device **373** with the diffusion regions **363**, **364**, and **366** becoming diffusion regions **363'**, **364'**, and **366'**. Since device **373** is a dummy device, its performance is not important. As a result, the design rule can be modified to allow irregular shaped diffusion region next to a dummy device. The embodiment shown in FIG. **3**D is merely an example. Other embodiments are also possible. For example, the diffusion region **363'** could extend all the way to the dummy gate structure **353** of the dummy device **373** in its entire width (similar to the region **313'** of FIG. **3**B).

[0034] FIG. **4**A shows a process flow **400** of designing and verifying a design layout, in accordance with some embodiments. At operation **401**, layout of gate structures and diffusion regions of devices for a semiconductor chip is designed. At operation **403**, an edge device is identified. At operation **405**, a dummy device is added next to the edge device and a dummy gate structure (such as a dummy polysilicon line) is added next to the dummy device. The dummy device shares a diffusion region with the edge device; therefore, the LOD and edge effect issue for the edge device are resolved or reduced. At operation **407**, the design layout of the devices is completed. After the design layout is completed, a design rule check is conducted to make sure all design rules are followed. At operation **409**, design rule violation is checked against the design layout and the design rule allows a gate structure of the dummy device be considered as a dummy gate structure. Examples of layouts and structures are shown in FIGS. **1**A-**1**G, in accordance with some embodiments.

[0035] FIG. **4**B shows a process flow **420** of designing and verifying a design layout, in accordance with some embodiments. At operation **421**, layout of gate structures and diffusion regions of devices for a semiconductor chip is designed. At operation **423**, two neighboring gate structures with different gate lengths are identified. At operation **425**, a dummy device is inserted between the two identified gate structures. The dummy device shares diffusion regions with devices of the two identified gate structures; therefore, the LOD and edge effect issues for the two devices with different gate widths are resolved or reduced. The gate width of the dummy device is the same as one of the two devices with different gate widths. At operation **427**, the design layout of the devices is completed. After the design layout is completed, a design rule check is conducted to make sure all design rules are followed. At operation **429**, design rule violation is checked against the design layout and the design rule allows the dummy device to share a diffusion region with a neighboring gate structure that has a different gate length. Examples of layouts and structures are shown in FIGS. **2**A-**2**D, in accordance with some embodiments.

[0036] FIG. **4**C shows a process flow **440** of designing and verifying a design layout, in accordance with some embodiments. At operation **441**, layout of gate structures and diffusion regions of devices for a semiconductor chip is designed. At operation **443**, a first device with an irregular diffusion region (or non-rectangular or L shaped region) and the first device being next to a second device with a different diffusion width is identified. At operation **445**, a dummy device is inserted between the first and the second devices. The dummy device shares diffusion regions with the first and the second devices; therefore, the LOD and edge effect issues for the first and the second devices are resolved or reduced. At operation **447**, the design layout of the devices is completed. After the design layout is completed, a design rule check is conducted to make sure all design rules are followed. At operation **449**, design rule violation is checked against the design layout. The design rule allows the dummy device to share diffusion regions with the first and the second devices. Examples of layouts and structures are shown in FIGS. **3**A-**3**D, in accordance with some embodiments.

[0037] The layouts, device structures, and methods described above utilize dummy devices to extend the diffusion regions of edge structures and/or non-allowed structures to the dummy device. Such extension of diffusion regions resolves or reduces LOD and edge effect issues. In addition, treating the gate structure of a dummy device next to an edge device also allows only one dummy structure to be added next to the dummy device and saves real estate on the semiconductor chip. The dummy devices are deactivated and their performance is not important. Therefore, utilizing dummy devices to extend the diffusion regions of edge structures and/or non-allowed structures according to design rules allows the resolution or reduction or LOD and edge effect issues without the penalty of yield reduction or increase in layout areas. In some embodiments, the gate lengths of the devices described above are less than 40 nm. In some other embodiments, the gate lengths of the devices described above are less than 35 nm.

[0038] One aspect of this description relates to a method. The method includes designing a first layout including gate structures and diffusion regions of a plurality of active devices, identifying an edge device of the plurality of active devices, and modifying the first layout resulting in a second layout. In some embodiments, modifying the first layout resulting in the second layout includes adding a dummy device next to the edge device, where the dummy device and the edge device have a shared diffusion region; adding a dummy gate structure next to the dummy device; and extending the shared diffusion region to at least the dummy device. In some embodiments, the method further includes performing a design rule check on the second layout, and fabricating, based on the second layout, at least one of a photolithography mask or at least one component in a layer of a semiconductor device. In some embodiments, the performing the design rule check considers a gate structure of the dummy device as one of two dummy gate structures next to the edge device.

[0039] Another aspect of this description relates to a method. The method includes designing a first layout including gate structures and diffusion regions of a semiconductor device, identifying neighboring gate structures having different gate lengths, where the neighboring gate structures include a first gate structure having a first gate length and a second gate structure having a second gate length different from the first gate length. The method further includes modifying the first layout resulting in a second layout including inserting a dummy device between the first gate structure and the second gate structure, and extending a first diffusion region of the first gate structure to the dummy device, where the first diffusion region is shared by the dummy device and the first gate structure. The method further includes performing a design rule check on the second layout and fabricating, based on the second layout, at least one of a photolithography mask or at least one component in a layer of the semiconductor device. In some embodiments, the performing the design rule check includes considering the sharing of the first diffusion region by the dummy device and the first gate structure as complying with a design rule of the design rule check.

[0040] Still another aspect of this description relates to a method. The method includes designing a first layout of gate structures and diffusion regions for a semiconductor device, identifying a first device having a first gate structure and an irregular diffusion region adjacent to a second device having a second gate structure and a diffusion region different from the irregular diffusion region, inserting a dummy device between the first gate structure and the second gate structure resulting in a second layout, wherein a first diffusion region is shared by the dummy device and the first gate structure, a second diffusion region is shared by the dummy device and the second gate structure, the first diffusion region or the second diffusion region has a rectangular shape, and the irregular diffusion region has a non-rectangular shape. The method further includes performing a design rule check on the second layout and fabricating, based on the second layout, at least one of a photolithography mask or at least one component in a layer of the semiconductor device. In some embodiments, the performing the design rule check includes considering the sharing of the first diffusion region by the dummy device and the first gate structure or the sharing of the second diffusion region by the dummy device and the second gate structure as complying with a design rule of the design rule check.

[0041] Various modifications, changes, and variations apparent to those of skill in the art may be made in the arrangement, operation, and details of the methods and systems disclosed. Although the foregoing disclosure has been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the disclosure. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the disclosure is not to be limited to the details given herein, but may be modified within the scope and equivalents of the disclosure.

What is claimed is:

1. A method, comprising:

designing a first layout including gate structures and diffusion regions of a plurality of active devices;

identifying an edge device of the plurality of active devices;

modifying the first layout resulting in a second layout comprising:

adding a dummy device next to the edge device, the dummy device and the edge device having a shared diffusion region;

adding a dummy gate structure next to the dummy device; and

extending the shared diffusion region to at least the dummy device;

performing a design rule check on the second layout, the performing the design rule check considers a gate structure of the dummy device as one of two dummy gate structures next to the edge device; and

fabricating, based on the second layout, at least one of a photolithography mask or at least one component in a layer of a semiconductor device.

2. The method of claim **1**, wherein extending the shared diffusion region to at least the dummy device comprises:

extending the shared diffusion region to at least a first side of the dummy device, the first side of the dummy device being closer to the edge device than a second side of the dummy device.

3. The method of claim **1**, wherein modifying the first layout resulting in the second layout further comprises:

adding an additional diffusion region on a side of the dummy device opposite from the edge device.

4. The method of claim **3**, wherein a length of the additional diffusion region is less than a length of the shared diffusion region.

5. The method of claim **4**, wherein the length of the additional diffusion region is equal to a length of another diffusion region on a side of the edge device opposite from the dummy device.

6. The method of claim **1**, wherein the gate structure of the dummy device has a first gate length and the gate structure of the edge device has a second gate length different from the first gate length.

7. The method of claim **6**, wherein the dummy gate structure has a gate length equal to the first gate length or the second gate length.

8. The method of claim **1**, further comprising deactivating the dummy device.

9. The method of claim **1**, further comprising:

removing at least one dummy gate structure, so that the dummy gate structure corresponds to a single dummy gate structure next to the dummy device.

10. A method, comprising:

designing a first layout including gate structures and diffusion regions of a semiconductor device;

identifying neighboring gate structures having different gate lengths, the neighboring gate structures including a first gate structure having a first gate length and a second gate structure having a second gate length different from the first gate length;

modifying the first layout resulting in a second layout comprising:
inserting a dummy device between the first gate structure and the second gate structure; and
extending a first diffusion region of the first gate structure to the dummy device, the first diffusion region being shared by the dummy device and the first gate structure;
performing a design rule check on the second layout, the performing the design rule check comprises considering the sharing of the first diffusion region by the dummy device and the first gate structure as complying with a design rule of the design rule check; and
fabricating, based on the second layout, at least one of a photolithography mask or at least one component in a layer of the semiconductor device.

11. The method of claim **10**, further comprising:
extending a second diffusion region of the second gate structure to the dummy device, the second diffusion region being shared by the dummy device and the second gate structure, and the first diffusion region and the second diffusion region having different widths.

12. The method of claim **12**, wherein performing the design rule check on the second layout further comprises:
considering the sharing of the second diffusion region by the dummy device and the second gate structure as complying with the design rule of the design rule check.

13. The method of claim **10**, further comprising:
adding another diffusion region between the dummy device and a second diffusion region of the second gate structure, the second diffusion region and the another diffusion region being shared by the dummy device and the second gate structure, and the first diffusion region and the another diffusion region having a same width.

14. The method of claim **13**, wherein performing the design rule check on the second layout further comprises:
considering the sharing of the second diffusion region and the another diffusion region by the dummy device and the second gate structure as complying with the design rule of the design rule check.

15. The method of claim **10**, further comprising deactivating the dummy device.

16. The method of claim **10**, wherein the dummy device has one of the first gate length or the second gate length.

17. A method, comprising:
designing a first layout of gate structures and diffusion regions for a semiconductor device;
identifying a first device having a first gate structure and an irregular diffusion region adjacent to a second device having a second gate structure and a diffusion region different from the irregular diffusion region;
inserting a dummy device between the first gate structure and the second gate structure resulting in a second layout, wherein a first diffusion region is shared by the dummy device and the first gate structure, a second diffusion region is shared by the dummy device and the second gate structure, the first diffusion region or the second diffusion region has a rectangular shape, and the irregular diffusion region has a non-rectangular shape;
performing a design rule check on the second layout, the performing the design rule check comprises considering the sharing of the first diffusion region by the dummy device and the first gate structure or the sharing of the second diffusion region by the dummy device and the second gate structure as complying with a design rule of the design rule check; and
fabricating, based on the second layout, at least one of a photolithography mask or at least one component in a layer of the semiconductor device.

18. The method of claim **17**, further comprising:
extending the first diffusion region of the first gate structure to the dummy device; and
extending the second diffusion region of the second gate structure to the dummy device.

19. The method of claim **15**, further comprising:
extending the first diffusion region of the first gate structure to at least a first side of the dummy device; and
adding an additional diffusion region between the second diffusion region of the second gate structure and a second side of the dummy device,
wherein the additional diffusion region adjacent to the second side of the dummy device is different from the second diffusion region of the second gate structure.

20. The method of claim **17**, further comprising deactivating the dummy device.

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