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(54) **THIN-FILM TRANSISTOR SUBSTRATE, LIQUID CRYSTAL DISPLAY DEVICE INCLUDING THE SAME, AND METHOD FOR PRODUCING THIN-FILM TRANSISTOR SUBSTRATE**

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(21) Appl. No.: **16/662,114**

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H01L 29/45	(2006.01)
H01L 29/423	(2006.01)
H01L 21/441	(2006.01)
H01L 21/471	(2006.01)
H01L 29/66	(2006.01)
G02F 1/1368	(2006.01)

(52) **U.S. Cl.**

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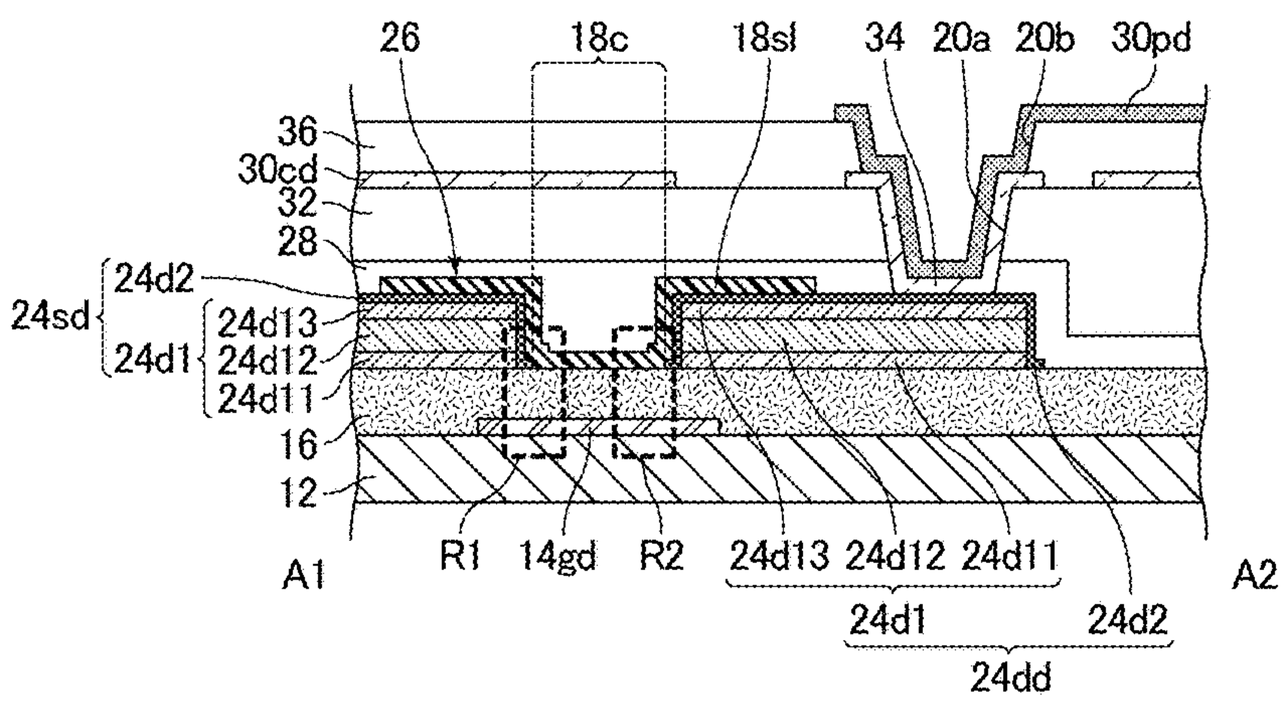
(57) **ABSTRACT**

The present invention provides a thin-film transistor substrate including a base substrate and a thin-film transistor, the thin-film transistor including: a gate electrode; a gate insulating layer; a source electrode and a drain electrode; and an oxide semiconductor layer in this order. The source electrode and the drain electrode each include a first conductive layer and a second conductive layer covering the first conductive layer. The second conductive layer contains at least one element selected from the group consisting of molybdenum, tantalum, tungsten, and nickel. The gate insulating layer in a region between the source electrode and the drain electrode has a smaller thickness than in a region below the source electrode and in a region below the drain electrode.



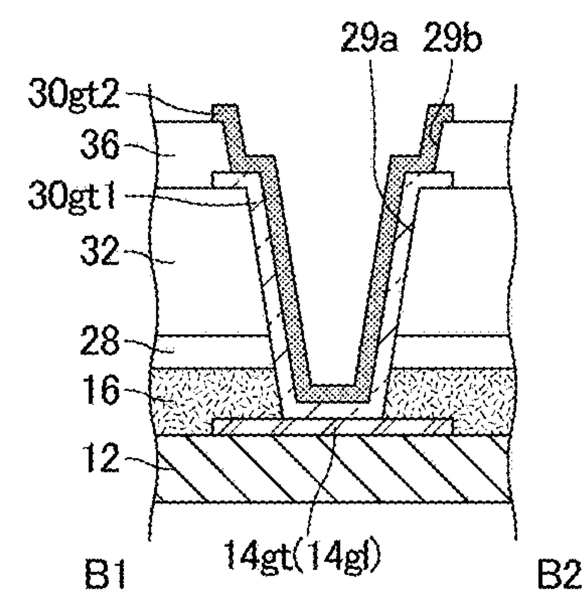


FIG.1

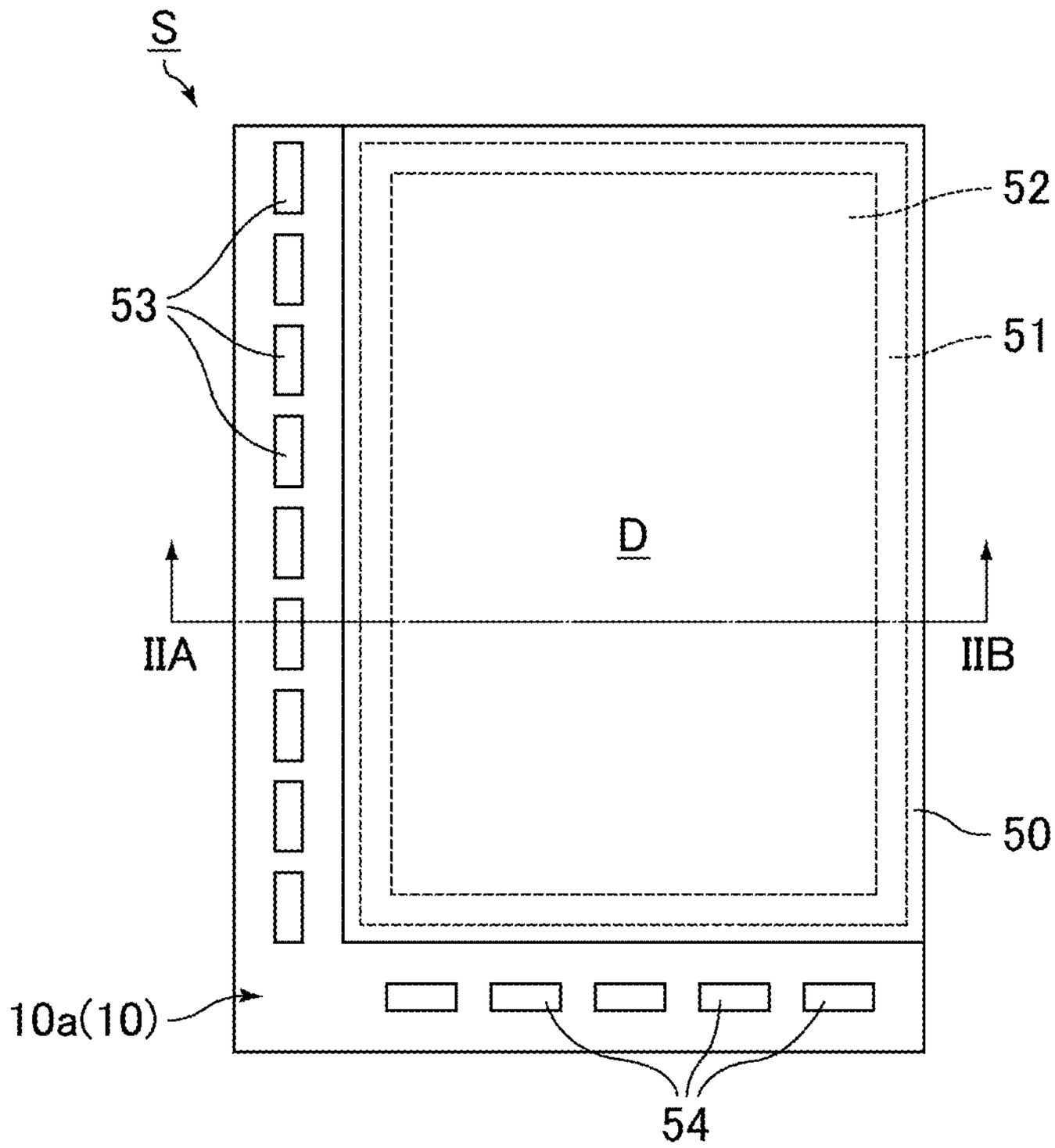

S
52
53
51
D
IIA
IIB
50
10a(10)
54

FIG.2

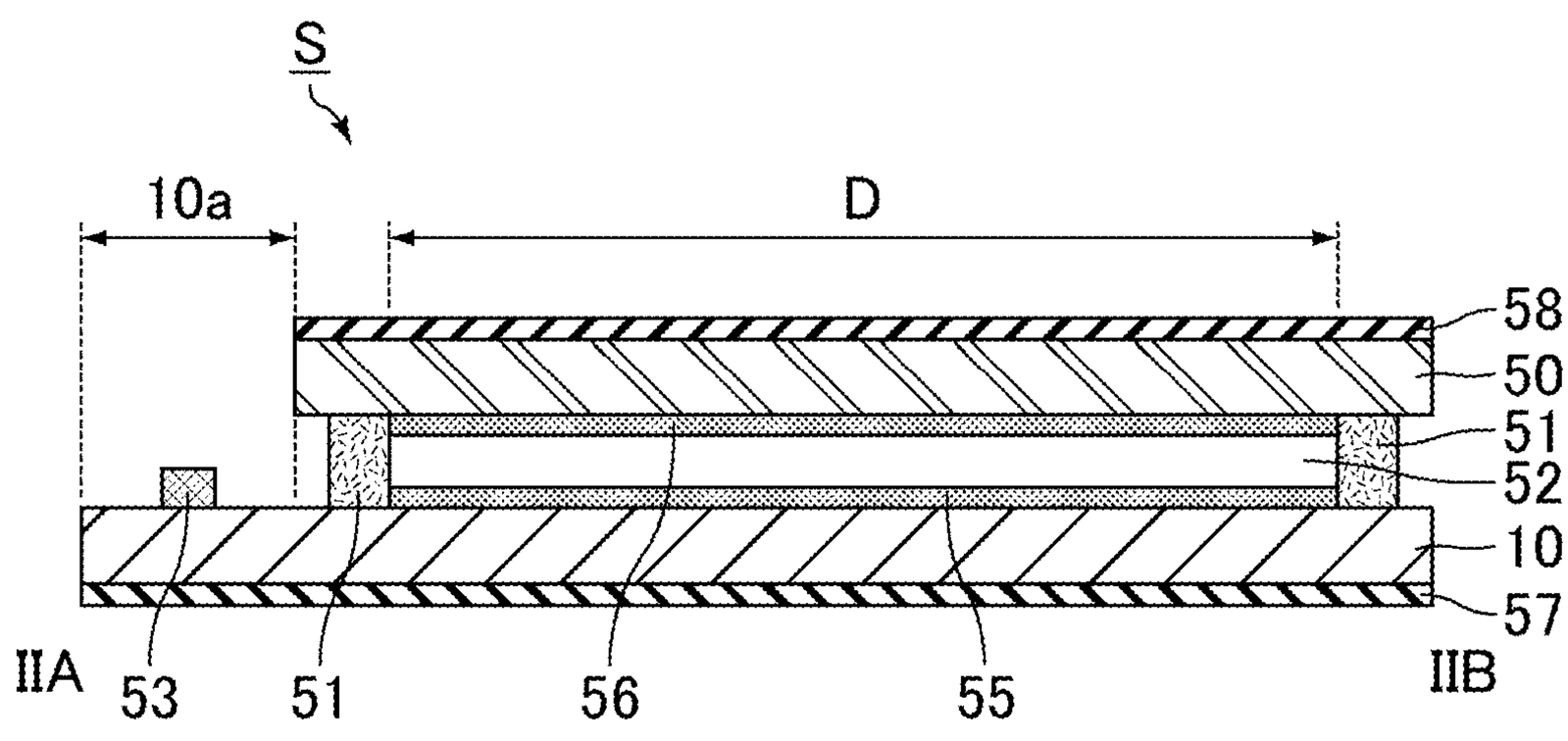

S
10a
D
58
50
51
52
10
57
IIA
53
51
56
55
IIB

FIG.3

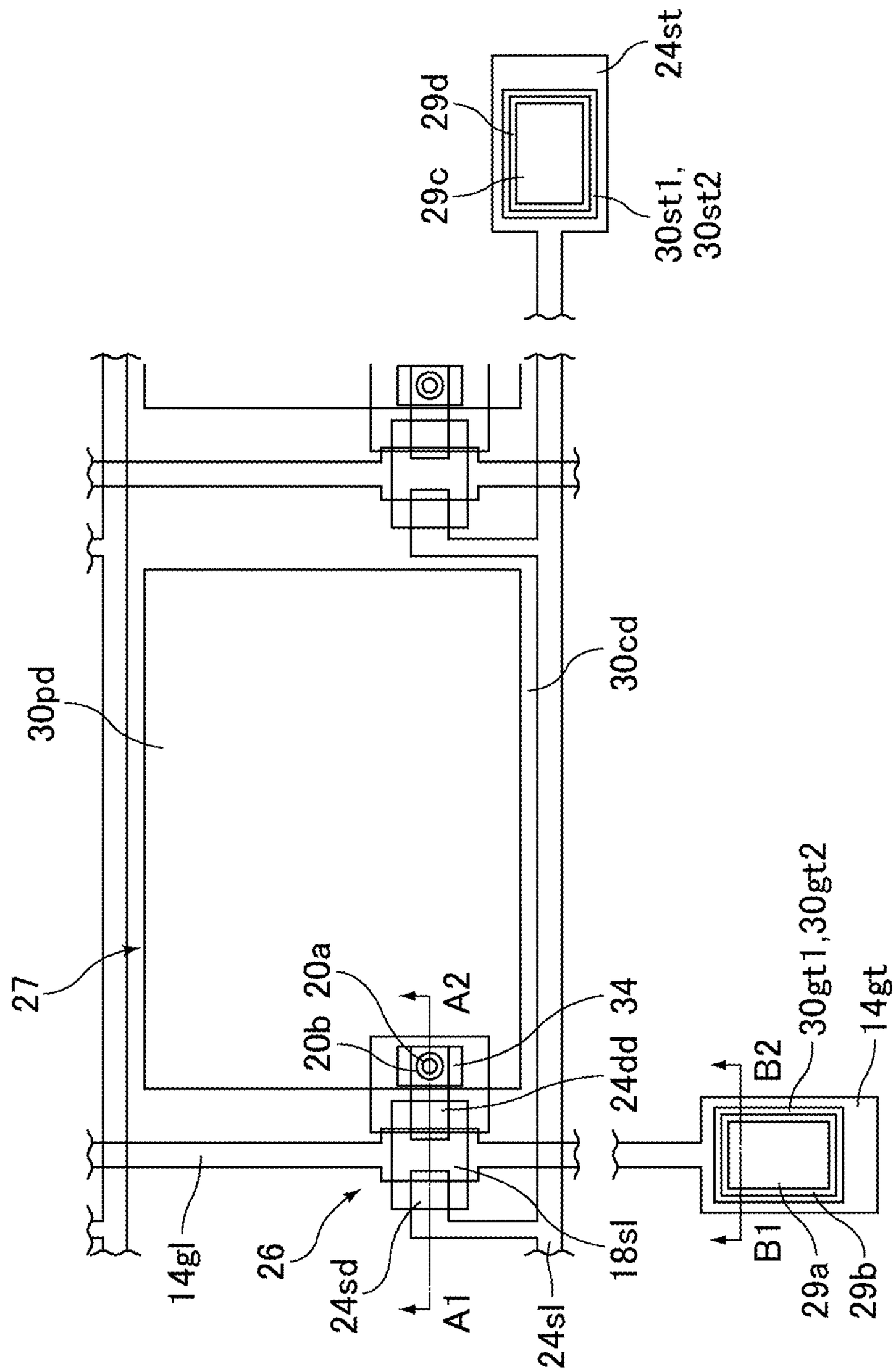

24st
29d
29c
30st1,
30st2
30cd
30pd
27
20a
20b
A2
34
24dd
30gt1,30gt2
14gt
B2
B1
29a
29b
18sl
24sl
A1
24sd
26
14gl

FIG.4

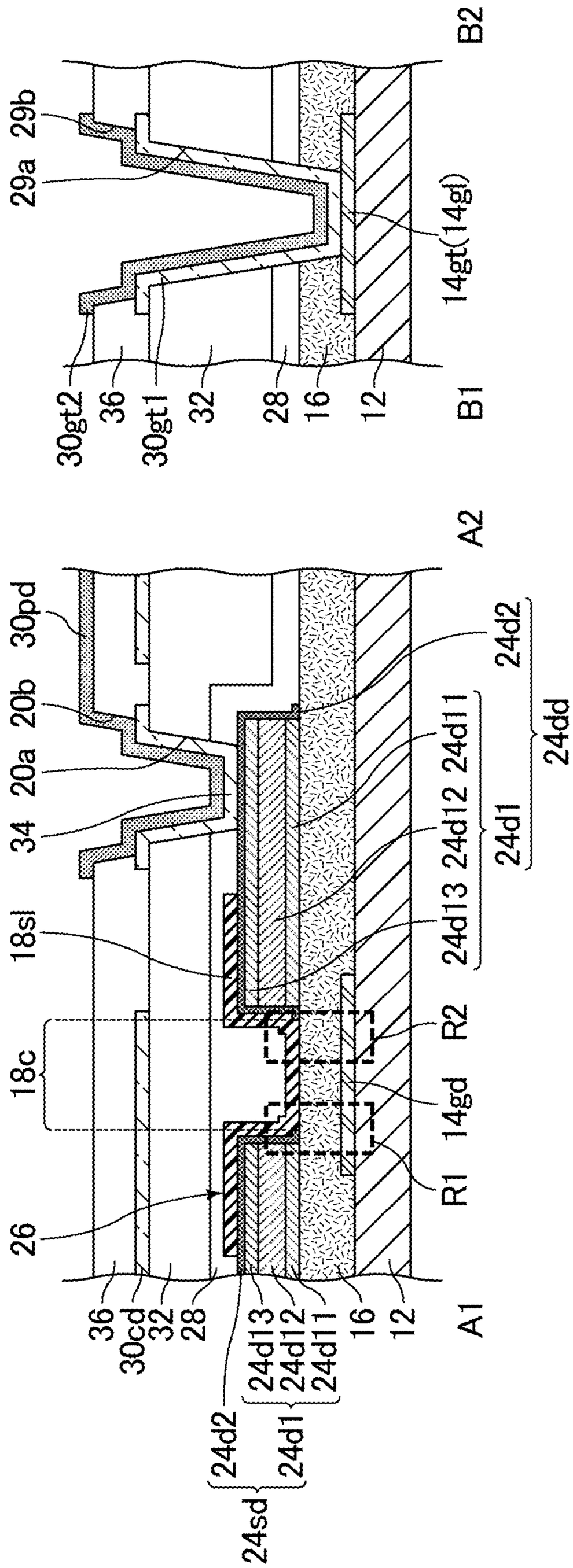

B2
29b
29a
14gt(14gl)
30gt2
36
30gt1
32
28
16
12
B1
A2
30pd
20b
20a
34
18sl
18c
26
24d2
24d11
24d12
24d13
24d1
24dd
R2
14gd
R1
36
30cd
32
28
24d13
24d12
24d11
16
12
A1
24d2
24d1
24sd

FIG.5A

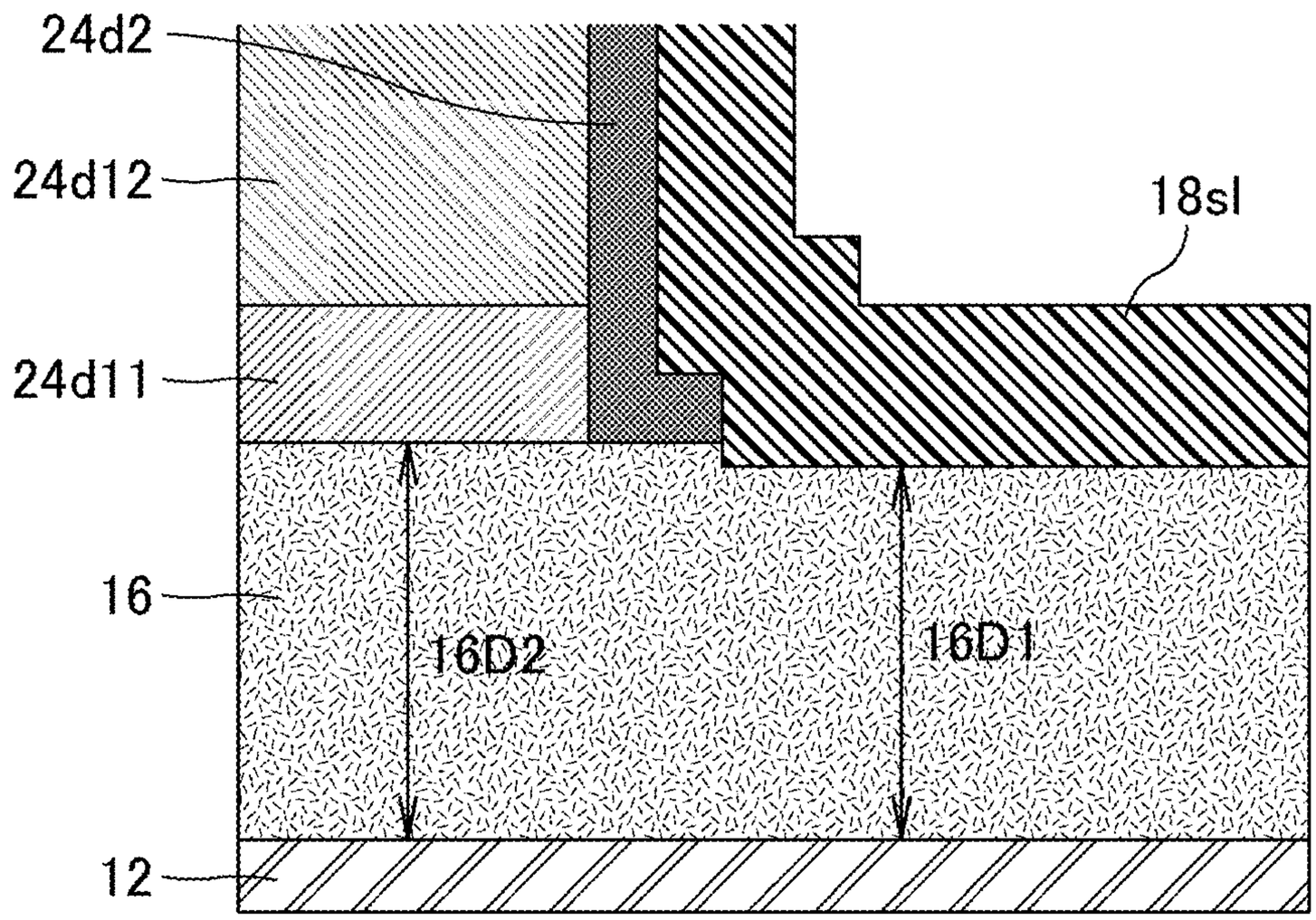

24d2
24d12
18sl
24d11
16
16D2
16D1
12

FIG.5B

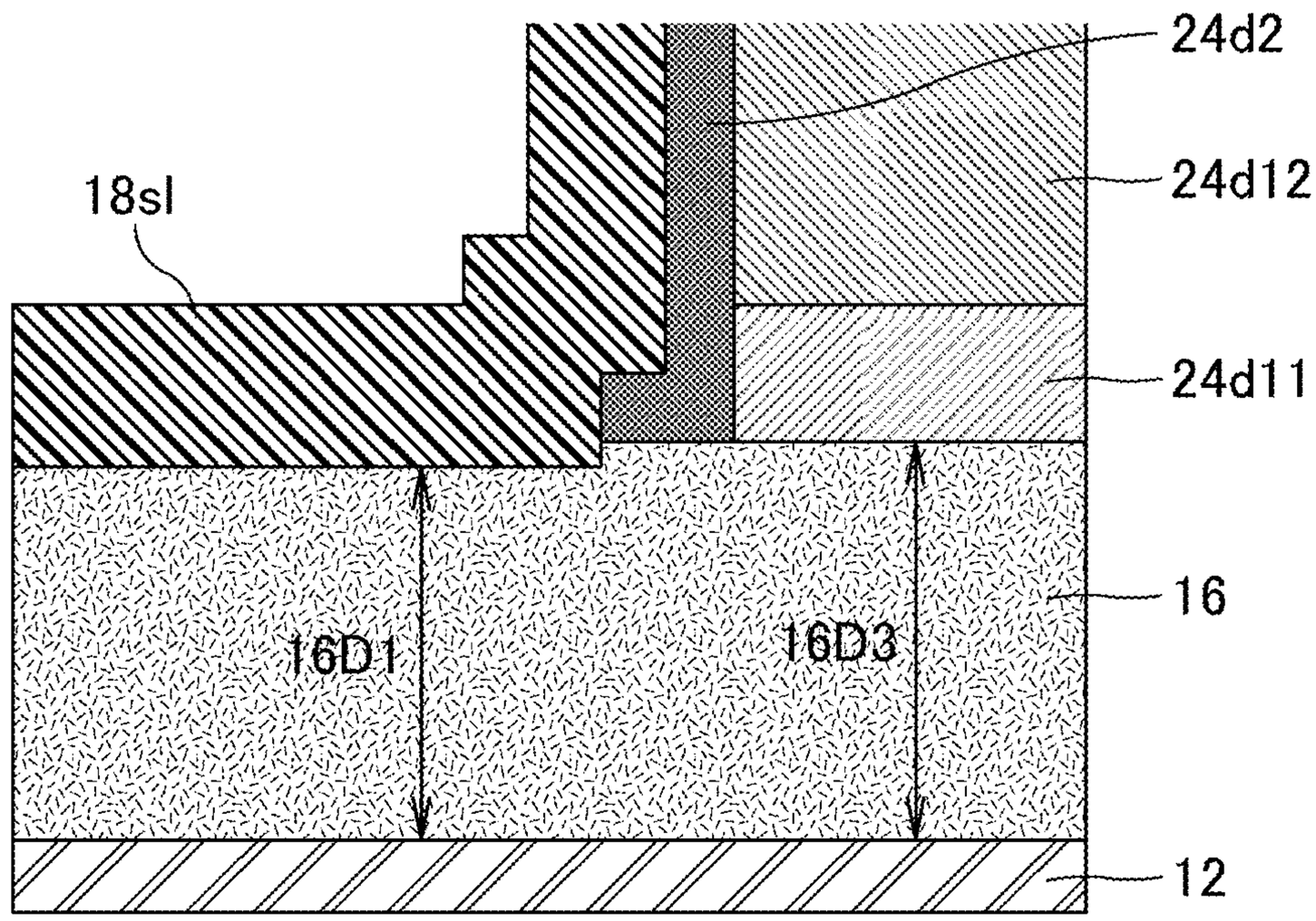

24d2
24d12
18sl
24d11
16
16D1
16D3
12

FIG.6

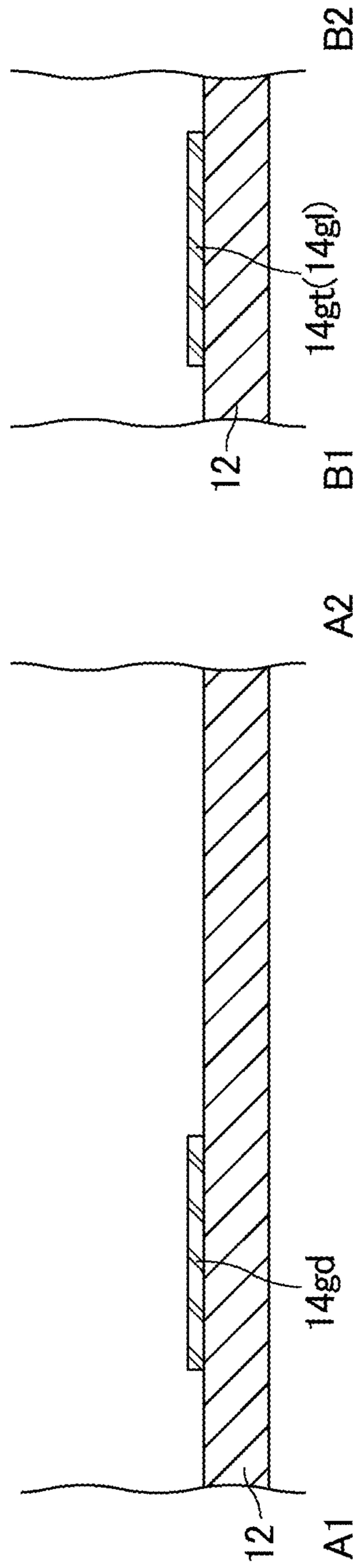

B2
14gt(14gl)
12
B1
A2
14gd
12
A1

FIG.7

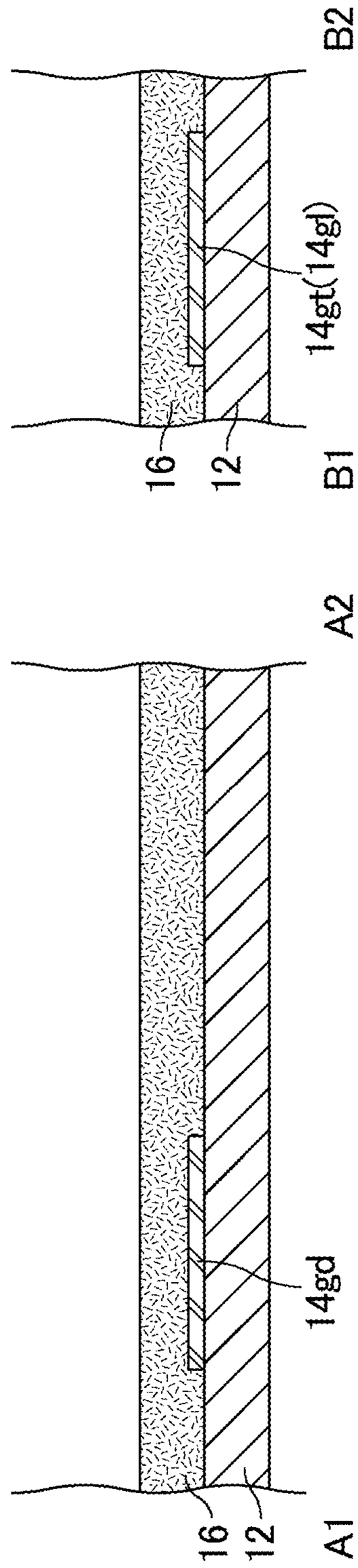

B2
14gt(14gl)
16
12
B1
A2
14gd
16
12
A1

FIG.8

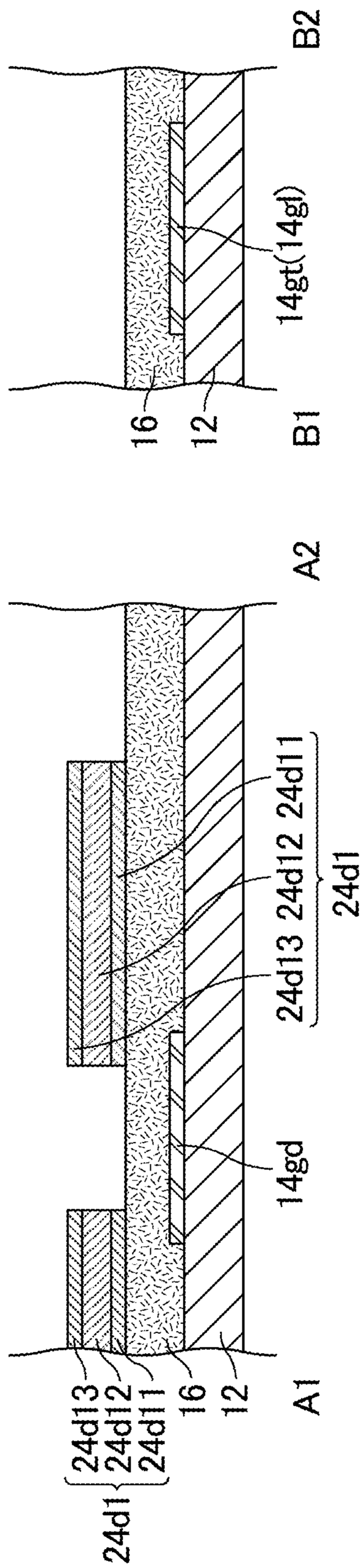

B2
14gt(14gl)
16
12
B1
A2
24d11
24d12
24d13
24d1
14gd
24d13
24d12
24d11
24d1
16
12
A1

FIG.9

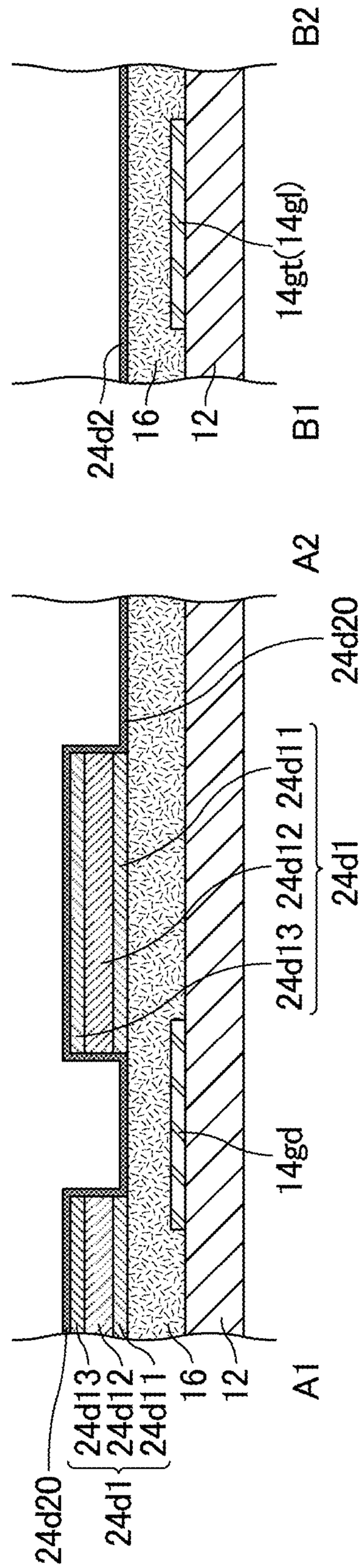

B2
14gt(14gl)
24d2
16
12
B1
A2
24d20
24d11
24d12
24d13
24d1
14gd
24d20
24d13
24d12
24d11
24d1
16
12
A1

FIG.10

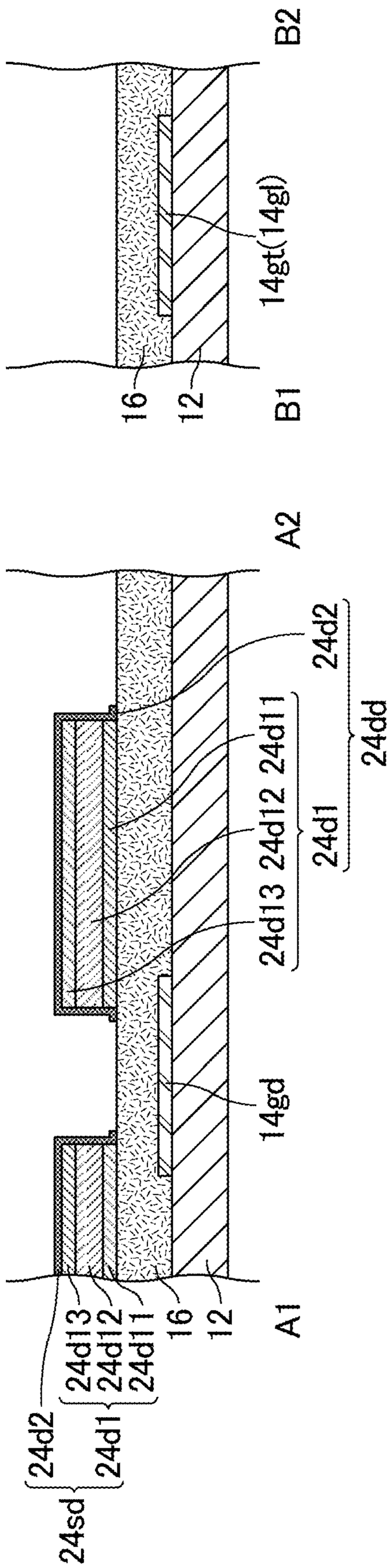

B2
14gt(14gl)
16
12
B1
A2
24d2
24d11
24d12
24d13
24dd
24d1
14gd
24d13
24d12
24d11
16
12
A1
24d2
24d1
24sd

FIG.11

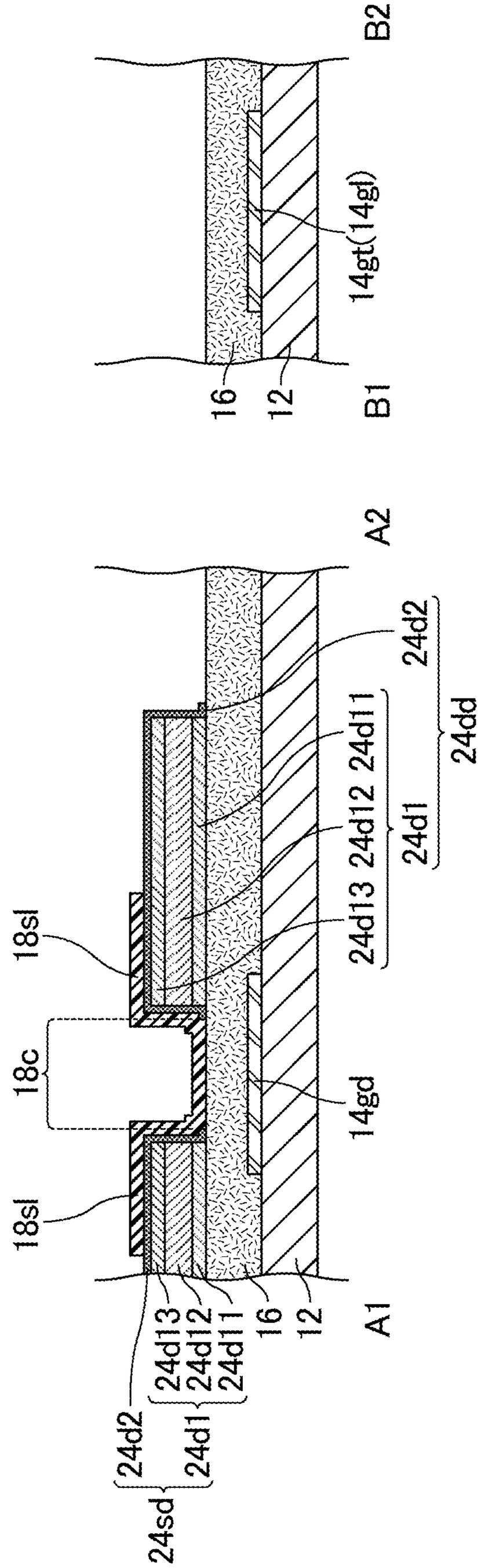

B2
14gt(14gl)
16
12
B1
A2
24d2
24d11
24d12
24dd
24d1
24d13
18sl
18c
14gd
18sl
24d13
24d12
24d11
16
12
A1
24d2
24d1
24sd

FIG.12

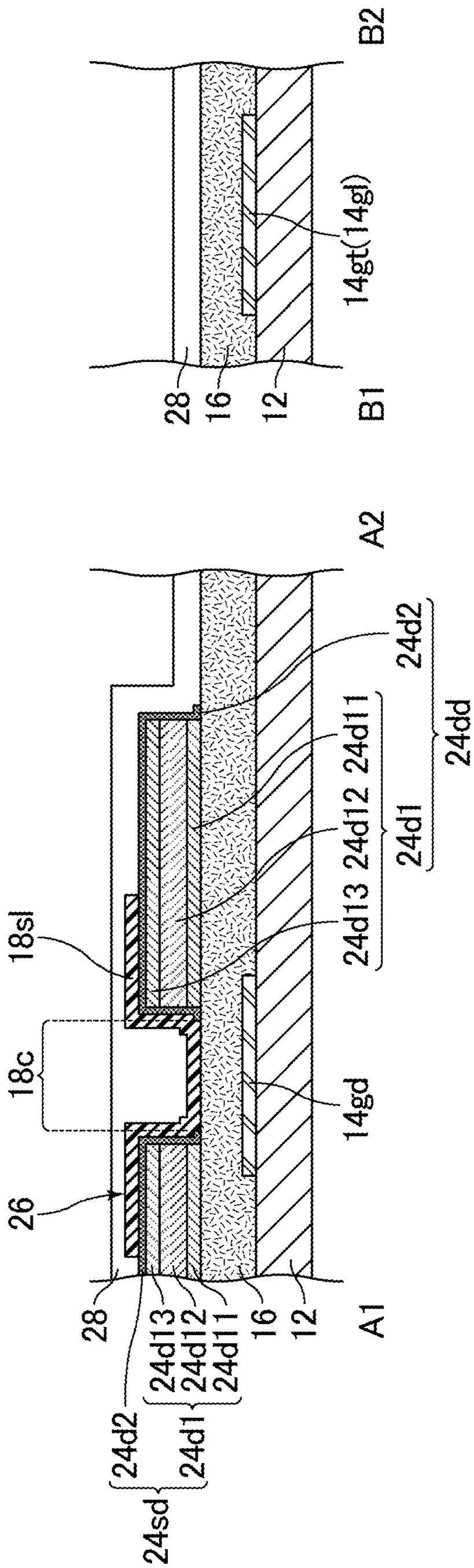

B2
14gt(14gl)
28
16
12
B1
A2
24d2
24d11
24dd
24d12
24d1
24d13
18sl
18c
14gd
26
28
24d13
24d12
24d11
16
12
A1
24d2
24d1
24sd

FIG.13

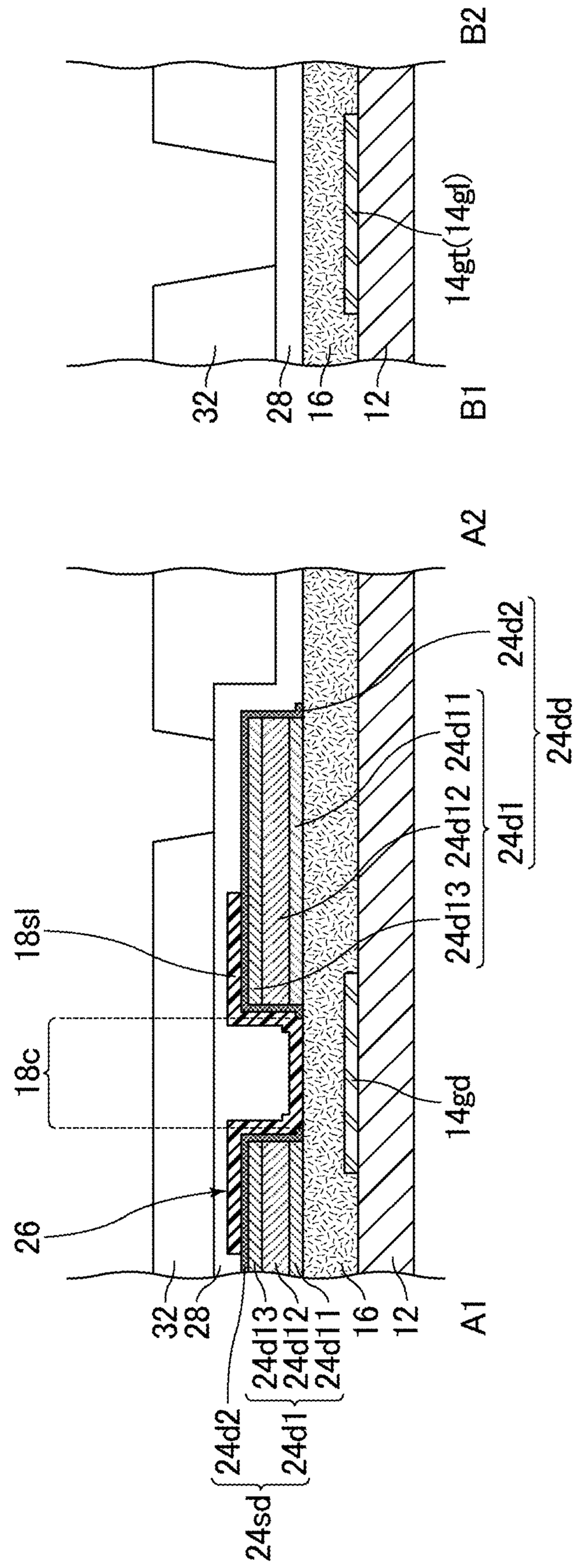

B2
14gt(14gl)
32
28
16
12
B1
A2
24d2
24d11
24dd
24d12
24d1
24d13
18sl
18c
14gd
26
32
28
24d13
24d12
24d11
16
12
A1
24d2
24d1
24sd

FIG.14

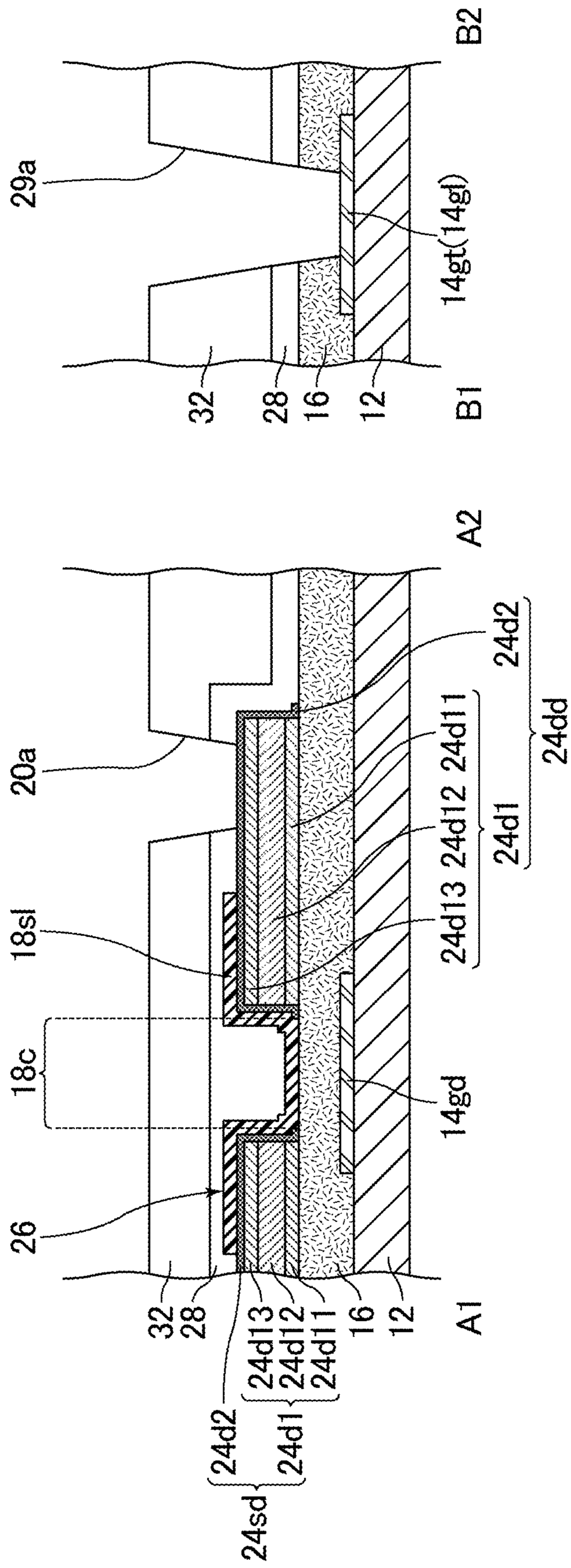

B2
29a
14gt(14gl)
32
28
16
12
B1
A2
24d2
24dd
24d11
24d12
24d1
24d13
20a
18sl
18c
14gd
26
32
28
24d13
24d12
24d11
16
12
A1
24d2
24d1
24sd

FIG.15

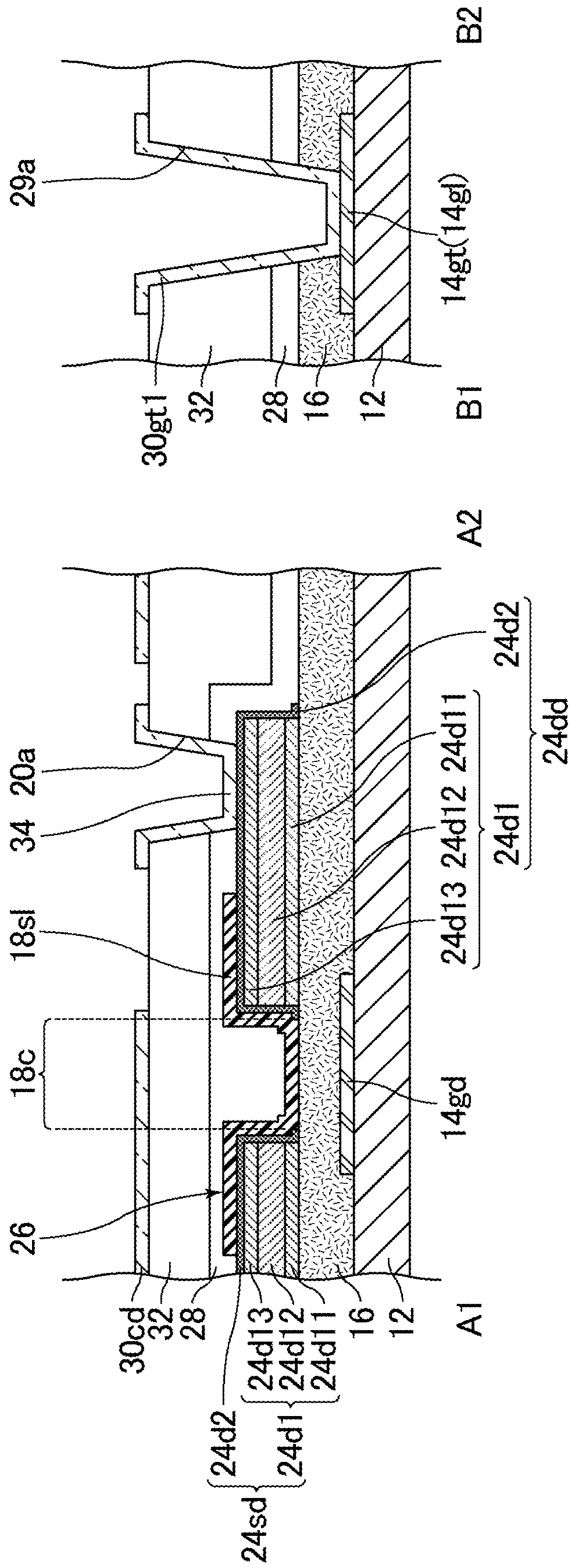
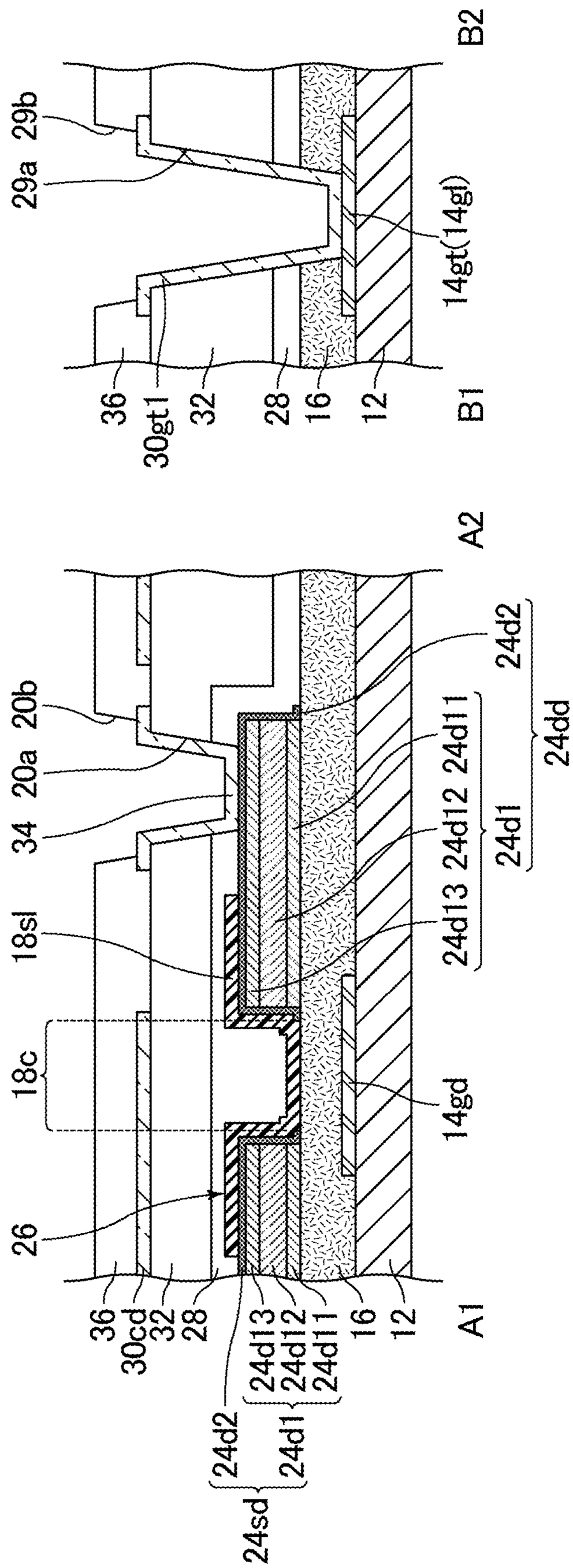

B2
29a
14gt(14gl)
30gt1
32
28
16
12
B1
A2
24d2
24d11
24dd
20a
34
24d12
24d1
18sl
24d13
18c
14gd
26
30cd
32
28
24d13
24d12
24d11
16
12
A1
24d2
24d1
24sd

FIG.16


B2
29b
29a
14gt(14gl)
36
30gt1
32
28
16
12
B1
A2
24d2
24d11
24dd
20b
20a
34
24d12
24d1
18sl
24d13
18c
14gd
26
36
30cd
32
28
24d13
24d12
24d11
16
12
A1
24d2
24d1
24sd

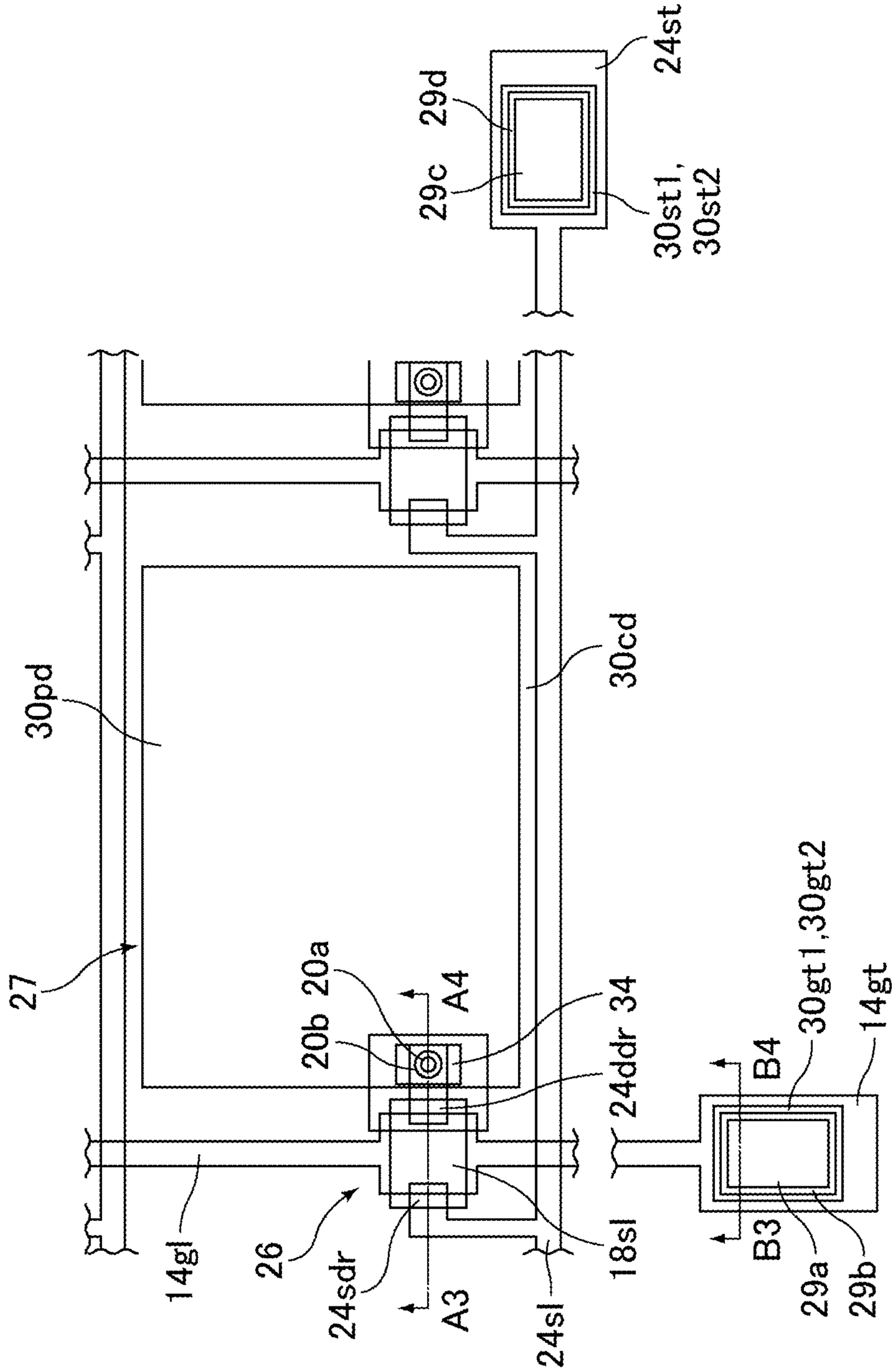

24st
29d
29c
30st1,
30st2
30cd
30pd
27
20a
20b
A4
34
24ddr
30gt1,30gt2
14gt
B4
B3
29a
29b
14gl
26
24sdr
A3
24sl
18sl

FIG.17

FIG.18

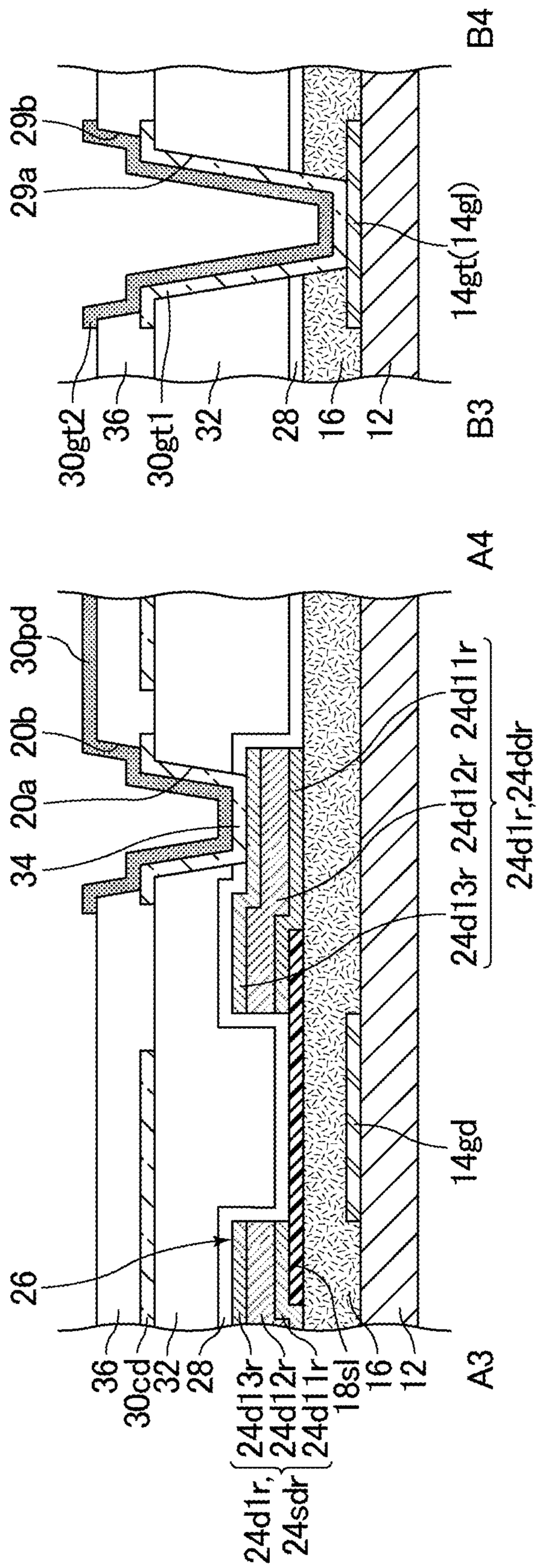

B4
29b
29a
14gt(14gl)
30gt2
36
30gt1
32
28
16
12
B3
A4
30pd
20b
20a
34
24d11r
24d12r
24d13r
24d1r,24ddr
14gd
26
36
30cd
32
28
24d13r
24d12r
24d11r
24d1r,
24sdr
18sl
16
12
A3

FIG.19

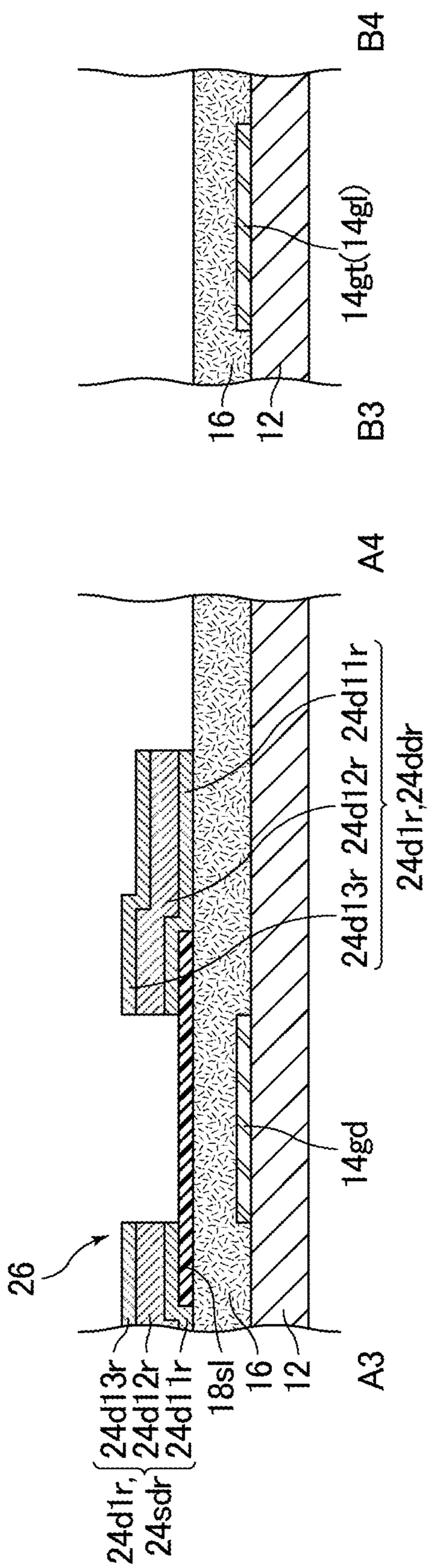

B4
14gt(14gl)
16
12
B3
A4
24d11r
24d12r
24d13r
24d1r,24ddr
14gd
26
24d1r,
24sdr
24d13r
24d12r
24d11r
18sl
16
12
A3

FIG.20

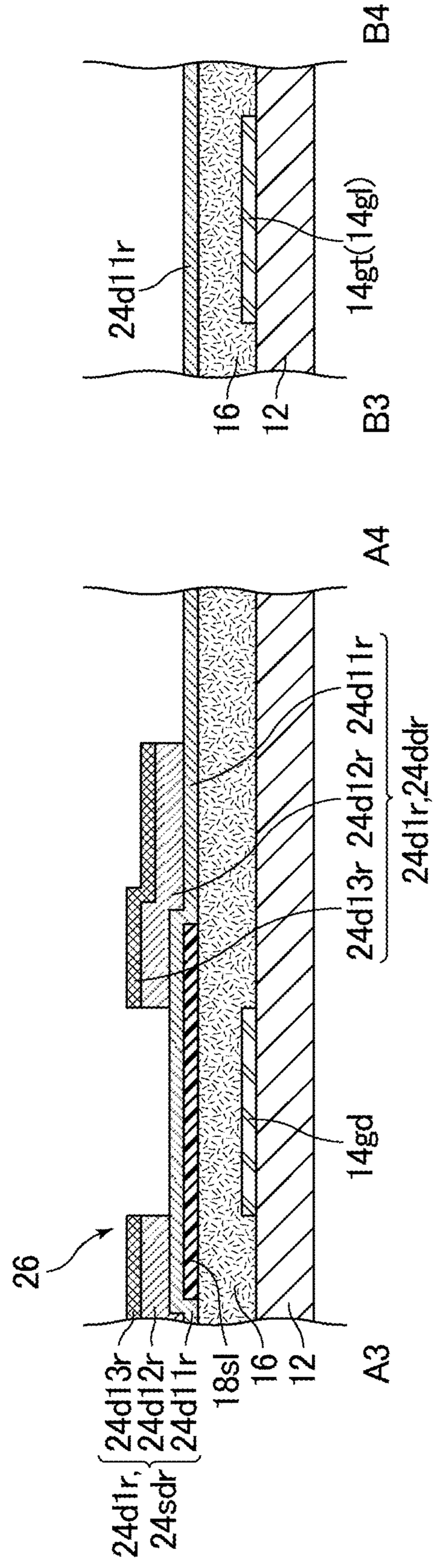
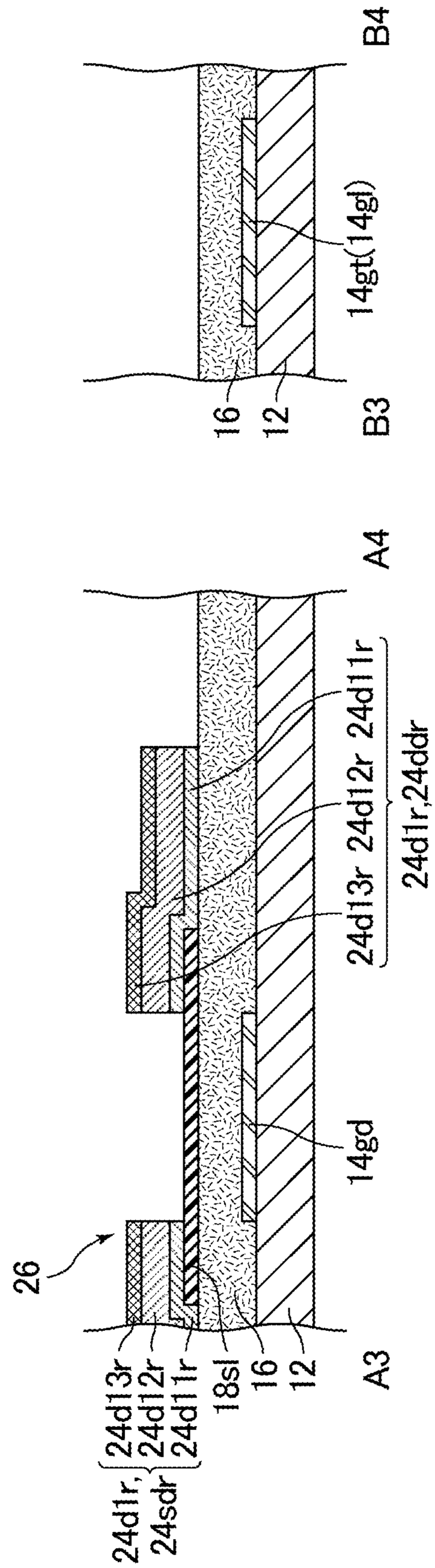

B4
24d11r
14gt(14gl)
16
12
B3
A4
24d11r
24d12r
24d13r
24d1r,24ddr
14gd
26
24d1r,
24sdr
24d13r
24d12r
24d11r
18sl
16
12
A3

FIG.21


B4
14gt(14gl)
16
12
B3
A4
24d11r
24d12r
24d13r
24d1r,24ddr
14gd
26
24d13r
24d12r
24d11r
24d1r,
24sdr
18sl
16
12
A3

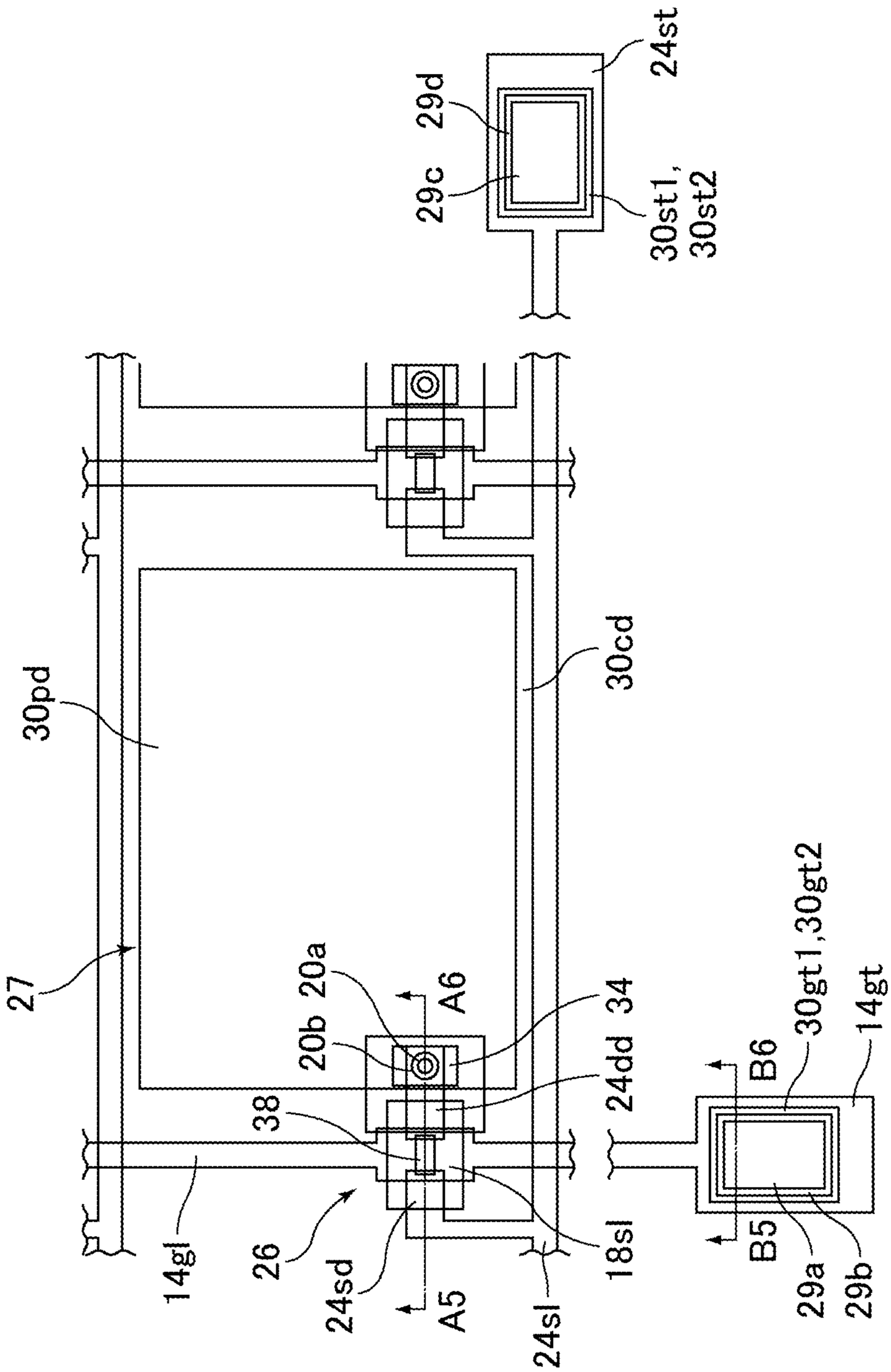

24st
29d
29c
30st1,
30st2
30pd
30cd
27
20a
20b
A6
34
24dd
38
30gt1,30gt2
14gt
B6
14gl
26
24sd
A5
24sl
18sl
B5
29a
29b

FIG.22

FIG.23

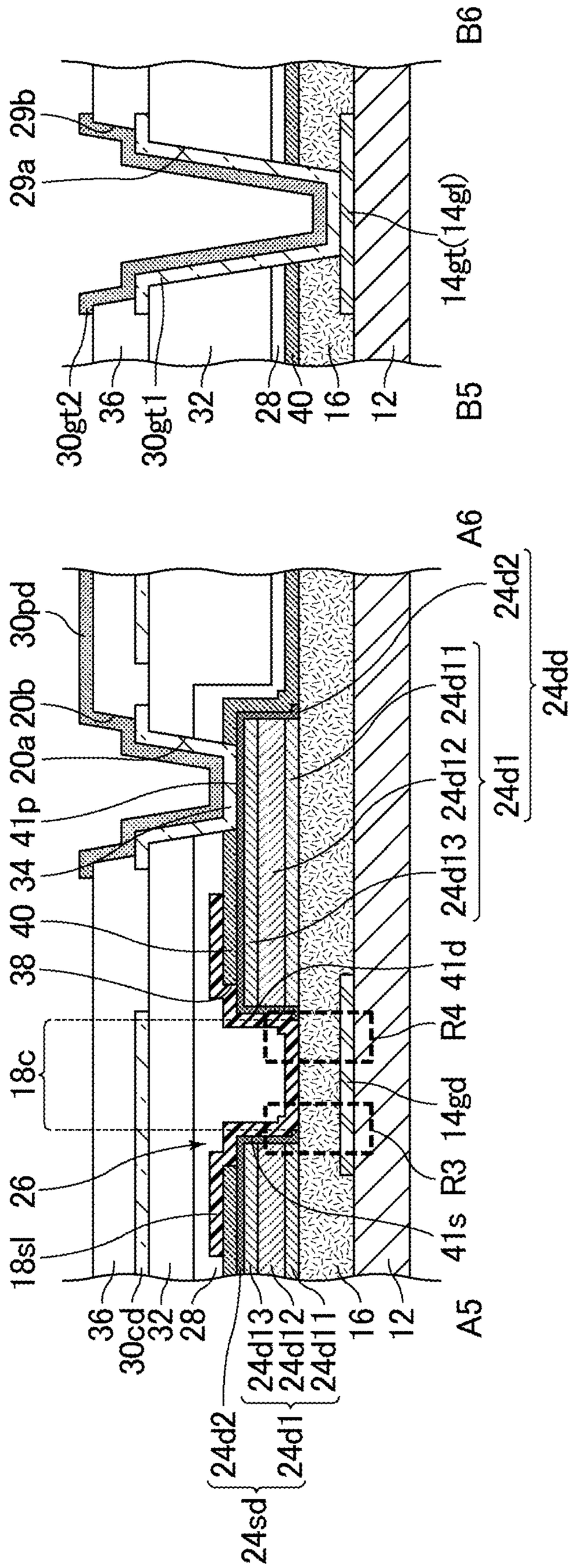

B6
29b
29a
14gt(14gl)
30gt2
36
30gt1
32
28
40
16
12
B5
A6
30pd
24d2
20b
24d11
24dd
20a
24d12
41p
24d1
34
24d13
40
38
41d
R4
18c
14gd
26
R3
18sl
41s
36
30cd
32
28
24d13
24d12
24d11
16
12
A5
24d2
24d1
24sd

FIG.24A

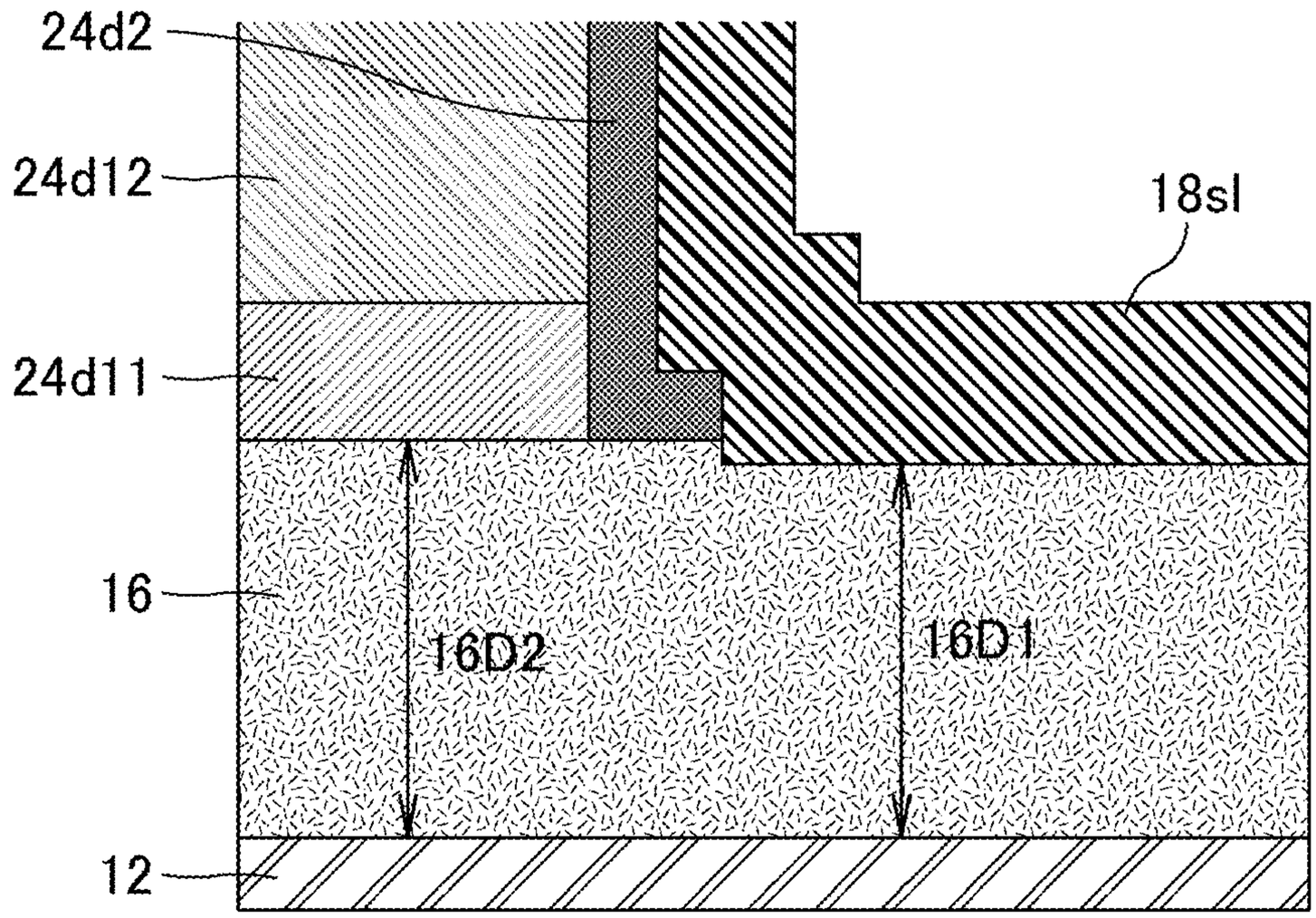


FIG.24B

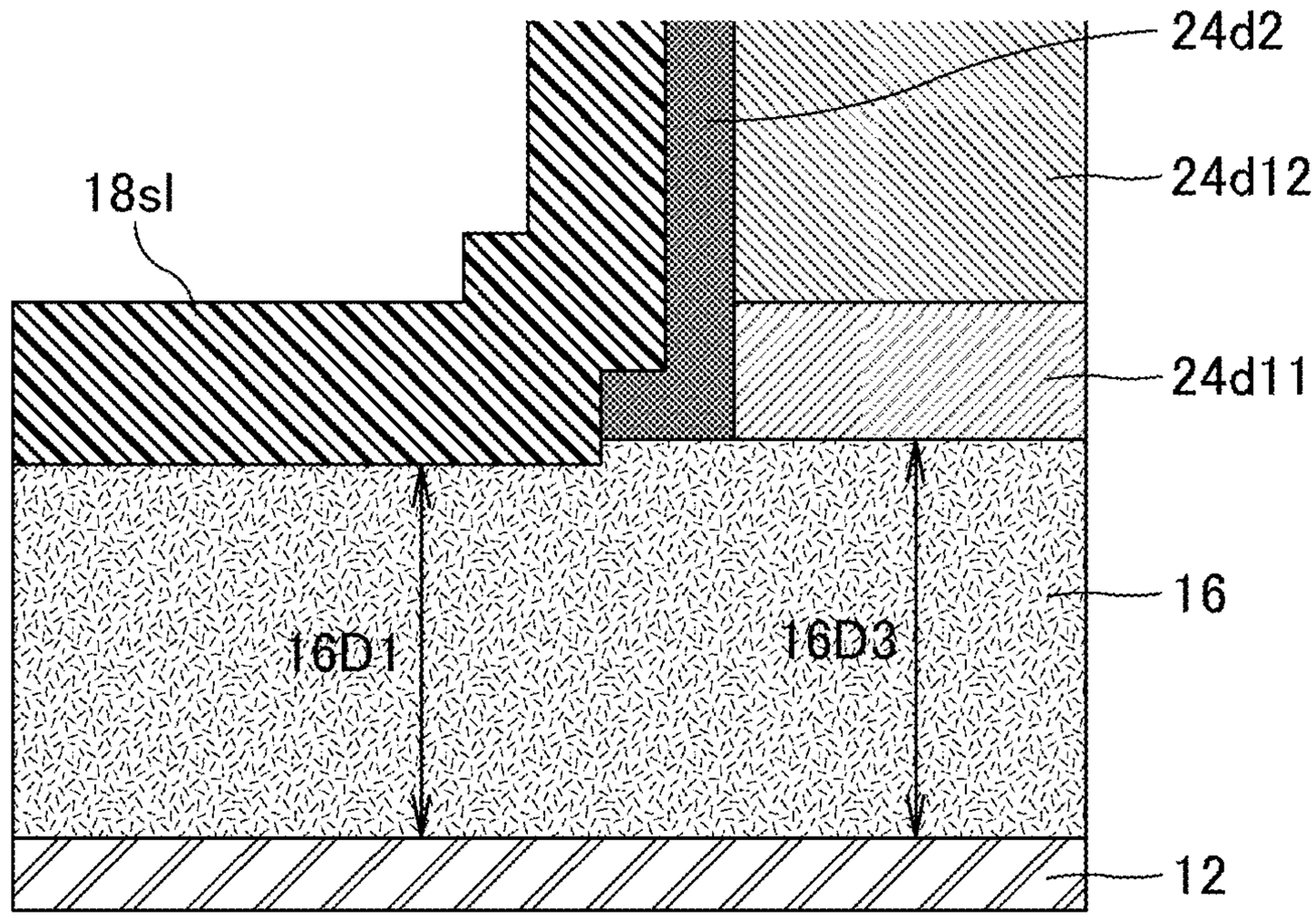


FIG.25

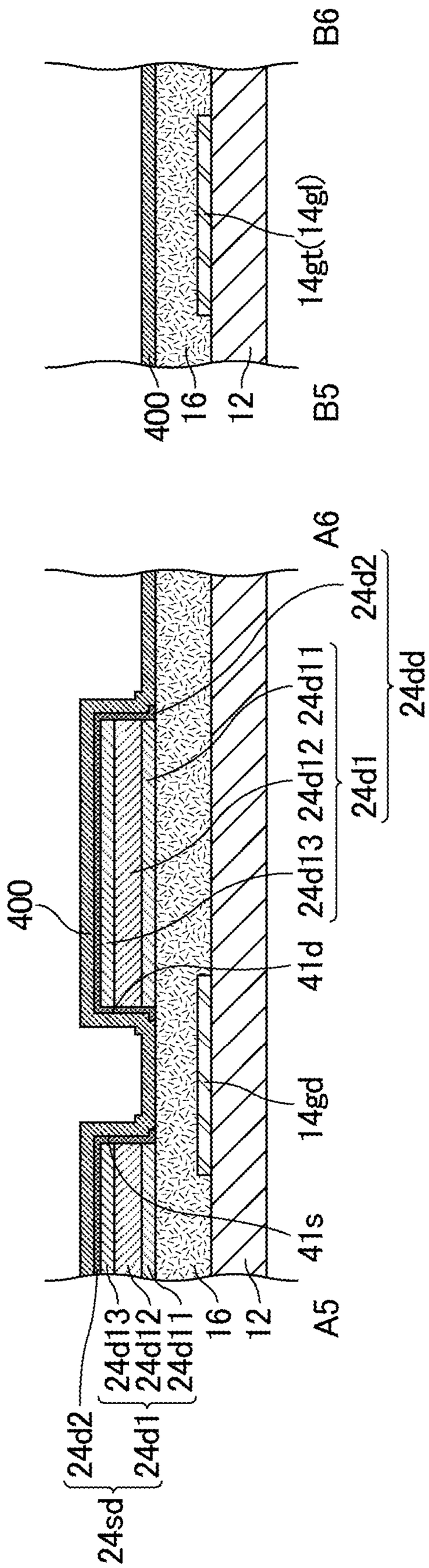

B6
14gt(14gl)
400
16
12
B5
A6
24d2
24d11
24dd
24d12
24d1
24d13
400
41d
14gd
41s
24d2
24d13
24d12
24d11
24d1
24sd
16
12
A5

FIG.26

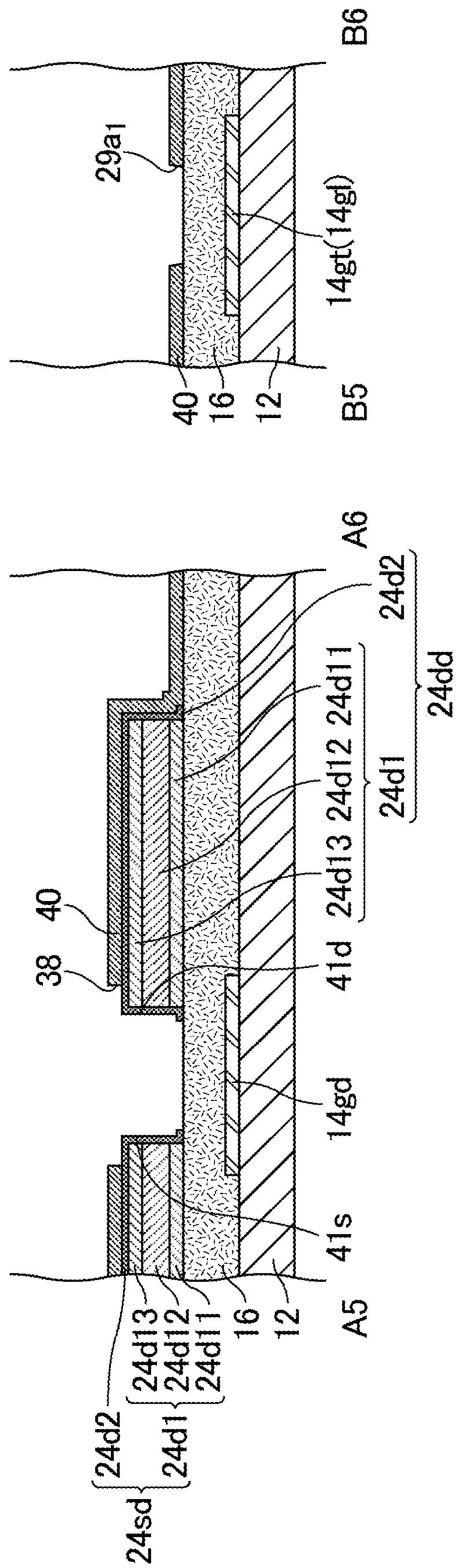

B6
29a1
14gt(14gl)
40
16
12
B5
A6
24d2
24d11
24dd
24d12
24d1
24d13
40
38
41d
14gd
41s
24d2
24d13
24d12
24d11
24d1
24sd
16
12
A5

FIG.27

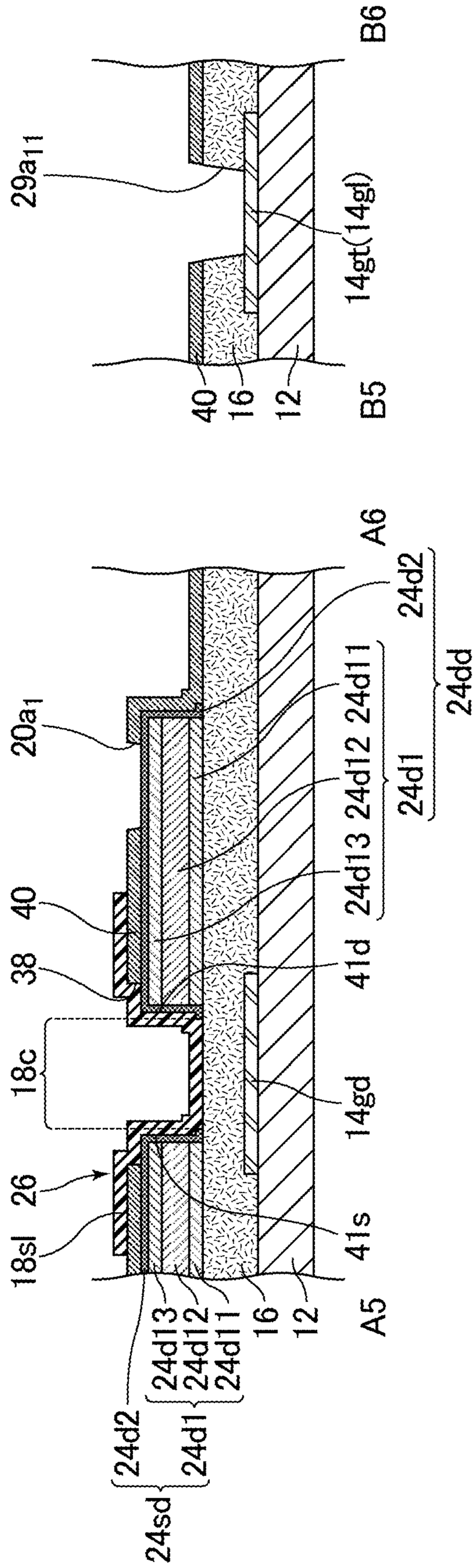
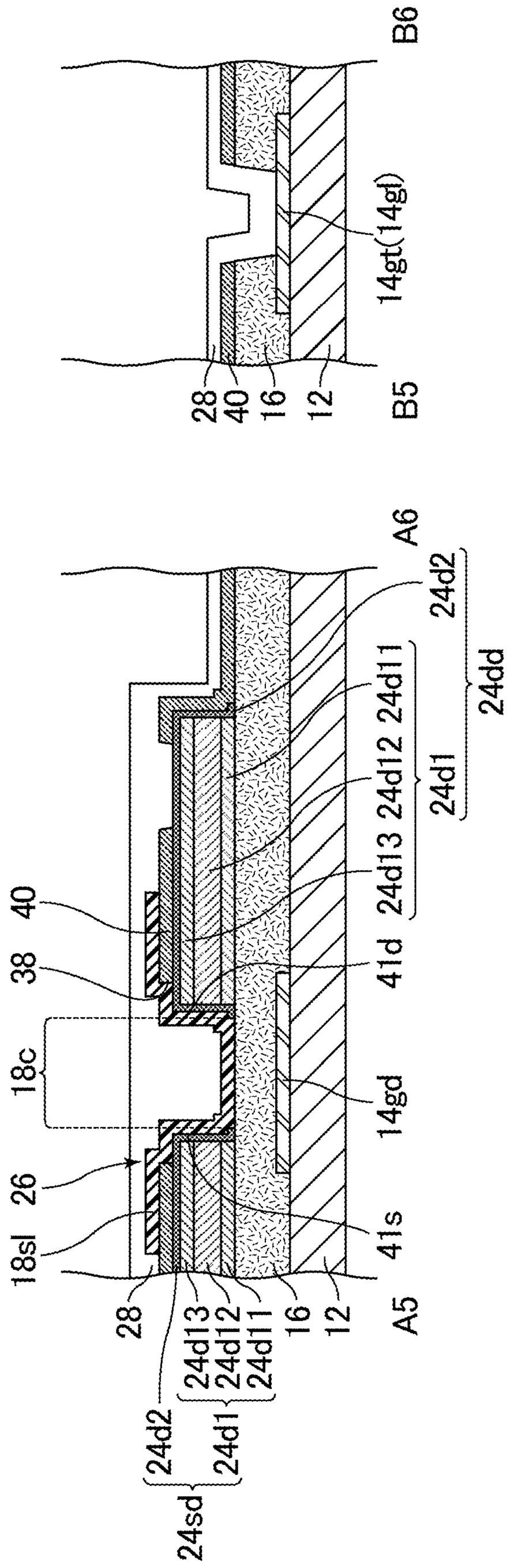

B6
29a11
14gt(14gl)
40
16
12
B5
A6
24d2
24d11
24dd
20a1
24d12
24d1
24d13
40
41d
38
18c
14gd
26
41s
18sl
24d13
24d12
24d11
16
12
A5
24d2
24d1
24sd

FIG.28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B5
A6
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24d11
24dd
24d12
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41d
18c
14gd
26
18sl
41s
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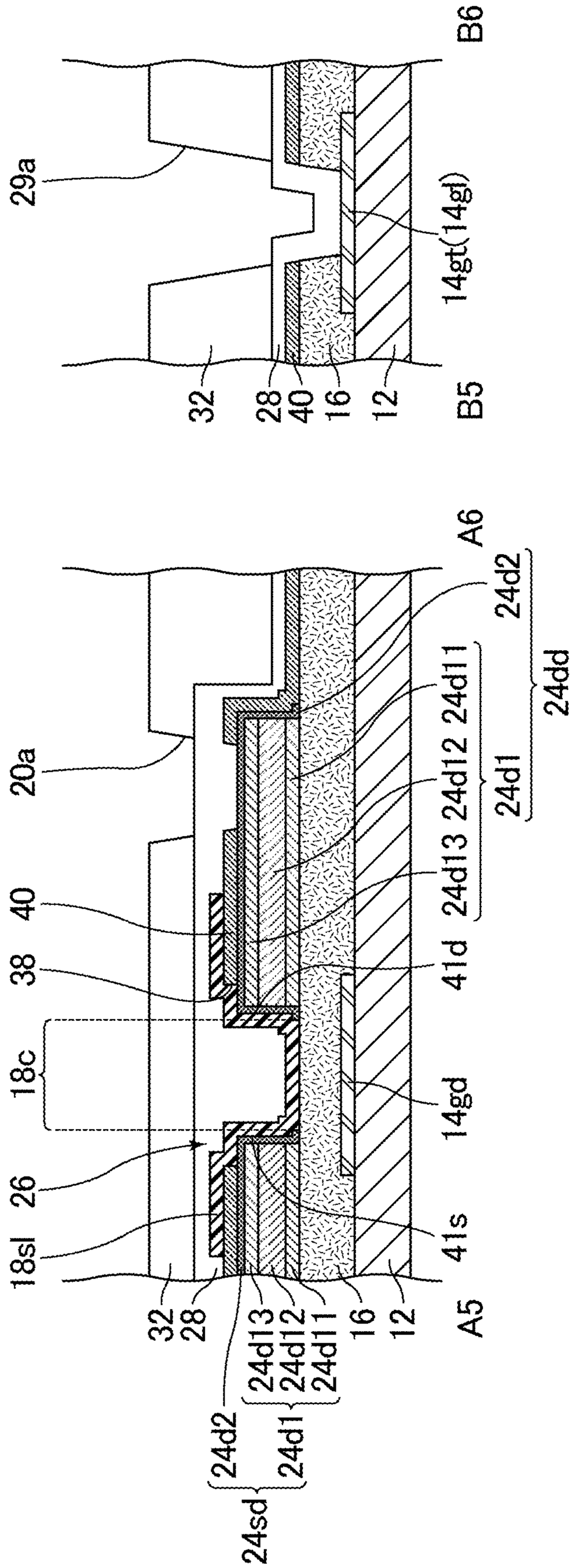
24d12
24d11
16
12
A5
24d2
24d1
24sd

FIG.29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B5
A6
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24dd
20a
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24d13
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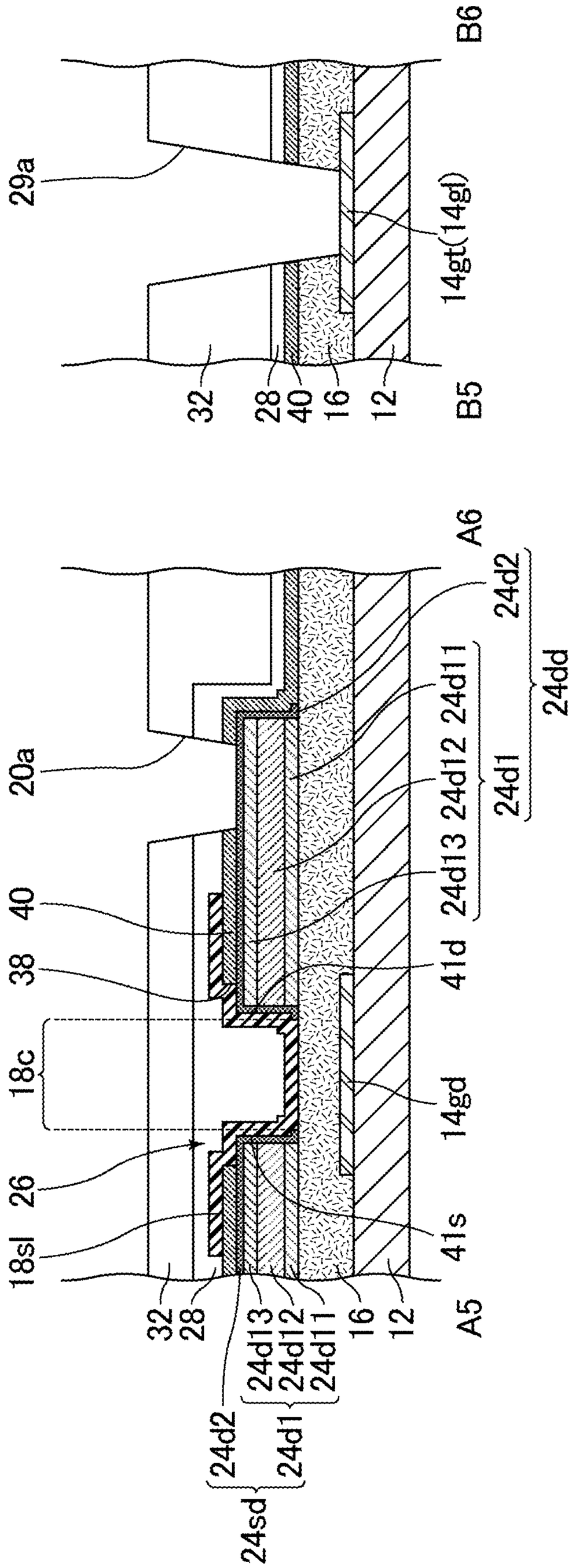
41d
38
18c
14gd
26
18sl
41s
32
28
24d13
24d12
24d11
16
12
A5
24d2
24d1
24sd

FIG.30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B5
A6
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24dd
20a
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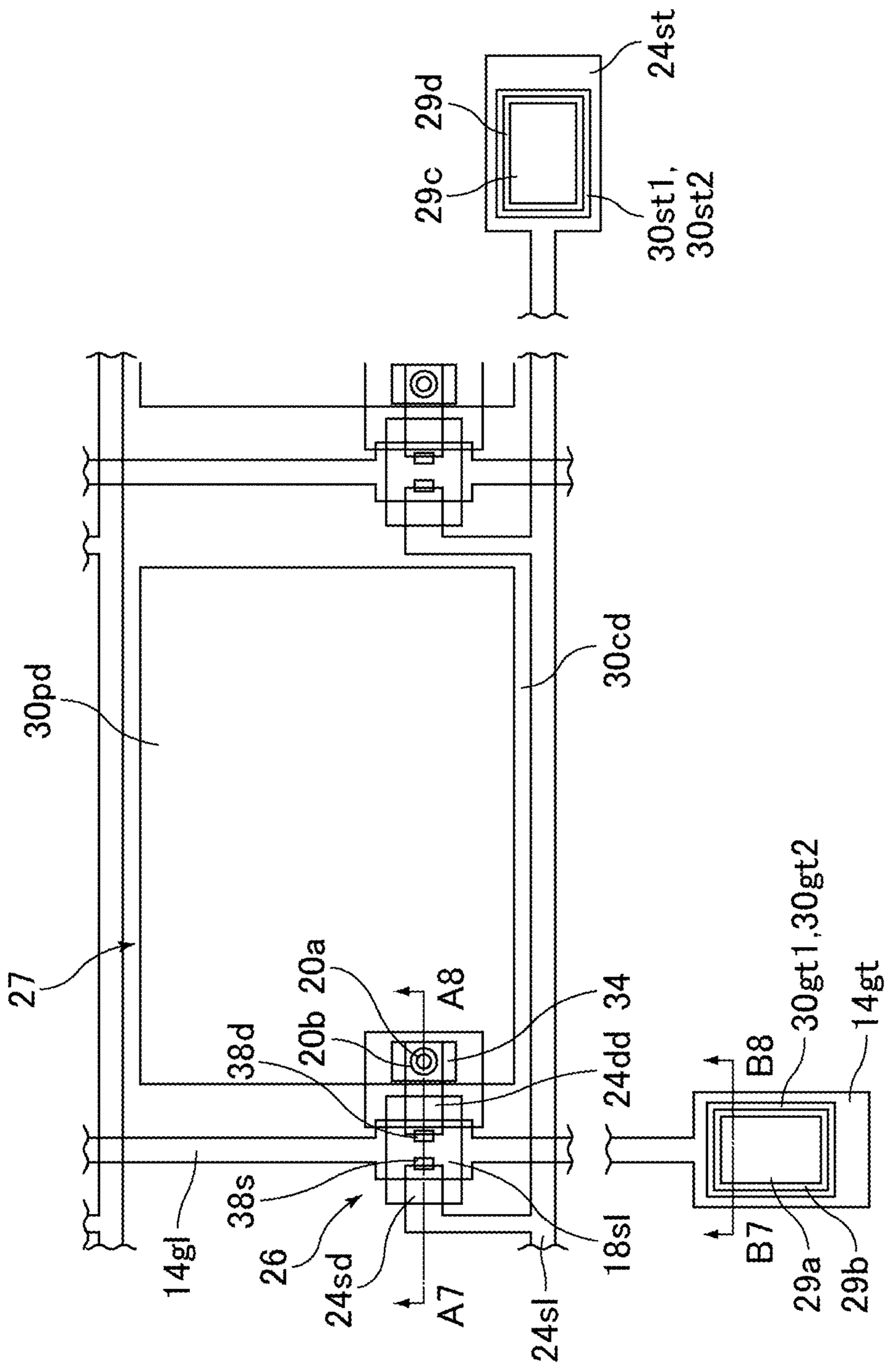
24d13
40
38
41d
18c
14gd
26
18sl
41s
32
28
24d13
24d12
24d11
16
12
A5
24d2
24d1
24sd

FIG.31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30st2
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27
20a
A8
34
38d
20b
24dd
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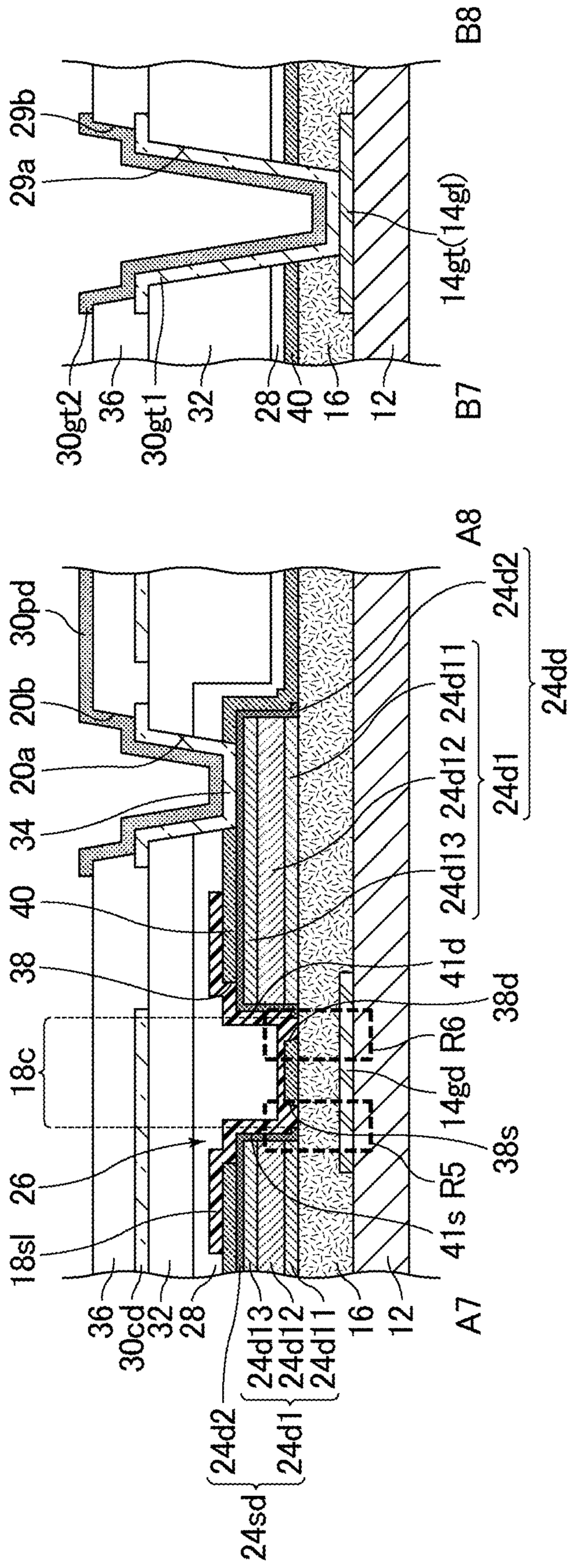
38s
14gl
26
24sd
A7
24sl
18sl
B7
29a
29b

FIG.32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40
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24dd
20a
24d12
24d1
34
24d13
40
41d
38
38d
R6
18c
14gd
38s
26
R5
41s
18sl
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30cd
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28
24d13
24d12
24d11
16
12
A7
24d2
24d1
24sd

FIG.33A

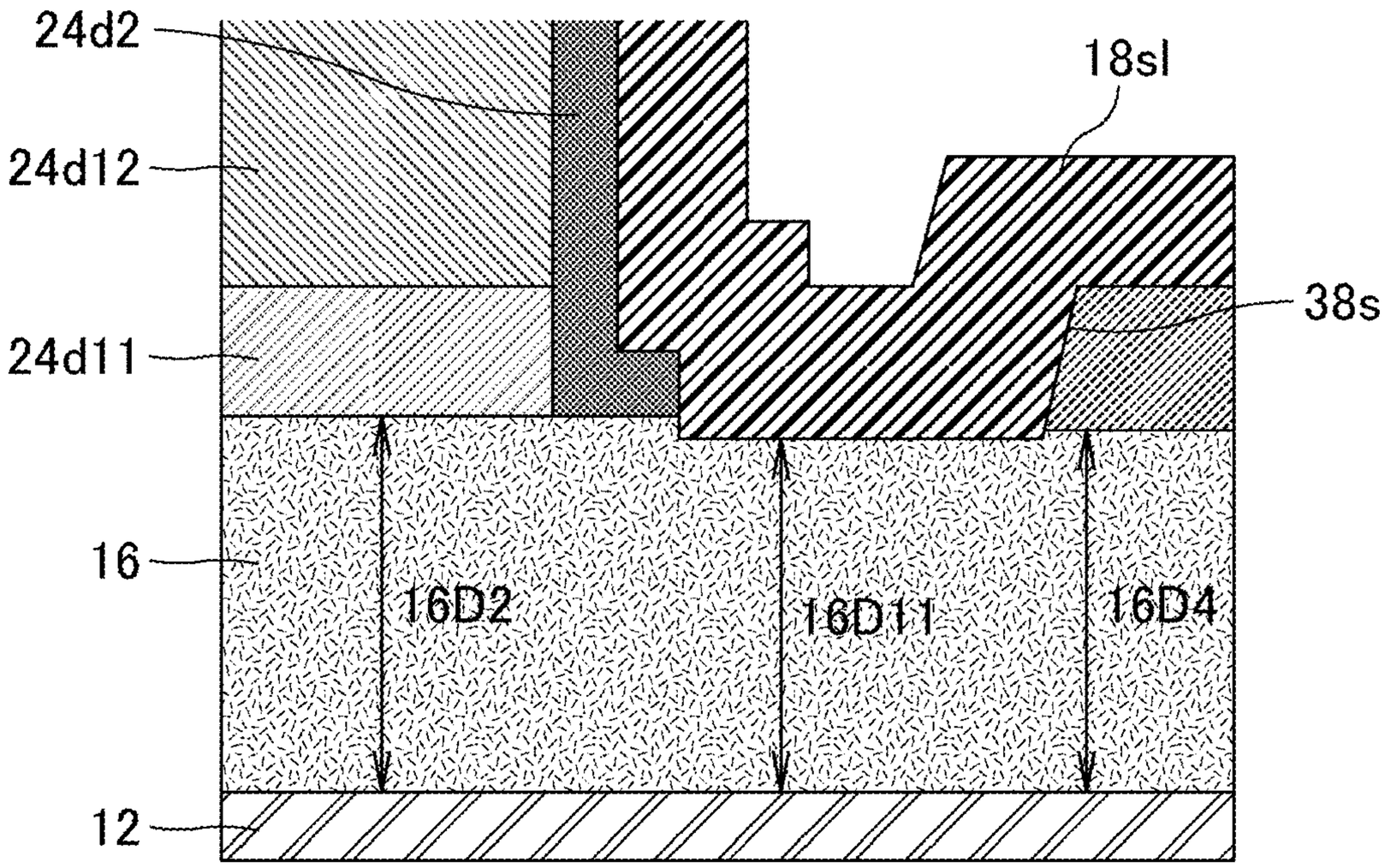


FIG.33B

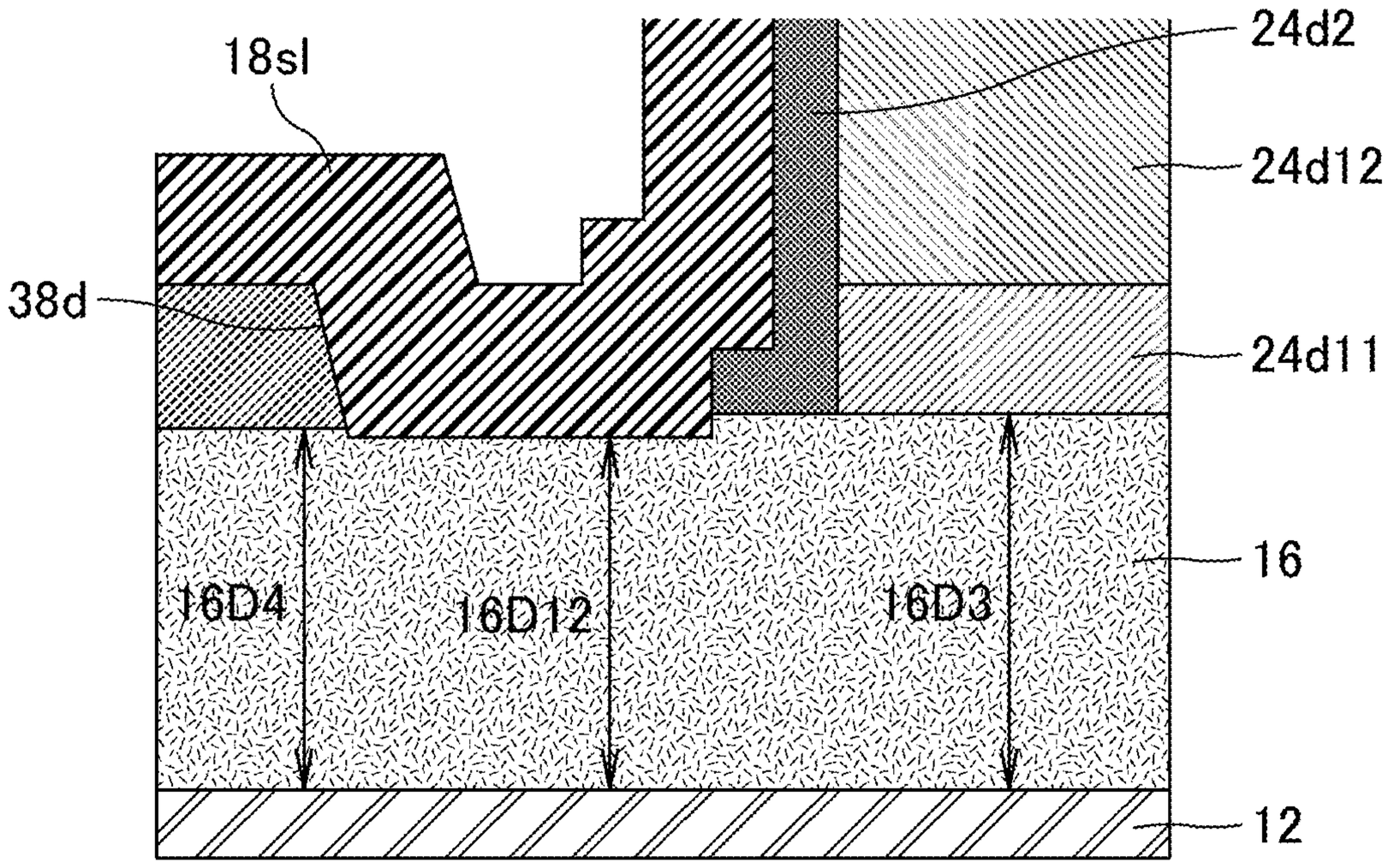
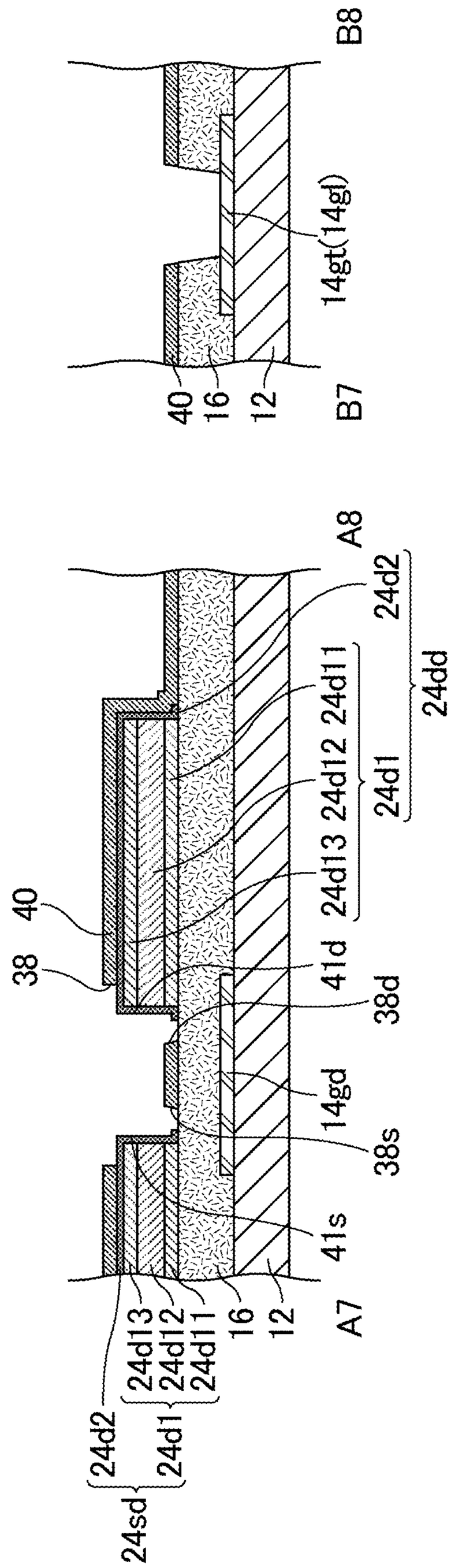


FIG.34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24d11
24dd
24d12
24d1
24d13
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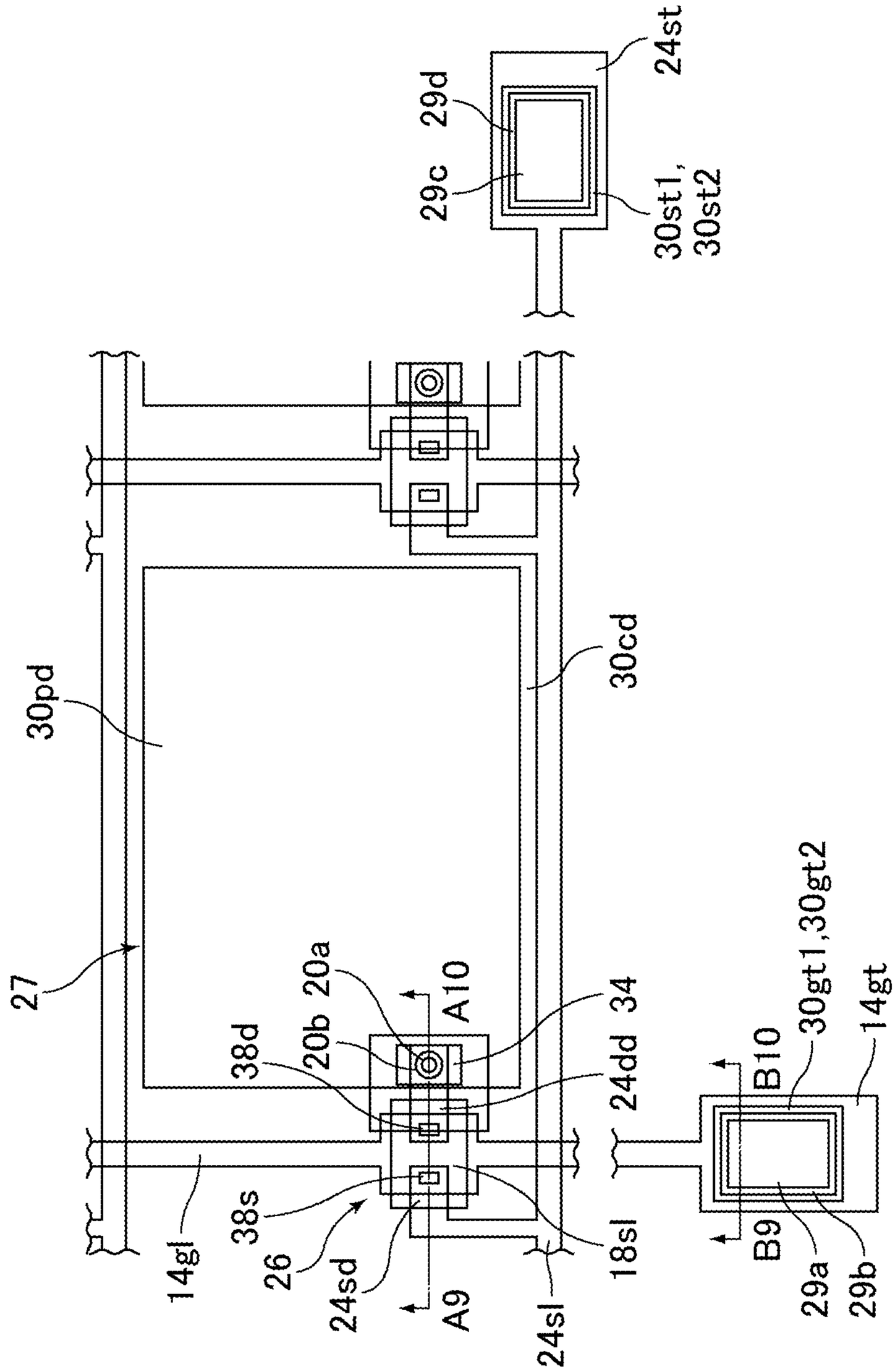
38
41d
38d
14gd
38s
41s
24d13
24d12
24d11
16
12
A7
24d2
24d1
24sd

FIG.35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20a
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38d
20b
34
24dd
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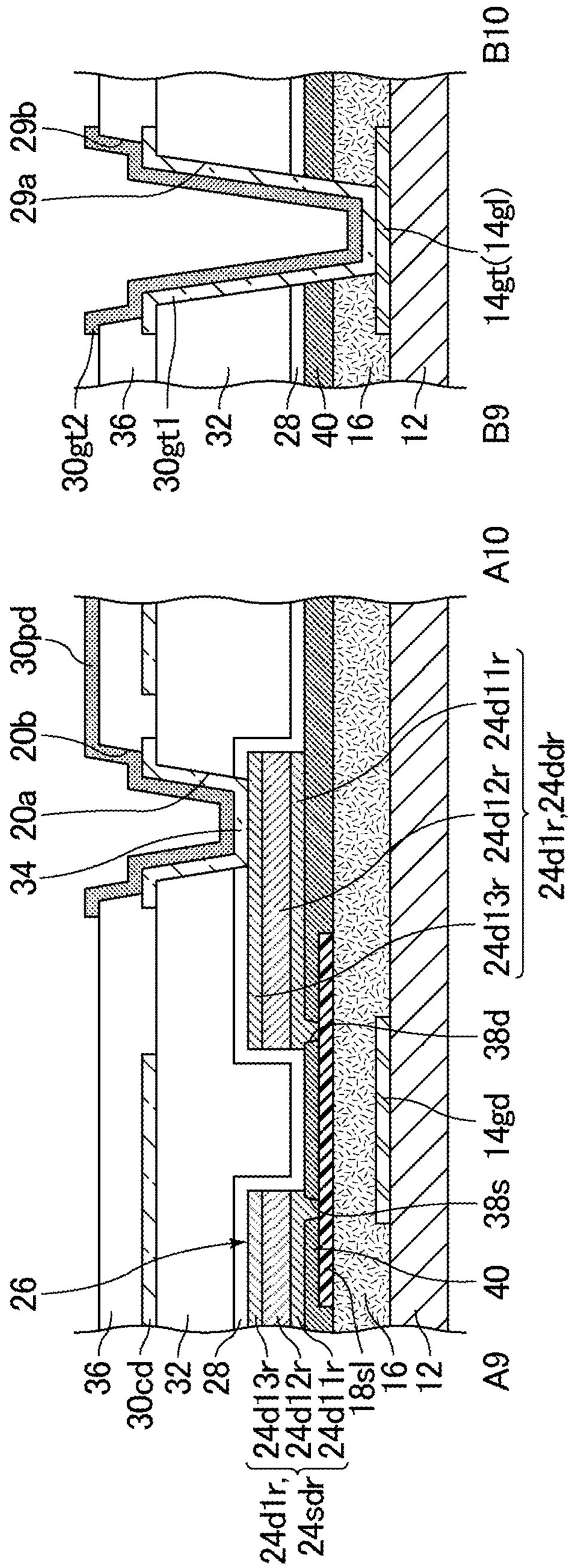
26
24sd
A9
24sl
18sl
14gl
30gt1,30gt2
14gt
B10
B9
29a
29b

FIG.36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29a
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36
30gt1
32
28
40
16
12
B9
A10
30pd
20b
20a
34
24d11r
24d12r
24d13r
24d1r,24ddr
38d
14gd
38s
40
26
36
30cd
32
28
24d13r
24d12r
24d11r
18sl
16
12
A9
24d1r,
24sdr

FIG.37

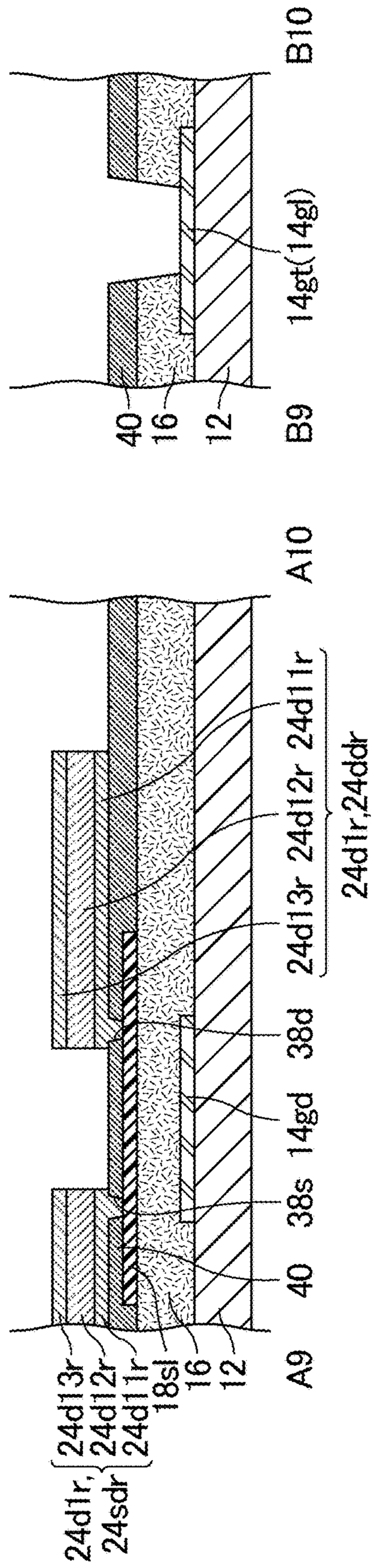
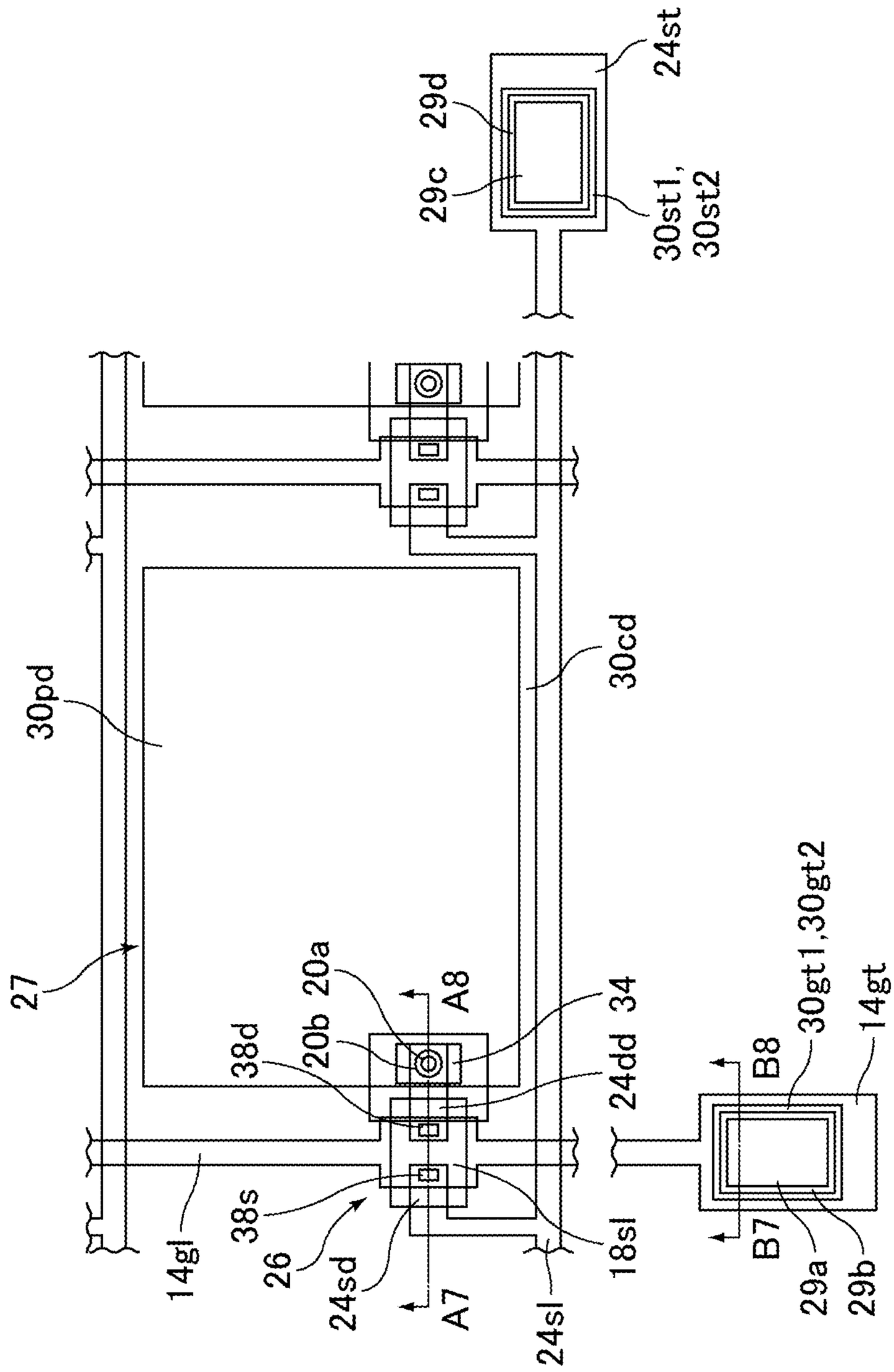

B10
14gt(14gl)
40
16
12
B9
A10
24d11r
24d12r
24d13r
24d1r,24ddr
38d
14gd
38s
40
16
12
18sl
24d11r
24d12r
24d13r
24d1r,
24sdr
A9

FIG.38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30st2
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A8
34
38d
20b
24dd
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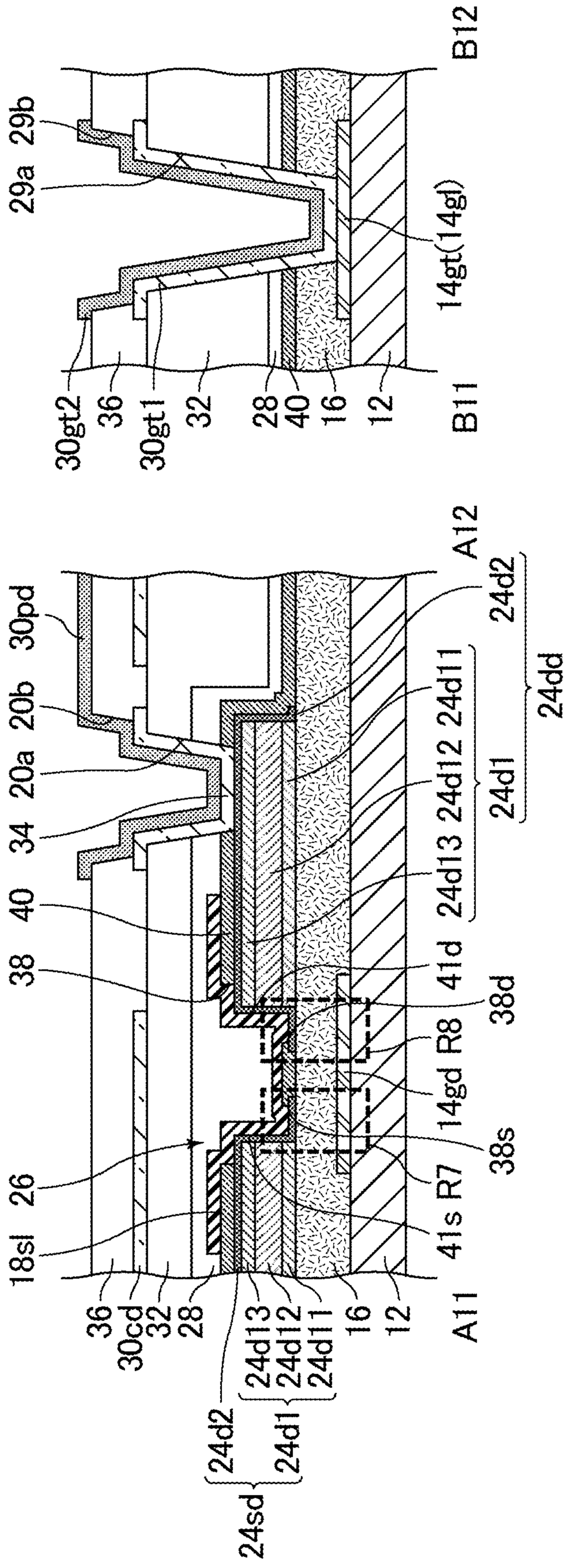
38s
26
24sd
A7
24sl
18sl
B7
29a
29b
14gl

FIG.39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B11
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29b
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B12
30pd
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40
38
26
18sl
36
30cd
32
28
24d2
24d1
24d13
24d12
24d11
16
12
A11
41s R7
38s
14gd R8
38d
41d
24d13
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24d11
24d1
24d2
24dd
A12

FIG.40A

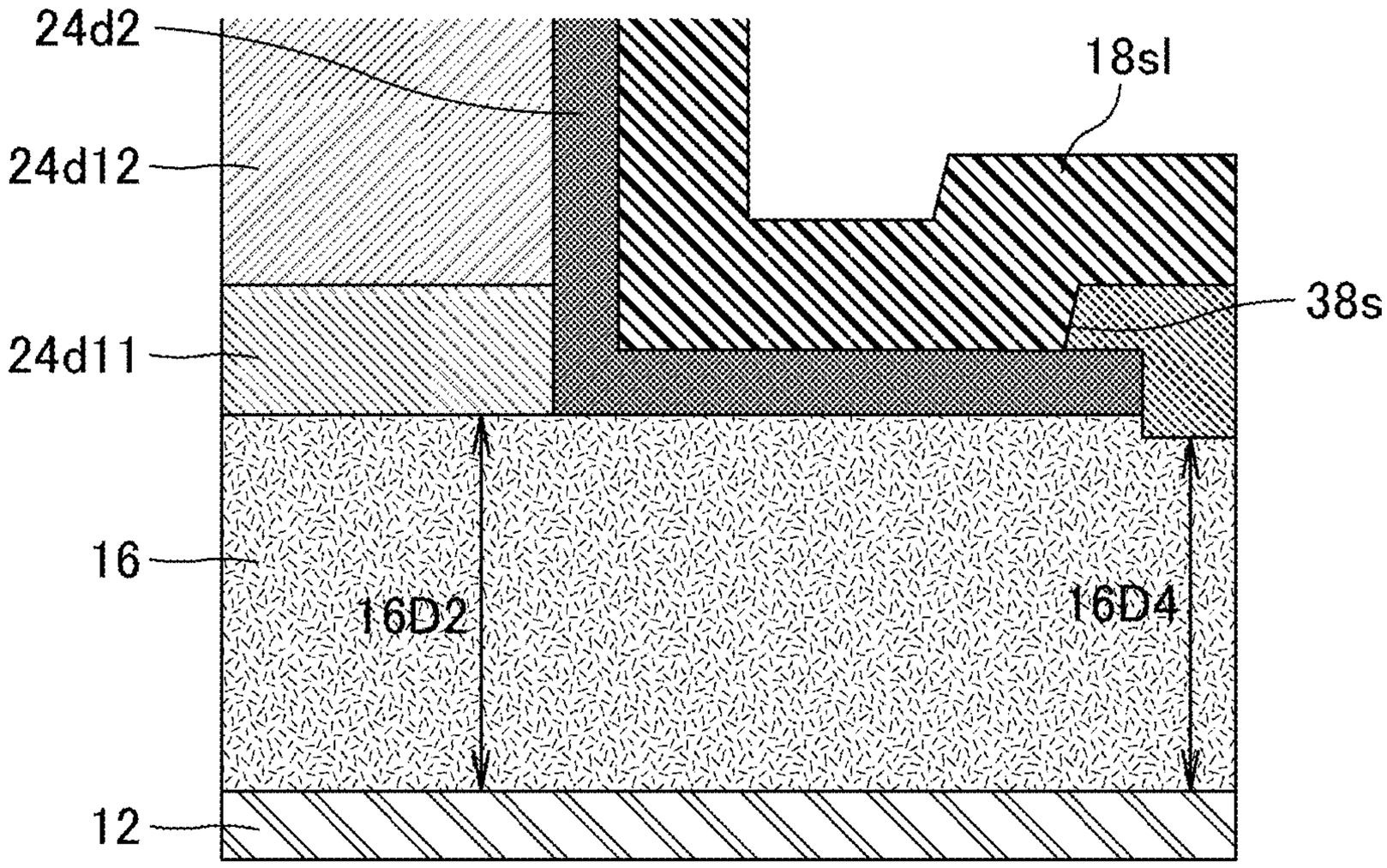


FIG.40B

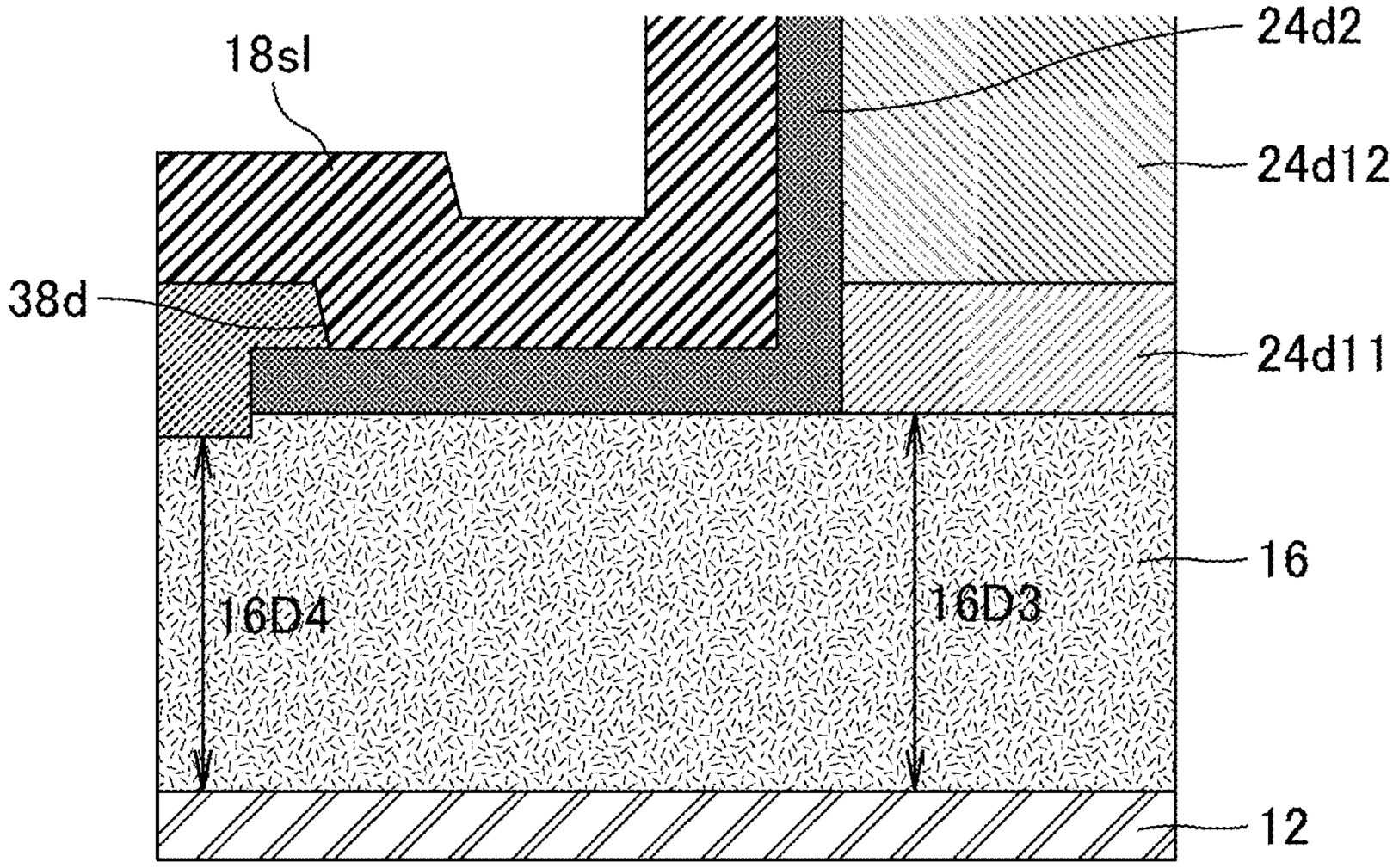
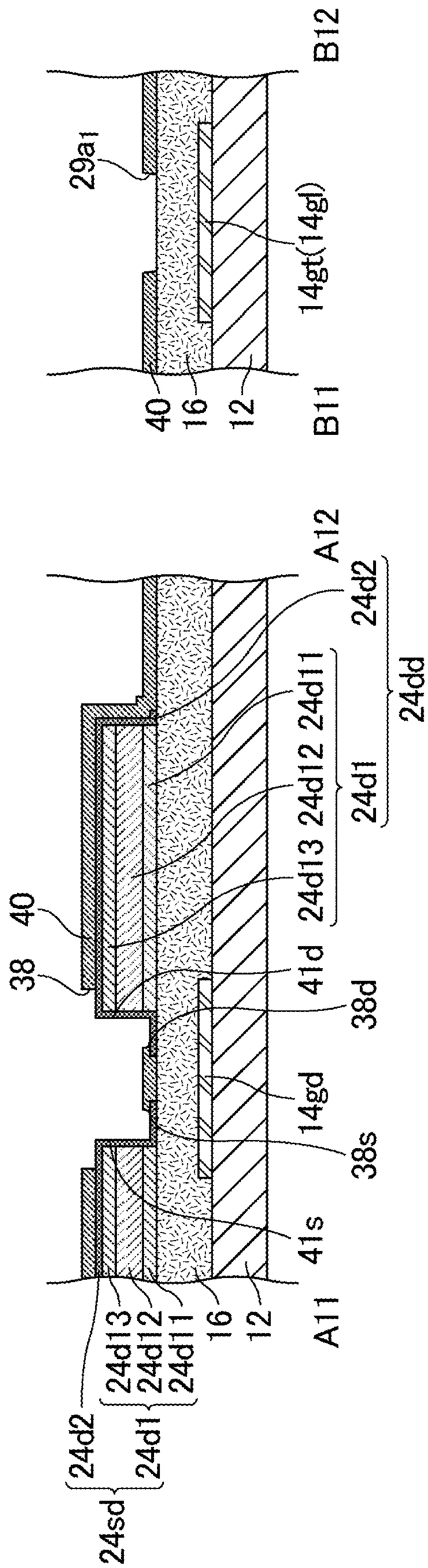


FIG.41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B11
A12
24d2
24d11
24dd
24d12
24d1
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38
41d
38d
14gd
38s
41s
24d13
24d12
24d11
16
12
A11
24d2
24d1
24sd

THIN-FILM TRANSISTOR SUBSTRATE, LIQUID CRYSTAL DISPLAY DEVICE INCLUDING THE SAME, AND METHOD FOR PRODUCING THIN-FILM TRANSISTOR SUBSTRATE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims priority under 35 U.S.C. § 119 to U.S. Provisional Application No. 62/752,390 filed on Oct. 30, 2018, the contents of which are incorporated herein by reference in their entirety.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to thin-film transistor (hereinafter, also referred to as TFT) substrates and liquid crystal display devices including a TFT substrate, and methods for producing a TFT substrate. The present invention specifically relates to a TFT substrate and a liquid crystal display device each including a TFT that includes a semiconductor layer formed from an oxide semiconductor, and a method for producing the TFT substrate.

Description of Related Art

[0003] In the field of TFT substrates constituting liquid crystal display devices, TFTs having good properties such as high carrier mobility, high reliability, and low off-current have been proposed recently. Such a TFT achieves the good properties by employing a semiconductor layer formed from an oxide semiconductor (hereinafter, also referred to as oxide semiconductor layer) as a switching element of a pixel, a minimum unit of an image, differently from conventional TFTs that employ a semiconductor layer formed from amorphous silicon.

[0004] As techniques relating to such an oxide semiconductor layer, for example, JP 2010-141308 A, JP 2014-232880 A, JP 2016-36043 A, and JP 2017-187782 A each disclose an oxide semiconductor layer which includes on one substrate a pixel and a drive circuit for driving the pixel and in which at least part of the drive circuit is formed of a thin-film transistor including an oxide semiconductor sandwiched by top and bottom gate electrodes. JP 2010-74148 A discloses a field effect transistor including: a gate electrode to which a gate voltage is applied; a source electrode and a drain electrode for obtaining a current in response to the gate voltage; an active layer provided adjacent to the source electrode and the drain electrode and formed of an oxide semiconductor including magnesium (Mg) and indium (In) as major components; and a gate insulating layer provided between the gate electrode and the active layer. The flow rate of oxygen gas supplied when forming the active layer is controlled so that the partial oxygen pressure becomes 1.7×10^{-3} Pa. The oxide semiconductor which constitutes the active layer is a $MgIn_2O_4$ oxide semiconductor having a volume resistivity of 10 Ωcm and having nonstoichiometric composition in regard to oxygen.

BRIEF SUMMARY OF THE INVENTION

[0005] A channel-etched TFT structure, which includes a semiconductor layer including an oxide semiconductor (e.g., In—Ga—Zn—O-based oxide semiconductor), is obtained by forming a gate layer, a gate insulating layer (also referred to as gate insulating film) on the gate layer, an oxide semiconductor layer on the gate insulating layer, and a source/drain layer (hereinafter, also referred to as SD layer) provided with source electrodes, drain electrodes, source lines, and drain lines. The SD layer is formed from Al or Cu, i.e., a metal having a low resistance. When the SD layer has a structure in which Al or Cu having a low resistance is sandwiched by Ti, the SD layer is formed by dry etching. In this case, the channel portion of each TFT has troubles due to plasma damage caused by the dry etching. Specifically, the TFT properties are degraded, namely, the threshold value is significantly reduced to the negative side, whereby the TFT may fail to function as a switching element.

[0006] In JP 2010-141308 A, JP 2014-232880 A, JP 2016-36043 A, and JP 2017-187782 A, a surface of the gate insulating layer serving as channels of the TFTs has undergone plasma treatment. When the plasma treatment is performed by asking treatment, the SD layer is oxidized and may possibly cause poor contact. When the plasma treatment is performed by etching the gate insulating layer, the SD layer is also etched and the lengths L of the TFT elements (channel lengths of the TFT elements) varies in the substrate plane to cause variation in carrier mobility and threshold value of the TFTs. When such TFTs are used for an X-ray sensor, for example, the sensitivity of the X-ray sensor is significantly varied. When the plasma treatment is performed before formation of the semiconductor layer, the surface of the gate insulating layer (interface between the gate insulating layer and the semiconductor layer) has a defect due to plasma damage and may fail in providing stable TFT properties (threshold value).

[0007] Even in the bottom-contact/bottom-gate TFT disclosed in FIG. **14** of JP 2010-74148 A, the top layer of the gate insulating layer, which corresponds to the interface between the gate insulating layer and the semiconductor layer, may be contaminated during resist removal in forming an SD layer. In this case, the threshold values of the TFTs are unstable to possibly cause reduced on-state current. In addition, etching the SD layer in the forming of an SD layer may cause a residue of the SD layer or an ionic residue. As a result, among the TFT properties, the off-leakage current increases and the threshold value shifts to the negative side. These troubles may cause the TFTs to fail to function as switching elements, possibly leading to unstable TFT properties.

[0008] The present invention has been made under the current situation in the art and aims to provide a thin-film transistor substrate achieving stable TFT properties, a liquid crystal display device including the thin-film transistor substrate, and a method for producing a thin-film transistor substrate.

[0009] (1) An embodiment of the present invention is a thin-film transistor substrate including a base substrate and a thin-film transistor, the thin-film transistor including: a gate electrode disposed on the base substrate; a gate insulating layer covering the gate electrode; a source electrode and a drain electrode facing each other and disposed above the gate electrode via the gate insulating layer; and an oxide semiconductor layer which faces the gate electrode via at least the gate insulating layer and whose first end and second end respectively overlap the source electrode and the drain electrode and are thereby respectively connected to the source electrode and the drain electrode, the source electrode

and the drain electrode each including a first conductive layer and a second conductive layer covering the first conductive layer, the second conductive layer containing at least one element selected from the group consisting of molybdenum, tantalum, tungsten, and nickel, the gate insulating layer in a region between the source electrode and the drain electrode having a smaller thickness than in a region below the source electrode and in a region below the drain electrode.

[0010] (2) In an embodiment of the present invention, the thin-film transistor substrate includes the structure (1), the thin-film transistor includes no etching stopper layer on the source electrode and on the drain electrode, and the oxide semiconductor layer faces the gate electrode via the gate insulating layer.

[0011] (3) In an embodiment of the present invention, the thin-film transistor substrate includes the structure (1), the thin-film transistor further includes an etching stopper layer on the source electrode and on the drain electrode, the thin-film transistor substrate further includes a protective insulating layer covering the thin-film transistor and a conductive layer disposed on the protective insulating layer and connected to the drain electrode via a first contact hole in the etching stopper layer and in the protective insulating layer, the etching stopper layer covers the source electrode except for a connection portion between the oxide semiconductor layer and the source electrode and covers the drain electrode except for a connection portion between the oxide semiconductor layer and the drain electrode and a connection portion between the conductive layer and the drain electrode, and the connection portion between the oxide semiconductor layer and the source electrode and the connection portion between the oxide semiconductor layer and the drain electrode are located in a region with the gate electrode.

[0012] (4) In an embodiment of the present invention, the thin-film transistor substrate includes the structure (3), the etching stopper layer is not present in a region between the oxide semiconductor layer and the gate insulating layer, and the oxide semiconductor layer faces the gate electrode via the gate insulating layer.

[0013] (5) In an embodiment of the present invention, the thin-film transistor substrate includes the structure (3), the etching stopper layer is present in a region between the oxide semiconductor layer and the gate insulating layer, and the oxide semiconductor layer is connected to the source electrode via a second contact hole in the etching stopper layer and connected to the drain electrode via a third contact hole in the etching stopper layer.

[0014] (6) In an embodiment of the present invention, the thin-film transistor substrate includes the structure (5), the second contact hole overlaps an end of the source electrode and the gate insulating layer in a part adjacent to the end of the source electrode, the third contact hole overlaps an end of the drain electrode and the gate insulating layer in a part adjacent to the end of the drain electrode, and the gate insulating layer in a region between the source electrode and the drain electrode and below the etching stopper layer has a greater thickness than in a region below the second contact hole and in a region below the third contact hole.

[0015] (7) In an embodiment of the present invention, the thin-film transistor substrate includes the structure (5), the second contact hole overlaps an end of the source electrode but does not overlap the gate insulating layer, the third contact hole overlaps an end of the drain electrode but does not overlap the gate insulating layer, and the gate insulating layer in a region between the source electrode and the drain electrode and below the etching stopper layer has a smaller thickness than in a region below the source electrode and in a region below the drain electrode.

[0016] (8) In an embodiment of the present invention, the thin-film transistor substrate includes the structure (1), (2), (3), (4), (5), (6), or (7), the first conductive layer is a laminate including a lower layer, a middle layer, and an upper layer stacked in the stated order from a base substrate side, the middle layer contains aluminum or copper, and the lower layer and the upper layer each contain titanium or molybdenum nitride.

[0017] (9) In an embodiment of the present invention, the thin-film transistor substrate includes the structure (1), (2), (3), (4), (5), (6), (7), or (8), the second conductive layer contains at least one substance selected from the group consisting of molybdenum, molybdenum nitride, a molybdenum alloy, a nitride of the molybdenum alloy, tantalum, tantalum nitride, a tantalum alloy, a nitride of the tantalum alloy, tungsten, tungsten nitride, a tungsten alloy, a nitride of the tungsten alloy, nickel, nickel nitride, a nickel alloy, and a nitride of the nickel alloy.

[0018] (10) In an embodiment of the present invention, the thin-film transistor substrate includes the structure (1), (2), (3), (4), (5), (6), (7), (8), or (9), the oxide semiconductor layer includes an indium gallium zinc oxide-based oxide semiconductor.

[0019] (11) Another embodiment of the present invention is a liquid crystal display device including: the thin-film transistor substrate having the structure (1), (2), (3), (4), (5), (6), (7), (8), (9), or (10); a counter substrate facing the thin-film transistor substrate; and a liquid crystal layer disposed between the thin-film transistor substrate and the counter substrate.

[0020] (12) Another embodiment of the present invention is a method for producing a thin-film transistor substrate, including in the following order: first patterning including forming a gate electrode conductive film on a base substrate and patterning the gate electrode conductive film using a first photomask to form a gate electrode; formation of a gate insulating layer including forming a gate insulating layer so as to cover the gate electrode; second patterning including forming a first conductive film so as to cover the gate insulating layer and patterning the first conductive film using a second photomask; third patterning including forming a second conductive film containing at least one element selected from the group consisting of molybdenum, tantalum, tungsten, and nickel and patterning the second conductive film using a third photomask to form a source electrode and a drain electrode; hydrofluoric acid treatment including treating a gate insulating layer side surface of the base substrate with hydrofluoric acid; and fourth patterning including forming an oxide semiconductor film so as to cover the source electrode and the drain electrode and patterning the oxide semiconductor film using a fourth photomask to form an oxide semiconductor layer.

[0021] (13) In an embodiment of the present invention, the production method includes the structure (12), and, between the hydrofluoric acid treatment and the fourth patterning, fifth patterning including forming an insulating film so as to cover the source electrode and the drain electrode and patterning the insulating film using a fifth photomask to form an etching stopper layer.

[0022] (14) In an embodiment of the present invention, the production method includes the structure (13), and, between the fifth patterning and the fourth patterning, second hydrofluoric acid treatment including treating the gate insulating layer side surface of the base substrate with hydrofluoric acid.

[0023] (15) In an embodiment of the present invention, the production method includes the structure (12), (13), or (14), and the second conductive film is a conductive film containing at least one substance selected from the group consisting of molybdenum, molybdenum nitride, a molybdenum alloy, a nitride of the molybdenum alloy, tantalum, tantalum nitride, a tantalum alloy, a nitride of the tantalum alloy, tungsten, tungsten nitride, a tungsten alloy, a nitride of the tungsten alloy, nickel, nickel nitride, a nickel alloy, and a nitride of the nickel alloy.

[0024] (16) In an embodiment of the present invention, the production method includes the structure (12), (13), (14), or (15), and the oxide semiconductor film is an indium gallium zinc oxide-based oxide semiconductor.

[0025] The present invention provides a thin-film transistor substrate achieving stable TFT properties, a liquid crystal display device including the thin-film transistor substrate, and a method for producing a thin-film transistor substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] FIG. **1** is a schematic plan view of a liquid crystal display device of Embodiment 1.

[0027] FIG. **2** is a schematic cross-sectional view taken along the line IIA-IIB in FIG. **1**.

[0028] FIG. **3** is a schematic plan view showing the structures of one pixel and ends of lines on a TFT substrate of Embodiment 1.

[0029] FIG. **4** includes schematic cross-sectional views taken along the line A**1**-A**2** and the line B**1**-B**2** in FIG. **3**.

[0030] FIG. **5**A is a schematic cross-sectional view of a region R**1** surrounded by a broken line in FIG. **4**.

[0031] FIG. **5**B is a schematic cross-sectional view of a region R**2** surrounded by a broken line in FIG. **4**.

[0032] FIG. **6** includes schematic cross-sectional views of the regions shown in FIG. **4**, each showing a state where a gate electrode is formed in first patterning in production of the TFT substrate of Embodiment 1.

[0033] FIG. **7** includes schematic cross-sectional views of the regions shown in FIG. **4**, each showing a state where a gate insulating layer is formed in formation of a gate insulating layer in production of the TFT substrate of Embodiment 1.

[0034] FIG. **8** includes schematic cross-sectional views of the regions shown in FIG. **4**, each showing a state where a first conductive film is patterned in second patterning in production of the TFT substrate of Embodiment 1.

[0035] FIG. **9** includes schematic cross-sectional views of the regions shown in FIG. **4**, each showing a state where a second conductive film is formed in third patterning in production of the TFT substrate of Embodiment 1.

[0036] FIG. **10** includes schematic cross-sectional views of the regions shown in FIG. **4**, each showing a state where the second conductive film is patterned in the third patterning in production of the TFT substrate of Embodiment 1.

[0037] FIG. **11** includes schematic cross-sectional views of the regions shown in FIG. **4**, each showing a state where an oxide semiconductor layer is formed in fourth patterning in production of the TFT substrate of Embodiment 1.

[0038] FIG. **12** includes schematic cross-sectional views of the regions shown in FIG. **4**, each showing a state where a protective insulating layer formed from silicon oxide is formed in fifth patterning in production of the TFT substrate of Embodiment 1.

[0039] FIG. **13** includes schematic cross-sectional views of the regions shown in FIG. **4**, each showing a state where a protective insulating layer formed from transparent insulating resin is formed in the fifth patterning in production of the TFT substrate of Embodiment 1.

[0040] FIG. **14** includes schematic cross-sectional views of the regions shown in FIG. **4**, each showing a state where a contact hole is formed in the gate insulating layer and in the protective insulating layer formed from silicon oxide in the fifth patterning in production of the TFT substrate of Embodiment 1.

[0041] FIG. **15** includes schematic cross-sectional views of the regions shown in FIG. **4**, each showing a state where a common electrode is formed in sixth patterning in production of the TFT substrate of Embodiment 1.

[0042] FIG. **16** includes schematic cross-sectional views of the regions shown in FIG. **4**, each showing a state where a protective insulating layer formed from a silicon oxide film or a silicon nitride film is formed in seventh patterning in production of the TFT substrate of Embodiment 1.

[0043] FIG. **17** is a schematic plan view showing the structures of one pixel and ends of lines on a TFT substrate of Comparative Embodiment 1.

[0044] FIG. **18** includes schematic cross-sectional views taken along the line A**3**-A**4** and the line B**3**-B**4** in FIG. **17**.

[0045] FIG. **19** includes schematic cross-sectional views of the regions shown in FIG. **18**, each showing a production process of a TFT substrate of Specific Example 1 of Comparative Embodiment 1.

[0046] FIG. **20** includes schematic cross-sectional views of the regions shown in FIG. **18**, each showing a production process of a TFT substrate of Specific Example 2 of Comparative Embodiment 1.

[0047] FIG. **21** includes schematic cross-sectional views of the regions shown in FIG. **18**, each showing a production process of the TFT substrate of Specific Example 2 of Comparative Embodiment 1.

[0048] FIG. **22** is a schematic plan view showing the structures of one pixel and ends of lines on a TFT substrate of Embodiment 2.

[0049] FIG. **23** includes schematic cross-sectional views taken along the line A**5**-A**6** and the line B**5**-B**6** in FIG. **22**.

[0050] FIG. **24**A is a schematic cross-sectional view of a region R**3** surrounded by a broken line in FIG. **23**.

[0051] FIG. **24**B is a schematic cross-sectional view of a region R**4** surrounded by a broken line in FIG. **23**.

[0052] FIG. **25** includes schematic cross-sectional views of the regions shown in FIG. **23**, each showing a state where an insulating film is formed in fourth patterning in production of the TFT substrate of Embodiment 2.

[0053] FIG. **26** includes schematic cross-sectional views of the regions shown in FIG. **23**, each showing a state where an insulating film is patterned in the fourth patterning in production of the TFT substrate of Embodiment 2.

[0054] FIG. **27** includes schematic cross-sectional views of the regions shown in FIG. **23**, each showing a state where a contact hole is formed in fifth patterning in production of the TFT substrate of Embodiment 2.

[0055] FIG. **28** includes schematic cross-sectional views of the regions shown in FIG. **23**, each showing a state where a protective insulating layer formed from silicon oxide is formed in seventh patterning in production of the TFT substrate of Embodiment 2.

[0056] FIG. **29** includes schematic cross-sectional views of the regions shown in FIG. **23**, each showing a state where a protective insulating layer formed from transparent insulating resin is formed in the seventh patterning in production of the TFT substrate of Embodiment 2.

[0057] FIG. **30** includes schematic cross-sectional views of the regions shown in FIG. **23**, each showing a state where a contact hole is formed in the gate insulating layer and in the protective insulating layer formed from silicon oxide in the seventh patterning in production of the TFT substrate of Embodiment 2.

[0058] FIG. **31** is a schematic plan view showing the structures of one pixel and ends of lines on a TFT substrate of Embodiment 3.

[0059] FIG. **32** includes schematic cross-sectional views taken along the line A**7**-A**8** and the line B**7**-B**8** in FIG. **31**.

[0060] FIG. **33**A is a schematic cross-sectional view of a region R**5** surrounded by a broken line in FIG. **32**.

[0061] FIG. **33**B is a schematic cross-sectional view of a region R**6** surrounded by a broken line in FIG. **32**.

[0062] FIG. **34** includes schematic cross-sectional views of the regions shown in FIG. **32**, each showing a state where an insulating film is patterned in fourth patterning in production of the TFT substrate of Embodiment 3.

[0063] FIG. **35** is a schematic plan view showing the structures of one pixel and ends of lines on a TFT substrate of Comparative Embodiment 2.

[0064] FIG. **36** includes schematic cross-sectional views taken along the line A**9**-A**10** and the line B**9**-B**10** in FIG. **35**.

[0065] FIG. **37** includes schematic cross-sectional views of the regions shown in FIG. **36**, each showing a production process of a TFT substrate of Specific Example 1 of Comparative Embodiment 2.

[0066] FIG. **38** is a schematic plan view showing the structures of one pixel and ends of lines on a TFT substrate of Embodiment 4.

[0067] FIG. **39** includes schematic cross-sectional views taken along the line A**11**-A**12** and the line B**11**-B**12** in FIG. **38**.

[0068] FIG. **40**A is a schematic cross-sectional view of a region R**7** surrounded by a broken line in FIG. **39**.

[0069] FIG. **40**B is a schematic cross-sectional view of a region R**8** surrounded by a broken line in FIG. **39**.

[0070] FIG. **41** includes schematic cross-sectional views of the regions shown in FIG. **39**, each showing a state where an insulating film is patterned in fourth patterning in production of a TFT substrate of Embodiment 4.

DETAILED DESCRIPTION OF THE INVENTION

[0071] Embodiments of the present invention are described below. The embodiments, however, are not intended to limit the scope of the present invention, and modifications can be appropriately made to the design within the scope of the present invention.

Embodiment 1

[0072] FIG. **1** is a schematic plan view of a liquid crystal display device of Embodiment 1. FIG. **2** is a schematic cross-sectional view taken along the line IIA-IIB in FIG. **1**. FIG. **1** does not show a polarizing plate **58** shown in FIG. **2**.

<Structure of Liquid Crystal Display Device S>

[0073] A liquid crystal display device S includes a thin-film transistor (TFT) substrate **10** and a counter substrate **50** facing each other, a sealant **51** in a frame pattern which bonds the TFT substrate **10** and the counter substrate **50** at their outer edges, and a liquid crystal layer **52** enclosed inside the sealant **51** between the TFT substrate **10** and the counter substrate **50**.

[0074] The liquid crystal display device S is a transmissive liquid crystal display device and includes a display region D for image display in a region where the TFT substrate **10** and the counter substrate **50** overlap each other inside the sealant **51**, i.e., a region where the liquid crystal layer **52** is disposed. Outside the display region D is disposed a terminal region **10***a* that is an L-shaped part of the TFT substrate **10** protruding from the counter substrate **50**, for example.

[0075] The display region D has a rectangle shape, for example, and includes pixels, which are minimum units of an image, arranged in a matrix. On one side (left side in FIG. **1**) of the terminal region **10***a* are mounted gate driver integrated circuit (hereinafter, abbreviated to IC) chips **53** via anisotropic conductive films (hereinafter, abbreviated to ACFs). On another side (bottom side in FIG. **1**) of the terminal region **10***a* are mounted source driver IC chips **54** via ACFs.

[0076] The TFT substrate **10** and the counter substrate **50** each have a rectangle shape, for example, and as shown in FIG. **2**, respectively have alignment films **55** and **56** on their facing inner surfaces and respectively have polarizing plates **57** and **58** on their outer surfaces. The liquid crystal layer **52** is formed from a nematic liquid crystal material having electro-optical properties, for example.

<Structure of TFT Substrate **10**>

[0077] FIG. **3** and FIG. **4** show schematic structure views of the TFT substrate **10**. FIG. **3** is a schematic plan view showing the structures of one pixel and ends of lines on the TFT substrate of Embodiment 1. FIG. **4** includes schematic cross-sectional views taken along the line A**1**-A**2** and the line B**1**-B**2** in FIG. **3**. FIG. **4** shows, from left, a schematic cross-sectional view taken along the line A**1**-A**2** in FIG. **3** and a schematic cross-sectional view taken along the line B**1**-B**2** in FIG. **3**. FIG. **5**A is a schematic cross-sectional view of a region R**1** surrounded by a broken line in FIG. **4**. FIG. **5**B is a schematic cross-sectional view of a region R**2** surrounded by a broken line in FIG. **4**. FIG. **5**A and FIG. **5**B do not show the gate electrode.

[0078] As shown in FIG. **4**, the TFT substrate **10** includes an insulating substrate **12** such as a glass substrate serving as a base substrate. As shown in FIG. **3**, in the display region D, the insulating substrate **12** has parallel gate lines **14***gl* and parallel source lines **24***sl* that insect the gate lines **14***gl* via an insulating film. The gate lines **14***gl* and the source lines **24***sl* form a grid pattern to partition the pixels.

[0079] The TFT substrate **10** further includes, in each intersection of the gate lines **14***gl* and the source lines **24***sl*, i.e., in each pixel, a TFT **26**, a connection electrode **34**

functioning as the above mentioned conductive layer connected to a drain electrode **24***dd*, and a pixel electrode **30***pd* connected to a storage capacitance element **27** and the connection electrode **34**. The TFT substrate **10** also includes a common electrode **30***cd* provided in common in all the pixels.

[0080] The TFTs **26** are each a bottom-contact/bottom-gate TFT. As shown in FIG. **4** (the cross-sectional view taken along the line A**1**-A**2**), each TFT **26** includes a gate electrode **14***gd* on the insulating substrate **12**, a gate insulating layer **16** covering the gate electrode **14***gd*, a source electrode **24***sd* and the drain electrode **24***dd* facing each other above the gate electrode **14***gd* via the gate insulating layer **16**, and an oxide semiconductor layer **18***sl* which faces the gate electrode **14***gd* via the gate insulating layer **16** and whose first end and second end respectively overlap and are thereby connected to the source electrode **24***sd* and the drain electrode **24***dd*. The oxide semiconductor layer **18***sl* includes a channel region **18***c* in a region between the source electrode **24***sd* and the drain electrode **24***dd*. The source electrode **24***sd* is connected to a branch of the corresponding source line **24***sl*. The "gate electrode" as used herein means one of three electrodes constituting a TFT (the others are a source electrode and a drain electrode) and the charge generated in the channel region of the semiconductor layer is modulated in accordance with the voltage applied to the gate electrode to control the current between the source electrode and the drain electrode. The "source electrode" as used herein means one of the three electrodes constituting a TFT and is an electrode that serves as a donor for a carrier to flow in the semiconductor layer of the TFT. The "drain electrode" as used herein means one of the three electrodes constituting a TFT and is an electrode that serves as an acceptor for a carrier to flow in the semiconductor layer of the TFT.

[0081] The gate electrode **14***gd* is part of the gate line **14***gl* that constitutes the corresponding intersection and includes protrusions extending from the gate line **14***gl* to the respective sides in the width direction, as shown in FIG. **3**. Adjusting the width of each protrusion controls the channel length of the TFT **26**. Although not being shown, the gate electrode **14***gd* has a structure in which the gate line **14***gl*, an aluminum (Al) layer, and a molybdenum (Mo) layer, for example, are stacked in the stated order and integrated.

[0082] The gate insulating layer **16** is formed from, for example, silicon nitride (SiN), silicon oxide (SiO_2), or a multilayer film in which a silicon nitride film and a silicon oxide film are stacked in the stated order and integrated.

[0083] The oxide semiconductor layer **18***sl* is formed from an indium gallium zinc oxide (hereinafter, abbreviated to In—Ga—Zn—O) semiconductor. The oxide semiconductor layer **18***sl*, which is an In—Ga—Zn—O semiconductor layer in the present embodiment, may be an oxide semiconductor layer formed from an indium silicon zinc oxide (In—Si—Zn—O), an indium aluminum zinc oxide (In—Al—Zn—O), a tin silicon zinc oxide (Sn—Si—Zn—O), a tin aluminum zinc oxide (Sn—Al—Zn—O), a tin gallium zinc oxide (Sn—Ga—Zn—O), a gallium silicon zinc oxide (Ga—Si—Zn—O), a gallium aluminum zinc oxide (Ga—Al—Zn—O), an indium copper zinc oxide (In—Cu—Zn—O), a tin copper zinc oxide (Sn—Cu—Zn—O), an indium tin gallium oxide (In—Sn—Ga—O), an indium tin zinc oxide (In—Sn—Zn—O), an indium tin gallium zinc oxide (In—Sn—Ga—Zn—O), a tin oxide (Zn—O), or an indium oxide (In—O). The oxide semiconductor layer **18***sl* may be applied to a TFT substrate having a TFT formed from a combination of these oxides.

[0084] The source electrode **24***sd* and the drain electrode **24***dd* each include a first conductive layer **24***d***1** and a second conductive layer **24***d***2** covering the first conductive layer **24***d***1** . The second conductive layer **24***d***2** contains at least one element selected from the group consisting of molybdenum, tantalum, tungsten, and nickel. The gate insulating layer **16** may be contaminated in formation of the source electrode **24***sd* and the drain electrode **24***dd*, for example. Thereby, the threshold value (also referred to as threshold voltage) among the TFT properties may be unstable to possibly cause reduced on-state current. In production of the TFT substrate **10** of the present embodiment, in order to remove contaminants on the gate insulating layer **16**, for example, the surface of the gate insulating layer **16** in the region between the source electrode **24***sd* and the drain electrode **24***dd* is removed (modified) by etching with hydrofluoric acid before disposing the oxide semiconductor layer **18***sl*. This can stabilize the threshold value among the TFT properties and prevent or reduce a reduction in on-state current to achieve stable TFT properties. In the TFT substrate **10** of the present embodiment, the second conductive layer **24***d***2** contains at least one element selected from the group consisting of molybdenum, tantalum, tungsten, and nickel. When the conductive layer contains at least one element selected from the group consisting of molybdenum, tantalum, tungsten, and nickel, the conductive layer has hydrofluoric acid resistance and thus can prevent the source electrode **24***sd* and the drain electrode **24***dd* from being etched during the etching with hydrofluoric acid. This can achieve less variation in channel length of the TFT **26** in the substrate plane, and thereby can achieve less variation in carrier mobility and threshold value among the TFT properties. As a result, the TFT properties can further be stabilized.

[0085] When the surface of the gate insulating layer **16** in the region between the source electrode **24***sd* and the drain electrode **24***dd* is etched with hydrofluoric acid before disposing the oxide semiconductor layer **18***sl* as mentioned above, the gate insulating layer **16** in the region between the source electrode **24***sd* and the drain electrode **24***dd* is etched while the gate insulating layer **16** in the regions below the source electrode **24***sd* and the drain electrode **24***dd* is not etched. As a result, as shown in FIG. **5**A and FIG. **5**B, the thickness **16**D**1** of the gate insulating layer **16** in the region between the source electrode **24***sd* and the drain electrode **24***dd* is smaller than the thickness **16**D**2** of the gate insulating layer **16** in the region below the source electrode **24***sd* and is also smaller than the thickness **16**D**3** of the gate insulating layer **16** in the region below the drain electrode **24***dd*. The "thickness of a gate insulating layer" herein means the thickness from the upper surface of the base substrate (insulating substrate **12** of the present embodiment) to the upper surface of the gate insulating layer. The thickness of the gate insulating layer is expressed as the average of the thicknesses of the gate insulating layer measured at multiple points (e.g., 5 points in length×5 points in width=25 points).

[0086] The thickness **16**D**1** of the gate insulating layer is, for example, 40% or greater and 99.8% or smaller of the thickness **16**D**2** of the gate insulating layer and 40% or greater and 99.8% or smaller of the thickness **16**D**3** of the

gate insulating layer. The thickness **16**D**1** of the gate insulating layer is preferably 90% or greater and 99.5% or smaller of the thickness **16**D**2** of the gate insulating layer and 90% or greater and 99.5% or smaller of the thickness **16**D**3** of the gate insulating layer.

[0087] The first conductive layer **24***d***1** is a laminate including a lower layer **24***d***11**, a middle layer **24***d***12**, and an upper layer **24***d***13** stacked in the stated order from the insulating substrate **12** side. The middle layer **24***d***12** is sandwiched by the lower layer **24***d***11** from the bottom and the upper layer **24***d***13** from the top.

[0088] The middle layer **24***d***12** contains aluminum or copper, and the lower layer **24***d***11** and the upper layer **24***d***13** each contain titanium or molybdenum nitride. The substance (s) contained in the lower layer **24***d***11** and the upper layer **24***d***13** may be the same as each other or may be different at least in part.

[0089] The second conductive layer **24***d***2** covers the upper surface and the side surfaces of the first conductive layer **24***d***1** . The first conductive layer **24***d***1** is completely covered with a conductive layer containing at least one element selected from the group consisting of molybdenum, tantalum, tungsten, and nickel.

[0090] The second conductive layer **24***d***2** has a thickness of 10 nm or greater and 300 nm or smaller, for example. The second conductive layer **24***d***2** has a thickness of preferably 20 nm or greater and 200 nm or smaller, more preferably 40 nm or greater and 150 nm or smaller, still more preferably 90 nm or greater and 110 nm or smaller.

[0091] The second conductive layer **24***d***2** contains at least one element selected from the group consisting of molybdenum, tantalum, tungsten, and nickel. In other words, the second conductive layer **24***d***2** contains at least one substance selected from the group consisting of molybdenum, a compound containing molybdenum, tantalum, a compound containing tantalum, tungsten, a compound containing tungsten, nickel, and a compound containing nickel. The second conductive layer **24***d***2** contains, for example, at least one substance selected from the group consisting of molybdenum, molybdenum nitride, a molybdenum alloy (i.e., an alloy mainly containing molybdenum), a nitride of the molybdenum alloy, tantalum, tantalum nitride, a tantalum alloy (i.e., an alloy mainly containing tantalum), a nitride of the tantalum alloy, tungsten, tungsten nitride, a tungsten alloy (i.e., an alloy mainly containing tungsten), a nitride of the tungsten alloy, nickel, nickel nitride, a nickel alloy (i.e., an alloy mainly containing nickel), and a nitride of the nickel alloy.

[0092] Specific examples of the molybdenum nitride include MoN. Specific examples of the molybdenum alloy include MoNb, MoNi, MoNbNi, MoTa, and MoW. Specific examples of the tantalum nitride include TaN. Specific examples of the tantalum alloy include TaNb, TaW, and TaTi. Specific examples of the tungsten nitride include WN. Specific examples of the tungsten alloy include WNi, WNiFe, WNiCo, and WNiCu. Specific examples of the nickel nitride include NiN. Specific examples of the nickel alloy include NiMo and NiMoCo. The second conductive layer **24***d***2** preferably contains molybdenum or molybdenum nitride.

[0093] As shown in FIG. **4**, each TFT **26** includes no etching stopper layer on the source electrode **24***sd* and on the drain electrode **24***dd*, and the oxide semiconductor layer **18***sl* faces the gate electrode **14***gd* via the gate insulating layer **16**. The oxide semiconductor layer **18***sl* is in contact with the gate insulating layer **16** and faces the gate electrode **14***gd* in the region between the source electrode **24***sd* and the drain electrode **24***dd*.

[0094] As shown in FIG. **4**, each TFT **26** is covered with a protective insulating layer **28** formed from silicon oxide (SiO_2) and a protective insulating layer **32** formed from transparent insulating resin. The protective insulating layer **28** formed from silicon oxide can prevent the oxide semiconductor layer **18***sl* from having oxygen deficiency which may be caused by hydrogen desorption in the film when the protective insulating layer **28** is formed from a different substance such as silicon nitride. On the protective insulating layer **32** are disposed the common electrode **30***cd* and the connection electrode **34**. The common electrode **30***cd* and the connection electrode **34** are covered with a protective insulating layer **36** formed from silicon nitride (SiN) or silicon oxide (SiO_2). On the protective insulating layer **36** is disposed the pixel electrode **30***pd*.

[0095] The common electrode **30***cd* and each pixel electrode **30***pd* are each a transparent conductive film and formed from an indium tin oxide (hereinafter, referred to as ITO) or an indium zinc oxide (hereinafter, referred to as IZO). The common electrode **30***cd* is formed on the substantially entire display region D, and each pixel electrode **30***pd* is formed on the substantially entire pixel. The pixel electrode **30***pd* is provided with slits (not shown). The protective insulating layers **28** and **32** include a contact hole **20***a* and the protective insulating layer **36** includes a contact hole **20***b*. The contact holes **20***a* and **20***b* each function as a first contact hole that is formed in the region corresponding to the drain electrode **24***dd* and exposes the drain electrode **24***dd* in each pixel. The connection electrode **34** is formed in an island shape so as to be superimposed with the contact hole **20***a* in each pixel. The pixel electrode **30***pd* is connected to the drain electrode **24***dd* via the connection electrode **34** through the contact holes **20***a* and **20***b* in each pixel. In the present embodiment, the drain electrode **24***dd* and the pixel electrode **30***pd* are connected via the connection electrode **34**, and the connection electrode **34** functions as the above mentioned conductive layer. Alternatively, the pixel electrode **30***pd* may be directly connected to the drain electrode **24***dd* without the connection electrode **34**. In this case, the pixel electrode **30***pd* is directly connected to the drain electrode **24***dd* through the contact holes **20***a* and **20***b*, and the pixel electrode **30***pd* functions as the above mentioned conductive layer. In the present embodiment, the pixel electrode **30***pd* provided with slits is disposed above the common electrode **30***cd*. Alternatively, the positions of the pixel electrode **30***pd* and the common electrode **30***cd* may be switched, whereby the common electrode **30***cd* may be provided with slits and disposed above the pixel electrode **30***pd*. In this case, the pixel electrode **30***pd* is directly connected to the drain electrode **24***dd* through the contact hole **20***a* in the protective insulating layers **28** and **32** and functions as the above mentioned conductive layer.

[0096] Each storage capacitance element **27** consists of the pixel electrode **30***pd*, a dielectric layer that is a protective insulating layer in a region corresponding to the pixel electrode **30***pd*, and a common electrode in a region corresponding to the pixel electrode **30***pd* via the dielectric layer.

[0097] Each gate line **14***gl* extends to the terminal region **10***a* on which the gate driver IC chips **53** are mounted, and the lead-out end of the gate line **14***gl* constitutes a gate

terminal **14***gt* shown in FIG. **3**. This gate terminal **14***gt* is connected to a gate connection electrode **30***gt***1** disposed on the protective insulating layer **32** and to a gate connection electrode **30***gt***2** disposed on the protective insulating layer **36** through a contact hole **29***a* shown in FIG. **4** (the cross section taken along the line B**1**-B**2**), which is formed in the gate insulating layer **16** and the protective insulating layers **28** and **32**, and a contact hole **29***b* shown in FIG. **4** (the cross section taken along the line B**1**-B**2**), which is formed in the protective insulating layer **36**. The gate connection electrodes **30***gt***1** and **30***gt***2** are electrically connected to the gate driver IC chips **53**.

[0098] Each source line **24***sl* extends to the terminal region **10***a* on which the source driver IC chips **54** are mounted, and the lead-out end of the source line **24***sl* constitutes a source terminal **24***st* shown in FIG. **3**. This source terminal **24***st* is connected to a source connection electrode **30***st***1** disposed on the protective insulating layer **32** and a source connection electrode **30***st***2** disposed on the protective insulating layer **36** through a contact hole **29***c* formed in the protective insulating layers **28** and **32** and a contact hole **29***d* formed in the protective insulating layer **36**. The source connection electrodes **30***st***1** and **30***st***2** are electrically connected to the source driver IC chips **54**.

[0099] The ends of the common electrode **30***cd* reach the regions with the sealant **51** and are connected to common lines (not shown). Common voltage is applied to the common electrode **30***cd* via the common lines.

<Structure of Counter Substrate **50**>

[0100] Although not being shown, the counter substrate **50** includes a black matrix on an insulating substrate as a base substrate in a grid pattern that corresponds to the gate lines **14***gl* and the source lines **24***sl*; color filters with multiple colors including a red layer, a green layer, and a blue layer that are periodically arranged in the grid rectangles of the black matrix; an overcoat layer that is formed from transparent insulating resin and covers the black matrix and the color filters; and columnar photo spacers disposed on the overcoat layer.

<Operation of Liquid Crystal Display Device S>

[0101] In each pixel of the liquid crystal display device S having the above structure, a gate signal is sent from the corresponding gate driver IC chip **53** to the gate electrode **14***gd* via the gate line **14***gl*, whereby the TFT **26** is turned on. Then, a source signal is sent from the corresponding source driver IC chip **54** to the source electrode **24***sd* via the source line **24***sl*, whereby a predetermined charge is written in the pixel electrode **30***pd* via the oxide semiconductor layer **18***sl* and the drain electrode **24***dd* while the storage capacitance element **27** is charged. Here, a potential difference is caused between the pixel electrode **30***pd* and the common electrode **30***cd*, whereby a predetermined voltage is applied to the liquid crystal layer **52**. When the TFT **26** is turned off, the storage capacitance formed in the storage capacitance element **27** holds the voltage written in the pixel electrode **30***pd* so as not to be reduced. In each pixel of the liquid crystal display device S, the alignment of liquid crystal molecules is changed according to the magnitude of the voltage applied to the liquid crystal layer **52** to control the light transmittance of the liquid crystal layer **52**, whereby an image is displayed.

Production Method

[0102] An exemplary method for producing the TFT substrate **10** and the liquid crystal display device S is described with reference to FIG. **6** to FIG. **16**. FIG. **6** includes schematic cross-sectional views of the regions shown in FIG. **4**, each showing a state where a gate electrode is formed in first patterning in production of the TFT substrate of Embodiment 1. FIG. **7** includes schematic cross-sectional views of the regions shown in FIG. **4**, each showing a state where a gate insulating layer is formed in formation of a gate insulating layer in production of the TFT substrate of Embodiment 1. FIG. **8** includes schematic cross-sectional views of the regions shown in FIG. **4**, each showing a state where a first conductive film is patterned in second patterning in production of the TFT substrate of Embodiment 1. FIG. **9** includes schematic cross-sectional views of the regions shown in FIG. **4**, each showing a state where a second conductive film is formed in third patterning in production of the TFT substrate of Embodiment 1. FIG. **10** includes schematic cross-sectional views of the regions shown in FIG. **4**, each showing a state where the second conductive film is patterned in the third patterning in production of the TFT substrate of Embodiment 1. FIG. **11** includes schematic cross-sectional views of the regions shown in FIG. **4**, each showing a state where an oxide semiconductor layer is formed in fourth patterning in production of the TFT substrate of Embodiment 1. FIG. **12** includes schematic cross-sectional views of the regions shown in FIG. **4**, each showing a state where a protective insulating layer formed from silicon oxide is formed in fifth patterning in production of the TFT substrate of Embodiment 1. FIG. **13** includes schematic cross-sectional views of the regions shown in FIG. **4**, each showing a state where a protective insulating layer formed from transparent insulating resin is formed in the fifth patterning in production of the TFT substrate of Embodiment 1. FIG. **14** includes schematic cross-sectional views of the regions shown in FIG. **4**, each showing a state where a contact hole in formed in the gate insulating layer and in the protective insulating layer formed from silicon oxide in the fifth patterning in production of the TFT substrate of Embodiment 1. FIG. **15** includes schematic cross-sectional views of the regions shown in FIG. **4**, each showing a state where a common electrode is formed in sixth patterning in production of the TFT substrate of Embodiment 1. FIG. **16** includes schematic cross-sectional views of the regions shown in FIG. **4**, each showing a state where a protective insulating layer formed from a silicon oxide film or a silicon nitride film is formed in seventh patterning in production of the TFT substrate of Embodiment 1.

[0103] The method for producing the liquid crystal display device S of the present embodiment includes production of a TFT substrate, production of a counter substrate, attaching, and mounting.

<Production of TFT Substrate>

[0104] The production of a TFT substrate includes first patterning, formation of a gate insulating layer, second patterning, third patterning, hydrofluoric acid treatment, fourth patterning, fifth patterning, sixth patterning, seventh patterning, and eighth patterning in the stated order.

<First Patterning>

[0105] The insulating substrate **12** such as a glass substrate is prepared in advance. Then, films such as an aluminum

film (e.g., thickness: about 200 nm) and a molybdenum film (e.g., thickness: about 100 nm) are stacked thereon in the stated order by sputtering to form a laminated conductive film. Then, a resist pattern is formed on the laminated conductive film in the regions for forming the gate line **14***gl*, the gate electrode **14***gd*, and the gate terminal **14***gt* by photolithography using a first photomask. Using the resist pattern as a mask, the laminated conductive film is patterned by reactive ion etching (hereinafter, abbreviated as RIE). The RIE is a kind of dry etching and uses a chlorine-based gas. The resist pattern is removed with a resist stripper and the workpiece is washed. Thereby, the gate line **14***gl*, the gate electrode **14***gd*, and the gate terminal **14***gt* are simultaneously formed as shown in FIG. **6**.

<Formation of Gate Insulating layer>

[0106] On the substrate having the gate electrode **14***gd* and the gate terminal **14***gt* are formed a silicon nitride film (e.g., thickness: about 350 nm) and a silicon oxide film (e.g., thickness: about 50 nm) in the stated order by CVD to form the gate insulating layer **16** as shown in FIG. **7**.

<Second Patterning>

[0107] On the substrate having the gate insulating layer **16** are formed a molybdenum nitride film or a titanium film (e.g., thickness: about 50 nm), an aluminum film or a copper film (e.g., thickness: about 300 nm), and a molybdenum nitride film or a titanium film (e.g., thickness: about 100 nm) in the stated order by sputtering to form a first conductive film having a three-layer laminate structure. The first conductive film is patterned using a second photomask, whereby the first conductive layer **24***d***1** is formed as shown in FIG. **8** in which a lower layer **24***d***11** formed from molybdenum nitride or titanium, a middle layer **24***d***12** formed from an aluminum film or a copper film, and an upper layer **24***d***13** formed from molybdenum nitride or titanium are stacked in the stated order from the insulating substrate **12** side.

[0108] The lower layer **24***d***11** may be formed from molybdenum nitride, the middle layer **24***d***12** may be formed from aluminum or copper, and the upper layer **24***d***13** may be formed from molybdenum nitride. In this case, in the second patterning, a first conductive film in which a molybdenum nitride film, an aluminum film or a copper film, and a molybdenum nitride film are stacked in the stated order from the insulating substrate **12** side is patterned by wet etching with a mixed acid solution containing a phosphoric acid, acetic acid, and nitric acid, for example.

[0109] Alternatively, the lower layer **24***d***11** may be formed from titanium, the middle layer **24***d***12** may be formed from aluminum or copper, and the upper layer **24***d***13** may be formed from titanium. In this case, in the second patterning, a first conductive film in which a titanium film, an aluminum film or a copper film, and a titanium film are stacked in the stated order from the insulating substrate **12** side is patterned by dry etching, for example. When the dry etching is performed by RIE, for example, the RIE is performed using as a raw material gas a mixed gas containing Cl_2 (flow rate: about 100 sccm) and BCl_3 (flow rate: about 100 sccm) at a chamber pressure of about 4 Pa and at a high frequency power of about 1100 W, for example.

<Third Patterning>

[0110] On the substrate having the first conductive layer **24***d***1** is formed a second conductive film **24***d***20** formed from a molybdenum film or a molybdenum nitride film (e.g., thickness: about 100 nm) by sputtering as shown in FIG. **9**. The second conductive film is patterned using a third photomask, whereby the source electrode **24***sd* formed from the first conductive layer **24***d***1** and the second conductive layer **24***d***2** covering the first conductive layer **24***d***1** and the drain electrode **24***dd* formed from the first conductive layer **24***d***1** and the second conductive layer **24***d***2** covering the first conductive layer **24***d***1** are formed as shown in FIG. **10**. In the present embodiment, a molybdenum film or a molybdenum nitride film is formed as the second conductive film. The second conductive film is a film containing at least one element selected from the group consisting of molybdenum, tantalum, tungsten, and nickel. Specific examples of the second conductive film include, in addition to a molybdenum film and a molybdenum nitride film, a film formed from a molybdenum alloy, a film formed from a nitride of the molybdenum alloy, a tantalum film, a tantalum nitride film, a film formed from a tantalum alloy, a film formed from a nitride of the tantalum alloy, a tungsten film, a tungsten nitride film, a film formed from a tungsten alloy, a film formed from a nitride of the tungsten alloy, a nickel film, a nickel nitride film, a film formed from a nickel alloy, and a film formed from a nitride of the nickel alloy.

<Hydrofluoric Acid Treatment>

[0111] The gate insulating layer **16** side surface of the insulating substrate **12** is treated with hydrofluoric acid, whereby the surface of the gate insulating layer **16** is removed (modified) in the region between the source electrode **24***sd* and the drain electrode **24***dd*. Thereby, the surface of the gate insulating layer **16** in the region between the source electrode **24***sd* and the drain electrode **24***dd*, which may be contaminated during formation of the source electrode **24***sd* and the drain electrode **24***dd*, can be removed (modified) before the oxide semiconductor layer **18***sl* is formed in the fourth patterning. This can stabilize the threshold value among the TFT properties and prevent or reduce a reduction in on-state current to achieve stable TFT properties. In the present embodiment, the source electrode **24***sd* and the drain electrode **24***dd* include on their top surfaces the second conductive layer **24***d***2** that contains at least one element selected from the group consisting of molybdenum, tantalum, tungsten, and nickel. When the conductive layer contains at least one element selected from the group consisting of molybdenum, tantalum, tungsten, and nickel, the conductive layer has hydrofluoric acid resistance. Accordingly, even when the hydrofluoric acid treatment is performed after formation of the source electrode **24***sd* and the drain electrode **24***dd*, the conductive layer can prevent the source electrode **24***sd* and the drain electrode **24***dd* from being etched. This can resultantly achieve less variation in channel length of the TFT **26** in the substrate plane. Thereby, the TFT properties can further be stabilized.

[0112] The hydrofluoric acid treatment after formation of the source electrode **24***sd* and the drain electrode **24***dd* may be performed at a hydrofluoric acid concentration of 0.1% or higher and 20% or lower and at a temperature of 20 degrees or higher and 40 degrees or lower, for example.

<Fourth Patterning>

[0113] Then, an oxide semiconductor film (e.g., thickness: about 70 nm) formed from an In—Ga—Zn—O-based oxide

semiconductor is formed by sputtering so as to cover the source electrode **24***sd* and the drain electrode **24***dd*. Then, a resist pattern is formed for the oxide semiconductor film by photolithography using a first photomask. Using the resist pattern as a mask, the oxide semiconductor film is patterned by wet etching with an oxalic acid liquid. The resist pattern is removed with a resist stripper and the workpiece is washed. Thereby, the oxide semiconductor layer **18***sl* is formed as shown in FIG. **11**.

<Fifth Patterning (Formation of Protective Insulating Layer and Annealing)>

[0114] On the substrate having the source electrode **24***sd* and the drain electrode **24***dd* is formed a silicon oxide film by CVD to form the protective insulating layer **28** (e.g., thickness: about 270 nm) as shown in FIG. **12**.

[0115] The substrate having the protective insulating layer **28** is subjected to high temperature anneal treatment in an annealing chamber with an oxygen-containing atmosphere at a temperature of about 100° C. to about 450° C. and at an atmospheric pressure using an oxygen gas as a carrier gas. The protective insulating layer **28** formed from silicon oxide generally has a higher oxygen transmittance than a silicon nitride film, for example. Thus, oxygen used in the anneal treatment is effectively supplied to the channel region **18***c* of the oxide semiconductor layer **18***sl*. Even when the channel region **18***c* of the oxide semiconductor layer **18***sl* has been exposed to plasma by the CVD for forming the protective insulating layer **28** and thereby oxygen in the channel region **18***c* has been lost, the anneal treatment after formation of the protective insulating layer **28** can supplement the oxygen deficiency in the oxide semiconductor layer **18***sl*, whereby the properties of the oxide semiconductor layer **18***sl* can be stabilized.

[0116] On the substrate after the anneal treatment is formed a transparent insulating resin film (e.g., thickness: about 2 μm) formed from a positive photosensitive acrylic transparent resin by spin coating or slit coating. Then (after pre-baking), the regions for forming the contact holes **20***a*, **29***a*, and **29***c* and the regions to be removed are exposed to light by photolithography using a fifth photomask and developed, whereby patterning is performed. In order to make the resin transparent (bleached), the entire surface is exposed to light at an exposure dose of 280 to 350 mJ/cm^2 and then post-baked at 200° C. to 230° C., whereby the protective insulating layer **32** is formed as shown in FIG. **13**.

[0117] Using the pattern of the protective insulating layer **32** as a mask, the gate insulating layer **16** and the protective insulating layer **28** are patterned by reactive ion etching (hereinafter, abbreviated to RIE) using a fluorine-based gas, whereby the contact holes **20***a*, **29***a*, and **29***c* are formed as shown in FIG. **3** and FIG. **14**. In the present embodiment, the protective insulating layer **28** is patterned using the pattern of the protective insulating layer **32** as a mask. Alternatively, before formation of the protective insulating layer **32**, a resist pattern may be formed by conventional photolithography using a photomask, and the protective insulating layer **28** may be patterned using this resist pattern as a mask. Alternatively, after formation of the protective insulating layers **28** and **32**, a resist pattern may be formed by conventional photolithography using a photomask, and the protective insulating layers **28** and **32** may be patterned using this resist pattern as a mask.

<Sixth Patterning>

[0118] On the substrate having the patterned protective insulating layers **28** and **32** is formed a transparent conductive film such as an ITO film or an IZO film (e.g., thickness: about 70 nm) by sputtering. Then, a resist pattern is formed on the transparent conductive film in the regions for forming the common electrode **30***cd*, the connection electrode **34**, the gate connection electrode **30***gt***1**, and the source connection electrode **30***st***1** by photolithography using a sixth photomask. Using the resist pattern as a mask, the transparent conductive film is patterned by wet etching with an oxalic acid liquid. The resist pattern is removed with a resist stripper and the workpiece is washed. Thereby, the common electrode **30***cd*, the connection electrode **34**, the gate connection electrode **30***gt***1**, and the source connection electrode **30***st***1** are formed as shown in FIG. **15**.

<Seventh Patterning>

[0119] On the substrate having members such as the common electrode **30***cd* and the connection electrode **34**, a silicon oxide film or a silicon nitride film is formed by CVD to form the protective insulating layer **36** (e.g., thickness: about 300 nm).

[0120] On the substrate having the protective insulating layer **36** is formed a resist pattern with openings in the regions for forming the contact holes **20***b*, **29***b*, and **29***d* by photolithography using a seventh photomask. Using the resist pattern as a mask, the protective insulating layer **36** is patterned by RIE with a fluorine-based gas. The resist pattern is removed with a resist stripper and the workpiece is washed. Thereby, the contact holes **20***b*, **29***b*, and **29***d* are formed as shown in FIG. **3** and FIG. **16**.

<Eighth Patterning>

[0121] On the substrate having the contact holes **20***b*, **29***b*, and **29***d*, a transparent conductive film such as an ITO film or an IZO film (e.g., thickness: about 70 nm) is formed by sputtering. Then, a resist pattern is formed on the transparent conductive film in the regions for forming the pixel electrode **30***pd*, the gate connection electrode **30***gt***2**, and the source connection electrode **30***st***2** by photolithography using an eighth photomask. Using the resist pattern as a mask, the transparent conductive film is patterned by wet etching with an oxalic acid liquid. The resist pattern is removed with a resist stripper and the workpiece is washed. Thereby, the pixel electrode **30***pd*, the gate connection electrode **30***gt***2**, and the source connection electrode **30***st***2** are formed.

[0122] These steps provide the TFT substrate **10** shown in FIG. **4**.

[0123] Here, a comparative embodiment is given and the difference from the present embodiment is described. FIG. **17** is a schematic plan view showing the structures of one pixel and ends of lines on a TFT substrate of Comparative Embodiment 1. FIG. **18** includes schematic cross-sectional views taken along the line A**3**-A**4** and the line B**3**-B**4** in FIG. **17**. FIG. **18** shows, from left, a schematic cross-sectional view taken along the line A**3**-A**4** in FIG. **17** and a schematic cross-sectional view taken along the line B**3**-B**4** in FIG. **17**.

[0124] The TFT substrate of the present embodiment is a bottom-contact substrate, while the TFT substrate of Comparative Embodiment 1 is a top-contact substrate as shown in FIG. **17** and FIG. **18**. The TFT substrate of Comparative

Embodiment 1 has the same structure as that of the TFT substrate **10** of the present embodiment except for the position of the oxide semiconductor layer **18***sl* and the structures of a source electrode **24***sdr* and a drain electrode **24***ddr*. The oxide semiconductor layer **18***sl* of the TFT substrate of Comparative Embodiment 1 is disposed between the gate insulating layer **16** and the source electrodes **24***sdr* and between the gate insulating layer **16** and the drain electrodes **24***ddr*.

[0125] The source electrode **24***sdr* and the drain electrode **24***ddr* of the TFT substrate of Comparative Embodiment 1 are each formed from a first conductive layer **24***d***1***r*. The first conductive layer **24***d***1***r* has a laminate structure including a lower layer **24***d***11***r*, a middle layer **24***d***12***r*, and an upper layer **24***d***13***r* stacked in the stated order from the insulating substrate **12** side. Specific examples of the structure of the first conductive layer **24***d***1***r* include a structure in which the lower layer **24***d***11***r* formed from titanium, the middle layer **24***d***12***r* formed from aluminum or copper, and the upper layer **24***d***13***r* formed from titanium are stacked (hereinafter, also referred to as Specific Example 1 of Comparative Embodiment 1), and a structure in which the lower layer **24***d***11***r* formed from titanium, the middle layer **24***d***12***r* formed from aluminum or copper, and the upper layer **24***d***13***r* formed from molybdenum or molybdenum nitride are stacked (hereinafter, also referred to as Specific Example 2 of Comparative Embodiment 1).

[0126] FIG. **19** includes schematic cross-sectional views of the regions shown in FIG. **18**, each showing a production process of the TFT substrate of Specific Example 1 of Comparative Embodiment 1. FIG. **20** and FIG. **21** each include schematic cross-sectional views of the regions shown in FIG. **18**, each showing a production process of the TFT substrate of Specific Example 2 of Comparative Embodiment 1. In production of the TFT substrate of Comparative Embodiment 1, the gate lines **14***gl*, the gate electrodes **14***gd*, and the gate terminals **14***gt* are formed, the gate insulating layer **16** is formed, and then the oxide semiconductor layer **18***sl* is formed. Next, the first conductive film as a material of the first conductive layer **24***d***1***r* is formed and then etched to form the source electrodes **24***sdr* and the drain electrodes **24***dd*. In the case of Specific Example 1 of Comparative Embodiment 1, the first conductive film is etched by dry etching. Here, as shown in FIG. **19**, the channel portion of each TFT suffers plasma damage by the dry etching. The TFT properties are thereby degraded, and thus the threshold value is significantly reduced to have a negative value. As a result, the TFT fails to function as a switching element. In the case of Specific Example 2 of Comparative Embodiment 1, as shown in FIG. **20**, a molybdenum film or a molybdenum nitride film (corresponding to the upper layer **24***d***13***r*) and an aluminum film or a copper film (corresponding to the middle layer **24***d***12***r*) of the first conductive film are etched by wet etching using a mixed acid solution containing phosphoric acid, acetic acid, and nitric acid. Then, as shown in FIG. **21**, a titanium film (corresponding to the lower layer **24***d***11***r*) is etched by dry etching. Here, similarly to Specific Example 1 of Comparative Embodiment 1, the channel portion of each TFT suffers plasma damage by the dry etching. The TFT properties are thereby degraded and the threshold value is significantly reduced to have a negative value. As a result, the TFT fails to function as a switching element.

[0127] In contrast, in the method for producing the TFT substrate **10** of the present embodiment, as mentioned above, the surface of the gate insulating layer **16** in the TFT channel portion can be modified while preventing the channel side end of each source electrode **24***sd* and the channel side end of each drain electrode **24***dd* from being etched. As a result, the threshold value among the TFT properties can be stable to prevent malfunction of the switching element.

<Production of Counter Substrate>

[0128] To an insulating substrate such as a glass substrate is applied a black photosensitive resin by spin coating or slit coating, for example. The applied film is exposed to light using a photomask and then developed to be patterned, whereby a black matrix is formed.

[0129] To the substrate having the black matrix is applied a red, green, or blue negative acrylic photosensitive resin, for example. The applied film is exposed to light using a photomask and then developed to be patterned, whereby a color layer in the selected color (e.g., red layer) is formed. Two color layers in other two colors (e.g., green layer and blue layer) are formed in the same manner as above, whereby color filters are formed.

[0130] On the substrate having the color filters is formed a transparent insulating resin film formed from acrylic transparent resin by spin coating or slit coating, for example, whereby an overcoat layer is formed.

[0131] To the substrate having the overcoat layer is applied a positive phenol novolac-based photosensitive resin by spin coating. The applied film is exposed to light using a photomask and then developed to be patterned, whereby photo spacers are formed.

[0132] These steps provide the counter substrate **50**.

<Attaching>

[0133] To a surface of the TFT substrate **10** is applied a polyimide-based resin by printing. The applied film is subjected to baking and rubbing treatment, whereby an alignment film **55** is formed. Similarly, to a surface of the counter substrate **50** is applied a polyimide-based resin by printing. The applied film is subjected to baking and rubbing treatment, whereby the alignment film **56** is formed.

[0134] To the counter substrate **50** having the alignment film **56**, the sealant **51** such as a combination resin having ultraviolet curability and heat curability is applied in a rectangular frame pattern using a tool such as a dispenser. Then, a predetermined amount of liquid crystal material is dropped in the region inside the sealant **51** on the counter substrate **50**.

[0135] The counter substrate **50** with the dropped liquid crystal material and the TFT substrate **10** having the alignment film **55** are attached together under reduced pressure. The attached workpiece is placed under atmospheric pressure, whereby the surfaces of the attached workpiece are pressurized. The sealant **51** of the attached workpiece is irradiated with ultra violet (UV) light to be pre-cured. The attached workpiece is then heated so that the sealant **51** is post-cured, whereby the TFT substrate **10** and the counter substrate **50** are bonded.

[0136] Then, polarizing plates **57** and **58** are attached to the respective outer surfaces of the TFT substrate **10** and the counter substrate **50** that are bonded to each other.

<Mounting>

[0137] ACFs are placed in the terminal region **10***a* of the attached workpiece whose surfaces are covered with the polarizing plates **57** and **58**. Then, the gate driver IC chips **53** and the source driver IC chips **54** are mounted on the ACFs in the terminal region **10***a* of the attached workpiece by thermocompression bonding.

[0138] These steps provide the liquid crystal display device S.

Embodiment 2

[0139] In the present embodiment, the characteristic features of the present embodiment are mainly described and the same points as in Embodiment 1 are not described. The components having the same or a similar function have the same reference numerals in both the present embodiment and Embodiment 1, and such components are not described in the present embodiment. The present embodiment is substantially the same as Embodiment 1 except that the TFTs include an etching stopper layer, as described below.

<Structure of TFT Substrate **10**>

[0140] FIG. **22** and FIG. **23** show schematic structure views of the TFT substrate **10** of the present embodiment. FIG. **22** is a schematic plan view showing the structures of one pixel and ends of lines on the TFT substrate of Embodiment 2. FIG. **23** includes schematic cross-sectional views taken along the line A**5**-A**6** and the line B**5**-B**6** in FIG. **22**. FIG. **23** shows, from left, a schematic cross-sectional view taken along the line A**5**-A**6** in FIG. **22** and a schematic cross-sectional view taken along the line B**5**-B**6** in FIG. **22**.

[0141] In this embodiment, the TFT substrate **10** has the same planar layout as of the TFT substrate **10** of Embodiment 1 except that, as shown in FIG. **22**, the later described etching stopper layer **40** has contact holes **38** each in a region overlapping the corresponding source electrode **24***sd* and drain electrode **24***dd*.

[0142] In the TFT substrate **10**, as shown in FIG. **23**, the etching stopper layer **40** (e.g., thickness: about 200 nm) formed from silicon oxide (SiO_2) covers the source electrode **24***sd* except for a connection portion **41***s* between the oxide semiconductor layer **18***sl* and the source electrode **24***sd* and covers the drain electrode **24***dd* except for a connection portion **41***d* between the oxide semiconductor layer **18***sl* and the drain electrode **24***dd* and a connection portion **41***p* between the pixel electrode **30***pd* and the drain electrode **24***dd*, and the connection portions **41***s* and **41***d* are located in a region with the gate electrode **14***gd*. In the present embodiment, the etching stopper layer **40** is formed from SiO_2. Alternatively, the etching stopper layer **40** may be a laminate including a SiN film (e.g., thickness: about 100 nm) and a SiO_2 film (e.g., thickness: about 100 nm) stacked in the stated order from the insulating substrate **12** side, a laminate including a SiO_2 film (e.g., thickness: about 100 nm) and a SiN film (e.g., thickness: about 100 nm) stacked in the stated order from the insulating substrate **12** side, a SiN film (e.g., thickness: about 200 nm), or a SiON film (e.g., thickness: about 200 nm).

[0143] Here, in formation of the oxide semiconductor layer **18***sl*, when the oxide semiconductor film is etched with a mixed acid solution containing phosphoric acid, acetic acid, and nitric acid, for example, the source electrode **24***sd* and the drain electrode **24***dd* may also be etched with the mixed acid solution. The presence of the etching stopper layer **40** as in the present embodiment can prevent the source electrode **24***sd* and the drain electrode **24***dd* from being etched.

[0144] The phrase "the connection portion **41***s* is located in a region with the gate electrode **14***gd*" means that, in a plan view, at least part of the connection portion **41***s* is in a region with the gate electrode **14***gd*. Similarly, the phrase "the connection portion **41***d* is located in a region with the gate electrode **14***gd*" means that, in a plan view, at least part of the connection portion **41***d* is in a region with the gate electrode **14***gd*.

[0145] The contact hole **29***a* for connecting the gate connection electrode **30***gt***1** is formed in the gate insulating layer **16**, the etching stopper layer **40**, and the protective insulating layers **28** and **32**.

[0146] The etching stopper layer **40** is not present in the region between the oxide semiconductor layer **18***sl* and the gate insulating layer **16**, and the oxide semiconductor layer **18***sl* faces the gate electrode **14***gd* via the gate insulating layer **16**.

[0147] FIG. **24**A is a schematic cross-sectional view of the region R**3** surrounded by a broken line in FIG. **23**. FIG. **24**B is a schematic cross-sectional view of the region R**4** surrounded by a broken line in FIG. **23**. The source electrode **24***sd* and the drain electrode **24***dd* each include the first conductive layer **24***d***1** and the second conductive layer **24***d***2** covering the first conductive layer **24***d***1** . The second conductive layer **24***d***2** contains at least one element selected from the group consisting of molybdenum, tantalum, tungsten, and nickel. The gate insulating layer **16** may be contaminated in formation of the source electrode **24***sd* and the drain electrode **24***dd*, for example. Thereby, the threshold value among the TFT properties may be unstable to possibly cause reduced on-state current. In production of the TFT substrate **10** of the present embodiment, in order to remove contaminants on the gate insulating layer **16**, for example, the surface of the gate insulating layer **16** in the region between the source electrode **24***sd* and the drain electrode **24***dd* is removed (modified) by etching with hydrofluoric acid before disposing the oxide semiconductor layer **18***sl*. This can stabilize the threshold value among the TFT properties and prevent or reduce a reduction in on-state current to achieve stable TFT properties. In the TFT substrate **10** of the present embodiment, the second conductive layer **24***d***2** contains at least one element selected from the group consisting of molybdenum, tantalum, tungsten, and nickel. When the conductive layer contains at least one element selected from the group consisting of molybdenum, tantalum, tungsten, and nickel, the conductive layer has hydrofluoric acid resistance and thus can prevent the source electrode **24***sd* and the drain electrode **24***dd* from being etched during the etching with hydrofluoric acid. This can achieve less variation in channel length of the TFT **26** in the substrate plane, and thereby can achieve less variation in carrier mobility and threshold value among the TFT properties. As a result, the TFT properties can further be stabilized.

[0148] When the surface of the gate insulating layer **16** in the region between the source electrode **24***sd* and the drain electrode **24***dd* is etched with hydrofluoric acid before disposing the oxide semiconductor layer **18***sl* as mentioned above, the gate insulating layer **16** in the region between the source electrode **24***sd* and the drain electrode **24***dd* is etched

while the gate insulating layer **16** in the regions below the source electrode **24***sd* and the drain electrode **24***dd* is not etched. As a result, as shown in FIG. **24**A and FIG. **24**B, the thickness **16**D**1** of the gate insulating layer **16** in the region between the source electrode **24***sd* and the drain electrode **24***dd* is smaller than the thickness **16**D**2** of the gate insulating layer **16** in the region below the source electrode **24***sd* and is also smaller than the thickness **16**D**3** of the gate insulating layer **16** in the region below the drain electrode **24***dd*.

[0149] The thickness **16**D**1** of the gate insulating layer is, for example, 40% or greater and 99.8% or smaller of the thickness **16**D**2** of the gate insulating layer and 40% or greater and 99.8% or smaller of the thickness **16**D**3** of the gate insulating layer. The thickness **16**D**1** of the gate insulating layer is preferably 90% or greater and 99.5% or smaller of the thickness **16**D**2** of the gate insulating layer and 90% or greater and 99.5% or smaller of the thickness **16**D**3** of the gate insulating layer.

Production Method

[0150] An exemplary method for producing the TFT substrate **10** of the present embodiment is described with reference to FIG. **25** to FIG. **30**. FIG. **25** includes schematic cross-sectional views of the regions shown in FIG. **23**, each showing a state where an insulating film is formed in fourth patterning in production of the TFT substrate of Embodiment 2. FIG. **26** includes schematic cross-sectional views of the regions shown in FIG. **23**, each showing a state where an insulating film is patterned in the fourth patterning in production of the TFT substrate of Embodiment 2. FIG. **27** includes schematic cross-sectional views of the regions shown in FIG. **23**, each showing a state where a contact hole is formed in fifth patterning in production of the TFT substrate of Embodiment 2. FIG. **28** includes schematic cross-sectional views of the regions shown in FIG. **23**, each showing a state where a protective insulating layer formed from silicon oxide is formed in seventh patterning in production of the TFT substrate of Embodiment 2. FIG. **29** includes schematic cross-sectional views of the regions shown in FIG. **23**, each showing a state where a protective insulating layer formed from transparent insulating resin is formed in the seventh patterning in production of the TFT substrate of Embodiment 2. FIG. **30** includes schematic cross-sectional views of the regions shown in FIG. **23**, each showing a state where a contact hole is formed in the gate insulating layer and in the protective insulating layer formed from silicon oxide in the seventh patterning in production of the TFT substrate of Embodiment 2.

<Production of TFT Substrate>

[0151] The production of a TFT substrate includes first patterning to tenth patterning.

<First Patterning to Third Patterning>

[0152] In the same manner as in Embodiment 1, the first patterning to the third patterning and the hydrofluoric acid treatment (hereinafter, also referred to as first hydrofluoric acid treatment) are performed.

<Fourth Patterning>

[0153] On the substrate having the source electrode **24***sd* and the drain electrode **24***dd* is formed a silicon oxide film by CVD to form the insulating film **400** (e.g., thickness: about 200 nm) as shown in FIG. **25**.

[0154] On the substrate having the insulating film **400** is formed a resist pattern with openings in the regions for forming the contact holes **29***a* and **38** by photolithography using a fourth photomask. Using the resist pattern as a mask, the insulating film **400** is patterned by RIE with a fluorine-based gas. Thereby, the contact hole **38** and an opening **29***a* **1** for forming the contact hole **29***a* are formed as shown in FIG. **26**.

<Second Hydrofluoric Acid Treatment>

[0155] The gate insulating layer **16** side surface of the insulating substrate **12** is treated with hydrofluoric acid. This second hydrofluoric acid treatment may be performed at a hydrofluoric acid concentration of 0.2% or higher and 20% or lower and at a temperature of 20 degrees or higher and 40 degrees or lower, for example.

<Fifth Patterning>

[0156] The same process as in the fourth patterning of Embodiment 1 is performed. In the present embodiment, the etching stopper layer **40** is disposed. Thus, even when the oxide semiconductor film is etched in the fifth patterning with the etchant (e.g., mixed acid solution) used for etching of the first conductive film and/or the second conductive film, the etching stopper layer **40** can prevent the source electrode **24***sd* and the drain electrode **24***dd* from being etched by the etchant.

<Sixth Patterning>

[0157] On the substrate having the oxide semiconductor layer **18***sl*, a resist pattern with an opening in the region for forming the contact hole **20***a* is formed by photolithography using a sixth photomask. Using the resist pattern as a mask, the gate insulating layer **16** and the etching stopper layer **40** are patterned by RIE with a fluorine-based gas. Thereby, an opening **20***a***1** for forming the contact hole **20***a* and an opening **29***a***11** for forming the contact hole **29***a* are formed as shown in FIG. **27**. In the present embodiment, the patterning of the etching stopper layer **40** in the region with the gate terminal **14***gt* and the patterning of the gate insulating layer **16** in the region with the gate terminal **14***gt* are separately performed in the fourth patterning and the sixth patterning, respectively. If the etching stopper layer **40** and the gate insulating layer **16** are collectively etched, the gate insulating layer **16** in the channel portion is also etched to be eliminated. Thus, the gate insulating layer **16** is etched in the sixth patterning after the oxide semiconductor layer **18***sl* is disposed in the fifth patterning. In the case where the oxide semiconductor film is etched in the fifth patterning with the etchant (e.g., mixed acid solution) used for etching the first conductive film and/or the second conductive film and the opening **20***a* **1** is formed in the drain electrode **24***dd* after disposing the oxide semiconductor layer **18***sl*, the oxide semiconductor film can be etched without etching the drain electrode **24***dd* exposed through the opening **20***a* **1**. Thus, the etching stopper layer **40** also functions as an etching stopper layer that prevents the drain electrode **24***dd* from being processed.

<Seventh Patterning (Formation of Protective Insulating Layer and Annealing)>

[0158] The same process as that in the fifth patterning (formation of protective insulating layer and annealing) of Embodiment 1 is performed. Seventh patterning in the present embodiment is performed as shown in FIGS. **28** to **30**.

[0159] In the present embodiment, the gate insulating layer **16** in the region with the gate terminal **14***gt* is etched in the sixth patterning. Thus, in the seventh patterning, as shown in FIG. **28**, the protective insulating layer **28** is disposed to be in contact with the gate terminal **14***gt*. Then, in the same manner as in Embodiment 1, the protective insulating layer **32** is disposed as shown in FIG. **29**, and the contact holes **20***a* and **29***a* are formed as shown in FIG. **30**.

<Eighth Patterning to Tenth Patterning>

[0160] The same processes as in the sixth patterning to the eighth patterning of Embodiment 1 are performed, whereby the TFT substrate **10** as shown in FIG. **23** can be produced.

Embodiment 3

[0161] In the present embodiment, the characteristic features of the present embodiment are mainly described and the same points as in Embodiment 1 or 2 are not described. The components having the same or a similar function have the same reference numerals in both the present embodiment and Embodiment 1 or 2, and such components are not described in the present embodiment. The present embodiment is substantially the same as Embodiment 2 except that the etching stopper layer has a different shape, as described below.

<Structure of TFT Substrate **10**>

[0162] FIG. **31** and FIG. **32** show schematic structure views of the TFT substrate **10** of the present embodiment. FIG. **31** is a schematic plan view showing the structures of one pixel and ends of lines on a TFT substrate of Embodiment 3. FIG. **32** includes schematic cross-sectional views taken along the line A**7**-A**8** and the line B**7**-B**8** in FIG. **31**. FIG. **32** shows, from left, a schematic cross-sectional view taken along the line A**7**-A**8** in FIG. **31** and a schematic cross-sectional view taken along the line B**7**-B**8** in FIG. **31**.

[0163] In this embodiment, the TFT substrate **10** has the same planar layout as of the TFT substrate **10** of Embodiment 2 except that, as shown in FIG. **31**, the etching stopper layer **40** has a contact hole **38***s* as the second contact hole and a contact hole **38***d* as the third contact hole. The contact hole **38***s* overlaps an end of the source electrode **24***sd* and the gate insulating layer **16** in a part adjacent to the end of the source electrode **24***sd*. The contact hole **38***d* overlaps an end of the drain electrode **24***dd* and the gate insulating layer **16** in a part adjacent to the end of the drain electrode **24***dd*.

[0164] In the TFT substrate **10**, as shown in FIG. **32**, the etching stopper layer **40** is present in a region between the oxide semiconductor layer **18***sl* and the gate insulating layer **16**, and the oxide semiconductor layer **18***sl* is connected to the source electrode **24***sd* via the contact hole **38***s* formed in the etching stopper layer **40** and connected to the drain electrode **24***dd* via the contact hole **38***d* formed in the etching stopper layer **40**. The source electrode **24***sd* and the drain electrode **24***dd* are connected to the oxide semiconductor layer **18***sl* via the contact holes **38***s* and **38***d* formed in the etching stopper layer **40**.

[0165] FIG. **33**A is a schematic cross-sectional view of the region R**5** surrounded by a broken line in FIG. **31**. FIG. **33**B is a schematic cross-sectional view of the region R**6** surrounded by a broken line in FIG. **31**. The source electrode **24***sd* and the drain electrode **24***dd* each include the first conductive layer **24***d***1** and the second conductive layer **24***d***2** covering the first conductive layer **24***d***1** . The second conductive layer **24***d***2** contains at least one element selected from the group consisting of molybdenum, tantalum, tungsten, and nickel. The gate insulating layer **16** may be contaminated in formation of the source electrode **24***sd* and the drain electrode **24***dd*, for example. In this case, the threshold value among the TFT properties is unstable to possibly cause reduced on-state current. In production of the TFT substrate **10** of the present embodiment, in order to remove contaminants on the gate insulating layer **16**, for example, the surface of the gate insulating layer **16** in the region between the source electrode **24***sd* and the drain electrode **24***dd* is removed (modified) by etching with hydrofluoric acid before disposing the oxide semiconductor layer **18***sl*. This can stabilize the threshold value among the TFT properties and prevent or reduce a reduction in on-state current to achieve stable TFT properties.

[0166] Here, the TFT substrate **10** of the present embodiment includes the etching stopper layer **40** that can prevent the source electrode **24***sd* and the drain electrode **24***dd* from being etched in formation of the oxide semiconductor layer **18***sl*, as mentioned above. The etching stopper layer **40** is disposed on the source electrode **24***sd* and on the drain electrode **24***dd*, and is also disposed between the gate insulating layer **16** and the oxide semiconductor layer **18***sl* in a region between the source electrode **24***sd* and the drain electrode **24***dd*. The surface of the etching stopper layer **40** and the surface of the gate insulating layer **16** in the regions where the gate insulating layer **16** is in direct contact with the oxide semiconductor layer **18***sl*, i.e., the region between the etching stopper layer **40** and the source electrode **24***sd* and the region between the etching stopper layer **40** and the drain electrode **24***dd*, may be contaminated in the formation of the etching stopper layer **40**, for example. When the oxide semiconductor layer **18***sl* is formed on the contaminated etching stopper layer **40** and gate insulating layer **16**, the threshold value among the TFT properties may be unstable to possibly cause reduced on-state current. In production of the TFT substrate **10** of the present embodiment, in order to remove contaminants on the surface of the etching stopper layer **40** and the surface of the gate insulating layer **16**, for example, after formation of the etching stopper layer **40**, the surface of the etching stopper layer **40** and the surface of the gate insulating layer **16** are removed (modified) by etching with hydrofluoric acid, and then the oxide semiconductor layer **18***sl* is formed. Thereby, the TFT properties can be stabilized to a similar extent to the case without the etching stopper layer **40**.

[0167] In the TFT substrate **10** of the present embodiment, the second conductive layer **24***d***2** contains at least one element selected from the group consisting of molybdenum, tantalum, tungsten, and nickel. When the conductive layer contains at least one element selected from the group consisting of molybdenum, tantalum, tungsten, and nickel, the conductive layer has hydrofluoric acid resistance and thus can prevent the source electrode **24***sd* and the drain

electrode **24***dd* from being etched during the etching with hydrofluoric acid. This can achieve less variation in channel length of the TFT **26** in the substrate plane, and thereby can achieve less variation in carrier mobility and threshold value among the TFT properties. As a result, the TFT properties can further be stabilized.

[0168] When the surface of the gate insulating layer **16** in the region between the source electrode **24***sd* and the drain electrode **24***dd* is etched with hydrofluoric acid before disposing the oxide semiconductor layer **18***sl* as mentioned above, the gate insulating layer **16** in the region between the source electrode **24***sd* and the drain electrode **24***dd* is etched while the gate insulating layer **16** in the regions below the source electrode **24***sd* and the drain electrode **24***dd* is not etched. As a result, as shown in FIG. **33**A and FIG. **33**B, thicknesses **16**D**11**, **16**D**12**, and **16**D**4** of the gate insulating layer **16** in the region between the source electrode **24***sd* and the drain electrode **24***dd* are smaller than the thickness **16**D**2** of the gate insulating layer **16** in the region below the source electrode **24***sd* and are also smaller than the thickness **16**D**3** of the gate insulating layer **16** in the region below the drain electrode **24***dd*.

[0169] In the present embodiment, the etching with hydrofluoric acid is performed twice, i.e., before and after disposing the etching stopper layer **40**. Accordingly, in a region between the source electrode **24***sd* and the drain electrode **24***dd*, the gate insulating layer **16** in the part below the etching stopper layer **40** is treated with hydrofluoric acid once before formation of the etching stopper layer **40**, while the gate insulating layer **16** in the parts below the contact hole **38***s* and below the contact hole **38***d* is treated with hydrofluoric acid twice, i.e., before and after formation of the etching stopper layer **40**. As a result, in a region between the source electrode **24***sd* and the drain electrode **24***dd*, the gate insulating layer **16** in the part below the etching stopper layer **40** has the thickness **16**D**4** larger than the thickness **16**D**11** of the gate insulating layer **16** in the part below the contact hole **38***s* and larger than the thickness **16**D**12** of the gate insulating layer **16** in the part below the contact hole **38***d*.

[0170] The thickness **16**D**4** of the gate insulating layer is, for example, 40% or greater and 99.8% or smaller of the thickness **16**D**2** of the gate insulating layer and 40% or greater and 99.8% or smaller of the thickness **16**D**3** of the gate insulating layer. The thickness **16**D**4** of the gate insulating layer is preferably 90% or greater and 99.5% or smaller of the thickness **16**D**2** of the gate insulating layer and 90% or greater and 99.5% or smaller of the thickness **16**D**3** of the gate insulating layer.

[0171] The thickness **16**D**11** of the gate insulating layer is, for example, 40% or greater and 99.8% or smaller of the thickness **16**D**4** of the gate insulating layer and the thickness **16**D**12** of the gate insulating layer is 40% or greater and 99.8% or smaller of the thickness **16**D**4** of the gate insulating layer. The thickness **16**D**11** of the gate insulating layer is preferably 90% or greater and 99.5% or smaller of the thickness **16**D**4** of the gate insulating layer and the thickness **16**D**12** of the gate insulating layer is preferably 90% or greater and 99.5% or smaller of the thickness **16**D**4** of the gate insulating layer.

Production Method

[0172] An exemplary method for producing the TFT substrate **10** of the present embodiment is described with reference to FIG. **34**. FIG. **34** includes schematic cross-sectional views of the regions shown in FIG. **32**, each showing a state where an insulating film is patterned in fourth patterning in production of the TFT substrate of Embodiment 3.

<Production of TFT Substrate>

[0173] The production of a TFT substrate of the present embodiment is the same as the production of a TFT substrate of Embodiment 2 except that, in the fourth patterning, as shown in FIG. **34**, the contact holes **38***s* and **38***d* are formed and the etching stopper layer **40** is formed by etching the insulating film in the region between the source electrode **24***sd* and the drain electrode **24***dd*.

[0174] Here, a comparative embodiment is given in order to describe the difference from the present embodiment. FIG. **35** is a schematic plan view showing the structures of one pixel and ends of lines on a TFT substrate of Comparative Embodiment 2. FIG. **36** includes schematic cross-sectional views taken along the line A**9**-A**10** and the line B**9**-B**10** in FIG. **35**. FIG. **36** shows, from left, a schematic cross-sectional view taken along the line A**9**-A**10** in FIG. **35** and a schematic cross-sectional view taken along the line B**9**-B**10** in FIG. **35**.

[0175] The TFT substrate of the present embodiment is a bottom-contact substrate, while the TFT substrate of Comparative Embodiment 2 is a top-contact substrate as shown in FIG. **35** and FIG. **36**. The TFT substrate of Comparative Embodiment 2 has the same structure as that of the TFT substrate **10** of the present embodiment except for the positions of the oxide semiconductor layer **18***sl* and the etching stopper layer **40** and the structures of the source electrode **24***sdr* and the drain electrode **24***ddr*. The oxide semiconductor layer **18***sl* of the TFT substrate of Comparative Embodiment 2 is disposed between the gate insulating layer **16** and the source electrodes **24***sdr* and between the gate insulating layer **16** and the drain electrodes **24***ddr*. The etching stopper layer **40** is disposed between the oxide semiconductor layer **18***sl* and the source electrode **24***sdr* and between the oxide semiconductor layer **18***sl* and the drain electrode **24***ddr*.

[0176] The source electrode **24***sdr* and the drain electrode **24***ddr* of the TFT substrate of Comparative Embodiment 2 are each formed from the first conductive layer **24***d***1***r*. The first conductive layer **24***d***1***r* has a laminate structure including a lower layer **24***d***11***r*, a middle layer **24***d***12***r*, and an upper layer **24***d***13***r* stacked in the stated order from the insulating substrate **12** side. Specific examples of the structure of the first conductive layer **24***d***1***r* include a structure in which the lower layer **24***d***11***r* formed from titanium, the middle layer **24***d***12***r* formed from aluminum, and the upper layer **24***d***13***r* formed from titanium are stacked (hereinafter, also referred to as Specific Example 1 of Comparative Embodiment 2), and a structure in which the lower layer **24***d***11***r* formed from titanium, the middle layer **24***d***12***r* formed from aluminum or copper, and the upper layer **24***d***13***r* formed from molybdenum or molybdenum nitride are stacked (hereinafter, also referred to as Specific Example 2 of Comparative Embodiment 2).

[0177] FIG. **37** includes schematic cross-sectional views of the regions shown in FIG. **36**, each showing a production process of the TFT substrate of Specific Example 1 of Comparative Embodiment 2. In production of the TFT substrate of Comparative Embodiment 2, the gate lines **14***gl*,

the gate electrodes **14***gd*, and the gate terminals **14***gt* are formed, the gate insulating layer **16** is formed, the oxide semiconductor layer **18***sl* is formed, and then the etching stopper layer **40** is formed. Next, the first conductive film as a material of the first conductive layer **24***d***1***r* is formed and then etched to form the source electrodes **24***sdr* and the drain electrodes **24***dd*. In the case of Specific Example 1 of Comparative Embodiment 2, the first conductive film is etched by dry etching. Although the etching stopper layer **40** is disposed in Comparative Embodiment 2, the channel portion of each TFT may suffer plasma damage under some conditions for the dry etching. The TFT properties may be thereby degraded, and thus the threshold value may be significantly reduced to have a negative value. As a result, the TFT may fail to function as a switching element. Such a phenomenon may be caused when the electric power is set at a high level and thereby the rate of the dry etching is increased in order to improve the productivity. In the case of Specific Example 2 of Comparative Embodiment 2, a molybdenum film or a molybdenum nitride film (corresponding to the upper layer **24***d***13***r*) and an aluminum film or a copper film (corresponding to the middle layer **24***d***12***r*) of the first conductive film are etched by wet etching using a mixed acid solution containing phosphoric acid, acetic acid, and nitric acid. Then, a titanium film (corresponding to the lower layer **24***d***11***r*) is etched by dry etching. Here, similarly to Specific Example 1 of Comparative Embodiment 2, the channel portion of each TFT may suffer plasma damage under some conditions for the dry etching. The TFT properties may be thereby degraded and the threshold value may be significantly reduced to have a negative value. As a result, the TFT may fail to function as a switching element.

[0178] In contrast, in the method for producing the TFT substrate **10** of the present embodiment, as mentioned above, the surface of the gate insulating layer **16** in the TFT channel portion can be modified while preventing the channel side end of each source electrode **24***sd* and the channel side end of each drain electrode **24***dd* from being etched. As a result, the threshold value among the TFT properties can be stable to prevent malfunction of the switching element.

Embodiment 4

[0179] In the present embodiment, the characteristic features of the present embodiment are mainly described and the same points as in Embodiment 1, 2, or 3 are not described. The components having the same or a similar function have the same reference numerals in both the present embodiment and Embodiment 1, 2, or 3, and such components are not described in the present embodiment. The present embodiment is substantially the same as Embodiments 2 and 3 except that the etching stopper layer has a different shape, as described below.

<Structure of TFT Substrate **10**>

[0180] FIG. **38** and FIG. **39** show schematic structure views of the TFT substrate **10** of the present embodiment. FIG. **38** is a schematic plan view showing the structures of one pixel and ends of lines on the TFT substrate of Embodiment 3. FIG. **39** includes schematic cross-sectional views taken along the line A**11**-A**12** and the line B**11**-B**12** in FIG. **38**. FIG. **39** shows, from left, a schematic cross-sectional view taken along the line A**11**-A**12** in FIG. **38** and a schematic cross-sectional view taken along the line B**11**-B**12** in FIG. **38**.

[0181] In this embodiment, the TFT substrate **10** has the same planar layout as of the TFT substrate **10** of Embodiment 3 except that, as shown in FIG. **38**, the contact hole **38***s* overlaps an end of the source electrode **24***sd* but does not overlap the gate insulating layer **16**, and the contact hole **38***d* overlaps an end of the drain electrode **24***dd* but does not overlap the gate insulating layer **16**.

[0182] In the TFT substrate **10**, as shown in FIG. **39**, the etching stopper layer **40** is present between the oxide semiconductor layer **18***sl* and the gate insulating layer **16**, and the oxide semiconductor layer **18***sl* is connected to the source electrode **24***sd* through the contact hole **38***s* in the etching stopper layer **40** and connected to the drain electrode **24***dd* through the contact hole **38***d* in the etching stopper layer **40**. The source electrode **24***sd* and the drain electrode **24***dd* are connected to the oxide semiconductor layer **18***sl* through the contact holes **38***s* and **38***d* in the etching stopper layer **40**. Differently from the above Embodiment 3 where the contact holes **38***s* and **38***d* overlap the gate insulating layer **16**, in the present embodiment, the contact hole **38***s* overlaps an end of the source electrode **24***sd* but does not overlap the gate insulating layer **16**, while the contact hole **38***d* overlaps the drain electrode **24***dd* but does not overlap the gate insulating layer **16**.

[0183] FIG. **40**A is a schematic cross-sectional view of the region R**7** surrounded by a broken line in FIG. **39**. FIG. **40**B is a schematic cross-sectional view of the region R**8** surrounded by a broken line in FIG. **39**. The source electrode **24***sd* and the drain electrode **24***dd* each include the first conductive layer **24***d***1** and the second conductive layer **24***d***2** covering the first conductive layer **24***d***1** . The second conductive layer **24***d***2** contains at least one element selected from the group consisting of molybdenum, tantalum, tungsten, and nickel. The gate insulating layer **16** may be contaminated in formation of the source electrode **24***sd* and the drain electrode **24***dd*, for example. In this case, the threshold value among the TFT properties is unstable to possibly cause reduced on-state current. In production of the TFT substrate **10** of the present embodiment, in order to remove contaminants on the gate insulating layer **16**, for example, the surface of the gate insulating layer **16** in the region between the source electrode **24***sd* and the drain electrode **24***dd* is removed (modified) by etching with hydrofluoric acid and then disposing the oxide semiconductor layer **18***sl*. This can stabilize the threshold value among the TFT properties and prevent or reduce a reduction in on-state current to achieve stable TFT properties.

[0184] Here, the TFT substrate **10** of the present embodiment includes the etching stopper layer **40** that can prevent the source electrode **24***sd* and the drain electrode **24***dd* from being etched in formation of the oxide semiconductor layer **18***sl*, as mentioned above. The etching stopper layer **40** is disposed on the source electrode **24***sd* and on the drain electrode **24***dd*, and is also disposed between the gate insulating layer **16** and the oxide semiconductor layer **18***sl* in a region between the source electrode **24***sd* and the drain electrode **24***dd*. The surface of the etching stopper layer **40** may be contaminated in the formation of the etching stopper layer **40**, for example. When the oxide semiconductor layer **18***sl* is formed on the contaminated etching stopper layer **40**, the threshold value among the TFT properties may be unstable to possibly cause reduced on-state current. In production of the TFT substrate **10** of the present embodiment, in order to remove contaminants on the surface of the

etching stopper layer **40**, for example, after formation of the etching stopper layer **40**, the surface of the etching stopper layer **40** is removed (modified) by etching with hydrofluoric acid and then disposing the oxide semiconductor layer **18***sl*. Thereby, the TFT properties can be stabilized to a similar extent to the case without the etching stopper layer **40**.

[0185] In the TFT substrate **10** of the present embodiment, the second conductive layer **24***d***2** contains at least one element selected from the group consisting of molybdenum, tantalum, tungsten, and nickel. When the conductive layer contains at least one element selected from the group consisting of molybdenum, tantalum, tungsten, and nickel, the conductive layer has hydrofluoric acid resistance and thus can prevent the source electrode **24***sd* and the drain electrode **24***dd* from being etched during the etching with hydrofluoric acid. This can achieve less variation in channel length of the TFT **26** in the substrate plane, and thereby can achieve less variation in carrier mobility and threshold value among the TFT properties. As a result, the TFT properties can further be stabilized.

[0186] When the surface of the gate insulating layer **16** in the region between the source electrode **24***sd* and the drain electrode **24***dd* is etched with hydrofluoric acid before disposing the oxide semiconductor layer **18***sl* as mentioned above, the gate insulating layer **16** in the region between the source electrode **24***sd* and the drain electrode **24***dd* is etched while the gate insulating layer **16** in the regions below the source electrode **24***sd* and the drain electrode **24***dd* is not etched. As a result, as shown in FIG. **40**A and FIG. **40**B, the thickness **16**D**4** of the gate insulating layer **16** in a region between the source electrode **24***sd* and the drain electrode **24***dd* and below the etching stopper layer **40** is smaller than the thickness **16**D**2** of the gate insulating layer **16** in the region below the source electrode **24***sd* and is also smaller than the thickness **16**D**3** of the gate insulating layer **16** in the region below the drain electrode **24***dd*.

[0187] The thickness **16**D**4** of the gate insulating layer is, for example, 40% or greater and 99.8% or smaller of the thickness **16**D**2** of the gate insulating layer and 40% or greater and 99.8% or smaller of the thickness **16**D**3** of the gate insulating layer. The thickness **16**D**4** of the gate insulating layer is preferably 90% or greater and 99.5% or smaller of the thickness **16**D**2** of the gate insulating layer and 90% or greater and 99.5% or smaller of the thickness **16**D**3** of the gate insulating layer.

Production Method

[0188] An exemplary method for producing the TFT substrate **10** of the present embodiment is described with reference to FIG. **41**. FIG. **41** includes schematic cross-sectional views of the regions shown in FIG. **39**, each showing a state where an insulating film is patterned in fourth patterning in production of the TFT substrate of Embodiment 4.

<Production of TFT Substrate>

[0189] The production of a TFT substrate of the present embodiment is the same as the production of a TFT substrate of Embodiment 3 except that, as shown in FIG. **41**, the insulating film is etched to form the etching stopper layer **40** such that the etching stopper layer **40** has the contact hole **38***s* that overlaps an end of the source electrode **24***sd* but does not overlap the gate insulating layer **16**, and the contact hole **38***d* that overlaps an end of the drain electrode **24***dd* but does not overlap the gate insulating layer **16**. As described, in the present embodiment, the gate insulating layer **16** in the region between the source electrode **24***sd* and the drain electrode **24***dd* is covered with the etching stopper layer **40**. Thus, in the second hydrofluoric acid treatment in the present embodiment, the outermost surface of the etching stopper layer is removed by the hydrofluoric acid treatment.

Modified Example of Embodiments 1 to 4

[0190] The present invention is not limited by the above embodiments each giving an example where the TFT substrate **10** constitutes the transmissive liquid crystal display device S. The TFT substrate **10** of the present invention may be applied to other types of display devices such as reflective liquid crystal display devices, transflective liquid crystal display devices, and organic electroluminescent (EL) display devices, and methods for producing these devices.

[0191] The above embodiments of the present invention may appropriately be combined with each other within the spirit of the present invention.

What is claimed is:

1. A thin-film transistor substrate comprising a base substrate and a thin-film transistor,

the thin-film transistor including:

a gate electrode disposed on the base substrate;

a gate insulating layer covering the gate electrode;

a source electrode and a drain electrode facing each other and disposed above the gate electrode via the gate insulating layer; and

an oxide semiconductor layer which faces the gate electrode via at least the gate insulating layer and whose first end and second end respectively overlap the source electrode and the drain electrode and are thereby respectively connected to the source electrode and the drain electrode,

the source electrode and the drain electrode each including a first conductive layer and a second conductive layer covering the first conductive layer,

the second conductive layer containing at least one element selected from the group consisting of molybdenum, tantalum, tungsten, and nickel,

the gate insulating layer in a region between the source electrode and the drain electrode having a smaller thickness than in a region below the source electrode and in a region below the drain electrode.

2. The thin-film transistor substrate according to claim **1**,

wherein the thin-film transistor includes no etching stopper layer on the source electrode and on the drain electrode, and

the oxide semiconductor layer faces the gate electrode via the gate insulating layer.

3. The thin-film transistor substrate according to claim **1**,

wherein the thin-film transistor further includes an etching stopper layer on the source electrode and on the drain electrode,

the thin-film transistor substrate further comprises a protective insulating layer covering the thin-film transistor and a conductive layer disposed on the protective insulating layer and connected to the drain electrode via a first contact hole in the etching stopper layer and in the protective insulating layer,

the etching stopper layer covers the source electrode except for a connection portion between the oxide semiconductor layer and the source electrode and covers the drain electrode except for a connection portion between the oxide semiconductor layer and the drain electrode and a connection portion between the conductive layer and the drain electrode, and

the connection portion between the oxide semiconductor layer and the source electrode and the connection portion between the oxide semiconductor layer and the drain electrode are located in a region with the gate electrode.

4. The thin-film transistor substrate according to claim **3**, wherein the etching stopper layer is not present in a region between the oxide semiconductor layer and the gate insulating layer, and

the oxide semiconductor layer faces the gate electrode via the gate insulating layer.

5. The thin-film transistor substrate according to claim **3**, wherein the etching stopper layer is present in a region between the oxide semiconductor layer and the gate insulating layer, and

the oxide semiconductor layer is connected to the source electrode via a second contact hole in the etching stopper layer and connected to the drain electrode via a third contact hole in the etching stopper layer.

6. The thin-film transistor substrate according to claim **5**, wherein the second contact hole overlaps an end of the source electrode and the gate insulating layer in a part adjacent to the end of the source electrode,

the third contact hole overlaps an end of the drain electrode and the gate insulating layer in a part adjacent to the end of the drain electrode, and

the gate insulating layer in a region between the source electrode and the drain electrode and below the etching stopper layer has a greater thickness than in a region below the second contact hole and in a region below the third contact hole.

7. The thin-film transistor substrate according to claim **5**, wherein the second contact hole overlaps an end of the source electrode but does not overlap the gate insulating layer,

the third contact hole overlaps an end of the drain electrode but does not overlap the gate insulating layer, and

the gate insulating layer in a region between the source electrode and the drain electrode and below the etching stopper layer has a smaller thickness than in a region below the source electrode and in a region below the drain electrode.

8. The thin-film transistor substrate according to claim **1**, wherein the first conductive layer is a laminate including a lower layer, a middle layer, and an upper layer stacked in the stated order from a base substrate side,

the middle layer contains aluminum or copper, and

the lower layer and the upper layer each contain titanium or molybdenum nitride.

9. The thin-film transistor substrate according to claim **1**, wherein the second conductive layer contains at least one substance selected from the group consisting of molybdenum, molybdenum nitride, a molybdenum alloy, a nitride of the molybdenum alloy, tantalum, tantalum nitride, a tantalum alloy, a nitride of the tantalum alloy, tungsten, tungsten nitride, a tungsten alloy, a nitride of the tungsten alloy, nickel, nickel nitride, a nickel alloy, and a nitride of the nickel alloy.

10. The thin-film transistor substrate according to claim **1**, wherein the oxide semiconductor layer includes an indium gallium zinc oxide-based oxide semiconductor.

11. A liquid crystal display device comprising:

the thin-film transistor substrate according to claim **1**;

a counter substrate facing the thin-film transistor substrate; and

a liquid crystal layer disposed between the thin-film transistor substrate and the counter substrate.

12. A method for producing a thin-film transistor substrate, comprising in the following order:

first patterning including forming a gate electrode conductive film on a base substrate and patterning the gate electrode conductive film using a first photomask to form a gate electrode;

formation of a gate insulating layer including forming a gate insulating layer so as to cover the gate electrode;

second patterning including forming a first conductive film so as to cover the gate insulating layer and patterning the first conductive film using a second photomask;

third patterning including forming a second conductive film containing at least one element selected from the group consisting of molybdenum, tantalum, tungsten, and nickel and patterning the second conductive film using a third photomask to form a source electrode and a drain electrode;

hydrofluoric acid treatment including treating a gate insulating layer side surface of the base substrate with hydrofluoric acid; and

fourth patterning including forming an oxide semiconductor film so as to cover the source electrode and the drain electrode and patterning the oxide semiconductor film using a fourth photomask to form an oxide semiconductor layer.

13. The method for producing a thin-film transistor substrate according to claim **12**, further comprising, between the hydrofluoric acid treatment and the fourth patterning, fifth patterning including forming an insulating film so as to cover the source electrode and the drain electrode and patterning the insulating film using a fifth photomask to form an etching stopper layer.

14. The method for producing a thin-film transistor substrate according to claim **13**, further comprising, between the fifth patterning and the fourth patterning, second hydrofluoric acid treatment including treating the gate insulating layer side surface of the base substrate with hydrofluoric acid.

15. The method for producing a thin-film transistor substrate according to claim **12**,

wherein the second conductive film is a conductive film containing at least one substance selected from the group consisting of molybdenum, molybdenum nitride, a molybdenum alloy, a nitride of the molybdenum alloy, tantalum, tantalum nitride, a tantalum alloy, a nitride of the tantalum alloy, tungsten, tungsten nitride, a tungsten alloy, a nitride of the tungsten alloy, nickel, nickel nitride, a nickel alloy, and a nitride of the nickel alloy.

16. The method for producing a thin-film transistor substrate according to claim **12**,

wherein the oxide semiconductor film is an indium gallium zinc oxide-based oxide semiconductor.

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