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(12) **United States Patent**
Sumasu

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(54) **MOTOR CONTROL DEVICE**

(71) Applicant: **JTEKT CORPORATION**, Osaka-shi, Osaka (JP)

(72) Inventor: **Hiroshi Sumasu**, Kashihara (JP)

(73) Assignee: **JTEKT CORPORATION**, Osaka-shi (JP)

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(30) **Foreign Application Priority Data**

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(51) **Int. Cl.**

H03K 5/00	(2006.01)
H02P 27/08	(2006.01)
H02M 7/5387	(2007.01)
H02P 21/22	(2016.01)
H02M 1/44	(2007.01)
B62D 5/04	(2006.01)
H02P 21/00	(2016.01)

(52) **U.S. Cl.**

CPC ***H02P 27/08*** (2013.01); ***B62D 5/04*** (2013.01); ***H02M 1/44*** (2013.01); ***H02M 7/53871*** (2013.01); ***H02P 21/00*** (2013.01); ***H02P 21/22*** (2016.02); *B62D 5/0409* (2013.01); *B62D 5/0463* (2013.01); *H02P 21/0003* (2013.01)

(58) **Field of Classification Search**

CPC H02P 27/08; H02P 6/10; H02P 7/29; H02P 29/50; H02M 1/12; H02M 2001/0009

See application file for complete search history.

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Primary Examiner — Karen Masih

(74) *Attorney, Agent, or Firm* — Oliff PLC

(57) **ABSTRACT**

An electric motor that is controlled by a motor control device has two-system multi-phase motor coils. The motor control device includes a common mode noise reduction unit that changes a PWM count in a PWM cycle for at least one phase in one of two systems such that a current that flows through a stray capacitance because of an output voltage for one phase in the other system is canceled out with a current that flows through the stray capacitance because of an output voltage for the at least one phase in the one system in at least one PWM cycle in a current control cycle.

3 Claims, 16 Drawing Sheets

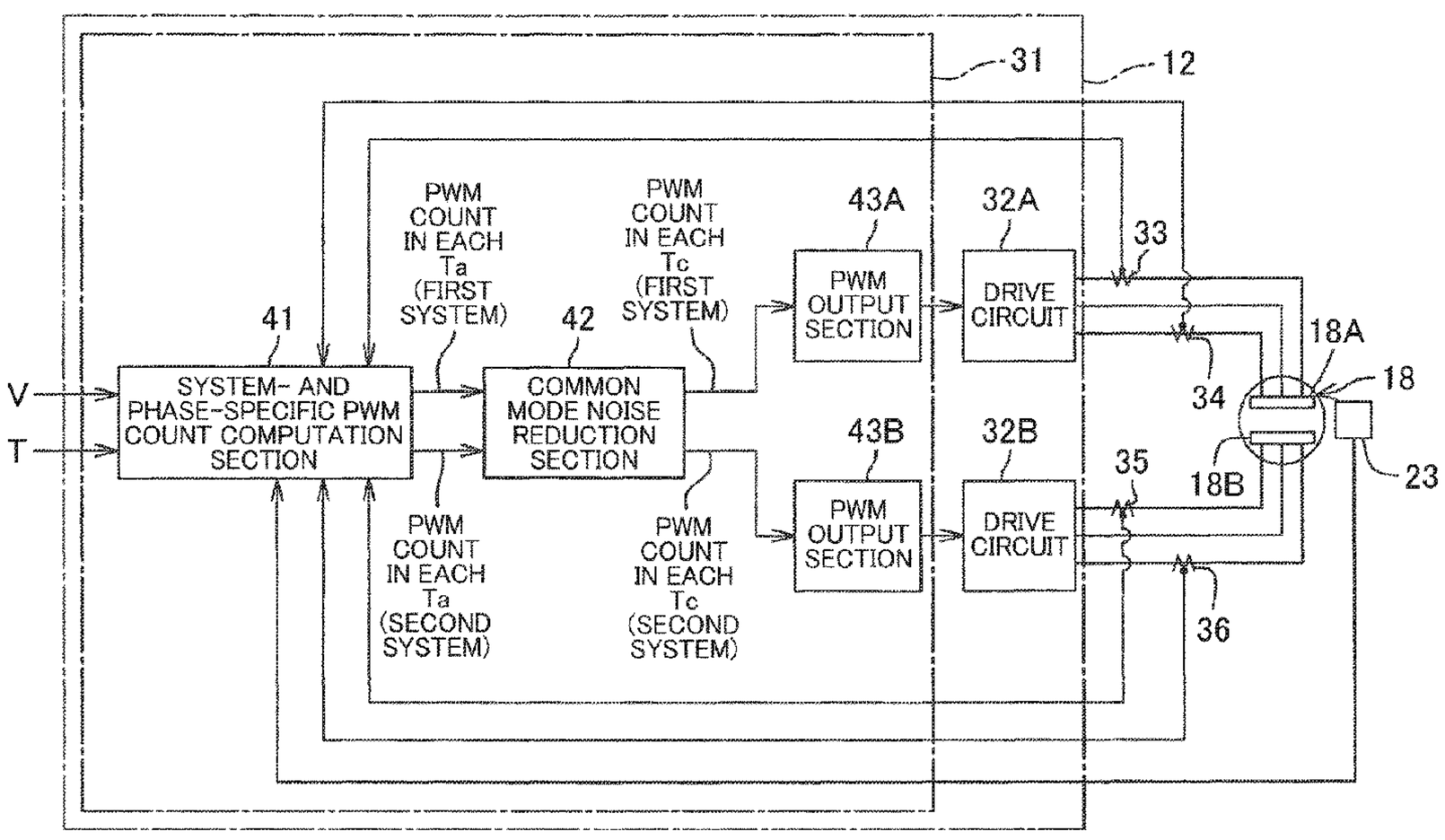


FIG. 1

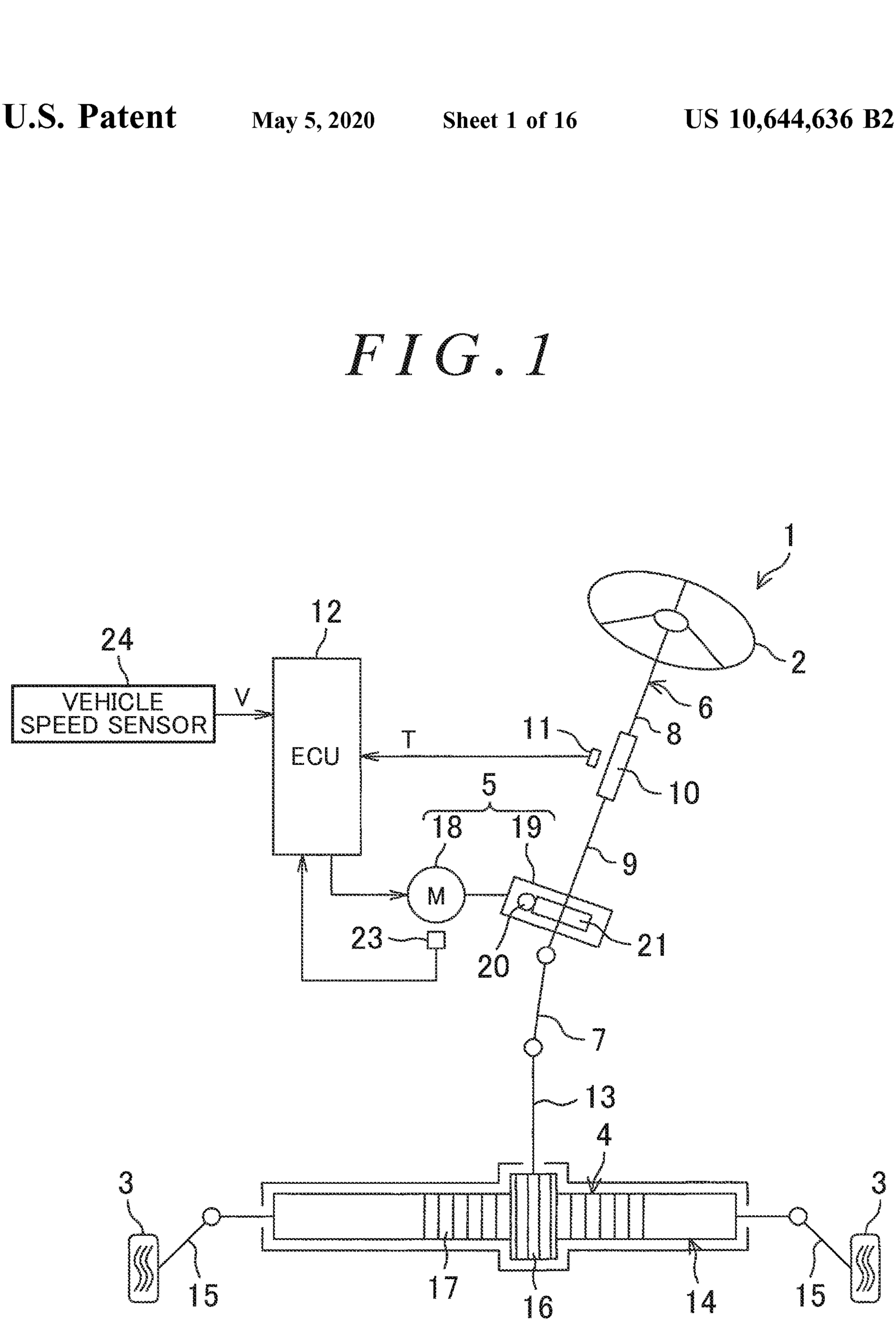
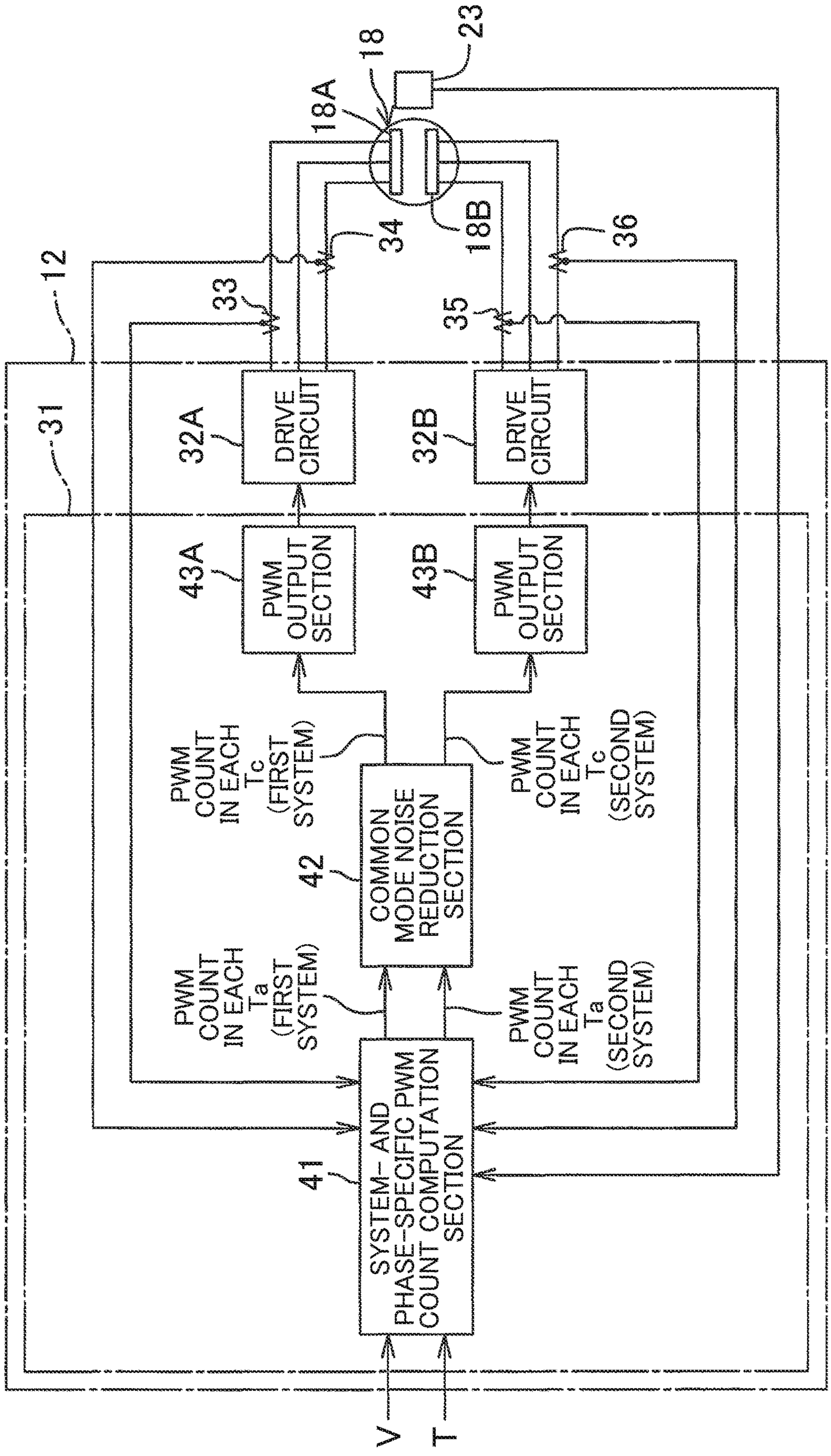

1
2
6
8
11
10
5
18
19
9
M
23
20
21
7
13
4
3
15
17
16
14
3
15
12
24
VEHICLE SPEED SENSOR
V
ECU
T

FIG. 2


12
31
33
34
35
36
18
18A
18B
23
32A
DRIVE CIRCUIT
32B
DRIVE CIRCUIT
43A
PWM OUTPUT SECTION
43B
PWM OUTPUT SECTION
PWM COUNT IN EACH Tc (FIRST SYSTEM)
PWM COUNT IN EACH Tc (SECOND SYSTEM)
42
COMMON MODE NOISE REDUCTION SECTION
PWM COUNT IN EACH Ta (FIRST SYSTEM)
PWM COUNT IN EACH Ta (SECOND SYSTEM)
41
SYSTEM- AND PHASE-SPECIFIC PWM COUNT COMPUTATION SECTION
V
T

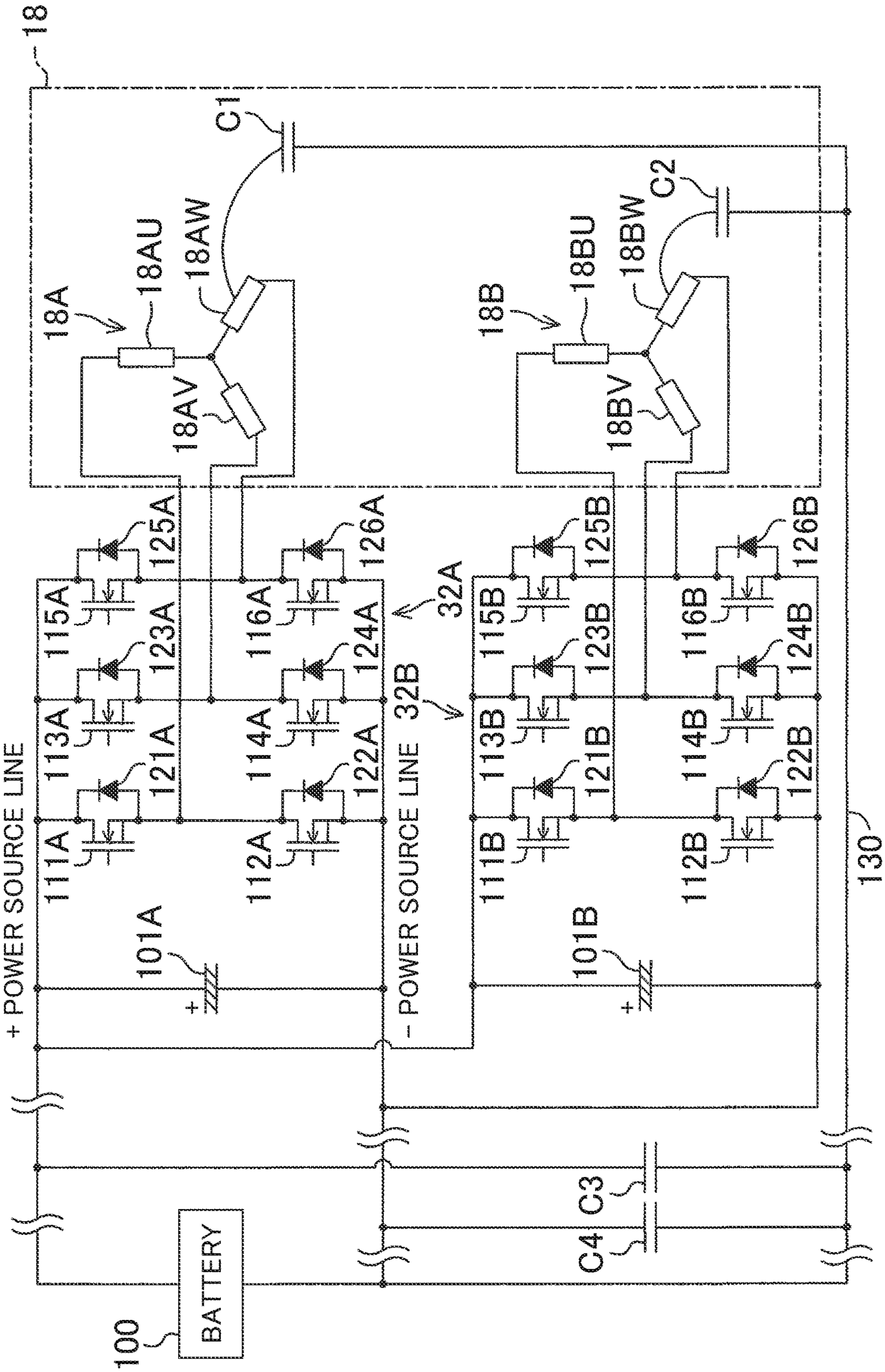

18
C1
C2
18A
18AU
18AV
18AW
18B
18BU
18BV
18BW
111A
112A
113A
114A
115A
116A
121A
122A
123A
124A
125A
126A
111B
112B
113B
114B
115B
116B
121B
122B
123B
124B
125B
126B
32A
32B
101A
101B
+ POWER SOURCE LINE
– POWER SOURCE LINE
130
C3
C4
100
BATTERY

FIG. 3

FIG. 4

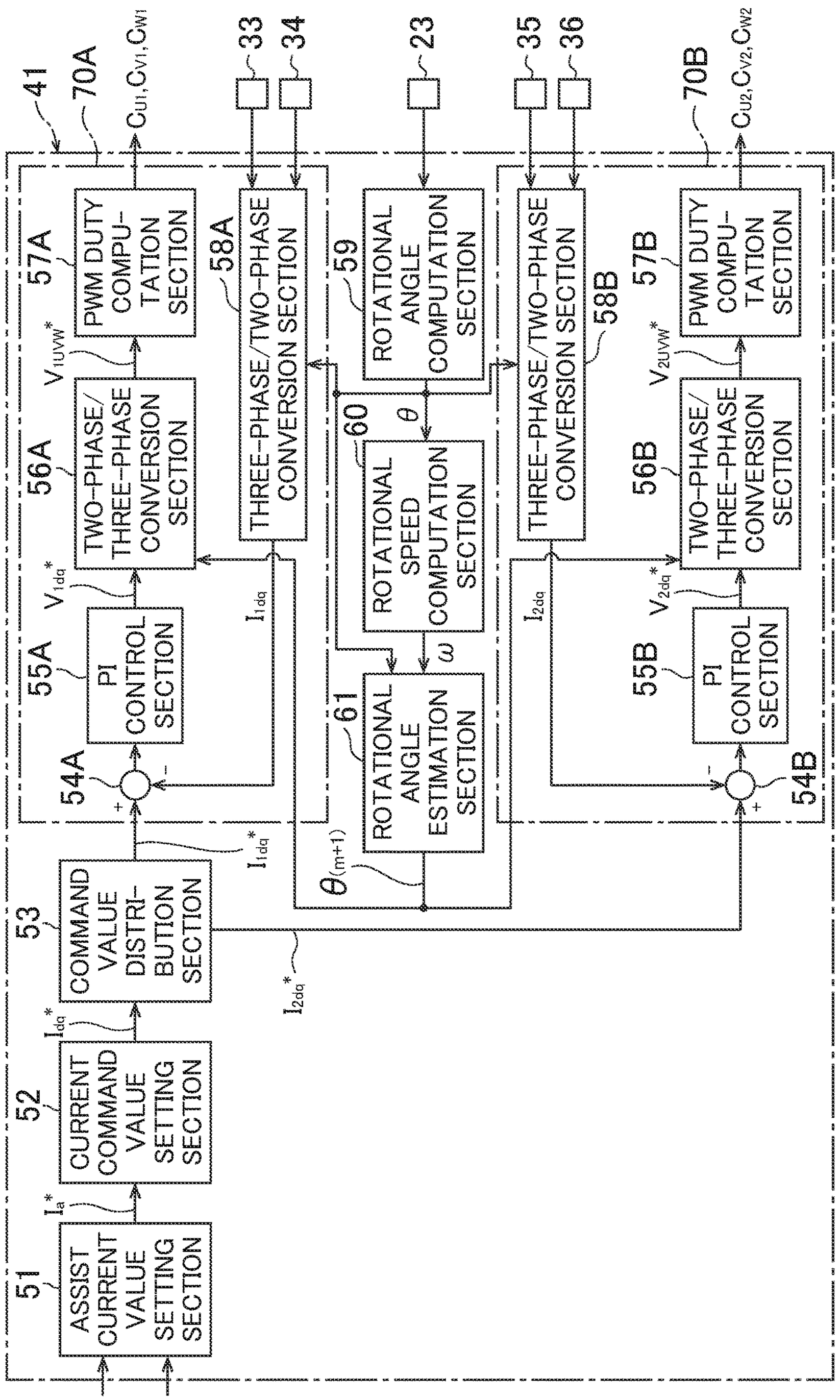

41
70A
C_{U1}, C_{V1}, C_{W1}
33
34
23
35
36
70B
C_{U2}, C_{V2}, C_{W2}
57A
PWM DUTY COMPU-TATION SECTION
58A
THREE-PHASE/TWO-PHASE CONVERSION SECTION
59
ROTATIONAL ANGLE COMPUTATION SECTION
58B
57B
PWM DUTY COMPU-TATION SECTION
V_{1UVW}^*
56A
TWO-PHASE/THREE-PHASE CONVERSION SECTION
V_{1dq}^*
55A
PI CONTROL SECTION
I_{1dq}
60
ROTATIONAL SPEED COMPUTATION SECTION
θ
ω
61
ROTATIONAL ANGLE ESTIMATION SECTION
$\theta_{(m+1)}$
54A
I_{1dq}^*
53
COMMAND VALUE DISTRI-BUTION SECTION
I_{2dq}^*
I_{2dq}
V_{2UVW}^*
56B
TWO-PHASE/THREE-PHASE CONVERSION SECTION
V_{2dq}^*
55B
PI CONTROL SECTION
54B
I_{dq}^*
52
CURRENT COMMAND VALUE SETTING SECTION
I_a^*
51
ASSIST CURRENT VALUE SETTING SECTION
V
T

FIG. 5A

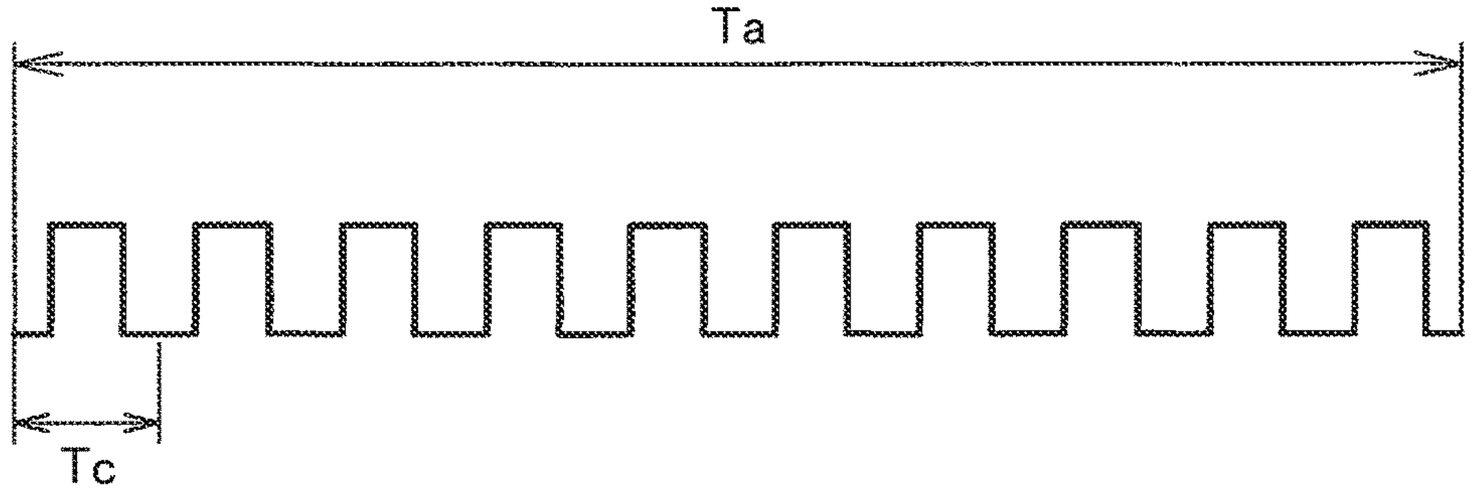


FIG. 5B

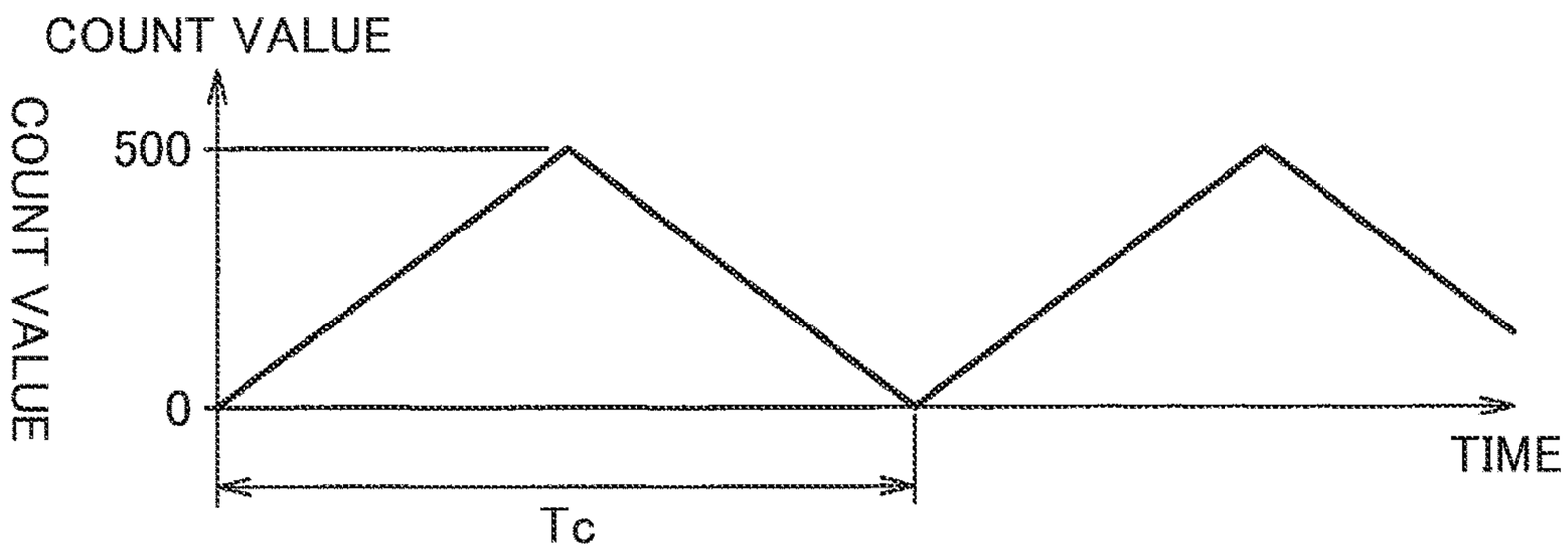


FIG. 5C

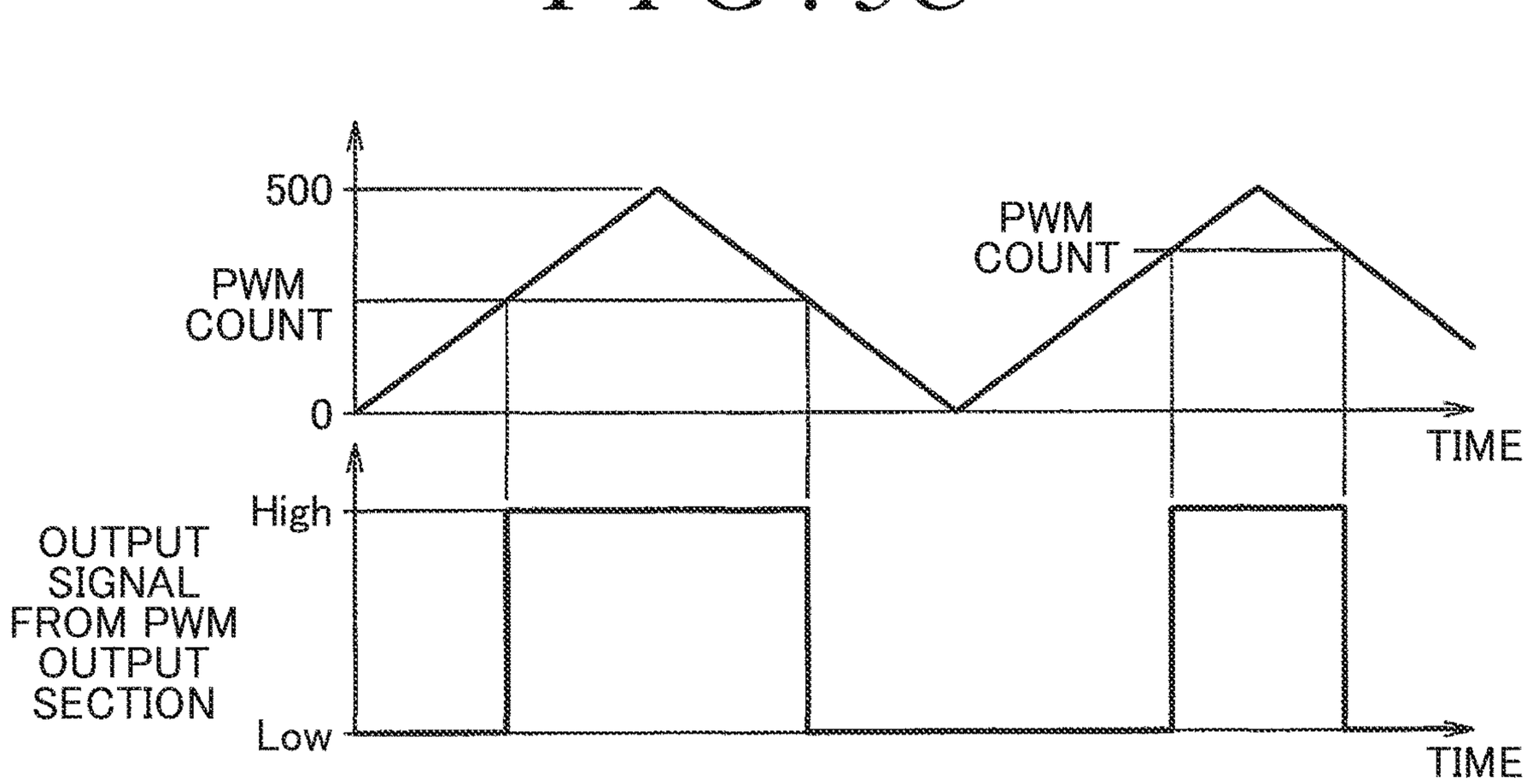
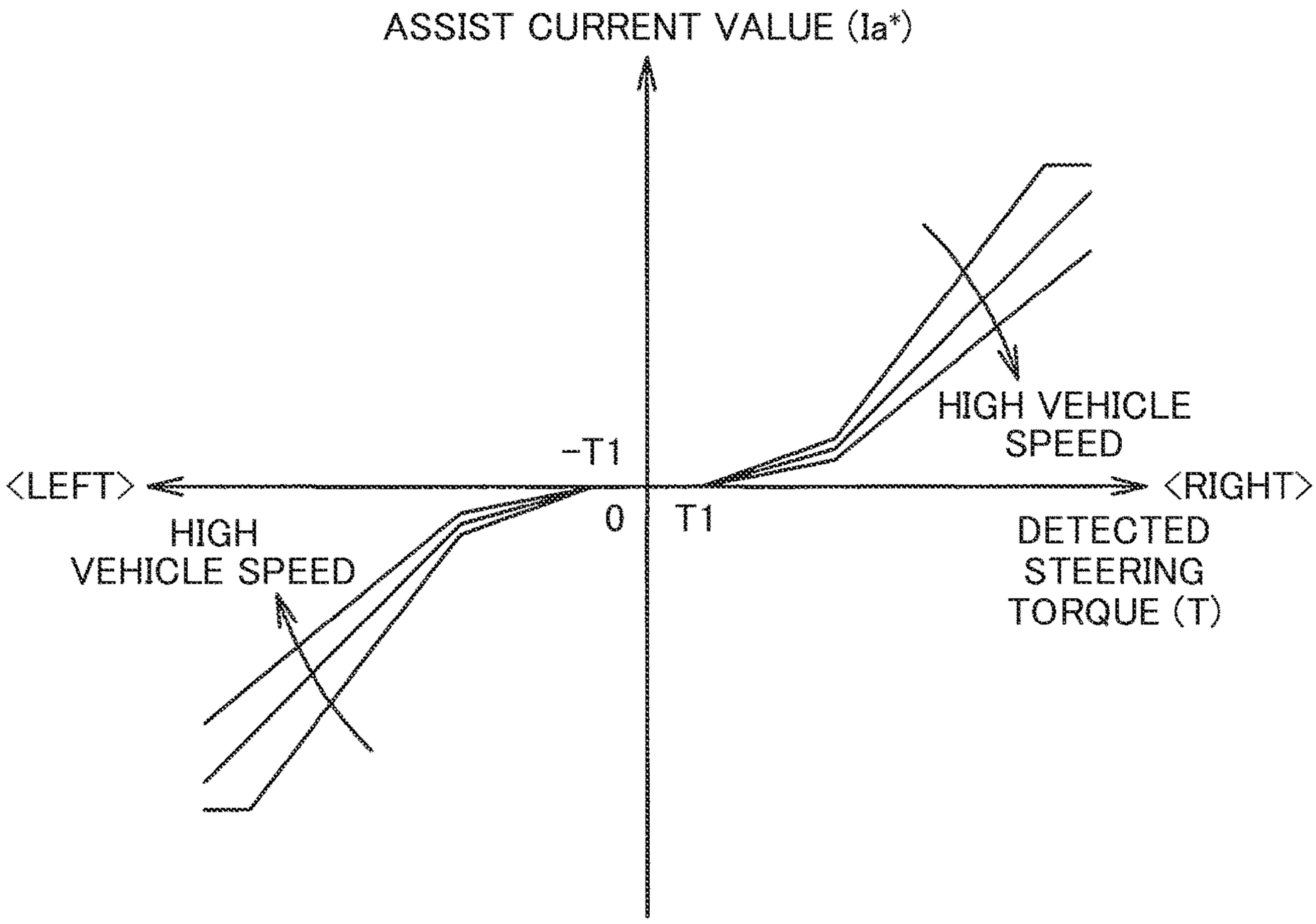


FIG. 6


ASSIST CURRENT VALUE (Ia*)
HIGH VEHICLE SPEED
-T1
<LEFT>
<RIGHT>
0
T1
HIGH VEHICLE SPEED
DETECTED STEERING TORQUE (T)

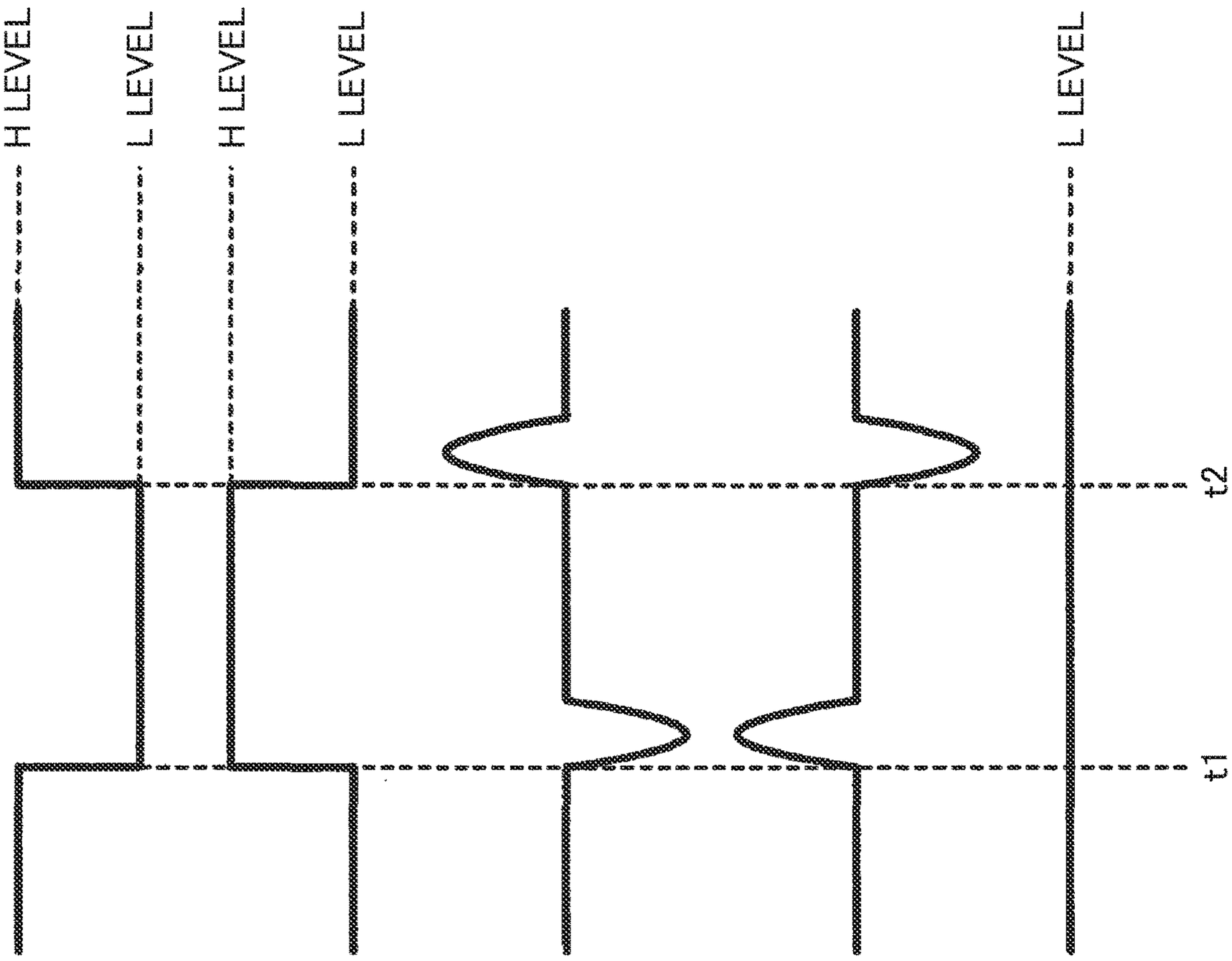


FIG. 7A OUTPUT VOLTAGE (PHASE VOLTAGE) FOR CERTAIN PHASE IN FIRST SYSTEM

FIG. 7B OUTPUT VOLTAGE (PHASE VOLTAGE) FOR CERTAIN PHASE IN SECOND SYSTEM

FIG. 7C CURRENT THAT FLOWS THROUGH STRAY CAPACITANCE ON MOTOR SIDE BECAUSE OF PHASE VOLTAGE IN FIG. 7A

FIG. 7D CURRENT THAT FLOWS THROUGH STRAY CAPACITANCE ON MOTOR SIDE BECAUSE OF PHASE VOLTAGE IN FIG. 7B

FIG. 7E CURRENT THAT FLOWS THROUGH STRAY CAPACITANCES BETWEEN POSITIVE AND NEGATIVE POWER SOURCE LINES AND FRAME GROUND

FIG. 8

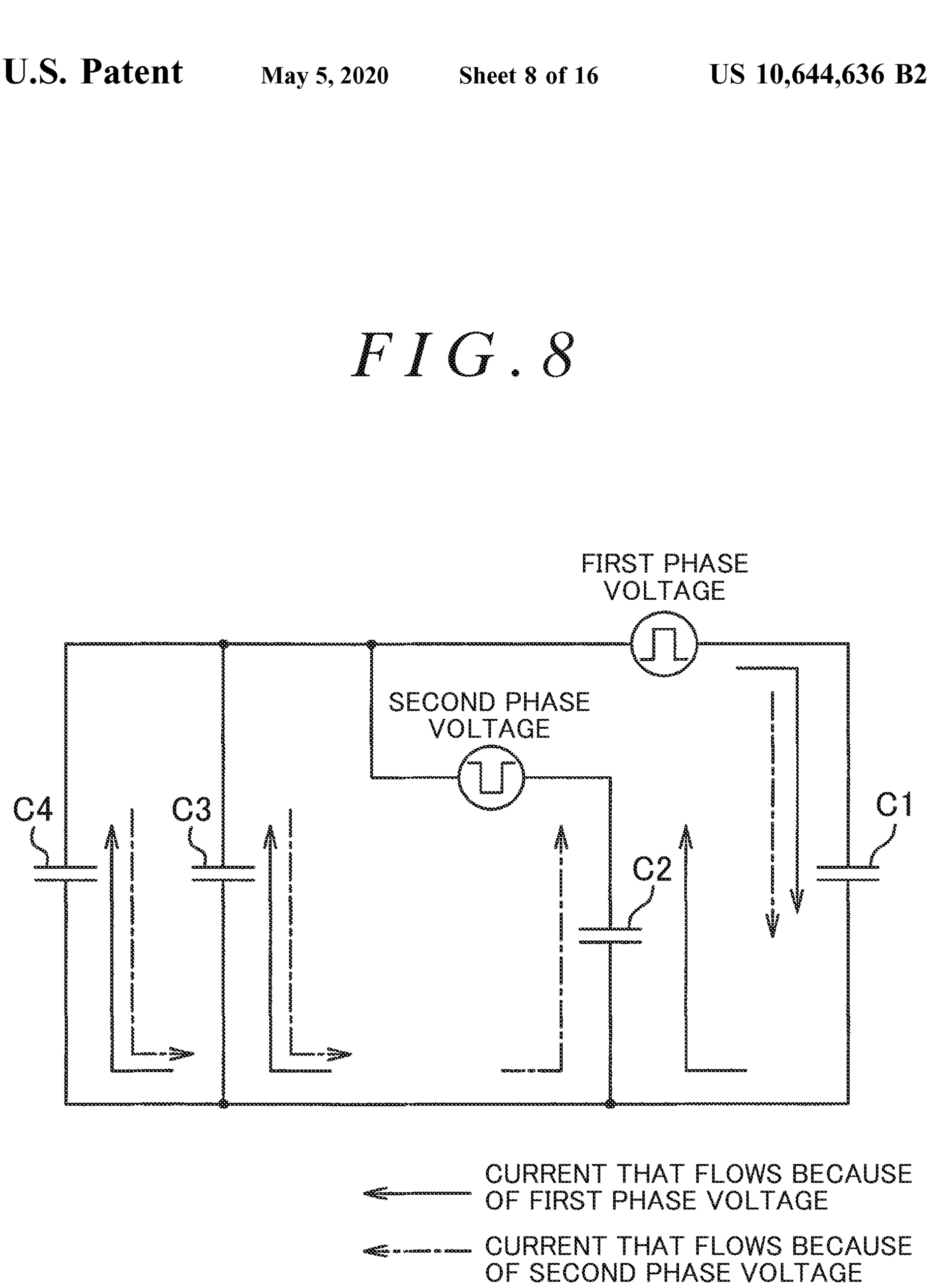
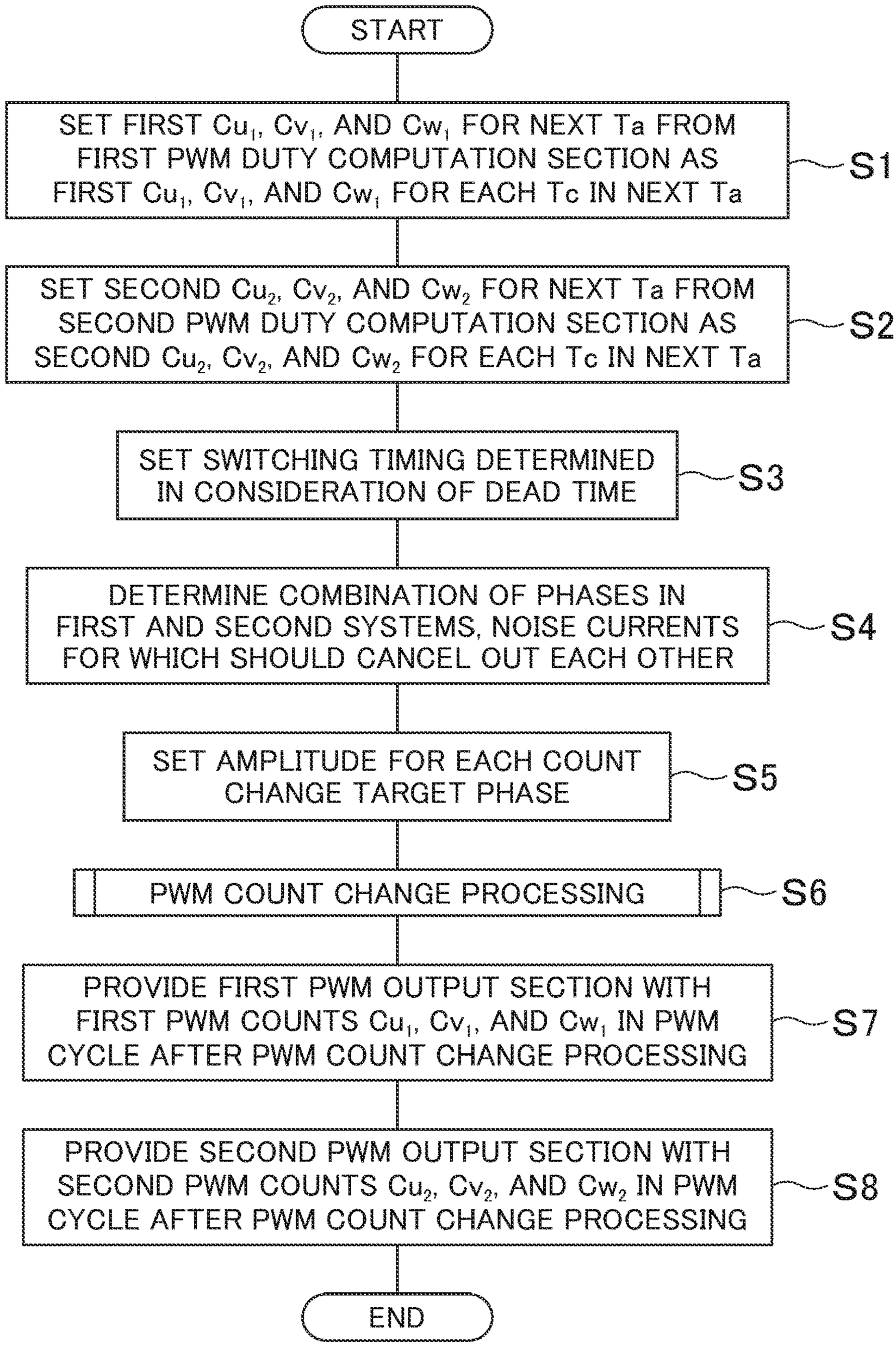

FIRST PHASE VOLTAGE
SECOND PHASE VOLTAGE
C4
C3
C2
C1
CURRENT THAT FLOWS BECAUSE OF FIRST PHASE VOLTAGE
CURRENT THAT FLOWS BECAUSE OF SECOND PHASE VOLTAGE

FIG. 9


START
SET FIRST Cu_1, Cv_1, AND Cw_1 FOR NEXT Ta FROM FIRST PWM DUTY COMPUTATION SECTION AS FIRST Cu_1, Cv_1, AND Cw_1 FOR EACH Tc IN NEXT Ta
S1
SET SECOND Cu_2, Cv_2, AND Cw_2 FOR NEXT Ta FROM SECOND PWM DUTY COMPUTATION SECTION AS SECOND Cu_2, Cv_2, AND Cw_2 FOR EACH Tc IN NEXT Ta
S2
SET SWITCHING TIMING DETERMINED IN CONSIDERATION OF DEAD TIME
S3
DETERMINE COMBINATION OF PHASES IN FIRST AND SECOND SYSTEMS, NOISE CURRENTS FOR WHICH SHOULD CANCEL OUT EACH OTHER
S4
SET AMPLITUDE FOR EACH COUNT CHANGE TARGET PHASE
S5
PWM COUNT CHANGE PROCESSING
S6
PROVIDE FIRST PWM OUTPUT SECTION WITH FIRST PWM COUNTS Cu_1, Cv_1, AND Cw_1 IN PWM CYCLE AFTER PWM COUNT CHANGE PROCESSING
S7
PROVIDE SECOND PWM OUTPUT SECTION WITH SECOND PWM COUNTS Cu_2, Cv_2, AND Cw_2 IN PWM CYCLE AFTER PWM COUNT CHANGE PROCESSING
S8
END

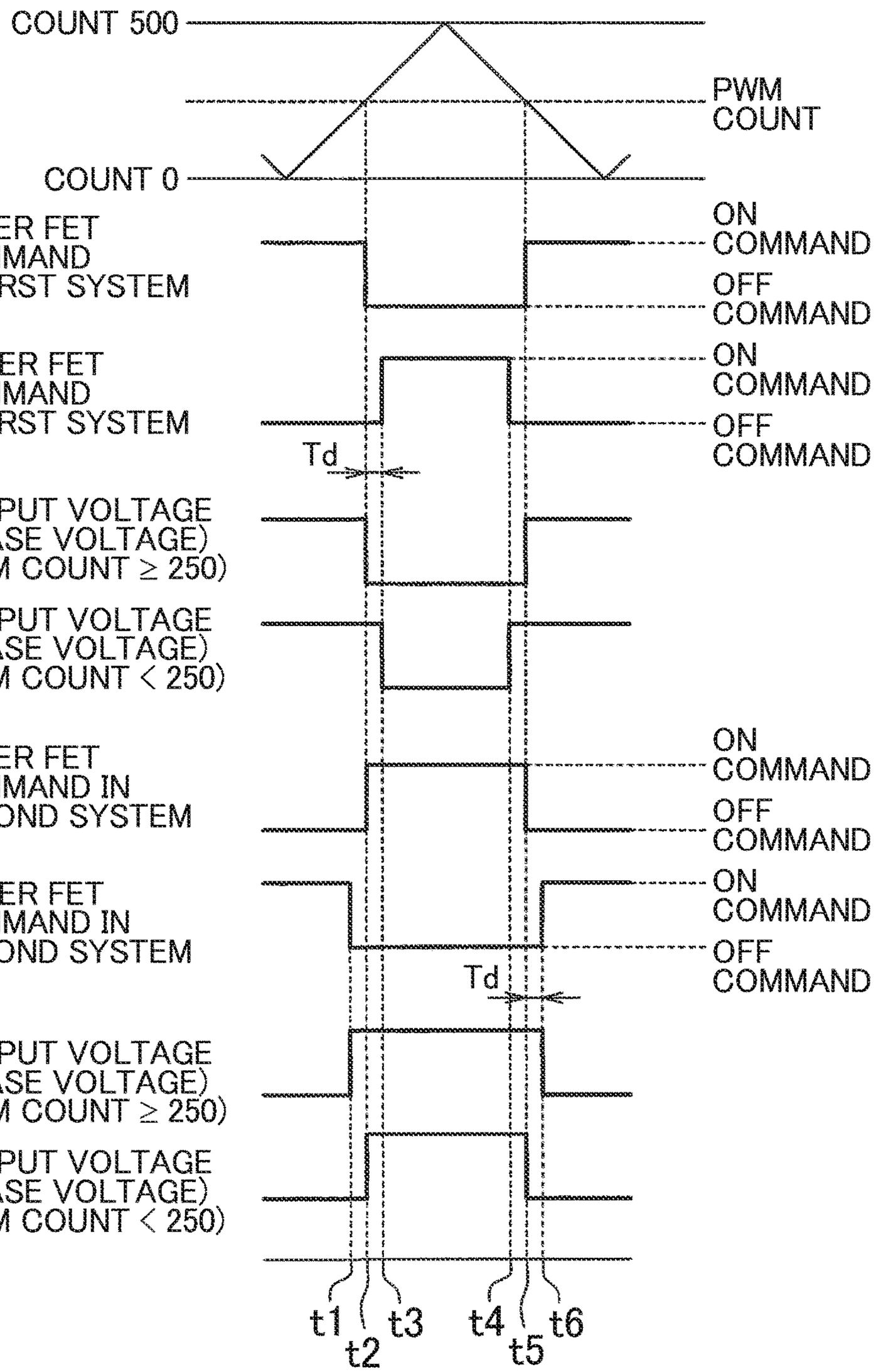


FIG. 10A UPPER FET COMMAND IN FIRST SYSTEM

FIG. 10B LOWER FET COMMAND IN FIRST SYSTEM

FIG. 10C OUTPUT VOLTAGE (PHASE VOLTAGE) (PWM COUNT ≥ 250)

FIG. 10D OUTPUT VOLTAGE (PHASE VOLTAGE) (PWM COUNT < 250)

FIG. 10E UPPER FET COMMAND IN SECOND SYSTEM

FIG. 10F LOWER FET COMMAND IN SECOND SYSTEM

FIG. 10G OUTPUT VOLTAGE (PHASE VOLTAGE) (PWM COUNT ≥ 250)

FIG. 10H OUTPUT VOLTAGE (PHASE VOLTAGE) (PWM COUNT < 250)

FIG. 11A

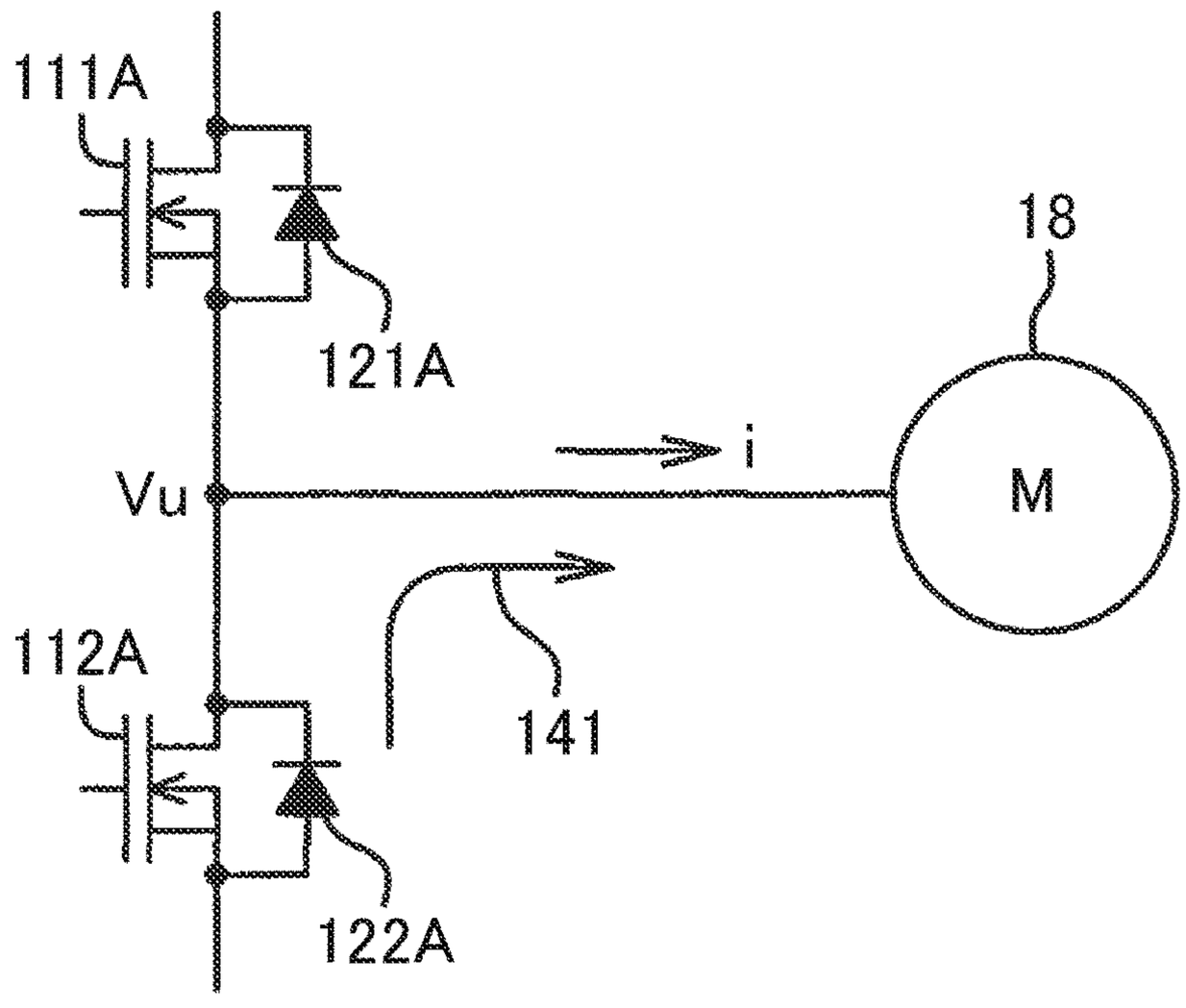


FIG. 11B

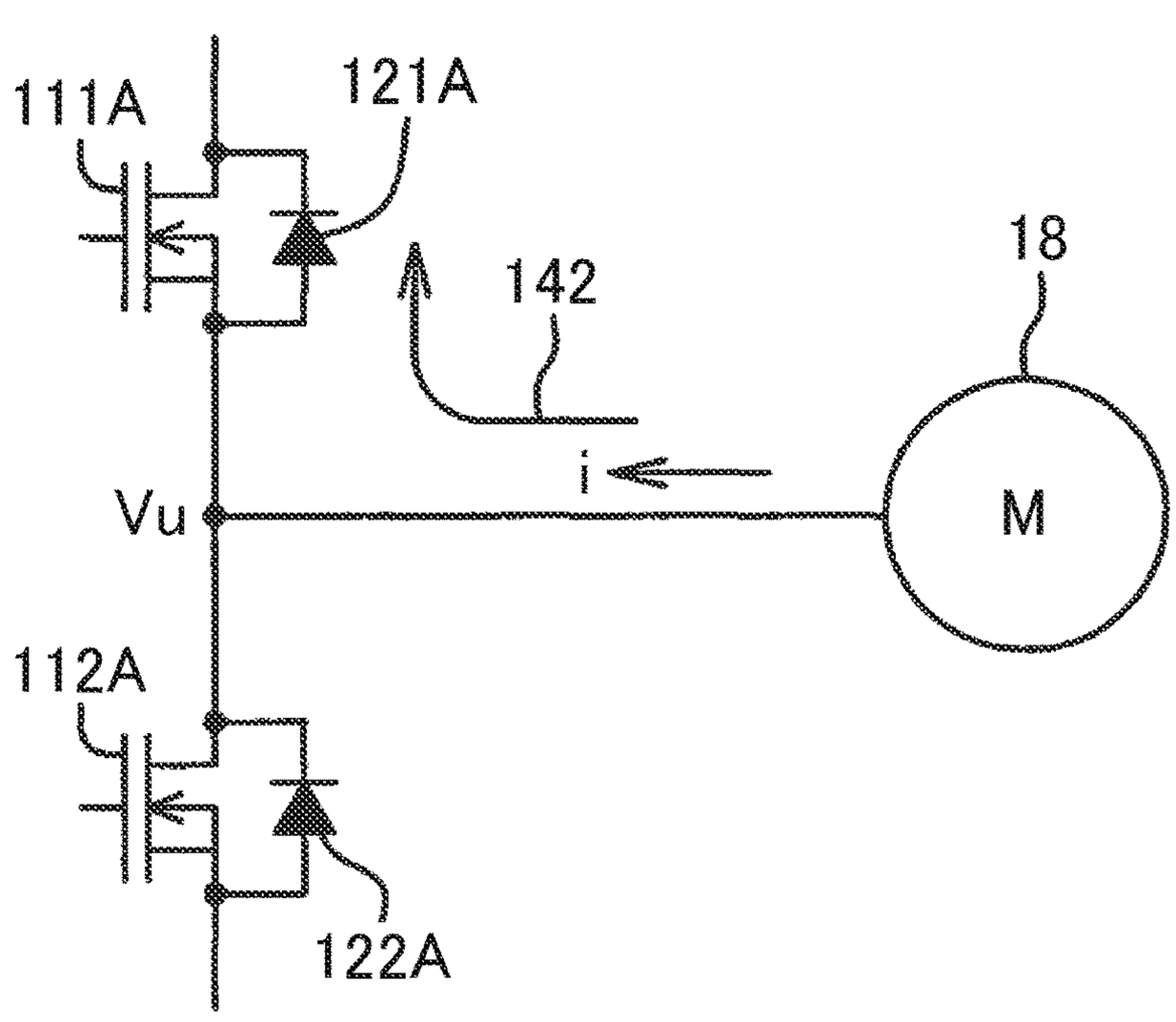


FIG. 12A

CYCLE NUMBER i	1	2	3	4	5	6	7	8	9	10	TOTAL
Cu_1 SET IN S1	400	400	400	400	400	400	400	400	400	400	4000
Cv_1 SET IN S1	200	200	200	200	200	200	200	200	200	200	2000
Cw_1 SET IN S1	100	100	100	100	100	100	100	100	100	100	1000
Cu_2 SET IN S2	350	350	350	350	350	350	350	350	350	350	3500
Cv_2 SET IN S2	300	300	300	300	300	300	300	300	300	300	3000
Cw_2 SET IN S2	50	50	50	50	50	50	50	50	50	50	500

FIG. 12B

CYCLE NUMBER i	1	2	3	4	5	6	7	8	9	10	TOTAL
Cu_1 SET IN S3	400	400	400	400	400	400	400	400	400	400	4000
Cv_1 SET IN S3	210	210	210	210	210	210	210	210	210	210	2100
Cw_1 SET IN S3	110	110	110	110	110	110	110	110	110	110	1100
Cu_2 SET IN S3	340	340	340	340	340	340	340	340	340	340	3400
Cv_2 SET IN S3	290	290	290	290	290	290	290	290	290	290	2900
Cw_2 SET IN S3	50	50	50	50	50	50	50	50	50	50	500

FIG. 13A

CYCLE NUMBER i	1	2	3	4	5	6	7	8	9	10	TOTAL
A-PHASE	x	−x	x	−x	x	−x	x	−x	x	−x	0
B-PHASE	−x	x	−x	x	−x	x	−x	x	−x	x	0

FIG. 13B

CYCLE NUMBER i	1	2	3	4	5	6	7	8	9	10	TOTAL
AMPLITUDE FOR V-PHASE IN FIRST SYSTEM	160	−160	160	−160	160	−160	160	−160	160	−160	0
AMPLITUDE FOR W-PHASE IN FIRST SYSTEM	−60	60	−60	60	−60	60	−60	60	−60	60	0
AMPLITUDE FOR U-PHASE IN SECOND SYSTEM	60	−60	60	−60	60	−60	60	−60	60	−60	0
AMPLITUDE FOR V-PHASE IN SECOND SYSTEM	−110	110	−110	110	−110	110	−110	110	−110	110	0

FIG. 13C

CYCLE NUMBER i	1	2	3	4	5	6	7	8	9	10	TOTAL
FINAL Cu_1	400	400	400	400	400	400	400	400	400	400	4000
FINAL Cv_1	360	40	360	40	360	40	360	40	360	40	2000
FINAL Cw_1	40	160	40	160	40	160	40	160	40	160	1000
FINAL Cu_2	410	290	410	290	410	290	410	290	410	290	3500
FINAL Cv_2	190	410	190	410	190	410	190	410	190	410	3000
FINAL Cw_2	50	50	50	50	50	50	50	50	50	50	500

FIG. 13D

CYCLE NUMBER i	1	2	3	4	5	6	7	8	9	10	TOTAL
Cu_1 AT ACTUAL TIMING	400	400	400	400	400	400	400	400	400	400	4000
Cv_1 AT ACTUAL TIMING	370	50	370	50	370	50	370	50	370	50	2100
Cw_1 AT ACTUAL TIMING	50	170	50	170	50	170	50	170	50	170	1100
Cu_2 AT ACTUAL TIMING	400	280	400	280	400	280	400	280	400	280	3400
Cv_2 AT ACTUAL TIMING	180	400	180	400	180	400	180	400	180	400	2900
Cw_2 AT ACTUAL TIMING	50	50	50	50	50	50	50	50	50	50	500

MOTOR CONTROL DEVICE

INCORPORATION BY REFERENCE

The disclosure of Japanese Patent Application No. 2017-195157 filed on Oct. 5, 2017, including the specification, drawings and abstract, is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a motor control device that controls an electric motor that has two-system multi-phase motor coils.

2. Description of the Related Art

In a motor control device that performs vector control on a three-phase electric motor, two-phase current command values are computed in each current control cycle. Two-phase voltage command values are computed on the basis of the deviation between the two-phase current command values and detected two-phase current values. The two-phase voltage command values are subjected to a two-phase/three-phase conversion performed using the rotational angle of the electric motor, so that phase voltage command values (three-phase voltage command values) for U-phase, V-phase, and W-phase are computed. A U-phase PWM signal, a V-phase PWM signal, and a W-phase PWM signal with duties corresponding to the phase voltage command values for U-phase, V-phase, and W-phase are generated, and supplied to a three-phase inverter circuit. (See Japanese Patent Application Publication No. 1-50766 (JP 1-50766 A), for example.)

Six switching elements that constitute the three-phase inverter circuit are controlled in accordance with the U-phase PWM signal, the V-phase PWM signal, and the W-phase PWM signal so that a voltage corresponding to the three-phase voltage command values is applied to the three-phase electric motor. Consequently, a motor current that flows through the three-phase electric motor is controlled so as to be equal to the two-phase current command values. In such a motor control device, a current flows through a stray capacitance that is present between the three-phase electric motor and a frame ground at the time of rise and the time of fall of output voltages (phase voltages) for each phase in each PWM cycle.

Since this current flows through the frame ground, noise may be radiated from the frame ground. In the case where the motor control device is mounted on an electric power steering (EPS) system mounted on a vehicle, long positive and negative power supply lines extend from a vehicle power source (battery) to the EPS. Therefore, a noise current that flows through the frame ground intrudes into the positive and negative power supply lines in the vicinity of the vehicle power source through the stray capacitance which is formed between the positive and negative power supply lines and the frame ground. The noise current then flows through the long positive and negative power supply lines to radiate noise from the lines. Consequently, common mode noise is generated.

There is known a motor control device that controls a three-phase electric motor (two-system motor) that has two-system three-phase motor coils using two-system drive circuits that supply power to the respective two-system three-phase motor coils. In such a motor control device that controls the two-system motor, a current flows through a stray capacitance that is present between the three-phase electric motor and a frame ground at the time of rise and the time of fall of output voltages (phase voltages) for each phase in each PWM cycle for each of the two-system drive circuits. Therefore, in the case where the two-system motor is controlled, the frequency of generation of common mode noise is high compared to a case where drive of a three-phase electric motor (one-system motor) that has a one-system three-phase motor coil is controlled.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a motor control device that is configured to reduce common mode noise.

According to an aspect of the present invention, a motor control device controls an electric motor that has two-system multi-phase motor coils. The motor control device includes: a pulse width modulation (PWM) count computation unit that computes a PWM count for each phase in each system in each current control cycle that includes a plurality of PWM cycles; a PWM count setting unit that sets the PWM count for each phase in each system in a current control cycle as a PWM count in each PWM cycle in the current control cycle for the corresponding phase in the corresponding system; and a common mode noise reduction unit that changes the PWM count in a PWM cycle for at least one phase in one of the two systems such that a current that flows through a stray capacitance because of an output voltage for one phase in the other system is canceled out with a current that flows through the stray capacitance because of an output voltage for the at least one phase in the one system in at least one PWM cycle in the current control cycle. The common mode noise reduction unit includes a PWM count change unit that changes the PWM count for the at least one phase in the one system, of a PWM signal in each PWM cycle in the current control cycle for each phase in each system, such that an output voltage waveform for the at least one phase is a waveform obtained by inverting an output voltage waveform for the one phase in the other system in the at least one PWM cycle without changing a total value of PWM counts for the at least one phase in the current control cycle.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and further features and advantages of the invention will become apparent from the following description of example embodiments with reference to the accompanying drawings, wherein like numerals are used to represent like elements and wherein:

FIG. **1** is a schematic diagram illustrating a schematic configuration of an electric power steering system to which a motor control device according to an embodiment of the present invention is applied;

FIG. **2** is a block diagram illustrating the electric configuration of an ECU;

FIG. **3** is an electric circuit diagram mainly illustrating the configuration of a first motor drive circuit and a second motor drive circuit;

FIG. **4** is a block diagram illustrating the configuration of a system- and phase-specific PWM count computation section;

FIG. **5**A is a schematic chart illustrating the relationship between a PWM signal cycle Tc and a current control cycle Ta;

FIG. **5**B is a waveform chart illustrating a carrier waveform;

FIG. **5**C is a schematic chart illustrating how to generate a PWM signal;

FIG. **6** is a graph illustrating an example of an assist current value Ia* set with respect to detected steering torque T;

FIGS. **7**A to **7**E illustrate the basic idea of a common mode noise reduction performed by a common mode noise reduction section;

FIG. **8** is a circuit diagram illustrating an equivalent circuit that places a focus on common mode noise currents;

FIG. **9** is a flowchart illustrating an example of operation of the common mode noise reduction section;

FIGS. **10**A to **10**H are schematic charts mainly illustrating the relationship between a PWM count in each PWM cycle for a certain phase and an upper FET command and a lower FET command for the relevant phase in each system;

FIG. **11**A illustrates a current path during a dead time period with a current flowing from the point of connection between an upper FET and a lower FET toward an electric motor;

FIG. **11**B illustrates a current path during a dead time period with a current flowing from the electric motor toward the point of connection between the upper FET and the lower FET;

FIG. **12**A is a schematic table illustrating an example of PWM counts in each PWM cycle for phases in each system set in steps S**1** and S**2**;

FIG. **12**B is a schematic table illustrating an example of PWM counts in each PWM cycle for phases in each system set in step S**3**;

FIG. **13**A is a schematic table illustrating an example of two amplitude patterns applied to two count change target phases in the same system;

FIG. **13**B is a schematic table illustrating an example of the amplitude in each PWM cycle for V-phase in the first system, W-phase in the first system, U-phase in the second system, and V-phase in the second system;

FIG. **13**C is a schematic table illustrating an example of the final PWM count for each phase in each system in each PWM cycle; and

FIG. **13**D is a schematic table illustrating the switching timing that coincides with an output voltage for each phase in each system corresponding to the final PWM count indicated in FIG. **13**C.

DETAILED DESCRIPTION OF EMBODIMENTS

An embodiment in which the present invention is applied to an electric power steering system will be described in detail below with reference to the accompanying drawings. FIG. **1** is a schematic diagram illustrating a schematic configuration of an electric power steering system to which a motor control device according to an embodiment of the present invention is applied. An electric power steering (EPS) system **1** includes a steering wheel **2**, a steering operation mechanism **4**, and a steering assist mechanism **5**. The steering wheel **2** is a steering member configured to steer the vehicle. The steering operation mechanism **4** steers steered wheels **3** in conjunction with rotation of the steering wheel **2**. The steering assist mechanism **5** assists a driver in steering. The steering wheel **2** and the steering operation mechanism **4** are mechanically coupled to each other via a steering shaft **6** and an intermediate shaft **7**.

The steering shaft **6** includes an input shaft **8** coupled to the steering wheel **2**, and an output shaft **9** coupled to the intermediate shaft **7**. The input shaft **8** and the output shaft **9** are coupled so as to be rotatable relative to each other via a torsion bar **10**. A torque sensor **11** is disposed in the vicinity of the torsion bar **10**. The torque sensor **11** detects steering torque T applied to the steering wheel **2** on the basis of the amount of relative rotational displacement between the input shaft **8** and the output shaft **9**. In the embodiment, the steering torque T which is detected by the torque sensor **11** is detected as a positive value when the vehicle is steered to the right, and as a negative value when the vehicle is steered to the left, for example, and the magnitude of the steering torque T is larger as the absolute value of the positive or negative value is larger.

The steering operation mechanism **4** is composed of a rack-and-pinion mechanism that includes a pinion shaft **13** and a rack shaft **14** that serves as a steered shaft. The steered wheels **3** are coupled to end portions of the rack shaft **14** via tie rods **15** and knuckle arms (not illustrated). The pinion shaft **13** is coupled to the intermediate shaft **7**. The pinion shaft **13** is rotated in conjunction with a steering operation of the steering wheel **2**. A pinion **16** is coupled to the distal end (the lower end in FIG. **1**) of the pinion shaft **13**.

The rack shaft **14** extends linearly along the right-left direction of the automobile. A rack **17** meshed with the pinion **16** is formed at an intermediate portion of the rack shaft **14** in the axial direction. The pinion **16** and the rack **17** convert rotation of the pinion shaft **13** into movement of the rack shaft **14** in the axial direction. The steered wheels **3** can be steered by moving the rack shaft **14** in the axial direction.

When the steering wheel **2** is operated (rotated), rotation of the steering wheel **2** is transferred to the pinion shaft **13** via the steering shaft **6** and the intermediate shaft **7**. The pinion **16** and the rack **17** convert rotation of the pinion shaft **13** into movement of the rack shaft **14** in the axial direction. Consequently, the steered wheels **3** are steered. The steering assist mechanism **5** includes an electric motor **18** for steering assist, and a speed reduction mechanism **19** configured to transfer output torque from the electric motor **18** to the steering operation mechanism **4**. The electric motor **18** is a three-phase brushless motor (two-system motor) that has a three-phase motor coil **18**A (see FIGS. **2** and **3**) in a first system and a three-phase motor coil **18**B (see FIGS. **2** and **3**) in a second system. The three-phase motor coil **18**A in the first system is driven by a drive circuit **32**A (see FIGS. **2** and **3**) in the first system to be discussed later. The three-phase motor coil **18**B in the second system is driven by a drive circuit **32**B (see FIGS. **2** and **3**) in the second system.

The electric motor **18** is provided with a rotational angle sensor **23** such as a resolver configured to detect the rotational angle of a rotor of the electric motor **18**. The speed reduction mechanism **19** is composed of a worm gear mechanism that includes a worm shaft **20** and a worm wheel **21** meshed with the worm shaft **20**. The worm shaft **20** is rotationally driven by the electric motor **18**. The worm wheel **21** is coupled so as to be rotatable together with the steering shaft **6**. The worm wheel **21** is rotationally driven by the worm shaft **20**.

When the worm shaft **20** is rotationally driven by the electric motor **18**, the worm wheel **21** is rotationally driven to rotate the steering shaft **6**. Rotation of the steering shaft **6** is transferred to the pinion shaft **13** via the intermediate shaft **7**. Rotation of the pinion shaft **13** is converted into movement of the rack shaft **14** in the axial direction. Consequently, the steered wheels **3** are steered. That is, the worm shaft **20** is rotationally driven by the electric motor **18** to enable steering assist by the electric motor **18**.

The vehicle is provided with a vehicle speed sensor **24** configured to detect a vehicle speed V. The steering torque T which is detected by the torque sensor **11**, the vehicle speed V which is detected by the vehicle speed sensor **24**, an output signal from the rotational angle sensor **23**, etc. are input to an electronic control unit (ECU) **12**. The ECU **12** controls the electric motor **18** on the basis of such input signals.

FIG. **2** is a block diagram illustrating the overall electric configuration of the ECU **12**. Hereinafter, the three-phase motor coil **18**A in the first system will be referred to as a first motor coil **18**A, and the three-phase motor coil **18**B in the second system will be referred to as a second motor coil **18**B. The first motor coil **18**A has stator coils **18**AU, **18**AV, and **18**AW (see FIG. **3**) for U-phase, V-phase, and W-phase. The second motor coil **18**B has stator coils **18**BU, **18**BV, and **18**BW (see FIG. **3**) for U-phase, V-phase, and W-phase. The phase difference between the first motor coil **18**A and the second motor coil **18**B is preferably 0 degrees, 120 degrees, or 240 degrees.

The ECU **12** includes a microcomputer **31**, a first drive circuit **32**A, and a second drive circuit **32**B. The first drive circuit **32**A is controlled by the microcomputer **31**, and supplies power to the first motor coil **18**A of the electric motor **18**. The second drive circuit **32**B is controlled by the microcomputer **31**, and supplies power to the second motor coil **18**B of the electric motor **18**. FIG. **3** is an electric circuit diagram mainly illustrating the configuration of the first motor drive circuit **32**A and the second motor drive circuit **32**B.

The first motor drive circuit **32**A is a three-phase inverter circuit. The first motor drive circuit **32**A includes a first smoothing capacitor **101**A, a plurality of switching elements **111**A to **116**A, and a plurality of diodes **121**A to **126**A. The first smoothing capacitor **101**A is connected in series with a power source (battery) **100**. The first smoothing capacitor **101**A is connected between both terminals of the power source **100**. In the embodiment, the switching elements **111**A to **116**A are each constituted from an n-channel metal oxide semiconductor field effect transistor (MOSFET). Hereinafter, the switching elements **111**A to **116**A will be occasionally referred to as FETs **111**A to **116**A.

The FETs **111**A to **116**A include an upper FET **111**A for U-phase, a lower FET **112**A for U-phase connected in series thereto, an upper FET **113**A for V-phase, a lower FET **114**A for V-phase connected in series thereto, an upper FET **115**A for W-phase, and a lower FET **116**A for W-phase connected in series thereto. The switching elements **111**A to **116**A are connected in inverse parallel with the diodes **121**A to **126**A, respectively.

The drain of the upper FET **111**A, **113**A, **115**A is connected to a positive electrode terminal of the first smoothing capacitor **101**A. The source of the upper FET **111**A, **113**A, **115**A is connected to the drain of the lower FET **112**A, **114**A, **116**A, respectively. The source of the lower FET **112**A, **114**A, **116**A is connected to a negative electrode terminal of the first smoothing capacitor **101**A.

The point of connection between the upper FET **111**A and the lower FET **112**A for U-phase is connected to the stator coil **18**AU for U-phase of the first motor coil **18**A. The point of connection between the upper FET **113**A and the lower FET **114**A for V-phase is connected to the stator coil **18**AV for V-phase of the first motor coil **18**A. The point of connection between the upper FET **115**A and the lower FET **116**A for W-phase is connected to the stator coil **18**AW for W-phase of the first motor coil **18**A. The FETs **111**A to **116**A are controlled on the basis of a PWM signal output from a first PWM output section **43**A (see FIG. **2**) to be discussed later.

The second motor drive circuit **32**B is a three-phase inverter circuit. The second motor drive circuit **32**B includes a second smoothing capacitor **101**B, a plurality of switching elements **111**B to **116**B, and a plurality of diodes **121**B to **126**B. The second smoothing capacitor **101**B is connected in series with the power source (battery) **100**. The second smoothing capacitor **101**B is connected between both terminals of the power source **100**. In the embodiment, the switching elements **111**B to **116**B are each constituted from an n-channel MOSFET. Hereinafter, the switching elements **111**B to **116**B will be occasionally referred to as FETs **111**B to **116**B.

The FETs **111**B to **116**B include an upper FET **111**B for U-phase, a lower FET **112**B for U-phase connected in series thereto, an upper FET **113**B for V-phase, a lower FET **114**B for V-phase connected in series thereto, an upper FET **115**B for W-phase, and a lower FET **116**B for W-phase connected in series thereto. The switching elements **111**B to **116**B are connected in inverse parallel with the diodes **121**B to **126**B, respectively.

The drain of the upper FET **111**B, **113**B, **115**B is connected to a positive electrode terminal of the second smoothing capacitor **101**B. The source of the upper FET **111**B, **113**B, **115**B is connected to the drain of the lower FET **112**B, **114**B, **116**B, respectively. The source of the lower FET **112**B, **114**B, **116**B is connected to a negative electrode terminal of the second smoothing capacitor **101**B.

The point of connection between the upper FET **111**B and the lower FET **112**B for U-phase is connected to the stator coil **18**BU for U-phase of the second motor coil **18**B. The point of connection between the upper FET **113**B and the lower FET **114**B for V-phase is connected to the stator coil **18**BV for V-phase of the second motor coil **18**B. The point of connection between the upper FET **115**B and the lower FET **116**B for W-phase is connected to the stator coil **18**BW for W-phase of the second motor coil **18**B. The FETs **111**B to **116**B are controlled on the basis of a PWM signal output from a second PWM output section **43**B (see FIG. **2**) to be discussed later.

In FIG. **3**, the power source **100** is mounted on a vehicle. A negative (−) electrode of the power source **100** is electrically connected to a frame (chassis) **130**, which is made of metal, of the vehicle. Therefore, the frame **130** is at the same potential as the negative electrode of the power source **100**. The electric power steering system **1** on which the electric motor **18** is mounted is attached to the frame **130** with a bolt or the like. The + power source line and the − power source line of the ECU are connected to the positive and negative electrodes, respectively, of the power source **100** through long lines. Therefore, stray capacitances C**1** and C**2** are present between the first and second motor coils **18**A and **18**B, respectively, and the frame **130**. In addition, stray capacitances C**3** and C**4** are present between the positive and negative lines, respectively, which connect between the power source **100** and the electric power steering system **1** and the frame ground.

Returning FIG. **2**, two current sensors **33** and **34** are provided in power supply lines configured to connect between the first drive circuit **32**A and the first motor coil **18**A. Such current sensors **33** and **34** are provided so as to be able to detect phase currents that flow through two of three power supply lines configured to connect between the first drive circuit **32**A and the first motor coil **18**A.

Similarly, two current sensors **35** and **36** are provided in power supply lines configured to connect between the second drive circuit **32**B and the second motor coil **18**B. Such current sensors **35** and **36** are provided so as to be able to detect phase currents that flow through two of three power supply lines configured to connect between the second drive circuit **32**B and the second motor coil **18**B. The microcomputer **31** includes a central processing unit (CPU) and a memory (such as a read-only memory (ROM), a random-access memory (RAM), and a non-volatile memory), and executes a predetermined program to function as a plurality of function processing sections. The function processing sections include a system- and phase-specific PWM count computation section **41**, a common mode noise reduction section **42**, the first PWM output section **43**A, and the second PWM output section **43**B.

FIG. **4** is a block diagram illustrating the configuration of the system- and phase-specific PWM count computation section **41**. The system- and phase-specific PWM count computation section **41** computes a PWM count in each current control cycle for each phase in each system. The system- and phase-specific PWM count computation section **41** includes an assist current value setting section **51**, a current command value setting section **52**, a command value distribution section **53**, a first system computation section **70**A, a second system computation section **70**B, a rotational angle computation section **59**, a rotational speed computation section **60**, and a rotational angle estimation section **61**.

The first system computation section **70**A includes a first current deviation computation section **54**A, a first proportional-integral (PI) control section **55**A, a first two-phase/three-phase conversion section **56**A, a first PWM duty computation section **57**A, and a first three-phase/two-phase conversion section **58**A. The second system computation section **70**B includes a second current deviation computation section **54**B, a second proportional-integral (PI) control section **55**B, a second two-phase/three-phase conversion section **56**B, a second PWM duty computation section **57**B, and a second three-phase/two-phase conversion section **58**B.

As indicated in FIG. **5**A, a cycle of the PWM signal (hereinafter referred to as a "PWM cycle") Tc is shorter than a current control cycle Ta. The current control cycle Ta is the computation cycle of the control loop of the motor current. That is, the current control cycle Ta is the computation cycle of each block included in the first system computation section **70**A and the second system computation section **70**B in FIG. **4**. The current control cycle Ta is determined in consideration of the scale of the program, the computation capacity of the microcomputer **31**, etc. In the embodiment, PWM duties are updated by the PWM duty computation sections **57**A and **57**B at the first timing in the present current control cycle Ta to output updated PWM duties C_{u1}, C_{v1}, C_{w1}, C_{u2}, C_{v2}, and C_{w2}. In the embodiment, Tc is one-tenth of Ta. In other words, each current control cycle Ta includes ten PWM cycles Tc. The first cycle of the ten PWM cycles Tc may be referred to as a first cycle, and the subsequent cycles may be referred to as second, third, . . . , ninth, and tenth cycles. The cycle number of the PWM cycles may be represented by i (i=1, 2, . . . , 9, and 10). The frequency (=1/Tc) of the PWM signal is called a carrier frequency.

A PWM waveform generation method according to the present embodiment will be described. In the microcomputer **31**, the clocks of a PWM clock frequency generated by a clock generator (not illustrated) are counted up and counted down by a counter (not illustrated). The count value of the counter is indicated in FIG. **5**B in which the horizontal axis represents the time and the vertical axis represents the count value. The count value is interpreted as an unsigned integer. The count value may be called a carrier count. In the embodiment, the waveform in FIG. **5**B is a carrier waveform. The carrier waveform is a triangular waveform. One cycle of the triangular waveform is equal to Tc. The frequency (carrier frequency) of the PWM signal is determined by the maximum value of the carrier waveform, that is, the maximum value of the count value. In the present embodiment, the PWM clock frequency is 100 [MHz], and the frequency of the PWM signal (hereinafter referred to as a "PWM frequency") is set to 100 [kHz]. Therefore, the maximum value of the count value is 100,000,000÷100,000÷2=500. Since the clocks are counted up and down, 100,000,000/100,000 is divided by 2.

As illustrated in FIG. **5**C, the PWM output sections **43**A and **43**B (see FIG. **2**) compare a given PWM count and the count value of the counter, and output a High or Low signal to the drive circuits **32**A and **32**B (see FIG. **2**), respectively. The PWM output sections **43**A and **43**B output a High signal while the count value of the counter is equal to or more than the PWM count, and output a Low signal otherwise, for example. The High and Low signals are used as the PWM signal. Operation of the PWM output sections **43**A and **43**B will be discussed in detail later.

Returning FIG. **4**, the rotational angle computation section **59** computes a rotational angle θ (electrical angle) of the rotor of the electric motor **18** on the basis of an output signal from the rotational angle sensor **23** in each current control cycle Ta. The rotor rotational angle θ, which is computed by the rotational angle computation section **59**, is provided to the first and second three-phase/two-phase conversion sections **58**A and **58**B, the rotational speed computation section **60**, and the rotational angle estimation section **61**. In the embodiment, the rotor rotational angle θ is acquired (detected) at the timing at the middle of the current control cycle Ta.

The rotational speed computation section **60** computes a rotational speed (angular speed) ω of the rotor of the electric motor **18** by differentiating the rotor rotational angle θ, which is computed by the rotational angle computation section **59**, with respect to time. The rotational speed ω, which is computed by the rotational speed computation section **60**, is provided to the rotational angle estimation section **61**. The rotational angle estimation section **61** estimates a rotor rotational angle $\theta_{(m+1)}$ at the middle of the next current control cycle Ta on the basis of the following formula (1) using the rotor rotational angle $\theta_{(m+1)}$ at the middle of the previous current control cycle Ta, which is acquired in the previous current control cycle Ta.

$$\theta_{(m+1)}=\theta_{(m-1)}+\omega\cdot 2Ta \tag{1}$$

The rotor rotational angle $\theta_{(m+1)}$ at the next current control cycle Ta, which is estimated by the rotational angle estimation section **61**, is provided to the first and second two-phase/three-phase conversion sections **56**A and **56**B. The assist current value setting section **51** sets an assist current value Ia* in each current control cycle Ta on the basis of the detected steering torque T, which is detected by the torque sensor **11**, and the vehicle speed V, which is detected by the vehicle speed sensor **24**. An example of the assist current value Ia* which is set with respect to the detected steering torque T is illustrated in FIG. **6**. The detected steering torque T has a positive value when the torque is applied to steer the vehicle to the right, and a negative value when the torque is applied to steer the vehicle to the left, for example. The assist current value Ia* has a positive value when the electric

motor **18** should generate a steering assist force for steering the vehicle to the right, and a negative value when the electric motor **18** should generate a steering assist force for steering the vehicle to the left. The assist current value Ia* is positive when the detected steering torque T has a positive value, and is negative when the detected steering torque T has a negative value.

When the detected steering torque T has a very small value in the range (torque dead band) of −T1 to T1 (e.g. T1=0.4 N·m), the assist current value Ia* is set to zero. In the case where the detected steering torque T has a value outside the range of −T1 to T1, the assist current value Ia* is set such that the absolute value thereof becomes larger as the absolute value of the detected steering torque T becomes larger. The assist current value Ia* is also set such that the absolute value thereof becomes smaller as the vehicle speed V, which is detected by the vehicle speed sensor **24**, becomes higher. Consequently, a large assist force is generated during low-speed travel, and a small assist force is generated during high-speed travel.

The current command value setting section **52** sets the values of currents that should flow on the coordinate axes of a dq coordinate system as current command values on the basis of the assist current value Ia*, which is set by the assist current value setting section **51**. Specifically, the current command value setting section **52** sets a d-axis current command value I_d* and a q-axis current command value I_q* (which will hereinafter be referred to collectively as "two-phase current command values I_{dq}*"). Further specifically, the current command value setting section **52** sets the q-axis current command value I_q* to the assist current value I_a*, which is set by the assist current value setting section **51**, and sets the d-axis current command value I_d* to zero. The two-phase current command values I_{dq}*, which are set by the current command value setting section **52**, are provided to the command value distribution section **53**.

The command value distribution section **53** distributes the two-phase current command values I_{dq}* to the first system computation section **70**A and the second system computation section **70**B. In the embodiment, the command value distribution section **53** distributes half the two-phase current command values I_{dq}* to each of the first system computation section **70**A and the second system computation section **70**B. That is, in the embodiment, both the rate of distribution of the two-phase current command values I_{dq}* to the first system computation section **70**A and the rate of distribution of the two-phase current command values I_{dq}* to the second system computation section **70**B are 50%. The two-phase current command values distributed to the first system computation section **70**A are referred to as first two-phase current command values I_{1dp}*. The first two-phase current command values I_{1dq}* include a first d-axis current command value I_{1d}* and a first q-axis current command value I_{1q}*. The two-phase current command values distributed to the second system computation section **70**B are referred to as second two-phase current command values I_{2dp}*. The second two-phase current command values I_{2dq}* include a second d-axis current command value I_{2d}* and a second q-axis current command value I_{2q}*.

Next, the first system computation section **70**A will be described. The first three-phase/two-phase conversion section **58**A first computes a U-phase current I_{1U}, a V-phase current I_{1V}, and a W-phase current I_{1W} (which will hereinafter be referred to collectively as "detected three-phase currents I_{1UVW}") for the first system from the phase currents for two phases, which are detected by the current sensors **33** and **34**. The first three-phase/two-phase conversion section **58**A then performs a coordinate conversion on the detected three-phase currents I_{1UVW} for the UVW coordinate system in the first system into detected two-phase currents I_{1dq} for the dq coordinate system in the first system. The detected two-phase currents I_{1dq} for the first system include a first detected d-axis current I_{1d} and a first detected q-axis current I_{1q}. The rotor rotational angle θ, which is computed by the rotational angle computation section **59**, is used in the coordinate conversion.

The first current deviation computation section **54**A computes a deviation of the first detected d-axis current I_{1d} from the first d-axis current command value I_{1d}* and a deviation of the first detected q-axis current I_{1q} from the first q-axis current command value I_{1q}*. Such deviations are provided to the first PI control section **55**A. The first PI control section **55**A performs a PI computation on the current deviations, which are computed by the first current deviation computation section **54**A. Consequently, first two-phase voltage command values V_{1dq}* (a first d-axis voltage command value V_{1d}* and a first q-axis voltage command value V_{1q}*) to be applied to the first motor coil **18**A are generated. The first two-phase voltage command values V_{1dq}* are provided to the first two-phase/three-phase conversion section **56**A.

The first two-phase/three-phase conversion section **56**A performs a two-phase/three-phase conversion on the first two-phase voltage command values V_{1dq}*, which are computed by the first PI control section **55**A in the present current control cycle Ta, using an estimated rotational angle value $\theta_{(m+1)}$ for the next current control cycle Ta, which is computed by the rotational angle estimation section **61** in the present current control cycle Ta. Consequently, first three-phase voltage command values V_{1UVW}* for the next current control cycle Ta are computed. The first three-phase voltage command values V_{1UVW}* include a first U-phase voltage command value V_{1U}*, a first V-phase voltage command value V_{1V}*, and a first W-phase voltage command value V_{1W}*. Consequently, the first three-phase voltage command values V_{1UVW}* for the next current control cycle Ta are obtained.

The first three-phase voltage command values V_{1UVW}* for the next current control cycle Ta, which are obtained by the first two-phase/three-phase conversion section **56**A, are provided to the first PWM duty computation section **57**A. The first PWM duty computation section **57**A generates a first U-phase PWM count (PWM duty) Cu_1, a first V-phase PWM count Cv_1, and a first W-phase PWM count Cw_1 for the next current control cycle Ta on the basis of the first three-phase voltage command values V_{1UVW}* for the next current control cycle Ta, and provides such counts to the common mode noise reduction section **42** (see FIG. **2**).

For example, the first U-phase PWM count Cu_1 is calculated as follows. That is, the first PWM duty computation section **57**A computes the first U-phase PWM count Cu_1 for a certain current control cycle Ta on the basis of the following formula (2) using the first U-phase voltage command value V_{1U}* for the relevant current control cycle Ta, which is obtained by the first two-phase/three-phase conversion section **56**A, and the maximum value (in the example, 500) of the PWM count.

$$Cu_1 = V_{1U}^* \times (\text{maximum value of } PWM \text{ count}/Vb) = V_{1U}^* \times (500/Vb) \quad (2)$$

In the formula (2), Vb is the power source voltage for the first drive circuit **32**A (output voltage of the power source

100). The first V-phase PWM count Cv_1 can be computed by using the first V-phase voltage command value V_{1V}* in place of the first U-phase voltage command value V_{1U}* on the right side of the formula (2). The first W-phase PWM count Cw_1 can be computed by using the first W-phase voltage command value V_{1W}* in place of the first U-phase voltage command value V_{1U}*.

Next, the second system computation section **70**B will be described. The second three-phase/two-phase conversion section **58**B first computes a U-phase current I_{2U}, a V-phase current I_{2V}, and a W-phase current I_{2W} (which will hereinafter be referred to collectively as "detected three-phase currents I_{2UVW}") for the second system from the phase currents for two phases, which are detected by the current sensors **35** and **36**. The second three-phase/two-phase conversion section **58**B then performs a coordinate conversion on the detected three-phase currents I_{2UVW} for the UVW coordinate system in the second system into detected two-phase currents I_{2dq} for the dq coordinate system in the second system. The detected two-phase currents I_{2dq} for the second system include a second detected d-axis current I_{2d} and a second detected q-axis current I_{2q}. The rotor rotational angle θ, which is computed by the rotational angle computation section **59**, is used in the coordinate conversion.

The second current deviation computation section **54**B computes a deviation of the second detected d-axis current I_{2d} from the second d-axis current command value I_{2d}* and a deviation of the second detected q-axis current I_{2q} from the second q-axis current command value I_{2q}*. Such deviations are provided to the second PI control section **55**B. The second PI control section **55**B performs a PI computation on the current deviations, which are computed by the second current deviation computation section **54**B. Consequently, second two-phase voltage command values V_{2dq}* (a second d-axis voltage command value V_{2d}* and a second q-axis voltage command value V_{2q}*) to be applied to the second motor coil **18**B are generated. The second two-phase voltage command values V_{2dq}* are provided to the second two-phase/three-phase conversion section **56**B.

The second two-phase/three-phase conversion section **56**B performs a two-phase/three-phase conversion on the second two-phase voltage command values V_{2dq}*, which are computed by the second PI control section **55**B in the present current control cycle Ta, using an estimated rotational angle value $\theta_{(m+1)}$ for the next current control cycle Ta, which is computed by the rotational angle estimation section **61** in the present current control cycle Ta. Consequently, second three-phase voltage command values V_{2UVW}* for the next current control cycle Ta are computed. The second three-phase voltage command values V_{2UVW}* include a second U-phase voltage command value V_{2U}*, a second V-phase voltage command value V_{2V}*, and a second W-phase voltage command value V_{2W}*. Consequently, the second three-phase voltage command values V_{2UVW}* for the next current control cycle Ta are obtained.

The second three-phase voltage command values V_{2UVW}* for the next current control cycle Ta, which are obtained by the second two-phase/three-phase conversion section **56**B, are provided to the second PWM duty computation section **57**B. The second PWM duty computation section **57**B generates a second U-phase PWM count (PWM duty) Cu_2, a second V-phase PWM count Cv_2, and a second W-phase PWM count Cw_2 for the next current control cycle Ta on the basis of the second three-phase voltage command values V_{2UVW}* for the next current control cycle Ta, and provides such counts to the common mode noise reduction section **42** (see FIG. **2**).

For example, the second U-phase PWM count Cu_2 is calculated as follows. That is, the second PWM duty computation section **57**B computes the second U-phase PWM count Cu_2 for a certain current control cycle Ta on the basis of the following formula (3) using the second U-phase voltage command value V_{2U}* for the relevant current control cycle Ta, which is obtained by the second two-phase/three-phase conversion section **56**B, and the maximum value (in the example, 500) of the PWM count.

$$\begin{aligned} Cu_2 &= \text{maximum value of } PWM \text{ count} - \\ &\quad \{V_{2U}^* \times (\text{maximum value of } PWM \text{ count}/Vb)\} \\ &= \text{maximum value of } PWM \text{ count} - \\ &\quad \{V_{2U}^* \times (500/Vb)\} \end{aligned} \tag{3}$$

In the formula (3), Vb is the power source voltage for the second drive circuit **32**B (output voltage of the power source **100**). The second V-phase PWM count Cv_2 can be computed by using the second V-phase voltage command value V_{2V}* in place of the second U-phase voltage command value V_{2U}* on the right side of the formula (3). The second W-phase PWM count Cw_2 can be computed by using the second W-phase voltage command value V_{2W}* in place of the second U-phase voltage command value V_{2U}*.

The common mode noise reduction section **42** is provided to reduce common mode noise by canceling out a part of a noise current generated by turning on and off of the switching elements in the first drive circuit **32**A with a part of a noise current generated by turning on and off of the switching elements in the second drive circuit **32**B. The common mode noise reduction section **42** performs processing (noise reduction processing) for reducing common mode noise on the first and second U-phase PWM counts Cu_1 and Cu_2, V-phase PWM counts Cv_1 and Cv_2, and W-phase PWM counts Cw_1 and Cw_2 for the next current control cycle Ta, which are provided from the first and second PWM duty computation sections **57**A and **57**B. Consequently, the first U-phase PWM count, V-phase PWM count, and W-phase PWM count for each PWM cycle Tc in the next current control cycle Ta and the second U-phase PWM count, V-phase PWM count, and W-phase PWM count for each PWM cycle Tc in the next current control cycle Ta are obtained. Operation of the common mode noise reduction section **42** will be discussed in detail later.

The first U-phase PWM count, V-phase PWM count, and W-phase PWM count for each PWM cycle Tc in the next current control cycle Ta after being subjected to the noise reduction processing, which is performed by the common mode noise reduction section **42**, are provided to the first PWM output section **43**A. On the other hand, the second U-phase PWM count, V-phase PWM count, and W-phase PWM count for each PWM cycle Tc in the next current control cycle Ta after being subjected to the noise reduction processing, which is performed by the common mode noise reduction section **42**, are provided to the second PWM output section **43**B.

The first PWM output section **43**A stores the first U-phase PWM count, V-phase PWM count, and W-phase PWM count for each PWM cycle Tc in the current control cycle Ta, which are provided from the common mode noise reduction section **42**, for a plurality of current control cycles. The first PWM output section **43**A generates first U-phase PWM signal, V-phase PWM signal, and W-phase PWM signal for each PWM cycle Tc in the present current control cycle on the basis of the first U-phase PWM count, V-phase PWM

count, and W-phase PWM count for each PWM cycle Tc in the present current control cycle Ta, which are provided from the common mode noise reduction section **42** in the previous current control cycle Ta, and supplies such signals to the first drive circuit **32**A. Specifically, the first PWM output section **43**A generates, for each PWM cycle Tc in the present current control cycle Ta, U-phase PWM signal, V-phase PWM signal, and W-phase PWM signal with duties corresponding to the first U-phase PWM count, V-phase PWM count, and W-phase PWM count, respectively, for each PWM cycle Tc in the relevant current control cycle Ta, and supplies such signals to the first drive circuit **32**A.

The six FETs **111**A to **116**A, which constitute the first drive circuit **32**A, are controlled in accordance with the PWM signals, which are provided from the first PWM output section **43**A. Consequently, a voltage corresponding to the first three-phase voltage command values V_{1UVW}* for each PWM cycle Tc is applied to the stator coils **18**AU, **18**AV, and **18**AW for respective phases of the first motor coil **18**A. The first current deviation computation section **54**A and the first PI control section **55**A constitute a current feedback control unit. A motor current that flows through the first motor coil **18**A is controlled so as to become closer to the first two-phase current command values I_{1dq}*, which are distributed to the first system computation section **70**A by the command value distribution section **53**, through operation of the current feedback control unit.

The second PWM output section **43**B stores the second U-phase PWM count, V-phase PWM count, and W-phase PWM count for each PWM cycle Tc in the current control cycle Ta, which are provided from the common mode noise reduction section **42**, for a plurality of current control cycles. The second PWM output section **43**B generates second U-phase PWM signal, V-phase PWM signal, and W-phase PWM signal for each PWM cycle Tc in the present current control cycle on the basis of the second U-phase PWM count, V-phase PWM count, and W-phase PWM count for each PWM cycle Tc in the present current control cycle Ta, which are provided from the common mode noise reduction section **42** in the previous current control cycle Ta, and supplies such signals to the second drive circuit **32**B. Specifically, the second PWM output section **43**B generates, for each PWM cycle Tc in the present current control cycle Ta, U-phase PWM signal, V-phase PWM signal, and W-phase PWM signal with duties corresponding to the second U-phase PWM count, V-phase PWM count, and W-phase PWM count, respectively, for each PWM cycle Tc in the relevant current control cycle Ta, and supplies such signals to the second drive circuit **32**B.

The six FETs **111**B to **116**B, which constitute the second drive circuit **32**B, are controlled in accordance with the PWM signals, which are provided from the second PWM output section **43**B. Consequently, a voltage corresponding to the second three-phase voltage command values V_{2UVW}* for each PWM cycle Tc is applied to the stator coils **18**BU, **18**BV, and **18**BW for respective phases of the second motor coil **18**B. The second current deviation computation section **54**B and the second PI control section **55**B constitute a current feedback control unit. A motor current that flows through the second motor coil **18**B is controlled so as to become closer to the second two-phase current command values I_{2dq}*, which are distributed to the second system computation section **70**B by the command value distribution section **53**, through operation of the current feedback control unit.

The common mode noise reduction section **42** will be described in detail below. First, the basic idea of the common mode noise reduction which is performed by the common mode noise reduction section **42** will be described with reference to FIGS. **7**A to **7**E. In the case where the waveform of an output voltage (hereinafter referred to as a first phase voltage) for a certain phase in the first system is as indicated in FIG. **7**A, a current that flows through the stray capacitance C**1** (see FIG. **3**), which is present between the first motor coil **18**A and the frame ground, because of the first phase voltage is as indicated in FIG. **7**C. That is, a current in the − direction flows through the stray capacitance C**1** at a time of fall t**1** of the first phase voltage, and a current in the + direction flows through the stray capacitance C**1** at a time of rise t**2** of the first phase voltage.

If the waveform of an output voltage (hereinafter referred to as a second phase voltage) for a certain phase in the second system is a waveform obtained by inverting the waveform of the first phase voltage in FIG. **7**A as indicated in FIG. **7**B, a current that flows through the stray capacitance C**2** (see FIG. **3**), which is present between the second motor coil **18**B and the frame ground, because of the second phase voltage is as indicated in FIG. **7**D. That is, a current in the + direction flows through the stray capacitance C**2** at a time of rise t**1** of the second phase voltage, and a current in the − direction flows through the stray capacitance C**2** at a time of fall t**2** of the second phase voltage. Thus, the current which flows through the stray capacitance C**1** because of the first phase voltage and the current which flows through the stray capacitance C**1** because of the second phase voltage cancel out each other at each of time t**1** and time t**2**. Therefore, as indicated in FIG. **7**E, the currents which flow through the stray capacitances C**3** and C**4** (see FIG. **3**), which are present between the positive and negative power source lines and the frame ground, respectively, are reduced.

FIG. **8** illustrates an equivalent circuit that places a focus on common mode noise currents. The first phase voltage and the second phase voltage can be considered as noise generation sources. The positive and negative electrodes of the power source **100** can be considered as being short-circuited for alternating currents such as the common mode noise currents. In FIG. **8**, common mode noise currents due to the first phase voltage flow as indicated by the continuous arrows. Common mode noise currents due to the second phase voltage flow as indicated by the long dashed short dashed arrows. Thus, the common mode noise currents which flow through each of the stray capacitances C**3** and C**4** are opposite in direction to each other, and thus cancel out each other. As a result, the total of the common mode noise currents is reduced.

The common mode noise reduction section **42** changes the PWM count in a PWM cycle for at least one phase in one of the two systems such that a current that flows through a stray capacitance because of an output voltage for one phase in the other system is canceled out with a current that flows through the stray capacitance because of an output voltage for one phase in the one system in at least one PWM cycle in a current control cycle.

In the embodiment, the common mode noise reduction section **42** changes the PWM counts in a PWM cycle for two phases in one of the two systems such that a current that flows through a stray capacitance because of an output voltage for one phase in the other system is canceled out with a current that flows through the stray capacitance because of one of output voltages for two phases in the one system in each PWM cycle in a current control cycle.

FIG. **9** is a flowchart illustrating an example of operation of the common mode noise reduction section.

The common mode noise reduction section **42** (see FIG. **2**) first sets the first U-phase, V-phase, and W-phase PWM counts Cu_1, Cv_1, and Cw_1 for the next current control cycle Ta, which are provided from the first PWM duty computation section **57**A (see FIG. **4**), as the first U-phase, V-phase, and W-phase PWM counts Cu_1, Cv_1, and Cw_1 for each PWM cycle Tc in the next current control cycle Ta (step S**1**).

Similarly, the common mode noise reduction section **42** sets the second U-phase, V-phase, and W-phase PWM counts Cu_2, Cv_2, and Cw_2 for the next current control cycle Ta, which are provided from the second PWM duty computation section **57**B, as the second U-phase, V-phase, and W-phase PWM counts Cu_2, Cv_2, and Cw_2 for each PWM cycle Tc in the next current control cycle Ta (step S**2**).

FIG. **12**A is a schematic table illustrating an example of the first U-phase, V-phase, and W-phase PWM counts Cu_1, Cv_1, and Cw_1 for each PWM cycle Tc in the current control cycle Ta, which are set in step S**1**, and the second U-phase, V-phase, and W-phase PWM counts Cu_2, Cv_2, and Cw_2 for each PWM cycle Tc in the current control cycle Ta, which are set in step S**2**. Next, the common mode noise reduction section **42** sets a switching timing determined in consideration of the dead time for each phase in each system (step S**3**).

FIGS. **10**A to **10**H are schematic charts mainly illustrating the relationship between the final PWM count in each PWM cycle for a certain phase and an upper FET command and a lower FET command for the relevant phase in each system. In other words, FIGS. **10**A to **10**H are schematic charts illustrating an example of operation of the first PWM output section **43**A and the second PWM output section **43**B (see FIG. **2**) for a certain phase. In the embodiment, as discussed earlier, the carrier waveform is a triangular waveform, and the value that can be output as the PWM count is set to 0 to 500. In the embodiment, the count value corresponding to the dead time is set to 10.

An upper FET command and a lower FET command for the first system will be described. In the embodiment, the switching timing of the upper FET in the first system is set such that the upper FET command for the first system is an off command when the carrier count is larger than the PWM count. That is, as indicated in FIG. **10**A, the upper FET command is varied from an on command to an off command when the carrier count becomes equal to the PWM count (time t**2**) while the carrier count is counting up. The upper FET command is varied from an off command to an on command when the carrier count becomes equal to the PWM count (time t**5**) while the carrier count is counting down.

As indicated in FIG. **10**B, when a dead time Td elapses (time t**3**) from time t**2**, the lower FET command is varied from an off command to an on command. The lower FET command is varied from an on command to an off command at the time (time t**4**) the dead time Td earlier than time t**5**. An upper FET command and a lower FET command for the second system will be described. In the embodiment, the switching timing of the upper FET in the second system is set such that the upper FET command for the second system is an on command when the carrier count is larger than the PWM count. That is, as indicated in FIG. **10**E, the upper FET command is varied from an off command to an on command when the carrier count becomes equal to the PWM count (time t**2**) while the carrier count is counting up. The upper FET command is varied from an on command to an off command when the carrier count becomes equal to the PWM count (time t**5**) while the carrier count is counting down.

As indicated in FIG. **10**F, the lower FET command is varied from an on command to an off command at the time (time t**1**) the dead time Td earlier than time t**2**. When the dead time Td elapses (time t**6**) from time t**5**, the lower FET command is varied from an off command to an on command. An output voltage (phase voltage) for a certain phase during a dead time period will be described with reference to FIGS. **11**A and **11**B. Here, U-phase in the first system will be described as an example. The same description also applies to the remaining two phases in the first system and the phases in the second system.

As illustrated in FIG. **11**A, in a state in which a current is flowing from the point of connection between the upper FET **111**A and the lower FET **112**A toward the electric motor **18**, a current flows through the diode **122**A, which is connected in inverse parallel with the lower FET **112**A, during a dead time period. Thus, the output voltage (phase voltage) Vu is at L level during the dead time period. Therefore, the period during which the phase voltage Vu is at L level is the same as an off period of the upper FET **111**A.

As illustrated in FIG. **11**B, in a state in which a current is flowing from the electric motor **18** toward the point of connection between the upper FET **111**A and the lower FET **112**A, on the other hand, a current flows through the diode **121**A, which is connected in inverse parallel with the upper FET **111**A, during a dead time period. Thus, the output voltage (phase voltage) Vu is at H level during the dead time period. Therefore, the period during which the phase voltage Vu is at L level is shorter than an off period of the upper FET **111**A. In other words, the period during which the phase voltage Vu is at H level is longer than an on period of the upper FET **111**A.

In the case where the PWM count is equal to or more than half the maximum value of the PWM count (equal to or more than 250) in the first system, the on time of the upper FET is longer than that for the case where the PWM count is less than half the maximum value of the PWM count. Thus, in the embodiment, for convenience of description, it is considered that a current is flowing from the point of connection between the upper FET and the lower FET toward the electric motor **18** (as illustrated in FIG. **11**A) in the case where the PWM count is equal to or more than 250. Therefore, it is considered that the output voltage (phase voltage) is at L level during a dead time period. Thus, in this case, it is considered that the phase voltage is varied as indicated in FIG. **10**C, and thus the level variation timing of the phase voltage and the switching timing of the upper FET coincide with each other.

In the case where the PWM count is less than half the maximum value of the PWM count (less than 250) in the first system, on the other hand, the on time of the upper FET is shorter than that for the case where the PWM count is equal to or more than half the maximum value of the PWM count. Thus, in the embodiment, for convenience of description, it is considered that a current is flowing from the electric motor **18** toward the point of connection between the upper FET and the lower FET (as illustrated in FIG. **11**B) in the case where the PWM count is less than 250. Therefore, it is considered that the output voltage (phase voltage) is at H level during a dead time period. Thus, in this case, it is considered that the phase voltage is varied as indicated in FIG. **10**D, and thus the level variation timing of the phase voltage and the switching timing of the upper FET do not coincide with each other. A virtual PWM count (switching timing determined in consideration of the dead time) at which the switching timing of the upper FET coincides with the level variation timing of the phase voltage has a value

obtained by adding a count value (in the embodiment, "10") corresponding to the dead time to the actual PWM count.

In the case where the PWM count is equal to or more than half the maximum value of the PWM count (equal to or more than 250) in the second system, the on time of the upper FET is shorter than that for the case where the PWM count is less than half the maximum value of the PWM count. Thus, in the embodiment, for convenience of description, it is considered that a current is flowing from the electric motor **18** toward the point of connection between the upper FET and the lower FET (as illustrated in FIG. **11**B) in the case where the PWM count is equal to or more than 250. Therefore, it is considered that the output voltage (phase voltage) is at H level during a dead time period. Thus, in this case, it is considered that the phase voltage is varied as indicated in FIG. **10**G and thus the level variation timing of the phase voltage and the switching timing of the upper FET do not coincide with each other. A virtual PWM count (switching timing determined in consideration of the dead time) at which the switching timing of the upper FET coincides with the level variation timing of the phase voltage has a value obtained by subtracting a count value (in the embodiment, "10") corresponding to the dead time from the actual PWM count.

In the case where the PWM count is less than half the maximum value of the PWM count (less than 250) in the second system, on the other hand, the on time of the upper FET is longer than that for the case where the PWM count is equal to or more than half the maximum value of the PWM count. Thus, in the embodiment, for convenience of description, it is considered that a current is flowing from the point of connection between the upper FET and the lower FET toward the electric motor **18** (as illustrated in FIG. **11**A) in the case where the PWM count is less than 250. Therefore, it is considered that the output voltage (phase voltage) is at L level during a dead time period. Thus, in this case, it is considered that the phase voltage is varied as indicated in FIG. **10**H, and thus the level variation timing of the phase voltage and the switching timing of the upper FET coincide with each other.

In the embodiment, for convenience of description, the direction of the phase current in the first system and the second system is estimated on the basis of whether or not the PWM count is equal to or more than half the maximum value of the PWM count. However, the direction of the phase current may be estimated on the basis of a detected value of the phase current. In step S**3**, for each PWM count in the PWM cycle Tc for each phase in each system set in steps S**1** and S**2**, the common mode noise reduction section **42** computes a PWM count (switching timing determined in consideration of the dead time) that coincides with the level variation timing of the output voltage (phase voltage) for the relevant phase.

Specifically, for a PWM count that is equal to or more than 250, of the first U-phase, V-phase, and W-phase PWM counts Cu_1, Cv_1, and Cw_1 for each PWM cycle Tc in the next current control cycle Ta, the common mode noise reduction section **42** sets the value of the PWM count, as it is, as the PWM count which coincides with the level variation timing of the output voltage (phase voltage) for the relevant phase. For a PWM count that is less than 250, of the first U-phase, V-phase, and W-phase PWM counts Cu_1, Cv_1, and Cw_1, the common mode noise reduction section **42** sets a value obtained by adding a count value (in the embodiment, "10") corresponding to the dead time to the value of the PWM count as the PWM count which coincides with the level variation timing of the output voltage (phase voltage) for the relevant phase.

For a PWM count that is equal to or more than 250, of the second U-phase, V-phase, and W-phase PWM counts Cu_2, Cv_2, and Cw_2 for each PWM cycle Tc in the next current control cycle Ta, the common mode noise reduction section **42** sets a value obtained by subtracting a count value (in the embodiment, "10") corresponding to the dead time from the value of the PWM count as the PWM count which coincides with the level variation timing of the output voltage (phase voltage) for the relevant phase.

For a PWM count that is less than 250, of the second U-phase, V-phase, and W-phase PWM counts Cu_2, Cv_2, and Cw_2, the common mode noise reduction section **42** sets the value of the PWM count, as it is, as the PWM count which coincides with the level variation timing of the output voltage (phase voltage) for the relevant phase. In the case where the PWM count in each PWM cycle for each phase in each system set in steps S**1** and S**2** is as indicated in FIG. **12**A, the PWM count in each PWM cycle for each phase in each system set in step S**3** is as indicated in FIG. **12**B. When FIGS. **12**A and **12**B are compared with each other, it is seen that the PWM count Cv_1 for V-phase in the first system is varied from 200 to 210, and that the PWM count Cw_1 for W-phase in the first system is varied from 100 to 110. It is also seen that the PWM count Cu_2 for U-phase in the second system is varied from 350 to 340, and that the PWM count Cv_2 for V-phase in the second system is varied from 300 to 290.

Next, the common mode noise reduction section **42** determines such a combination of phases in the first system and the second system that noise currents for the phases should cancel out each other, on the basis of the PWM count in each PWM cycle for each phase in each system, which is set in the processing in step S**3** (step S**4**). Specifically, the common mode noise reduction section **42** first sets as a first reference phase, of the phases in the systems, a phase that has a PWM count that is the closest to the maximum value (in the embodiment, "500") or the minimum value (in the embodiment, "0") of the PWM count, of the PWM counts which are set in the processing in step S**3**. In the example in FIG. **12**B, of the PWM counts for the phases in the systems, the PWM count Cw_2 (Cw_2=50) for W-phase in the second system is the closest to 500 or 0, and thus W-phase in the second system is set as the first reference phase.

Next, the common mode noise reduction section **42** assigns, of the phases in the different system (in the example, the first system) other than the system of the first reference phase (in the example, W-phase in the second system), two phases with PWM counts that are close to the PWM count (in the example, Cw_2) for the first reference phase as count change target phases with PWM counts to be changed in order to cancel out a noise current for the first reference phase. In the example in FIG. **12**B, for W-phase in the second system, which is the first reference phase, V-phase and W-phase in the first system are assigned as the count change target phases for canceling out a noise current for the first reference phase.

The common mode noise reduction section **42** also sets the remaining one phase (in the example, U-phase) in the system (in the example, the first system) to which the count change target phases, which are assigned for the first reference phase, belong as a second reference phase. The common mode noise reduction section **42** then assigns two of the phases in the different system (in the example, the second system) other than the system of the second reference phase

(in the example, U-phase in the first system) as count change target phases with PWM counts to be changed in order to cancel out a noise current for the second reference phase. For example, the common mode noise reduction section **42** assigns two phases (in the example, U-phase and V-phase) in the second system other than the first reference phase as the count change target phases for canceling out a noise current for the second reference phase.

Next, the common mode noise reduction section **42** sets an amplitude for canceling out a noise current for each count change target phase (step S**5**). In order to change a PWM count value for a certain count change target phase such that the total value of PWM count values in the current control cycle Ta is not changed, an amplitude that matches an amplitude pattern for A-phase indicated in FIG. **13**A or an amplitude that matches an amplitude pattern for B-phase indicated in FIG. **13**A, for example, may be added to the PWM count value for the relevant count change target phase. The symbol "x" in FIG. **13**A indicates an amplitude prescription value that prescribes the absolute value of the amplitude.

The amplitude pattern for A-phase is applied to one of the two count change target phases in the same system, and the amplitude pattern for B-phase is applied to the other. In the example, the amplitude pattern for A-phase is applied to V-phase in the first system, and the amplitude pattern for B-phase is applied to W-phase in the first system. In addition, the amplitude pattern for A-phase is applied to U-phase in the second system, and the amplitude pattern for B-phase is applied to V-phase in the second system.

The common mode noise reduction section **42** computes the amplitude prescription value x for each of V-phase in the first system, W-phase in the first system, U-phase in the second system, and V-phase in the second system on the basis of the PWM count in each PWM cycle for each phase in each system, which is set in the processing in step S**3**, as follows. The common mode noise reduction section **42** computes the absolute value of the difference between the PWM count for V-phase in the first system and the PWM count for W-phase in the second system, a noise current for which should be canceled out, as the amplitude prescription value x for V-phase in the first system. In the example, the amplitude prescription value x for V-phase in the first system is 160 (=210−50).

The common mode noise reduction section **42** computes the absolute value of the difference between the PWM count for W-phase in the first system and the PWM count for W-phase in the second system, a noise current for which should be canceled out, as the amplitude prescription value x for W-phase in the first system. In the example, the amplitude prescription value x for W-phase in the first system is 60 (=110−50).

The common mode noise reduction section **42** computes the absolute value of the difference between the PWM count for U-phase in the second system and the PWM count for U-phase in the first system, a noise current for which should be canceled out, as the amplitude prescription value x for U-phase in the second system. In the example, the amplitude prescription value x for U-phase in the second system is 60 (=400−340).

The common mode noise reduction section **42** computes the absolute value of the difference between the PWM count for V-phase in the second system and the PWM count for U-phase in the first system, a noise current for which should be canceled out, as the amplitude prescription value x for V-phase in the second system. In the example, the amplitude prescription value x for V-phase in the second system is 110 (=400−290). The common mode noise reduction section **42** sets an amplitude in each PWM cycle Tc for each count change target phase on the basis of the amplitude prescription value x for each count change target phase computed in this manner and the amplitude pattern which is applied to the relevant phase.

The amplitudes in each PWM cycle Tc for V-phase in the first system, W-phase in the first system, U-phase in the second system, and V-phase in the second system, which are set on the basis of the PWM count in each PWM cycle for each phase in each system which is indicated in FIG. **12**B, are indicated in FIG. **13**B. Next, the common mode noise reduction section **42** performs PWM count change processing for changing the PWM counts for the count change target phases (step S**6**). Specifically, the common mode noise reduction section **42** changes the PWM counts for the count change target phases in each PWM cycle Tc in the next current control cycle Ta, which are set in steps S**1** and S**2**, in accordance with the amplitude for each count change target phase, which is set in step S**5**.

More specifically, the common mode noise reduction section **42** adds, to the PWM counts for the count change target phases in each PWM cycle Tc, which are set in steps S**1** and S**2**, the amplitudes for the respective count change target phases, which are set in step S**5**. Consequently, the PWM counts for the count change target phases in each PWM cycle Tc are changed. Next, the common mode noise reduction section **42** provides the first PWM output section **43**A with the first U-phase, V-phase, and W-phase PWM counts Cu_1, Cv_1, and Cw_1 in each PWM cycle after the PWM count change processing in step S**6** as the final first U-phase, V-phase, and W-phase PWM counts Cu_1, Cv_1, and Cw_1 in each PWM cycle Tc in the next current control cycle Ta (step S**7**).

In addition, the common mode noise reduction section **42** provides the second PWM output section **43**B with the second U-phase, V-phase, and W-phase PWM counts Cu_2, Cv_2, and Cw_2 in each PWM cycle after the PWM count change processing in step S**5** as the final second U-phase, V-phase, and W-phase PWM counts Cu_2, Cv_2, and Cw_2 in each PWM cycle Tc in the next current control cycle Ta (step S**8**). The common mode noise reduction section **42** then ends the processing in the present current control cycle Ta.

In the case where the PWM count in each PWM cycle for each phase in each system, which is set in steps S**1** and S**2**, has a value indicated in FIG. **12**A and the amplitudes for the count change target phases have values indicated in FIG. **13**B, the final PWM count in each PWM cycle for each phase in each system is as indicated in FIG. **13**C. The switching timing (switching timing determined in consideration of the dead time) that coincides with an output voltage for each phase corresponding to the final PWM count, which is indicated in FIG. **13**C, is as indicated in FIG. **13**D. The PWM counts in each PWM cycle for the count change target phases in FIG. **13**D can be obtained by adding, to the PWM counts in each PWM cycle for the count change target phases which are set in step S**3**, the amplitudes for the respective count change target phases which are computed in step S**4**.

As indicated in FIG. **13**D, the PWM count for W-phase in the second system in each PWM cycle Tc coincides with the PWM count for either V-phase or W-phase in the first system. Therefore, the noise current which flows through the stray capacitance C**2** (see FIG. **3**) on the second motor coil **18**B side because of an output voltage (phase voltage) for W-phase in the second system is canceled out with the noise current which flows through the stray capacitance C**1** on the

first motor coil **18**A side because of an output voltage (phase voltage) for either V-phase or W-phase in the first system. Consequently, common mode noise is reduced.

Similarly, as indicated in FIG. **13**D, the PWM count for U-phase in the first system in each PWM cycle Tc coincides with the PWM count for either U-phase or V-phase in the second system. Therefore, the noise current which flows through C**3** and C**4** through the stray capacitance C**1** on the first motor coil **18**A side because of an output voltage (phase voltage) for U-phase in the first system is canceled out with the noise current which flows through C**3** and C**4** through the stray capacitance C**2** on the second motor coil **18**B side because of an output voltage (phase voltage) for either U-phase or V-phase in the second system. Consequently, common mode noise is reduced.

In the embodiment, the present invention is applied to a motor control device for an electric power steering system. However, the present invention is also applicable to a motor control device that is used for devices other than an electric power steering system. Besides, a variety of design changes may be made without departing from the scope described in the claims.

What is claimed is:

1. A motor control device that controls an electric motor that has two-system multi-phase motor coils, the motor control device comprising:

a pulse width modulation (PWM) count computation unit that computes a PWM count for each phase in each system in each current control cycle that includes a plurality of PWM cycles;

a PWM count setting unit that sets the PWM count for each phase in each system in a current control cycle as a PWM count in each PWM cycle in the current control cycle for a corresponding phase in a corresponding system; and

a common mode noise reduction unit that changes the PWM count in a PWM cycle for at least one phase in one of the two systems such that a current that flows through a stray capacitance because of an output voltage for one phase in another system is canceled out with a current that flows through the stray capacitance because of an output voltage for the at least one phase in the one system in at least one PWM cycle in the current control cycle, wherein

the common mode noise reduction unit includes a PWM count change unit that changes the PWM count for the at least one phase in the one system, of a PWM signal in each PWM cycle in the current control cycle for each phase in each system, such that an output voltage waveform for the at least one phase is a waveform obtained by inverting an output voltage waveform for the one phase in the other system in the at least one PWM cycle without changing a total value of PWM counts for the at least one phase in the current control cycle.

2. The motor control device according to claim **1**, wherein:

the common mode noise reduction unit changes PWM counts in a PWM cycle for second and third phases, which are two phases in the one system, such that a current that flows through a stray capacitance because of an output voltage for a first phase, which is one phase in the other system, is canceled out with a current that flows through the stray capacitance because of an output voltage for the second or third phase in each PWM cycle in the current control cycle; and

the common mode noise reduction unit includes

a first PWM count change unit that changes the PWM count for the second phase in each PWM cycle in the current control cycle such that an output voltage waveform for the second phase is a waveform obtained by inverting an output voltage waveform for the first phase in half the predetermined number of PWM cycles in the current control cycle without changing a total value of PWM counts for the second phase in the current control cycle, and

a second PWM count change unit that changes the PWM count for the third phase in each PWM cycle in the current control cycle such that an output voltage waveform for the third phase is a waveform obtained by inverting an output voltage waveform for the first phase in the other half of the predetermined number of PWM cycles in the current control cycle without changing a total value of PWM counts for the third phase in the current control cycle.

3. The motor control device according to claim **2**, further comprising:

a second common mode noise reduction unit that changes PWM counts in PWM cycles for fifth and sixth phases, which are two phases in the other system and are other than the first phase, such that a current that flows through a stray capacitance because of an output voltage for a fourth phase, which is one phase in the one system and is other than the second and third phases, is canceled out with a current that flows through the stray capacitance because of an output voltage for the fifth or sixth phase in each PWM cycle in the current control cycle, wherein

the second common mode noise reduction unit includes

a third PWM count change unit that changes the PWM count for the fifth phase in each PWM cycle in the current control cycle such that an output voltage waveform for the fifth phase is a waveform obtained by inverting an output voltage waveform for the fourth phase in half the predetermined number of PWM cycles in the current control cycle without changing a total value of PWM counts for the fifth phase in the current control cycle, and

a fourth PWM count change unit that changes the PWM count for the sixth phase in each PWM cycle in the current control cycle such that an output voltage waveform for the sixth phase is a waveform obtained by inverting an output voltage waveform for the fourth phase in the other half of the predetermined number of PWM cycles in the current control cycle without changing a total value of PWM counts for the sixth phase in the current control cycle.

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